# TPS27SA08-Q1 24-V, 10-A, Single-Channel Automotive Smart High Side Switch

## 1 Features

- Single-channel smart high-side switch with a typical 9-mΩ $R_{ON}$ ($T_J$ = 25°C)
- Intended for 24-V supply systems with 40-V load dump
- Improve reliability through overcurrent protection:
  - Current limit threshold nominally at 20 A
  - Current limiting (clamping) on reaching the threshold
- Qualified for automotive applications:
  - AEC Q-100 qualified
  - Device temperature grade 1: –40°C to +125°C ambient operating temperature range
  - Device HBM ESD classification level 2
  - Device CDM ESD classification level C4B
- Robust integrated output protection:
  - Integrated thermal protection
  - Protection against short to ground and supply
  - Automatic FET switch-on during reverse supply
  - Automatic shut off if loss of supply and ground occurs
  - Integrated output clamp to demagnetize inductive loads
  - Configurable fault handling
- Analog sense output can be configured to accurately measure:
  - Load current
  - Supply voltage
  - Device temperature
- Provides FLT indication back to MCU
  - Detection of open load in off-state and short-to-GND

## 2 Applications

- AC charging (pile) station
- DC charging (pile) station
- Power distribution switch
- Seat comfort module
- Powertrain heating elements
- Inductive loads

## 3 Description

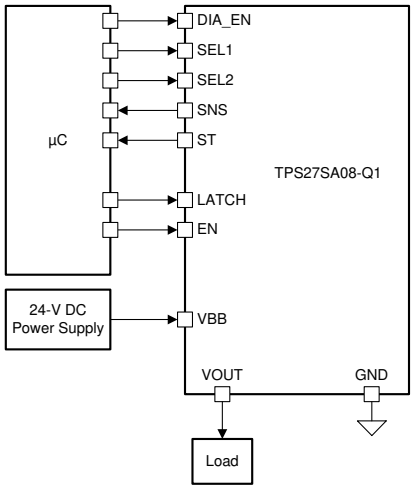
The TPS27SA08-Q1 device is a single-channel smart high-side switch intended for use with 24-V supply systems. The device integrates robust protection and diagnostic features to ensure output port protection even during harmful events like short circuits. The device protects against faults through a reliable current limit, which react to an overcurrent event by regulating the output current at the set point (nominally 20 A). The TPS27SA08-Q1 device also provides a high accuracy analog current sense that allows for improved diagnostics when driving varied load profiles. By reporting load current, device temperature, and supply voltage to a system MCU, the device enables predictive maintenance and load diagnostics that lengthen the system lifetime.

The TPS27SA08-Q1 device is available in a small 16-pin HTSSOP package which allows for reduced PCB footprint.

**Device Information**

| PART NUMBER | PACKAGE(1) | BODY SIZE (NOM) |
|---|---|---|
| TPS27SA08-Q1 | HTSSOP (16) | 5.00 mm × 4.40 mm |

(1) For all available packages, see the orderable addendum at the end of the data sheet.




**Simplified Schematic**

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## 4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

| DATE | REVISION | NOTES |
|---|---|---|
| December 2020 | * | Initial release. |

## 5 Device Summary Table

| Full Device Number | Current Limit ($I_{CL}$) | Overcurrent Behavior | Device Qualification |
|---|---|---|---|
| TPS27SA08C-Q1 | 20 A | Clamp Current at $I_{CL}$ until Thermal Shutdown | AEC Q-100 qualified |

# 6 Pin Configuration and Functions

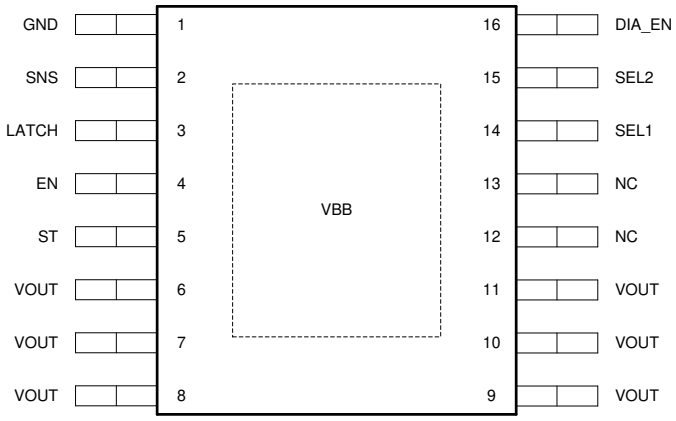



**Figure 6-1. PWP Package 16-Pin HTSSOP Top View**

**Table 6-1. Pin Functions**

| PIN | | I/O | DESCRIPTION |
|---|---|---|---|
| NO. | NAME | | |
| 1 | GND | — | Device ground |
| 2 | SNS | O | Sense output |
| 3 | LATCH | I | Sets fault handling behavior (latched or auto-retry) |
| 4 | EN | I | Switch control input, active high |
| 5 | $\overline{ST}$ | O | Switch diagnostic feedback, active low |
| 6, 7, 8, 9, 10, 11 | VOUT | O | Switch output |
| 12 | NC | -- | No Connect |
| 13 | NC | -- | No Connect |
| 14 | SEL1 | I | Diagnostics Select 1 |
| 15 | SEL2 | I | Diagnostics Select 2 |
| 16 | DIA_EN | I | Diagnostic enable, active high |
| Exposed pad | VBB | I | Power supply input |

## 6.1 Recommended Connections for Unused Pins

The TPS27SA08-Q1 device is designed to provide an enhanced set of diagnostic and protection features. However, if the system design only allows for a limited number of I/O connections, some pins may be considered as optional.

**Table 6-2. Connections for Optional Pins**

| PIN NAME | CONNECTION IF NOT USED | IMPACT IF NOT USED |
|---|---|---|
| SNS | Ground through 1-kΩ resistor | Analog sense is not available. |
| LATCH | Float or ground through $R_{PROT}$ resistor | With LATCH unused, the device will auto-retry after a fault. If latched behavior is desired it is possible to use one microcontroller output to control the latch function of several high-side channels. |
| $\overline{ST}$ | Float | All faults are indicated by the analog SNS pin. The $\overline{ST}$ pin provides the additional benefits:<br>• Provide fault indication when DIA_EN = 0<br>• Provide fault indication regardless of SELx pin conditions<br>• Provide fault indication to a simple digital I/O (rather than ADC or comparator used with the SNS signal) |
| SEL1 | Float or ground through $R_{PROT}$ resistor | SEL1 selects between the $V_{BB}$ and $T_J$ sensing features. With SEL1 unused, only load diagnostics are available. |
| SEL2 | Ground through $R_{PROT}$ resistor | With SEL2 = 0 V, $V_{BB}$ measurement diagnostics are not available. |
| DIA_EN | Float or ground through $R_{PROT}$ resistor | With DIA_EN unused, analog sense, open-load and short-to-supply diagnostics are not available. |

$R_{PROT}$ is used to protect the pins from excess current flow during reverse supply conditions, for more information please see the section on *Reverse Supply* protection.

# 7 Specifications

## 7.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

| | | | MIN | MAX | UNIT |
|---|---|---|---|---|---|
| $V_{BB}$ | Maximum continuous supply voltage | | | 36 | V |
| $V_{TR1}$ | Maxium supply voltage - long tranisent | Duration < 300 ms | | 40 | V |
| $V_{TR2}$ | Maxium transient voltage at the supply input | VBB to IC GND | | 54 | V |
| $V_{Rev}$ | Reverse supply voltage, $V_{REV}$ ≤ 3 minutes, with GND network. | | –36 | | V |
| $V_{EN}$ | Enable pin voltage | | –1 | 7 | V |
| $V_{LATCH}$ | LATCH pin voltage | | –1 | 7 | V |
| $V_{ST}$ | Status pin voltage | | –1 | 7(2) | V |
| $V_{DIA\_EN}$ | Diagnostic Enable pin voltage | | –1 | 7 | V |
| $V_{SNS}$ | Sense pin voltage | | –1 | 7 | V |
| $V_{SEL1}$, $V_{SEL2}$ | Select pin voltage | | –1 | 7 | V |
| $I_{GND}$ | Reverse ground current | $V_{BB}$ < 0 V | | –50 | mA |
| $T_J$ | Maximum junction temperature | | | 150 | °C |
| $T_{stg}$ | Storage temperature | | –65 | 150 | °C |

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

(2) These pins are adjacent to pins that will handle high-voltages. In the event of a pin-to-pin short, there will not be device damage.

## 7.2 ESD Ratings

| | | | | VALUE | UNIT |
|---|---|---|---|---|---|
| $V_{(ESD)}$ | Electrostatic discharge | Human-body model (HBM), per AEC Q100-002(1) | All pins except exposed pad and pins 6 to 11 | ±2000 | V |
| | | | Exposed pad and pins 6 to 11 | ±4000 | |
| | | Charged-device model (CDM), per AEC Q100-011 | All pins | ±750 | |
| $V_{(ESD1)}$ | Electrostatic discharge | Contact/Air discharge, per IEC 61000-4-2 (2) | VBB (exposed pad) and VOUT pins | ±8/±15 | kV |
| $V_{(surge)}$ | Transient surge | Surge protection with 42 Ω, per IEC 61000-4-5; 1.2/50 µs (2) | VBB (exposed pad) and VOUT pins | ±1000 | V |

(1) AEC Q100-002 indicates that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

(2) Tested with the application circuit and supply voltage of 24-V DC input.

## 7.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

| | | MIN | MAX | UNIT |
|---|---|---|---|---|
| $V_{BB}$ | Nominal supply voltage | 8 | 36 | V |
| $V_{EN}$ | Enable voltage | –1 | 5.5 | V |
| $V_{LATCH}$ | LATCH voltage | –1 | 5.5 | V |
| $V_{DIA\_EN}$ | Diagnostic enable voltage | –1 | 5.5 | V |
| $V_{SEL1}$, $V_{SEL2}$ | Select voltage | –1 | 5.5 | V |
| $V_{ST}$ | Status voltage | 0 | 5.5 | V |
| $V_{SNS}$ | Sense voltage | –1 | $V_{SNSclamp}$ | V |

## 7.3 Recommended Operating Conditions (continued)

over operating free-air temperature range (unless otherwise noted)

| | | | MIN | MAX | UNIT |
|---|---|---|---|---|---|
| $I_{MAX}$ | Continuous load current | $T_A$ = 70°C | 0 | 10 | A |

## 7.4 Thermal Information

| THERMAL METRIC(1) (2) | | TPS27SA08-Q1 PWP (HTSSOP) 16 PINS | UNIT |
|---|---|---|---|
| $R_{\theta JA}$ | Junction-to-ambient thermal resistance | 32.8 | °C/W |
| $R_{\theta JC(top)}$ | Junction-to-case (top) thermal resistance | 30.7 | °C/W |
| $R_{\theta JB}$ | Junction-to-board thermal resistance | 9.3 | °C/W |
| $\psi_{JT}$ | Junction-to-top characterization parameter | 2.6 | °C/W |
| $\psi_{JB}$ | Junction-to-board characterization parameter | 9.4 | °C/W |
| $R_{\theta JC(bot)}$ | Junction-to-case (bottom) thermal resistance | 1.0 | °C/W |

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report.
(2) The thermal parameters are based on a 4-layer PCB according to the JESD51-5 and JESD51-7 standards.

## 7.5 Electrical Characteristics

$V_{BB}$ = 8 V to 36 V, $T_J$ = –40°C to 125°C (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| **INPUT VOLTAGE AND CURRENT** | | | | | | |
| $V_{Clamp}$ | $V_{DS}$ clamp voltage | | 40 | | 58 | V |
| $V_{UVLOF}$ | $V_{BB}$ undervoltage lockout falling | | | 2.5 | 3 | V |
| $V_{UVLOR}$ | $V_{BB}$ undervoltage lockout rising | | | 2.5 | 3 | V |
| $I_{SB}$ | Standby current (includes MOSFET leakage) | $V_{BB}$ = 24 V, $T_J$ = 25°C<br>$V_{EN}$ = $V_{DIA\_EN}$ = 0 V, $V_{OUT}$ = 0 V | | | 0.8 | µA |
| | | $V_{BB}$ = 24 V, $T_J$ = 85°C<br>$V_{EN}$ = $V_{DIA\_EN}$ = 0 V, $V_{OUT}$ = 0 V | | | 1 | µA |
| | | $V_{BB}$ = 24 V, $T_J$ = 125°C,<br>$V_{EN}$ = $V_{DIA\_EN}$ = 0 V, $V_{OUT}$ = 0 V | | | 6 | µA |
| $I_{OUT\_OFF}$ | Output leakage current | $V_{BB}$ = 24 V, $T_J$ = 25°C<br>$V_{EN}$ = $V_{DIA\_EN}$ = 0 V, $V_{OUT}$ = 0 V | | 0.01 | 0.5 | µA |
| | | $V_{BB}$ = 24 V, $T_J$ = 125°C<br>$V_{EN}$ = $V_{DIA\_EN}$ = 0 V, $V_{OUT}$ = 0 V | | | 6 | µA |
| $I_{DIA}$ | Current consumption in diagnostic mode | $V_{BB}$ = 24 V, $I_{SNS}$ = 0 mA<br>$V_{EN}$ = 0 V, $V_{DIA\_EN}$ = 5 V, $V_{OUT}$ = 0 V | | 3 | 6 | mA |
| $I_Q$ | Quiescent current | $V_{BB}$ = 24 V<br>$V_{EN}$ = 5 V $V_{DIA\_EN}$ = 0 V, $I_{OUT}$ = 0 A, $V_{SELX}$ = 0 V | | 2.4 | 5.2 | mA |
| $t_{STBY}$ | Standby mode delay time | $V_{EN}$ = $V_{DIA\_EN}$ = 0 V to Standby | | 20 | | ms |
| **$R_{ON}$ CHARACTERISTICS** | | | | | | |
| $R_{ON}$ | On-resistance Includes MOSFET and package | $T_J$ = 25°C, 6 V ≤ $V_{BB}$ ≤ 36 V | | 9 | | mΩ |
| | | $T_J$ = 150°C, 6 V ≤ $V_{BB}$ ≤ 36 V | | | 20 | mΩ |
| | | $T_J$ = 25°C, 3 V ≤ $V_{BB}$ ≤ 6 V | | | 15 | mΩ |
| $R_{ON(REV)}$ | On-resistance during reverse polarity | $T_J$ = 25°C, -18 V ≤ $V_{BB}$ ≤ –8 V | | 9 | | mΩ |
| | | $T_J$ = 105°C, –18 V ≤ $V_{BB}$ ≤ –8 V | | | 20 | mΩ |
| **CURRENT SENSE CHARACTERISTICS** | | | | | | |

## 7.5 Electrical Characteristics (continued)

$V_{BB}$ = 8 V to 36 V, $T_J$ = –40°C to 125°C (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| $K_{SNS}$ | Current sense ratio $I_{OUT}$ / $I_{SNS}$ | | | | 4600 | | |
| $I_{SNSI}$ | Current sense current and current sense accuracy | $V_{EN}$ = $V_{DIA\_EN}$ = 5 V, $V_{SEL1}$ = $V_{SEL2}$ = 0 V | $I_{OUT}$ = 8 A | | 1.74 | | mA |
| $I_{SNSI}$ | Current sense current and current sense accuracy | $V_{EN}$ = $V_{DIA\_EN}$ = 5 V, $V_{SEL1}$ = $V_{SEL2}$ = 0 V | $I_{OUT}$ = 8 A | –5 | | 5 | % |
| $I_{SNSI}$ | Current sense current and current sense accuracy | $V_{EN}$ = $V_{DIA\_EN}$ = 5 V, $V_{SEL1}$ = $V_{SEL2}$ = 0 V | $I_{OUT}$ = 3 A | | 0.65 | | mA |
| $I_{SNSI}$ | Current sense current and current sense accuracy | $V_{EN}$ = $V_{DIA\_EN}$ = 5 V, $V_{SEL1}$ = $V_{SEL2}$ = 0 V | $I_{OUT}$ = 3 A | –5 | | 5 | % |
| $I_{SNSI}$ | Current sense current and current sense accuracy | $V_{EN}$ = $V_{DIA\_EN}$ = 5 V, $V_{SEL1}$ = $V_{SEL2}$ = 0 V | $I_{OUT}$ = 780 mA | | 0.217 | | mA |
| $I_{SNSI}$ | Current sense current and current sense accuracy | $V_{EN}$ = $V_{DIA\_EN}$ = 5 V, $V_{SEL1}$ = $V_{SEL2}$ = 0 V | $I_{OUT}$ = 780 mA | –5 | | 5 | % |
| $I_{SNSI}$ | Current sense current and current sense accuracy | $V_{EN}$ = $V_{DIA\_EN}$ = 5 V, $V_{SEL1}$ = $V_{SEL2}$ = 0 V | $I_{OUT}$ = 300 mA | | 0.065 | | mA |
| $I_{SNSI}$ | Current sense current and current sense accuracy | $V_{EN}$ = $V_{DIA\_EN}$ = 5 V, $V_{SEL1}$ = $V_{SEL2}$ = 0 V | $I_{OUT}$ = 300 mA | –12 | | 12 | % |
| $I_{SNSI}$ | Current sense current and current sense accuracy | $V_{EN}$ = $V_{DIA\_EN}$ = 5 V, $V_{SEL1}$ = $V_{SEL2}$ = 0 V | $I_{OUT}$ = 100 mA | | 0.022 | | mA |
| $I_{SNSI}$ | Current sense current and current sense accuracy | $V_{EN}$ = $V_{DIA\_EN}$ = 5 V, $V_{SEL1}$ = $V_{SEL2}$ = 0 V | $I_{OUT}$ = 100 mA | –42 | | 42 | % |
| **$T_J$ SENSE CHARACTERISTICS** | | | | | | | |
| $I_{SNST}$ | Temperature sense current | $V_{DIA\_EN}$ = 5 V, $V_{SEL1}$ = 5 V, $V_{SEL2}$ = 0 V | $T_J$ = –40°C | | 0.12 | | mA |
| | | | $T_J$ = 25°C | | 0.85 | | mA |
| | | | $T_J$ = 85°C | | 1.52 | | mA |
| | | | $T_J$ = 150°C | | 2.25 | | mA |
| $dI_{SNST}/dT$ | Coefficient | | | | 0.0112 | | mA/°C |
| **$V_{BB}$ SENSE CHARACTERISTICS** | | | | | | | |
| $I_{SNSV}$ | Voltage sense current | $V_{DIA\_EN}$ = 5 V, $V_{SEL1}$ = 5 V, $V_{SEL2}$ = 5 V | $V_{BB}$ = 3 V | | 0.26 | | mA |
| | | | $V_{BB}$ = 8 V | | 0.69 | | mA |
| | | | $V_{BB}$ = 13.5 V | | 1.17 | | mA |
| | | | $V_{BB}$ = 18 V | | 1.56 | | mA |
| | | | $V_{BB}$ = 28 V | | 2.43 | | mA |
| $dI_{SNSV}/dV$ | Coefficient | | | | 0.0867 | | mA/V |
| **SNS CHARACTERISTICS** | | | | | | | |
| $I_{SNSFH}$ | $I_{SNS}$ fault high level | $V_{DIA\_EN}$ = 5 V, $V_{SEL1}$ = 0 V, $V_{SEL2}$ = 0 | | 6 | 6.9 | 7.6 | mA |
| $I_{SNSleak}$ | $I_{SNS}$ leakage | $V_{DIA\_EN}$ = 0 V | | 0 | | 1 | µA |
| $V_{SNSclamp}$ | $V_{SNS}$ clamp | | | | 5.9 | | V |
| $I_{CL}$ | Current threshold at which current limit loop engages | | $T_J$ = –40°C | 17 | 22.2 | 27.8 | A |
| $I_{CL}$ | Current threshold at which current limit loop engages | | $T_J$ = 25°C | 15 | 20 | 25 | A |
| $I_{CL\_REG}$ | Current limit regulation level | | $T_J$ = 25°C | | 24 | | A |
| $I_{CL}$ | Current threshold at which current limit loop engages | | $T_J$ = 125°C | 12.8 | 16 | 20 | A |
| **CURRENT LIMIT CHARACTERISTICS** | | | | | | | |
| **FAULT CHARACTERISTICS** | | | | | | | |
| $V_{OL}$ | Open-load detection voltage | $V_{EN}$ = 0 V, $V_{DIA\_EN}$ = 5 V | | 2 | 2.5 | 4 | V |

## 7.5 Electrical Characteristics (continued)

$V_{BB}$ = 8 V to 36 V, $T_J$ = –40°C to 125°C (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| $t_{OL1}$ | OL and STB indication time - switch disabled | From falling edge of EN<br>$V_{EN}$= 5 V to 0 V, $V_{DIA\_EN}$ = 5 V, $V_{SELx}$ = 00<br>$I_{OUT}$ = 0 mA, $V_{OUT}$ = 4 V | 300 | 500 | 700 | µs |
| $t_{OL2}$ | OL and STB indication time - switch disabled | From rising edge of DIA_EN<br>$V_{EN}$ = 0 V, $V_{DIA\_EN}$ = 0 V to 5 V, $V_{SELx}$ = 00<br>$I_{OUT}$ = 0 mA, $V_{OUT}$ = 4 V | | | 50 | µs |
| $t_{OL3}$ | OL and STB indication time - switch disabled | From rising edge of VOUT<br>$V_{EN}$ = 0 V, $V_{DIA\_EN}$ = 5 V, $V_{SELx}$ = 00<br>$I_{OUT}$ = 0 mA, $V_{OUT}$ = 0 V to 4 V | | | 50 | µs |
| $T_{ABS}$ | Thermal shutdown | | 160 | | | °C |
| $T_{HYS}$ | Thermal shutdown hysteresis | | | 20 | | °C |
| $t_{RETRY}$ | Retry time | Minimum time from fault shutdown to switch re-enable (for thermal shutdown, current limit, and energy limit) | 1 | 2 | 3 | ms |
| **EN PIN CHARACTERISTICS**(1) | | | | | | |
| $V_{IL, EN}$ | Input voltage low level | | | | 0.8 | V |
| $V_{IH, EN}$ | Input voltage high level | No GND network Diode | 2 | | | V |
| $V_{IHYS, EN}$ | Input voltage hysteresis | No GND network Diode | | 250 | | mV |
| $I_{IL, EN}$ | Input current low level | $V_{EN}$ = 0.8 V | | 0.8 | | µA |
| $I_{IH, EN}$ | Input current high level | $V_{EN}$ = 2.0 V | | 2 | | µA |
| $R_{EN}$ | Internal pulldown resistor | | | 1 | | MΩ |
| **DIA_EN PIN CHARACTERISTICS** (1) | | | | | | |
| $V_{IL, DIA\_EN}$ | Input voltage low level | No GND network Diode | | | 0.8 | V |
| $V_{IH, DIA\_EN}$ | Input voltage high level | No GND network Diode | 2 | | | V |
| $V_{IHYS, DIA\_EN}$ | Input voltage hysteresis | | | 250 | | mV |
| $I_{IL, DIA\_EN}$ | Input current low level | $V_{DIA\_EN}$ = 0.8 V | | 0.8 | | µA |
| $I_{IH, DIA\_EN}$ | Input current high level | $V_{DIA\_EN}$ = 2.0 V | | 2 | | µA |
| $R_{DIA\_EN}$ | Internal pulldown resistor | | | 1 | | MΩ |
| **SEL1 AND SEL2 PIN CHARACTERISTICS** (1) | | | | | | |
| $V_{IL, SELx}$ | Input voltage low level | No GND network Diode | | | 0.8 | V |
| $V_{IH, SELx}$ | Input voltage high level | | 2 | | | V |
| $V_{IHYS, SELx}$ | Input voltage hysteresis | | | 250 | | mV |
| $I_{IL, SELx}$ | Input current low level | $V_{SELx}$ = 0.8 V | | 0.8 | | µA |
| $I_{IH, SELx}$ | Input current high level | $V_{SELx}$ = 2.0 V | | 2 | | µA |
| $R_{SELx}$ | Internal pulldown resistor | | | 1 | | MΩ |
| **LATCH PIN CHARACTERISTICS** (1) | | | | | | |
| $V_{IL, LATCH}$ | Input voltage low level | No GND network Diode | | | 0.8 | V |
| $V_{IH, LATCH}$ | Input voltage high level | No GND network Diode | 2 | | | V |
| $V_{IHYS, LATCH}$ | Input voltage hysteresis | | | 250 | | mV |
| $I_{IL, LATCH}$ | Input current low level | $V_{LATCH}$ = 0.8 V | | 0.8 | | µA |
| $I_{IH, LATCH}$ | Input current high level | $V_{LATCH}$ = 2.0 V | | 2 | | µA |
| $R_{LATCH}$ | Internal pulldown resistor | | | 1 | | MΩ |
| **$\overline{ST}$ PIN CHARACTERISTICS** (1) | | | | | | |
| $V_{OL, ST}$ | Output voltage low level | $I_{ST}$ = 1 mA | | | 0.4 | V |

## 7.5 Electrical Characteristics (continued)

$V_{BB}$ = 8 V to 36 V, $T_J$ = –40°C to 125°C (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| $I_{STleak}$ | Leakage current | $V_{ST}$ = 5 V | | | 2 | µA |

(1) $V_{BB}$ = 3 to 28 V

## 7.6 Switching Characteristics

$V_{BB}$ = 36 V, $T_J$ = –40°C to 150°C (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| $t_{DR}$ | Turn-on delay time | $V_{BB}$ = 24 V, $R_L$ = 8 Ω | 20 | 70 | 100 | µs |
| $t_{DF}$ | Turn-off delay time | $V_{BB}$ = 24 V, $R_L$ = 8 Ω | 20 | 50 | 125 | µs |
| $SR_R$ | VOUT rising slew rate | $V_{BB}$ = 24 V, 20% to 80% of $V_{OUT}$, $R_L$ = 8 Ω | 0.1 | 0.35 | 0.8 | V/µs |
| $SR_F$ | VOUT falling slew rate | $V_{BB}$ = 24 V, 80% to 20% of $V_{OUT}$, $R_L$ = 8 Ω | 0.2 | 0.5 | 0.9 | V/µs |
| $t_{ON}$ | Turn-on time | $V_{BB}$ = 24 V, $R_L$ = 8 Ω | 39 | 100 | 180 | µs |
| $t_{OFF}$ | Turn-off time | $V_{BB}$ = 24 V, $R_L$ = 8 Ω | 39 | 90 | 180 | µs |
| $t_{ON}$ - $t_{OFF}$ | Turn-on and off matching | 200-µs enable pulse | –80 | 0 | 80 | µs |
| $E_{ON}$ | Switching energy losses during turn-on | $V_{BB}$ = 24 V, $R_L$ = 8 Ω | | 0.4 | | mJ |
| $E_{OFF}$ | Switching energy losses during turn-off | $V_{BB}$ = 24 V, $R_L$ = 8 Ω | | 0.4 | | mJ |

## 7.7 SNS Timing Characteristics

$V_{BB}$ = 8 to 36 V, $T_J$ = –40°C to 150°C (unless otherwise noted)

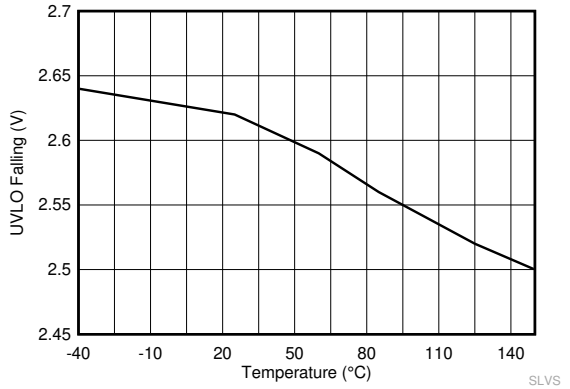
| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| **SNS TIMING - CURRENT SENSE** | | | | | | |
| $t_{SNSION1}$ | Settling time from rising edge of DIA_EN | $V_{EN}$ = 5 V, $V_{DIA\_EN}$ = 0 V to 5 V<br>$R_{SNS}$ = 1 kΩ, $R_L$ = 2.6 Ω | | | 40 | µs |
| $t_{SNSION2}$ | Settling time from rising edge of EN | $V_{EN}$ = $V_{DIA\_EN}$ = 0 V to 5 V<br>$R_{SNS}$ = 1 kΩ, $R_L$ = 2.6 Ω | | | 180 | µs |
| $t_{SNSION3}$ | Settling time from rising edge of EN | $V_{EN}$ = 0 V to 5 V, $V_{DIA\_EN}$ = 5 V<br>$R_{SNS}$ = 1 kΩ, $R_L$ = 2.6 Ω | | | 180 | µs |
| $t_{SNSIOFF1}$ | Settling time from falling edge of DIA_EN | $V_{EN}$ = 5 V, $V_{DIA\_EN}$ = 5 V to 0 V<br>$R_{SNS}$ = 1 kΩ, $R_L$ = 2.6 Ω | | | 20 | µs |
| $t_{SETTLEH}$ | Settling time from rising edge of load step | $V_{EN}$ = 5 V, $V_{DIA\_EN}$ = 5 V<br>$R_{SNS}$ = 1 kΩ, $I_{OUT}$ = 1 A to 5 A | | | 20 | µs |
| $t_{SETTLEL}$ | Settling time from falling edge of load step | $V_{EN}$ = 5 V, $V_{DIA\_EN}$ = 5 V<br>$R_{SNS}$ = 1 kΩ, $I_{OUT}$ = 5 A to 1 A | | | 20 | µs |
| **SNS TIMING - TEMPERATURE SENSE** | | | | | | |
| $t_{SNSTON1}$ | Settling time from rising edge of DIA_EN | $V_{EN}$ = 5 V, $V_{DIA\_EN}$ = 0 V to 5 V<br>$R_{SNS}$ = 1 kΩ | | | 40 | µs |
| $t_{SNSTON2}$ | Settling time from rising edge of DIA_EN | $V_{EN}$ = 0 V, $_{VDIA\_EN}$ = 0 V to 5 V<br>$R_{SNS}$ = 1 kΩ | | | 70 | µs |
| $t_{SNSTOFF}$ | Settling time from falling edge of DIA_EN | $V_{EN}$ = X, $V_{DIA\_EN}$ = 5 V to 0 V<br>$R_{SNS}$ = 1 kΩ | | | 20 | µs |
| **SNS TIMING - VOLTAGE SENSE** | | | | | | |
| $t_{SNSVON1}$ | Settling time from rising edge of DIA_EN | $V_{EN}$ = 5 V, $V_{DIA\_EN}$ = 0 V to 5 V<br>$R_{SNS}$ = 1 kΩ | | | 40 | µs |
| $t_{SNSVON2}$ | Settling time from rising edge of DIA_EN | $V_{EN}$ = 0 V, $V_{DIA\_EN}$ = 0 V to 5 V<br>$R_{SNS}$ = 1 kΩ | | | 70 | µs |

## 7.7 SNS Timing Characteristics (continued)

$V_{BB}$ = 8 to 36 V, $T_J$ = –40°C to 150°C (unless otherwise noted)

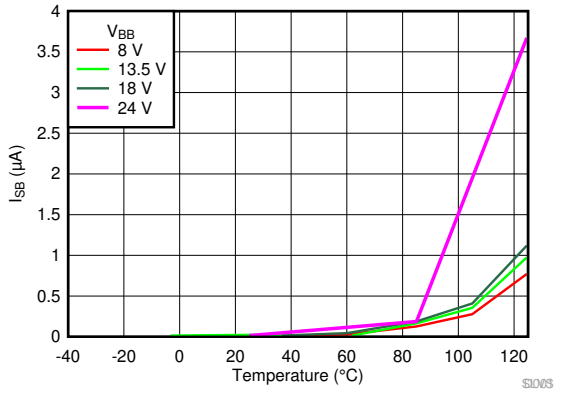
| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| $t_{SNSVOFF}$ | Settling time from falling edge of DIA_EN | $V_{EN}$ = X, $V_{DIA\_EN}$ = 5 V to 0 V<br>$R_{SNS}$ = 1 kΩ | | | 20 | µs |
| **SNS TIMING - MULTIPLEXER** | | | | | | |
| $t_{MUX}$ | Settling time from temperature sense to current sense | $V_{EN}$= X, $V_{DIA\_EN}$ = 5 V<br>$V_{SEL1}$ = 5 V to 0 V, $V_{SEL2}$ = 0 V<br>$R_{SNS}$ = 1 kΩ, $R_L$ = 2.6 Ω | | | 60 | µs |
| | Settling time from temperature sense to voltage sense | $V_{EN}$ = X, $V_{DIA\_EN}$ = 5 V<br>$V_{SEL1}$ = 5 V, $V_{SEL2}$ = 0 V to 5 V<br>$R_{SNS}$ = 1 kΩ | | | 60 | µs |
| | Settling time from voltage sense to temperature sense | $V_{EN}$ = X, $V_{DIA\_EN}$ = 5 V<br>$V_{SEL1}$ = 5 V, $V_{SEL2}$ = 5 V to 0 V<br>$R_{SNS}$ = 1 kΩ | | | 60 | µs |
| | Settling time from voltage sense to current sense | $V_{EN}$ = X, $V_{DIA\_EN}$ = 5 V<br>$V_{SEL1}$ = $V_{SEL2}$ = 5 V to 0 V,<br>$R_{SNS}$ = 1 kΩ, $R_L$ = 2.6 Ω | | | 60 | µs |
| | Settling time from current sense to temperature sense | $V_{EN}$ = X, $V_{DIA\_EN}$ = 5 V<br>$V_{SEL1}$ = 0 V to 5 V, $V_{SEL2}$ = 0 V<br>$R_{SNS}$ = 1 kΩ, $R_L$ = 2.6 Ω | | | 60 | µs |
| | Settling time from current sense to voltage sense | $V_{EN}$ = X, $V_{DIA\_EN}$ = 5 V<br>$V_{SEL1}$ = $V_{SEL2}$ = 0 V to 5 V<br>$R_{SNS}$ = 1 kΩ, $R_L$ = 2.6 Ω | | | 60 | µs |

## 7.8 Typical Characteristics




$V_{BB}$ = 13.5 V to 0 V  $R_{OUT}$ = 1 kΩ  $V_{DIAG\_EN}$ = 0 V
$V_{EN}$ = 5 V

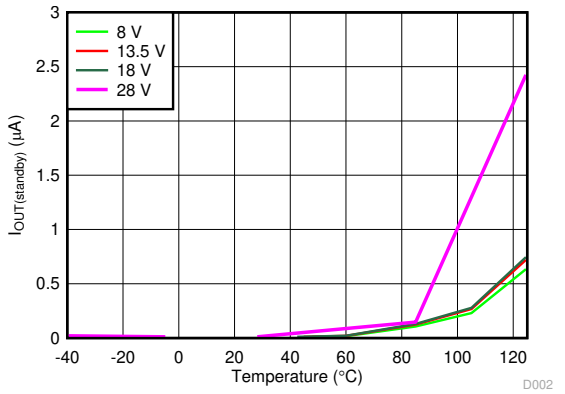
**Figure 7-1. Falling Undervoltage Lockout ($V_{UVLOF}$) vs Temperature**




$V_{OUT}$ = 0 V  $V_{EN}$ = 0 V  $V_{DIAG\_EN}$ = 0 V

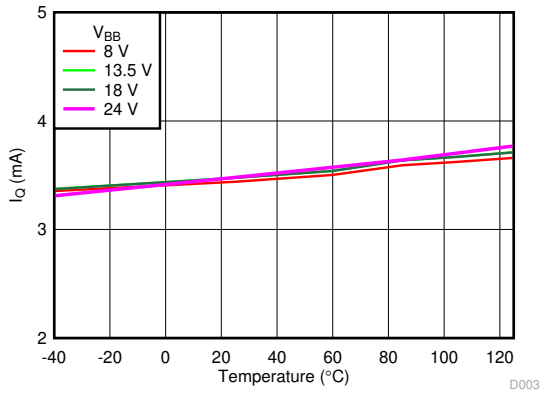
**Figure 7-2. Standby Current ($I_{SB}$) vs Temperature**

## 7.8 Typical Characteristics (continued)



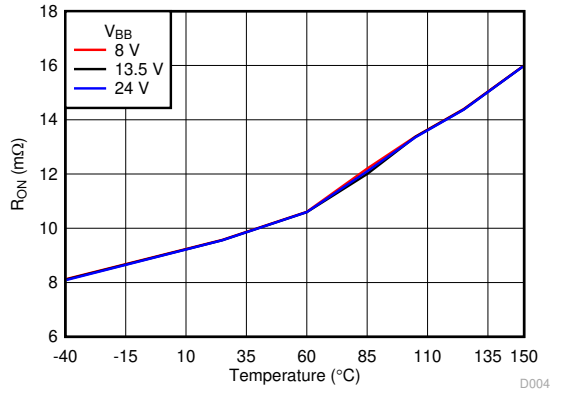

$V_{OUT}$ = 0 V $V_{EN}$ = 0 V $V_{DIAG\_EN}$ = 0 V

**Figure 7-3. Output Leakage Current ($I_{OUT(standby)}$) vs Temperature**



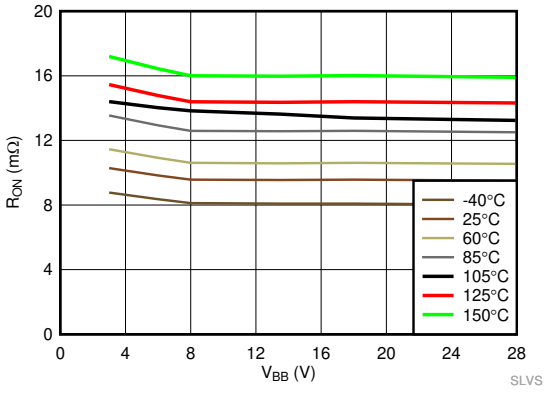

$I_{OUT}$ = 0 A $V_{EN}$ = 5 V $V_{DIAG\_EN}$ = 5 V
$R_{SNS}$ = 1 kΩ $V_{SEL1}$ = $V_{SEL2}$ = 0 V

**Figure 7-4. Quiescent Current ($I_Q$) vs Temperature**



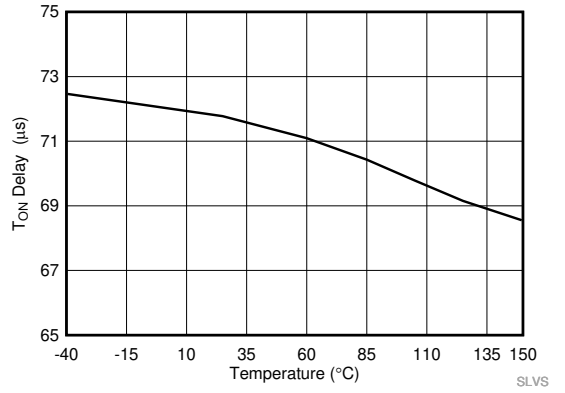

$I_{OUT}$ = 200 mA $V_{EN}$ = 5 V $V_{DIAG\_EN}$ = 0 V
$R_{SNS}$ = 1 kΩ

**Figure 7-5. On Resistance ($R_{ON}$) vs Temperature**



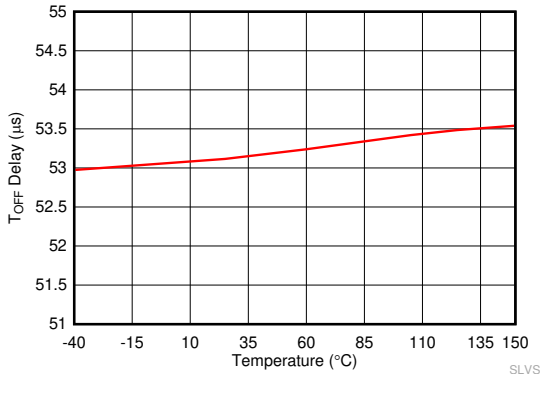

$I_{OUT}$ = 200 mA $V_{EN}$ = 5 V $V_{DIAG\_EN}$ = 0 V
$R_{SNS}$ = 1 kΩ $V_{BB}$ = 13.5 V

**Figure 7-6. On Resistance ($R_{ON}$) vs $V_{BB}$**




$R_{OUT}$ = 2.6 Ω $V_{EN}$ = 0 V to 5 V $V_{DIAG\_EN}$ = 0 V
$R_{SNS}$ = 1 kΩ $V_{BB}$ = 13.5 V

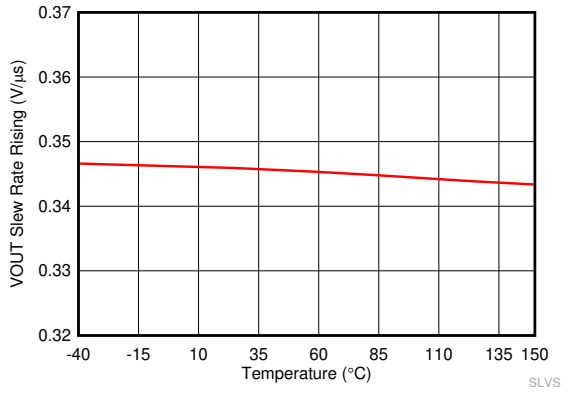
**Figure 7-7. Turn-on Delay Time ($t_{DR}$) vs Temperature**




$R_{OUT}$ = 2.6 Ω $V_{EN}$ = 5 V to 0 V $V_{DIAG\_EN}$ = 0 V
$R_{SNS}$ = 1 kΩ $V_{BB}$ = 13.5 V

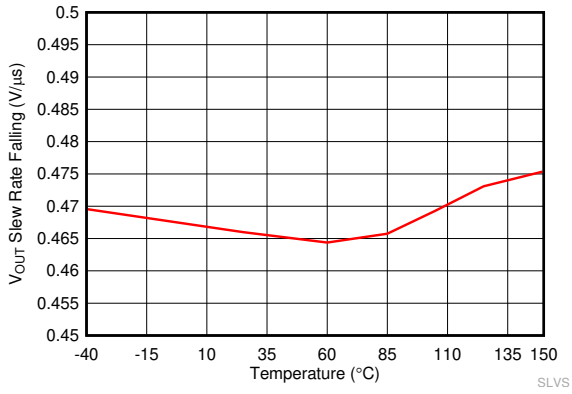
**Figure 7-8. Turn-off Delay Time ($t_{DF}$) vs Temperature**

## 7.8 Typical Characteristics (continued)



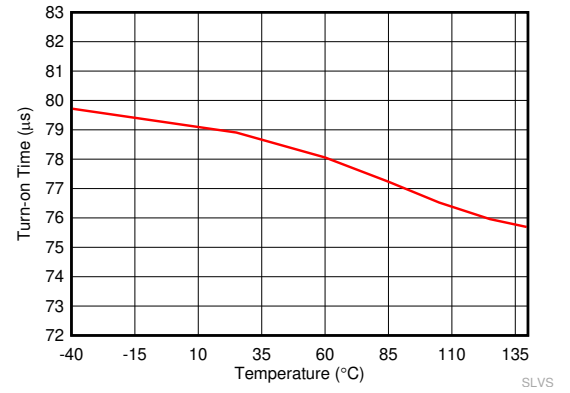

$R_{OUT}$ = 2.6 Ω $V_{EN}$ = 0 V to 5 V $V_{DIAG\_EN}$ = 0 V
$R_{SNS}$ = 1 kΩ $V_{BB}$ = 13.5 V

**Figure 7-9. $V_{OUT}$ Slew Rate Rising ($SR_R$) vs Temperature**



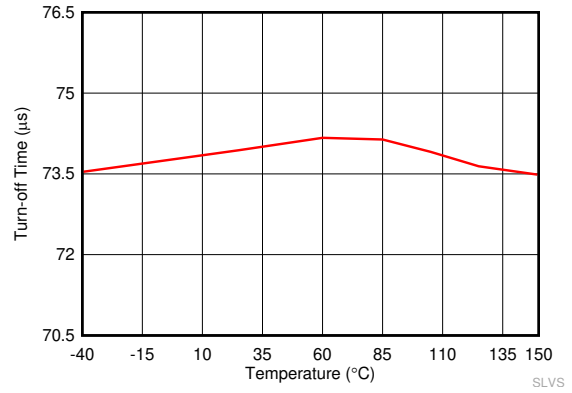

$R_{OUT}$ = 2.6 Ω $V_{EN}$ = 5 V to 0 V $V_{DIAG\_EN}$ = 0 V
$R_{SNS}$ = 1 kΩ $V_{BB}$ = 13.5 V

**Figure 7-10. $V_{OUT}$ Slew Rate Falling ($SR_F$) vs Temperature**



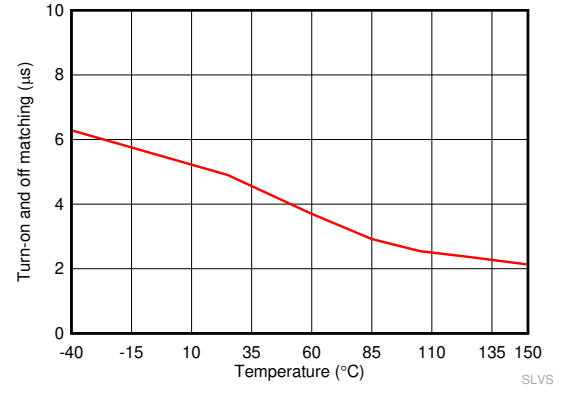

$R_{OUT}$ = 2.6 Ω $V_{EN}$ = 0 V to 5 V $V_{DIAG\_EN}$ = 0 V
$R_{SNS}$ = 1 kΩ $V_{BB}$ = 13.5 V

**Figure 7-11. Turn-on Time ($t_{ON}$) vs Temperature**



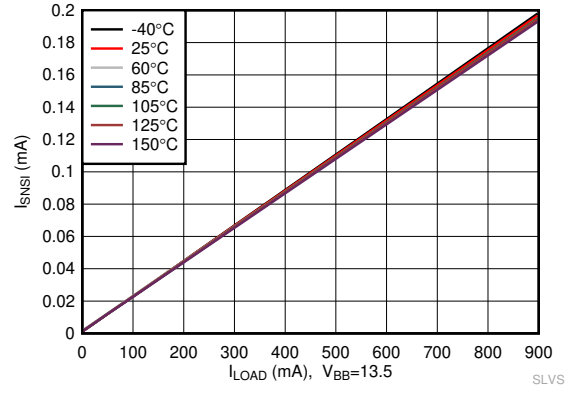

$R_{OUT}$ = 2.6 Ω $V_{EN}$ = 5 V to 0 V $V_{DIAG\_EN}$ = 0 V
$R_{SNS}$ = 1 kΩ $V_{BB}$ = 13.5 V

**Figure 7-12. Turn-off Time ($t_{OFF}$) vs Temperature**




$R_{OUT}$ = 2.6 Ω $V_{EN}$ = 0 V to 5 V and 5 V to 0 V $V_{DIAG\_EN}$ = 0 V
$R_{SNS}$ = 1 kΩ $V_{BB}$ = 13.5 V

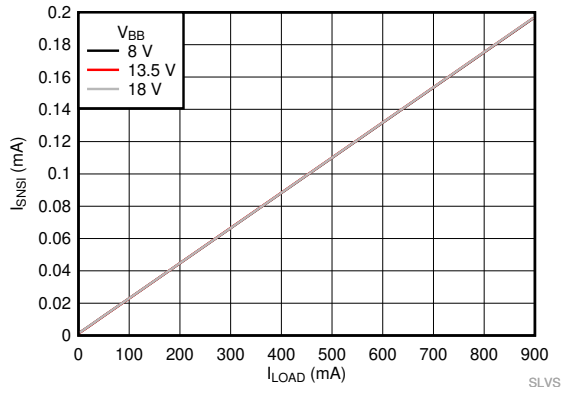
**Figure 7-13. Turn-on and Turn-off Matching ($t_{ON}$ - $t_{OFF}$) vs Temperature**




$V_{SEL1}$ = $V_{SEL2}$ = 0 V $V_{EN}$ = 5 V $V_{DIAG\_EN}$ = 5 V
$R_{SNS}$ = 1 kΩ $V_{BB}$ = 13.5 V

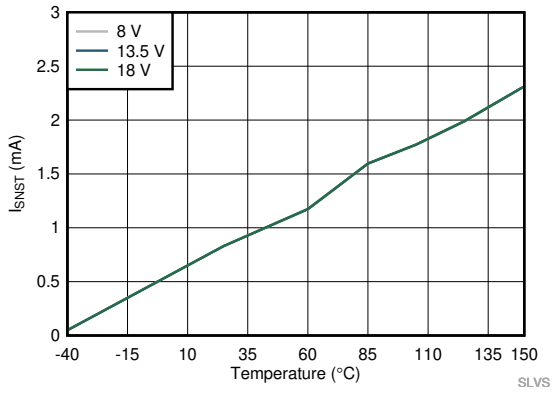
**Figure 7-14. Current Sense Output Current ($I_{SNSI}$ ) vs Load Current ($I_{OUT}$) across Temperature**

## 7.8 Typical Characteristics (continued)



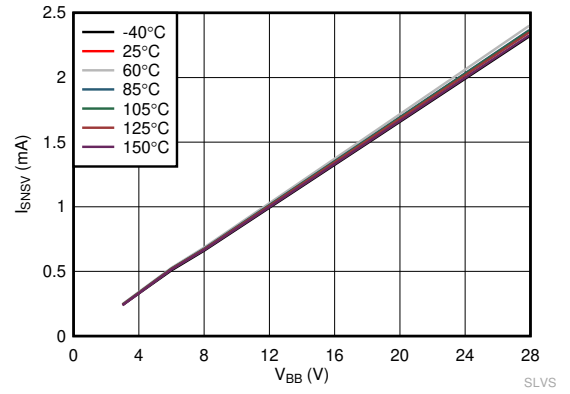

$V_{SEL1}$ = $V_{SEL2}$ = 0 V  $V_{EN}$ = 5 V  $V_{DIAG\_EN}$ = 5 V
$R_{SNS}$ = 1 kΩ  $T_A$ = 25°C

**Figure 7-15. Current Sense Output Current ($I_{SNSI}$) vs Load Current ($I_{OUT}$) across $V_{BB}$**



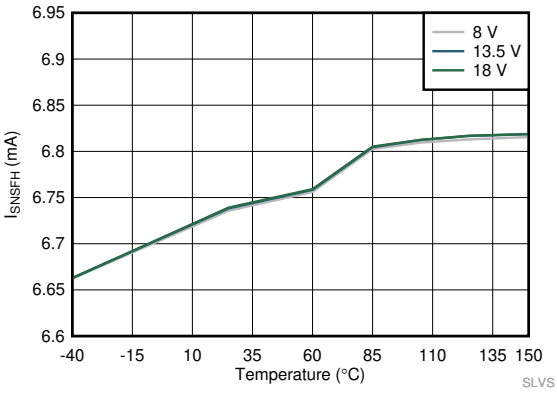

$V_{SEL1}$ = 5 V  $V_{SEL2}$ = 0 V  $V_{DIAG\_EN}$ = 5 V
$R_{SNS}$ = 1 kΩ  $V_{EN}$ = 0 V

**Figure 7-16. Temperature Sense Output Current ($I_{SNST}$) vs Temperature**



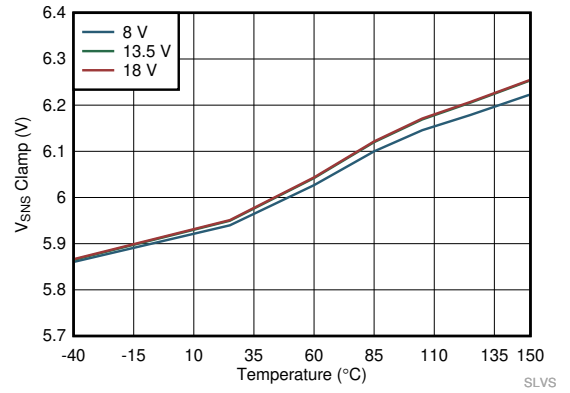

$V_{SEL1}$ = $V_{SEL2}$ = 5 V  $V_{EN}$ = 0 V  $V_{DIAG\_EN}$ = 5 V
$R_{SNS}$ = 1 kΩ  $I_{OUT}$ = 0 A

**Figure 7-17. Voltage Sense Output Current ($I_{SNSV}$) vs $V_{BB}$**



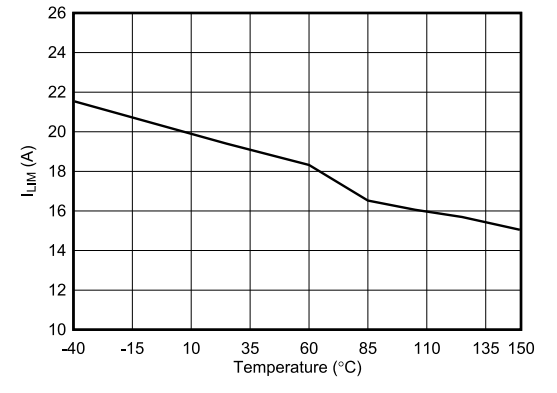

$V_{SEL1}$ = $V_{SEL2}$ = 0 V  $V_{EN}$ = 0 V  $V_{DIAG\_EN}$ = 5 V
$R_{SNS}$ = 500 Ω  $V_{OUT}$ Floating

**Figure 7-18. Fault High Output Current ($I_{SNSFH}$) vs Temperature**




$V_{SEL1}$ = $V_{SEL2}$ = 0 V  $V_{EN}$ = 5 V  $V_{DIAG\_EN}$ = 5 V
$R_{SNS}$ = 10 kΩ  $I_{OUT}$ = 4 A

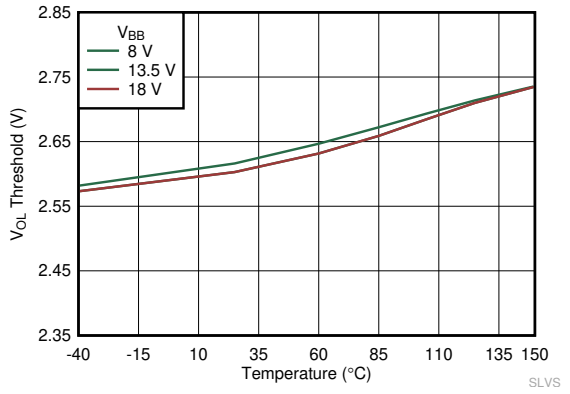
**Figure 7-19. Sense Pin Clamp Voltage ($V_{SNSCLAMP}$) vs Temperature**




$V_{BB}$ = 13.5 V  $V_{OUT}$ = 0 V  $V_{DIAG\_EN}$ = 0 V
Device Version C  $V_{EN}$ = 5 V  $V_{LATCH}$ = 5 V

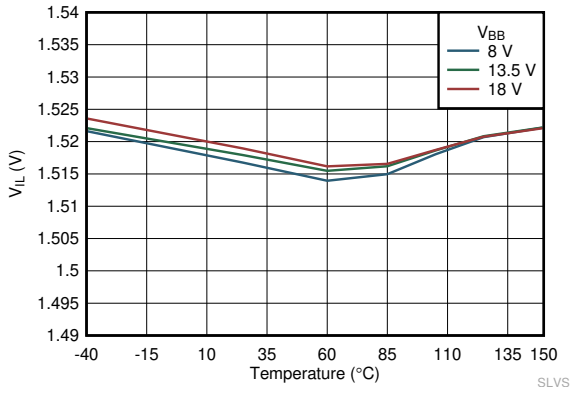
**Figure 7-20. Current Limit ($I_{CL}$) vs Temperature**

## 7.8 Typical Characteristics (continued)



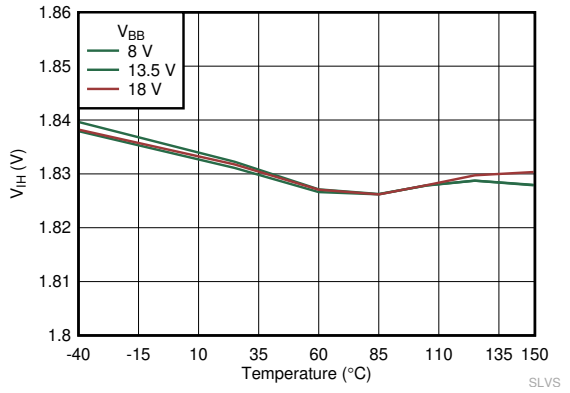

$V_{EN}$ = 0 V $V_{OUT}$ = 0 V to 5 V $I_{OUT}$ = 0 A
$V_{DIAG\_EN}$= 5 V $V_{SEL1}$ = $V_{SEL2}$ = 0 V

**Figure 7-21. Open Load Detection Voltage ($V_{OL}$) vs Temperature**



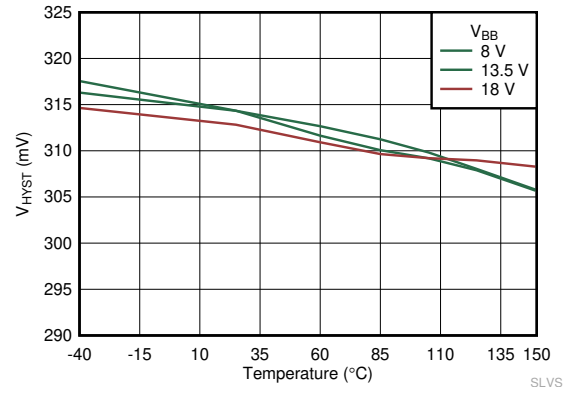

$V_{EN}$ = 3.3 V to 0 V $V_{OUT}$ = 0 V $V_{DIAG\_EN}$ = 0 V
$R_{OUT}$ = 1 kΩ

**Figure 7-22. $V_{IL}$ vs Temperature**



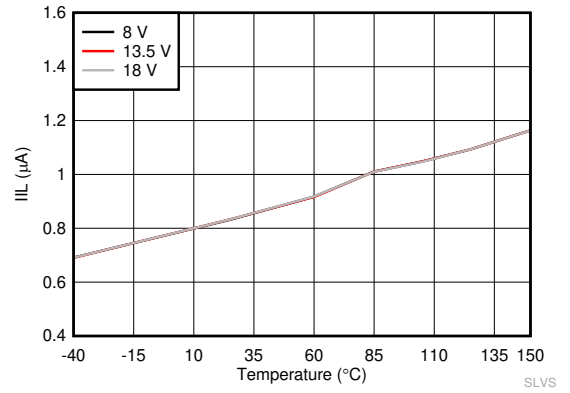

$V_{EN}$ = 0 V to 3.3 V $V_{OUT}$ = 0 V $V_{DIAG\_EN}$ = 0 V
$R_{OUT}$ = 1 kΩ

**Figure 7-23. $V_{IH}$ vs Temperature**



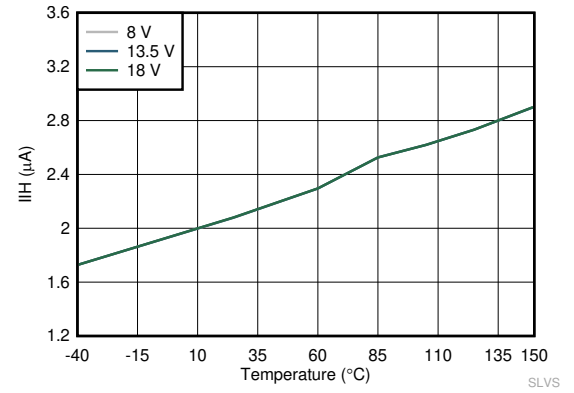

$V_{EN}$ = 0 V to 3.3 V and 3.3 V to 0 V $V_{OUT}$ = 0 V $V_{DIAG\_EN}$ = 0 V
$R_{OUT}$ = 1 kΩ

**Figure 7-24. $V_{IHYS}$ vs Temperature**




$V_{EN}$ = 0.8 V $V_{OUT}$ = 0 V $V_{DIAG\_EN}$ = 0 V
$R_{OUT}$ = 1 kΩ

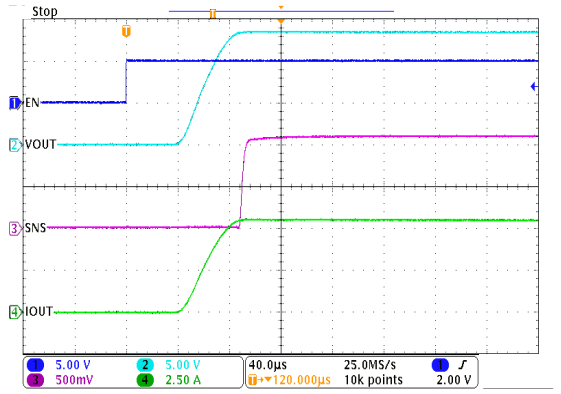
**Figure 7-25. $I_{IL}$ vs Temperature**




$V_{EN}$ = 2 V $V_{OUT}$ = 0 V $V_{DIAG\_EN}$ = 0 V
$R_{OUT}$ = 1 kΩ

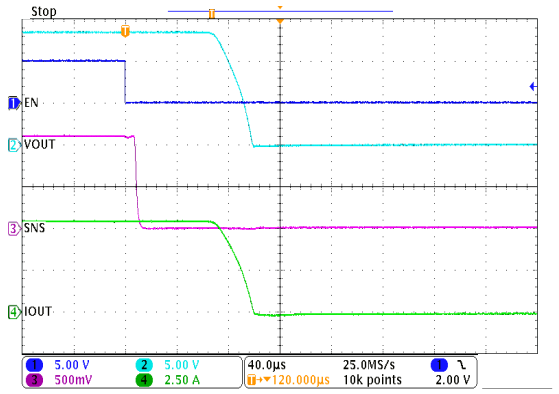
**Figure 7-26. $I_{IH}$ vs Temperature**

## 7.8 Typical Characteristics (continued)



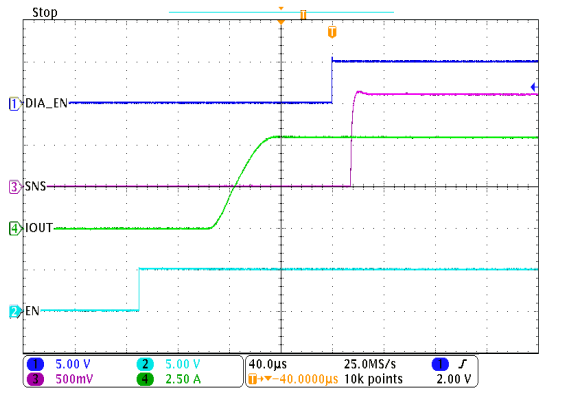

$R_{OUT}$ = 2.6 Ω $R_{SNS}$ = 1 kΩ $V_{DIA\_EN}$ = 5 V
$V_{SEL1}$ = $V_{SEL2}$ = 0 V

**Figure 7-27. Turn-on Time ($t_{ON}$)**



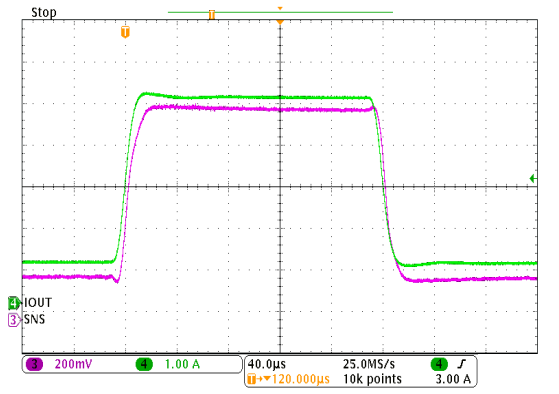

$R_{OUT}$ = 2.6 Ω $R_{SNS}$ = 1 kΩ $V_{DIA\_EN}$ = 5 V
$V_{SEL1}$ = $V_{SEL2}$ = 0 V

**Figure 7-28. Turn-off Time ($t_{OFF}$) and Sense Settle Time ($t_{SNSION2}$)**



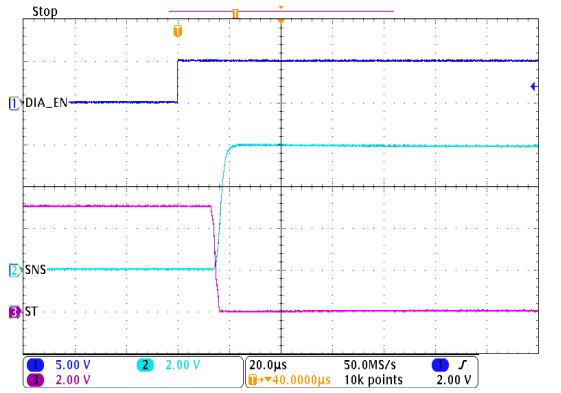

$R_{OUT}$ = 2.6 Ω $R_{SNS}$ = 1 kΩ $V_{DIA\_EN}$= 0 V to 5 V
$V_{SEL1}$ = $V_{SEL2}$ = 0 V

**Figure 7-29. $I_{SNS}$ Settling Time ($t_{SNSION1}$) on DIA_EN Transition**



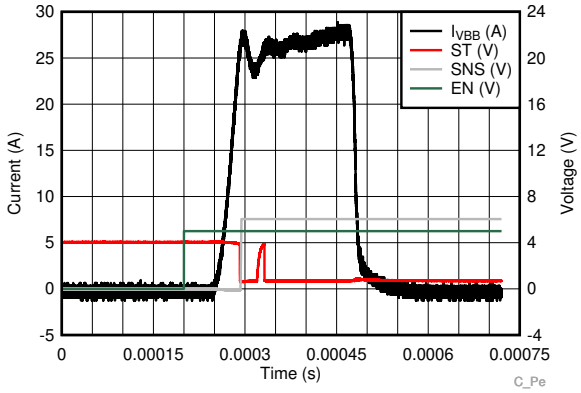

$I_{OUT}$ = 1 A to 5 A $R_{SNS}$ = 1 kΩ $V_{DIA\_EN}$ = 5 V
$V_{SEL1}$ = $V_{SEL2}$ = 0 V

**Figure 7-30. $I_{SNS}$ Settling Time ($t_{SETTLEH}$) on Rising Load Step**




$V_{OUT}$ = $V_{BB}$ $R_{SNS}$ = 1 kΩ $V_{SEL1}$ = $V_{SEL2}$ = 0 V
$V_{EN}$ = 0 V $V_{DIAG\_EN}$ = 5 V

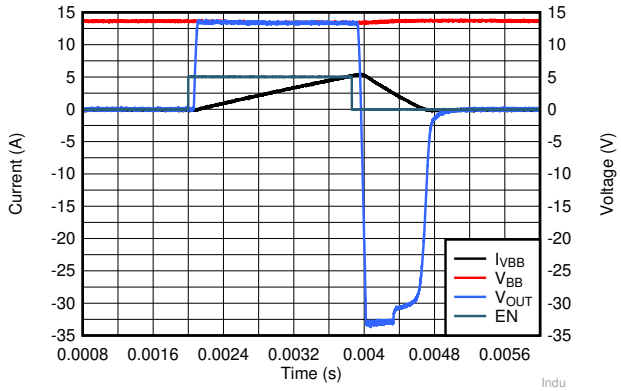
**Figure 7-31. Open Load Detection Time ($t_{OL2}$) on Rising DIAG_EN**




$V_{BB}$ = 13.5 V C Device Version $V_{OUT}$ = 0 V
$V_{EN}$ = 0 V to 5 V $T_A$ = 25°C

**Figure 7-32. Short Circuit Behavior**

## 7.8 Typical Characteristics (continued)




$V_{BB}$ = 13.5 V
$V_{EN}$ = 0 V to 5 V, 5 V to 0 V
$T_A$ = 125°C
$L_{OUT}$ = 5 mH

**Figure 7-33. Inductive Load Demagnetization**

# 8 Parameter Measurement Information

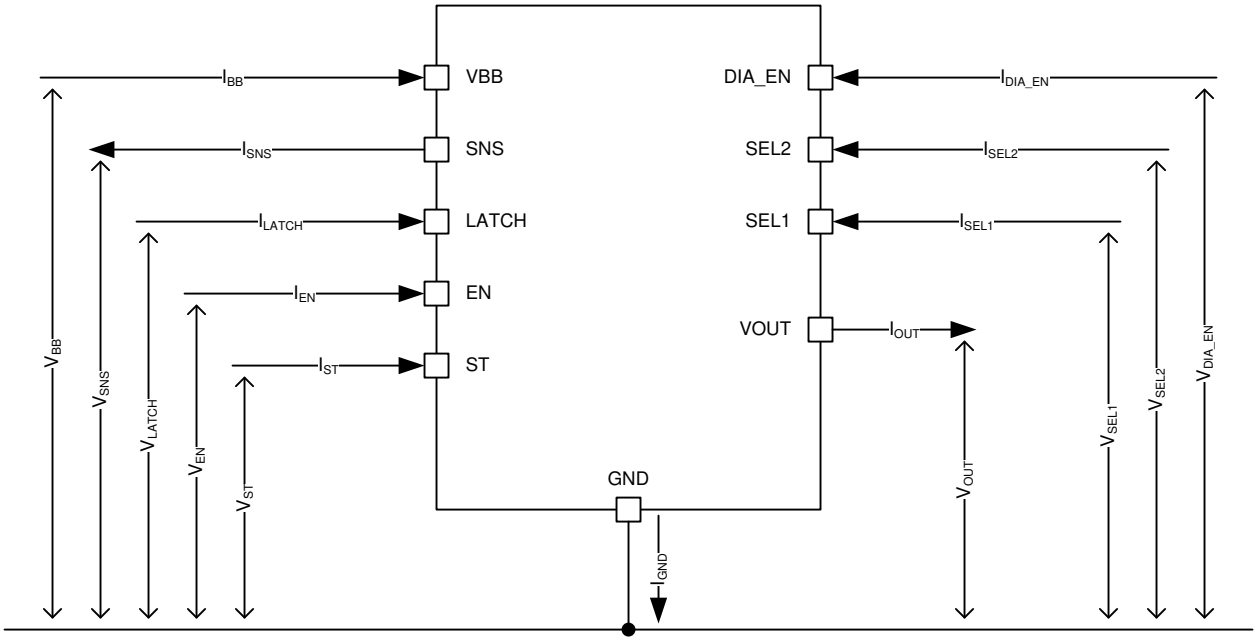



**Figure 8-1. Parameter Definitions**

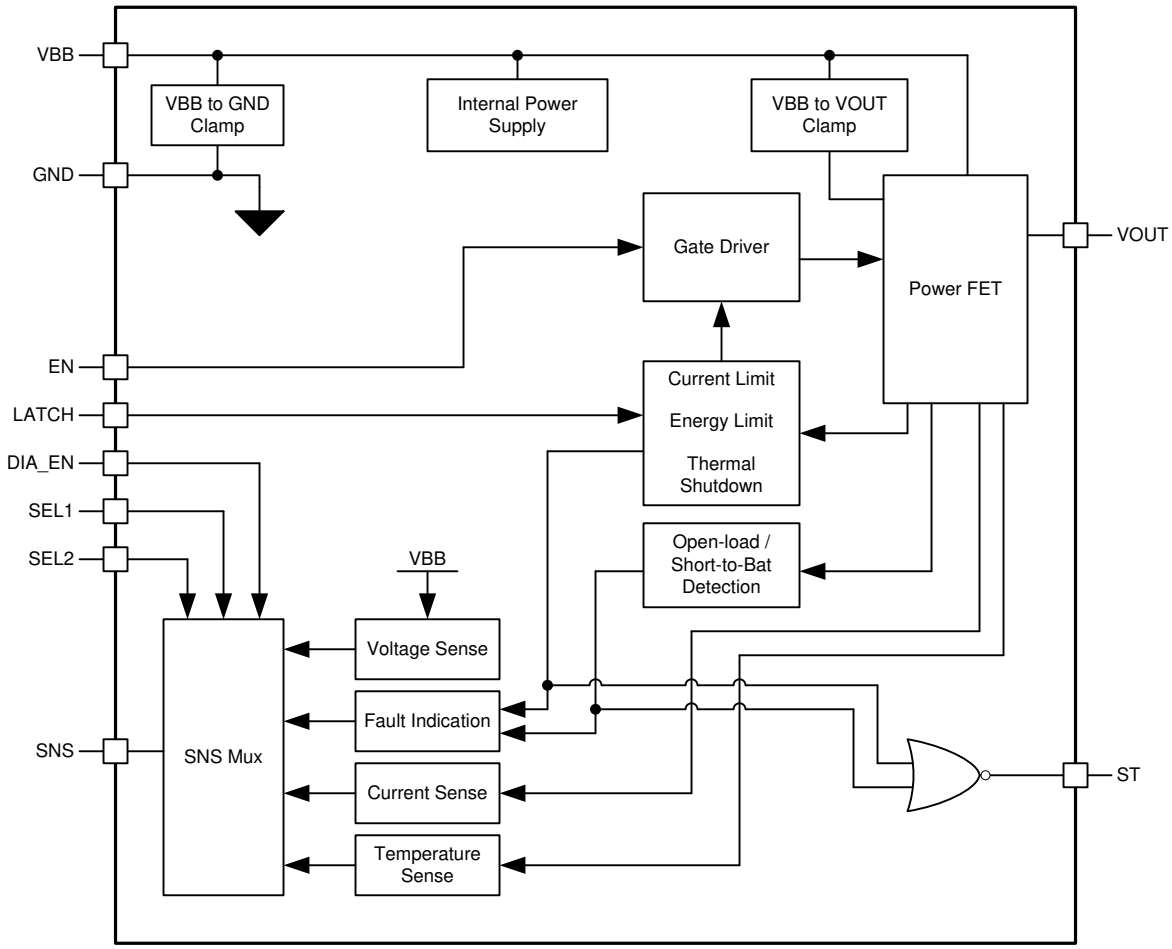
# 9 Detailed Description

## 9.1 Overview

The TPS27SA08-Q1 device is a single-channel smart high-side power switch intended for use with 24-V supply automotive systems. Many protection and diagnostic features are integrated in the device. Diagnostics features include the analog SNS output and the open-drain fault indication ($\overline{ST}$). The analog SNS output is capable of providing a signal that is proportional to device temperature, supply voltage, or load current. The high-accuracy load current sense allows for diagnostics of complex loads.

This device includes protection through thermal shutdown, current limit, transient withstand, and reverse supply operation. For more details on the protection features, refer to the *Feature Description* and *Application Information* sections of the document.

## 9.2 Functional Block Diagram



## 9.3 Feature Description

### 9.3.1 Protection Mechanisms

The TPS27SA08-Q1 device is designed to operate in a rugged automotive environment. The protection mechanisms allow the device to be robust against many system-level events such as reverse supply, short-to-ground and more.

There are additional protection features which, if triggered, will cause the switch to automatically disable:

- Thermal Shutdown
- Energy Limit

When any of these protections are triggered, the device will enter the FAULT state. In the FAULT state, the fault indication will be available on both the SNS pin and the $\overline{ST}$ pin (see the diagnostic section of the data sheet for more details).

The switch is no longer held off and the fault indication is reset when all of the below conditions are met:

- LATCH pin is low
- $t_{RETRY}$ has expired
- All faults are cleared (thermal shutdown, current limit, energy limit)

#### *9.3.1.1 Thermal Shutdown*

The TPS27SA08-Q1 device includes temperature sensors on the FET and inside of the device controller. When $T_{J,FET} > T_{ABS}$, the device will see a thermal shutdown fault. After the fault is detected, the switch will turn off. The fault is cleared when the switch temperature decreases by the hysteresis value, $T_{HYS}$.

#### *9.3.1.2 Current Limit*

When $I_{OUT}$ reaches the current limit threshold, $I_{CL}$, the device remains enabled and limits the current $I_{OUT}$ to close to the threshold, $I_{CL}$ . In the case that the device remains enabled and limits $I_{OUT}$, the thermal shutdown and/or energy limit protection feature may be triggered due to the high amount of power dissipation in the device.

During a short circuit event, the device will hit the $I_{CL}$ threshold that is listed in the *Specifications* and then regulate the output current close to the threshold value to protect the device. The device will detect a short circuit event when the output current exceeds $I_{CL}$, however the measured maximum current may exceed the $I_{CL}$ threshold due to the finite response time of the TPS27SA08-Q1 device current limit regulation loop. The device is guaranteed to protect itself during a short circuit event over the nominal supply voltage range (as defined in the *Specifications* section) at 125°C.

##### 9.3.1.2.1 Current Limit Foldback

The TPS27SA08-Q1 device implements a current limit foldback feature that is designed to protect the device in the case of a long-term fault condition. If the device undergoes three consecutive fault shutdown events (any of thermal shutdown, current limit, or energy limit), the current limit will be reduced to half of the original value. The device will revert back to the original current limit threshold if either of the following occurs:

- The device goes to *Standby Delay*.
- The switch turns-on and turns-off without any fault occurring.

##### 9.3.1.2.2 Undervoltage Lockout (UVLO)

The device monitors the supply voltage $V_{BB}$ to prevent unpredicted behaviors in the event that the supply voltage is too low. When the supply voltage falls down to $V_{UVLOF}$, the output stage is shut down automatically. When the supply rises up to $V_{UVLOR}$, the device turns back on.

During an initial ramp of $V_{BB}$ from 0 V at a ramp rate slower than 1 V/ms, $V_{EN}$ pin will have to be held low until $V_{BB}$ is above UVLO threshold (with respect to board ground) and the supply voltage to the device has reliably reached above the UVLO condition. For best operation, ensure that $V_{BB}$ has risen above UVLO before setting the $V_{EN}$ pin to high.

#### 9.3.1.2.3 $V_{BB}$ during Short-to-Ground

When $V_{OUT}$ is shorted to ground, the module power supply ($V_{BB}$) can have a transient decrease. This is caused by the sudden increase in current flowing through the wiring harness cables. To achieve ideal system behavior, it is recommended that the module maintain $V_{BB}$ > 3 V during $V_{OUT}$ short-to-ground. This is typically accomplished by placing bulk capacitance on the power supply node.

### *9.3.1.3 Energy Limit*

The energy limiting feature is implemented to protect the switch from excessive stress. The device will continuously monitor the amount of energy dissipated in the FET. If the energy limit threshold is reached, the switch will automatically disable. In practice, the energy limit will only be reached during a fault event such as short-to-ground.

Energy limit events have the same system-level behavior as thermal shutdown events.

### *9.3.1.4 Voltage Transients*

The TPS27SA08-Q1 device contains two voltage clamps which protect the device against system-level voltage transients.

The clamp from $V_{BB}$ to GND is primarily used to protect the controller from positive transients on the supply line. The clamp from $V_{BB}$ to $V_{OUT}$ is primarily used to limit the voltage across the FET when switching off an inductive load. Both clamp levels are set to protect the device during these fault conditions. If the voltage potential from $V_{BB}$ to GND exceeds the $V_{BB}$ clamp level, the clamp will allow current to flow through the device from $V_{BB}$ to GND (Path 2). If the voltage potential from $V_{BB}$ to $V_{OUT}$ exceeds $V_{CLAMP}$, the power FET will allow current to flow from $V_{BB}$ to $V_{OUT}$ (Path 3).

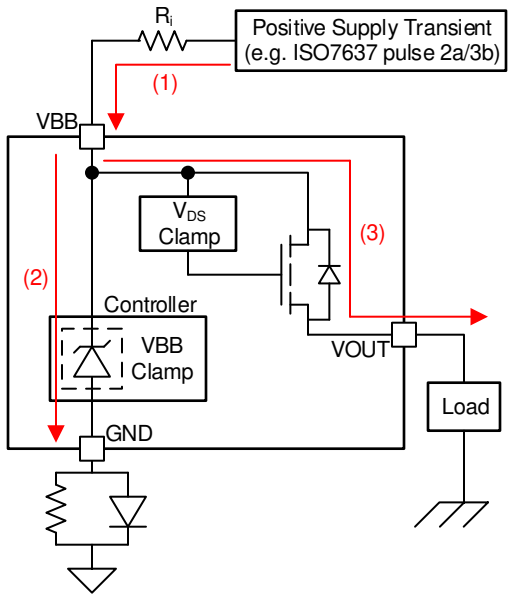



**Figure 9-1. Current Path During Supply Voltage Transient**

#### 9.3.1.4.1 Driving Inductive and Capacitive Loads

When switching off an inductive load, the inductor may impose a negative voltage on the output of the switch. The TPS27SA08-Q1 device includes a voltage clamp to limit voltage across the FET. The maximum acceptable load inductance is a function of the device robustness. With a 5-mH load, the TPS27SA08-Q1 device can withstand a single pulse of 95 mJ inductive dissipation at 125°C and can withstand 56 mJ of inductive dissipation with a 10-Hz repetitive pulse. If the application parameters exceed this device limit, it is necessary to use a protection device like a freewheeling diode to dissipate the energy stored in the inductor. Figure 9-2 shows the TPS27SA08-Q1 device discharging a 5-mH load that is driven at 5 A.

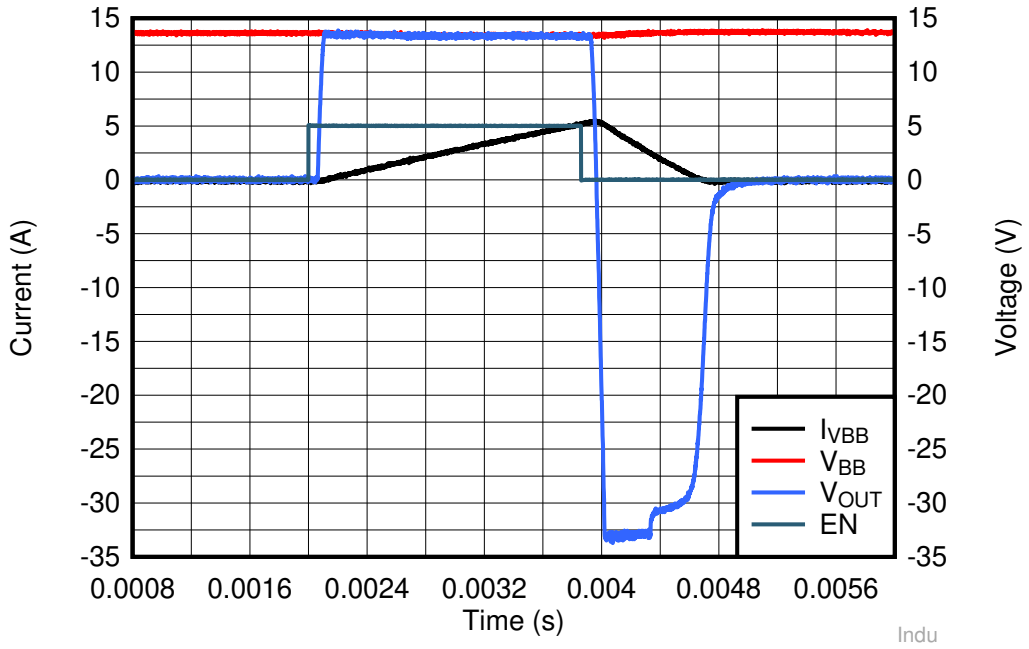



**Figure 9-2. Inductive Discharge (5 mH, 5 A)**

In addition, the TPS27SA08-Q1 device current limit provides an ideal way to charge a capacitive load safely with limited inrush current. With no protection, charging a large capacitive load can lead to high inrush currents that pull a supply down, however by using a relatively low current limit value (regulation around 24 A), the capacitive load can be charged without impact to the power supply.

For more information on driving inductive or capacitive loads, reference *TI's "How To Drive Inductive, Capacitive, and Lighting Loads with Smart High Side Switch* application report.

#### *9.3.1.5 Reverse supply*

In the reverse supply condition, the switch will automatically be enabled (regardless of EN status) to prevent power dissipation inside the MOSFET body diode. In many applications (for example, resistive load), the full load current may be present during reverse supply. In order to activate the automatic switch on feature, the SEL2 pin must have a path to module ground. This may be path 1 as shown below, or, if the SEL2 pin is unused, the path may be through $R_{PROT}$ to module ground.

Protection features (for example, thermal shutdown) are not available during reverse supply. Care must be taken to ensure that excessive power is not dissipated in the switch during the reverse supply condition.

There are two options for blocking reverse current in the system. Option 1 is to place a blocking device (FET or diode) in series with the supply. This will block all current paths. Option 2 is to place a blocking diode in series with the GND node of the high-side switch. This method will protect the controller portion of the switch (path 2), but it will not prevent current from flowing through the load (path 3). The diode used for Option 2 may be shared amongst multiple high-side switches.

Path 1 shown in Figure 9-3 is blocked inside of the device.

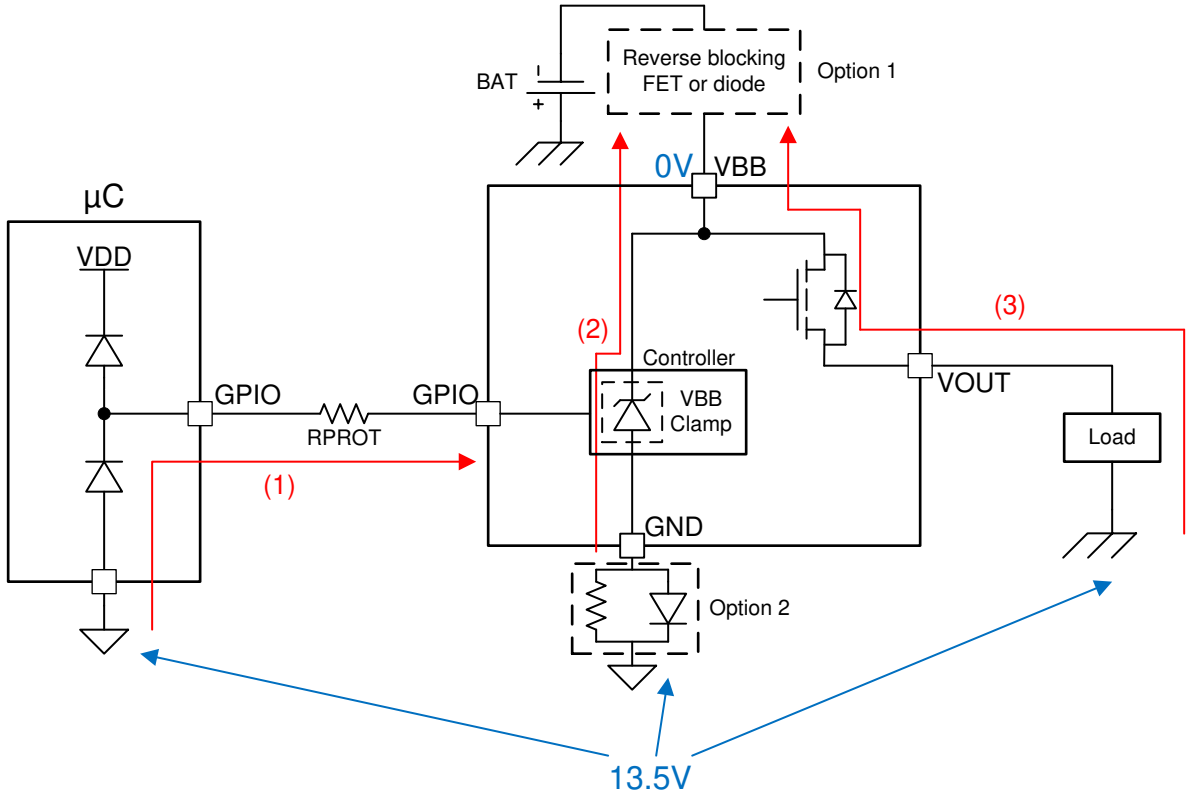



**Figure 9-3. Current Path During Reverse supply**

#### *9.3.1.6 Fault Event – Timing Diagrams*

**Note**

All timing diagrams assume that the SELx pins are set to 00.

The LATCH, DIA_EN, and EN pins are controlled by the user. The timing diagrams represent a possible use-case.

Figure 9-4 shows the active current limiting behavior of TPS27SA08-Q1 device and the LATCH pin functionality. The switch will not shutdown until either the energy limit or the thermal shutdown is reached.

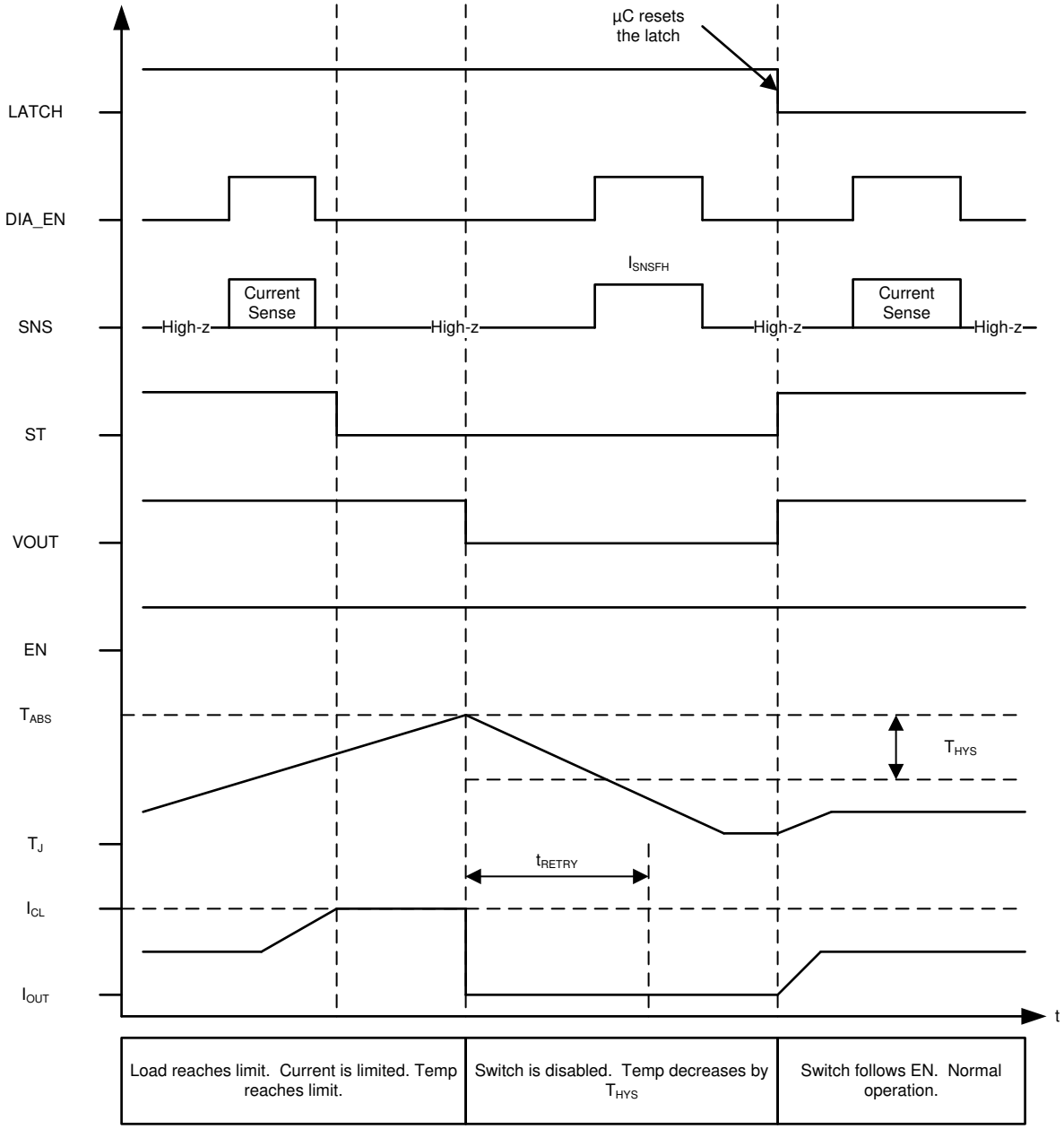



**Figure 9-4. Current Limit - Latched Behavior**

Figure 9-5 shows the active current limiting behavior of TPS27SA08-Q1 device. The switch will not shutdown until either thermal shutdown or energy limit is tripped. In this example, LATCH is tied to GND and the switch is turned ON when the FET temperature is low enough.

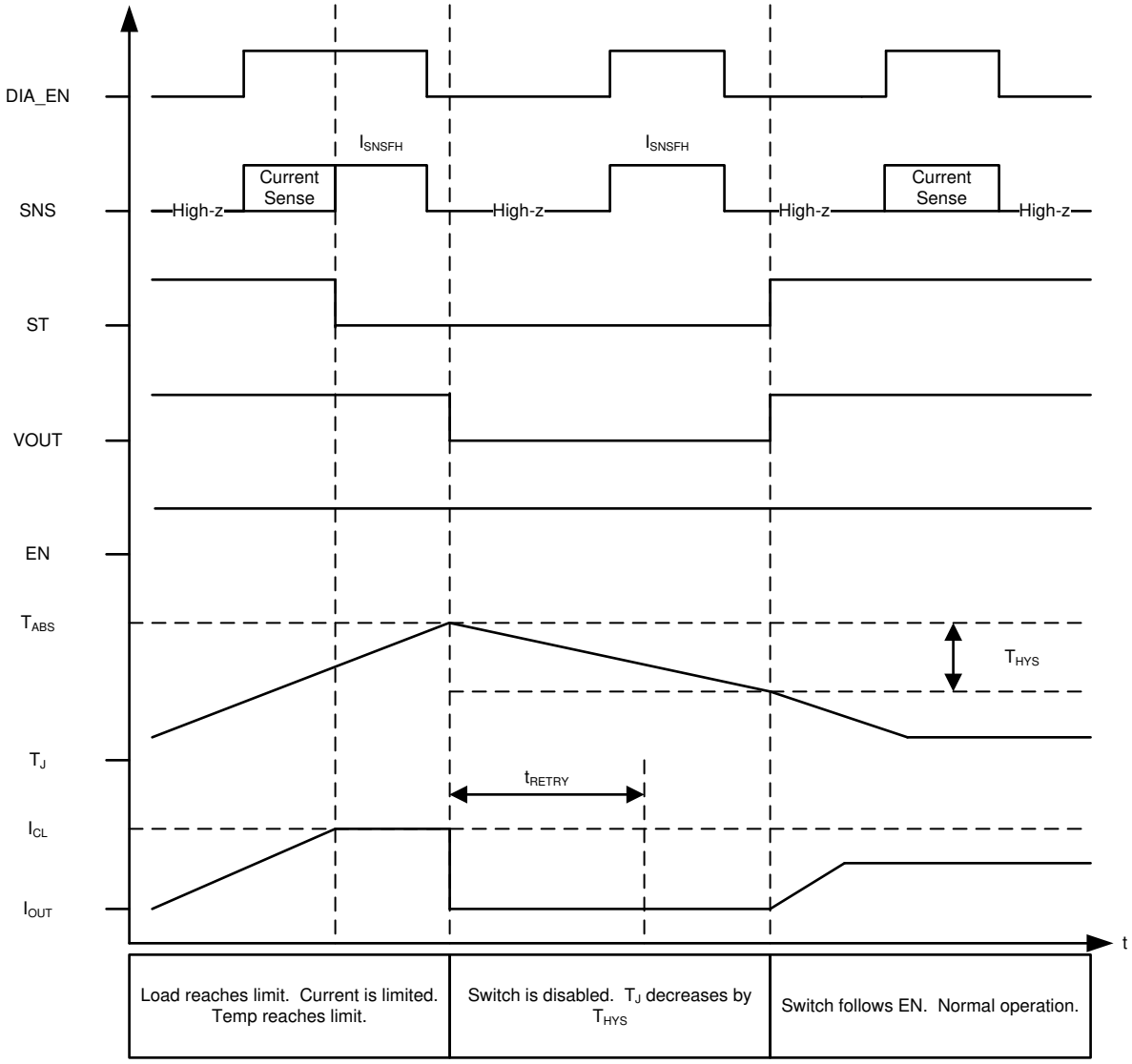



**Figure 9-5. Current Limit - LATCH Pin Permanently Low**

deWhen the switch retries after a shutdown event, the SNS fault indication will remain until $V_{OUT}$ has risen to $V_{BB}$ – 1.8 V. Once $V_{OUT}$ has risen, the SNS fault indication is reset and current sensing is available. $\overline{ST}$ fault indication is reset as soon as the switch is re-enabled (does not wait for $V_{OUT}$ to rise). If there is a short-to-ground and $V_{OUT}$ is not able to rise, the SNS fault indication will remain indefinitely. The following diagram illustrates auto-retry behavior and provides a zoomed-in view of the fault indication during retry.

**Note**

Figure 9-6 assumes that $t_{RETRY}$ has expired by the time that $T_J$ reaches the hysteresis threshold.

LATCH = 0 V and DIA_EN = 5 V

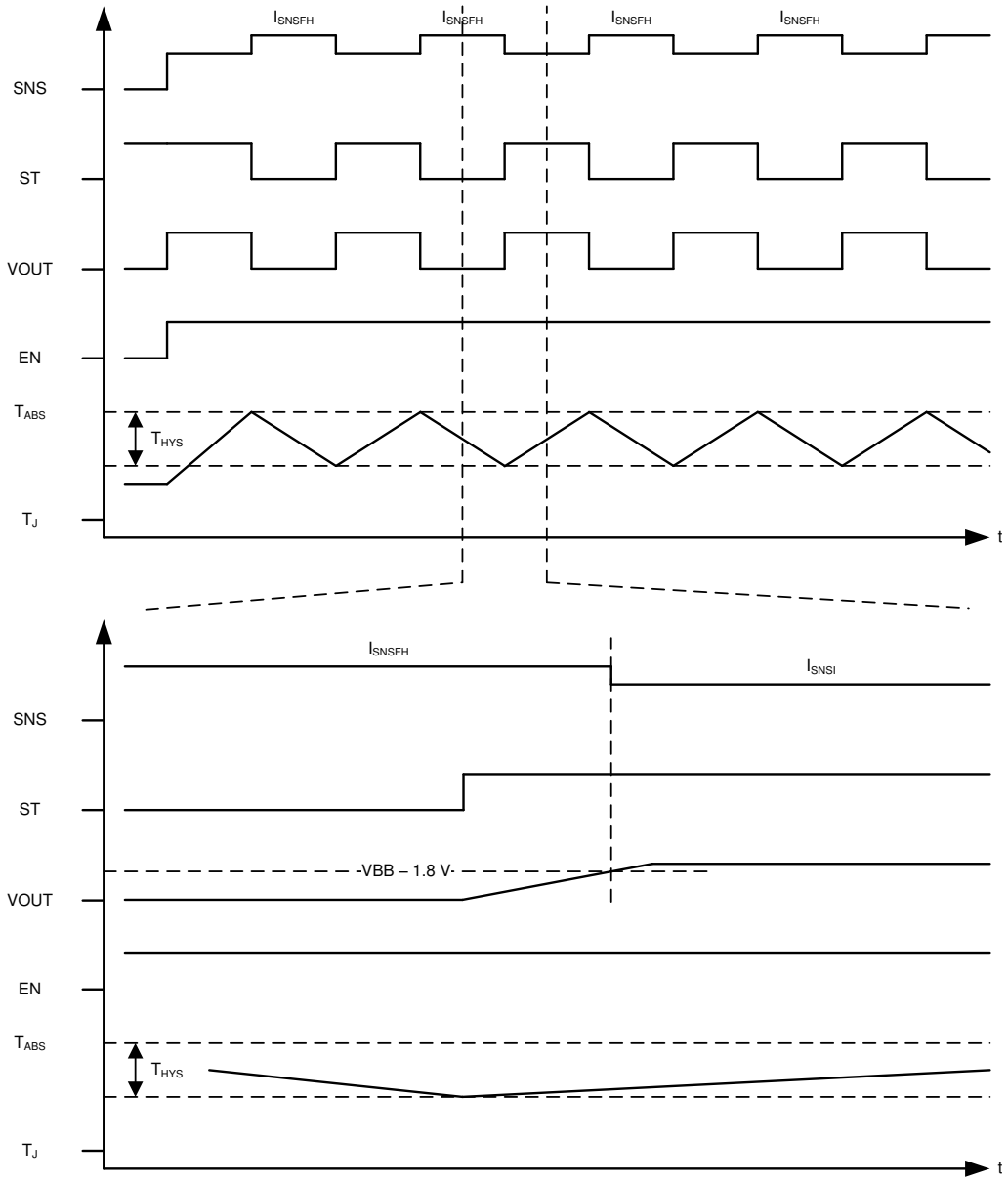



**Figure 9-6. Fault Indication During Retry**

## 9.3.2 Diagnostic Mechanisms

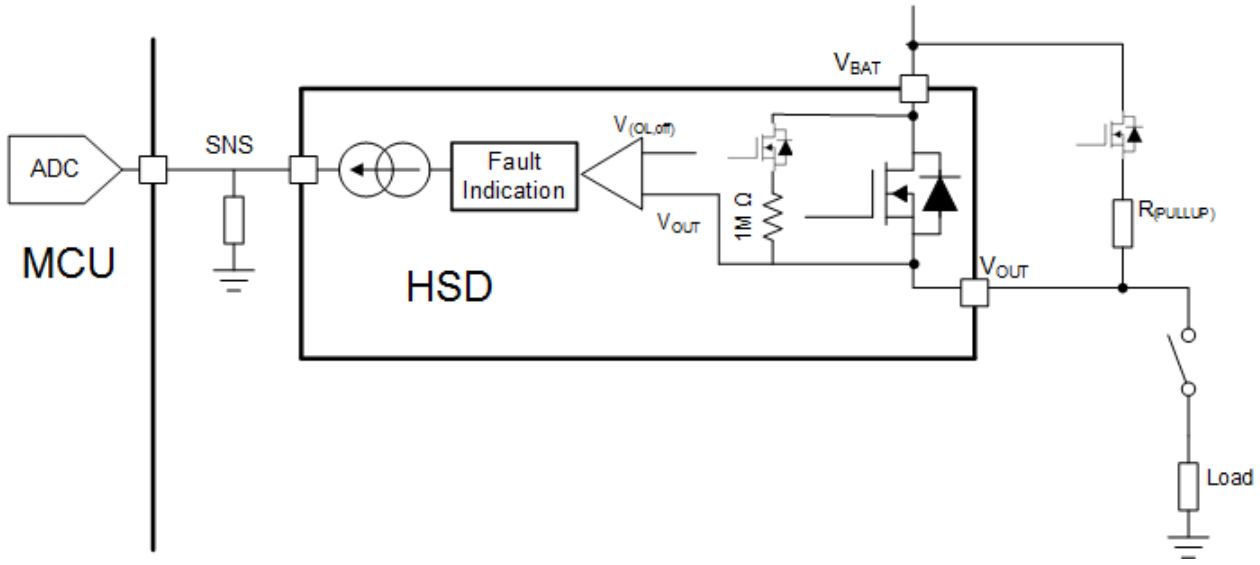
### *9.3.2.1 $V_{OUT}$ Short-to-supply and Open-Load*

#### 9.3.2.1.1 Detection With Switch Enabled

When the switch is enabled, the $V_{OUT}$ short-to-supply and open-load conditions can be detected with the current sense feature. In both cases, the load current will be measured through the SNS pin and will be below the expected value.

#### 9.3.2.1.2 Detection With Switch Disabled

While the switch is disabled, if DIA_EN is high, an internal comparator will detect the condition of $V_{OUT}$. If the load is disconnected (open load condition) or there is a short to supply the$_{OUT}$ voltage will be higher than the open load threshold ($V_{OL,off}$) and a fault is indicated on the SNS pin. An internal pull-up of 1 MΩ is in series with an internal MOSFET switch, so no external component is required if only a completely open load needs to be detected. However, if there is significant leakage or other current draw even when the load is disconnected, a lower value pull-up resistor and switch can be added externally to set the $V_{OUT}$ voltage above the $V_{OL,off}$ during open load conditions.




A. This figure assumes that the device ground and the load ground are at the same potential. In application, there may be a ground shift voltage of 1 V to 2 V.

**Figure 9-7. Short-to-supply and Open-Load Detection**

The detection circuitry is only enabled when DIA_EN = HIGH and EN = LOW.

If $V_{OUT} > V_{OL}$, the SNS pin will go to the fault level.

If $V_{OUT} < V_{OL}$, then there is no fault indication.

The fault indication will only occur if the SEL1 pin is set to diagnose the channel.

While the switch is disabled and DIA_EN is high, the fault indication mechanisms will continuously represent the present status. For example, if $V_{OUT}$ decreases from > $V_{OL}$ to < $V_{OL}$, the fault indication is reset. Additionally, the fault indication is reset upon the falling edge of DIA_EN or the rising edge of EN.

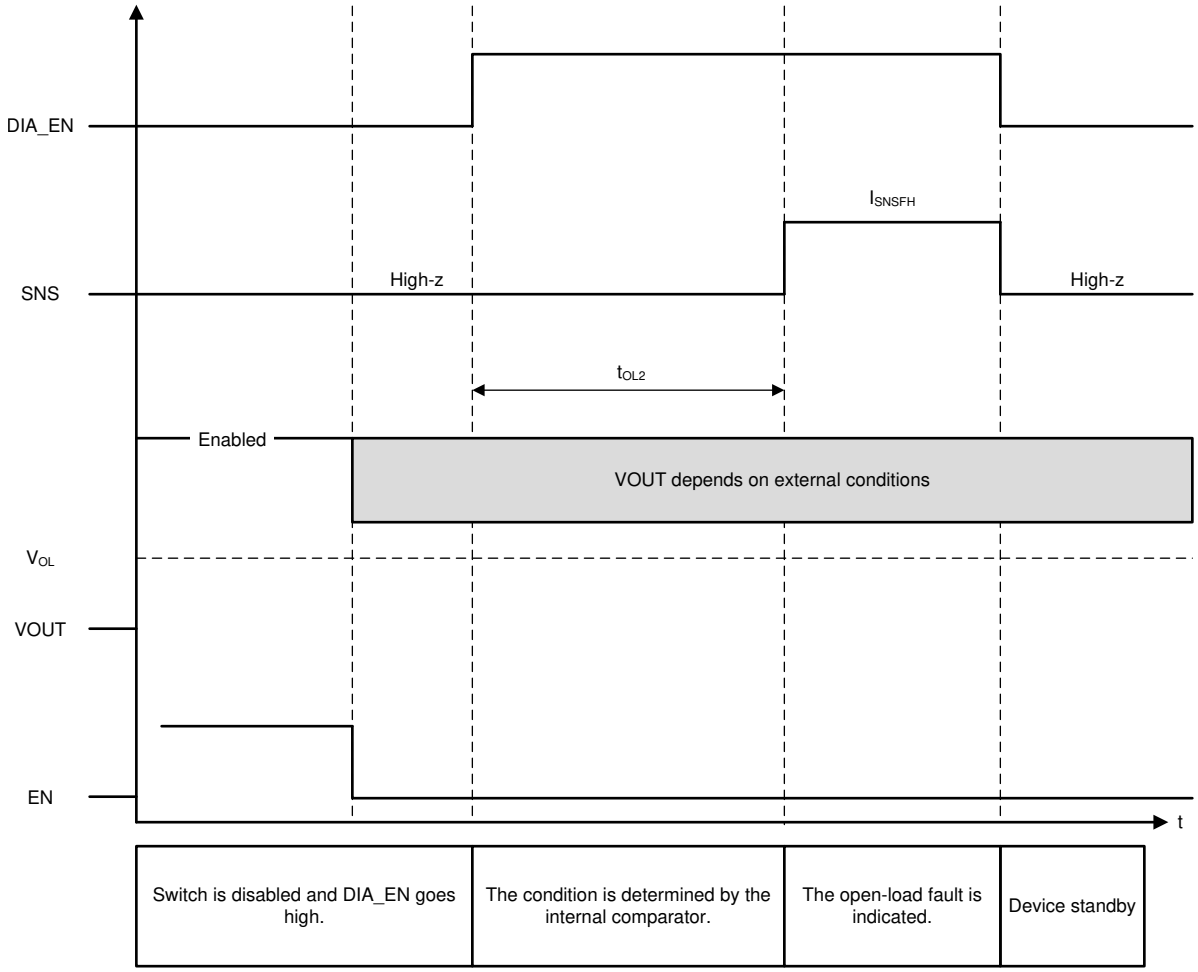



**Figure 9-8. Open Load**

### *9.3.2.2 SNS Output*

The SNS output may be used to sense the load current, supply voltage, or device temperature. The SELx pins will select the desired sense signal. The sense circuit will provide a current that is proportional to the selected parameter. This current will be sourced into an external resistor to create a voltage that is proportional to the selected parameter. This voltage may be measured by an ADC or comparator.

To ensure accurate sensing measurement, the sensing resistor should be connected to the same ground potential as the µC ADC.

The SNS Output includes an internal clamp, $V_{SNSclamp}$. This clamp is designed to prevent a high voltage at the SNS output and the ADC input.

**Table 9-1. Analog Sense Transfer Function**

| PARAMETER | TRANSFER FUNCTION |
|---|---|
| Load current | $I_{SNSI} = I_{OUT} / 4600$ |
| Supply voltage(1) | $I_{SNSV} = (V_{BB}) \times dI_{SNSV} / dV$ |
| Device temperature | $I_{SNST} = (T_J – 25°C) \times dI_{SNST} / dT + 0.85$ |

(1) Voltage potential between the $V_{BB}$ pin and the GND pin.

The SNS output will also be used to indicate system faults. $I_{SNS}$ will go to the predefined level, $I_{SNSFH}$, when there is a fault. This level is defined in the electrical specifications.

#### 9.3.2.2.1 $R_{SNS}$ Value

The following factors should be considered when selecting the $R_{SNS}$ value:

- Current sense ratio
- Largest and smallest diagnosable load current
- Full-scale voltage of the ADC
- Resolution of the ADC

For an example of selecting $R_{ISNS}$ value, reference in the applications section of this data sheet.

##### *9.3.2.2.1.1 High Accuracy Load Current Sense*

In many systems, it is required that the high-side switch provide diagnostic information about the downstream load. With more complex loads, high accuracy sensing is required. A few examples follow:

- **Solenoid Protection**: Often solenoids are precisely controlled by low-side switches. However, in a fault event, the low-side switch cannot disconnect the solenoid from the power supply. A high-side switch can be used to continuously monitor several solenoids. If the system current becomes higher than expected, the high-side switch can disable the module.

##### *9.3.2.2.1.2 SNS Output Filter*

To achieve the most accurate current sense value, it is recommended to apply filtering to the SNS output. There are two methods of filtering:

- Low-Pass RC filter between the SNS pin and the ADC input. This filter is illustrated in Figure 10-1 and typical values for the resistor and capacitor are given. The designer should select a $C_{SNS}$ capacitor value based on system requirements. A larger value will provide improved filtering. A smaller value will allow for faster transient response.
- The ADC and microcontroller can also be used for filtering. It is recommended that the ADC collects several measurements of the SNS output. The median value of this data set should be considered as the most accurate result. By performing this median calculation, the microcontroller is able to filter out any noise or outlier data.

### *9.3.2.3 $\overline{ST}$ Pin*

The $\overline{ST}$ pin is an open-drain output. The pin indicates the status of the switch channel. The output is high-z when there is no fault condition. The output is pulled low when there is a fault condition.

### *9.3.2.4 Fault Indication and SNS Mux*

The following faults will be communicated via the SNS and $\overline{ST}$ outputs:

- Switch shutdown, due to:
  - Thermal Shutdown
  - Current limit
  - Energy limit
- Active current limiting
- Open-Load / $V_{OUT}$ shorted-to-supply

Open-load / Short-to-supply are not indicated while the switch is enabled (though these conditions can be detected via the sense current). Hence, if there is a fault indication corresponding to an enabled channel, then it must be either switch shutdown or active current limiting.

The SNS pin will only indicate the fault if the SELx = 00. Switch shutdown fault indication will occur on the $\overline{ST}$ pin regardless of the SELx pins; however, OL/STB fault indication is only available when the SELx = 00.

**Table 9-2. SNS Mux**

| INPUTS | | | | OUTPUTS | |
|---|---|---|---|---|---|
| DIA_EN | SEL1 | SEL2 | FAULT DETECT(1) | SNS | ST |
| 0 | X | X | 0 | High-z | High-z |
| 0 | X | X | 1 | High-z | Pull low |
| 1 | 0 | 0 | 0 | Load current | High-z |
| 1 | 0 | 1 | 0 | Not Used | Not Used |
| 1 | 1 | 0 | 0 | Device temperature | High-z |
| 1 | 1 | 1 | 0 | Supply voltage | High-z |
| 1 | 0 | 0 | 1 | $I_{SNSFH}$ | Pull low |
| 1 | 0 | 1 | 1 | Not Used | Not Used |
| 1 | 1 | 0 | 1 | Device temperature | Pull low |
| 1 | 1 | 1 | 1 | Supply voltage | Pull low |

(1) Fault Detect encompasses the below conditions:
- Switch shutdown and waiting for retry
- Active current limiting
- OL / STB

### *9.3.2.5 Resistor Sharing*

Multiple high-side switch channels may use the same SNS resistor as shown in Figure 9-9 below. This reduces the total number of passive components in the system and the number of ADC terminals that are required of the microcontroller.

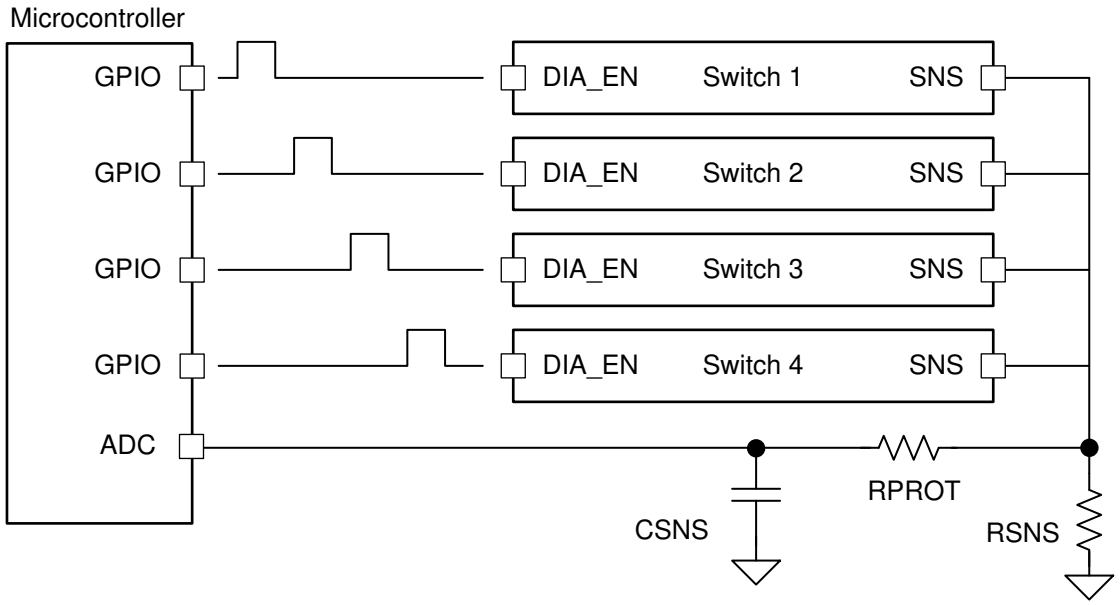



**Figure 9-9. Sharing $R_{SNS}$ Among Multiple Devices**

### *9.3.2.6 High-Frequency, Low Duty-Cycle Current Sensing*

Some applications will operate with a high-frequency, low duty-cycle PWM. Such applications require fast settling of the SNS output. For example, a 250-Hz, 5% duty cycle PWM will have an on-time of only 200 µs. The microcontroller ADC may sample the SNS signal after the defined settling time, $t_{SNSION3}$.

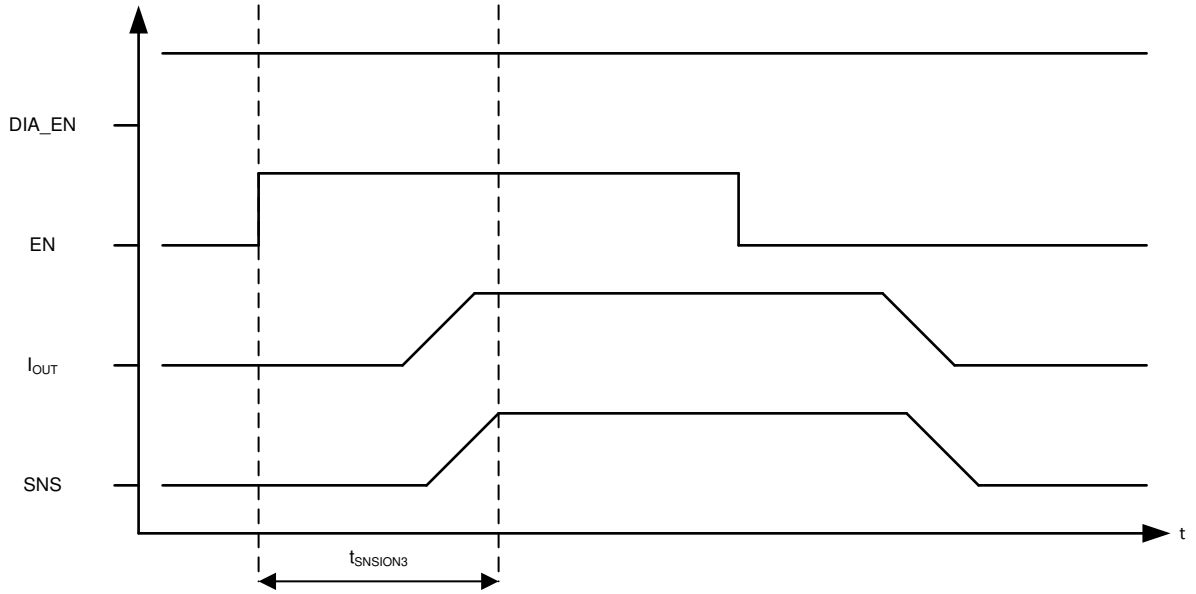



**Figure 9-10. Current Sensing in Low-Duty Cycle Applications**

## 9.4 Device Functional Modes

### 9.4.1 Off

Off state occurs when the device is not powered.

### 9.4.2 Standby

Standby state is a low-power mode used to reduce power consumption to the lowest level. Diagnostic capabilities are not available in Standby mode.

### 9.4.3 Diagnostic

Diagnostic state may be used to perform diagnostics while the switch is disabled.

### 9.4.4 Standby Delay

The Standby Delay state is entered when EN and DIA_EN are low. After $t_{STBY}$, if the EN and DIA_EN pins are still low, the device will go to Standby State.

### 9.4.5 Active

In Active state, the switch is enabled. The diagnostic functions may be turned on or off during Active state.

### 9.4.6 Fault

The Fault state is entered if a fault shutdown occurs (thermal shutdown, current limit, energy limit). After all faults are cleared, the LATCH pin is low, and the retry timer has expired, the device will transition out of Fault state. If the Enable pin is high, the switch will re-enable. If the Enable pin is low, the switch will remain off.

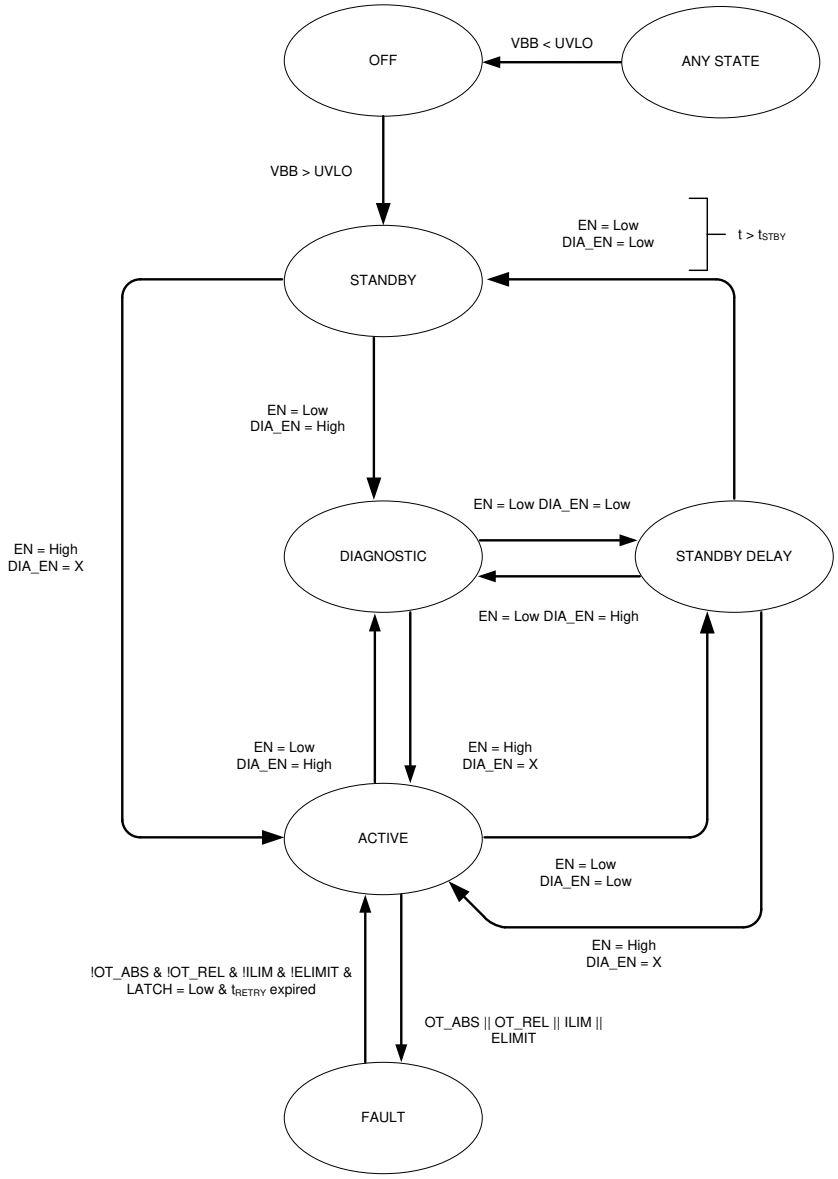


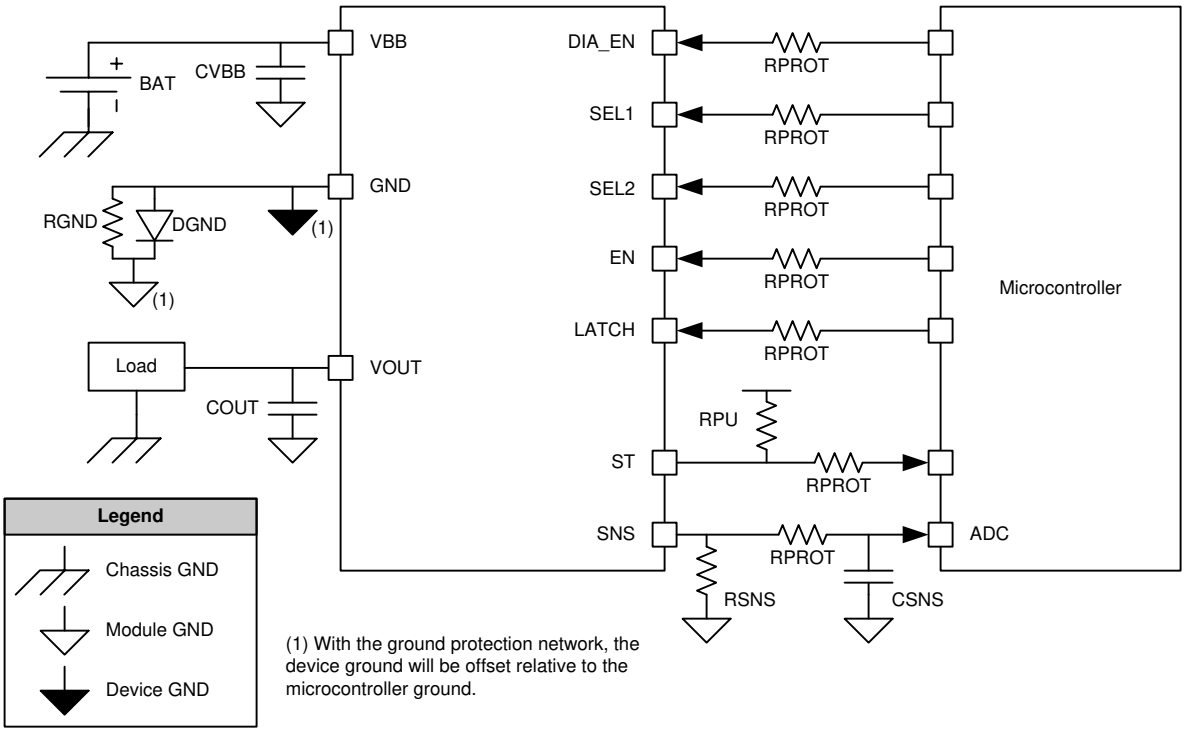

**Figure 9-11. State Diagram**

# 10 Application and Implementation

**Note**

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

## 10.1 Application Information




With the ground protection network, the device ground will be offset relative to the microcontroller ground.

**Figure 10-1. System Diagram**

**Table 10-1. Recommended External Components**

| COMPONENT | TYPICAL VALUE | PURPOSE |
|---|---|---|
| $R_{PROT}$ | 15 kΩ | Protect microcontroller and device I/O pins |
| $R_{SNS}$ | 1 kΩ | Translate the sense current into sense voltage |
| $R_{PU}$ | 10 kΩ | Provide pull-up source for open-drain output |
| $C_{SNS}$ | 100 pF - 10 nF | Low-pass filter for the ADC input |
| $R_{GND}$ | 4.7 kΩ | Stabilize GND potential during turn-off of inductive load |
| $D_{GND}$ | BAS21 Diode | Protects device during reverse supply |
| $C_{VBB}$ | 220 nF to Device GND | Filtering of voltage transients (for example, ESD, ISO7637-2) and improved emissions |
| | 100 nF to Module GND | Stabilize the input supply and filter out low frequency noise |
| $C_{OUT}$ | 22 nF | Filtering of voltage transients (for example, ESD, ISO7637-2) |

### 10.1.1 Ground Protection Network

As discussed in the section regarding Reverse supply, $D_{GND}$ may be used to prevent excessive reverse current from flowing into the device during a reverse supply event. Additionally, $R_{GND}$ is placed in parallel with $D_{GND}$ if the switch is used to drive an inductive load. The ground protection network ($D_{GND}$ and $R_{GND}$) may be shared amongst multiple high-side switches.

A minimum value for $R_{GND}$ may be calculated by using the absolute maximum rating for $I_{GND}$. During the reverse supply condition, $I_{GND} = V_{BB} / R_{GND}$:

$$R_{GND} \geq V_{BB} / I_{GND} \quad (1)$$

- Set $V_{BB}$ = –13.5 V
- Set $I_{GND}$ = –50 mA (absolute maximum rating)

$R_{GND} \geq$ –13.5 V / –50 mA = 270 Ω

In this example, it is found that $R_{GND}$ must be at least 270 Ω. It is also necessary to consider the power dissipation in $R_{GND}$ during the reverse supply event:

$$P_{RGND} = V_{BB}^{2} / R_{GND} \quad (2)$$

$P_{RGND} = (13.5\ V)^2 / 270\ \Omega = 0.675$ W

In practice, $R_{GND}$ may not be rated for such a high power. In this case, a larger resistor value should be selected.

### 10.1.2 Interface With Microcontroller

The ground protection network will cause the device ground to be at a higher potential than the module ground (and microcontroller ground). This offset will impact the interface between the device and the microcontroller.

Logic pin voltage will be offset by the forward voltage of the diode. For input pins (for example, EN), the designer must consider the $V_{IH}$ specification of the switch and the $V_{OH}$ specification of the microcontroller. For a system that *does not* include $D_{GND}$, it is required that $V_{OH} > V_{IH}$. For a system that *does* include $D_{GND}$, it is required that $V_{OH} > (V_{IH} + V_F)$. $V_F$ is the forward voltage of $D_{GND}$.

For use of the status pin, ST, a similar consideration is necessary. The designer must consider the $V_{OL,\ ST}$ specification and the $V_{IL}$ specification of the microcontroller. For a system that includes DGND, it is required that $V_{OL,\ ST} + V_F < V_{IL,\ \mu C}$.

The sense resistor, $R_{SNS}$, should be terminated to the microcontroller ground. In this case, the ADC can accurately measure the SNS signal even if there is an offset between the microcontroller ground and the device ground.

### 10.1.3 I/O Protection

$R_{PROT}$ is used to protect the microcontroller I/O pins during system-level voltage transients such as ISO pulses or reverse supply. A large resistance value ensures that current through the pin is limited to a safe level.

### 10.1.4 Inverse Current

Inverse current occurs when 0 V < $V_{BB}$ < $V_{OUT}$. In this case, current may flow from $V_{OUT}$ to $V_{BB}$. Inverse current cannot be caused by a purely resistive load. However, a capacitive or inductive load can cause inverse current. For example, if there is a significant amount of load capacitance and the $V_{BB}$ node has a transient droop, $V_{OUT}$ may be greater than $V_{BB}$.

TPS27SA08-Q1 device will not detect inverse current. When the switch is enabled, inverse current will pass through the switch. When the switch is disabled, inverse current may pass through the MOSFET body diode. The device will continue operating in the normal manner during an inverse current event.

### 10.1.5 Loss of GND

The ground connection may be lost either on the device level or on the module level. If the ground connection is lost, both switches will be disabled. If the switch was already disabled when the ground connection was lost, the switch will remain disabled. When the ground is reconnected, normal operation will resume.

### 10.1.6 Thermal Information

When outputting current, the TPS27SA08-Q1 device will heat up due to the power dissipation. Figure 10-2 shows the transient thermal impedance curve that can be used to determine the device temperature during 1-W pulse of a given length.

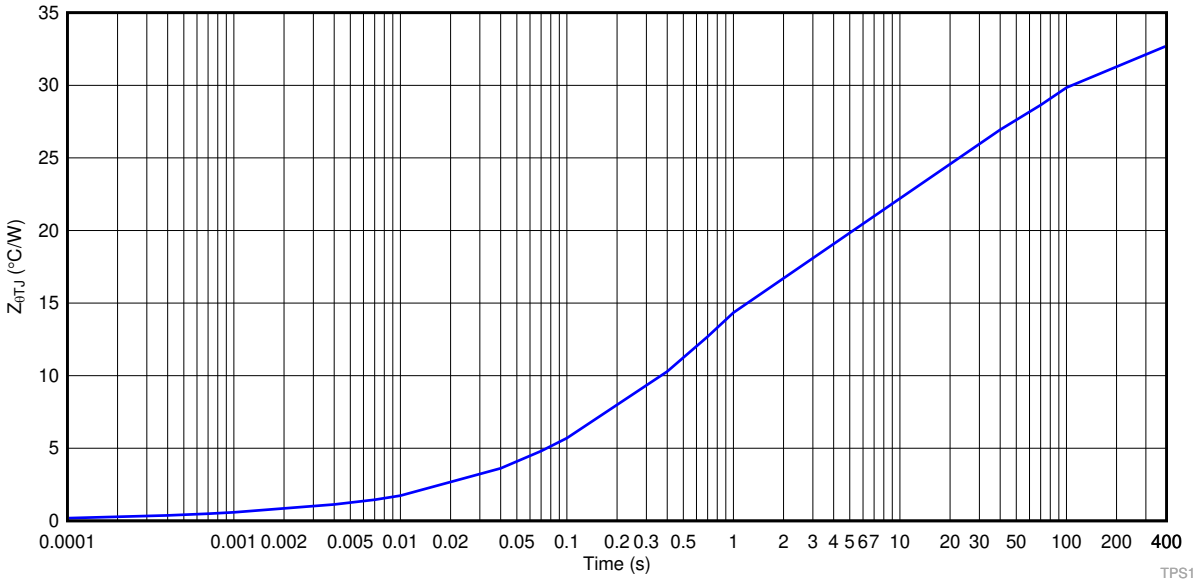



**Figure 10-2. Transient Thermal Impedance**

## 10.2 Typical Application

This application example demonstrates how the TPS27SA08-Q1 device can be used to power resistive heater loads as in seat heaters. Figure 10-3 shows a typical application where the load is a resistive seat heater. This document highlights the basics of this type of application, however for a more detailed discussion reference *TI's Smart Power Switch Seat Heater Reference Design*.

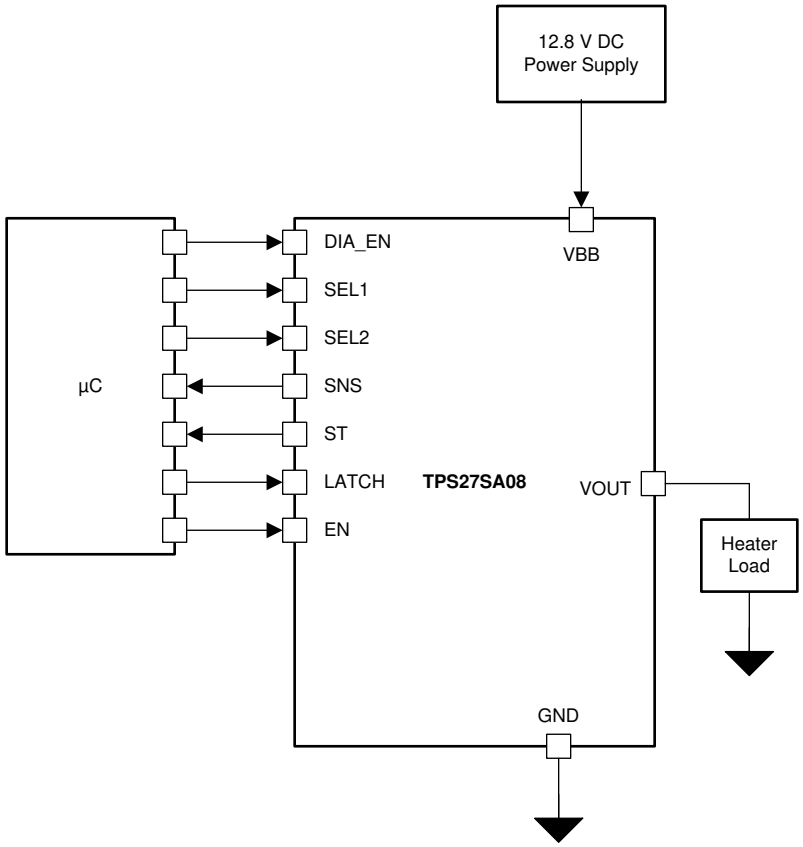



**Figure 10-3. Block Diagram for Powering Heater Loads**

### 10.2.1 Design Requirements

For this design example, use the input parameters shown in Table 10-2.

**Table 10-2. Design Parameters**

| DESIGN PARAMETER | EXAMPLE VALUE |
|---|---|
| $V_{BB}$ | 12.8 V |
| Heater Load | 90-W max |
| Load Current Sense | 100 mA to 20 A |
| Ambient temperature | 85°C |
| $R_{\theta JA}$ | 32.8°C/W (depending on PCB) |

### 10.2.2 Detailed Design Procedure

#### *10.2.2.1 Thermal Considerations*

The DC current under maximum load power condition will be around 7.03 A. Power dissipation in the switch is calculated in Equation 3. $R_{ON}$ is assumed to be 20 mΩ because this is the maximum specification. In practice, $R_{ON}$ will be lower.

$$P_{FET} = I^2 \times R_{ON} \quad (3)$$

$$P_{FET} = (7.03\ A)^2 \times 20\ m\Omega = 0.988\ W \quad (4)$$

The junction temperature of the device can be calculated using Equation 5 and the $R_{\theta JA}$ value from the *Specifications* section.

$$T_J = T_A + R_{\theta JA} \times P_{FET} \quad (5)$$

$T_J$ = 85°C + 32.8°C/W × 0.988 W = 117.4°C

The maximum junction temperature rating for TPS27SA08-Q1 device is $T_J$ = 150°C. Based on the above example calculation, the device temperature will stay below the maximum rating.

#### *10.2.2.2 Diagnostics*

If the resistive heating load is disconnected (heater malfunction), an alert is desired. Open-load detection can be performed in the switch-enabled state via the current sense feature of the TPS27SA08-Q1 device. Alternatively, under open load condition in off-state with diagnostics enabled, the current in the SNS pin will be the fault current and the can be detected from the sense voltage measurement.

##### 10.2.2.2.1 Selecting the $R_{ISNS}$ Value

Table 10-3 shows the requirements for the load current sense in this application. The $K_{SNS}$ value is specified for the device and can be found in the *Specifications* section.

**Table 10-3. $R_{SNS}$ Calculation Parameters**

| PARAMETER | EXAMPLE VALUE |
|---|---|
| Current Sense Ratio ($K_{SNS}$) | 4600 |
| Largest diagnosable load current | 20 A |
| Smallest diagnosable load current | 50 mA |
| Full-scale ADC voltage | 5 V |
| ADC resolution | 10 bit |

The load current measurement requirements of 20 A ensures that current can be sensed up to the 20-A current limit, while the low level of 100 mA allows for accurate measurement of low load currents.

The $R_{SNS}$ resistor value should be selected such that the largest diagnosable load current puts $V_{SNS}$ at about 90% of the ADC full-scale. With this design, any ADC value above 90% can be considered a fault. Additionally, the $R_{SNS}$ resistor value should ensure that the smallest diagnosable load current does not cause $V_{SNS}$ to fall below 1 LSB of the ADC. With the given example values, a 1-kΩ sense resistor satisfies both requirements shown in Table 10-4.

**Table 10-4. $V_{SNS}$ Calculation**

| LOAD (A) | SENSE RATIO | $I_{SNS}$ (mA) | $R_{SNS}$ (Ω) | $V_{SNS}$ (V) | % OF 5-V ADC |
|---|---|---|---|---|---|
| 0.050 | 4600 | 0.011 | 1000 | 0.011 | 0.22% |
| 20.000 | 4600 | 4.348 | 1000 | 4.348 | 87% |

### 10.2.3 Application Curves

Figure 10-4 shows the behavior of the TPS27SA08-Q1 device in this application when the MCU provides an enable pulse to beginning heating the resistive element. Shortly after the EN pin goes high, the load current begins to flow and the SNS pin measures the output current.

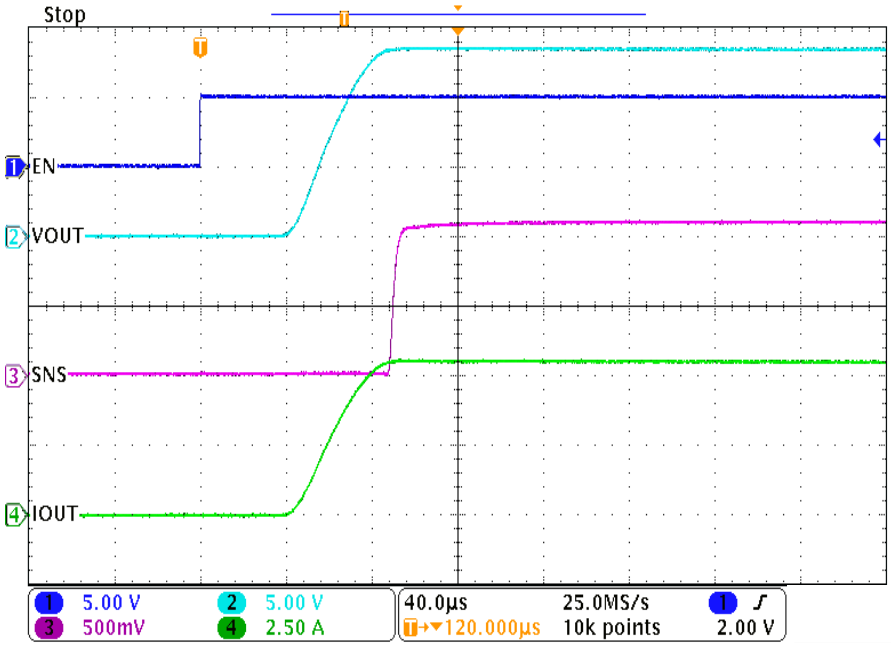



**Figure 10-4. Heater Turn-on Time**

By measuring the voltage on the SNS pin, the TPS27SA08-Q1 device can communicate back to the system MCU what the load current is. Figure 10-5 shows that when the seat heater approaches full load and $I_{OUT}$ jumps from a low load current of 1 A up to a 5-A load current, the load step is mirrored on the SNS pin.

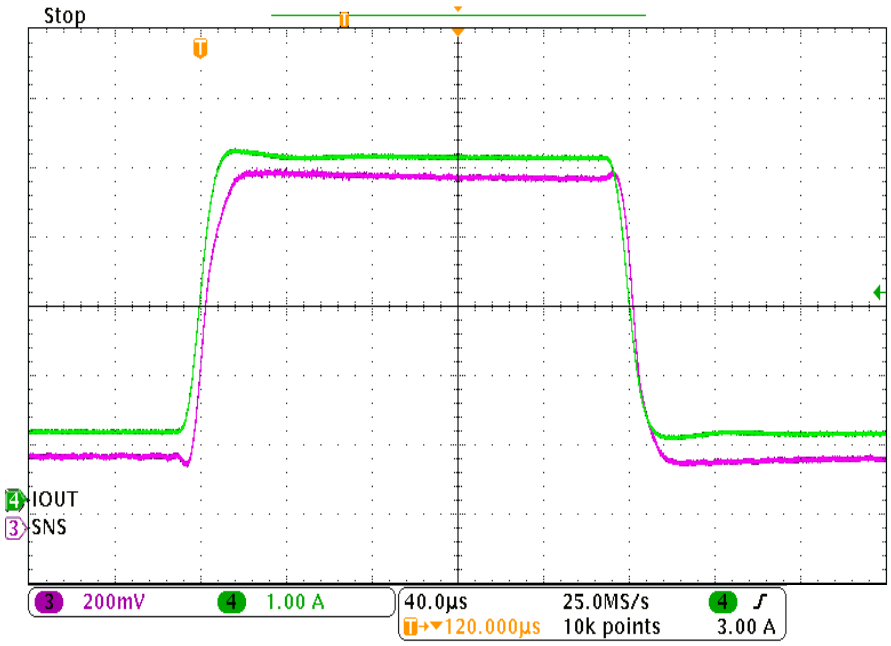



**Figure 10-5. SNS Response During Heater Load Step**

One common concern in these type of applications is that the heating element can accidentally lose connection, creating an open load situation. In this case, it is ideal for the TPS27SA08-Q1 device to recognize that the load has been removed and report a FLT to the MCU. Figure 10-6 shows the behavior of the TPS27SA08-Q1 device when there is no load attached. As soon as the DIAG_EN pin is engaged, the SNS output goes high and the $\overline{ST}$ output engages low. By monitoring these pins, the MCU can recognize there is a fault and notify the user that maintenance is required.

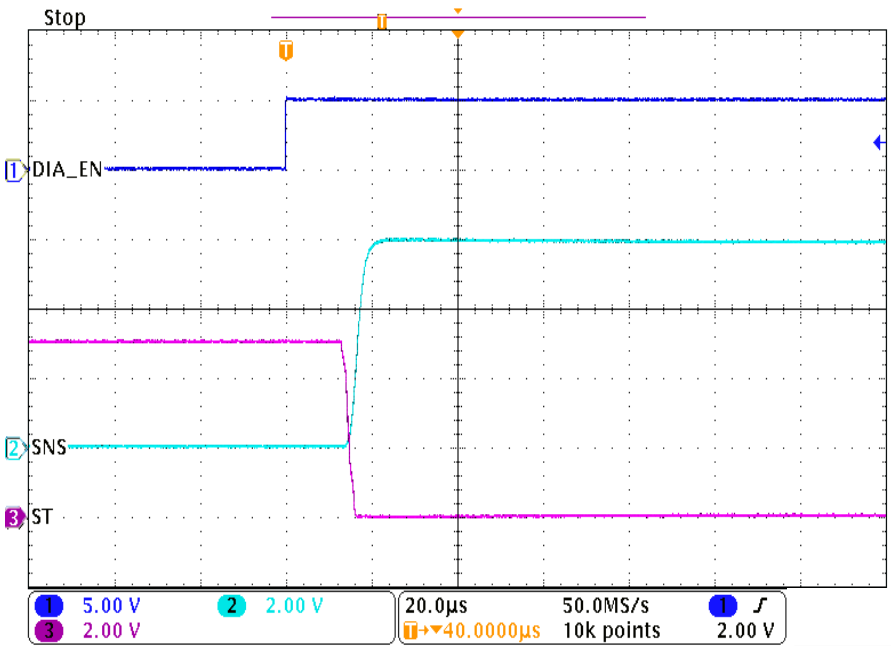



**Figure 10-6. Open Load Detection if Heating Element is Missing**

Importantly, the TPS27SA08-Q1 device will also protect the system in the event of a short-circuit. Figure 10-7 shows the behavior of the device if it is enabled into a short circuit condition. The current will be clamped to near the current limit threshold ($I_{CL}$) until it hits an over temperature event, at which point the FET will be turned off. In this way, the system is protected from unchecked overcurrent in the event of a short circuit.

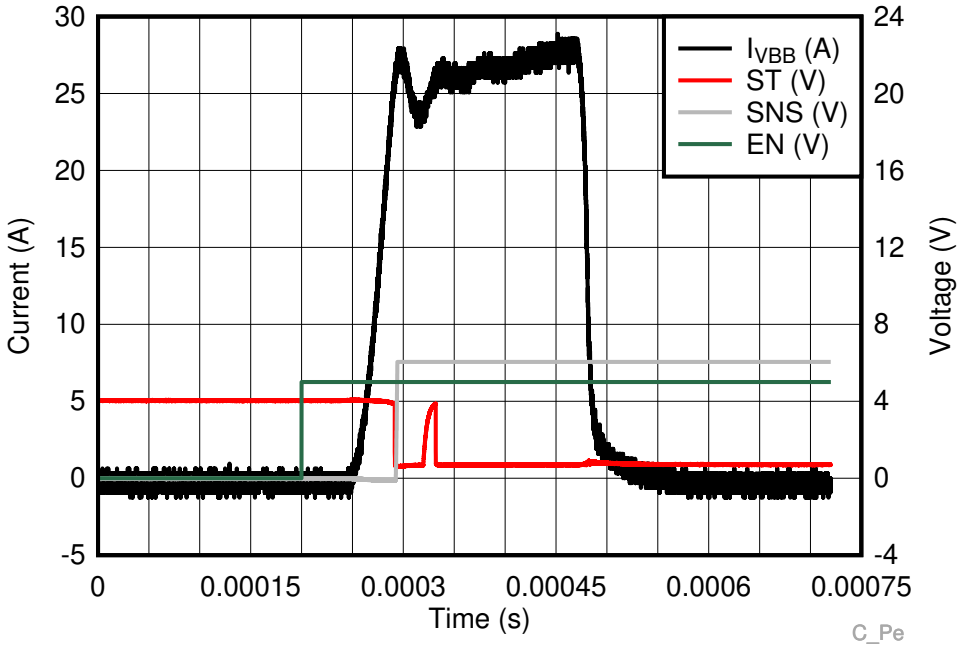



**Figure 10-7. Overcurrent Behavior During Short Circuit Event**

## 11 Power Supply Recommendations

The TPS27SA08-Q1 device is designed to operate in a 24-V system. The nominal supply voltage range is 8 V to 36 V. The device is also designed to withstand voltage transients beyond this range. When operating outside of the nominal voltage range, the device will exhibit normal functional behavior. However, parametric specifications may not be guaranteed.

# 12 Layout

## 12.1 Layout Guidelines

To achieve optimal thermal performance, connect the exposed pad to a large copper pour. On the top PCB layer, the pour may extend beyond the pad dimensions as shown in the example below. In addition to this, it is recommended to also have a $V_{BB}$ plane either on one of the internal PCB layers or on the bottom layer. Vias should connect this plane to the top $V_{BB}$ pour.

TPS27SA08-Q1 device has 6 $V_{OUT}$ pins. All $V_{OUT}$ pins must be shorted together on the PCB. Additionally, the layout should ensure that the current path is symmetrical for both sides of the device. If the path is not symmetrical, there will be some imbalance in current spreading across the power FET. This can impact accuracy of the current sense measurement.

## 12.2 Layout Example

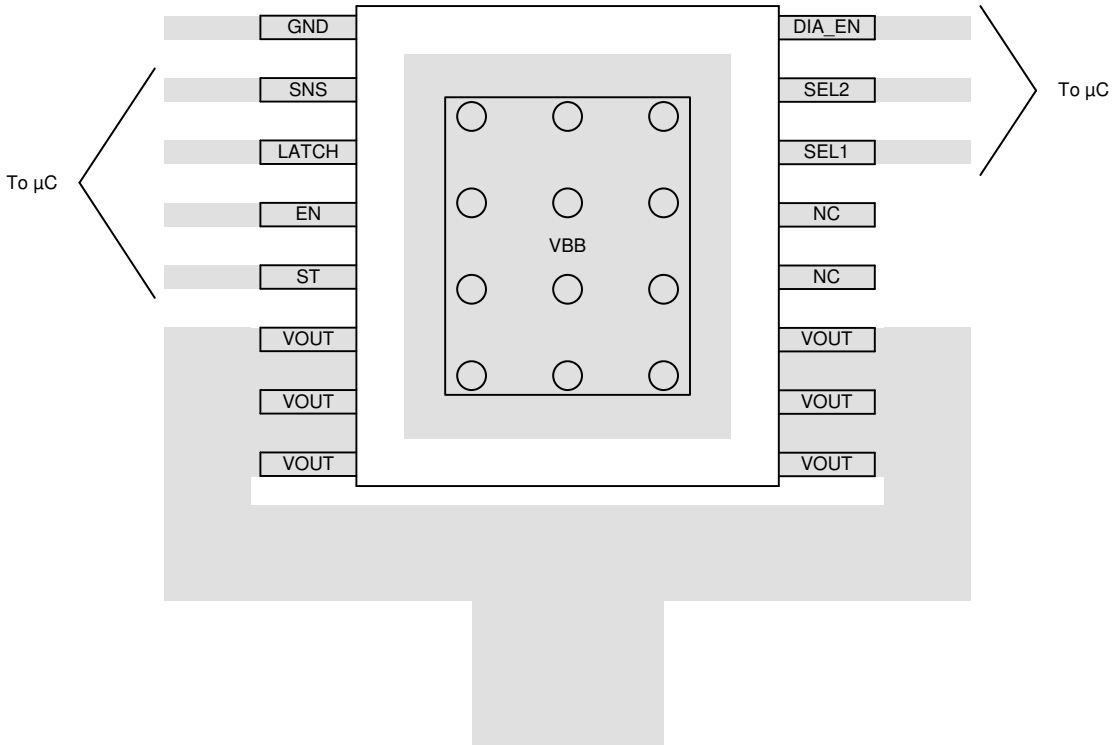



**Figure 12-1. PWP Layout Example**

# 13 Device and Documentation Support

## 13.1 Device Support

### 13.1.1 Related Documentation

For related documentation see the following:

- *TI's "How To Drive Inductive, Capacitive, and Lighting Loads with Smart High Side Switch*
- *Short Circuit Reliability Test for Smart Power Switches*
- *TI's Smart Power Switch Seat Heater Reference Design*
- *Reverse Battery Protection for High Side Switches*

## 13.2 Trademarks

All trademarks are the property of their respective owners.

## 13.3 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

## 13.4 Glossary

**TI Glossary** This glossary lists and explains terms, acronyms, and definitions.

## 14 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

## PACKAGING INFORMATION

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead finish/ Ball material (6) | MSL Peak Temp (3) | Op Temp (°C) | Device Marking (4/5) | Samples |
|---|---|---|---|---|---|---|---|---|---|---|---|
| TPS27SA08CQPWPRQ1 | ACTIVE | HTSSOP | PWP | 16 | 3000 | RoHS-Exempt & Green | NIPDAU | Level-3-260C-168HRS | -40 to 125 | 27A08QC | Samples |

(1) The marketing status values are defined as follows:
**ACTIVE:** Product device recommended for new designs.
**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.
**OBSOLETE:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

**OTHER QUALIFIED VERSIONS OF TPS27SA08-Q1 :**

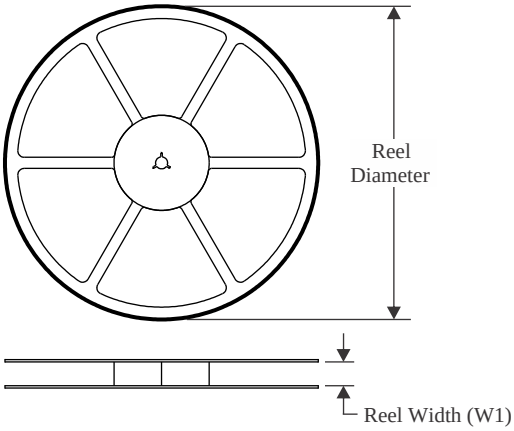
- Catalog: TPS27SA08

NOTE: Qualified Version Definitions:

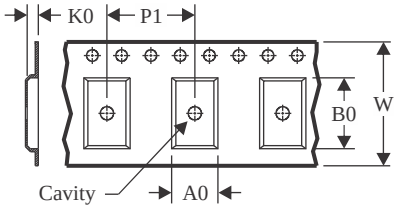
- Catalog - TI's standard catalog product

## TAPE AND REEL INFORMATION

**REEL DIMENSIONS**

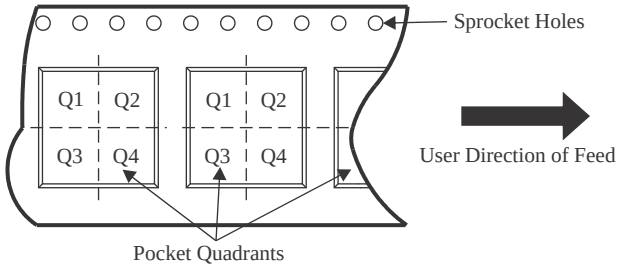



**TAPE DIMENSIONS**




| | |
|---|---|
| A0 | Dimension designed to accommodate the component width |
| B0 | Dimension designed to accommodate the component length |
| K0 | Dimension designed to accommodate the component thickness |
| W | Overall width of the carrier tape |
| P1 | Pitch between successive cavity centers |

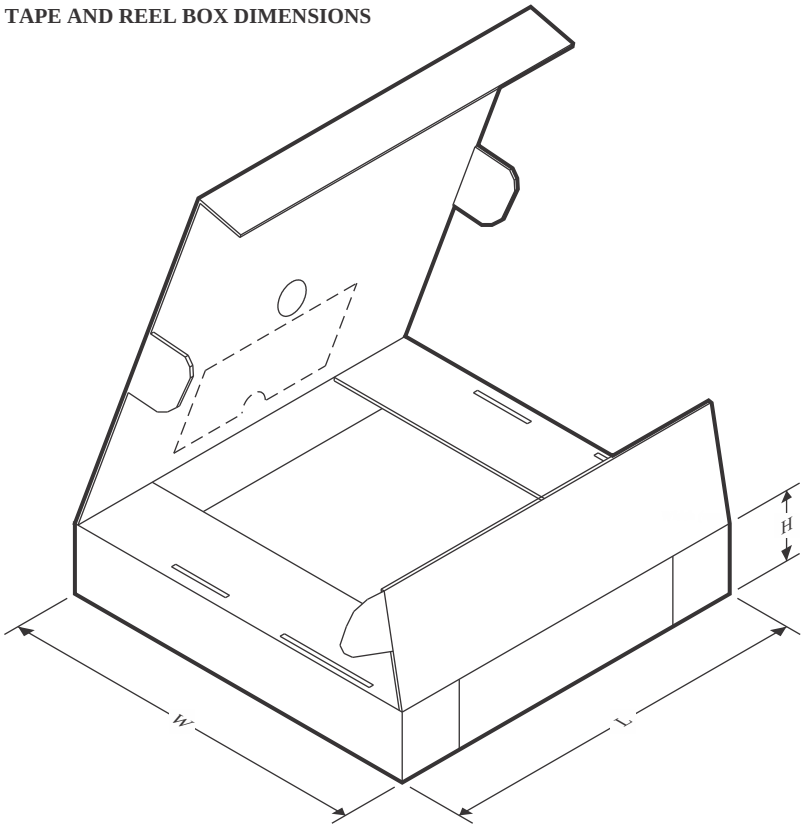
**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**




*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| TPS27SA08CQPWPRQ1 | HTSSOP | PWP | 16 | 3000 | 330.0 | 12.4 | 6.9 | 5.6 | 1.6 | 8.0 | 12.0 | Q1 |

TAPE AND REEL BOX DIMENSIONS

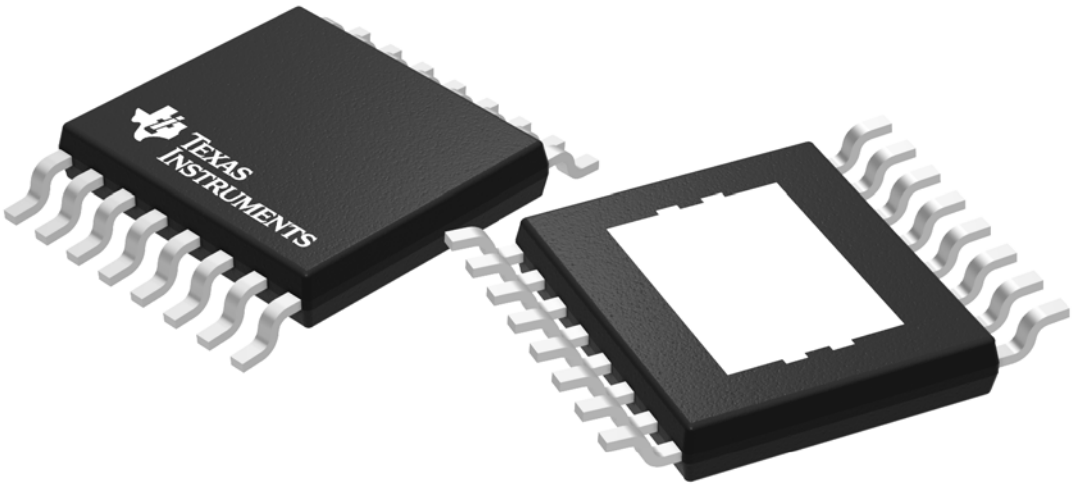



*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|---|---|---|---|---|---|---|---|
| TPS27SA08CQPWPRQ1 | HTSSOP | PWP | 16 | 3000 | 350.0 | 350.0 | 43.0 |

# PWP 16 PowerPAD™ TSSOP - 1.2 mm max height

PLASTIC SMALL OUTLINE



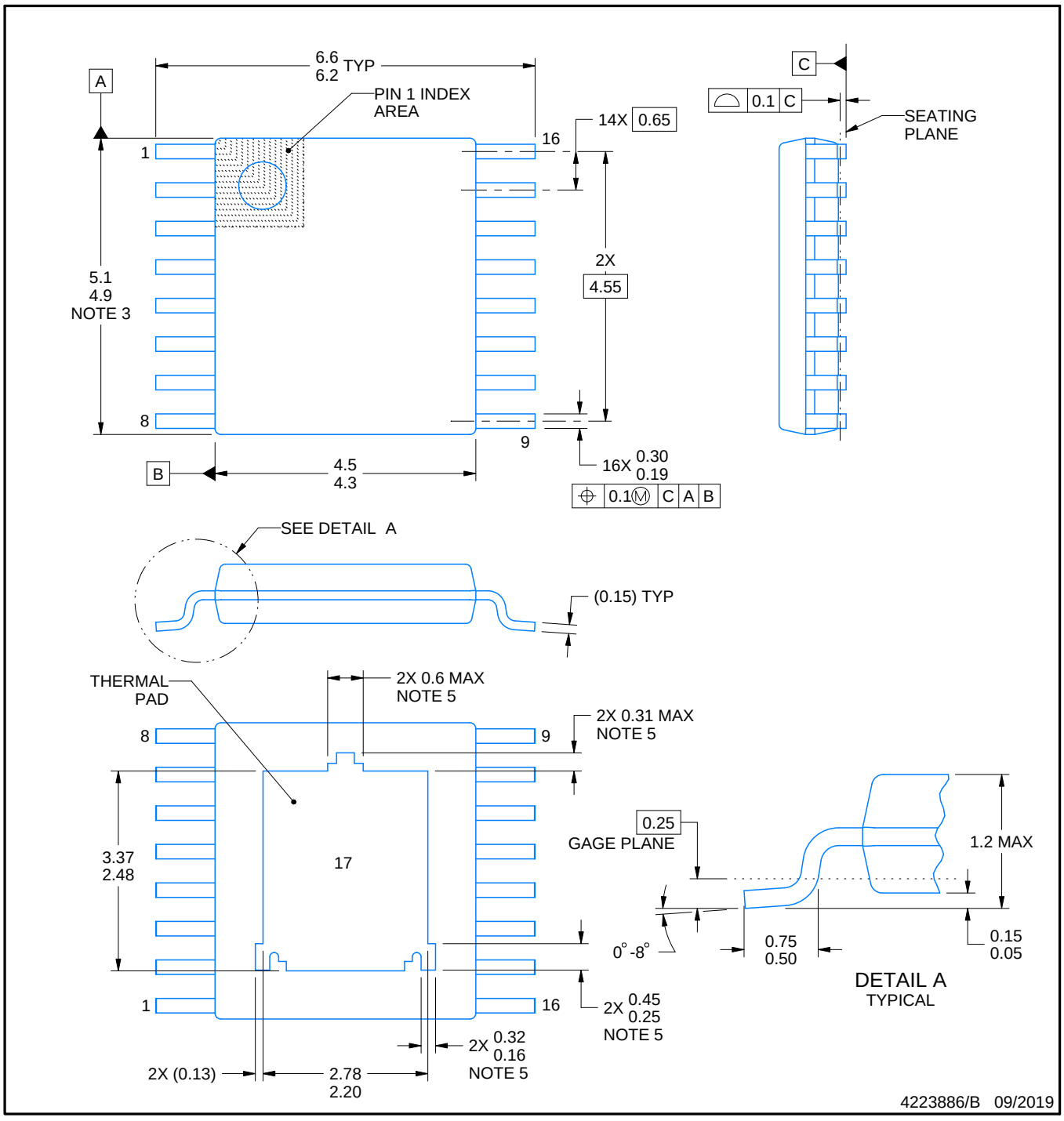

Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

# PACKAGE OUTLINE

## PWP0016M

## PowerPAD™ TSSOP - 1.2 mm max height

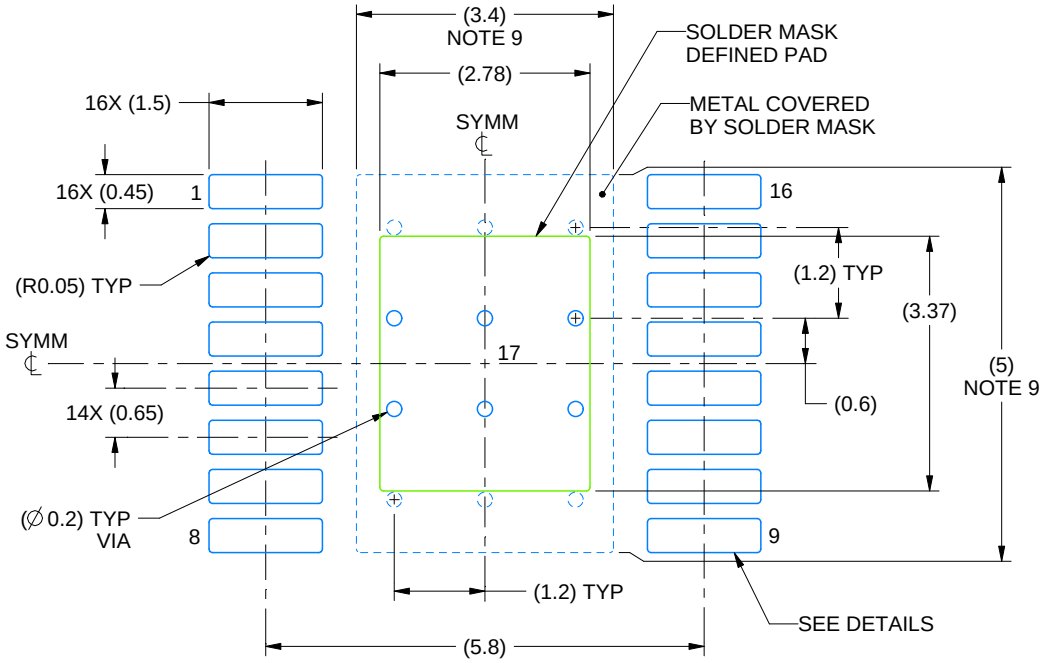
SMALL OUTLINE PACKAGE



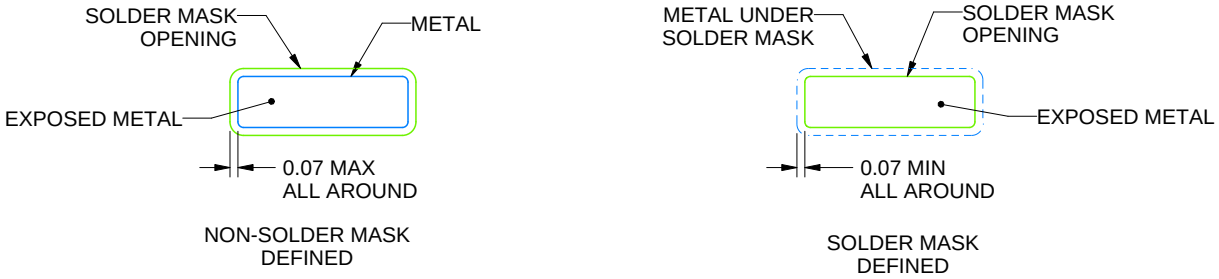

PowerPAD is a trademark of Texas Instruments.

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. Reference JEDEC registration MO-153.
5. Features may differ or may not be present.




LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X




SOLDER MASK DETAILS

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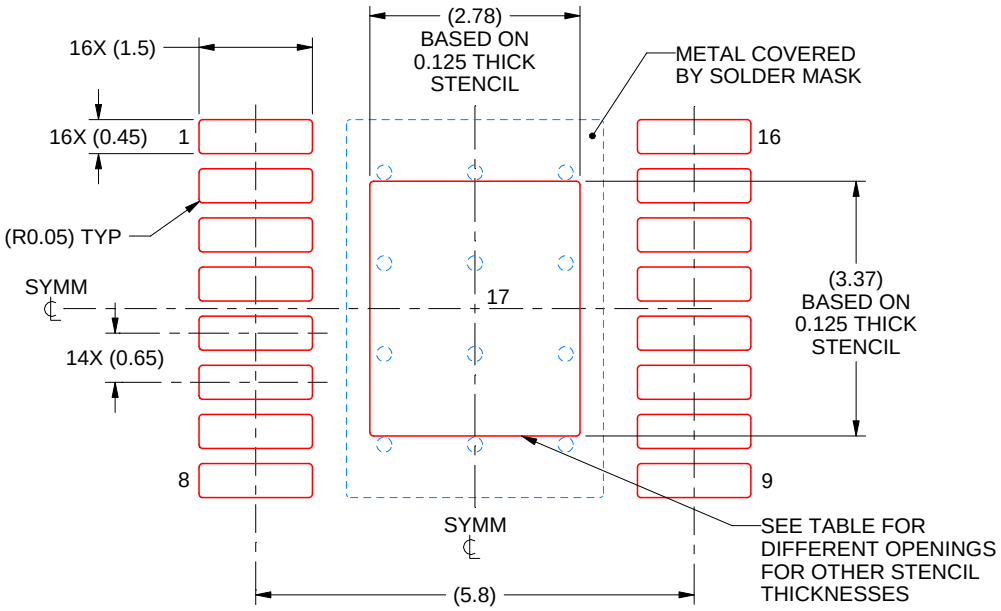
NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature numbers SLMA002 (www.ti.com/lit/slma002) and SLMA004 (www.ti.com/lit/slma004).
9. Size of metal pad may vary due to creepage requirement.
10. Vias are optional depending on application, refer to device data sheet. It is recommended that vias under paste be filled, plugged or tented.




SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

| STENCIL THICKNESS | SOLDER STENCIL OPENING |
|---|---|
| 0.1 | 3.11 X 3.77 |
| 0.125 | 2.78 X 3.37 (SHOWN) |
| 0.15 | 2.54 X 3.08 |
| 0.175 | 2.35 X 2.85 |

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NOTES: (continued)

11. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
12. Board assembly site may have different recommendations for stencil design.

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