TPS2HC08-Q1 9.5mΩ Dual-Channel Automotive Smart High-Side Switch

1 Features

- Dual-Channel smart high-side switch with full diagnostics
  - Control using GPIO pins
  - Open-drain status output
  - Current sense analog output: sense accuracy <±4% at ≥ 1A
- Wide operating voltage: 3V to 28V
- Low R_{ON}: 9.5mΩ typical, 16.5mΩ max at 150°C
- Ultra-low standby current: <1.4μA at 85°C
- Adjustable current limit with and without thermal regulation
  - Current limit range: 7.5A to 25A
- Protection
  - Overload and short-circuit protection
  - Undervoltage lockout (UVLO)
  - Thermal shutdown and swing with self recovery
  - Integrated output clamp to demagnetize inductive loads
  - Loss-of-GND, loss-of-battery, and reverse battery protection
- Diagnostics
  - Global fault report for fast interrupt
  - Overcurrent and short-to-ground detection
  - Open-load and short-to-battery detection
- Qualified for automotive applications
  - AEC-Q100 qualified with the following results:
    - Temperature grade 1: –40°C to 125°C ambient operating temperature range
  - Passed electrical transient disturbance immunity tests (ISO7637-2 and ISO16750-2)
- Small footprint: 11-pin wettable flank VQFN-HR 2.2mm × 3.6mm, 0.55mm pitch
- Functional Safety Capable
  - Documentation available to aid functional safety system design

2 Applications

- Zone control module
- Body control module
- Incandescent and LED lighting
- Front door module
- Seat heater

3 Description

TPS2HC08-Q1 is a dual-channel, smart high-side switch, with integrated NMOS power FETs and charge pump, designed for 12V automotive battery systems. The low on-resistance (9.5mΩ) minimizes device power dissipation when driving output load current up to 7.5A DC when both channels are enabled or 10A DC when only one channel is enabled.

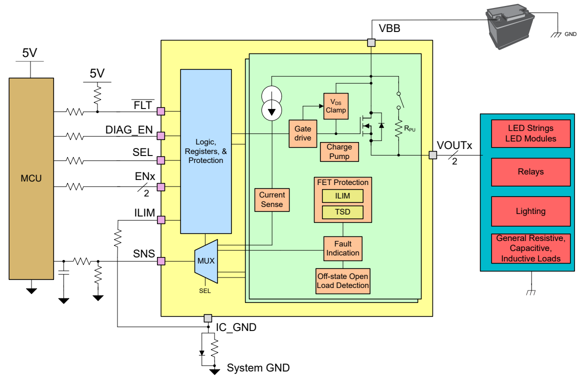
The device integrates protection features such as thermal shutdown, output clamp, and current limit. TPS2HC08-Q1 implements an adjustable current limiting circuit that improves the reliability of the system by reducing inrush current when driving large capacitive loads and minimizing overload current. The adjustable current limit can be adjusted from (7.5A to 25A) using an external resistor on the ILIM pin. The device offers both thermal-regulated current limiting for capacitive loads at startup and non-regulated current limiting for motor inrush or bulb applications.

The device also provides an accurate current sense that allows for improved load diagnostics such as overload and open-load detection, enabling better predictive maintenance. TPS2HC08-Q1 is available in a 11-pin, 2.2mm × 3.6mm VQFN-HR wettable-flank package with 0.55mm pitch, minimizing the PCB footprint.

Package Information

PART NUMBER	PACKAGE(1)	PACKAGE SIZE(2)
TPS2HC08-Q1	VAH (VQFN-HR, 11)	2.2mm × 3.6mm

(1) See the orderable addendum at the end of the data sheet.
(2) The package size is a nominal value and includes pins.



Typical Application Schematic

Table of Contents

1 Features............1
2 Applications............1
3 Description............1
4 Device Comparison Table............3
5 Pin Configuration and Functions............4
6 Specifications............5
6.1 Absolute Maximum Ratings............5
6.2 ESD Ratings............5
6.3 Recommended Operating Conditions............5
6.4 Thermal Information............6
6.5 Electrical Characteristics............6
6.6 SNS Timing Characteristics............9
6.7 Switching Characteristics............10
6.8 Typical Characteristics............11
7 Parameter Measurement Information............17
8 Detailed Description............18
8.1 Overview............18
8.2 Functional Block Diagram............19
8.3 Feature Description............20
8.4 Device Functional Modes............56
9 Application and Implementation............58
9.1 Application Information............58
9.2 Typical Application............58
9.3 Power Supply Recommendations............63
9.4 Layout............63
10 Device and Documentation Support............67
10.1 Third-Party Products Disclaimer............67
10.2 Receiving Notification of Documentation Updates..67
10.3 Support Resources............67
10.4 Trademarks............67
10.5 Electrostatic Discharge Caution............67
10.6 Glossary............67
11 Revision History............67
12 Mechanical, Packaging, and Orderable Information............68

4 Device Comparison Table

TPS2HC08-Q1 is part of a high current, smart high-side switch family, which has multiple device versions. The following tables shows the details of the versions and which versions are going to be available for each device.

Table 4-1. Version Table

VERSION[(2)]	SLEW RATE	OPEN LOAD DETECTION DELAY
P	Nominal (0.45V/µs)	0.4ms delay
M[(1)]	Nominal (0.45V/µs)	2.4ms delay
D[(1)]	Slow (0.06V/µs)	0.4ms delay
B[(1)]	Slow (0.06V/µs)	2.4ms delay

(1) Device in preview. Please contact TI for more information.
(2) All versions are GPIO controlled.

Table 4-2. Device Comparison Table

PART NUMBER	PLANNED VERSIONS	NUMBER OF CHANNELS	ON-RESISTANCE at 25°C	ADJUSTABLE CURRENT LIMIT RANGE	OVERCURRENT BEHAVIOR
TPS2HC08-Q1	P, D, M, B	2	9.5mΩ	7.5A - 25A	• Current limiting with thermal regulation when external resistor is used on ILIM pin • Current limiting with no thermal regulation when ILIM pin = GND
TPS2HC16-Q1	P, M	2	18.7mΩ	5A - 15A	
TPS1HC08-Q1	P, D, M	1	9.8mΩ	10A - 20A	
TPS1HC04-Q1	P, D	1	4.9mΩ	15A - 48A	
TPS1HC03-Q1	P, D, M	1	3.2mΩ	20A - 55A	
TPS1HC16-Q1	P	1	16mΩ	7A - 14A	
TPS2HC30-Q1	P	2	30mΩ	3.5A - 11A	

5 Pin Configuration and Functions

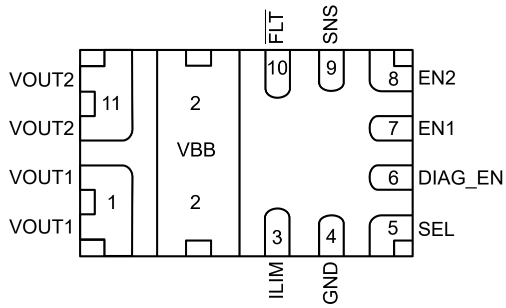


Figure 5-1. VAH (VQFN-HR-11 Package, TPS2HC08-Q1 (top view)

Table 5-1. Pin Functions

PIN		TYPE	DESCRIPTION
NO.	NAME		
1	VOUT1	Power	Channel 1 output, connect to load.
2	VBB	Power	Power supply.
3	ILIM	Output	Adjustable current limit. Connect R_{LIM} to GND to set the current limit.
4	GND	Power	Ground of device. Connect to resistor-diode ground network to have reverse battery protection.
5	SEL	Input	Selects the channel to output on the SNS pin.
6	DIAG_EN	Input	Enable-disable pin for diagnostics, internal pulldown.
7	EN1	Input	Input control for channel 1 activation, internal pulldown.
8	EN2	Input	Input control for channel 2 activation, internal pulldown.
9	SNS	Output	Analog current sense output corresponding to load current. Connect R_{SNS} to ground to convert to a voltage. Also shows fault status by going high.
10	$\overline{FLT}$	Output	Open drain global fault output. Referred to FAULT, FLT, or fault pin.
11	VOUT2	Power	Channel 2 output, connect to load.

6 Specifications

6.1 Absolute Maximum Ratings

Over operating free-air temperature range (unless otherwise noted)[(1)]

		MIN	MAX	UNIT
Maximum continuous supply voltage, VBB			28	V
Load dump voltage, V_{LD}	ISO16750-2:2010(E)		35	V
Reverse Polarity Voltage	Maximum duration of 3 minutes and with the application circuit	–18		V
Enable pin current, I_{ENx}		–1	20	mA
Enable pin voltage, V_{ENx}		–1	7	V
Diagnostic Enable pin current, I_{DIAG_EN}		–1	20	mA
Diagnostic Enable pin voltage, V_{DIAG_EN}		–1	7	V
SEL pin current, I_{SEL}		–1	20	mA
SEL pin voltage, V_{SEL}		–1	7	V
Sense pin current, I_{SNS}		–150	10	mA
FLT pin current, I_{FLT}		-30	10	mA
FLT pin voltage, V_{FLT}		–0.3	VBB	V
ILIM pin current, I_{ILIM}		-30	10	mA
ILIM pin voltage, V_{ILIM}		–0.3	VBB	V
Reverse ground current, I_{GND}	V_{BB} < 0V		–50	mA
Energy dissipation during turnoff, E_{AS}	Single pulse, one channel, VBB = 13.5V, L_{OUT} = 5mH, $T_{J,start}$ = 125°C, nominal slew rate (version P)		96[(2)]	mJ
Energy dissipation during turnoff, E_{AR}	Repetitive pulse, one channel, 13.5V, I_{OUT} = 10A, $T_{J,start}$ = 125°C, nominal slew rate (version P)		13[(2)]	mJ
Maximum junction temperature, T_J			150	°C
Storage temperature, T_{stg}		–65	150	°C

(1) Operation outside the Absolute Maximum Ratings may cause permanent device damage. Absolute Maximum Ratings do not imply functional operation of the device at these or any other conditions beyond those listed under Recommended Operating Conditions. If used outside the Recommended Operating Conditions but within the Absolute Maximum Ratings, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.
(2) For further details, see the section regarding switch-off of an inductive load.

6.2 ESD Ratings

				VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge[(1)]	Human-body model (HBM), per AEC Q100-002 Classification Level 2[(2)]	All pins except VBB and VOUT	±2000	V
			VBB and VOUT	±4000	
		Charged-device model (CDM), per AEC Q100-011 Classification Level C5	All pins	±750	

(1) All ESD strikes are with reference from the pin mentioned to GND
(2) AEC-Q100-002 indicates that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specifications.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted) [(1)]

		MIN	MAX	UNIT
V_{VBB_NOM}	Nominal supply voltage [(1)]	4	18	V
V_{VBB_EXT}	Extended supply voltage[(2)]	3	28	V

6.3 Recommended Operating Conditions (continued)

over operating free-air temperature range (unless otherwise noted) [1]

		MIN	MAX	UNIT
V_{VBB_SC}	Short circuit supply voltage capability		24	V
V_{ENx}	Enable voltage	–1	5.5	V
V_{DIAG_EN}	Diagnostic Enable voltage	–1	5.5	V
V_{SEL}	Select voltage	–1	5.5	V
V_{SNS}	Sense voltage	–1	5.5	V
T_A	Operating free-air temperature	–40	125	°C

(1) All operating voltage conditions are measured with respect to device GND
(2) Device will function within extended operating range, however some timing parametric values might not apply. See the respective sections for what voltages are used. Additionally more explanation can be found in Power Supply Recommendations

6.4 Thermal Information

THERMAL METRIC [1] [2]		TPS2HC08-Q1 VAH 11 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	41.6	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	37.3	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	9.3	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	1.9	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	9.3	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	9.8	°C/W

(1) For more information about traditional and new thermal metrics, see the SPRA953 application report.
(2) The thermal parameters are based on a 4-layer PCB according to the JESD51-5 and JESD51-7 standards.

6.5 Electrical Characteristics

V_{BB} = 6V to 18V, T_J = –40°C to 150°C (unless otherwise noted); Typical application is V_{BB} = 13.5V, R_{LIM} = Open (unless otherwise specified)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
INPUT VOLTAGE AND CURRENT							
V_{UVLOR}	V_{BB} undervoltage lockout	Measured with respect to device GND pin	V_{BB} rising threshold	3.7	3.85	4.0	V
V_{UVLOF}			V_{BB} falling threshold	2.8	2.9	3.0	V
V_{DET1}	V_{BB} detection 1 threshold	Active, diagnostic, or standby state	V_{BB} rising threshold	19	20.5	22.5	V
			V_{BB} falling threshold	18.4	19.5	20.7	V
V_{DET2}	VBB detection 2 threshold	active state	V_{BB} rising threshold	24.5	26	28	V
			V_{BB} falling threshold	22.5	24	26	V
V_{HV_R}	VBB high voltage wake-up threshold	V_{BB} voltage to transition from sleep to standby state	V_{BB} rising threshold	20.9	25	28.1	V
V_{HV_F}	VBB high voltage wake-up threshold	V_{BB} voltage to transition from standby to sleep state	V_{BB} falling threshold	18			V
V_{Clamp}	VDS clamp voltage	$V_{BB} \geq V_{DET1}$	T_J = 25°C	35		37	V
			T_J = –40°C to 150°C	31		42	V
		$V_{BB} < V_{DET1}$	T_J = –40°C to 150°C	24		35	V

6.5 Electrical Characteristics (continued)

V_{BB} = 6V to 18V, T_J = –40°C to 150°C (unless otherwise noted); Typical application is V_{BB} = 13.5V, R_{LIM} = Open (unless otherwise specified)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
I_{SLEEP}	Standby current (total device leakage including both MOSFET channels)	V_{ENx} = V_{DIAG_EN} = 0V, V_{OUT} = 0V	T_J = 25°C			1.2	µA
			T_J = 85°C			1.4	µA
			T_J = 150°C			12	µA
$I_{OUT(SLEEP)}$	Output leakage current per channel	V_{EN} = V_{DIAG_EN} = 0V, V_{OUT} = 0V	T_J = 25°C		0.01	0.5	µA
			T_J = 85°C			0.7	µA
			T_J = 150°C			6	µA
I_{DIAG}	Diagnostic state current consumption	V_{ENx} = 5V, V_{DIAG_EN} = 0V, V_{OUT} = 0V, I_{SNS} = 0mA			1.9	2.4	mA
		V_{ENx} = 0V, V_{DIAG_EN} = 5V, V_{OUT} = 0V, I_{SNS} = 0mA			1.9	2.4	mA
I_{Q_1CH}	Quiescent current, one channel enabled	V_{EN} = V_{DIA_EN} = 5V, I_{OUT} = 0A				3	mA
I_Q	Quiescent current both channels enabled	V_{EN} = V_{DIA_EN} = 5V, I_{OUT} = 0A				3.2	mA
t_{STBY}	Standby mode delay time	V_{ENx} = V_{DIAG_EN} = 0V, V_{BB} < V_{HV_F} to standby		13	16	19	ms
RON CHARACTERISTICS							
R_{ON}	On-resistance	3V ≤ V_{BB} ≤ 28V, I_{OUT}= 1A	T_J = 25°C		9.5	11	mΩ
			T_J = 150°C			16.5	mΩ
ΔR_{ON}	Delta On-resistance between channels	6V ≤ V_{BB} ≤ 28V, I_{OUT}= 1A	T_J= -40°C to 150°C		0.5	5	%
$R_{ON(REV)}$	On-resistance during reverse polarity	-18V ≤ V_{BB} ≤ -6V	T_J = 25°C		9.5	11	mΩ
			T_J = 150°C			16.8	mΩ
IL_{NOM}	Continuous load current, per channel	Two channels enabled, T_A = 85°C			7.5		A
		One channel enabled, T_A = 85°C			10		A
V_F	Source-to-drain body diode voltage	V_{EN} = 0 V I_{OUT} = –1 A		0.15	0.6	0.8	V
CURRENT SENSE CHARACTERISTICS							
V_{BB_ISNS}	V_{BB} headroom needed for full current sense and fault functionality(2)	V_{DIAG_EN} = 3.3V		5.3			V
		V_{DIAG_EN} = 5V		6.5			V
K_{SNS}	Current sense ratio I_{OUT} / I_{SNS}	I_{OUT} = 1A			3008		
K_{SNS}	Current sense ratio I_{OUT} / I_{SNS} across I_{OUT}	V_{BB} > V_{BB_ISNS}, V_{EN} = V_{DIAG_EN} = 5V	I_{OUT} = 5A		3020		
				-3.5		4	%
			I_{OUT} = 2A		3016		
				-3.5		4	%
			I_{OUT} = 1A		3008		
				-4.5		4.5	%
			I_{OUT} = 500mA		2990		
				-9.5		8.5	%
			I_{OUT} = 200mA		2931		
				-24		19	%
I_{SNSFH}	I_{SNS} fault high-level	V_{DIAG_EN} > $V_{IH,DIAG\_EN}$		5.5	7.4	9.5	mA
$I_{SNSleak\_disabled}$	I_{SNS} leakage (Diagnostics disabled)	V_{DIA_EN} = 0 V	Force 0V on SNS Pin	-100	1	100	nA
CURRENT LIMIT CHARACTERISTICS							

6.5 Electrical Characteristics (continued)

V_{BB} = 6V to 18V, T_J = –40°C to 150°C (unless otherwise noted); Typical application is V_{BB} = 13.5V, R_{LIM} = Open (unless otherwise specified)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
R_{LIM}	R_{LIM} Short Circuit Detection Range				20		kΩ
	R_{LIM} Open Detection Range				66.66		kΩ
$I_{CL\_FLT\_Trip}$	Ratio of Current at which fault assertion happens to actual current limit[2]	T_J = –40°C to 150°C	R_{LIM} = 20 kΩ to 66.5 kΩ	74	80		%
K_{CL}	Current Limit Ratio[1]	T_J = –40°C to 150°C	R_{LIM} = 20kΩ	405	500	635	A × kΩ
			R_{LIM} = 33.2kΩ	405	500	635	A × kΩ
			R_{LIM} = 66.5kΩ	405	500	635	A × kΩ
I_{CL}	I_{CL} Current Limit Threshold	T_J = –40°C to 150°C	R_{LIM} = GND		25		A
			R_{LIM} = OPEN		7.5		A
I_{CB}	Peak current threshold when short is applied while switch enabled[2]	R_{LIM} = 16.9kΩ to 66.5kΩ	T_J = –40°C	23			A
			T_J = 25°C		25		A
			T_J = 150°C	22			A
I_{CL_HV}	I_{CL} current limit derating at high voltage[2]	T_J = –40°C to 150°C	$V_{BB} < V_{DET1}$		I_{CL}		A
			$V_{DET1} \leq V_{BB} < V_{DET2}$		$(I_{CL})/2$	20	
			$V_{BB} \geq V_{DET2}$		$(I_{CL})/3$	10	
I_{CL_LNPK}	Linear mode peak[2]	T_J = –40°C to 150°C	$R_{LIM} \geq$ 24.9kΩ			1.45 × I_{CL}	A
			R_{LIM} < 24.9kΩ		1.45 × I_{CL}	I_{CB}	A
FAULT CHARACTERISTICS							
V_{OL}	Open-load detection voltage (VBB - V_{OUTx} voltage)	V_{EN} = 0V, V_{DIAG_EN} = 5V, diagnostic state		1.5	2.2	2.9	V
R_{PU}	Open-load (OL) detection internal pull-up resistor per channel	V_{EN} = 0V, V_{DIAG_EN} = 5V, diagnostic state, (VBB - V_{OUTx} = 2.7V)			90		kΩ
t_{OL}	Open-load (OL) detection deglitch time	V_{EN} = 0V, V_{DIAG_EN} = 5V, When $V_{BB} - V_{OUT} < V_{OL}$, duration longer than t_{OL}		200		550	µs
t_{OL1}	OL and STB indication-time from EN falling	V_{EN} = 5V to 0V, V_{DIAG_EN} = 5V, I_{OUT} = 0mA, V_{OUT} = V_{BB} - V_{OL}		200		550	µs
t_{OL2}	OL and STB indication-time from DIAG_EN rising	V_{EN} = 0V, V_{DIAG_EN} = 0V to 5V, I_{OUT} = 0mA, V_{OUT} = V_{BB} - V_{OL}		200		4050	µs
T_{ABS}	Thermal shutdown[2]			150	165	180	°C
T_{REL}	Relative thermal shutdown				85		°C
T_{HYS}	Thermal shutdown hysteresis				28		°C
$V_{\overline{FLT}}$	$\overline{FLT}$ low output voltage	$I_{\overline{FLT}}$ = 2.5mA				0.2	V
$t_{FAULT\_\overline{FLT}}$	Fault indication-time[2]	V_{DIAG_EN} = 5V, time between fault and $\overline{FLT}$ asserting				20	µs
t_{FAULT_SNS}	Fault indication-time[2]	V_{DIAG_EN} = 5V, time between fault and I_{SNS} settling at I_{SNSFH}				30	µs
t_{RETRY_WINDOW}	Initial retry time window				40		ms
$t_{RETRY, INT}$	Retry time in initial retry window	Time from thermal shutdown to switch re-enable		100	160	300	µs
$t_{RETRY,EXTD}$	Retry time in extended overcurrent window			50	80	150	ms

6.5 Electrical Characteristics (continued)

V_{BB} = 6V to 18V, T_J = –40°C to 150°C (unless otherwise noted); Typical application is V_{BB} = 13.5V, R_{LIM} = Open (unless otherwise specified)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
EN PIN CHARACTERISTICS						
$V_{IL, ENx}$	Input voltage low-level	No GND Network			0.8	V
$V_{IH, ENx}$	Input voltage high-level	No GND Network	1.5			V
$V_{IHYS, ENx}$	Input voltage hysteresis			320		mV
R_{ENx}	Internal pulldown resistor		150	200	500	kΩ
$I_{IL,\_ENx}$	Input current low-level(2)	V_{ENx} = 0.8V	1.6	4	5.5	μA
$I_{IH, ENx}$	Input current high-level(2)	V_{ENx} = 5V	19	25	35	μA
DIAG_EN PIN CHARACTERISTICS						
$V_{IL, DIAG\_EN}$	Input voltage low-level	No GND Network			0.8	V
$V_{IH, DIAG\_EN}$	Input voltage high-level	No GND Network	1.5			V
$V_{IHYS, DIAG\_EN}$	Input voltage hysteresis			320		mV
R_{DIAG_EN}	Internal pulldown resistor		100	200	500	kΩ
$I_{IL, DIAG\_EN}$	Input current low-level(2)	V_{DIAG_EN} = 0.8V	1.6	4	5.5	μA
$I_{IH, DIAG\_EN}$	Input current high-level(2)	V_{DIAG_EN} = 5V	19	25	35	μA
SEL PIN CHARACTERISTIC						
$V_{IL, SEL}$	Input voltage low-level	No GND Network			0.8	V
$V_{IH, SEL}$	Input voltage high-level	No GND Network	1.5			V
$V_{IHYS, SEL}$	Input voltage hysteresis			320		mV
R_{SEL}	Internal pulldown resistor		100	350	500	kΩ
$I_{IL, SEL}$	Input current low-level(2)	V_{SEL} = 0.8V	1.7	2.3	3.3	μA
$I_{IH, SEL}$	Input current high-level(2)	V_{SEL} = 5V	11	14	20	μA

(1) To calculate I_{CL} from K_{CL} use equation $I_{CL} = K_{CL} / R_{LIM}$
(2) Parameter specified by design; not subject to production test.

6.6 SNS Timing Characteristics

V_{BB} = 6V to 18V, V_{ENx} = 5V, V_{DIAG_EN} = 5V, R_{SNS} = 1kΩ, T_J = –40°C to +150°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
SNS TIMING - CURRENT SENSE						
$t_{SNSION1}$	Settling time from rising edge of DIAG_EN	V_{DIAG_EN} = 0V to 5V, I_{OUTx} = 1A			20	μs
		V_{DIAG_EN} = 0V to 5V, I_{OUTx} = 50mA			20	μs
$t_{SNSION2}$	Settling time from rising edge of EN and DIAG_EN, 50% of V_{DIAG_EN}, V_{EN} to 90% of I_{SNS}	$V_{EN} = V_{DIAG\_EN}$ = 0V to 5V, I_{OUTx} = 1A			170	μs
		$V_{EN} = V_{DIAG\_EN}$ = 0V to 5V, I_{OUTx} = 50mA			170	μs
$t_{SNSION3}$	Settling time from rising edge of EN with DIAG_EN = 5V, 50% of V_{EN} to 90% of I_{SNS}	V_{ENx} = 0V to 5V, V_{DIAG_EN} = 5V, I_{OUTx} = 1A			110	μs
$t_{SNSIOFF}$	Settling time from falling edge of DIAG_EN, 50% of V_{DIAG_EN} to 5% of I_{SNS}	V_{ENx} = 5V, V_{DIAG_EN} = 5V to 0V , I_{OUTx} = 1A			10	μs
$t_{SETTLEH}$	Settling time from rising edge of load step	I_{OUTx} = 50mA to 1A			20	μs
$t_{SETTLEL}$	Settling time from falling edge of load step	I_{OUTx} = 1A to 50mA			20	μs
t_{MUX1}	Settling time from switching from CHx to CHy	V_{SEL} = 0V to 5V, I_{OUT1} = 50mA, I_{OUT2} = 1A			20	μs
t_{MUX2}	Settling time from switching from CHx to CHy with any fault	V_{EN1} = 5V, V_{EN2} = 0V, V_{SEL} = 0V to 5V, I_{OUT1} = 1A, CH2 = I_{SNSFH}			20	μs

6.7 Switching Characteristics

V_{BB} = 13.5V, R_L = 10Ω, T_J = –40°C to +150°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{DR}	Channel Turn-on delay time	50% of ENx to 20% of VOUTx from standby state	6	12	30	μs
		50% of ENx to 20% of VOUTx from sleep state	10	45	70	μs
t_{DF}	Channel Turn-off delay time	50% of ENx to 80% of VOUTx	35	80	121	μs
SR_R	VOUT rising slew rate	20% to 80% of VOUTx (version = D, B)	0.02	0.06	0.1	V/μs
		20% to 80% of VOUTx (version = P, M)	0.3	0.45	0.65	V/μs
SR_F	VOUT falling slew rate	80% to 20% of VOUTx (version = D, B)	0.02	0.06	0.1	V/μs
		80% to 20% of VOUTx (version = P, M)	0.3	0.5	0.7	V/μs
t_{ON}	Channel Turn-on time	50% of EN to 80% of VOUT, from sleep state	35	60	110	μs
		50% of EN to 80% of VOUT, from standby state	15	30	90	μs
t_{OFF}	Channel Turn-off time	50% of EN to 20% of VOUT	50	90	130	μs
$t_{ON} - t_{OFF}$	Turn-on and off matching(1)	1ms enable pulse	–75		40	μs
		200μs enable pulse	-90		40	μs
Δ_{PWM}	PWM accuracy - average load current(1)	200μs enable pulse (1ms period)	–45		25	%
		≤500Hz, 50% Duty cycle	–12		12	%
E_{ON}	Switching energy losses during turn-on	V_{BB} = 18V, R_L = 3.3Ω, 0% to 100% of VOUT		0.63		mJ
		V_{BB} = 18V, R_L = 3.3Ω, 10% to 90% of VOUT		0.59		mJ
E_{OFF}	Switching energy losses during turn-off	V_{BB} = 18V, R_L = 3.3Ω, 100% to 0% of VOUT		0.77		mJ
		V_{BB} = 18V, R_L = 3.3Ω, 90% to 10% of VOUT		0.67		mJ

(1) Parameter specified by design; not subject to production test.

6.8 Typical Characteristics

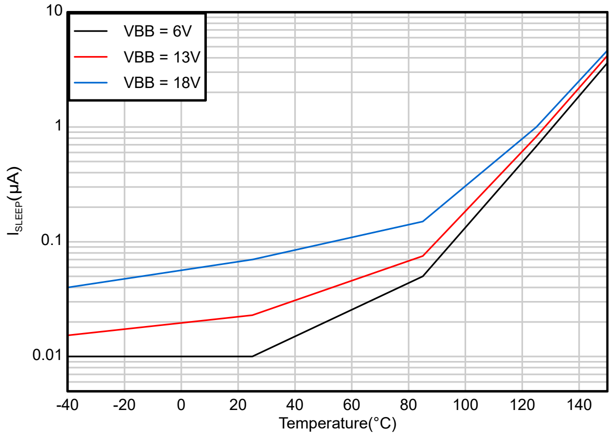


Figure 6-1. Standby Current (I_{SLEEP}) vs Temperature

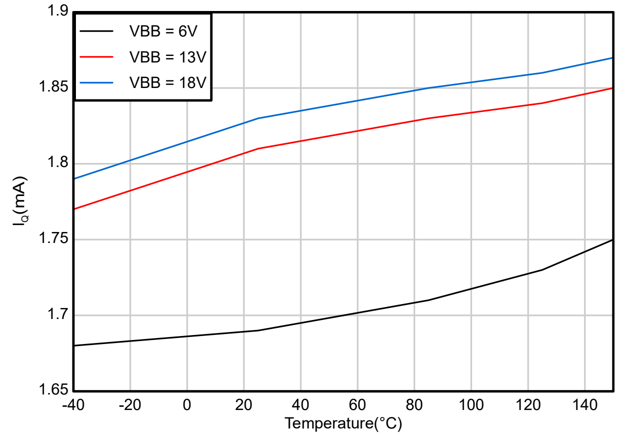


Figure 6-2. Quiescent Current (I_Q) vs Temperature with Both Channels Enabled

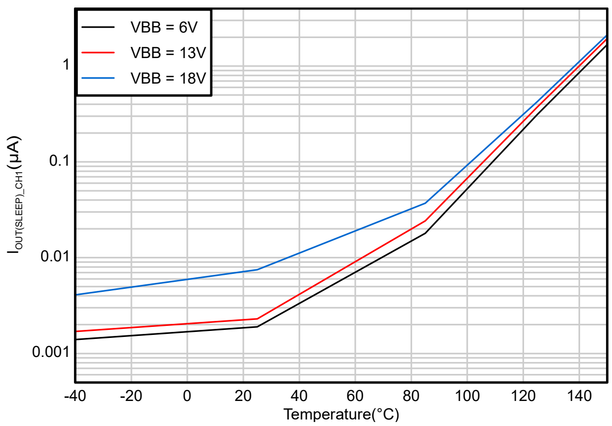


Figure 6-3. Output Leakage Current ($I_{OUT(SLEEP)}$) vs Temperature for Channel 1

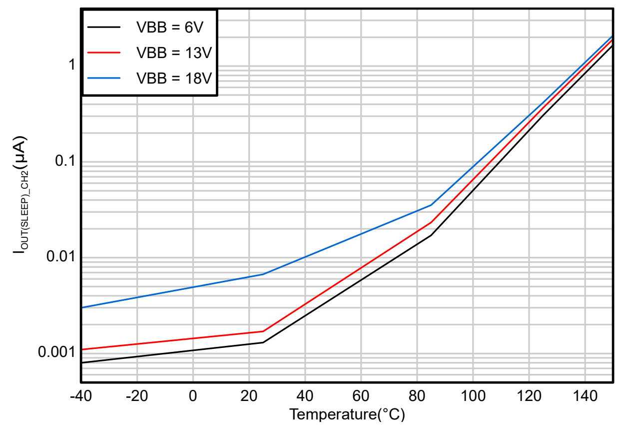


Figure 6-4. Output Leakage Current ($I_{OUT(SLEEP)}$) vs Temperature for Channel 2

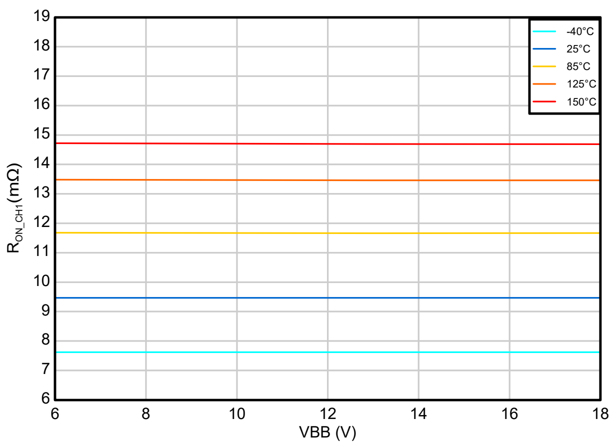


Figure 6-5. On-resistance (R_{ON}) vs VBB for Channel 1

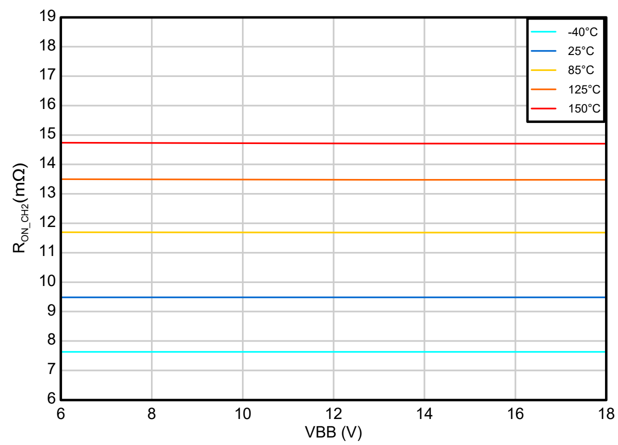


Figure 6-6. On-resistance (R_{ON}) vs VBB for Channel 2

6.8 Typical Characteristics (continued)

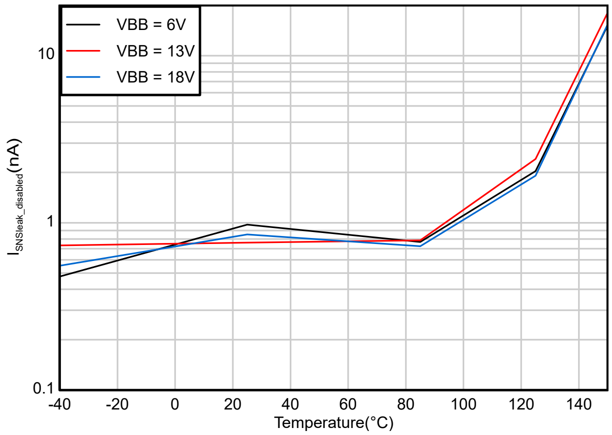


Figure 6-7. I_{SNS} leakage with Diagnostics disabled vs Temperature

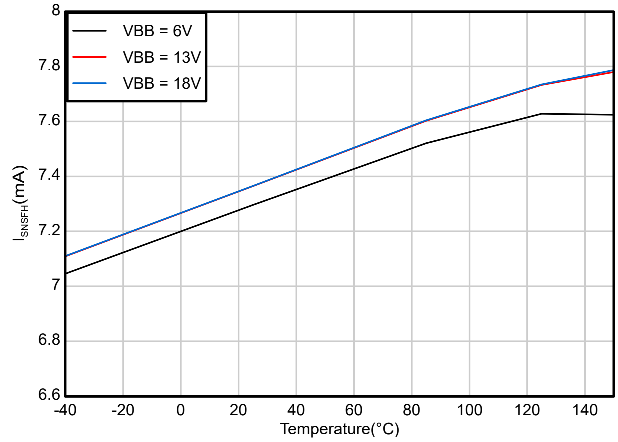


Figure 6-8. I_{SNS} fault high-level current vs Temperature

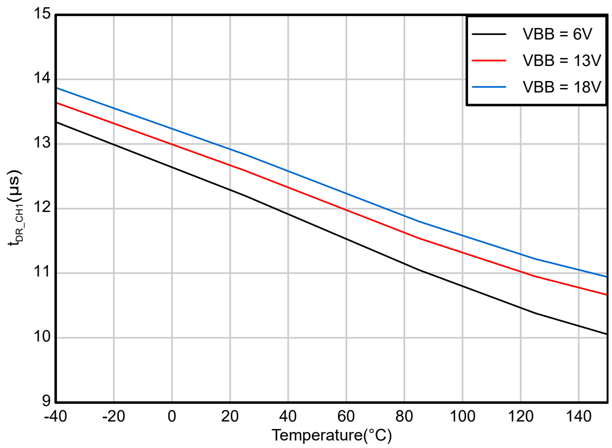


Figure 6-9. Channel Turn-on Delay Time (t_{DR}) vs Temperature for Channel 1

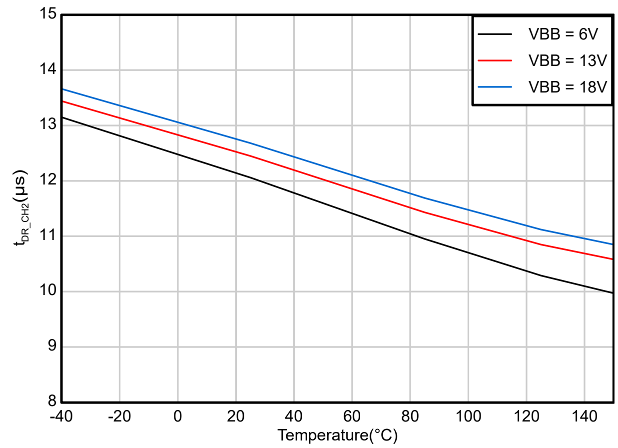


Figure 6-10. Channel Turn-on Delay Time (t_{DR}) vs Temperature for Channel 2

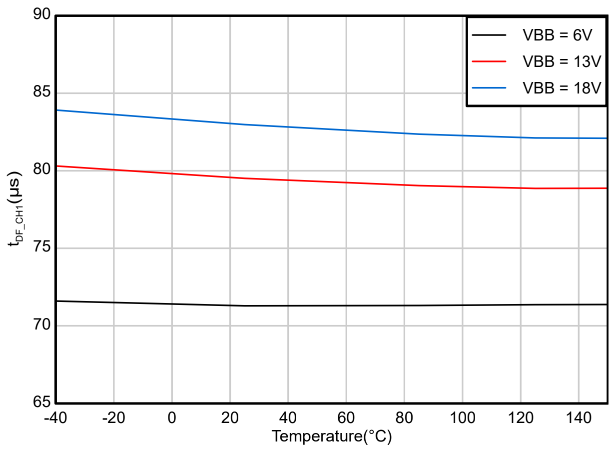


Figure 6-11. Channel Turn-off Delay Time (t_{DF}) vs Temperature for Channel 1

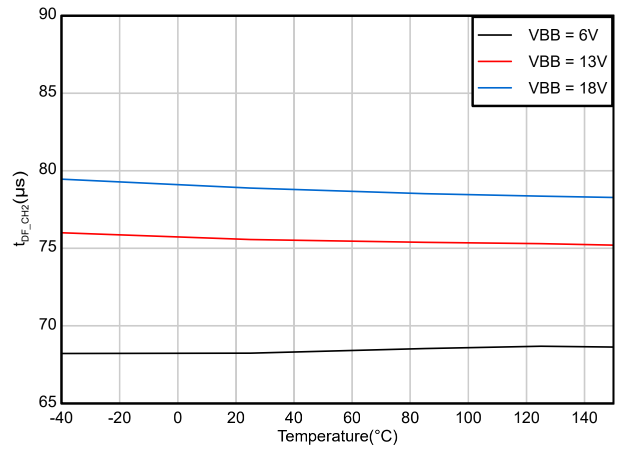


Figure 6-12. Channel Turn-off Delay Time (t_{DF}) vs Temperature for Channel 2

6.8 Typical Characteristics (continued)

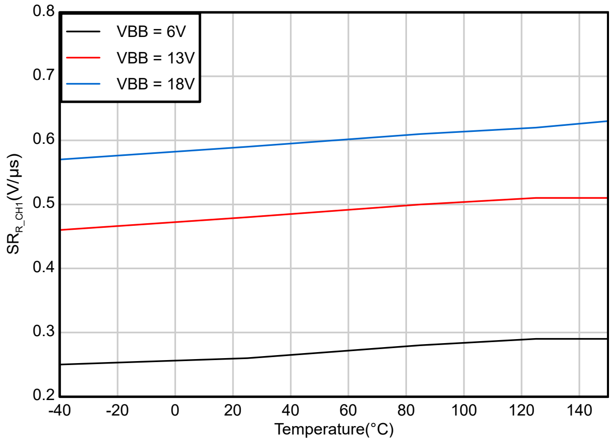


Figure 6-13. VOUT Rising Slew Rate (SR_R) vs Temperature for Channel 1 (P version)

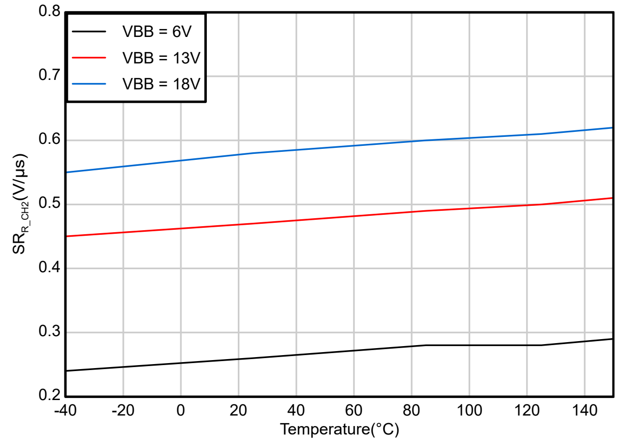


Figure 6-14. VOUT Rising Slew Rate (SR_R) vs Temperature for Channel 2 (P version)

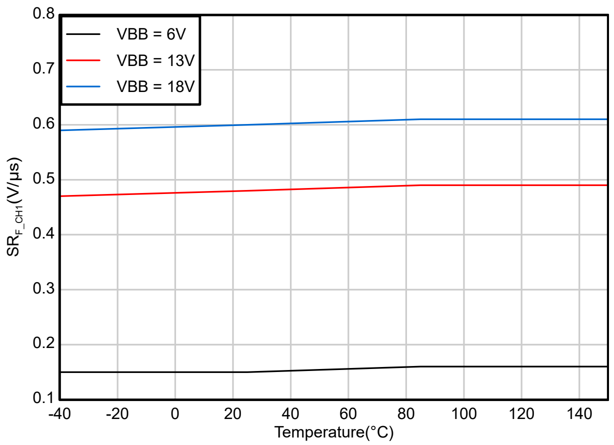


Figure 6-15. VOUT Falling Slew Rate (SR_F) vs Temperature for Channel 1 (P version)

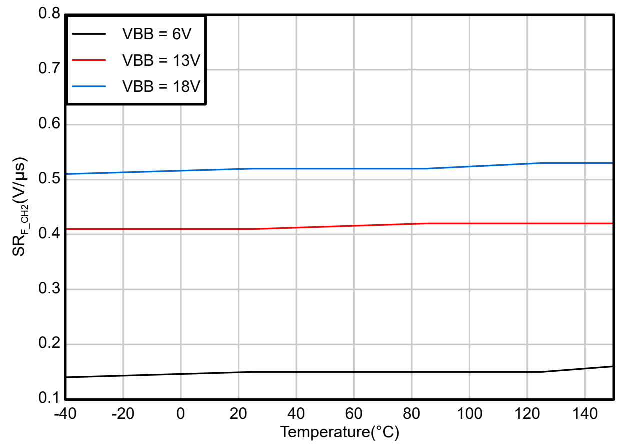


Figure 6-16. VOUT Falling Slew Rate (SR_F) vs Temperature for Channel 2 (P version)

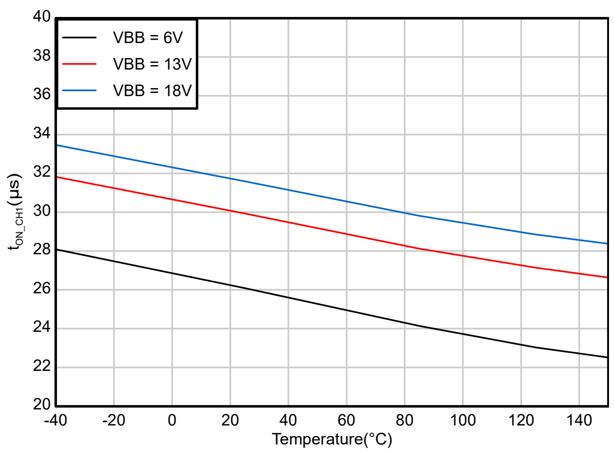


Figure 6-17. Channel Turn-on Time (t_{ON}) vs Temperature for Channel 1

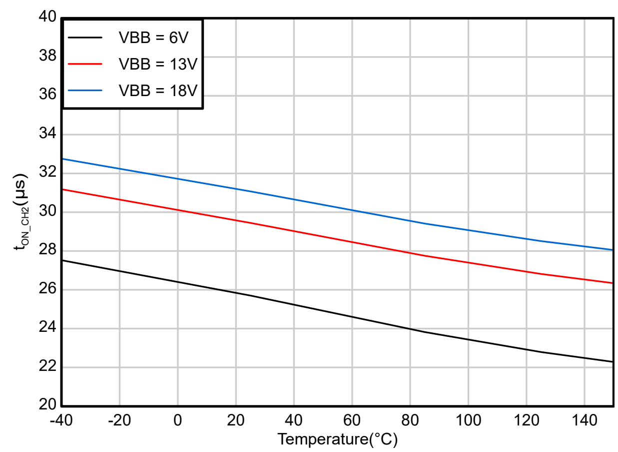


Figure 6-18. Channel Turn-on Time (t_{ON}) vs Temperature for Channel 2

6.8 Typical Characteristics (continued)

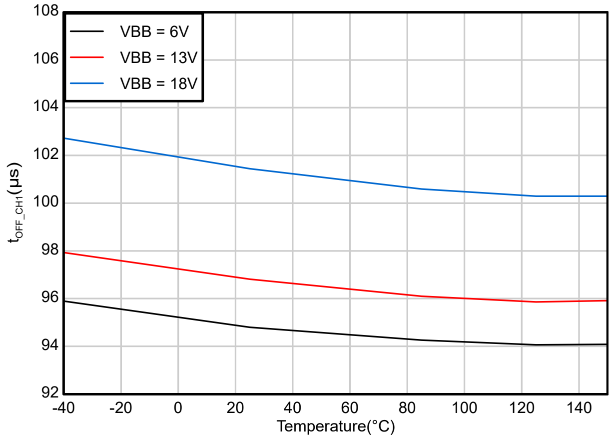


Figure 6-19. Channel Turn-off Time (t_{OFF}) vs Temperature for Channel 1

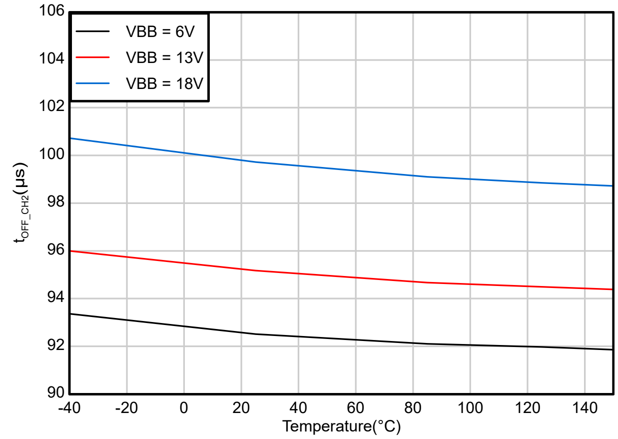


Figure 6-20. Channel Turn-off Time (t_{OFF}) vs Temperature for Channel 2

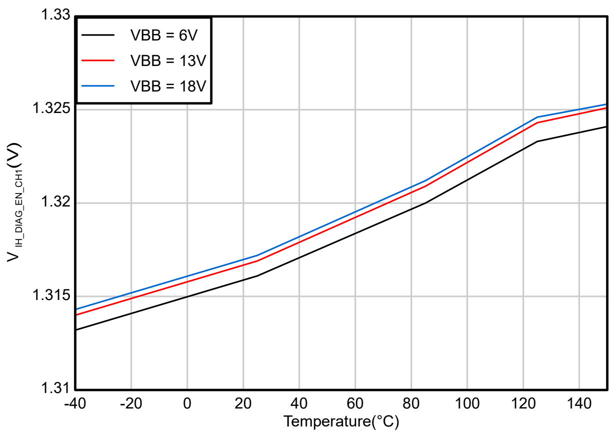


Figure 6-21. DIAG_EN Input Voltage High Level vs Temperature

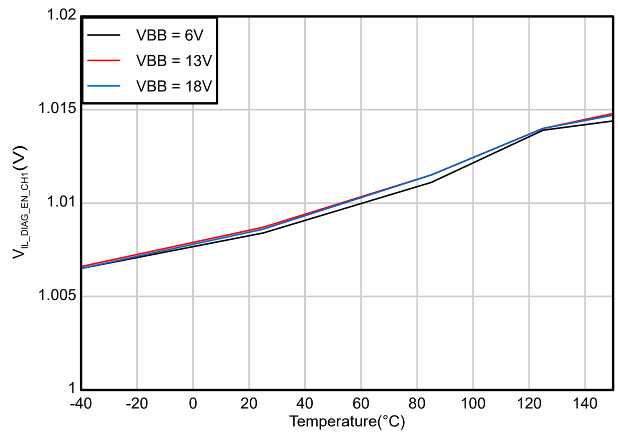


Figure 6-22. DIAG_EN Input Voltage Low Level vs Temperature

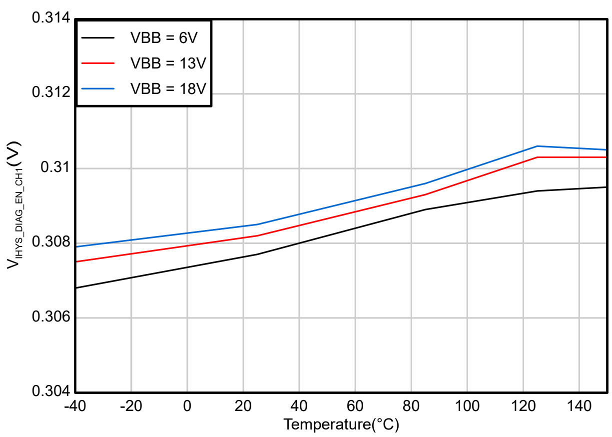


Figure 6-23. DIAG_EN Input Voltage Hysteresis vs Temperature

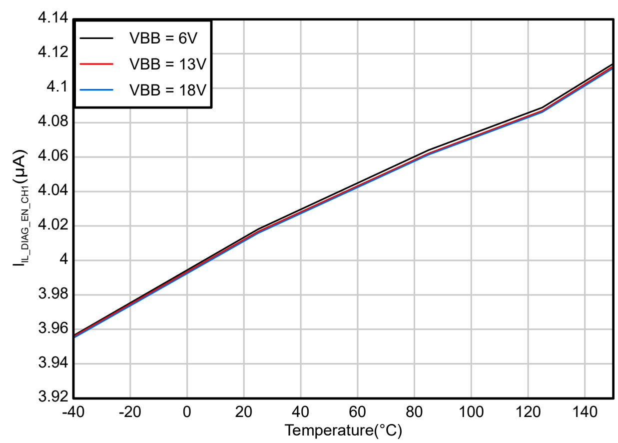


Figure 6-24. DIAG_EN Input Current Low Level vs Temperature

6.8 Typical Characteristics (continued)

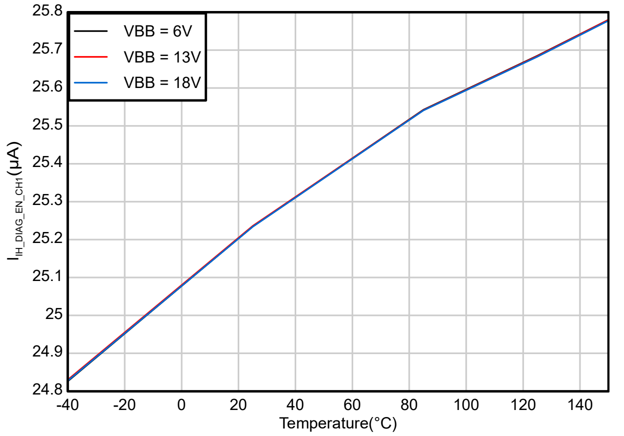


Figure 6-25. DIAG_EN Input Current High Level vs Temperature

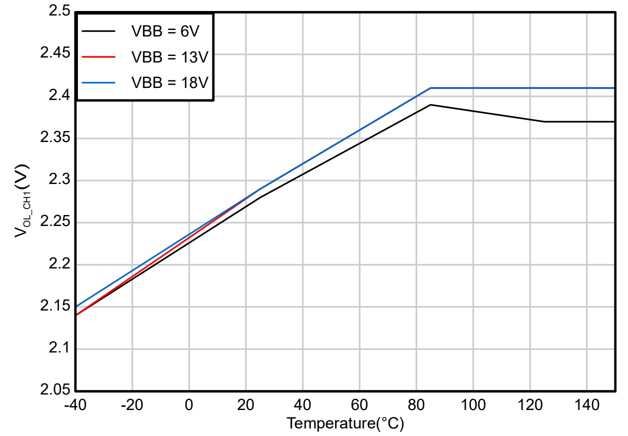


Figure 6-26. Open-Load Detection Voltage (V_{OL}) vs Temperature for Channel 1

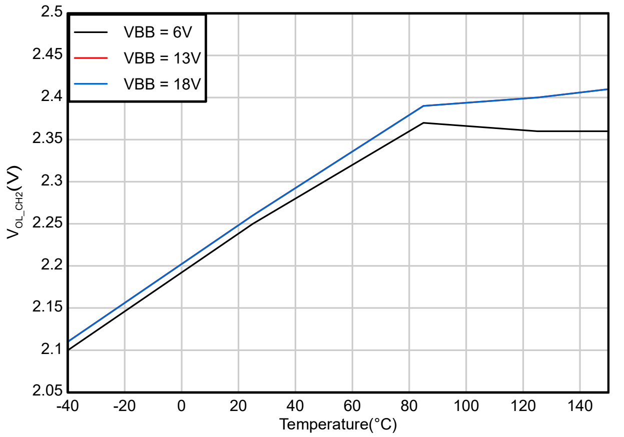


Figure 6-27. Open-Load Detection Voltage (V_{OL}) vs Temperature for Channel 2

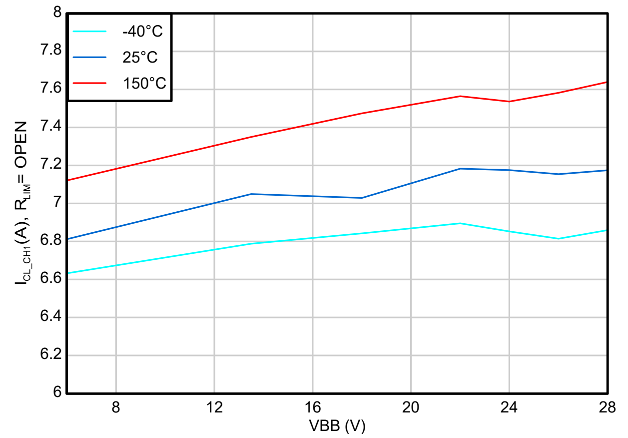


Figure 6-28. Current Limit Regulation Level (I_{CL}) vs VBB for Channel 1, R_{LIM} = OPEN

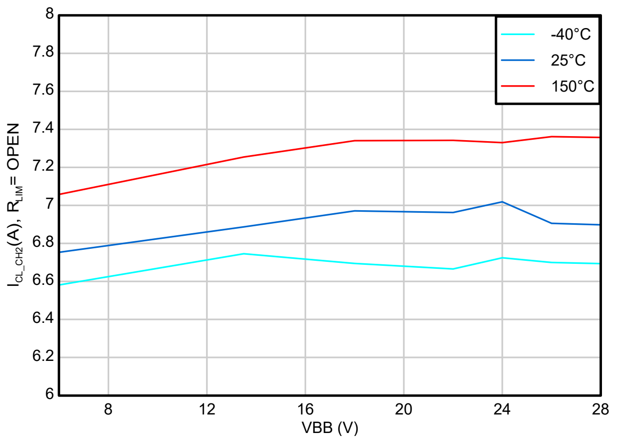


Figure 6-29. Current Limit Regulation Level (I_{CL}) vs VBB for Channel 2, R_{LIM} = OPEN

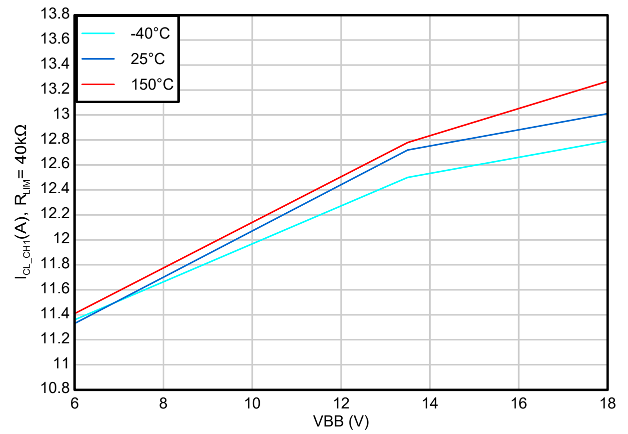


Figure 6-30. Current Limit Regulation Level (I_{CL}) vs VBB for Channel 1, R_{LIM} = 40kΩ

6.8 Typical Characteristics (continued)

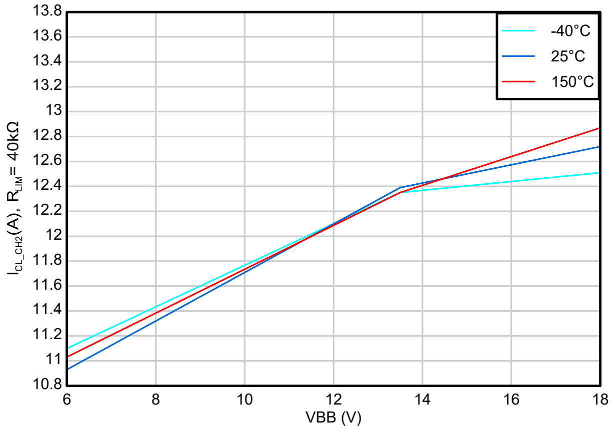


Figure 6-31. Current Limit Regulation Level (I_{CL}) vs VBB for Channel 2, R_{LIM} = 40kΩ

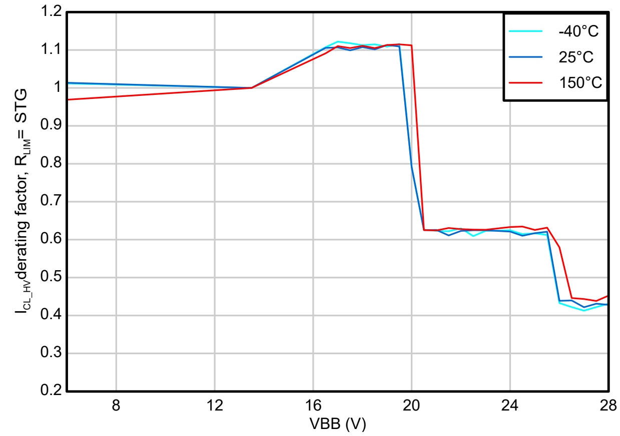


Figure 6-32. Current Limit Derating factor (I_{CL_HV}) vs VBB for both channels, R_{LIM} = GND

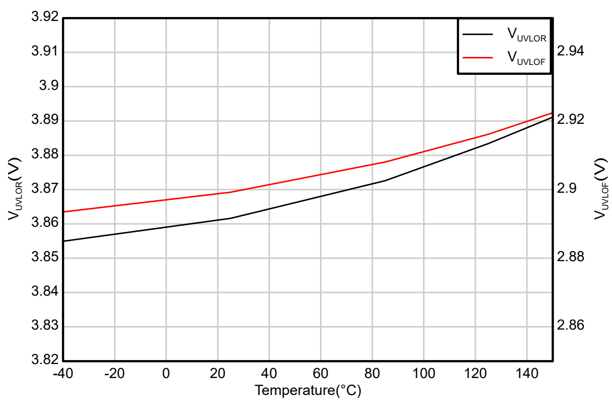


Figure 6-33. Undervoltage Lockout Thresholds (V_{UVLOR}, V_{UVLOF}) vs Temperature

7 Parameter Measurement Information

For reference purposes throughout the data sheet, current directions on the respective pins are as shown by the arrows in Figure 7-1. All voltages are measured relative to the ground plane.

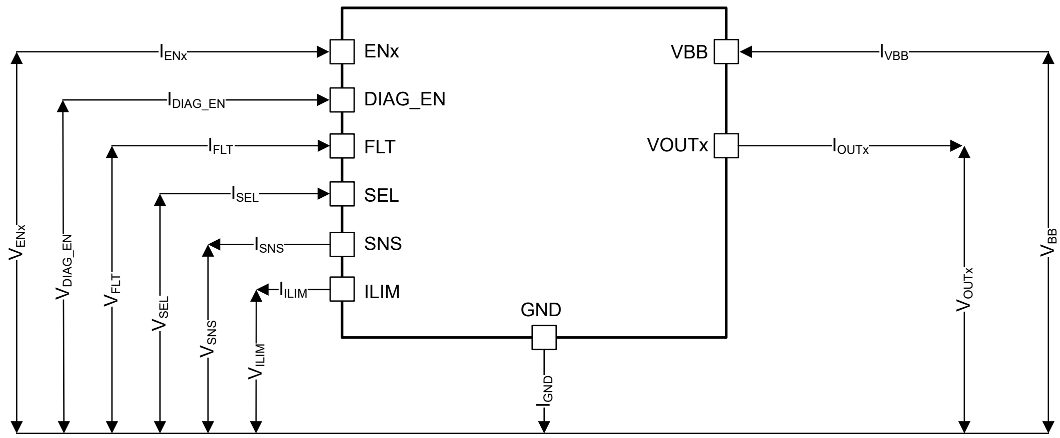
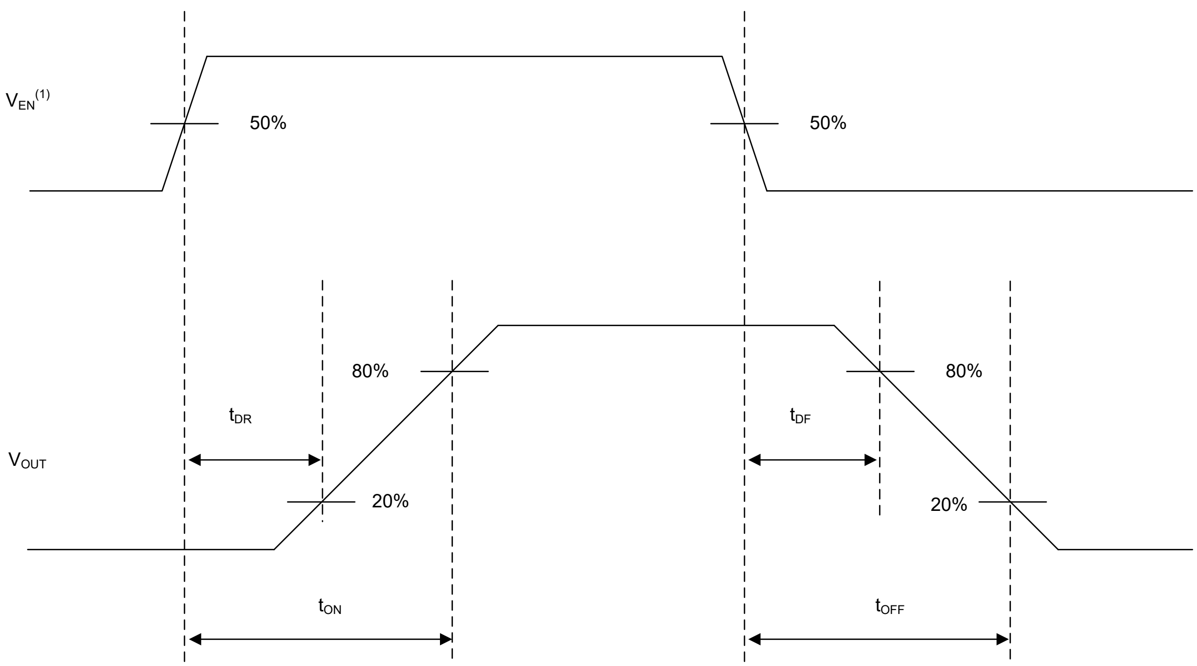


Figure 7-1. Voltage and Current Conventions



Rise and fall time of VEN is 100 ns.

Figure 7-2. Switching Characteristics Definitions

8 Detailed Description

8.1 Overview

The TPS2HC08-Q1 is a dual-channel, fully-protected, high side power switch with integrated NMOS power FETs and charge pump. Full diagnostics and high-accuracy current-sense features enable intelligent control of the load. The device offers two pins to support both digital status and analog current-sense output. The current-sense output can be set to high-impedance state when diagnostics are disabled, which can enable multiplexing of the MCU analog interface between multiple devices.

The device has dedicated logic pins to enable each of the two channels and a separate DIAG_EN pin to enable the diagnostic output. The SEL pin allows to select the channel to be output on the analog current sense (SNS) pin. The device also implements a global $\overline{\text{FLT}}$ pin with an open-drain structure, to be used as an interrupt to the MCU. When a fault condition occurs, the pin is pulled down to GND. An external pullup is required to match the microcontroller supply level.

High-accuracy current sensing allows for better real-time monitoring and more-accurate diagnostics without additional in-line calibration. A current mirror is used to source 1 / K_{SNS} of the load current, which is reflected as voltage across a resistor on the SNS pin. The SNS pin can also report a fault by sourcing a current of I_{SNSFH} out of the SNS pin. During fault the SNS pin voltage is represented by $I_{SNSFH} \times R_{SNS}$. If this voltage violates the acceptable voltage range of the MCU ADC, an external Zener diode or resistor divider on the SNS pin has to be connected.

The device also offers a programmable current-limit function which greatly improves the reliability of the whole system by clamping the inrush current effectively at start-up when charging large capacitances or during short-circuit conditions. The high-accuracy current limit of the device can be set using an external resistor between 7.5A to 25A. The device also offers current limit settings with and without thermal regulation. The thermal regulated current limit can be useful when charging large capacitors at startup. The current limit setting without thermal regulation is useful for loads such high motor stall currents or bulb loads.

A voltage clamp is built in to address switching off the energy of inductive loads, such as relays, solenoids, pumps, motors, and so forth. With the benefits of process technology and excellent IC layout, the TPS2HC08-Q1 device can achieve excellent power dissipation capacity, which can help save the external free-wheeling circuitry in most cases. For more details, see Inductive-Load Switching-Off Clamp.

The TPS2HC08-Q1 device can be used as a high side power switch for a wide variety of resistive, inductive, and capacitive loads, including bulbs, LEDs, relays, solenoids, and heaters.

8.2 Functional Block Diagram

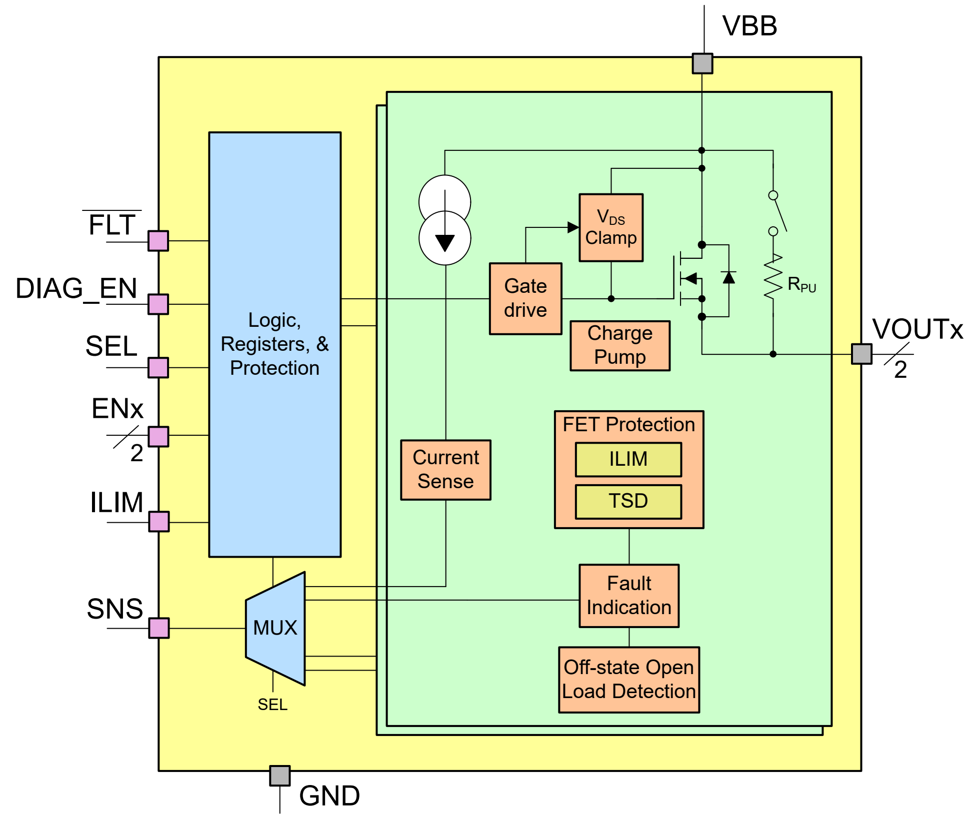


Figure 8-1. Functional Block Diagram

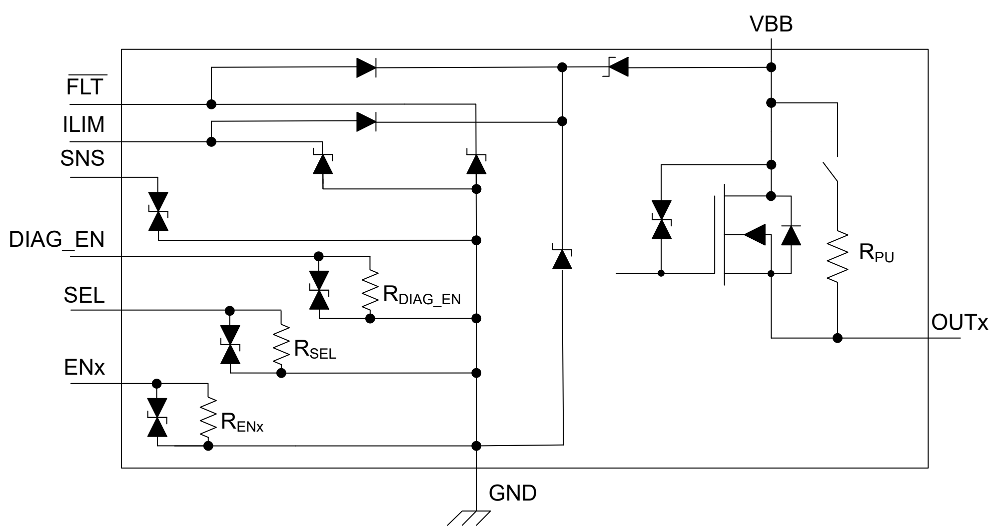


Figure 8-2. Internal Diodes Diagram

The above figure shows the internal diodes structure of the device. There are back-to-back diodes connected between GND pin and low voltage IO pins to provide voltage clamp along with the internal pulldown resistor to keep pins in known state. The FLT and ILIM pins have internal protection structure to withstand voltage up to VBB, making it robust against adjacent pin short. A drain-to-source clamp structure, comprising back-to-back zener and diode, is also implemented across the power switch to protect against inductive energy demagnetisation.

8.3 Feature Description

8.3.1 Accurate Current Sense

The high-accuracy current-sense function allows a better real-time monitoring effect and accurate diagnostics without further calibration. A current mirror is used to source 1 / K_{SNS} of the load current, flowing out to the external resistor between the SNS pin and GND, and reflected as voltage on the SNS pin.

K_{SNS} is the ratio of the output current and the sense current. The accuracy values of K_{SNS} quoted in the electrical characteristics do take into consideration temperature and supply voltage. Each device is internally calibrated while in production, so post-calibration by users is not required.

The sense resistor value, R_{SNS}, can be chosen to maximize the range of currents needed to be measured by the system. The R_{SNS} value must be chosen based on application need. The minimum R_{SNS} value is bounded by the ADC minimum acceptable voltage, $V_{ADC,min}$, for the minimum load current needed to be measured by the system, $I_{LOAD,min}$. The maximum R_{SNS} value is bounded by the ADC maximum acceptable voltage, $V_{ADC,max}$, for the I_{SNSFH} (check Electrical Characteristics for the minimum specification) during fault condition. The SNS pin current during fault condition, I_{SNSFH} should be significantly higher than the SNS pin current at maximum load currrent ($I_{LOAD,max}$), to provide sufficient headroom voltage (V_{HR}) to determine difference between the maximum readable current and a fault condition. Use Equation 1 to calculate the value of R_{SNS} without any external zener diode or resistor divider on SNS pin.

$$\frac{(V_{ADC,min} \times K_{SNS})}{I_{LOAD,min}} \leq R_{SNS} \leq \frac{V_{ADC,max}}{I_{SNSFH}} \quad (1)$$

To get better resolution in current sense voltage, an external Zener diode or resistor divider can be connected to the SNS pin to clamp the SNS pin voltage to ADC maximum acceptable voltage, $V_{ADC,max}$ during the fault condition. In this case, user needs to select R_{SNS} resistor to achieve required headroom voltage (V_{HR}) between the maximum readable current and a fault condition. Use Equation 2 to calculate the value of R_{SNS} in this scenario.

$$\frac{(V_{ADC,min} \times K_{SNS})}{I_{LOAD,min}} \leq R_{SNS} \leq \frac{((V_{ADC,max} - V_{HR}) \times K_{SNS})}{I_{LOAD,max}} \quad (2)$$

In some applications, where there is a higher load current range the above applicable boundary equation can only satisfy either the lower or upper bound. In these cases, more emphasis can be put on the lower measurable current values which increases R_{SNS}. Likewise, if the higher currents are of more interest the R_{SNS} can be decreased. In case a GND network is used for reverse polarity protection, the voltage drop across the GND network has to be taken into account to ensure that the SNS pin voltage does not exceed the maximum acceptable ADC voltage.

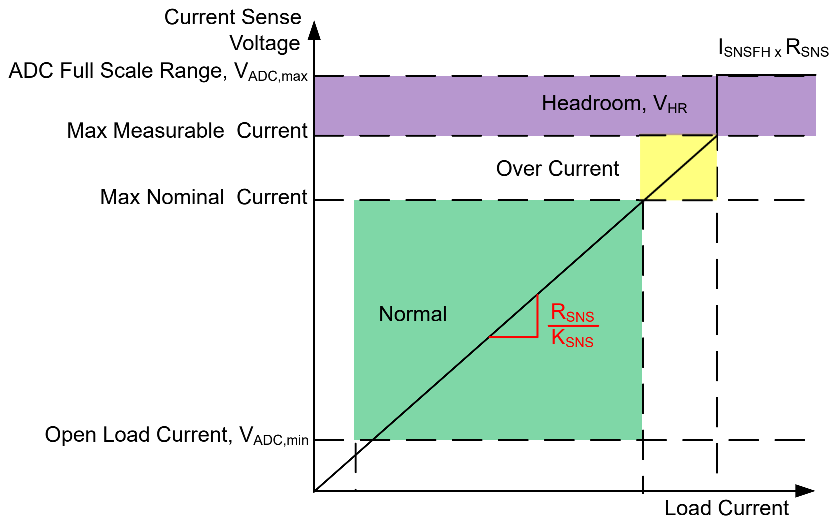


Figure 8-3. Voltage Indication on the Current-Sense Pin

The maximum current the system wants to read, $I_{LOAD,max}$, must be below the current-limit threshold because after the current-limit threshold is tripped the SNS pin current goes to I_{SNSFH}. Figure 8-4 shows the SNS pin behavior for 5A load step on channel 1 of the device with 1kΩ R_{SNS}.

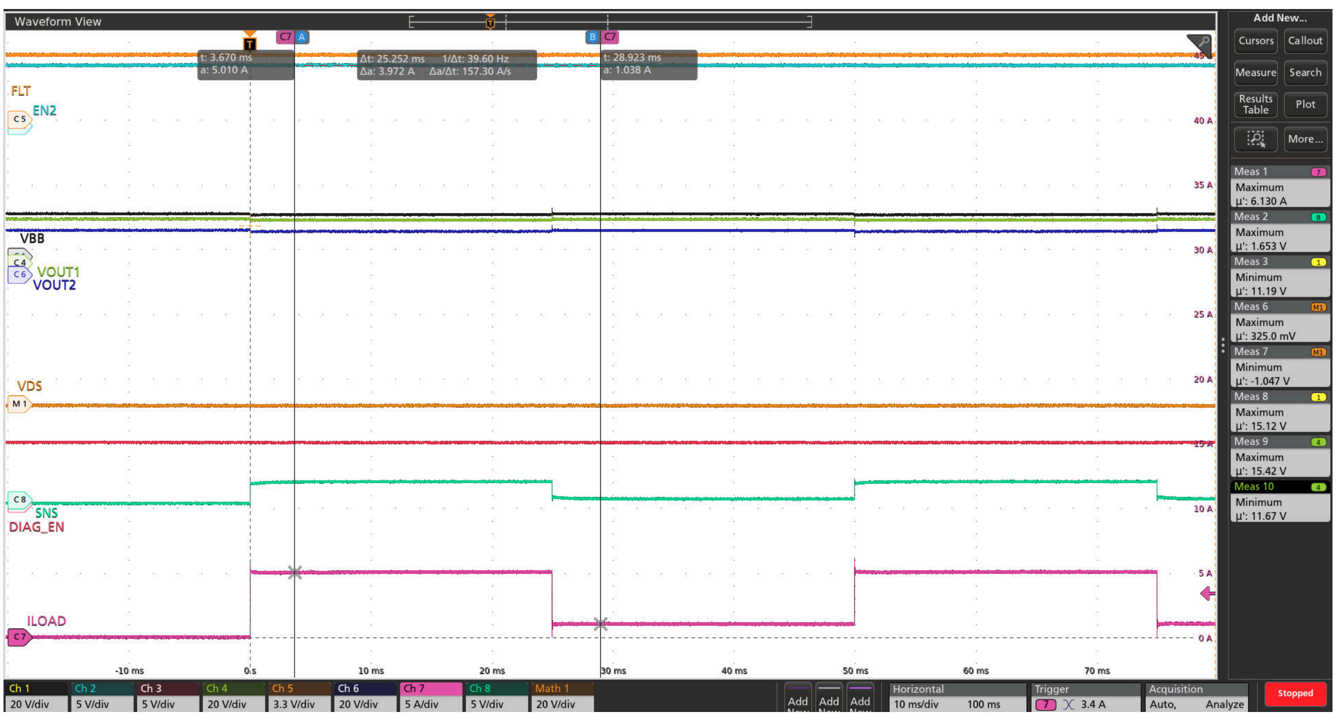


Figure 8-4. SNS Pin Voltage with Varying Load Current on Channel 1 (R_{SNS} = 1kΩ, SEL = 0)

8.3.1.1 SNS Response Time

Some applications can operate with a high frequency, low duty cycle PWM. Such applications require fast settling of the SNS output. For example, a 250Hz, 5% duty cycle PWM has an on-time of only 200μs. The microcontroller ADC can sample the SNS signal after the defined settling time. The following figures shows response time of SNS signal with EN and DIAG_EN being pulled high respectively. The fast response time of the device SNS signal easily allows current sense read by ADC in such applications.

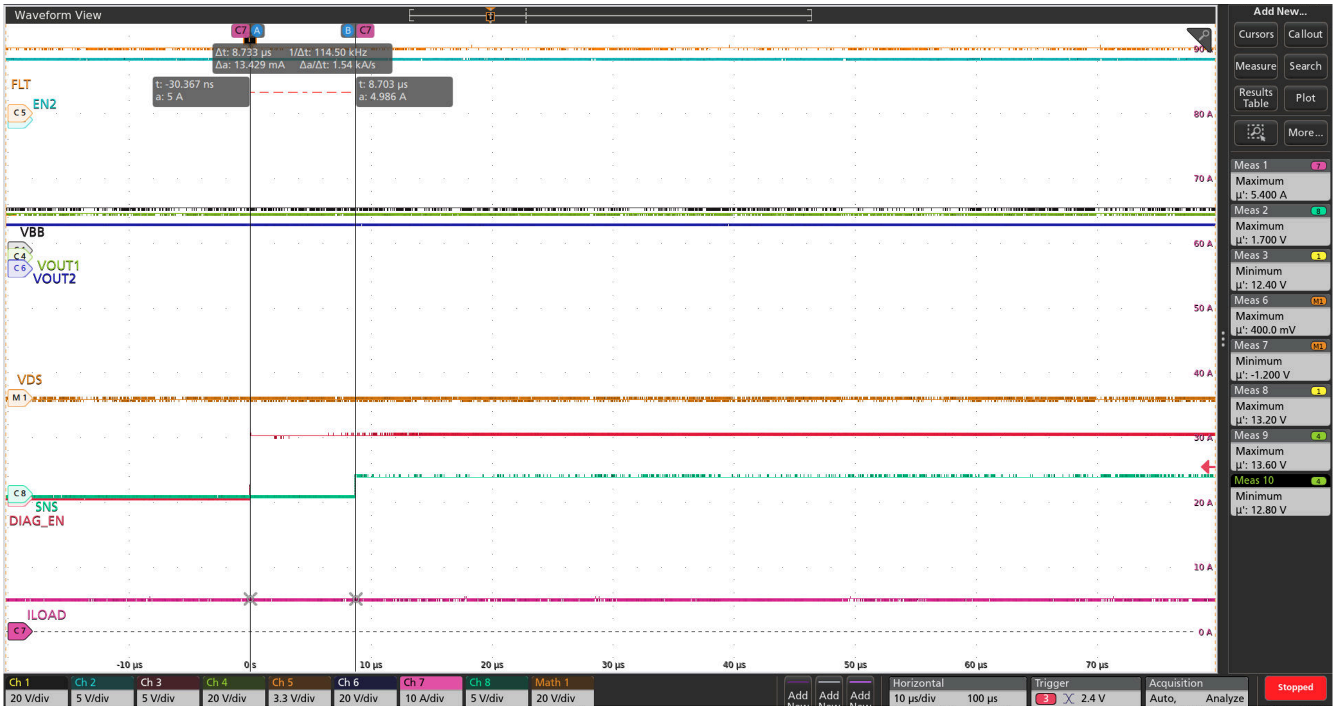


Figure 8-5. SNS Response Time with DIAG_EN ($t_{SNSION1}$)

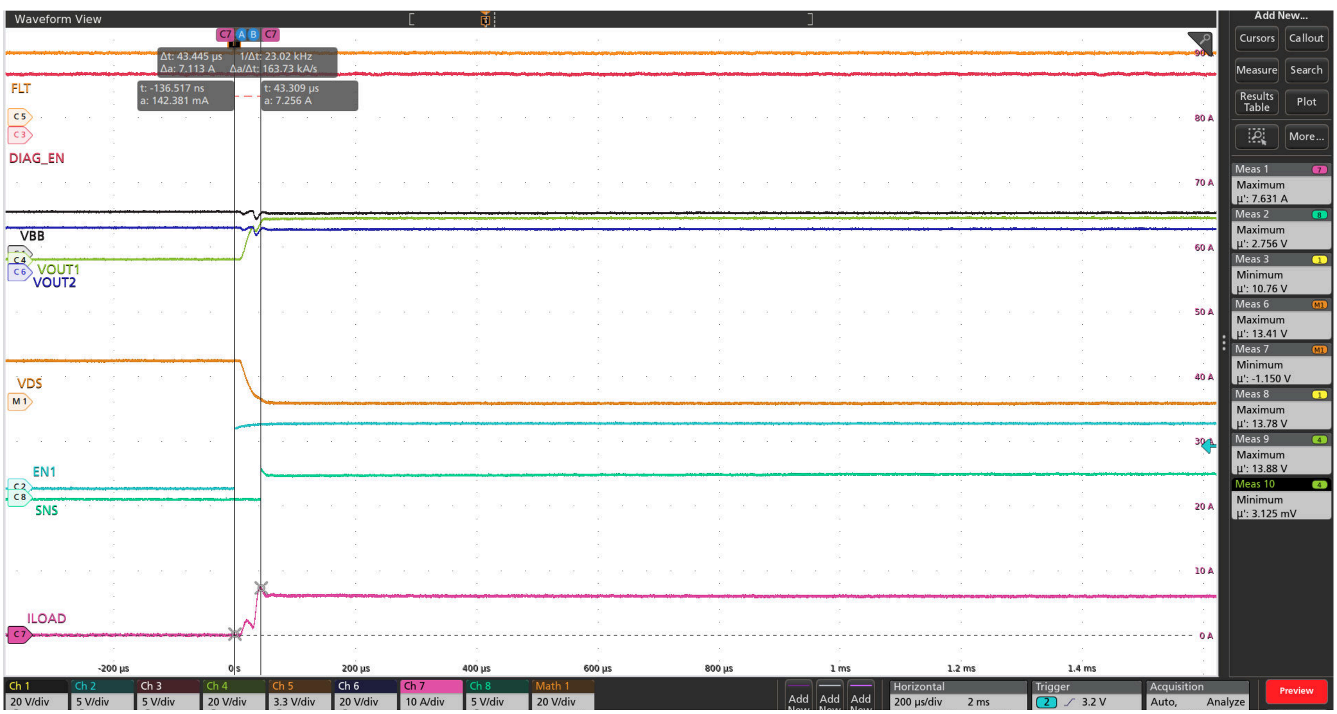


Figure 8-6. SNS Response Time with EN ($t_{SNSION3}$)

Note

Rise and fall times of control signals are 100ns. Control signals include: ENx, DIAG_EN and SEL. Both the channels have same sense timings with appropriate SEL setting.

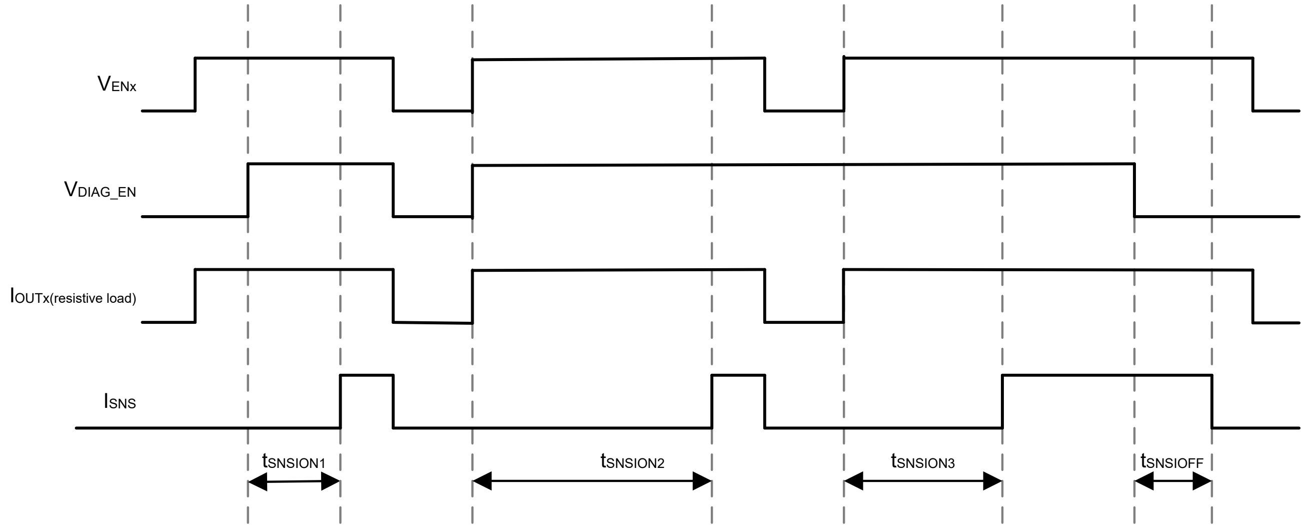


Figure 8-7. SNS Settling Time From EN or DIAG_EN

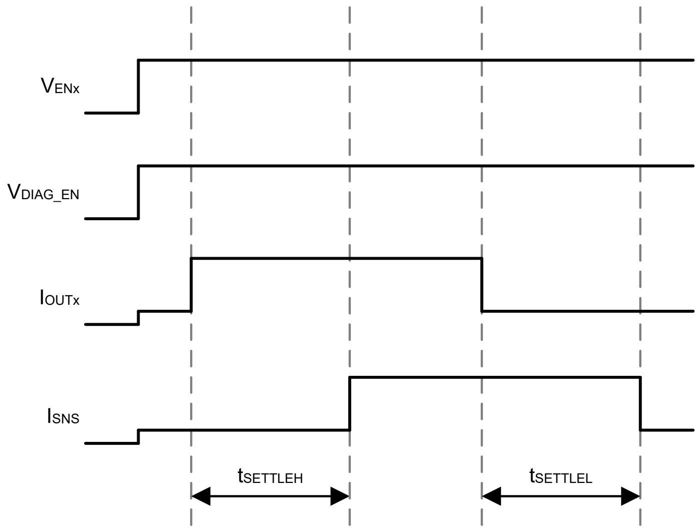


Figure 8-8. SNS Settling Time From Load step

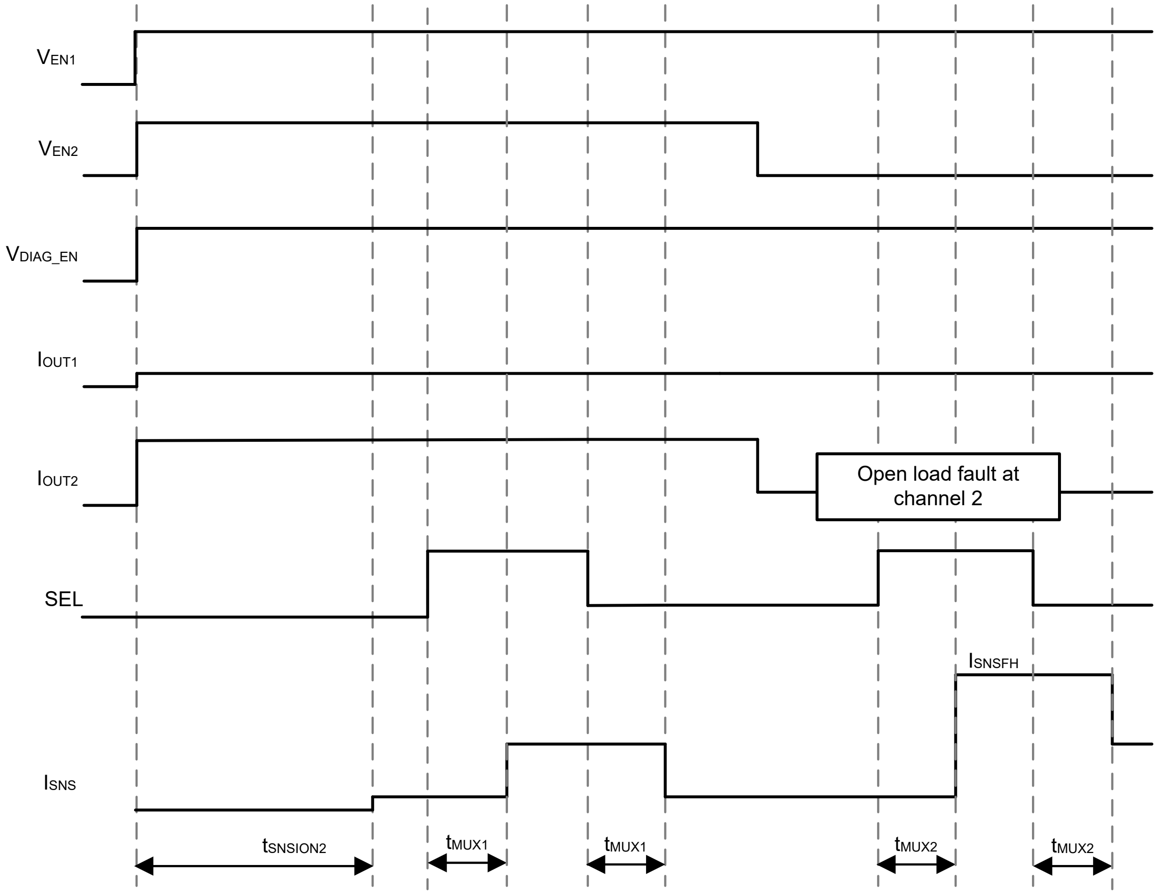


Figure 8-9. SNS Settling Time From Switching From CHx to CHy

8.3.1.2 SNS Output Filter

Due to the internal architecture, the SNS pin signal has a ripple component at a frequency of approximately 1.6MHz. Based on the R_{SNS} value, appropriate C_{SNS} can be connected on SNS pin to filter out this ripple component and reduce the peak-to-peak ripple of the SNS pin voltage. Table 8-1 shows the typical peak-to-peak ripple voltage values with and without C_{SNS} on SNS pin. The designer can select a C_{SNS} capacitor value based on system requirements. A larger value can provide improved filtering. A smaller value can allow for faster transient response. For example, the 150pF C_{SNS} with 1kΩ R_{SNS} adds 750ns (5RC) to the settling time of SNS voltage.

Table 8-1. SNS Ripple (Typical measurement at VBB = 13.5V, I_{LIM} = OPEN, T_A = 25°C)

R_L (Load resistor)	R_{SNS}	C_{SNS}	PEAK-TO-PEAK RIPPLE WITHOUT C_{SNS} (mV)	PEAK-TO-PEAK RIPPLE WITH C_{SNS} (mV)
10Ω	1kΩ	150pF	105mV	50mV
2.2Ω	1kΩ	150pF	157mV	55mV

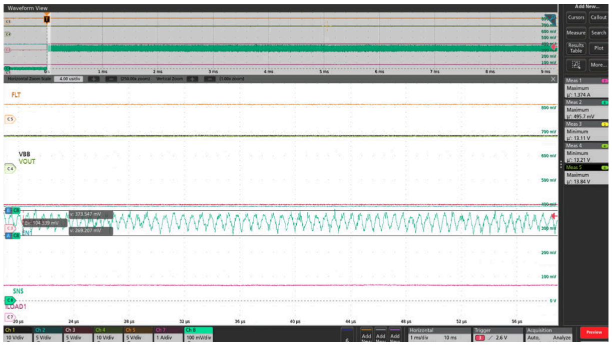


Figure 8-10. SNS Pin Ripple Without C_{SNS} at VBB = 13.5V , I_{LIM} = OPEN, R_L = 10Ω, R_{SNS} = 1kΩ and T_A = 25°C

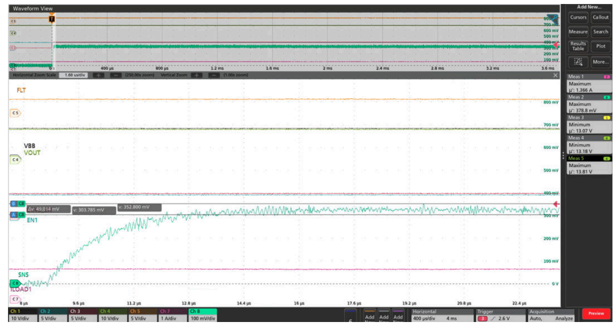


Figure 8-11. SNS Pin Ripple With 150pF C_{SNS} at VBB = 13.5V , I_{LIM} = OPEN, R_L = 10Ω, R_{SNS} = 1kΩ and T_A = 25°C

8.3.1.3 Multiplexing of Current Sense Across Channels

The SEL pin is used to multiplex the shared current-sense function between the two channels. Pulling the SEL pin high or low sets the corresponding channel to be output on the SNS pin if DIAG_EN is high. $\overline{FLT}$ still represents a global interrupt that goes low if a fault occurs on any channel. See Table 8-6 for more details.

8.3.1.4 Multiplexing of Current Sense Across Devices

Figure 8-12 shows SNS pin sharing across two devices using common R_{SNS} resistor. Similarly multiple devices can be configured to share SNS pin. When DIAG_EN is set high, the selected channel current sense output can be enabled using associated ENx and SEL signal, and a current proportional to the load current (I_{LOAD}/ K_{SNS}) flows out of the SNS pin through the external sense resistor to ground. This current is reflected as a voltage that can be measured by an MCU's ADC input. When DIAG_EN is set low, the SNS pin is placed in a high-impedance (tri-state) condition. This feature allows multiple TPS2HC08-Q1 devices to share the same sense resistor and ADC input pin, as only one device can drive the SNS pin at any given time.

K_{SNS} is designed such that SNS pin current at maximum rated load current is same across the device family. This allows for devices with different current ratings to be multiplexed by having same R_{SNS} resistor and ADC full scale range.

When implementing current sense multiplexing across devices, the disabled state SNS pin leakage current ($I_{SNSleak\_disabled}$) from devices (with DIAG_EN set to low) introduces measurement error when reading the current from an active device. For TPS2HC08-Q1 device, the disabled state SNS pin leakage is very low (typical few nA), allowing higher count of devices to be multiplexed.

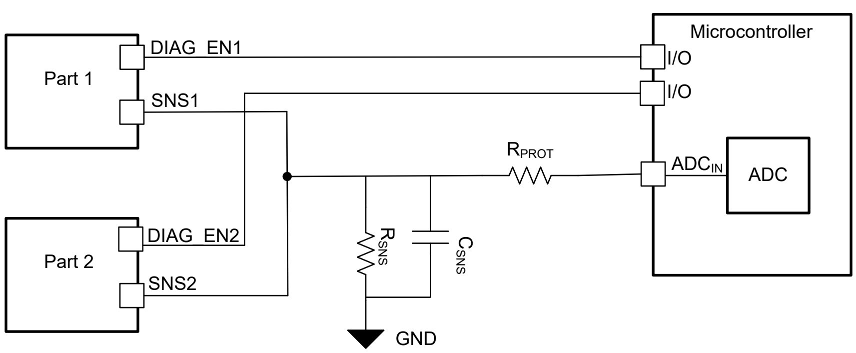


Figure 8-12. SNS Multiplexing Across Multiple Devices

8.3.2 Overcurrent Protection

The TPS2HC08-Q1 provides thermal shutdown and current limiting protection during overcurrent events to protect the internal power MOSFETs. These protection functions are enabled when the device is in the active state. Each channel has an independent thermal shutdown and current limiting circuitry. The current limit fault gets asserted at about 80% ($I_{CL\_FLT\_Trip}$) of set current limit value.

8.3.2.1 Adjustable Current Limit

The TPS2HC08-Q1 offers a high accuracy, adjustable current which enables higher reliability and provides protection to the power supply during a short circuit or power up with large capacitance. An adjustable current limit can also save system costs by reducing PCB traces, connector size, and the capacity of the preceding power stage by setting the current limit at a lower level.

The current limit of the device can be adjusted via an external resistor on the ILIM pin. The value which is set by the ILIM pin is applied to both the channels. The device provides ILIM settings with a thermal regulated current limit which adjusts the current limit level based on the relative temperature of the FET and the controller. This avoids fast heating of the FET and delays the trigger of relative thermal shutdown, which enables the device to charge up large capacitors at startup. With ILIM pin shorted to GND, the device current limit can be configured without thermal regulation where the device limits the current at the set ILIM value. Table 8-2 details the different settings that are possible based on the ILIM pin configuration.

Table 8-2. Current Limit Settings Through ILIM Pin

R_{LIM} VALUE on ILIM pin	TYP $I_{CL} = K_{CL} / R_{LIM}$	THERMAL REGULATION
ILIM = GND or R_{LIM}< 20kΩ	Maximum setting of 25A	Disabled
R_{LIM} = 20kΩ	25A	Enabled
20kΩ < R_{LIM} < 66.66 kΩ	$I_{CL} = K_{CL} / R_{LIM}$	Enabled
R_{LIM} = 66.66kΩ	7.5A	Enabled
ILIM = Open or R_{LIM} > 66.66kΩ	Minimum setting of 7.5A	Enabled

The device also offers a fast-trip circuit breaker function which is used when a short-circuit occurs while a channel is enabled which is also known as a hot-short. Once the I_{CB} threshold is reached, the device quickly turns off the channel to protect the internal MOSFET. Additionally, the device provides a current limit foldback function at higher voltages to help protect the internal power MOSFETs during high V_{DS} events.

The different overcurrent events that can occur in a system are:

- hot-short
- enable into short
- current overload (slow creep)

A hot-short occurs when a channel is enabled and a short-circuit condition is applied to the output of a channel. Enabling in to short occurs when there is already a short on the output of the MOSFET and the channel is enabled into the short-circuit condition. Current overload or also known as slow creep can occur if there is a slow rising overcurrent event at the output.

The next sections describe how the current limiting with thermal regulation and without thermal regulation work along with the circuit breaker and thermal shutdown functions to help protect against the various overcurrent conditions that can occur.

8.3.2.1.1 Current Limiting With Thermal Regulation

Based on the ILIM setting the device can be configured to limit current with thermal regulation. The thermal regulation works by monitoring the relative temperature of the MOSFET ($T_{J,FET}$) to the temperature of controller ($T_{J,CONTROLLER}$) and reducing the current limit based on the relative temperature.

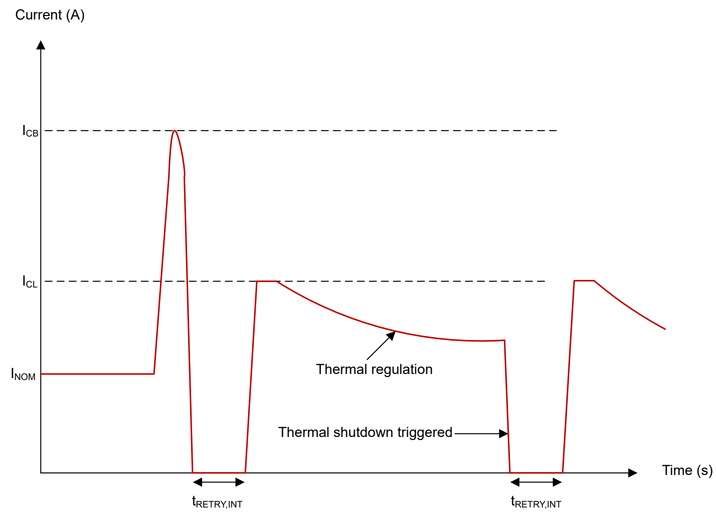


Figure 8-13. On-State Short-Circuit Behavior with Thermal Regulation

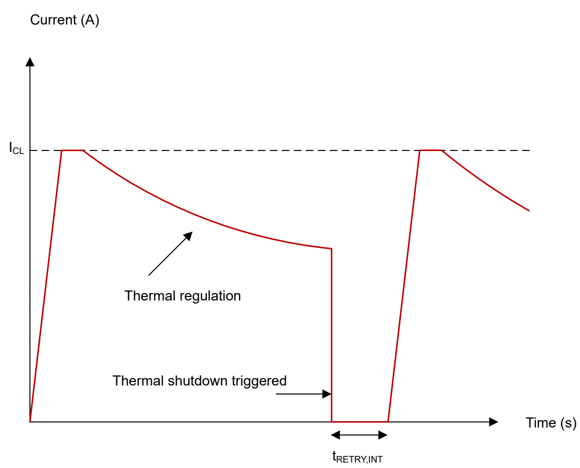


Figure 8-14. Enable Into Short with Thermal Regulation

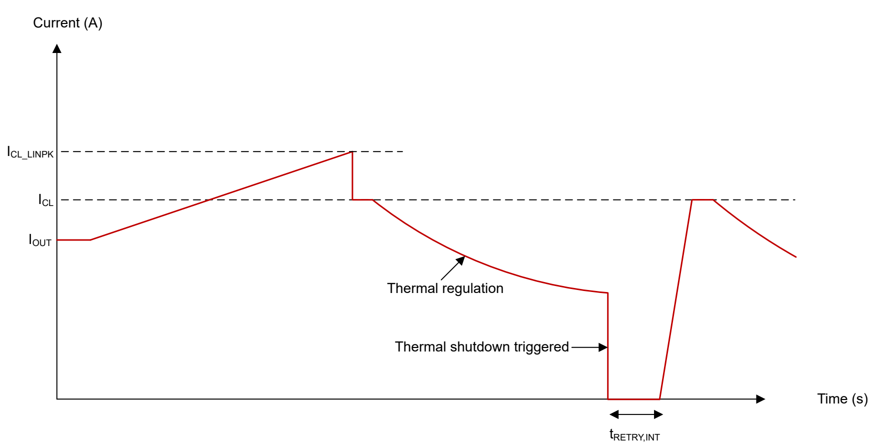


Figure 8-15. Overload Behavior (current creep) with Thermal Regulation

8.3.2.1.2 Current Limiting With No Thermal Regulation

Based on the ILIM setting, the device can be configured to limit current without thermal regulation. The device limits the current based on the setting at the ILIM pin. Applications where this can be used are bulb loads and motor loads with high inrush currents.

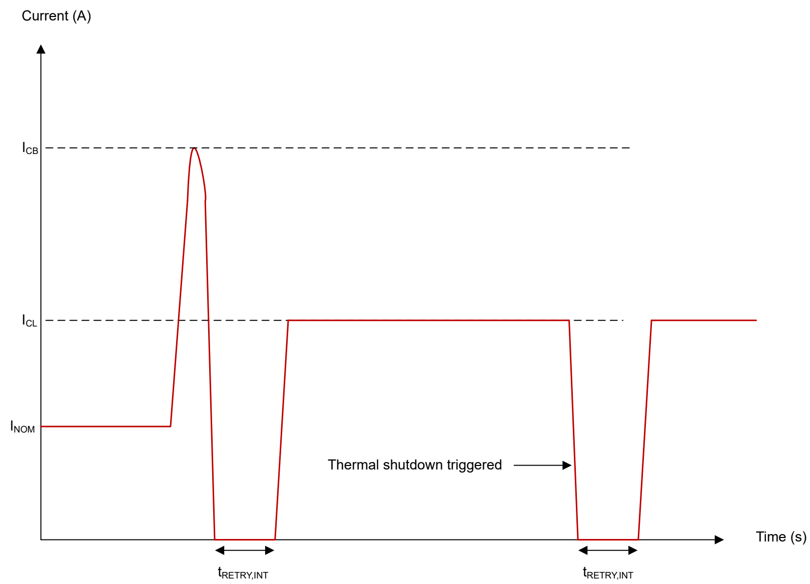


Figure 8-16. On-State Short-Circuit Behavior with No Thermal Regulation

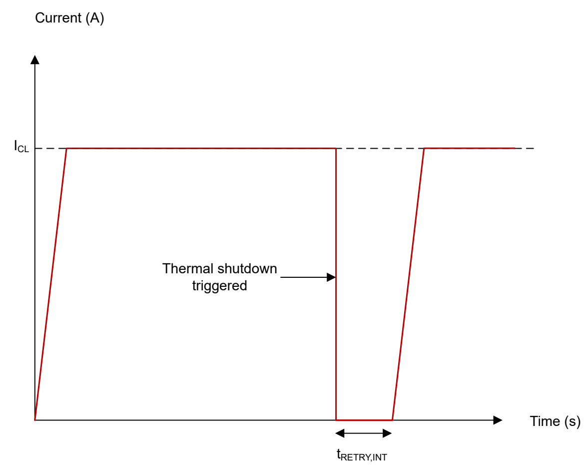


Figure 8-17. Enable Into Short with No Thermal Regulation

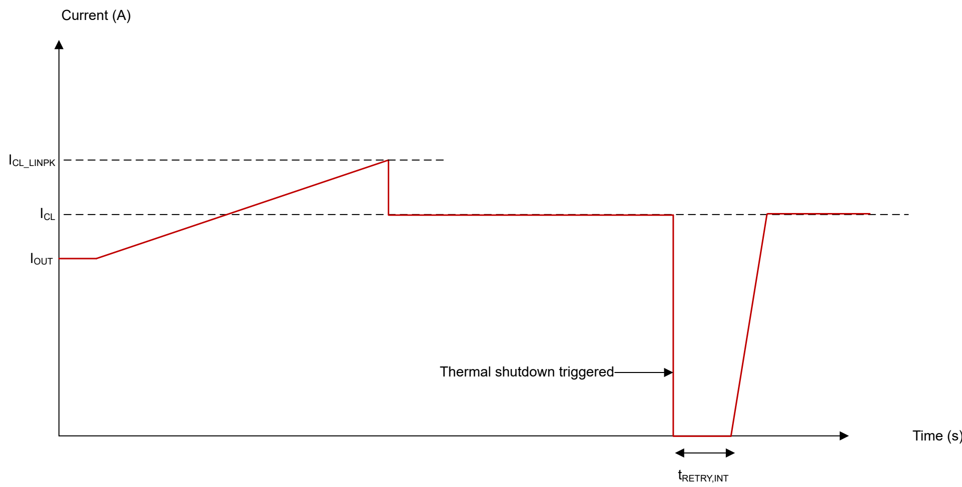


Figure 8-18. Overload Behavior (current creep) with No Thermal Regulation

8.3.2.1.3 Current Limit Foldback

To protect the MOSFET from overcurrent at high V_{DS} voltages the device offers a current limit foldback mechanism. If the ILIM is set to greater than nominal load current value and the VBB voltage is greater than V_{DET1} then the current limit folds back to 1/2 of current limit setting. If the V_{BB} voltage is above V_{DET2}, the current limit folds back 1/3 of current limit setting. Figure 6-32 shows device current limit foldback behavior across VBB voltage.

8.3.2.1.4 Current Limit Accuracy

The adjustable current limit of the device can be set using Equation 3 for valid range of R_{LIM} resistor mentioned in Table 8-2.

$$R_{LIM} = K_{CL} / I_{CL} \tag{3}$$

The accuracy of current limit depends on R_{LIM} resistor tolerance and K_{CL} parameter variation (K_{CL_min}, K_{CL_max}) mentioned in Section 6.5. For example, for 33.2kΩ R_{LIM} resistor with 1% tolerance, the I_{CL} can be calculated as below.

I_{CL} (max) = K_{CL_max} / R_{LIM_min}, where R_{LIM_min} = 0.99*R_{LIM}

I_{CL} (min) = K_{CL_min} / R_{LIM_max}, where R_{LIM_max} = 1.01*R_{LIM}

For R_{LIM} GND and OPEN case, K_{CL} parameter variation contributes to I_{CL} variation.

8.3.2.2 Thermal Shutdown

The device includes a temperature sensor on each power FET and within the controller portion of the device to monitor the temperature of each FET ($T_{J,FET}$) and the temperature of the controller ($T_{J,CONTROLLER}$). There are two cases that the device considers to be a thermal shutdown fault:

- **Relative thermal shutdown (T_{REL}):** $T_{J,FET} – T_{J,CONTROLLER} > T_{REL}$
- **Absolute thermal shutdown (T_{ABS}):** $T_{J,FET} > T_{ABS}$

If either the above faults occur, the relevant switch is turned off. Each channel is turned off based on the measurement of the temperature sensor for that channel. As a result, if the thermal fault is detected on only one channel, the other channel continues normal operation.

8.3.2.2.1 Relative Thermal Shutdown

A relative thermal shutdown event can occur when there is a large peak power event such as a short-to-ground event where the FET temperature ($T_{J,FET}$) quickly rises relative to the controller temperature ($T_{J,CONTROLLER}$). Once the relative temperature ($T_{J,FET} – T_{J,CONTROLLER}$) exceeds T_{REL} the relevant channel is turned off.

8.3.2.2.2 Absolute Thermal Shutdown

An absolute thermal shutdown occurs when the FET temperature ($T_{J,FET}$) rises above T_{ABS}. This can occur when a channel is subjected to long durations of overcurrent such as a permanent short use case. Once the FET temperature ($T_{J,FET}$) exceeds T_{ABS} the relevant channel is turned off.

8.3.3 Retry Protection Mechanism From Thermal Shutdown

When a thermal shutdown occurs, the associated device channel shuts off and implements a retry protection mechamism to improve system reliability. Figure 8-20 explains how the affected channel responds depending on the load current and duration of the overcurrent event.

For load current lower than current limit, device enters into infinite thermal shutdown retry cycles phase until the device recovers from the thermal shutdown fault. In this case, the device turn off time depends on cooling time needed with inherent 200µs delay.

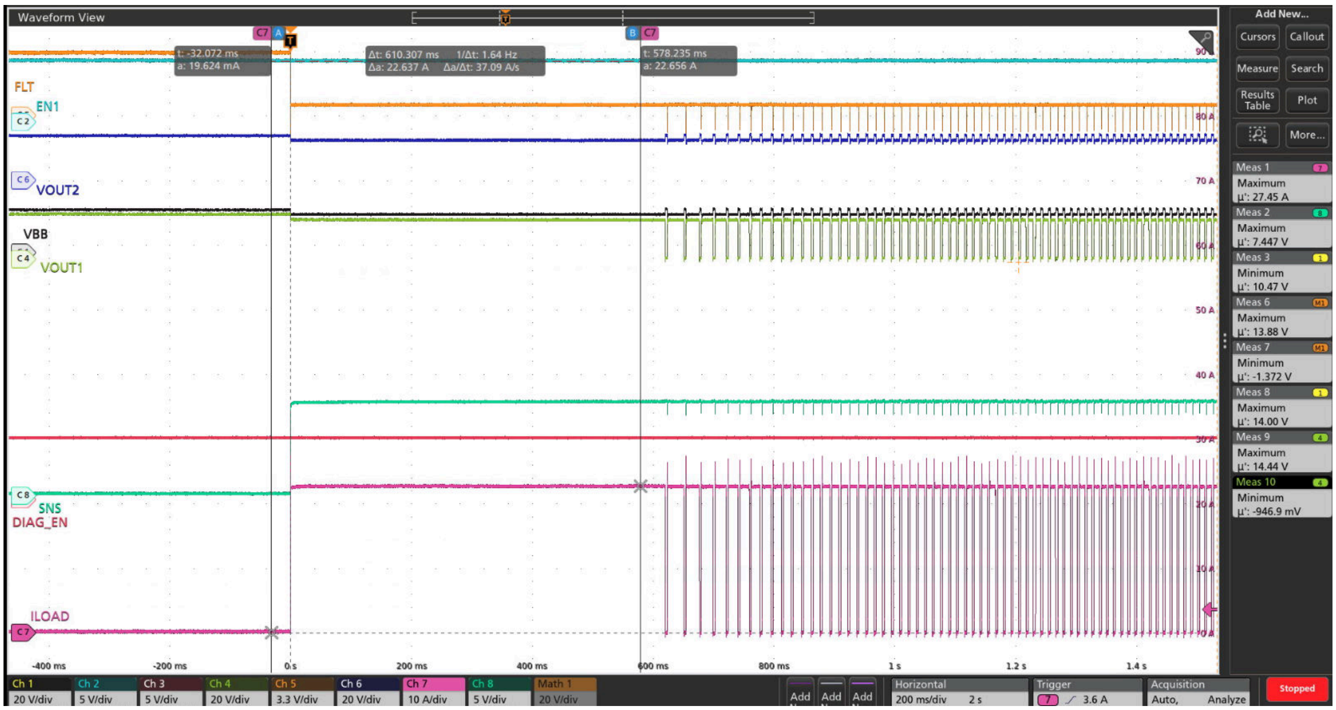


Figure 8-19. Device Enters Into Infinite Thermal Shutdown Retry Phase For Load Current (22A electronic load) Less Than Current Limit (ILIM = GND)

For load current higher than current limit, device implements a finite retry cycles phase protection mechanism based on the duration of the overcurrent event, that can trigger when either of the below fault conditions occur:

1. **Absolute thermal shutdown (T_{ABS}):** $T_{J,FET} > T_{ABS}$
2. **Relative thermal shutdown (T_{REL}):** $T_{J,FET} – T_{J,CONTROLLER} > T_{REL}$
3. **Circuit Breaker (I_{CB})**: A fast-trip protection that triggers when current exceeds the I_{CB} threshold during a hot-short condition. This quickly turns off the channel to protect the internal MOSFET.

The finite retry cycles phase protection mechanism has below durations:

1. **Initial Retry Window ($t < t_{RETRY\_WINDOW}$)**:
   - After I_{CB} or thermal shutdown triggers.
   - Retry attempts occur every $t_{RETRY, INT}$ minimum duration.
   - Each retry can start with I_{CB} peak followed by current limit (I_{CL}) peaks.
2. **Extended Overcurrent Window ($t > t_{RETRY\_WINDOW}$)**:

- Limited to 6 retry attempts.
- First retry cycle happens with minimum $t_{RETRY, EXTD}/2$ duration.
- Successive 5 retry cycles happen with minimum $t_{RETRY, EXTD}$ duration.
- Current peaks are typically limited to I_{CL}.

3. **Latch-off Condition**:
    - After 6 unsuccessful retry attempts.
    - Requires ENx pin toggle to reset.

Table 8-3. Response To Thermal Shutdown

LOAD CURRENT	CONDITIONS		MINIMUM RETRY TIME
I_{LOAD} < I_{CL}	-		Infinite retry
I_{LOAD} > I_{CL}	t < t_{RETRY_WINDOW}		$t_{RETRY, INT}$ = 160µs (typical)
	t > t_{RETRY_WINDOW}	$n_{RETRY,EXTD}$ < 6	$t_{RETRY, EXTD}$ = 80ms (typical)
		$n_{RETRY,EXTD}$ > 6	Latch-off

In any of the above retry cases the relevant channel restarts when the conditions shown below are fullfilled.

1. **Temperature Recovery**: the T_{ABS} or T_{REL} to recover below the T_{HYS} level to restart the device.
2. **Retry Window**: For I_{LOAD} > I_{CL}, appropriate t_{RETRY_WINDOW} interval must elapse.

In case of I_{LOAD} > I_{CL}, if the retry timer has expired and the temperature of T_{ABS} or T_{REL} has not recovered below the T_{HYS} level, the channel does not retry until the temperature falls below the T_{HYS} level. Once a channel latches off due to an extended overcurrent event, the ENx pin can be brought from high to low (with minimum pulse duration of about 20us) to reset the $\overline{FLT}$ and SNS signal. The output of the channel then follows the ENx pin after the initial toggle from high to low.

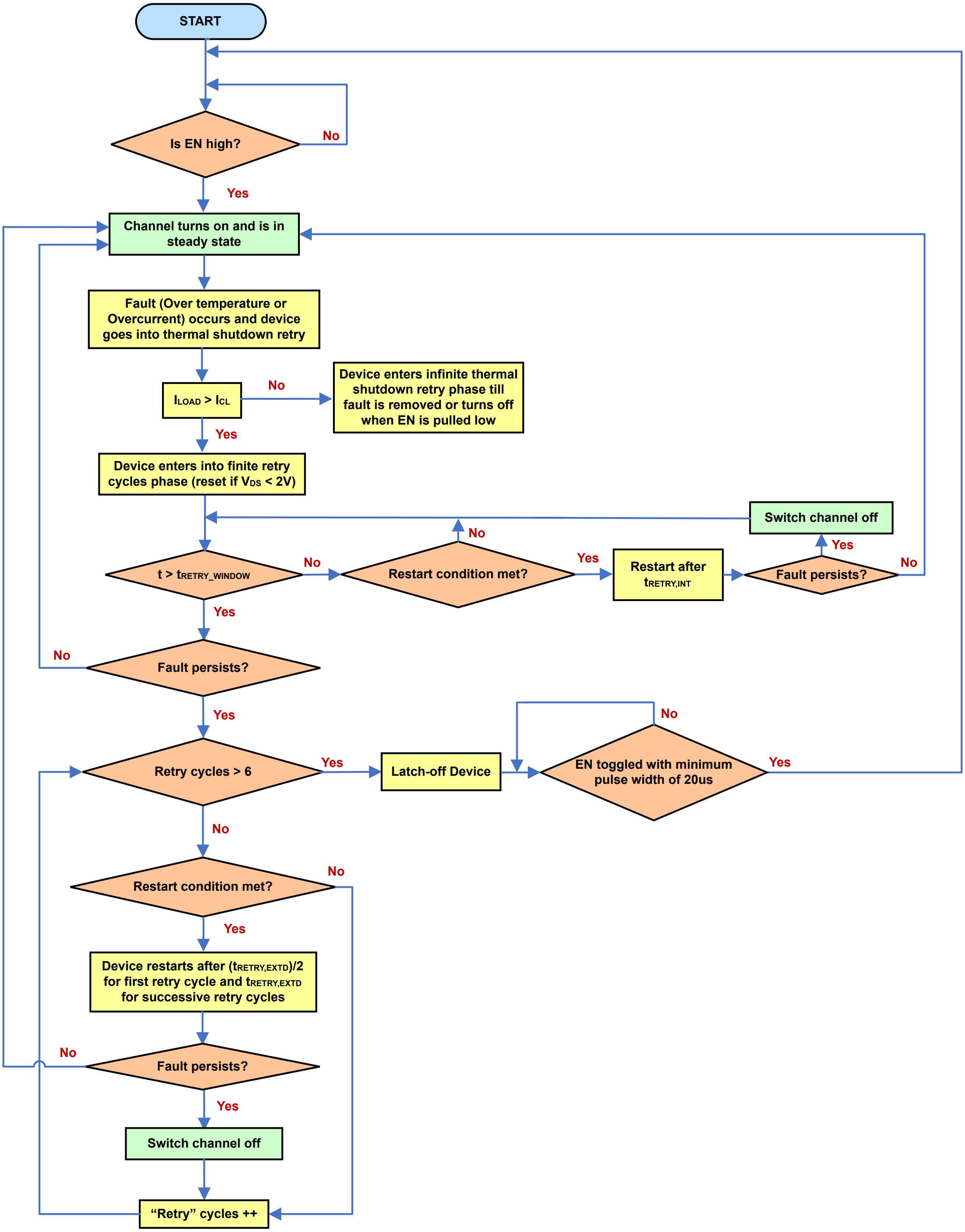


Figure 8-20. Retry Protection Mechanism

Figure 8-21 and Figure 8-22 below shows how the device retries after a hot-short with and without thermal regulation, respectively. When the device experiences a thermal fault and enters the retry cycle, the first current peak in initial retry window reaches I_{CB} threshold, triggering fast trip circuit breaker. Successive current peaks are lower and correspond to set current limit (I_{CL}) value.

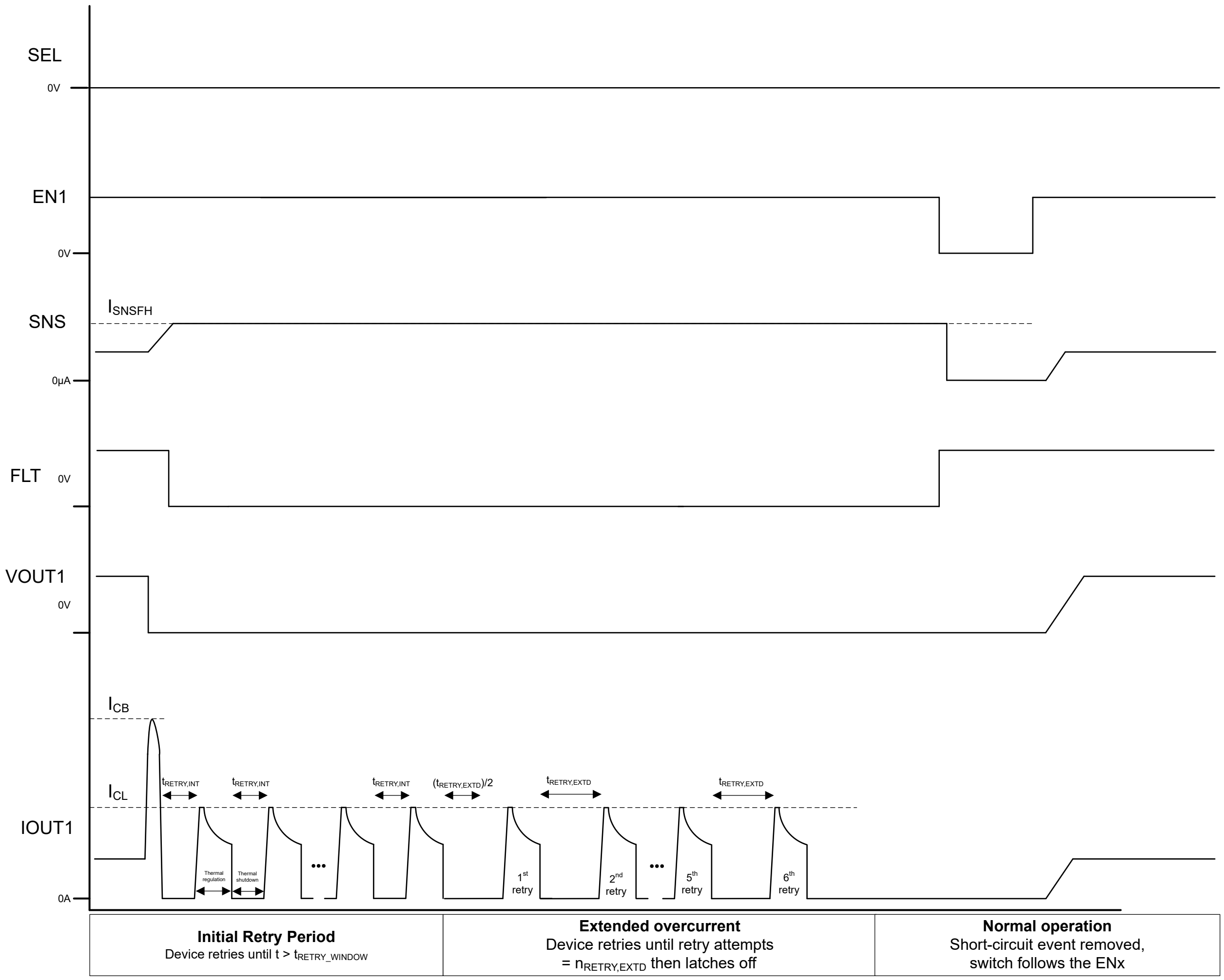


Figure 8-21. Retry Behavior After Hot-Short with Thermal Regulation

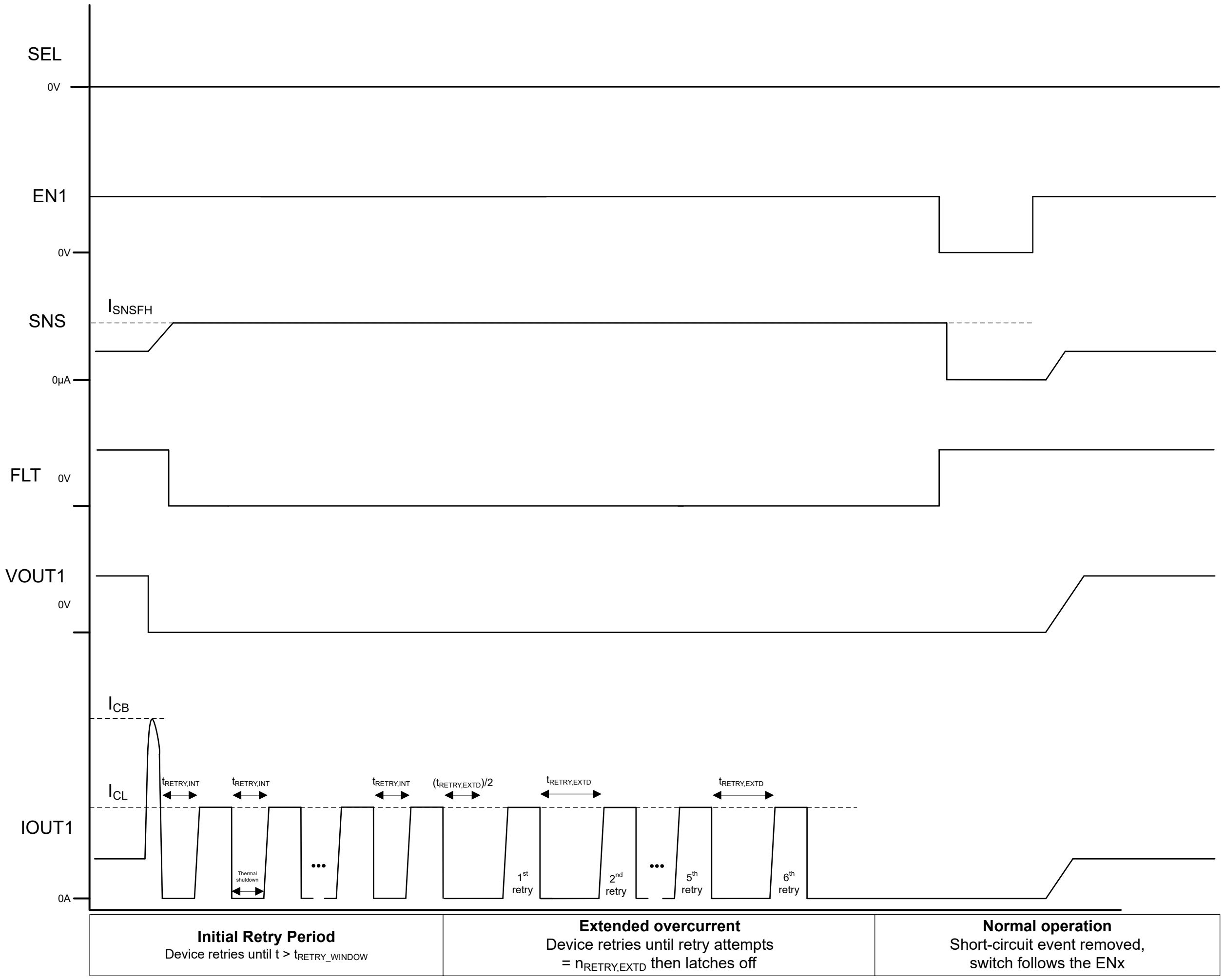


Figure 8-22. Retry Behavior After Hot-Short with No Thermal Regulation

In case the device enters inite retry cycles phase protection mechanism due to I_{CB} fault without thermal shutdown fault, the device can stay in thermal regulation in initial retry window and directly enter thermal shutdown retry behavior in extended retry window. Figure 8-23 shows this behavior where the finite retry cycles phase protection mechanism is triggered by I_{CB} fault.

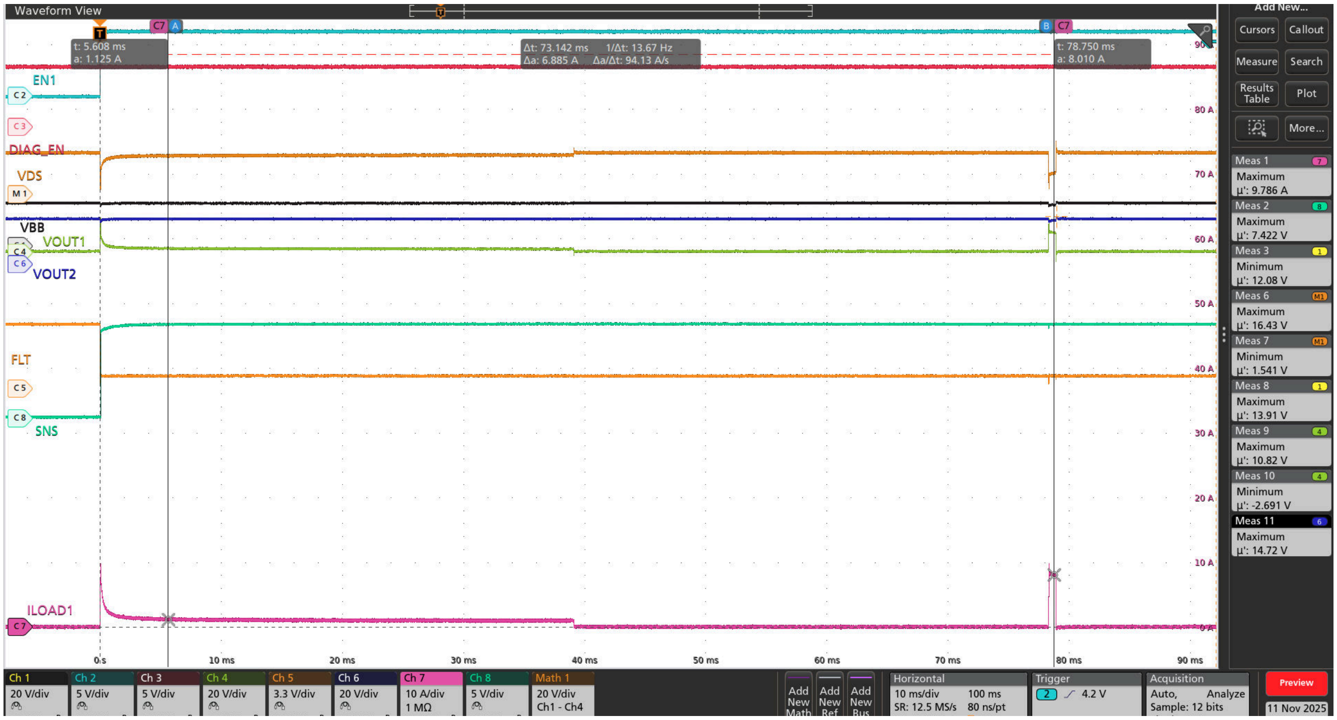


Figure 8-23. Device Entering Into Extended Retry Window with Thermal Regulation Behavior in Initial Retry Window

8.3.3.1 Reliable Switch-On Behavior

During the commanded switch-on sequence, the TPS2HC08-Q1 provides reliable switch-on behavior with below device features:

1. **Adjustable Current Limit**: The device permits current up to the configured current limit (I_{CL}), which can be precisely adjusted between 7.5A to 25A using the external R_{LIM} resistor.
2. **Thermal Regulation of Current Limit**: As the FET temperature rises during switch-on, the thermal regulation circuitry reduces the current limit to maintain safe operating conditions.
3. **Retry protection mechanism from Thermal Shutdown**: If the thermal threshold is reached during initial startup, the device enters a well-defined retry sequence designed specifically for reliable load startup.

8.3.4 Inductive-Load Switching-Off Clamp

When switching an inductive load off, the inductive reactance tends to pull the output voltage negative. Excessive negative voltage can cause the power FET to break down. To protect the power FET, an internal clamp between drain and source is implemented, namely $V_{DS(clamp)}$.

$$V_{DS(clamp)} = V_{VS} - V_{OUT} \tag{4}$$

During the period of demagnetization (t_{decay}), the power FET is turned on for inductance-energy dissipation. The total energy is dissipated in the high-side switch. Total energy includes the energy of the power supply ($E_{(VS)}$) and the energy of the load ($E_{(load)}$). If resistance is in series with inductance, some of the load energy is dissipated on the resistance.

$$E_{(HSS)} = E_{(VS)} + E_{(load)} = E_{(VS)} + E_{(L)} - E_{(R)} \tag{5}$$

When an inductive load switches off, $E_{(HSS)}$ causes high thermal stressing on the device.. The upper limit of the power dissipation depends on the device intrinsic capacity, ambient temperature, and board dissipation condition.

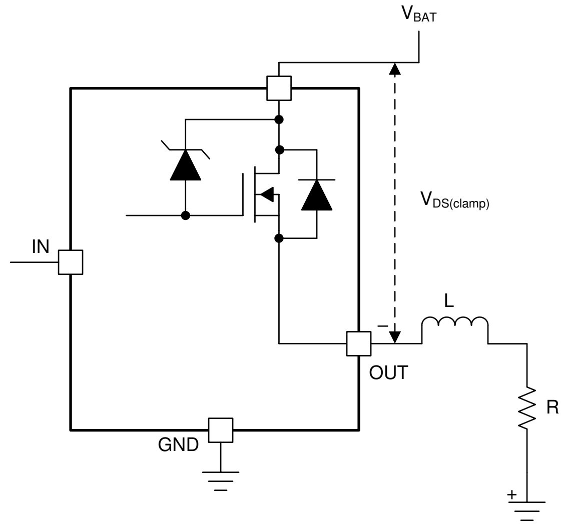


Figure 8-24. Drain-to-Source Clamping Structure

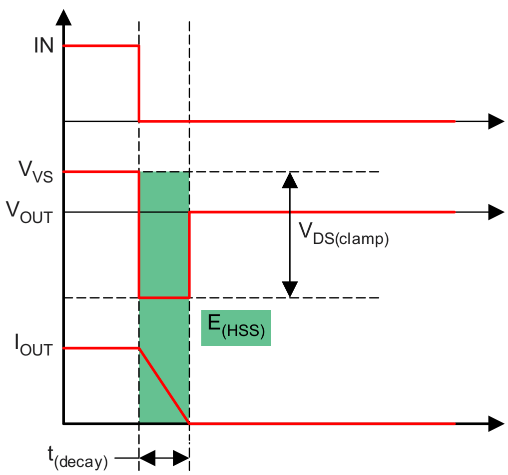


Figure 8-25. Inductive Load Switching-Off Diagram

From the perspective of the high-side switch, $E_{(HSS)}$ equals the integration value during the demagnetization period.

$$E_{(HSS)} = \int_{0}^{t_{(decay)}} V_{DS(clamp)} \times I_{OUT}(t)dt$$

$$t_{(decay)} = \frac{L}{R} \times \ln\left(\frac{R \times I_{OUT(max)} + |V_{OUT}|}{|V_{OUT}|}\right)$$

$$E_{(HSS)} = L \times \frac{V_{VS} + |V_{OUT}|}{R^2} \times \left[R \times I_{OUT(max)} - |V_{OUT}| \ln\left(\frac{R \times I_{OUT(max)} + |V_{OUT}|}{|V_{OUT}|}\right)\right] \tag{6}$$

When R approximately equals 0, $E_{(HSD)}$ can be given simply as:

$$E_{(HSS)} = \frac{1}{2} \times L \times I_{OUT(max)}^2 \frac{V_{VS} + |V_{OUT}|}{|V_{OUT}|} \tag{7}$$

Note that for PWM-controlled inductive loads, adding the external freewheeling circuitry as shown below is recommended to protect the device from repetitive power stressing. TVS is used to achieve the fast decay.

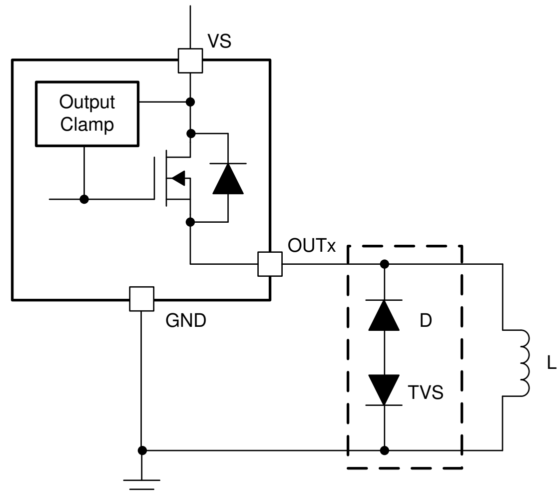


Figure 8-26. Protection with External Circuitry

Figure 8-27 shows the VDS clamp engaging during 5mH inductive load discharge. Figure 8-28 and Figure 8-29 shows maximum energy dissipation capability of the device during inductive load turn off.

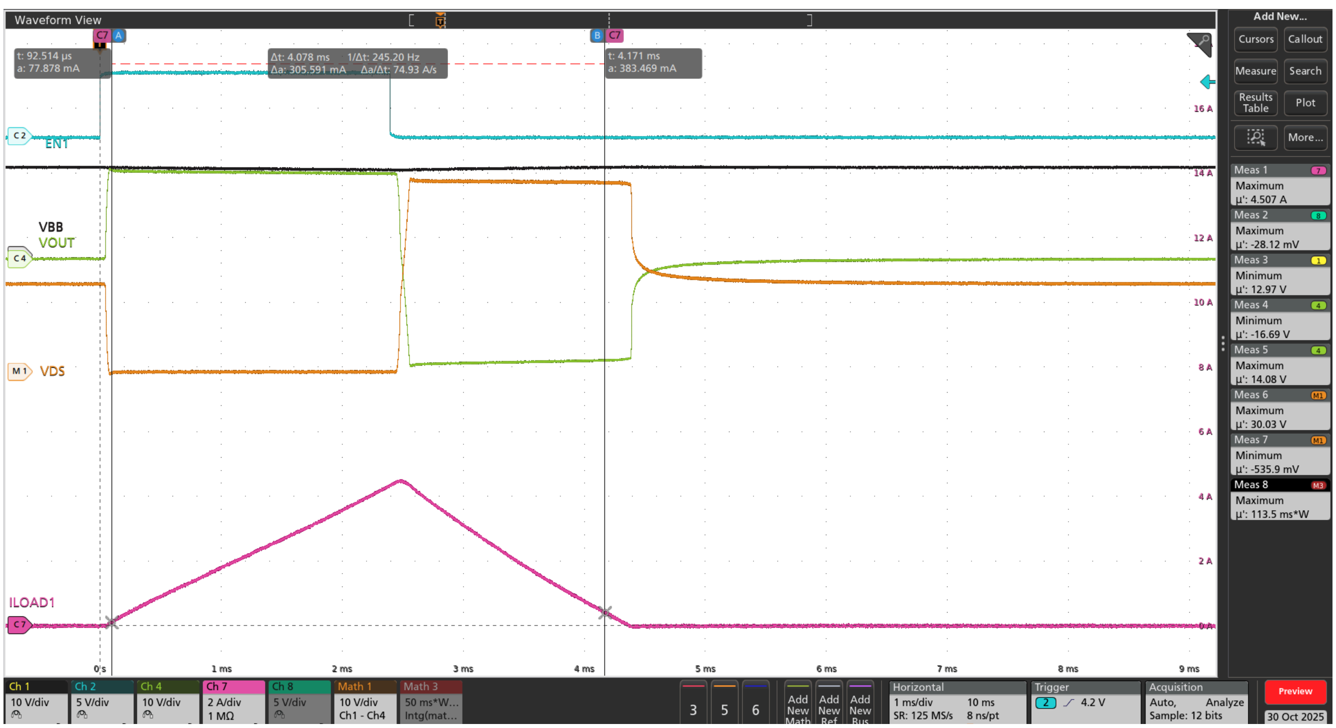


Figure 8-27. 5mH Inductive Load Driving (VBB = 13.5V, T_A = 25°C)

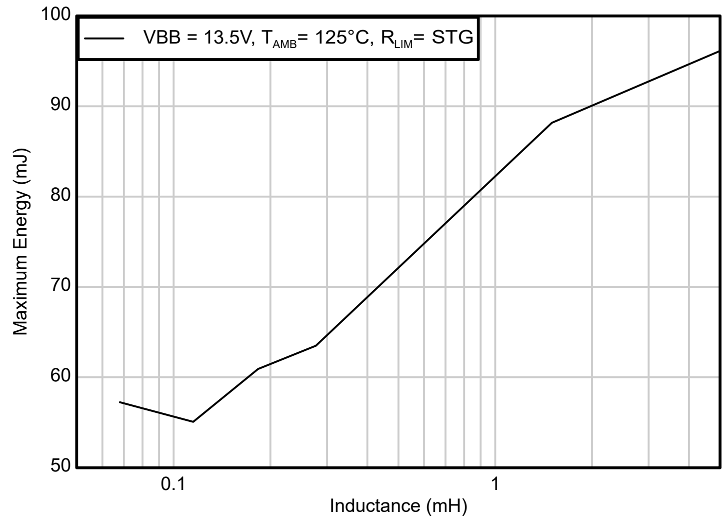


Figure 8-28. Maximum Energy Dissipation for Inductive Switch OFF vs Inductance (single pulse, VBB = 13.5V, T_A = 125°C)

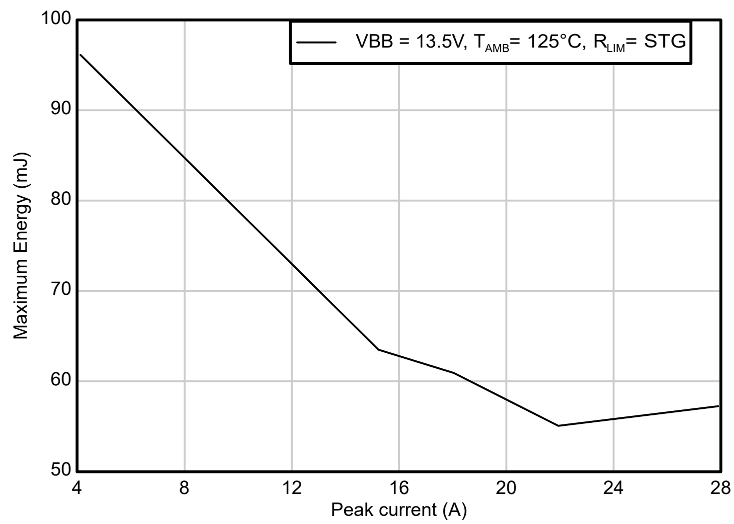


Figure 8-29. Maximum Energy Dissipation for Inductive Switch OFF vs Peak Current (single pulse, VBB = 13.5V, T_A = 125°C)

8.3.5 Slower Slew Rate Option

The TPS2HC08-Q1 offers device versions (D, B) with slower rising and falling slew rate for automotive seat heater applications. Such applications require that 10%-90% rise and fall times of the PWM currents must stay at or below 80A/msec. The slower slew rate helps reduce electromagnetic interference in the vehicle's electrical system. Without proper slew rate control, the fast switching of current in the seat heater application can cause EMC issues in the system.

8.3.6 Capacitive Load Charging

The TPS2HC08-Q1 incorporates an advanced adjustable current limiting circuit with thermal regulation that significantly improves system reliability by effectively managing inrush currents when charging large capacitive loads. The device also provides protection against current limit and overcurrent faults by turning off the smart high side switch. With no protection, charging a large capacitive load can lead to high inrush currents that pull a supply down, however by using the low thermal regulated current limit device options the capacitive load can be safely charged.

8.3.6.1 Adjustable Current Limiting for Inrush Control

Adjustable current limit feature of the device allows precise control of inrush current during capacitive load charging. By selecting an appropriate external resistor value on the ILIM pin, designers can:

- Tailor the maximum charging current to match specific capacitive load requirements.
- Protect upstream power supplies from excessive current draw during startup.
- Reduce PCB trace width requirements and connector sizing by limiting peak currents.
- Minimize voltage droop on the supply rail during capacitive charging.
- Enable the use of smaller, more cost-effective components throughout the system.

Figure 8-30 and Figure 8-31 compares the 1mF capacitive load charging at same conditions with device configured to minimum (ILIM pin OPEN) and maximum (ILIM pin shorted to ground (STG)) current limit setting. The lower current limit limits the inrush current while charging the 1mF capacitive load and provides clean startup of the load without triggering thermal shutdown.

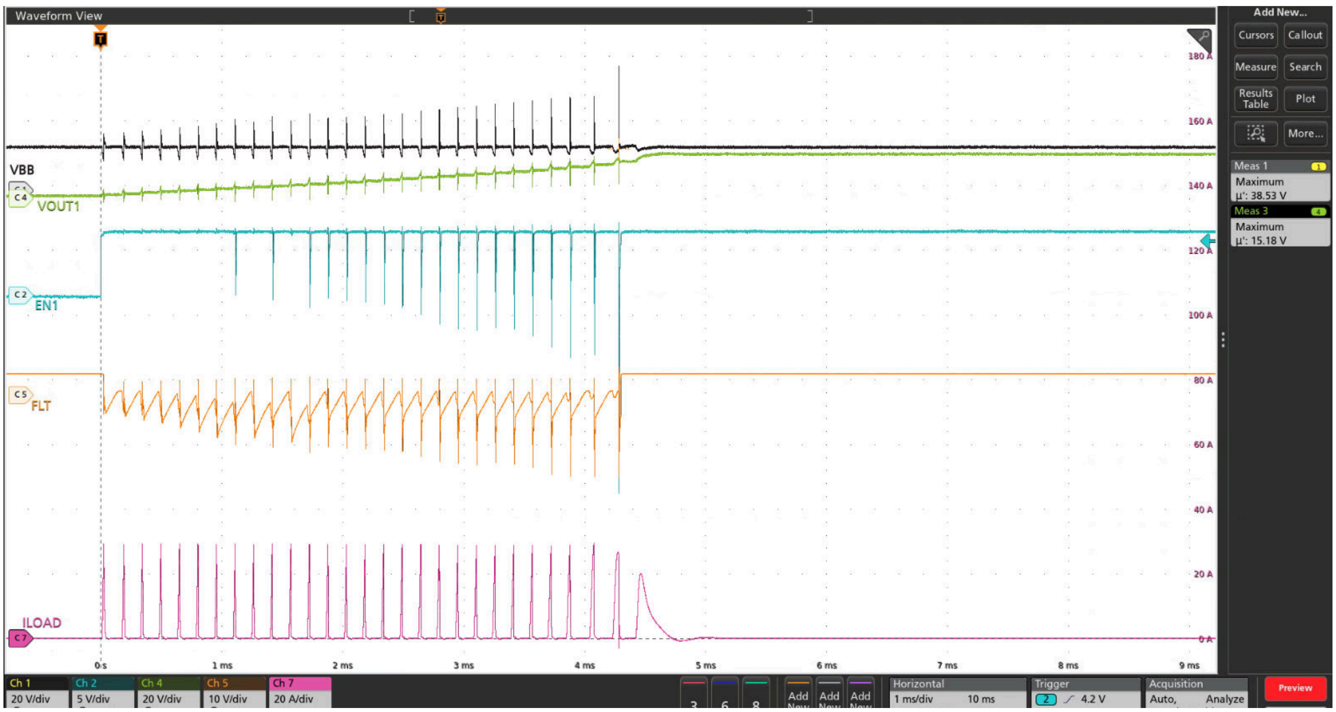


Figure 8-30. 1mF Capacitive Load Charging with Channel 1 of TPS2HC08-Q1 Device at 13.5V VBB, ILIM Pin shorted to ground and 125°C Ambient Temperature (no load on channel 2)

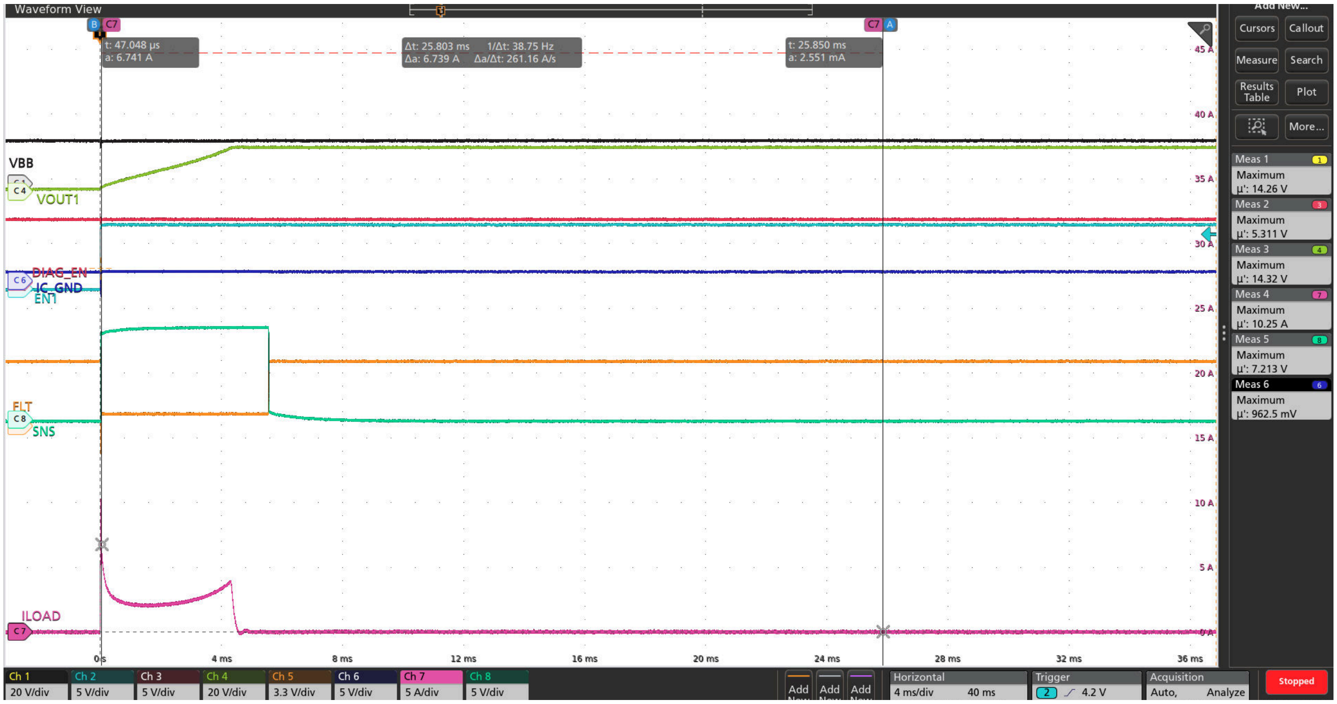


Figure 8-31. 1mF Capacitive Load Charging with Channel 1 of TPS2HC08-Q1 Device at 13.5V VBB, ILIM Pin OPEN and 125°C Ambient Temperature (no load on channel 2)

8.3.6.2 Current Limit with Thermal Regulation for Capacitive Loads

When configured with an external resistor on the ILIM pin, the TPS2HC08-Q1 enables thermal-regulated current limiting. The thermal regulation works through a negative feedback mechanism by continuously monitoring the relative temperature of the power FET ($T_{J,FET}$) compared to the controller temperature ($T_{J,CONTROLLER}$). As the temperature difference increases during high-current events, the device automatically reduces the current limit to maintain safe operation while allowing maximum charging current. This feature provides below advantages for capacitive load charging:

- **Expanded Capacitive Load Range**: The thermal-regulated current limiting significantly expands the range of capacitive loads that can be safely charged without triggering thermal shutdown, as shown in Figure 8-32. By dynamically adjusting current based on thermal conditions, the device can handle much larger capacitances than traditional high-side switches.
- **Elimination of Manual Pulsing**: Previously, without thermal regulation of current limit, customers often resorted to manually pulsing switches on and off to charge large capacitive loads. This approach introduced significant noise and EMI concerns into the system. The device thermal regulation eliminates the need for this practice.
- **Prevention of Thermal Runaway**: The thermal regulation implements a negative feedback loop that stabilizes the system during capacitive charging. As temperature rises, current is automatically reduced, preventing the uncontrolled thermal escalation seen in conventional switces.

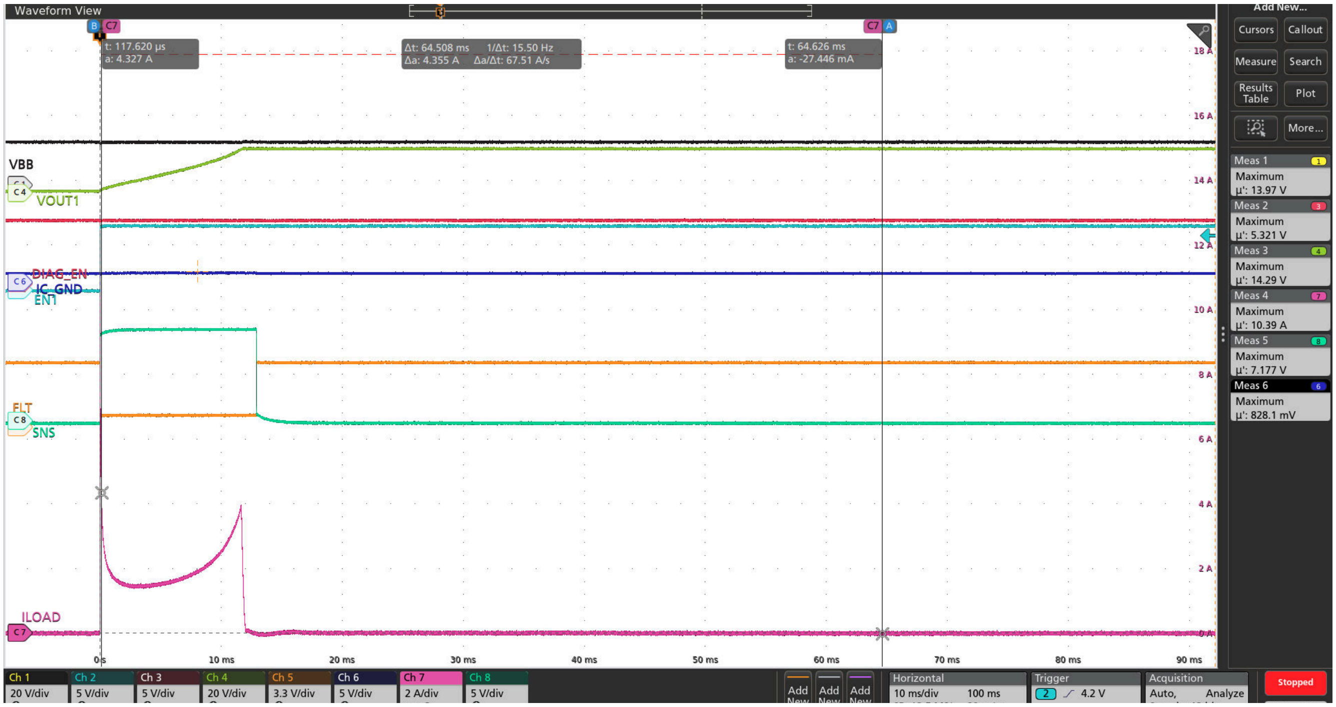


Figure 8-32. 2mF Capacitive Load Charging with Channel 1 of TPS2HC08-Q1 Device at 13.5V VBB, ILIM Pin OPEN and 125°C Ambient Temperature (no load on channel 2)

8.3.6.3 Retry Thermal Shutdown Behavior for Capacitive Loads

For large capacitive loads, device can trigger thermal shutdown fault and enter into retry thermal shutdown flow. In this case, the retry protection mechanism (Section 8.3.3) of the device allows load to turn on reliably with multiple retry cycles. For most properly sized capacitive loads, the thermal regulation can prevent reaching thermal shutdown conditions, resulting in smooth capacitive charging without interruption. Figure 8-30 shows capactive load charging with multiple thermal shutdown retry cycles. This behavior can be acceptable in applications where capacitive load has high enough load impedance connected in parallel, hence not discharging the capacitor significantly when the device is off during thermal shutdown.

8.3.6.4 Impact of DC Load on Capacitive Charging Capability

When designing systems with both capacitive and DC loads on the same channel, it's important to consider the combined thermal impact:

- **Thermal Budget Consumption**: Any DC load connected in parallel with a capacitive load consumes part of the device's thermal budget. The power dissipation from the DC load (I^2R) generates heat that raises the baseline temperature of the power FET.
- **Reduced Capacitive Charging Capability**: With a power dissipation across FET to DC load, the margin between operating temperature and thermal shutdown threshold is reduced. This effectively decreases the maximum capacitance that can be safely charged without triggering thermal shutdown.
- **Accelerated Thermal Shutdown**: The combined heating effect of DC load current and capacitive charging current can accelerate the onset of thermal shutdown. This can cause the device to enter the retry mechanism earlier and more frequently during capacitive charging.
- **Design Considerations**: When both load types must be supported simultaneously:
  - Select a more conservative (higher) R_{LIM} value to reduce the current limit.
  - Provide adequate PCB copper area for improved thermal dissipation.
  - For critical applications, consider using separate channels for DC and capacitive loads.

For more information on driving inductive or capacitive loads, reference TI's How To Drive Inductive, Capacitive, and Lighting Loads with Smart High Side Switch application report.

8.3.6.5 Device Capability

The table below shows some data for capacitive load charging across device family at VBB = 18V, T_A = 125°C. Only single channel is enabled for TPS2HC08-Q1 and TPS2HC16-Q1 devices.

Table 8-4. Capacitive Load Charging Results Across Device Family

PART NUMBER	ILIM	CAPACITIVE LOAD	CHARGING TIME	THERMAL SHUTDOWN TRIGGERED
TPS2HC08-Q1	OPEN	2mF	23ms	No
	GND	1mF	8ms	Yes
TPS2HC16-Q1	OPEN	47uF	1ms	No
	GND	220uF	5ms	Yes
TPS1HC08-Q1	OPEN	220uF	2.1ms	No
	GND	1mF	8ms	Yes
TPS1HC04-Q1	OPEN	680uF	3.1ms	No
	GND	470uF	2ms	Yes
TPS1HC03-Q1	OPEN	680uF	3.7ms	No
	OPEN	1mF	6ms	Yes

8.3.7 Bulb Charging

Figure 8-33 shows a simple bulb model as a combination of capacitive and resistive elements that define the startup and steady-state characteristics:

- **R_{inrush}** : The initial cold filament resistance that limits peak inrush current at startup.
- **C_{inrush}** : Represents the energy storage required for the filament to generate sufficient heat for proper illumination.
- **R_{dc}** : The steady-state hot filament resistance that determines normal operating current (Vbattery / R_{dc}).

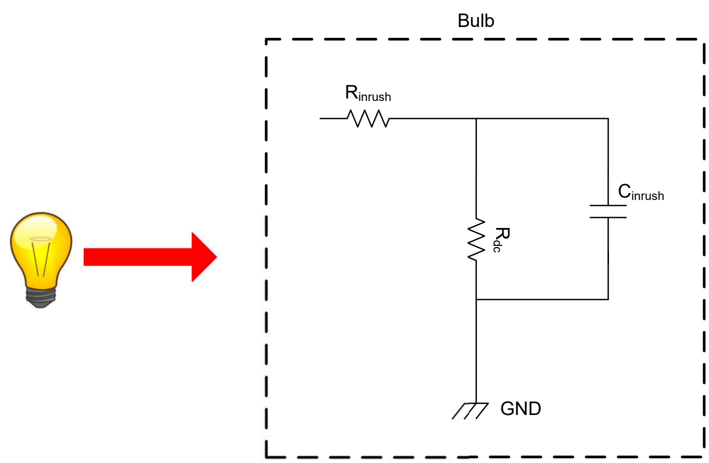


Figure 8-33. Simple Bulb Model

During cold startup, the filament resistance (R_{inrush}) can be 7-10 times lower than the steady-state value (R_{dc}), resulting in substantial inrush currents and need of low R_{ON} (on-resistance) switch.

In real environment, a bulb is introduced to many inductances and resistances when placed in a vehicle. Figure 8-34 shows simplified vehicle architecture model in real environment consisting of below complex electrical network that significantly affects the bulb turn-on behavior and peak current.

- **$R_{vehicle}$** : The total wire harness and connector resistance in the path from battery to chassis ground excluding $R_{ds,on\ switch}$ (R_{ON} of the switch) typically ranges from 45mΩ to 130mΩ in production vehicles. The short and long cable harness length typically makes 50mΩ and 100mΩ of $R_{vehicle}$ respectively.
- **$L_{vehicle}$** : Wire harness inductance affects current slew rate and turn-on timing.
- **System resistances**: Connector contact resistance and ground path resistance contribute to the overall circuit behavior.

The three primary components that determine peak inrush current during bulb charging are:

- **$R_{vehicle}$** : Higher vehicle resistance reduces peak current.
- **$R_{ds,on\ switch}$** : The switch's on-resistance (R_{ON}) contributes to current limiting.
- **R_{inrush}** : The cold filament resistance of the specific bulb.

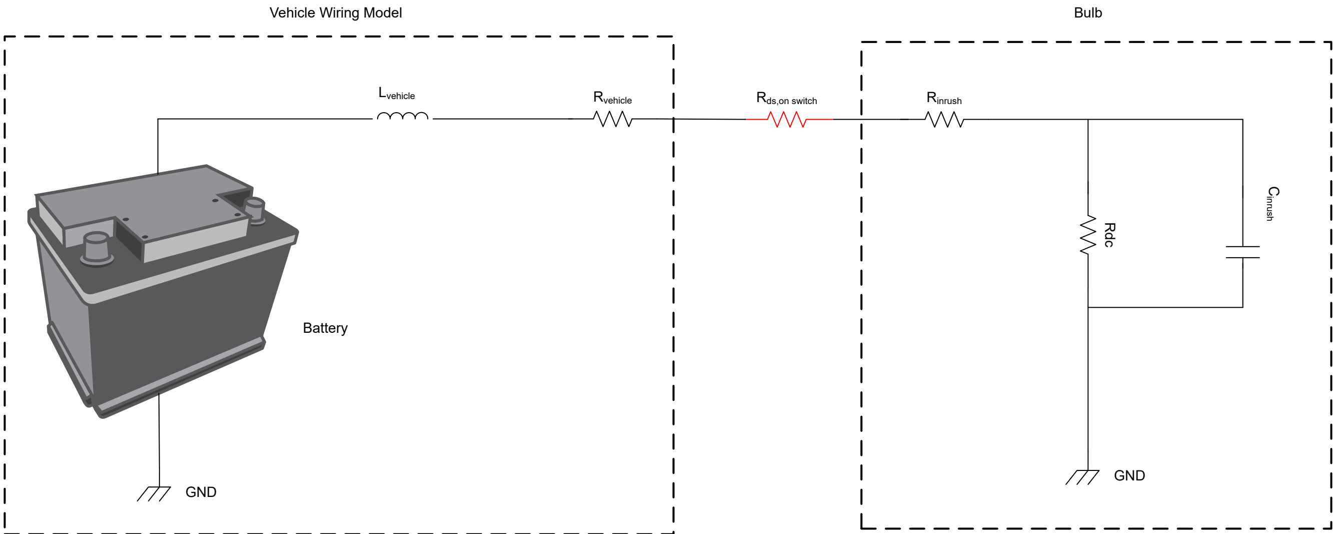


Figure 8-34. Simplified Vehicle Architecture Model

8.3.7.1 Non-Thermal Regulated Mode for Bulb Loads

For bulb loads with high inrush currents, the TPS2HC08-Q1 offers a specialized non-thermal regulated current limit mode that can be enabled by connecting the ILIM pin directly to GND. This mode provides consistent and predictable current limiting behavior regardless of temperature conditions with below device features.

- Maintains a fixed current limit of 25A regardless of temperature.
- Allows the device to handle the high initial current demand.

Figure 8-35 shows the 35W bulb charging behavior of the device in non-thermal regulated current limit mode, set by grounding the ILIM pin. In non-thermal regulated mode, device is able to meet the high inrush current demand of the bulb load and turns on in < 10ms.

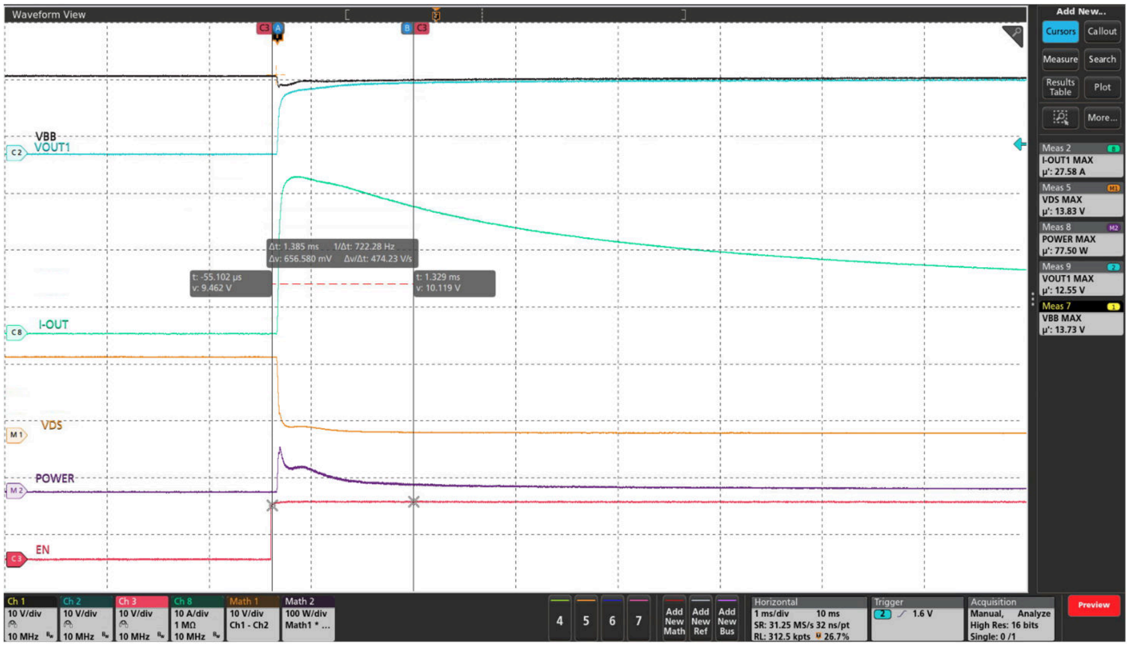


Figure 8-35. 35W Bulb Charging with TPS2HC08-Q1 Single Channel at 13.5V VBB, $T_{A\ (device)}$= 25°C, $T_{A\ (bulb)}$ = 25°C, ILIM = GND

8.3.7.2 Thermal Management During Bulb Inrush

For high wattage bulb loads or at cold temperature startup or high VBB voltage, with high inrush current demand, the device employs sophisticated thermal protection mechanisms:

- **Relative Thermal Shutdown**

  During high-inrush events, toggling of the switch output can be observed due to the FET heating up rapidly. When this occurs, the device enters a relative thermal shutdown ($T_{J,FET}$ - $T_{J,CONTROLLER}$ > T_{REL}) state and auto-recovers from this event within t_{RETRY_INT}. This rapid recovery allows the bulb to continue charging while preventing excessive thermal stress on the device.
- **Absolute Thermal Shutdown**

  If the junction temperature continues to rise despite relative thermal protection, an absolute thermal shutdown event occurs when the FET temperature exceeds T_{ABS} . In this case, the switch turns off to protect the device and auto-recovers from this event within t_{RETRY_EXT} once the temperature decreases sufficiently, resuming bulb charging.

Figure 8-36 shows the 35W bulb (at cold condition) charging behavior of the device in non-thermal regulated current limit mode, set by grounding the ILIM pin. The device engages in relative thermal shutdown protection and turns on the bulb after few cycles.

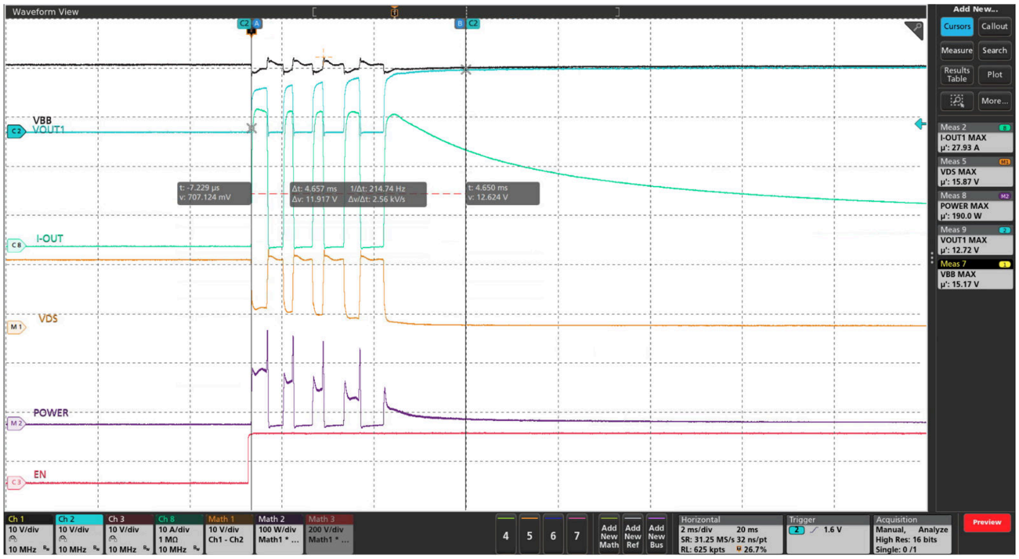


Figure 8-36. 35W Bulb Charging with TPS2HC08-Q1 Single Channel at 13.5V VBB, $T_{A\ (device)}$= 25°C, $T_{A\ (bulb)}$ = -40°C, ILIM = GND

8.3.7.3 Device Capability

The table below shows some data for bulb load charging across device family at VBB = 13.5V, T_A = -40°C. Only single channel is enabled for TPS2HC08-Q1 and TPS2HC16-Q1 devices.

Table 8-5. Bulb Load Charging Results Across Device Family (with short cable length, $R_{vehicle}$ = 50mohm)

PART NUMBER	ILIM	BULB LOAD	CHARGING TIME	THERMAL SHUTDOWN TRIGGERED
TPS2HC08-Q1	GND	35W	4.5ms	Yes
TPS2HC16-Q1	GND	27W	40ms	Yes
TPS1HC08-Q1	GND	35W	4.5ms	Yes
TPS1HC04-Q1	GND	60W	3.2ms	No
	GND	100W	6ms	Yes
TPS1HC03-Q1	GND	4 x 27W (with long cable harness length)	25ms	Yes
	GND	2 x 27W	1ms	Yes
	GND	35W	2ms	No

8.3.8 Fault Detection and Reporting

8.3.8.1 Diagnostic Enable Function

The DIAG_EN pin enables or disables the diagnostic functions. If multiple devices are used, but the ADC resource is limited in the microcontroller, the MCU can use GPIOs to set DIAG_EN high to enable the diagnostics of one device while disabling the diagnostics of the other devices by setting DIAG_EN low. In addition, the device can keep the power consumption to a minimum by setting DIAG_EN and all EN signals low.

Table 8-6. Diagnosis Configuration Table

DIAG_EN	ENx	SEL	SNS ACTIVATED CHANNEL	SNS	$\overline{FLT}$	PROTECTIONS AND DIAGNOSTICS
L	H	—	—	High impedance	See Table 8-8	SNS disabled, $\overline{FLT}$ reporting, full protection
	L				High impedance	Diagnostics disabled, no protection

Table 8-6. Diagnosis Configuration Table (continued)

DIAG_EN	ENx	SEL	SNS ACTIVATED CHANNEL	SNS	$\overline{FLT}$	PROTECTIONS AND DIAGNOSTICS
H	—	0	Channel 1	See Table 8-8	See Table 8-8	See Table 8-8
		1	Channel 2			

8.3.8.2 $\overline{FLT}$ Reporting

In active state with ENx high, the global $\overline{FLT}$ pin is used to monitor the global fault condition among the two channels regardless of DIAG_EN status. In case of off state diagnostics with ENx low, global $\overline{FLT}$ pin monitors the global fault condition among the two channels when DIAG_EN is high. When a fault condition occurs on any channel, the $\overline{FLT}$ pin is pulled down to GND. A 3.3V or 5V external pullup is required to match the supply level of the microcontroller.

After the $\overline{FLT}$ report, the microcontroller can check and identify the channel in fault status by the multiplexed current sensing. The SNS pin also works as a fault report by giving I_{SNSFH} current output when DIAG_EN is high.

8.3.8.3 $\overline{FLT}$ Timings

The below table shows the $\overline{FLT}$ pin timings.

Table 8-7. $\overline{FLT}$ Timings

CONDITION	TIMING
Open load or STB fault to $\overline{FLT}$ assertion in DIAGNOSTIC state.	See Section 8.3.9.1.2 (t_{OL}, t_{OL1}, t_{OL2})
Any other fault occurence to $\overline{FLT}$ assertion	See t_{FAULT_FLT}
Fault clearance to $\overline{FLT}$ reset	The internal design architecture causes maximum 1ms delay for $\overline{FLT}$ signal to reset from the fault clearance event.

8.3.8.4 Fault Table

The below table shows the response of the FLT (regardless of DIAG_EN being high) and SNS (with DIAG_EN being high) pins during different conditions.

Table 8-8. Fault Table

CONDITIONS	ENx	OUTx	CRITERION	SNS (with DIAG_EN high)	$\overline{FLT}$ (with external pull-up)	BEHAVIOR	FAULT RECOVERY
Normal	L	L	—	High Impedance	H	Normal	—
	H	VBB - I_{LOAD} × R_{ON}	—	I_{LOAD}/ K_{SNS}	H	Normal	—
Overcurrent	H	VBB - I_{LIM} × R_{ON}	Current limit triggered	I_{SNSFH}	L	Holds the current at the current limit until thermal shutdown or when the overcurrent event is removed	Auto-retry or latch, see Section 8.3.3
Hot short	H	L	output shorted to ground	I_{SNSFH}	L	Device will immediately shutdown, and reenable into current limit.	Auto-retry or latch, see Section 8.3.3

Table 8-8. Fault Table (continued)

CONDITIONS	ENx	OUTx	CRITERION	SNS (with DIAG_EN high)	$\overline{FLT}$ (with external pull-up)	BEHAVIOR	FAULT RECOVERY
Enable into permanent short	L to H	L	output shorted to ground	I_{SNSFH}	L	Device will enable into current limit until thermal shutdown.	Auto-retry or latch, see Section 8.3.3
Open load, short to battery (STB)	L	H	VBB – V_{OUT} < V_{OL}	I_{SNSFH}	L (when DIAG_EN is high)	Internal pull-up resistor is active to detect open load fault.	Auto
	H	H		I_{LOAD}/ K_{SNS}	H	Normal behavior. User can make judgement based on SNS pin output.	—
Absolute Thermal shutdown	H	—	T_{ABS} triggered	I_{SNSFH}	L	Shuts down when devices hits absolute thermal shutdown.	Auto-retry or latch, see Section 8.3.3
Relative Thermal Shutdown	H	—	T_{REL} triggered	I_{SNSFH}	L	Shuts down when devices hits relative thermal shutdown.	Auto-retry or latch, see Section 8.3.3

8.3.9 Full Diagnostics

8.3.9.1 Open-Load Detection

8.3.9.1.1 Channel On

If a channel is on and the DIAG_EN = Logic High, then the high accuracy current sense of the device can be used to detect open-loads in the on state through an external ADC. Please note there is no detection reported on the $\overline{FLT}$ pin. Determination of an open-load while a channel is on must be made by the user or system.

8.3.9.1.2 Channel Off

Open load detection is available in the off state if DIAG_EN = Logic High. If a channel is off and a load is connected to the channel, the output voltage is pulled low to ≅0V by the load. In the case of an open load on the channel, the output voltage is close to the supply voltage, VBB – V_{OUTx} < V_{OL}. The FLT pin goes low to indicate a fault to the MCU. If the particular channel experiencing the open load fault is selected through the SEL pin, then the SNS pin outputs I_{SNSFH} fault current. If the channel is not selected through the SEL pin then the SNS pin does not show I_{SNSFH} until the channel is selected through the SEL pin. There is always a leakage current $I_{OL,OFF}$ present on the output, due to the internal logic control path or external humidity, corrosion, and so forth. Thus, the device implements an internal pullup resistor (R_{PU}) on each channel to offset the leakage current. This pullup current must be less than the output load current to avoid false detection in the normal operation mode. To reduce the standby current, the device implements a switch and pullup resistor on each channel which is controlled by the DIAG_EN pin and the EN pin for that channel.

There are two settings for the open-load detection delay - 0.4ms (for P and D variants) and 2.4ms (for M and B variants). The 2.4ms open load detection delay represents the delay for the internal pullup (R_{PU}) resistor to engage between VBB and V_{OUTx} pins. This allows user to do fast DIAG_EN sequencing (DIAG_EN high pulse < 2.4ms) when SNS pins of multiple devices are tied to common R_{SNS} for MCU current sense reading. In this case, the open load fault will not engage for disabled devices during current sense read.

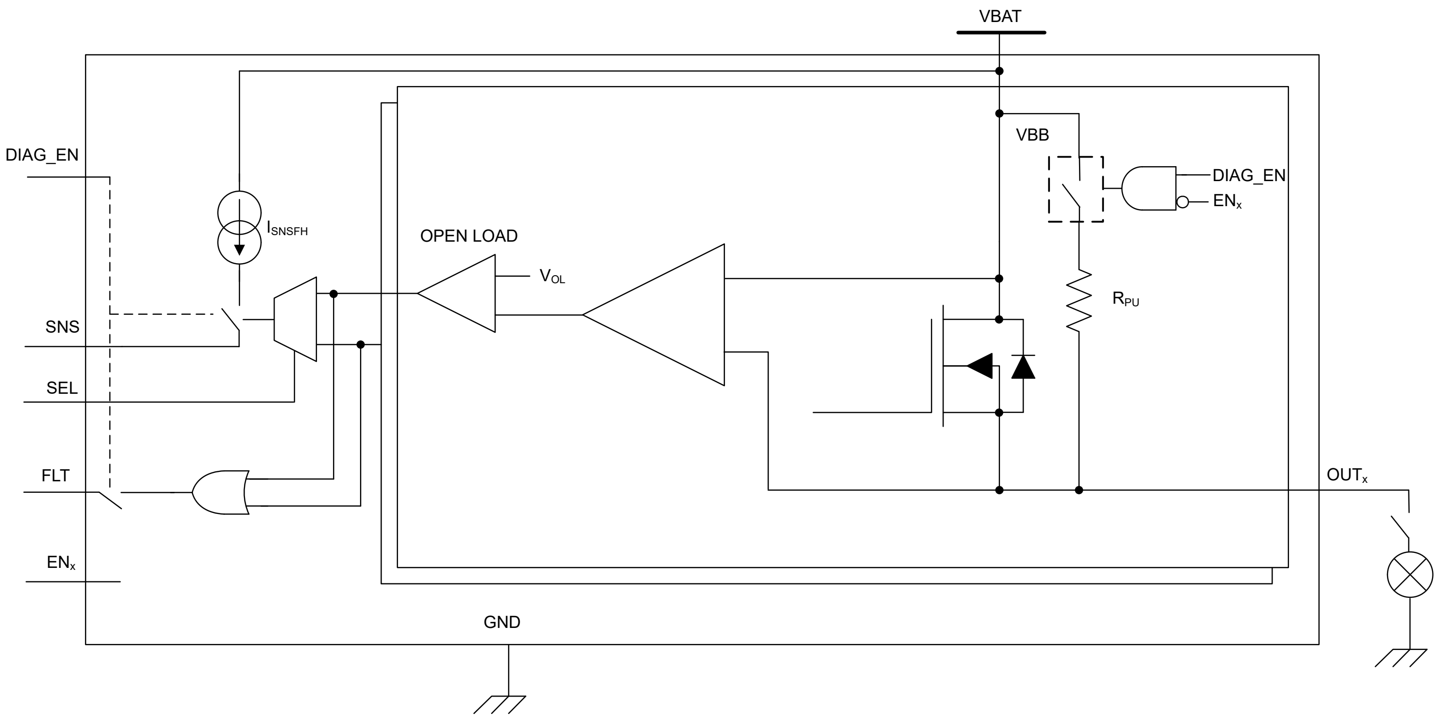
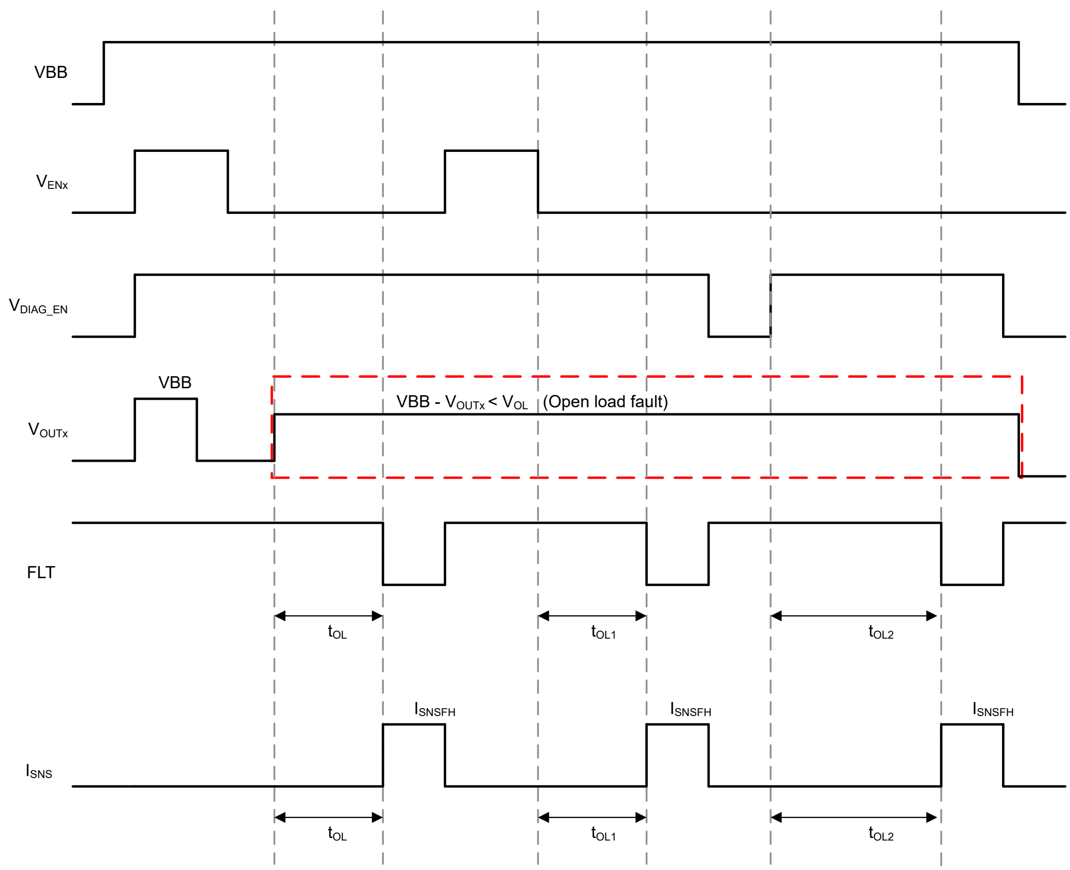


Figure 8-37. Open-Load Detection in Off-State



Note

Rise and fall times of control signals are 100ns. Control signals include: ENx, DIAG_EN and SEL.

Both the channels have same open-load detection timings with appropriate SEL setting.

Figure 8-38. Open-load Detection Timing Characteristics

8.3.9.2 Short-to-Battery Detection

Short-to-battery detection has the same detection mechanism and behavior as open-load detection, both in the on-state and off-state. See Table 8-8 for more details.

8.3.9.3 Reverse-Polarity and Battery Protection

Reverse-polarity, commonly referred to as reverse battery, occurs when the ground of the device goes to the battery potential, $V_{GND} = V_{BAT}$, and the supply pin goes to ground, VBB = 0V. In this case, if the EN pin has a path to the *ground* plane, then the FET turns on to lower the power dissipation through the main channel and prevent current flow through the body diode. Note that the resistor/diode ground network (if there is not a central blocking diode on the supply) must be present for the device to protect the device during a reverse battery event. The ground protection network will cause the device ground to be at a higher potential than the module ground (and microcontroller ground). This offset needs to be accounted for in logic pins interface between the device and the microcontroller.

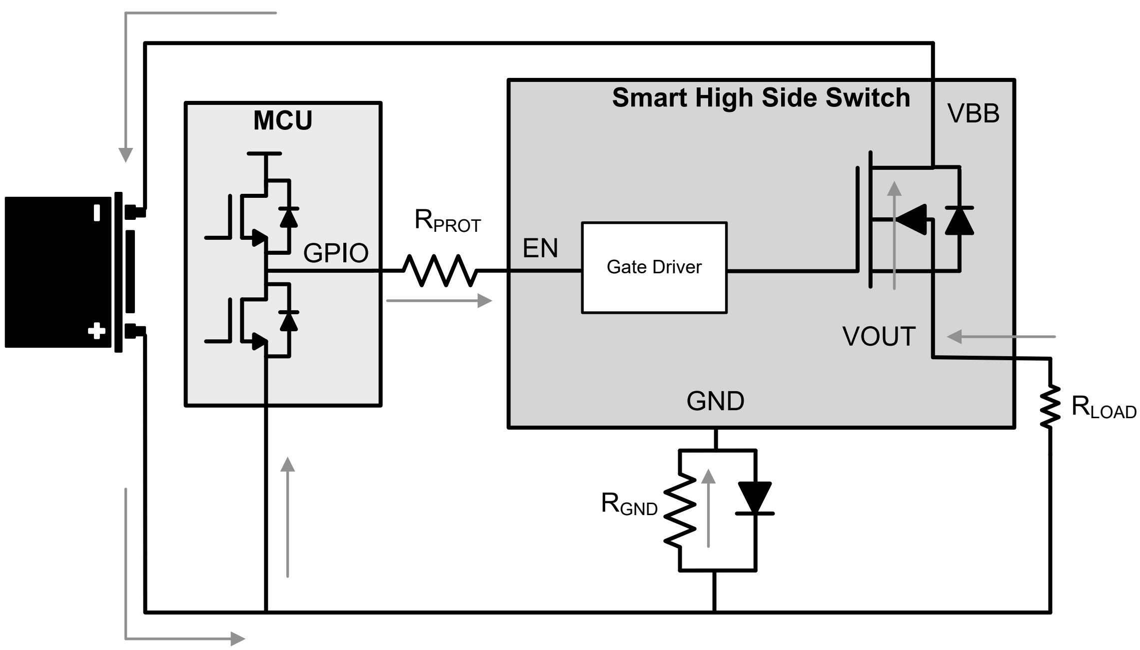


Figure 8-39. Reverse Battery Circuit

For more external protection circuitry information, see *Reverse Current Protection*.

8.3.10 Full Protections

8.3.10.1 UVLO Protection

The device monitors the supply voltage VBB, to prevent unpredicted behaviors when VBB is too low. When VBB falls down to V_{UVLOF}, the device shuts down. When VBB rises up to V_{UVLOR}, the device turns on.

8.3.10.2 Loss of GND Protection

When loss of GND occurs, output is turned off regardless of whether the enable signal is high or low.

Case 1 (loss of device GND): loss of GND protection is active when the thermal pad (Tab), IC_GND, and current limit ground are one trace connected to the system ground, as shown in Figure 8-40.

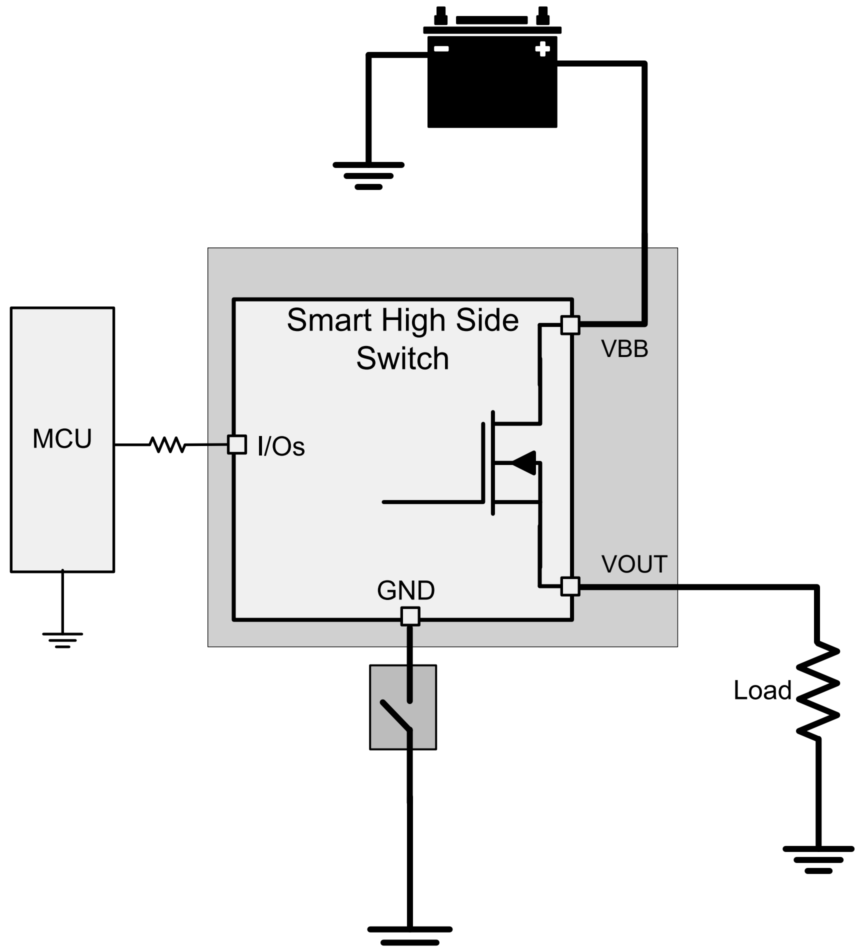


Figure 8-40. Loss of Device GND

Case 2 (loss of module GND): when the whole ECU module GND is lost, protections are also active. At this condition, the load GND remains connected.

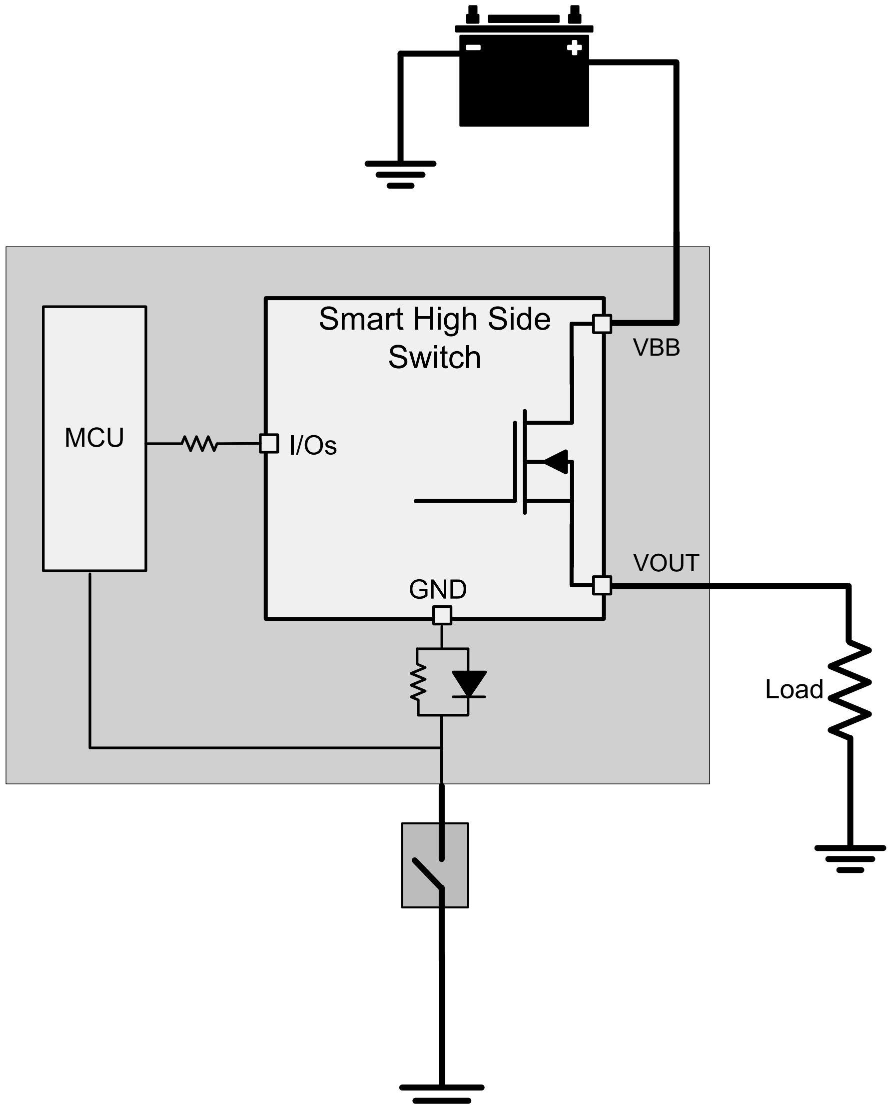


Figure 8-41. Loss of Module GND

8.3.10.3 Loss of Power Supply Protection

When loss of supply occurs, output is turned off regardless of whether the input is high or low. For a resistive or capacitive load, loss of supply protection is easy to achieve due to no more power. The worst case is a charged inductive load. In this case, the current is driven from all of the IOs to maintain the inductance output loop. TI recommends either the MCU serial resistor plus the GND network (diode and resistor in parallel) or external free-wheeling circuitry.

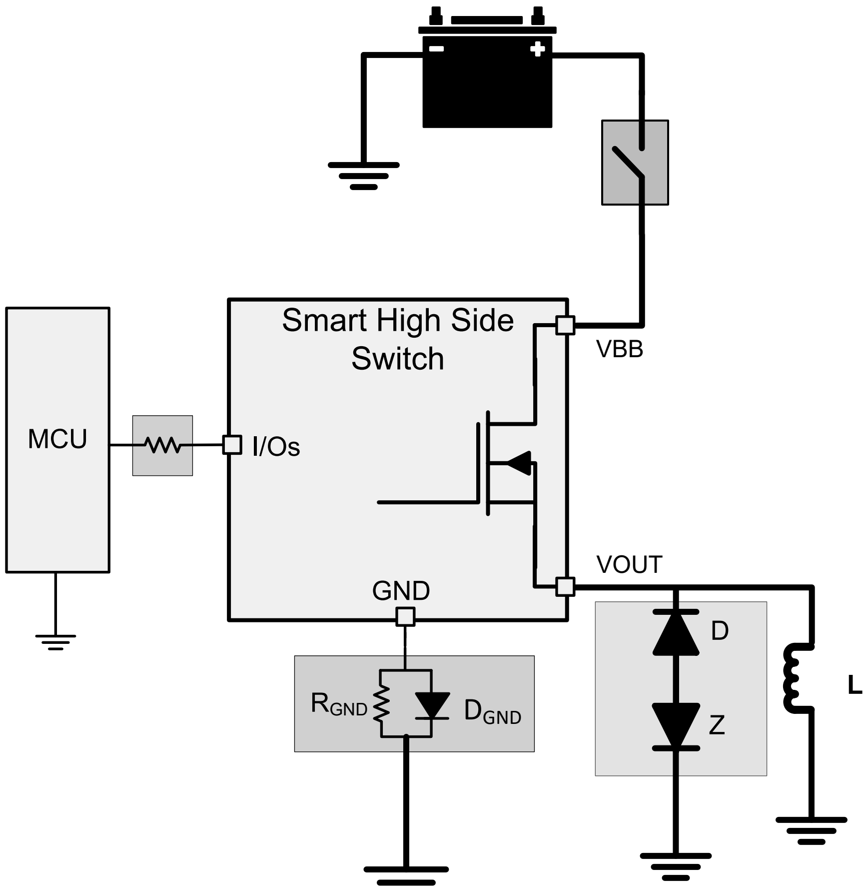


Figure 8-42. Loss of Battery

8.3.10.4 Reverse Current Protection

Method 1: block diode connected with VBB. Both the device and load are protected when in reverse polarity. The blocking diode does not allow any of the current to flow during reverse battery condition.

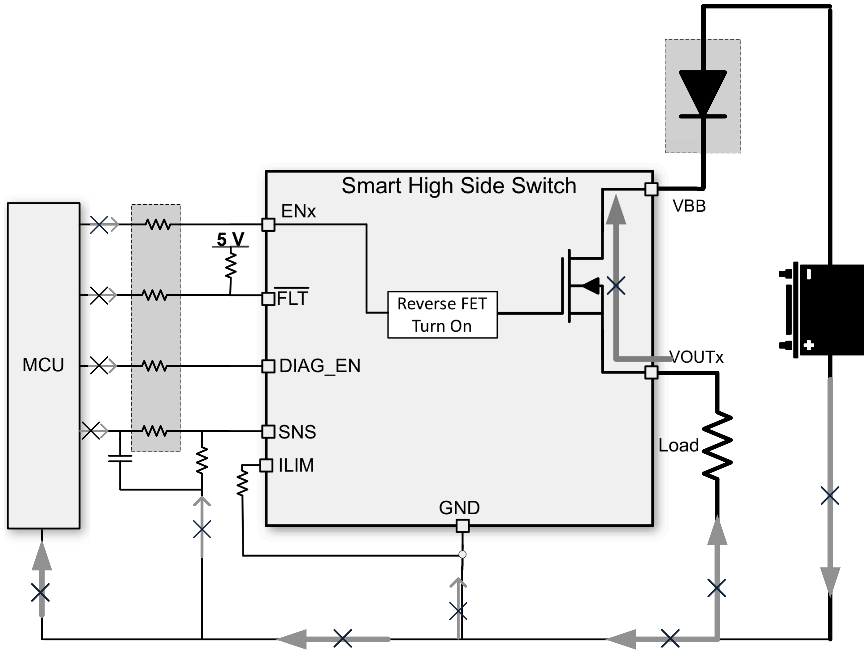


Figure 8-43. Reverse Protection with Block Diode

Method 2 (GND network protection): only the high-side device is protected under this connection. The load reverse current is limited by the impedance of the load. When reverse polarity happens, the continuous reverse current through the power FET must not make the heat build up be greater than the absolute maximum junction temperature. This can be calculated using the $R_{ON(REV)}$ value and the $R_{\theta JA}$ specification. In the reverse battery condition, the FET must come on to lower the power dissipation. This action is achieved through the path from EN to system ground where the positive voltage is being applied. No matter what types of connection are between the device GND and the board GND, if a GND voltage shift happens, verify that the following proper connections for the normal operation:

- Connect the current limit programmable resistor to the device GND.

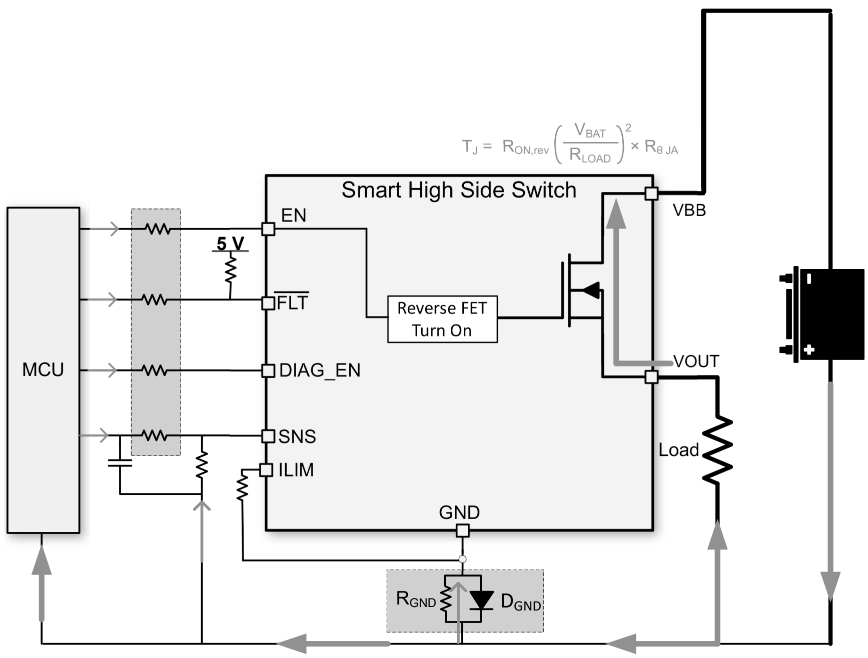


Figure 8-44. Reverse Protection with GND Network

- **Recommendation – resistor and diode in parallel:** a peak negative spike can occur when the inductive load is switching off, which can damage the HSS or the diode. So, TI recommends a resistor in parallel with the diode when driving an inductive load. The recommended selection are a 4.7kΩ resistor in parallel with an I_F > 100mA diode. If multiple high-side switches are used, the resistor and diode can be shared among devices.
- **Ground Resistor:** The higher resistor value contributes to a better current limit effect when the reverse battery or negative ISO pulses.

$$R_{GND} \geq \frac{(-V_{CC})}{(-I_{GND})} \tag{8}$$

  where

  – $-V_{CC}$ is the maximum reverse battery voltage (typically –16V).
  – $-I_{GND}$ is the maximum reverse current the ground pin can withstand, which is available in the *Absolute Maximum Ratings*.
- **Ground Diode:** A diode is needed to block the reverse voltage, which also brings a ground shift (≅600mV). Additionally, the diode must be ≅200V reverse voltage for the ISO 7637 pulse 1 testing so that the diode does not get biased.

8.3.10.5 Protection for MCU I/Os

In many conditions, such as the negative ISO pulse, or the loss of battery with an inductive load, a negative potential on the device GND pin can damage the MCU I/O pins (more likely, the internal circuitry connected to the pins). Therefore, the serial resistors between MCU and HSS are required.

Also, for proper protection against loss of GND, TI recommends 10kΩ resistance for the R_{PROT} resistors.

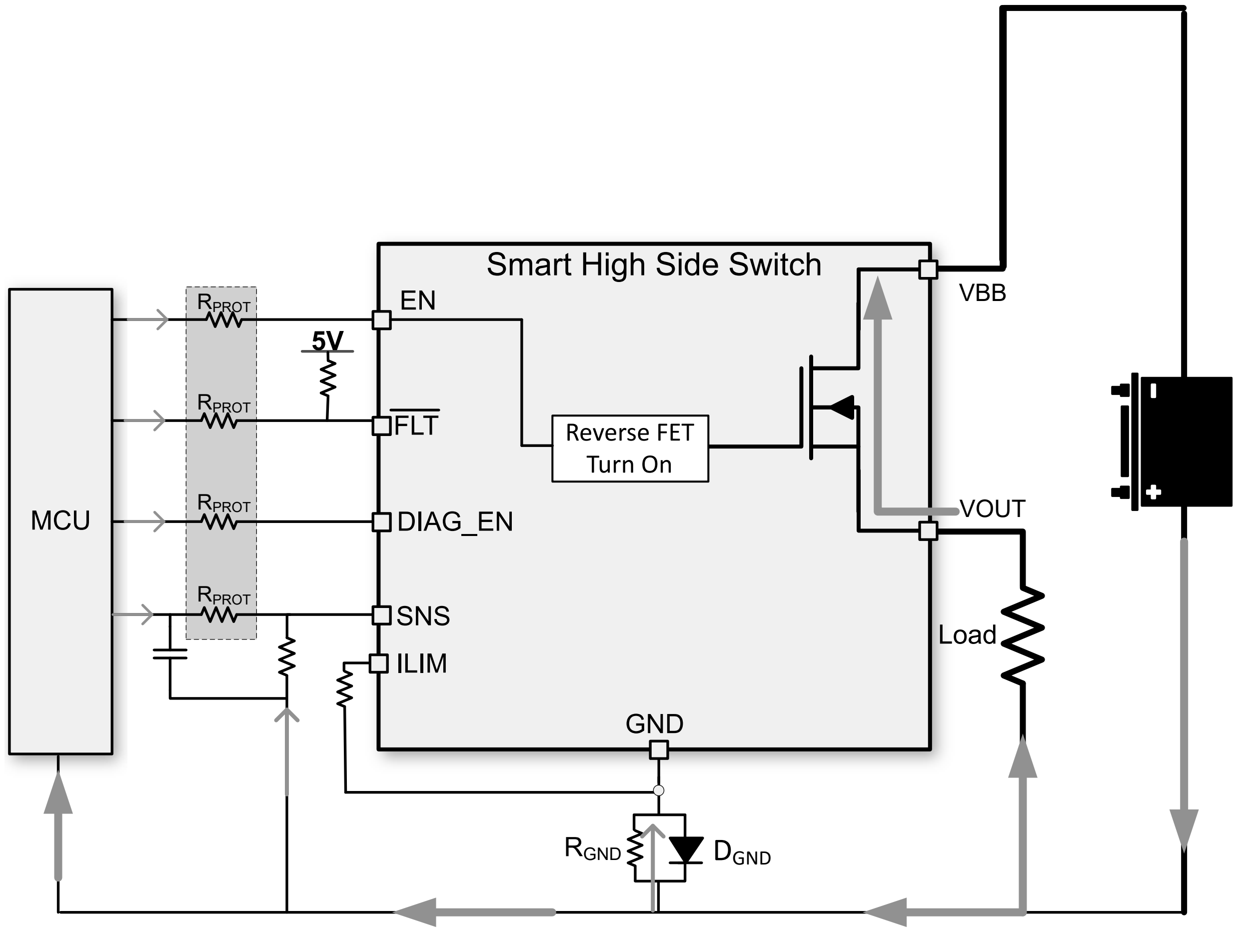


Figure 8-45. MCU I/O Protections

8.4 Device Functional Modes

The device has several states to transition into based on the ENx pin, DIAG_EN pin, and VBB voltage. The different states are referenced throughout the data sheet.

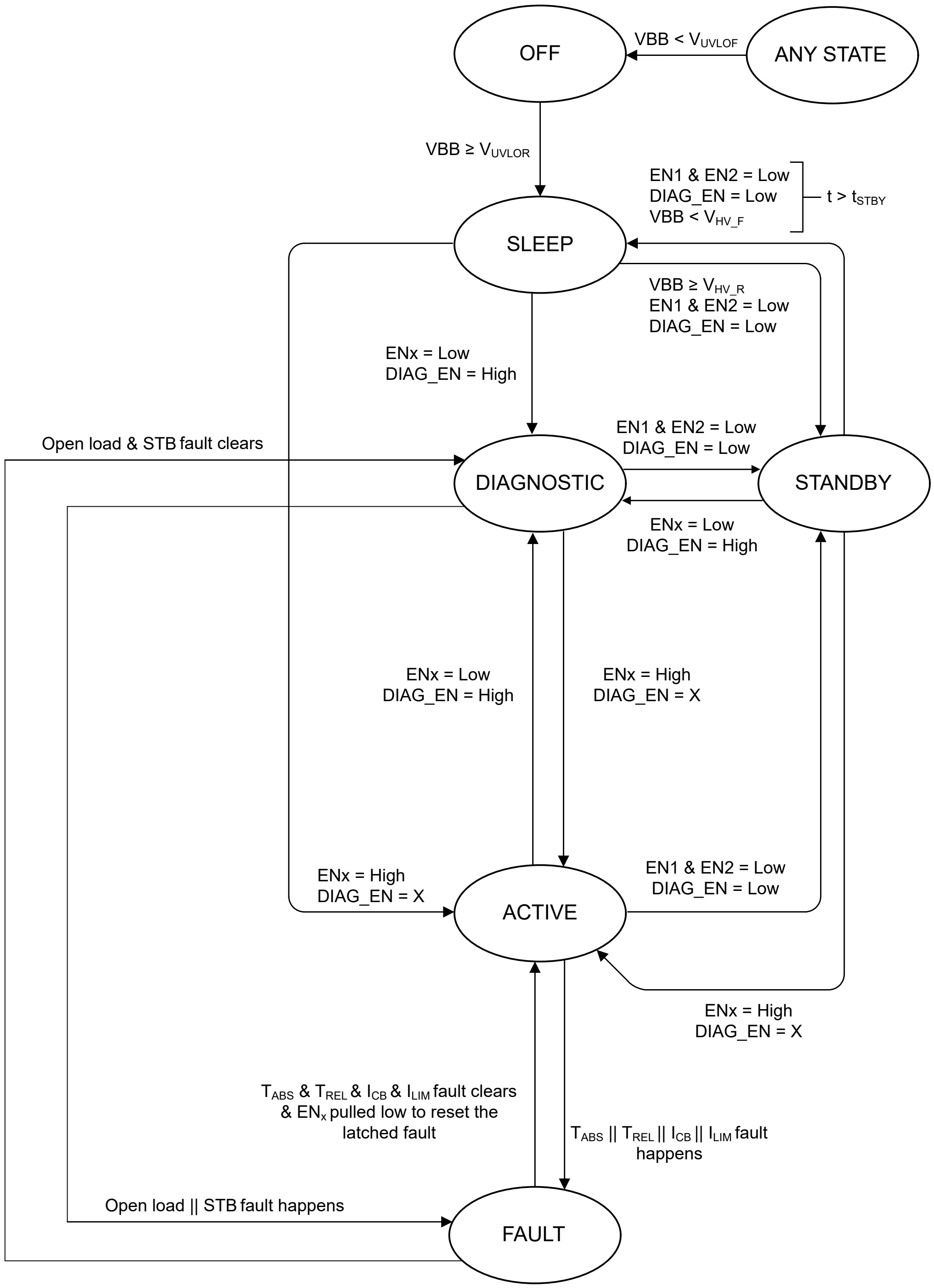


Figure 8-46. State Diagram

OFF

Device OFF state and occurs when the VBB voltage of the device is below the V_{UVLOF}.

SLEEP

This device state is entered from STANDBY state when all the ENx pins are pulled low for duration more than t_{STBY} amount of time and VBB is lower than V_{HV_F}. Outputs are all turned off. In the SLEEP state, all blocks inside the device are turned off and the current into the VBB is I_{SLEEP}. From SLEEP, the device can transfer into the ACTIVE state if any of the ENx pins are pulled high, the DIAGNOSTIC state if the DIAG_EN pin, without any of the ENx pins, goes high, or the STANDBY state if VBB is greater than V_{HV_R}.

STANDBY

The device STANDBY state is entered when the ENx pins are all low. Outputs are all turned off and the DIAG_EN pin is also low but there has not yet been t_{STBY} amount of time. This state is included so that the channel outputs can be modulated using PWM without any of the internal rails being cut off and put to SLEEP state. Once the device has waited t_{STBY} and VBB is less than V_{HV_F}, the device completely shuts down and transitions into SLEEP state. However, if the time is less than t_{STBY} and if either ENx pins were to go high, the device transitions into ACTIVE state. Similarly if the DIAG_EN goes high, the device transitions into DIAGNOSTIC state.

DIAGNOSTIC

The channel DIAGNOSTIC state is entered when the associated ENx pin is low and the DIAG_EN pin is high. Open-load or short-to-battery can be diagnosed in this state. Channel specific open load switch is enabled in this state. The device signals a $\overline{FLT}$ if any of the channels experience either an open-load or short-to-battery. The SNS pin outputs I_{SNSFH} current if the channel that has a fault is selected through the SEL pin.

ACTIVE

A channel enters ACTIVE state when the output is on by the associated ENx pin. In the ACTIVE state, the current limit value is set by the external resistor on the ILIM pin. If the DIAG_EN pin is pulled high while in the ACTIVE state, the SNS pin outputs a proportional current to the load current of the channel associated to the SEL pin configuration until a fault occurs on that channel. Additionally the $\overline{FLT}$ pin reports if there is a fault occurring on any channel. Any device channel can transition out of ACTIVE state to DIAGNOSTIC state by pulling the associated ENx low and keeping DIAG_EN high. The device can transition out of the ACTIVE state to STANDBY state by turning off all of the channels with DIAG_EN pulled low.

FAULT

The channel FAULT state occurs when the associated ENx pin is high but some event has caused the channel to behave differently from normal operation. These fault events include: absolute thermal shutdown, relative thermal shutdown, current limit, open load and short to battery faults. Each of these fault events either directly or eventually shut off the channel to protect the device and system.

9 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

9.1 Application Information

The TPS2HC08-Q1 device is capable of driving a wide variety of resistive, inductive, and capacitive loads, including bulbs, LEDs, relays, solenoids, heaters, and sub-modules. Full diagnostics and high-accuracy current-sense features enable intelligent control of the load. An external adjustable current limit improves the reliability of the whole system by clamping the inrush or overload current.

9.2 Typical Application

The following figure shows an example of the external circuitry connections for TPS2HC08-Q1.

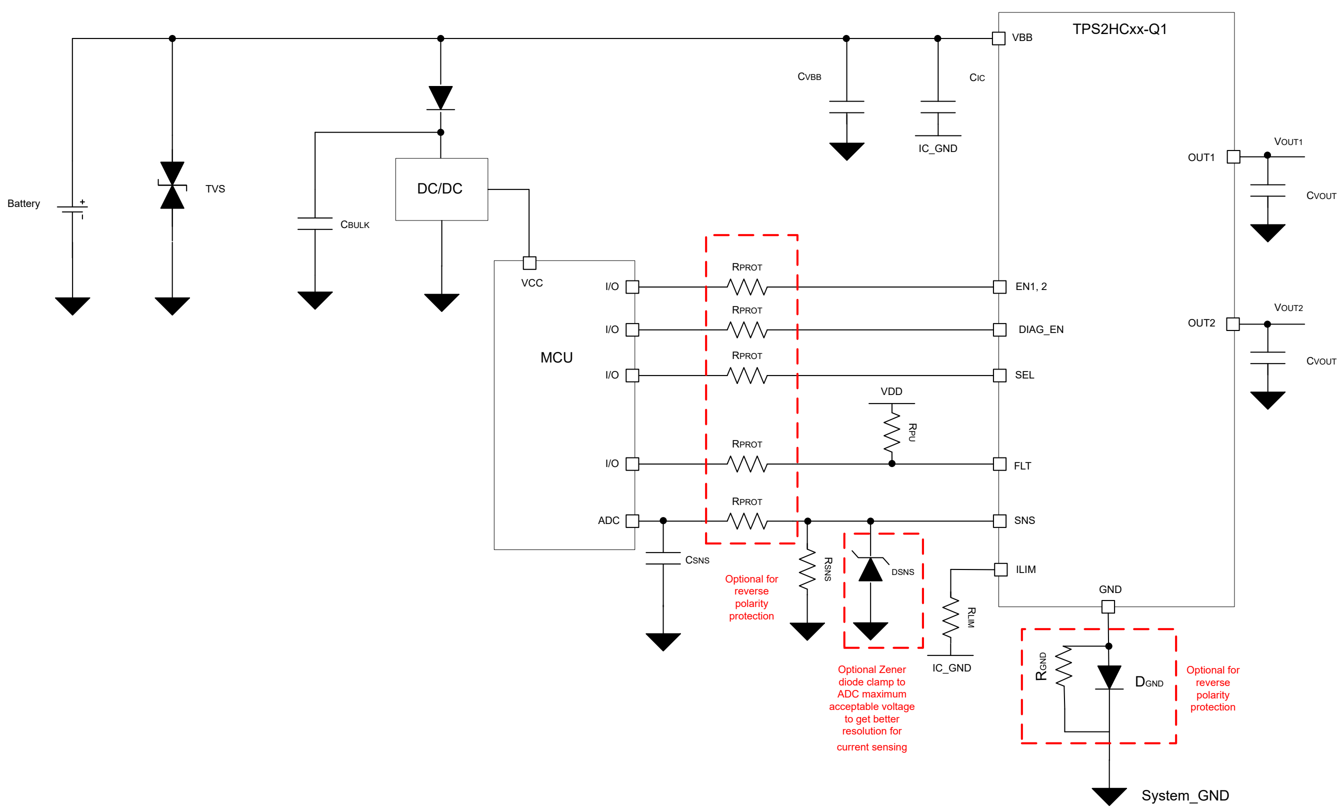


Figure 9-1. Typical Application Diagram

9.2.1 Design Requirements

Table 9-1. Recommended Component Values

COMPONENT	DESCRIPTION	PURPOSE
TVS	SMBJ39CA	Filter voltage transients coming from battery (ISO7637-2)
C_{VBB}	220nF	Better EMI performance
C_{IC}	100nF	Minimal amount of capacitance on input for EMI mitigation
C_{BULK}	10μF	Help filter voltage transients on the supply rail
R_{PROT}	10kΩ	Protection resistor for microcontroller and device I/O pins

Table 9-1. Recommended Component Values (continued)

COMPONENT	DESCRIPTION	PURPOSE
R_{LIM}	Values listed in Electrical Characteristics	Set current limit threshold
R_{SNS}	1kΩ	Translate the sense current into sense voltage
D_{SNS}	SMBJ50A	Clamp SNS pin voltage to ADC maximum acceptable voltage to have improved current sense resolution.
C_{FILTER}	100nF	Coupled with RPROT on the SNS line creates a low pass filter to filter out noise going into the ADC of the MCU
C_{VOUT}	22nF	Improves EMI performance, filtering of voltage transients
R_{PULLUP}	4.7kΩ	Pull up resistor for open-drain pins ($\overline{FLT}$ and LPM)
R_{GND}	4.7kΩ	Stabilize GND potential during turn-off of inductive load
D_{GND}	BAS21 Diode	Keeps GND close to system ground during normal operation

9.2.2 Detailed Design Procedure

The R_{SNS} resistor value can be calculated using Equation 1 in case of no external component connected on SNS pin and Equation 2 when an external zener diode or resistor divider is connected on SNS pin to clamp SNS pin voltage to ADC maximum acceptable voltage, $V_{ADC,max}$ for better current sense resolution. To achieve better current-sense accuracy, a 1% tolerance or better resistor is preferred.

Table 9-2. Typical Application

PARAMETER	VALUE (no external component connected on SNS pin)	VALUE (external zener diode or resistor divider is connected on SNS)
$I_{LOAD,max}$	7.5A	7.5A
$I_{LOAD,min}$	100mA	100mA
$V_{ADC,max}$	5V	5V
$V_{ADC,min}$	5mV	5mV
V_{HR} (needed)	1V	1V
K_{SNS}	3000	3000
K_{CL}	500	500
I_{SNSFH}	7.5mA	7.5mA
V_{HR} (calculated with maximum R_{SNS})	3.33V	-
R_{SNS} (minimum)	150Ω	150Ω
R_{SNS} (maximum)	667Ω	1600Ω

For this application with a zener diode (D_{SNS}) connected on SNS pin, a R_{SNS} value of 1000Ω can be chosen to satisfy the Equation 2 requirements.

In other applications with a higher dynamic current range, either more emphasis can be put on the lower end measurable values which increases R_{SNS}. Likewise, if the higher currents are of more interest the R_{SNS} can be decreased.

To set the adjustable current limit value I_{CL}, use Equation 9 to select the R_{LIM} value.

$$R_{LIM} = K_{CL} / I_{CL} \quad (9)$$

TI recommends R_{PROT} = 10kΩ for 5V MCU IO connections.

9.2.2.1 EMC Transient Disturbances Test

Due to the severe electrical conditions in the automotive environment, immunity capacity against electrical transient disturbances is required, especially for a high side power switch, which is connected directly to the battery. Detailed test requirements are in accordance with the ISO 7637-2:2011 and ISO 16750-2:2010 standards.

Table 9-3. ISO 7637-2:2011(E) in 12V System

TEST ITEM	TEST PULSE SEVERITY LEVEL AND Vs ACCORDINGLY(1) (2)		PULSE DURATION (t_d)	MINIMUM NUMBER OF PULSES OR TEST TIME	BURST-CYCLE PULSE-REPETITION TIME		INPUT RESISTANCE (Ω)(3)	FUNCTION PERFORMANCE STATUS CLASSIFICATION (4)
	LEVEL	Vs/V			MIN	MAX		
1	III	–112	2ms	500 pulses	0.5s	—	10	Status II
2a	III	55	50µs	500 pulses	0.2s	5s	2	Status II
2b	IV	10	0.2s to 2s	10 pulses	0.5s	5s	0 to 0.05	Status II
3a	IV	–220	0.1µs	1h	90ms	100ms	50	Status II
3b	IV	150	0.1µs	1h	90ms	100ms	50	Status II

(1) Tested both under input low condition and high condition.
(2) The pulse 2A voltage is 54V maximum from VBB with respect to ground. A voltage suppressing mechanism must be used to pass Level III. This test was run with an 1µF capacitor from VBB to system ground.
(3) GND pin network is a 4.7kΩ resistor in parallel with a diode BAS21-7-F.
(4) Status II: The function does not perform as designed during the test, but returns automatically to normal operation after the test.

Table 9-4. ISO 16750-2:2010(E) Load Dump Test B in 12V System

TEST ITEM	TEST PULSE SEVERITY LEVEL AND Vs ACCORDINGLY(1) (2)		PULSE DURATION (t_d)	MINIMUM NUMBER OF PULSES OR TEST TIME	BURST-CYCLE PULSE-REPETITION TIME	INPUT RESISTANCE (Ω)(3)	FUNCTION PERFORMANCE STATUS CLASSIFICATION(4) (5)
	LEVEL	Vs/V					
Test B		35	40ms to 400ms	5 pulses	60s	0.5 to 4	Status II

(1) Tested both under input low condition and high condition (DIAG_EN, EN, and VBB are all classified as inputs).
(2) Considering the worst test condition, the device is tested without any filter capacitors on VBB and VOUT.
(3) The GND pin network is a 4.7kΩ resistor in parallel with a diode BAS21-7-F.
(4) Status II: The function does not perform as designed during the test, but returns automatically to normal operation after the test.
(5) Select a 36V external suppressor.

9.2.3 Transient Thermal Performance

The TPS2HC08-Q1 device can experience different transient conditions that cause large currents to flow for a short duration of time. These may include:

- Inrush current during high capacitive or bulb load charging.
- Fault conditions such as output shorted to ground, triggering overcurrent protection.
- Briefly energizing a inductive load such as motor or solenoid for a limited time, then de-energizing.

In these transient cases, the thermal impedance parameter $Z_{\Theta JA}$ denotes the junction-to-ambient thermal performance. Figure 9-2 shows the simulated thermal impedance for according to JEDEC JESD51-2,-5,-7 standards under natural convection conditions using an FR4 2s2p board. The device (chip + package) was modeled on a 76.2 × 114.3 × 1.5mm board featuring two inner copper layers (two at 70µm Cu thickness and two at 35µm Cu thickness). Five thermal vias positioned beneath the VBB pad established contact with the first inner copper layer (12mm x 12mm). All simulations were performed at an ambient temperature of 25°C.

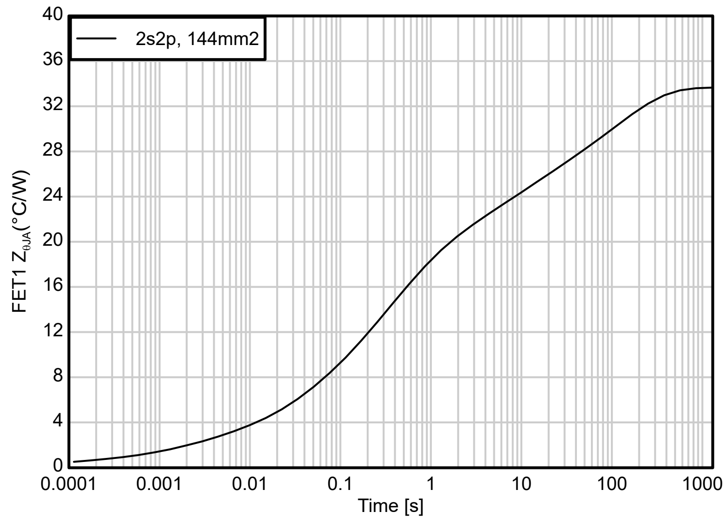
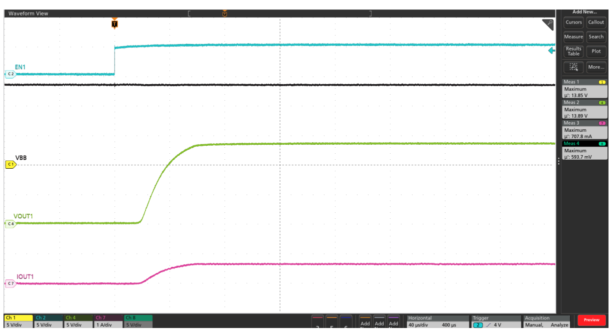


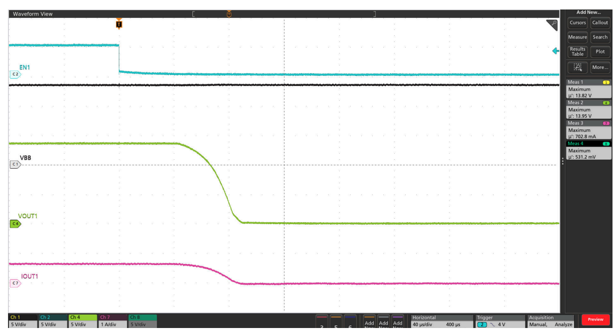
Figure 9-2. $Z_{\Theta JA}$ (transient thermal impedance) with JEDEC Standard 2s2p PCB Layout, 5 Thermal Vias Below VBB Pad

9.2.4 Application Curves



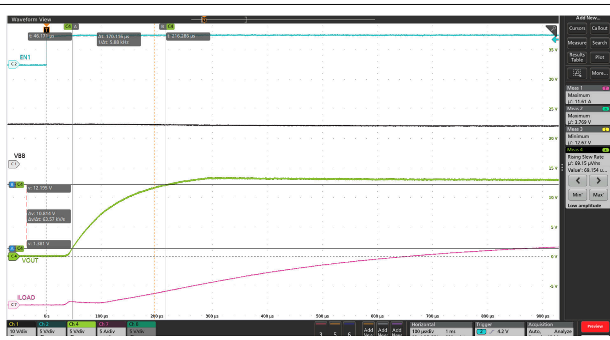
VBB = 13.5V Z_{OUT1} = 19Ω T_A = 25°C

Figure 9-3. Turn-on with Resistive Load



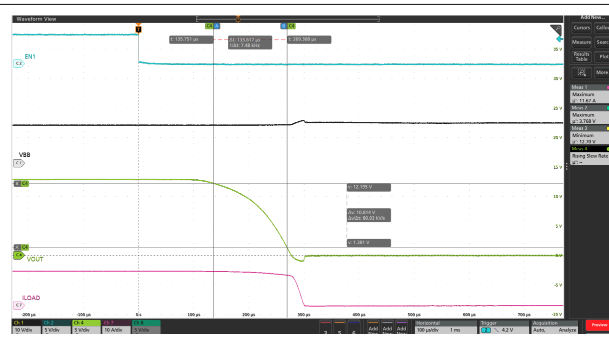
VBB = 13.5V Z_{OUT1} = 19Ω T_A = 25°C

Figure 9-4. Turn-off with Resistive Load



VBB = 13.5V I_{OUT1} = 11A T_A = 25°C
V_{EN} = 0V to 5V

Figure 9-5. Rising Slew Rate (P version)



VBB = 13.5V I_{OUT1} = 11A T_A = 25°C
V_{EN} = 5V to 0V

Figure 9-6. Falling Slew Rate (P version)

VBB = 13.5V | V_{OUT1} = Shorted-to-GND | T_A = 25°C
I_{LIM} = GND | V_{EN} = 5V

Figure 9-7. Device Turn-on Behavior with Channel 1 Output Shorted to GND

VBB = 13.5V | V_{OUT1} = Shorted-to-GND | T_A = 25°C
I_{LIM} = GND | V_{EN} = 5V

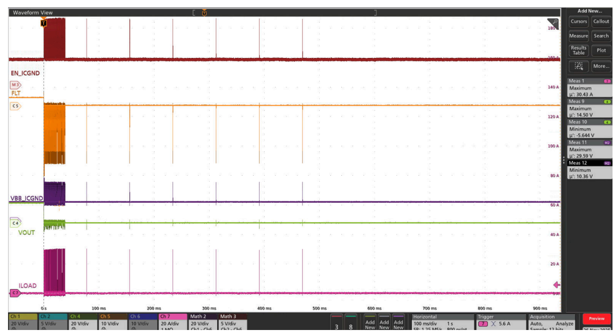
Figure 9-8. Device Turn-on Behavior with Channel 2 Output Shorted to GND

VBB = 13.5V | V_{OUT1} = open load | T_A = 25°C
DIAG_EN = PWM (200Hz) | V_{EN1} = 0V | SEL = 0

SNS outputs I_{SNSFH} current when DIAG_EN is high and is floating when DIAG_EN is low

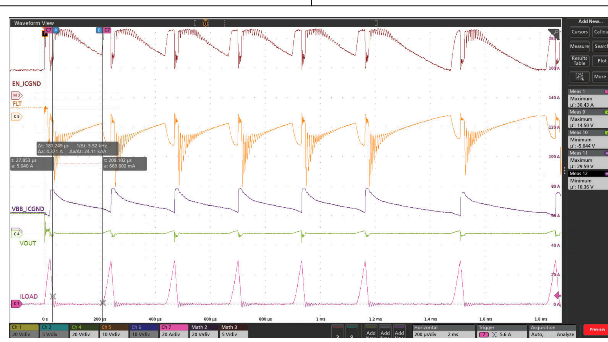
FLT = get asserts when DIAG_EN is high

Figure 9-9. Open Load Detection Delay with Open Load Fault on Channel 1



VBB = 13.5V | Z_{OUT1} = 1uH + 100mΩ | T_A = 25°C
V_{EN1} = 5V

Figure 9-10. Hot Short (Retry behavior)



VBB = 13.5V | Z_{OUT1} = 1uH + 100mΩ | T_A = 25°C
V_{EN1} = 5V

Figure 9-11. Hot Short (Retry behavior) Zoomed to Initial Retry Window

9.3 Power Supply Recommendations

The device is qualified for both automotive and industrial applications. The normal power supply connection is a 12V automotive system. The supply voltage must be within the range specified in the *Recommended Operating Conditions*.

Table 9-5. Voltage Operating Ranges

VBB VOLTAGE RANGE	NOTE
3V to 6V	Extended lower 12V automotive battery operation such as cold crank and start-stop. The device is fully functional and protected but some parametrics such as R_{ON}, current sense accuracy, current limit accuracy and timing parameters can deviate from specifications. Check the individual specifications in the *Electrical Characteristics* to confirm the voltage range.
6V to 18V	Nominal 12V automotive battery voltage range. All parametric specifications apply and the device is fully functional and protected.
18V to 28V	Extended upper 12V automotive battery operation such as double battery. The device is fully functional and protected (short-circuit protection up to 24V) but some parametrics such as R_{ON}, current sense accuracy, current limit accuracy, and timing parameters can deviate from specifications. Check the individual specifications in the *Electrical Characteristics* to confirm the voltage range.
35V	Load dump voltage. Device is operational and lets the pulse pass through without being damaged but does not protect against short circuits.

9.4 Layout

9.4.1 Layout Guidelines

To achieve good thermal performance, connect the VBB pad to a large copper pour. On the top PCB layer, the pour can extend beyond the package dimensions as shown in the layout examples below. In addition to this, having a VBB plane on one or more internal PCB layers and/or on the bottom layer is recommended. Vias must connect these planes to the top VBB pour. Connecting the VOUT1 and VOUT2 pads to large copper pours on the board can also help to achieve better thermal performance as the heat can transfer through the internal copper pillars to the large copper pours on the board.

TI recommends that the IO signals that connect to the microcontroller be routed to a via and then through an internal PCB layer.

If used in the design, the C_{IC} capacitor, must be placed as close as possible to the VBB and GND pin of the device. If a ground network is used for reverse battery protection, the C_{IC} capacitor must be connected from the VBB net to the IC_GND net. The C_{VBB} capacitor must be placed close to the VBB pin and connected to system ground to allow for best performance.

The R_{LIM} component must be placed close to the ILIM and GND pin of the device. If a ground network is used for reverse battery protection, the R_{LIM} must be connected from the ILIM pin to the IC_GND net for expected current limit performance.

The FLT and SNS pin traces must be routed far apart (orthogonal or in different layers) to avoid any coupling between the two signals.

The TPS1HC03-Q1 device footprint is compatible with all other devices in the family and can be used for common board design.

9.4.2 Layout Examples

9.4.2.1 Without a GND Network

Figure 9-12 below shows an example PCB layout without a GND network. TI recommends that the IO signals that connect to the microcontroller be routed to a via and then through an internal PCB layer.

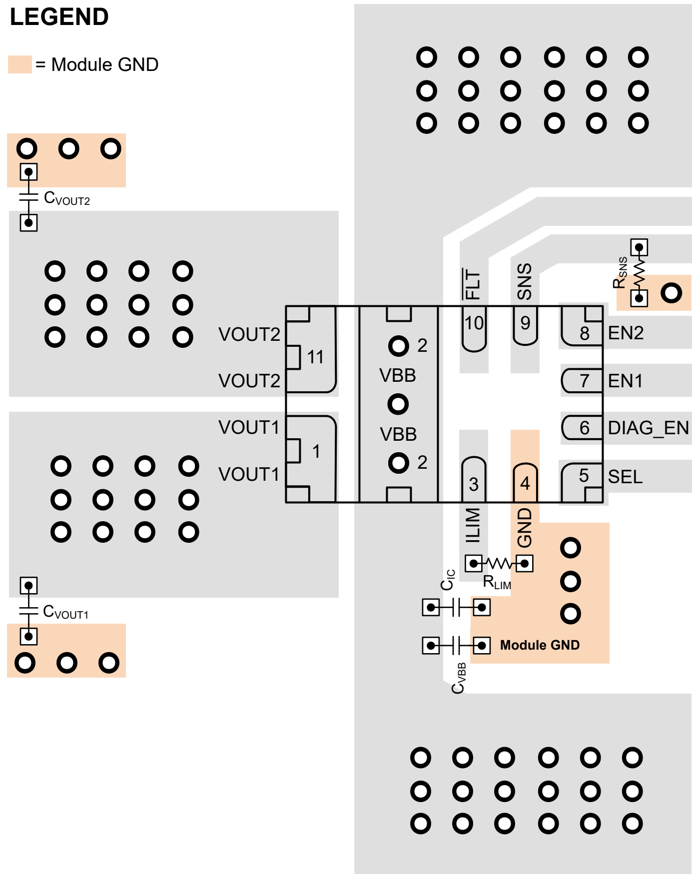


Figure 9-12. Layout Example without a GND Network

9.4.2.2 With a GND Network

Figure 9-13 below shows an example PCB layout with a GND network. TI recommends that the IO signals that connect to the microcontroller be routed to a via and then through an internal PCB layer.

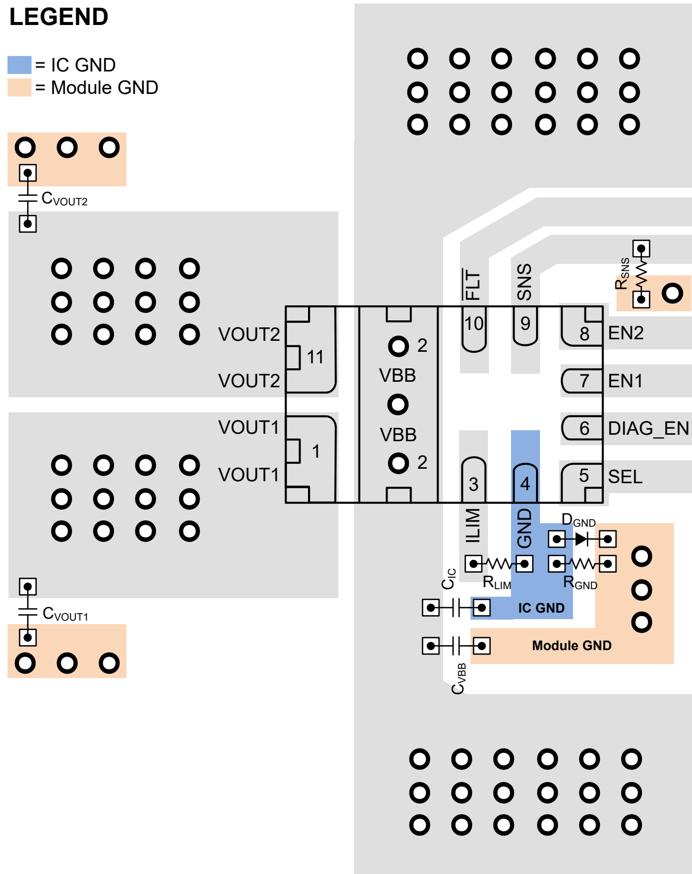


Figure 9-13. Layout Example with a GND Network

9.4.3 Wettable Flank Package

In traditional QFN packages, confirming proper solder connections to PCBs via Automatic Optical Inspection (AOI) is challenging. Exposed copper edges after package sawing are prone to oxidation, making reliable solder wetting difficult. Without a consistent solder fillet, proper solder connections cannot be visually confirmed during inspection.

To mitigate above challenge, wettable flank process employs mechanical and metallurgy-based techniques that enable the sidewall of QFN packages to be wettable to a specified height. This creates an inspectable solder fillet, providing visual confirmation of proper connection and meeting inspection requirements.

Wettable flank can be of three types – Dimple cut, Step cut and Immersion Tin. Dimple cut or step cut options feature visible grooves on package sidewalls, whereas the Immersion Sn approach uses tin plating on the sidewall without requiring physical grooves.

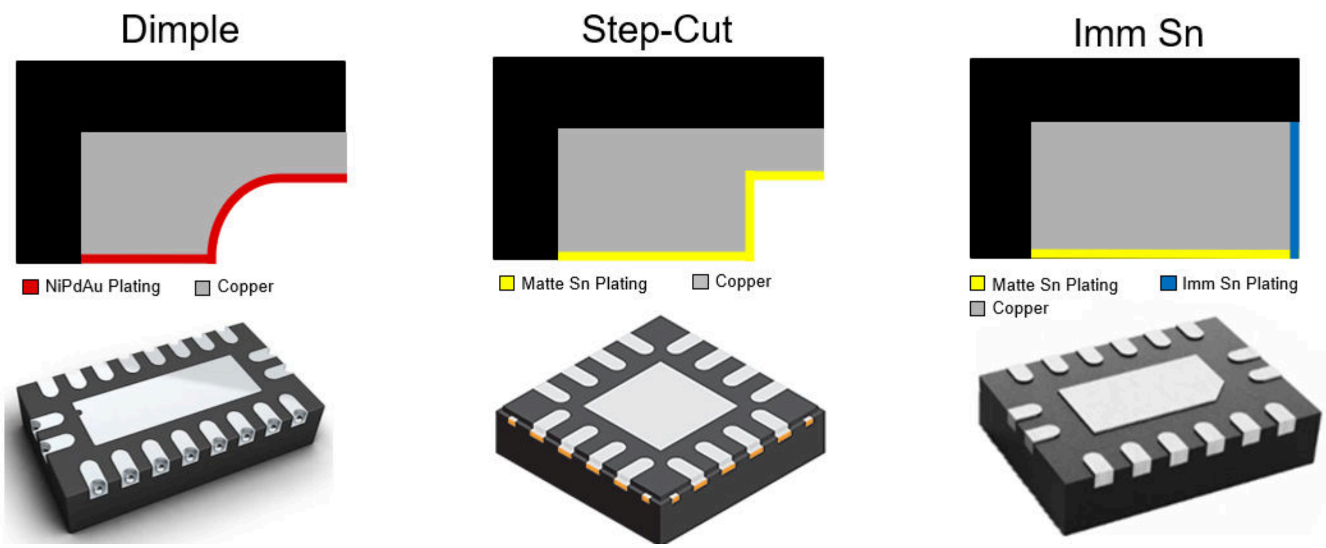


Figure 9-14. Types of Wettable Flank Packages

The VAH package of the TPS2HC08-Q1 uses the Immersion Sn plating option. This implementation meets industry requirements for minimum 100µm side-wetting of solder material, making sure reliable connections while allowing for automated optical inspection.

10 Device and Documentation Support

10.1 Third-Party Products Disclaimer

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ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

10.6 Glossary

TI Glossary This glossary lists and explains terms, acronyms, and definitions.

11 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision * (May 2025) to Revision A (December 2025) **Page**

- Updated from Advance Information to Production Data.. 1

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most-current data available for the designated device. This data is subject to change without notice and without revision of this document. For browser-based versions of this data sheet, see the left-hand navigation pane.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
PTPS2HC08PQVAHRQ1	Active	Preproduction	VQFN-HR (VAH) | 11	3000 | LARGE T&R	-	Call TI	Call TI	-40 to 125	

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

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