MIDRANGE INPUT SYNCHRONOUS BUCK CONTROLLER WITH VOLTAGE FEED-FORWARD

FEATURES

- **Operation Over 4.5-V to 28-V Input Range**
- **Fixed-Frequency Voltage-Mode Controller**
- **Integrated Unity Gain Amplifier for Remote Output Sensing**
- **Predictive Gate Drive™ Generation II for Improved Efficiency**
- **<1% Internal 700-mV Reference**
- **Input Voltage Feed Forward Control**
- **Prebiased Output Compatible**
- **Internal Gate Drive Outputs for High-Side and Synchronous N-Channel MOSFETs**
- **Switching Frequency Programmable to 1 MHz**
- **20-Pin QFN Package**
- **Thermal Shutdown Protection**
- **Software Design Tool and EVM Available**

APPLICATIONS

- **Power Modules**
- **Networking/Telecom**
- **Industrial**
- **Servers**

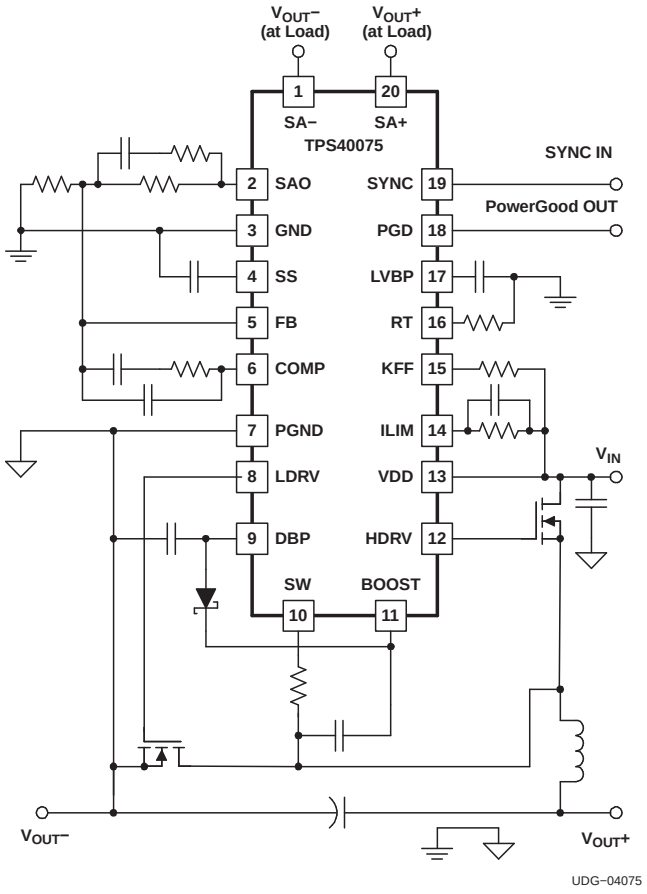
CONTENTS

DESCRIPTION

The TPS40075 is a mid voltage, wide input (4.5-V to 28-V), synchronous, step-down controller, offering design flexibility for a variety of user programmable functions, including; soft start, UVLO, operating frequency, voltage feed-forward and high-side FET sensed short circuit protection.

The TPS40075 drives external N-channel MOSFETs using second generation Predictive Gate Drive to minimize conduction in the body diode of the low side FET and maximize efficiency. Pre-biased outputs are supported by not allowing the low side FET to turn on until the voltage commanded by the closed loop soft start is greater than the pre-bias voltage. Voltage feed forward provides good response to input transients and provides a constant PWM gain over a wide input voltage operating range to ease compensation requirements. Programmable short circuit protection provides fault current limiting and hiccup recovery to minimize power dissipation with a shorted output. The 20-pin QFN package gives good thermal performance and a compact footprint.

SIMPLIFIED APPLICATION DIAGRAM



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

Predictive Gate Drive is a trademark of Texas Instruments.

ORDERING INFORMATION

T_A	PACKAGE	PART NUMBER
40°C to 85°C	Plastic QFN (RHL)	TPS40075RHLT(1)
		TPS40075RHLR(2)

(1) The TPS40075 is available taped and reeled only. Add an T suffix (i.e. TPS40075RHLT) to the orderable part number for quantities of 250 units per small reel. .
(2) Add an R suffix (i.e. TPS40075RHLR) to the orderable part number for quantities of 3,000 units per large reel.

DEVICE RATINGS

ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature range unless otherwise noted(1)

			TPS40075	UNIT
V_{DD}	Input voltage range	VDD, ILIM	30	V
		FB, KFF, PGD, SYNC	–0.3 to 6	
		SW	–0.3 to 40	
		SA+, SA-	–0.3 to 11	
		SW, transient < 50 ns	–2.5	
		SW, transient	–125	V × ns
V_{OUT}	Output voltage range	COMP, RT, SS	–0.3 to 6	V
		BOOST, HDRV	50	
		DBP, SAO, LDRV	10.5	
		LVBP	6	
I_{OUT}	Output current source	LDRV, HDRV	1.5	A
I_{OUT}	Output current sink	LDRV, HDRV	2.0	
		KFF	10	mA
I_{OUT}	Output current source	RT	1	
		LVBP	1.5	
T_J	Operating junction temperature range		–40 to 125	°C
T_{stg}	Storage temperature		–55 to 150	

(1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIIONS

		MIN	NOM	MAX	UNIT
V_{DD}	Input voltage	4.5		28	V
T_A	Operating free-air temperature	-40		85	°C

ELECTROSTATIC DISCHARGE (ESD) PROTECTION

PARAMETER	MIN	TYP	MAX	UNIT
Human body model		1500		V
CDM		1500		

PACKAGE DISSIPATION RATINGS(1)

AIRFLOW (LFM)	THERMAL IMPEDANCE JUNCTION-TO-AMBIENT (°C/W)	T_A = 25°C POWER RATING (W)	T_A = 85°C POWER RATING (W)
Natural Convection	42	2.38	0.95
200	35	2.85	1.14
400	31	3.22	1.29

(1) For more information on the RHL package and the test method, refer to TI technical brief, literature number SZZA017. The ratings in this table are for the JEDEC High-K board.

ELECTRICAL CHARACTERISTICS

T_A = –40°C to 85°C, V_{IN} = 12 V_{dc}, R_T = 90.9 kΩ, I_{KFF} = 300 µA, f_{SW} = 500 kHz, all parameters at zero power dissipation (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
INPUT SUPPLY						
V_{DD}	Input voltage range, VIN		4.5		28	V
OPERATING CURRENT						
I_{DD}	Quiescent current	Output drivers not switching		2.5	3.5	mA
LVBP						
V_{LVBP}	Output voltage	$T_A = T_J$ = 25°C	3.9	4.2	4.5	V
OSCILLATOR/RAMP GENERATOR						
f_{OSC}	Accuracy		450	500	550	kHz
V_{RT}	RT voltage		2.23	2.40	2.58	V
$t_{ON(min)}$	Minimum output pulse time(1)	C_{HDRV} = 0 nF			150	ns
V_{IH}	High-level input voltage, SYNC		2		5	V
V_{IL}	Low-level input voltage, SYNC				0.8	
I_{SYNC}	Input current, SYNC			5	10	µA
	Maximum duty cycle	V_{FB} = 0 V, 100 kHz ≤ f_{SW} ≤ 500 kHz	84%		95%	
		V_{FB} = 0 V, f_{SW} = 1 MHz	76%		93%	
V_{KFF}	Feed-forward voltage		0.35	0.40	0.45	V
I_{KFF}	Feed-forward current operating range(1)		20		1100	µA
SOFT START						
I_{SS}	Charge current		9.5	12	14.5	µA
t_{DSCH}	Discharge time	C_{SS} = 3.9 nF	25		75	µs
t_{SS}	Soft-start time	C_{SS} = 3.9 nF, V_{SS} rising from 0.7 V to 1.6 V	210	290	500	
V_{SSSD}	Shutdown threshold, V_{SS} falling		225	275	325	mV
V_{SSEN}	Enable threshold, V_{SS} rising		310		410	
$V_{SSSDHYS}$	Shutdown threshold hysteresis		35		130	
DBP						
V_{DBP}	Output voltage	V_{DD} > 10 V	7	8	9	V
		V_{VDD} = 4.5 V, I_{OUT} = 25 mA	4.0	4.3		
ERROR AMPLIFIER						
V_{FB}	Feedback regulation voltage total variation	$T_A = T_J$ = 25°C	0.698	0.700	0.704	V
		0°C ≤ $T_A = T_J$ ≤ 85°C	0.690	0.700	0.707	
		-40°C ≤ $T_A = T_J$ ≤ 85°C	0.690	0.700	0.715	
$V_{SS(offset)}$	Soft-start offset from VSS(1)	Offset from V_{SS} to error amplifier		1		
GBWP	Gain bandwidth(1)		5	10		MHz
A_{VOL}	Open loop gain		50			dB
I_{SRC}	Output source current		2.5	4.5		mA
I_{SINK}	Output sink current		2.5	6		
I_{BIAS}	Input bias current	V_{FB} = 0.7 V	–250		0	nA
SHORT CIRCUIT CURRENT PROTECTION						
I_{ILIM}	Current sink into ILIM pin		115	135	150	µA
$V_{ILIM(ofst)}$	Current limit offset voltage	V_{ILIM} = 11.5 V, (V_{SW} - V_{ILIM}) V_{VDD} = 12 V	–50	–30	–10	mV
t_{HSC}	Minimum HDRV pulse width	During short circuit		135	225	ns
	Propagation delay to output(1)			50		ns
t_{BLANK}	Blanking time(1)			50		ns

(1) Ensured by design. Not production tested.

ELECTRICAL CHARACTERISTICS (continued)

T_A = –40°C to 85°C, V_{IN} = 12 V_{dc}, R_T = 90.9 kΩ, I_{KFF} = 300 µA, f_{SW} = 500 kHz, all parameters at zero power dissipation (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{OFF}	Off time during a fault (SS cycle times)			7		cycles
V_{SW}	Switching level to end precondition(1)	(V_{VDD} - V_{SW})		2		V
t_{PC}	Precondition time (2)				100	ns
$V_{ILIM(pre)}$	Current limit precondition voltage threshold(2)			6.8		V
OUTPUT DRIVERS						
t_{HFALL}	High-side driver fall time(2)	C_{HDRV} = 2200 pF, (HDRV - SW)		36		ns
t_{HRISE}	High-side driver rise time(2)			48		
t_{HFALL}	High-side driver fall time(2)	C_{HDRV} = 2200 pF, (HDRV - SW) V_{VDD}= 4.5 V		72		ns
t_{HRISE}	High-side driver rise time(2)			96		
t_{LFALL}	Low-side driver fall time(2)	C_{LDRV} = 2200 pF		24		ns
t_{LRISE}	Low-side driver rise time(2)			48		
t_{LFALL}	Low-side driver fall time(2)	C_{LDRV} = 2200 pF, V_{DD}= 4.5 V		48		ns
t_{LRISE}	Low-side driver rise time(2)			96		
V_{OH}	High-level output voltage, HDRV	I_{HDRV}= -0.01 A, (V_{BOOST}- V_{HDRV})		0.7	1.0	V
		I_{HDRV} = -0.1 A, (V_{BOOST} - V_{HDRV})		0.95	1.35	
V_{OL}	Low-level output voltage, HDRV	(V_{HDRV} - V_{SW}), I_{HDRV} = 0.01A		0.06	0.10	V
		(V_{HDRV} - V_{SW}), I_{HDRV} = 0.1 A		0.65	1.00	
V_{OH}	High-level output voltage, LDRV	(V_{DBP} - V_{LDRV}), I_{LDRV}= -0.01A		0.65	1.00	V
		(V_{DBP} - V_{LDRV}), I_{LDRV} = -0.1 A		0.875	1.300	
V_{OL}	Low-level output voltage, LDRV	I_{LDRV} = 0.01 A		0.03	0.05	V
		I_{LDRV} = 0.1 A		0.3	0.5	
BOOST REGULATOR						
V_{BOOST}	Output voltage	V_{VDD}= 12 V	15.2	17.0		V
UVLO						
V_{UVLO}	Programmable UVLO threshold voltage	R_{KFF} = 90.9 kΩ, turn-on, V_{VDD} rising	6.2	7.2	8.2	V
	Programmable UVLO hysteresis	R_{KFF} = 90.9 kΩ	1.10	1.55	2.00	
	Fixed UVLO threshold voltage	Turn-on, V_{VDD} rising	4.15	4.30	4.45	
	Fixed UVLO hysteresis		275	365		mV
POWER GOOD						
V_{PGD}	Powergood voltage	I_{PGD} = 1 mA		370	550	mV
V_{FBH}	High-level output voltage, FB			770		
V_{FBL}	Low-level output voltage, FB			630		
SENSE AMPLIFIER						
V_{IO}	Input offset voltage	V_{SA+} = V_{SA-} = 1.25 V, Offset referenced to SA+ and SA-	-9		9	mV
A_{DIFF}	Differential gain	V_{SA+} - V_{SA-} = 4.5 V	0.995	1.000	1.005	
V_{ICM}	Input common mode range(3)		0		6	V
R_G	Internal resistance for setting gain		14	20	26	kΩ
I_{OH}	Output source current		2	10	15	mA
I_{OL}	Output sink current		15	25	35	
GBWP	Gain bandwidth(4)			2		MHz
THERMAL SHUTDOWN						

(2) Ensured by design. Not production tested.
(3) 3 V at internal amplifier terminals, 6 V at SA+ and SA- pins.
(4) Ensured by design. Not production tested.

ELECTRICAL CHARACTERISTICS (continued)

T_A = –40°C to 85°C, V_{IN} = 12 V_{dc}, R_T = 90.9 kΩ, I_{KFF} = 300 µA, f_{SW} = 500 kHz, all parameters at zero power dissipation (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Shutdown temperature threshold(4)			165		°C
Hysteresis(4)			15		

TYPICAL CHARACTERISTICS

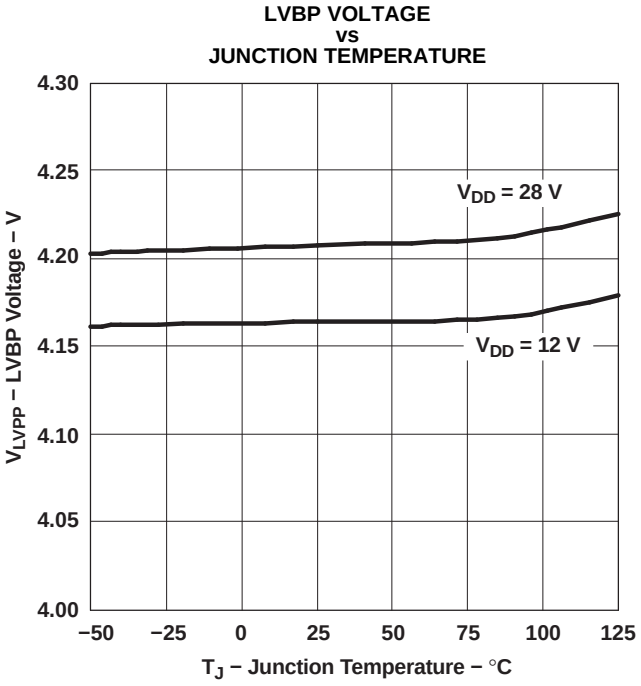


Figure 1.

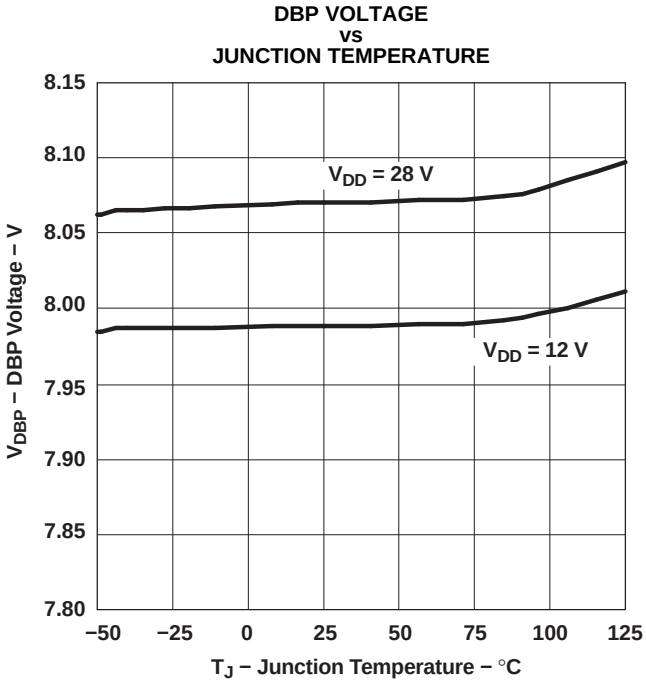


Figure 2.

TYPICAL CHARACTERISTICS (continued)

DBP VOLTAGE vs JUNCTION TEMPERATURE

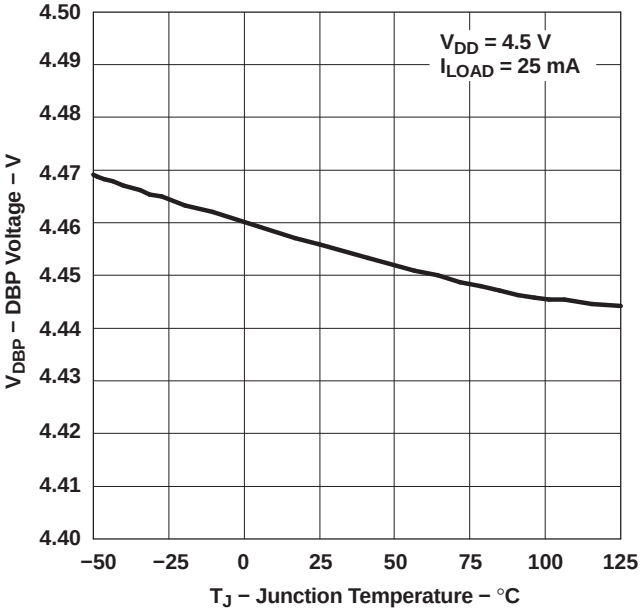


Figure 3.

BOOTSTRAP DIODE VOLTAGE vs JUNCTION TEMPERATURE

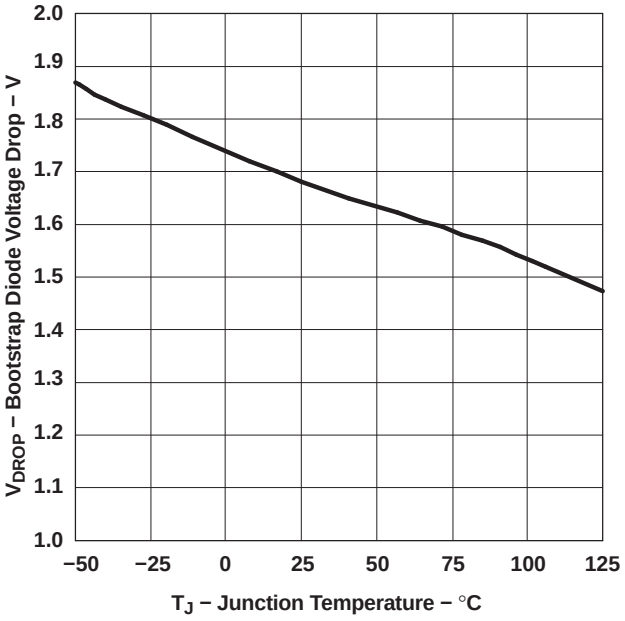


Figure 4.

CURRENT LIMIT OFFSET VOLTAGE vs JUNCTION TEMPERATURE

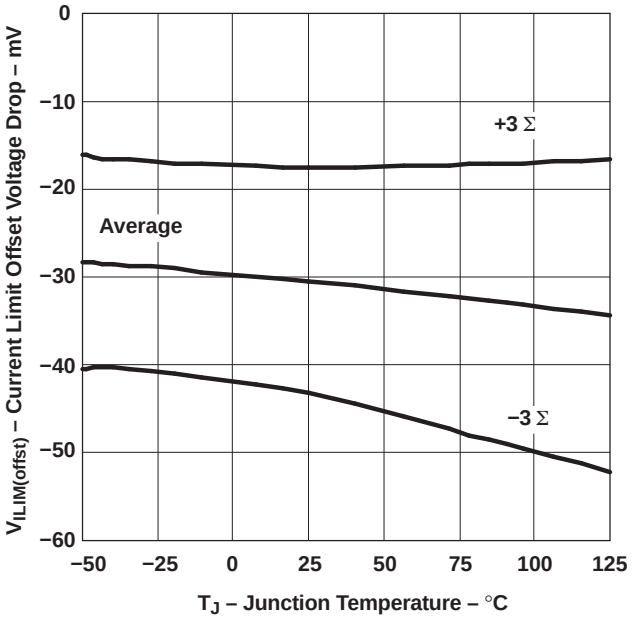


Figure 5.

CURRENT LIMIT SINK CURRENT vs JUNCTION TEMPERATURE

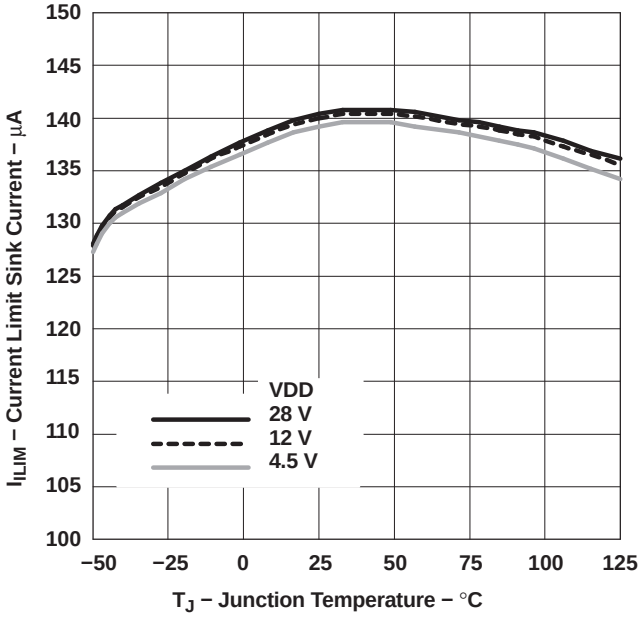


Figure 6.

TYPICAL CHARACTERISTICS (continued)

FEEDBACK REGULATION VOLTAGE
vs
JUNCTION TEMPERATURE

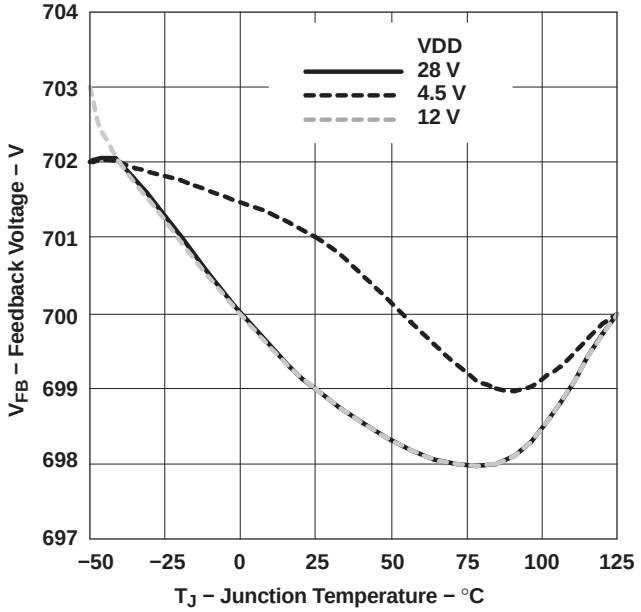


Figure 7.

SENSE AMPLIFIER OUTPUT CURRENT
vs
JUNCTION TEMPERATURE

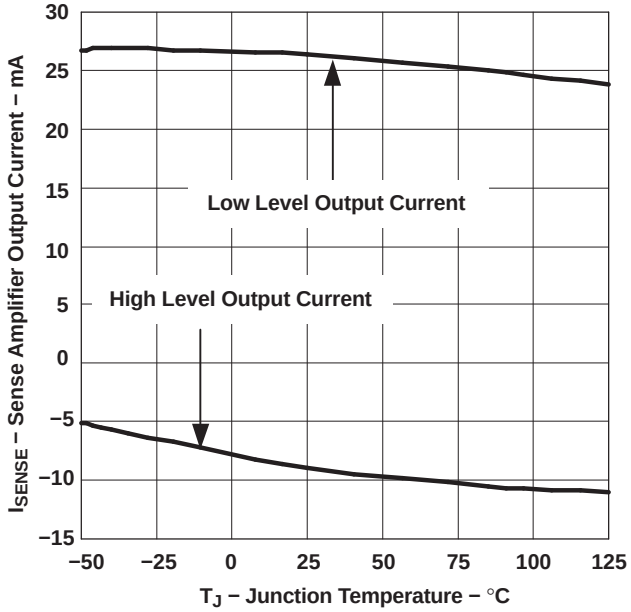


Figure 8.

CURRENT SENSE AMPLIFIER GAIN
vs
JUNCTION TEMPERATURE

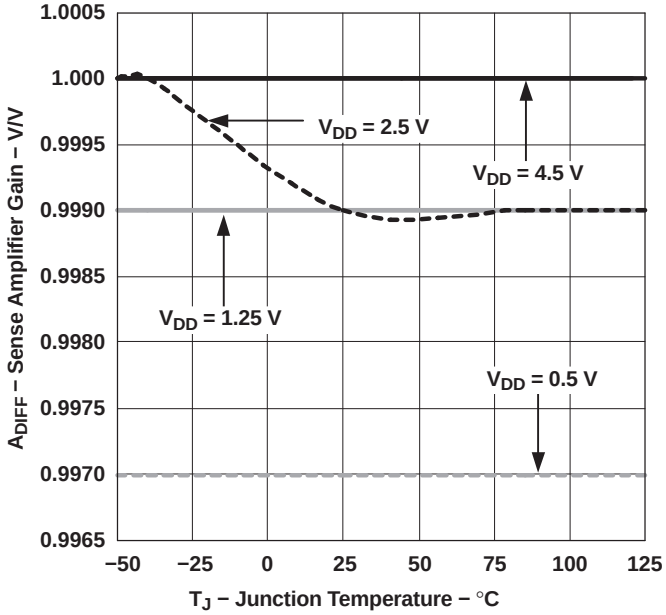


Figure 9.

SWITCHING FREQUENCY
vs
INPUT VOLTAGE

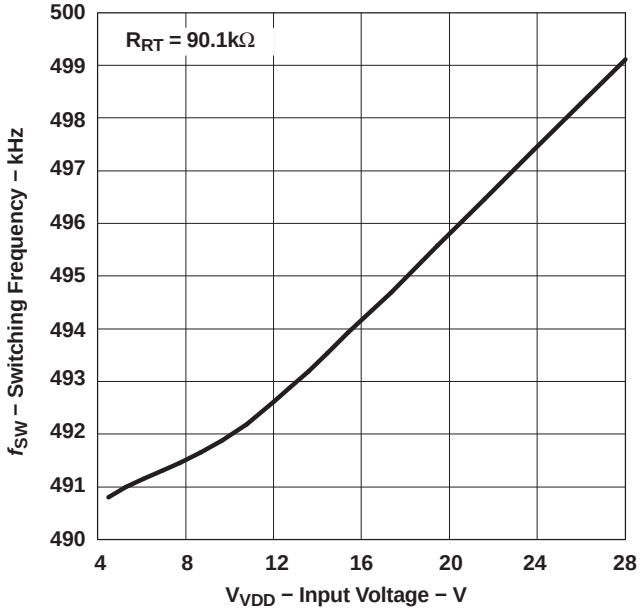


Figure 10.

TYPICAL CHARACTERISTICS (continued)

MAXIMUM DUTY CYCLE vs JUNCTION TEMPERATURE

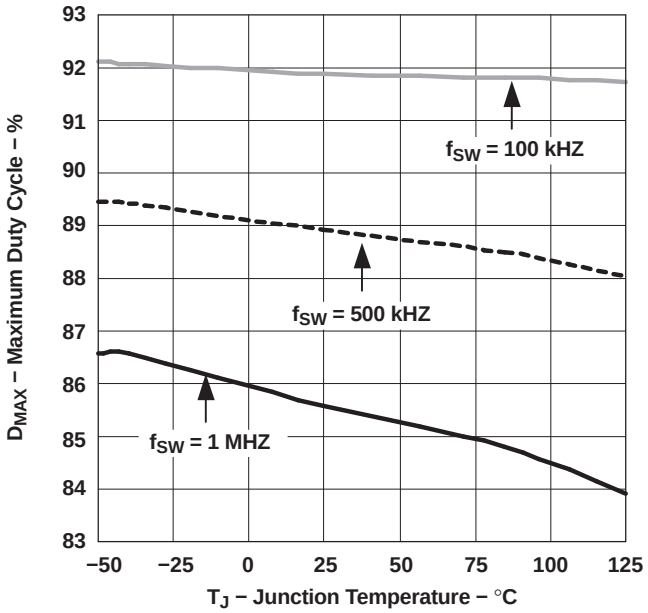


Figure 11.

UNDERVOLTAGE LOCKOUT vs JUNCTION TEMPERATURE

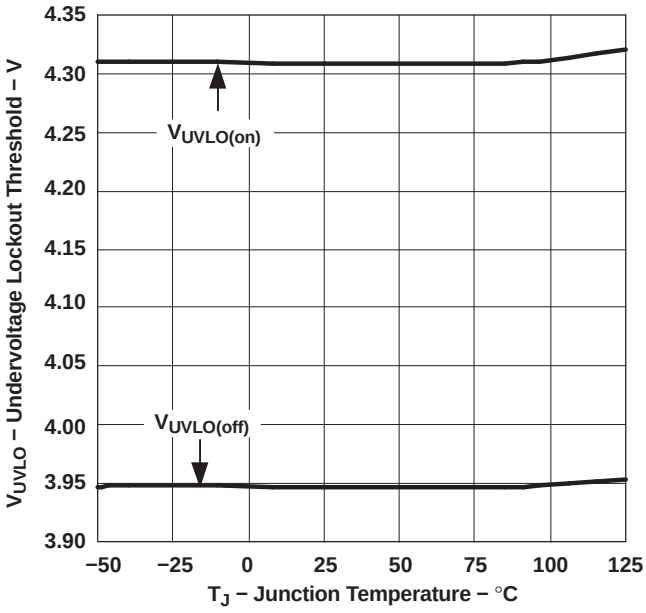


Figure 12.

PROGRAMMABLE UVLO THRESHOLD vs JUNCTION TEMPERATURE

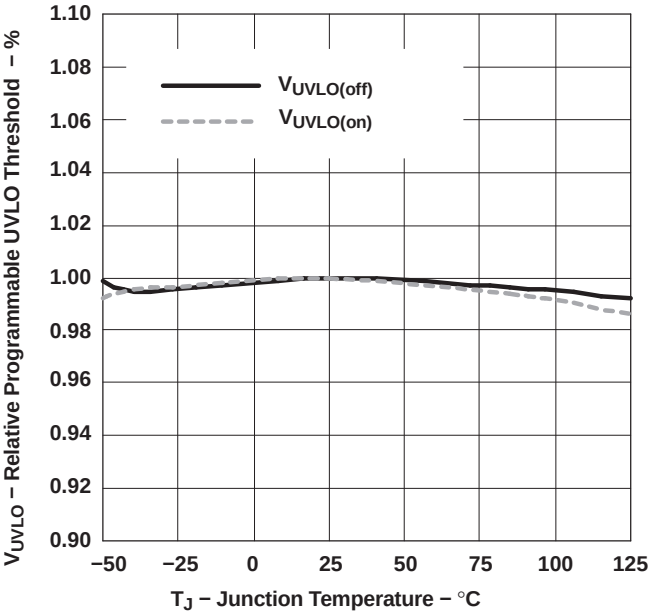


Figure 13.

SOFTSTART CHARGING CURRENT vs JUNCTION TEMPERATURE

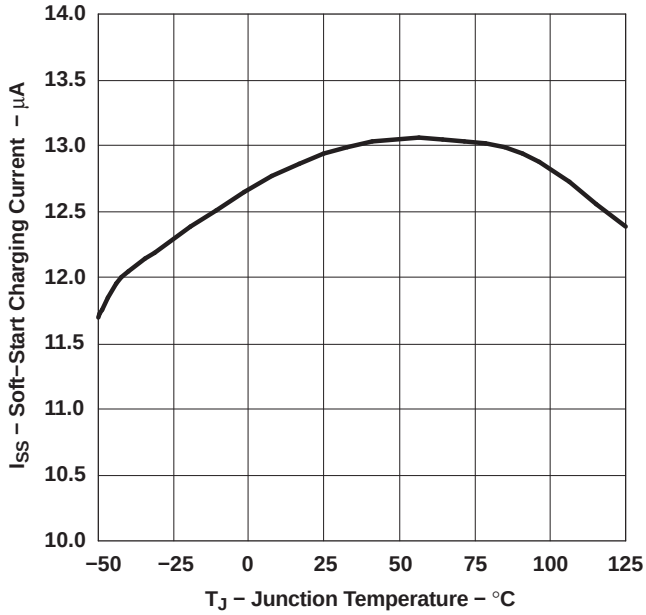


Figure 14.

TYPICAL CHARACTERISTICS (continued)

ERROR AMPLIFIER INPUT BIAS CURRENT vs JUNCTION TEMPERATURE

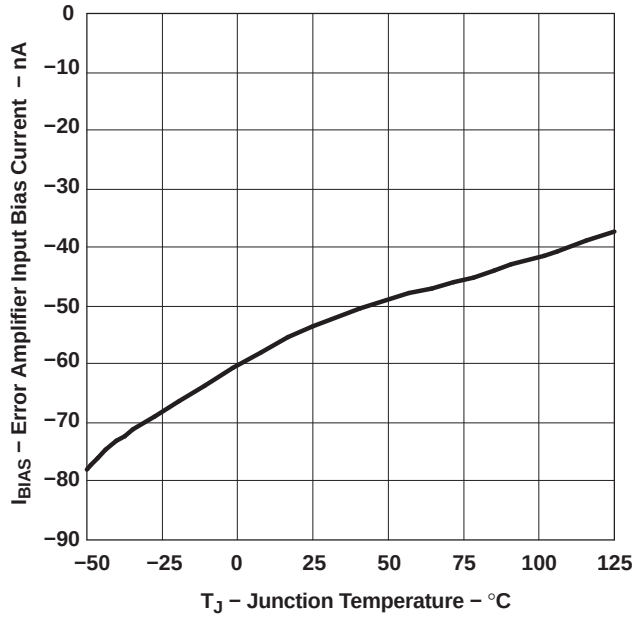


Figure 15.

MINIMUM OUTPUT VOLTAGE vs FREQUENCY

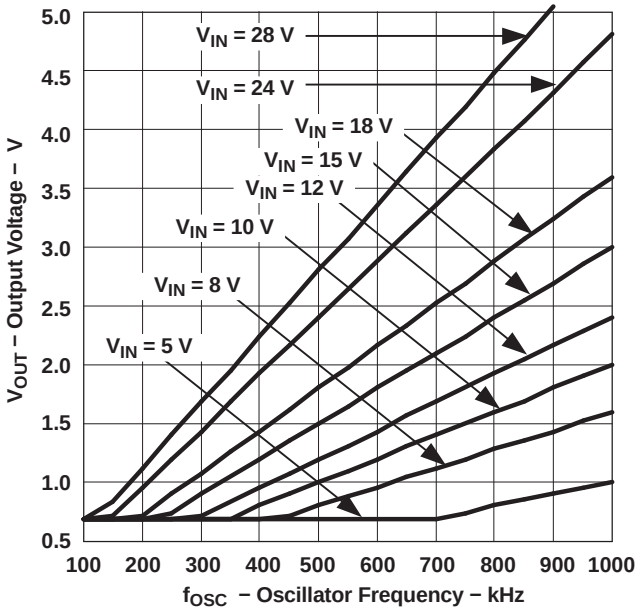


Figure 16.

SWITCHING FREQUENCY vs TIMING RESISTANCE

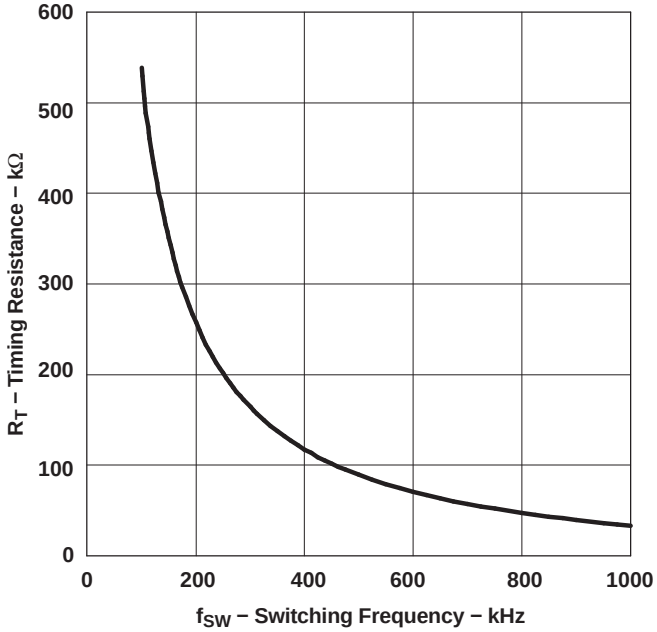


Figure 17.

TYPICAL SWITCHING FREQUENCY vs INPUT VOLTAGE

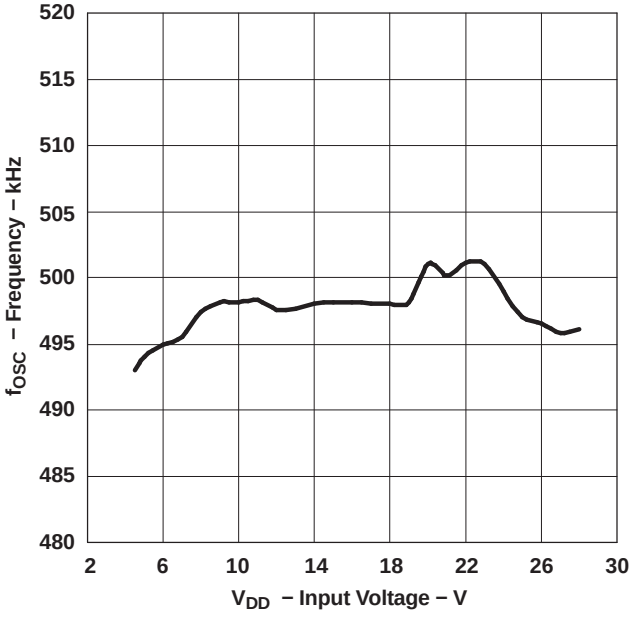


Figure 18.

TYPICAL CHARACTERISTICS (continued)

UVLO THRESHOLD VOLTAGE vs FEEDFORWARD IMPEDANCE

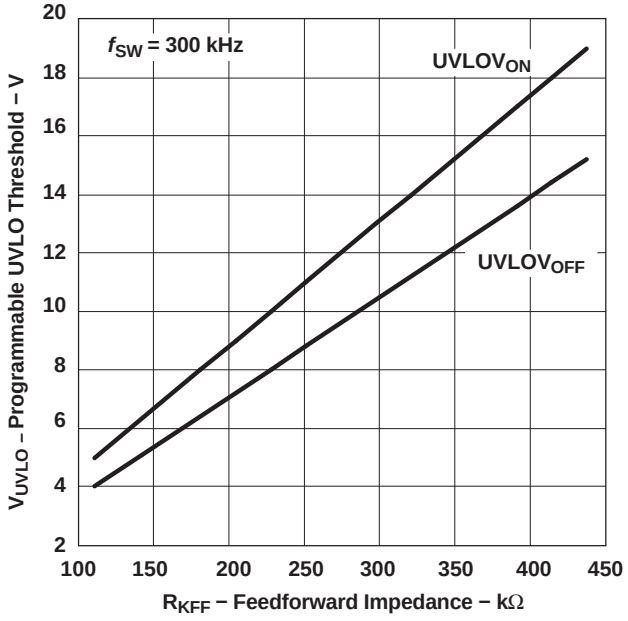


Figure 19.

UVLO THRESHOLD VOLTAGE vs FEEDFORWARD IMPEDANCE

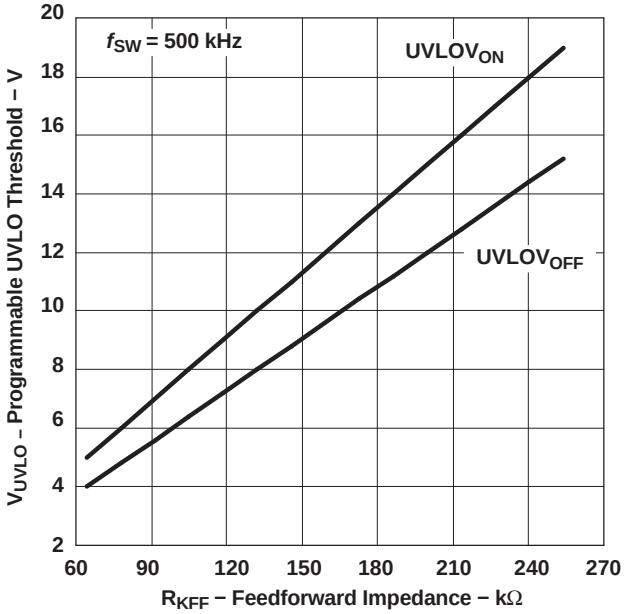


Figure 20.

UVLO THRESHOLD VOLTAGE vs FEEDFORWARD IMPEDANCE

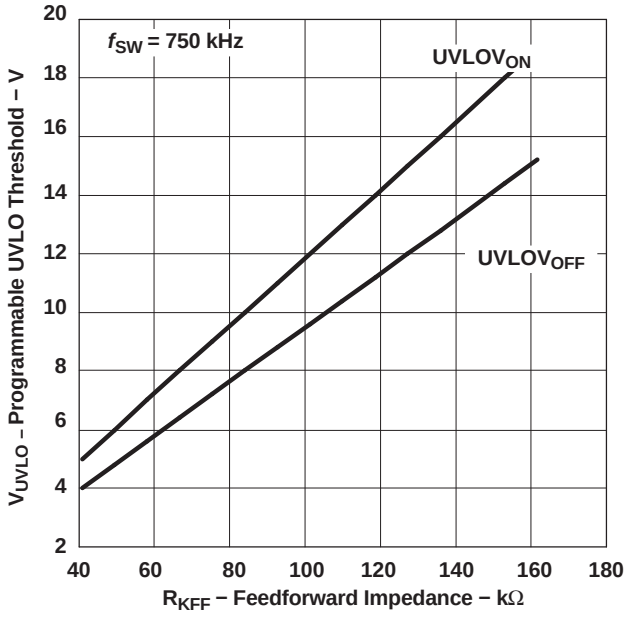


Figure 21.

TYPICAL MAXIMUM DUTY CYCLE vs INPUT VOLTAGE

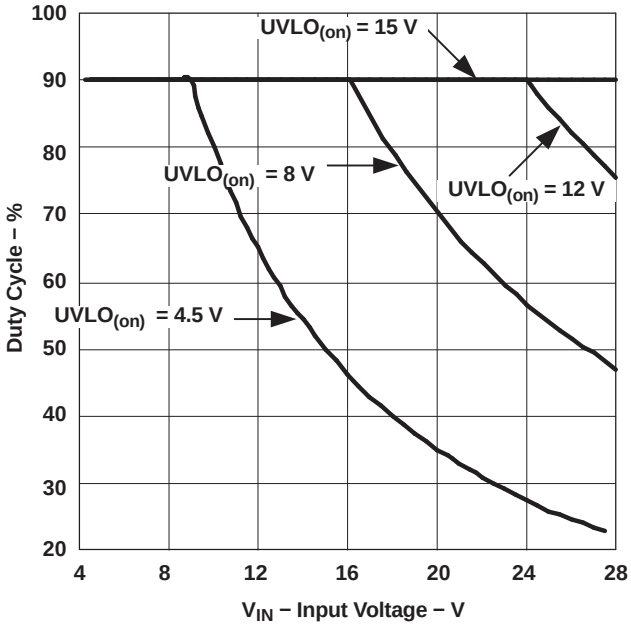


Figure 22.

TYPICAL CHARACTERISTICS (continued)

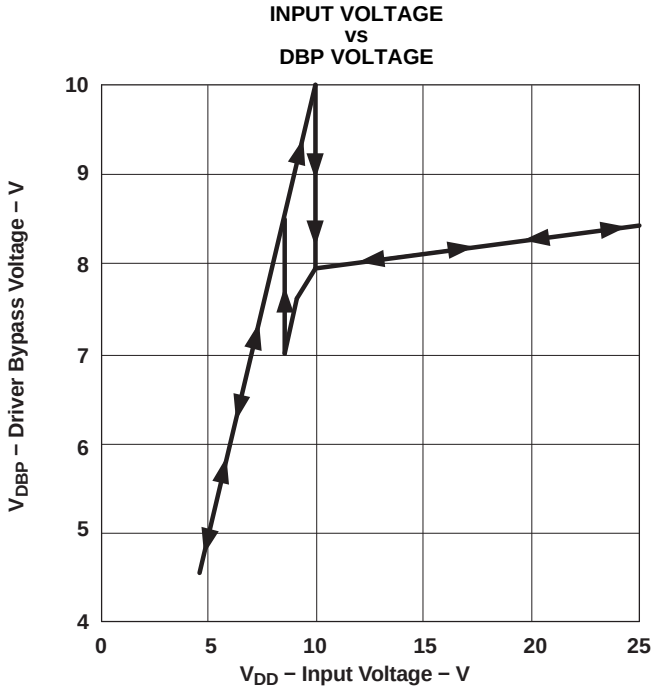


Figure 23.

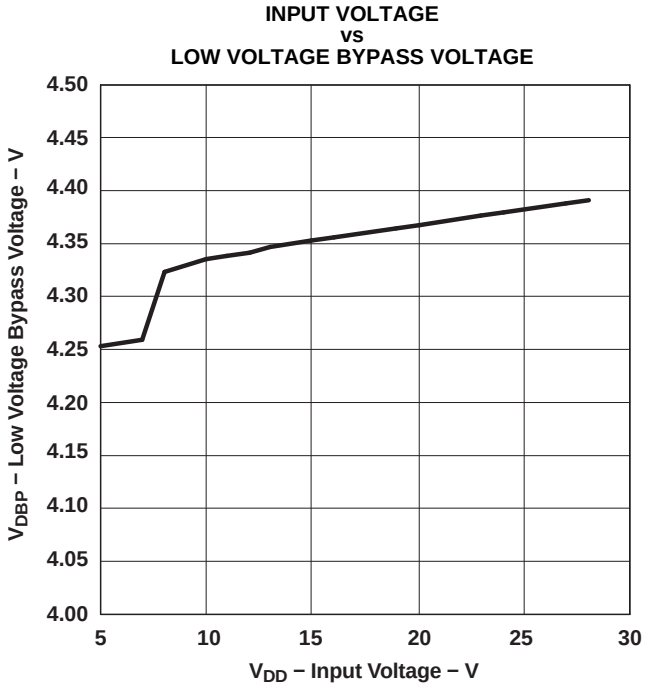


Figure 24.

TERMINAL INFORMATION

RHL PACKAGE
(BOTTOM VIEW)

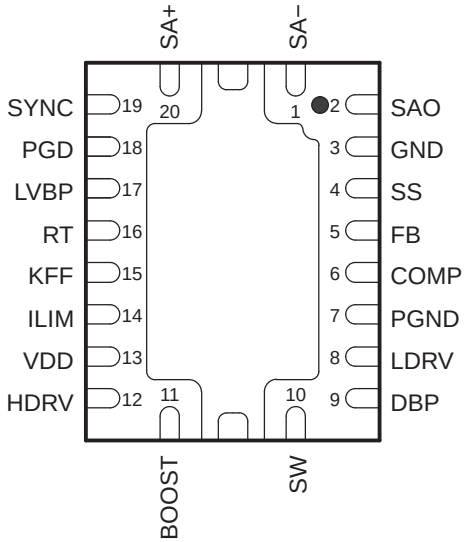
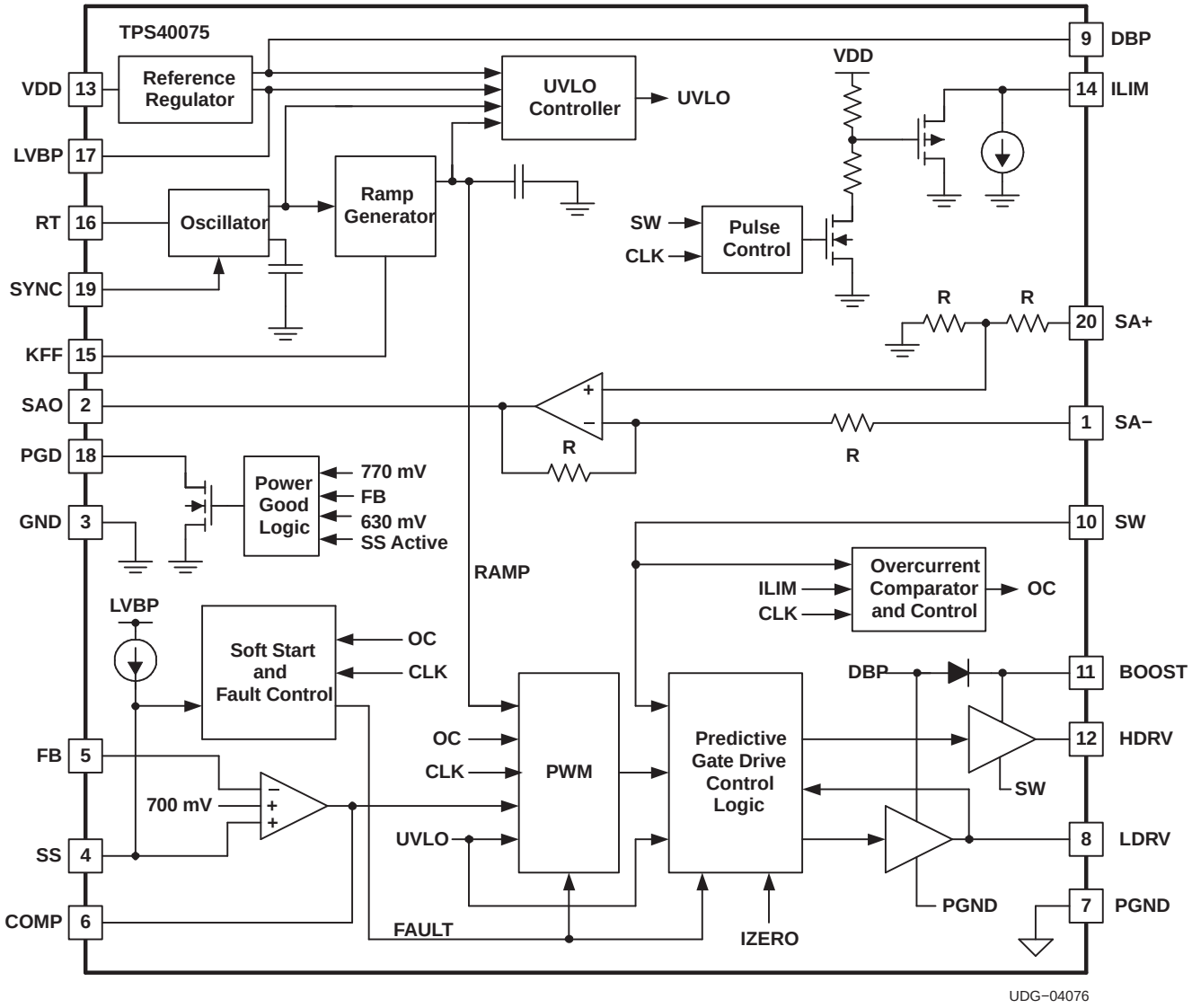


Table 1. TERMINAL FUNCTIONS

TERMINAL NAME	TERMINAL NO.	I/O	DESCRIPTION
BOOST	11	I	The BOOST voltage is 8-V greater than the input voltage. The peak voltage on BOOST is equal to the SW node voltage plus the voltage present at DBP less the bootstrap diode drop. This drop can be 1.4 V for the internal bootstrap diode or 300 mV for an external schottkey diode. The voltage differential between this pin and SW is the available drive voltage for the high-side FET.
COMP	6	O	Output of the error amplifier, input to the PWM comparator. A feedback network is connected from this pin to the FB pin to compensate the overall loop. This pin is internally clamped to a 3.4-V maximum output drive capability for quicker recovery from a saturated feedback loop situation.
DBP	9	O	8-V regulator output used for the gate drive of the N-channel synchronous rectifier and as the supply for charging the bootstrap capacitor. This pin should be bypassed to ground with a 1.0-µF ceramic capacitor.
FB	5	I	Inverting input to the error amplifier. In normal operation the voltage on this pin is equal to the internal reference voltage, 0.7 V.
GND	3	-	Ground reference for the device.
HDRV	12	O	Floating gate drive for the high-side N-channel MOSFET. This pin switches from BOOST (MOSFET on) to SW (MOSFET off).
ILIM	14	I	Short circuit protection programming pin. This pin is used to set the overcurrent threshold. An internal current sink from this pin to ground sets a voltage drop across an external resistor connected from this pin to VDD. The voltage on this pin is compared to the voltage drop (V_{VDD} -V_{SW}) across the high side N-channel MOSFET during conduction. Just prior to the beginning of a switching cycle this pin is pulled to approximately V_{VDD}/2 and released when SW is within 2 V of V_{VDD} or after a timeout (the precondition time) - whichever occurs first. Placing a capacitor across the resistor from ILIM to VDD allows the ILIM threshold to decrease during the switch on time, effectively programming the ILIM blanking time. See *Applications Information* section.
KFF	15	I	A resistor is connected from this pin to VDD programs the amount of input voltage feed-forward. The current fed into this pin is used to control the slope of the PWM ramp and program undervoltage lockout. Nominal voltage at this pin is maintained at 400 mV.
LDRV	8	O	Gate drive for the N-channel synchronous rectifier. This pin switches from DBP (MOSFET on) to PGND (MOSFET off). For proper operation, the total gate charge of the MOSFET connected to LDRV should be less than 50nC.
LVBP	17	O	4.2-V reference used for internal device logic and analog functions. This pin should be bypassed to GND with a 0.1-µF ceramic capacitor. External loads less than 1 mA and electrically quiet may be applied.
PGD	18	O	This is an open drain output that pulls to ground when soft start is active, or when the FB pin is outside a ±10% band around the 700 mV reference voltage.
PGND	7		Power ground reference for the device. There should be a low-impedance path from this pin to the source(s) of the lower MOSFET(s).
RT	16	I	A resistor is connected from this pin to GND to set the switching frequency.
SA+	20	I	Noninverting input of the remote voltage sense amplifier.
SA-	1	I	Inverting input of the remote voltage sense amplifier.
SAO	2	O	Output of the remote voltage sense amplifier.
SS	4	I	Soft-start programming pin. A capacitor connected from this pin to GND programs the soft-start time. The capacitor is charged with an internal current source of 12 µA. The resulting voltage ramp on the SS pin is used as a second non-inverting input to the error amplifier. The voltage at this error amplifier input is approximately 1 V less that that on the SS pin. Output voltage regulation is controlled by the SS voltage ramp until the voltage on the SS pin reaches the internal offset voltage of 1 V plus the internal reference voltage of 700 mV. If SS is below the internal offset voltage of 1 V (300 mV minimum ensured), the resulting output voltage is zero. Also provides timing for fault recovery attempts. Pulling this pin below 250 mV causes the controller to enter a shutdown state with HDRV and LDRV held in a low state.
SW	10	I	This pin is connected to the switched node of the converter and used for overcurrent sensing as well as gate drive timing. This pin is also the return path from the high-side FET for the floating high-side FET driver. A 1.5-Ω resistor in series with this pin is required for protection against substrate current issues.
SYNC	19	I	Logic input for pulse train to synchronize oscillator.
VDD	13	I	Supply voltage for the device.

SIMPLIFIED BLOCK DIAGRAM



APPLICATION INFORMATION

The TPS40075 allows the user to construct synchronous voltage mode buck converters with inputs ranging from 4.5 V to 28 V and outputs as low as 700 mV. Predictive gate drive circuitry optimizes switching delays for increased efficiency and improved converter output power capability. Voltage feed-forward is employed to ease loop compensation for wide input range designs and provide better line transient response.

An on-board unity gain differential amplifier is provided for remote sensing in applications that require the tightest load regulation. The TPS40075 incorporates circuitry to allow startup into a pre-existing output voltage without sinking current from the source of the pre-existing output voltage. This avoids damaging sensitive loads at startup. The controller can be synchronized to an external clock source or can free run at a user programmable frequency. An integrated power good indicator is available for logic (open drain) output of the condition of the output of the converter.

MINIMUM PULSE WIDTH

The TPS40075 has limitations on the minimum pulse width that can be used to design a converter. Reliable operation is guaranteed for nominal pulse widths of 150 ns and above. This places some restrictions on the conversion ratio that can be achieved at a given switching frequency. See Figure 16.

SLEW RATE LIMIT ON VDD

The regulator that supplies power for the drivers on the TPS40075 requires a limited rising slew rate on VDD for proper operation if the input voltage is above 10 V. If the slew rate is too great, this regulator can over shoot and damage to the part can occur. To ensure that the part operates properly, limit the slew rate to no more than 0.12 V/µs as the voltage at VDD crosses 8 V. If necessary, an R-C filter can be used on the VDD pin of the device. Connect the resistor from the VDD pin to the input supply of the converter. Connect the capacitor from the VDD pin to PGND. There should not be excessive (more than a 200-mV) voltage drop across the resistor in normal operation. This places some constraints on the R-C values that can be used. Figure 25 is a schematic fragment that shows the connection of the R-C slew rate limit circuit. Equation 1 and Equation 2 give values for R and C that limits the slew rate in the worst case condition.

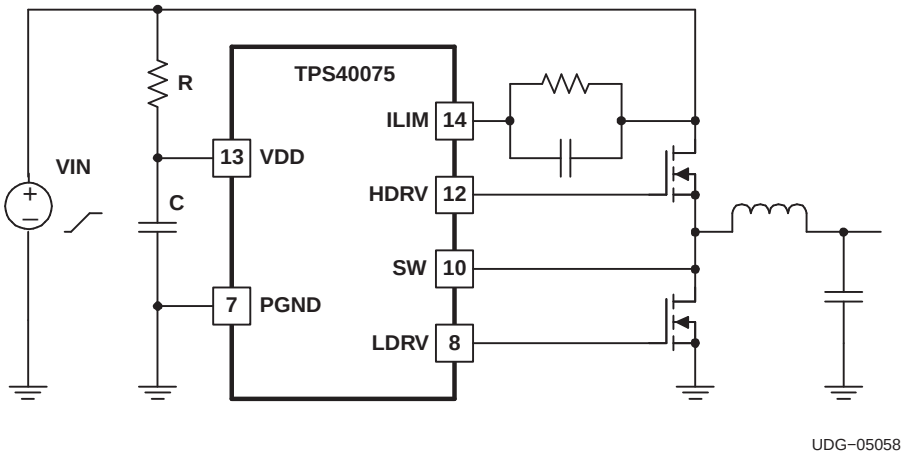


Figure 25. Limiting the Slew Rate

$$R < \frac{0.2\ V}{f_{SW} \times Q_{g(TOT)} + I_{IDD}} \quad (1)$$

$$C > \frac{V_{VIN} - 8\ V}{R \times SR} \quad (2)$$

where

- V_{VIN} is the final value of the input voltage ramp
- f_{SW} is the switching frequency
- $Q_{g(TOT)}$ is the combined total gate charge for both upper and lower MOSFETs (from MOSFET data sheet)
- I_{IDD} is the TPS40075 input current (3.5 mA maximum)
- SR is the maximum allowed slew rate [12×10^4] (V/s)

SETTING THE SWITCHING FREQUENCY (PROGRAMMING THE CLOCK OSCILLATOR)

The TPS40075 has independent clock oscillator and PWM ramp generator circuits. The clock oscillator serves as the master clock to the ramp generator circuit. Connecting a single resistor from RT to ground sets the switching frequency of the clock oscillator. The clock frequency is related to R_T by:

$$R_T = \left(\frac{1}{f_{SW}(kHz) \times 17.82 \times 10^{-6}} - 23 \right) k\Omega \quad (3)$$

PROGRAMMING THE RAMP GENERATOR CIRCUIT AND UVLO FUNCTION

The ramp generator circuit provides the actual ramp used by the PWM comparator and provides voltage feed-forward by varying the PWM ramp slope as the line voltage changes. As the input voltage to the converter increases, the slope of the PWM ramp increase by a proportionate amount. The programmable UVLO circuit works by monitoring the level reached by the PWM ramp during a clock cycle. The PWM ramp must reach approximately 1 V in amplitude during a clock cycle, or the converter is not be allowed to start. This programmable UVLO point is set via a single resistor (R_{KFF}) connected from KFF to VDD. R_{KFF} , V_{START} and R_{RT} are related by (approximately)

$$R_{KFF} = 0.131 \times R_T \times V_{UVLO(on)} - 1.61 \times 10^{-3} \times V_{UVLO(on)}^2 + 1.886 \times V_{UVLO} - 1.363 - 0.02 \times R_T - 4.87 \times 10^{-5} \times R_T^2 \quad (4)$$

where

- $V_{UVLO(on)}$ is in volts
- R_{KFF} and R_T are in kΩ

This yields typical numbers for the programmed startup voltage. The minimum and maximum values may vary up ±15% from this number. Figure 19 through Figure 21 show the typical relationship of $V_{UVLO(on)}$, $V_{UVLO(off)}$ and R_{KFF} at three common frequencies.

The programmable UVLO circuit incorporates 20% hysteresis from the start voltage to the shutdown voltage. For example, if the startup voltage is programmed to be 10 V, the controller starts when V_{DD} reaches 10 V and shuts down when V_{DD} falls below 8 V. The maximum duty cycle begins to decrease as the input voltage rises to twice the startup voltage. Below this point, the maximum duty cycle is as specified in the electrical table. Note that with this scheme, the theoretical maximum output voltage that the converter can produce is approximately two times the programmed startup voltage. For design, set the programmed startup voltage equal to or greater than the desired output voltage divided by maximum duty cycle (85% for frequencies 500 kHz and below). For example, a 5-V output converter should not have a programmed startup voltage below 5.9 V. Figure 22 shows the theoretical maximum duty cycle (typical) for various programmed startup voltages

If the programmable UVLO voltage is set below 6.5V nominal, a possibility exists that the part may enter factory test mode when powered down. This can cause an undesired output rise as power is removed from the converter. To prevent this from happening, connect a 330 kΩresistor from SS to GND. An example of this can be seen in Figure 37

Figure 26 shows the effect of changing input voltage on the duty cycle, and how that change takes place. The pulse width modulator (PWM) ramp input is generated using a current that is proportional to the current into the KFF pin. The TPS40075 holds this pin at a constant 400 mV, so connecting a resistor from KFF to the input power supply causes a current to flow into the KFF pin that is proportional to the input voltage. The slope of the ramp signal to the PWM is therefore proportional to the input voltage. This allows the duty cycle to change with variations in Vin without requiring much response from the error amplifier, resulting in very good line transient response. Another benefit is essentially constant PWM gain over the entire input voltage operating range. This makes the output control loop easier to design for a wide input range converter.

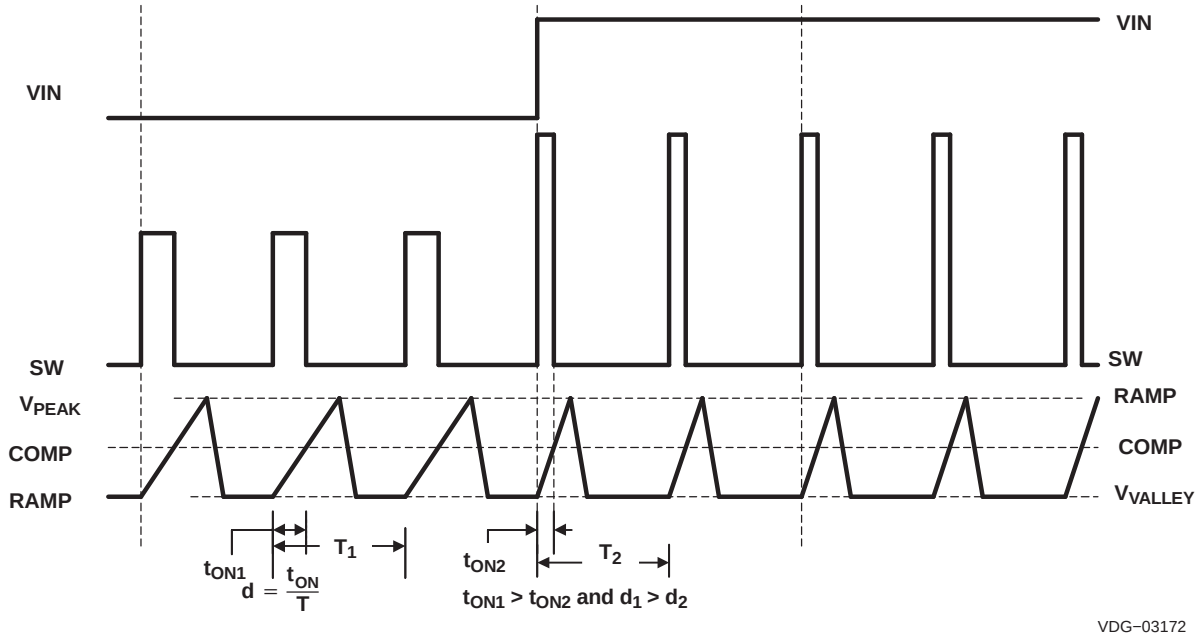


Figure 26. Voltage Feed-Forward and PWM Duty Cycle Waveforms

PROGRAMMING SOFT START

TPS40075 uses a closed-loop approach to ensure a controlled ramp on the output during start-up. Soft-start is programmed by connecting an external capacitor (C_{SS}) from the SS pin to GND. This capacitor is charged by a fixed current, generating a ramp signal. The voltage on SS is level shifted down approximately 1 V and fed into a separate non-inverting input to the error amplifier. The loop is closed on the lower of the level shifted SS voltage or the 700-mV internal reference voltage. Once the level shifted SS voltage rises above the internal reference voltage, output voltage regulation is based on the internal reference. To ensure a controlled ramp-up of the output voltage the soft-start time should be greater than the L-C_{OUT} time constant or:

$$t_{START} \geq 2\pi \times \sqrt{L \times C_{OUT}} \quad \text{(seconds)} \tag{5}$$

where

- L is the value of the filter inductor
- C_{OUT} is the value of the output capacitance
- t_{START} is the output ramp up-time

For a desired soft-start time, the soft-start capacitance, C_{SS}, can be found from:

$$C_{SS} = t_{SS} \times \frac{I_{SS}}{V_{FB}} \tag{6}$$

Please note: There is a direct correlation between t_{START} and the input current required during start-up. The lower t_{START} is, the higher the input current required during start-up since the output capacitance must be charged faster.

PROGRAMMING SHORT CIRCUIT PROTECTION

The TPS40075 uses a two-tier approach to short circuit protection. The first tier is a pulse-by-pulse protection scheme. Short circuit protection is implemented by sensing the voltage drop across the high-side MOSFET while it is turned on. The MOSFET drain to source voltage is compared to the voltage dropped across a resistor (R_{ILIM}) connected from VDD to the ILIM pin. The voltage drop across this resistor is produced by a constant current sink. If the voltage drop across the MOSFET exceeds the voltage drop across the ILIM resistor the switching pulse is immediately terminated. The MOSFET remains off until the next switching cycle is initiated.

In addition, just prior to the high-side MOSFET turning on, the ILIM pin is pulled down to approximately half of VDD. The ILIM pin is allowed to return to its nominal value after one of two events occur:

1. The SW node rises to within approximately 2 V of VDD
2. An internal timeout occurs, approximately 125-ns after ILIM is initially pulled down

If the SW node rises to within approximately 2-V of VDD, the device allows ILIM to go back to its nominal value. This is illustrated in Figure 27 A. T1 is the delay time from the internal PWM signal being asserted and the rise of SW. This includes the driver delay of 50 ns typical, and the turn on time of the high-side MOSFET. The MOSFET used should have a turn on time less than 75 ns. T2 is the reaction time of the sensing circuit that allows ILIM to start to return to its nominal value, typically 20ns.

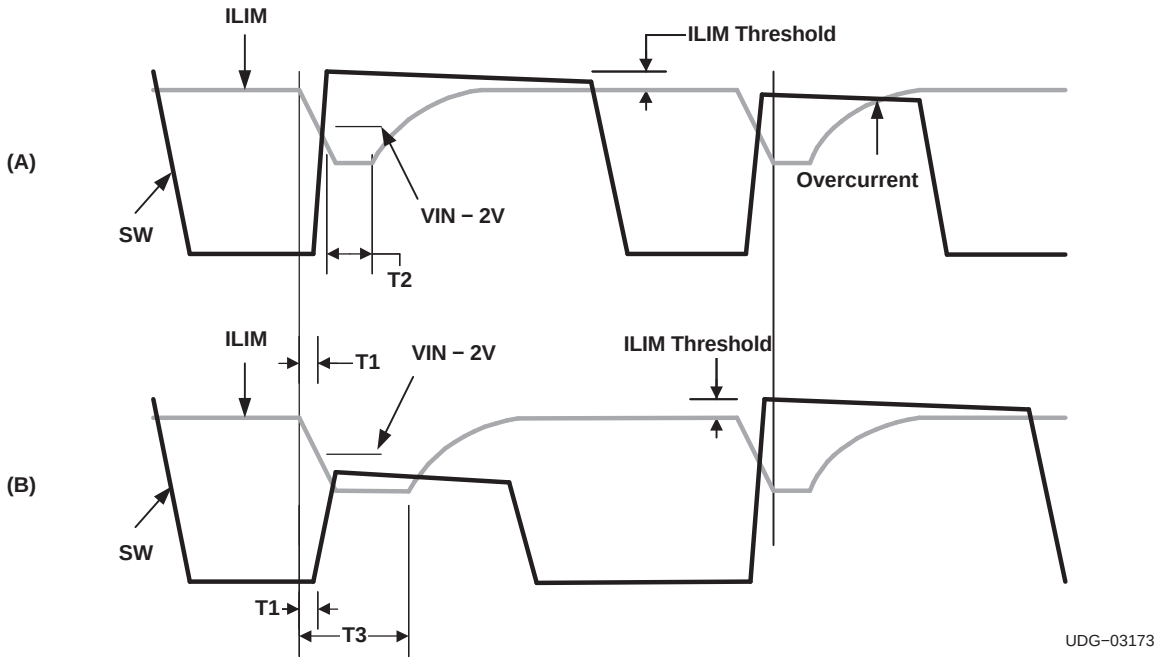


Figure 27. Switching and Current Limit Waveforms and Timing Relationship

The second event that can cause ILIM to return to its nominal value is for an internal timeout to expire. This is illustrated in Figure 27 B as T3. Here SW never rises to VDD-2, for whatever reason, and the internal timer times out. This allows the ILIM pin to start its transition back to its nominal value.

Prior to ILIM starting back to its nominal value, short circuit sensing is not enabled. In normal operation, this insures that the SW node is at a higher voltage than ILIM when short circuit sensing starts, avoiding false trips while allowing for a quicker blanking delay than would ordinarily be possible. Placing a capacitor across R_{ILIM} sets an exponential approach to the normal voltage at the ILIM pin. This exponential “decay” of the short circuit threshold can be used to compensate for ringing on the SW node after its rising edge and to help compensate for slower turn-on MOSFETs. Choosing the proper capacitance requires care. If the capacitance is too large, the voltage at ILIM does not approach the desired short circuit level quickly enough, resulting in an apparent shift in short circuit threshold as pulse width changes.

The comparator that looks at ILIM and SW to determine if a short circuit condition exists has a clamp on its SW input. This clamp makes the SW node never appear to fall more than 1.4 V (approximately, could be as much as 2 V at – 40°C) below VDD. While ILIM is more than 1.4 V below VDD short circuit sensing is effectively disabled, giving a programmable absolute blanking time. As a general rule, it is best to make the time constant of the R-C at the ILIM pin 20% or less of the nominal pulse width of the converter (See Equation 11)

The second tier protection incorporates a fault counter. The fault counter is incremented on each cycle with an overcurrent pulse and decremented on a clock cycle without an overcurrent pulse. When the counter reaches seven (7) a fault condition is declared by the controller. When this happens, the output drivers turn both MOSFETs off. Seven soft-start cycles are initiated (without activity on the HDRV and LDRV outputs) and the PWM is disabled during this period. The counter is decremented on each soft-start cycle. When the counter is decremented to zero the PWM is re-enabled and the controller attempts to restart. If the fault has been removed the output starts up normally. If the output fault is still present the counter counts seven overcurrent pulses and re-enters the second tier fault mode. Refer to Figure 28 for typical fault protection waveforms.

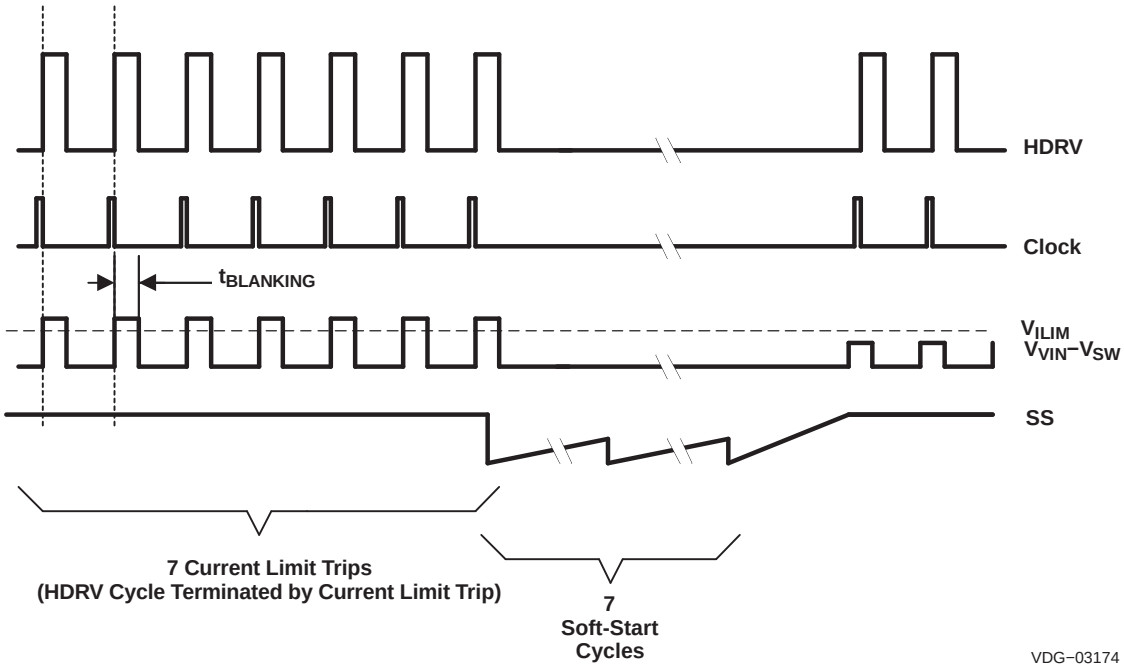


Figure 28. Typical Fault Protection Waveforms

The minimum short circuit limit threshold (I_{SCP}) depends on t_{START}, C_{OUT}, V_{OUT}, and the load current at turn-on (I_{LOAD}).

$$I_{SCP} > \frac{C_{OUT} \times V_{OUT}}{t_{START}} + I_{LOAD} \text{ (A)} \quad (7)$$

The short circuit limit programming resistor (R_{ILIM}) is calculated from:

$$R_{ILIM} = \frac{I_{SCP} \times R_{DS(onMAX)} + V_{ILIM\,(ofst)}}{I_{ILIM}} \ \Omega \quad (8)$$

where

- I_{ILIM} is the current into the ILIM pin (135 µA typical)
- $V_{ILIM(ofst)}$ is the offset voltage of the ILIM comparator (-30 mV typical)
- I_{SCP} is the short-circuit protection current
- $R_{DS(on)MAX}$ is the drain-to-source resistance of the high-side MOSFET

To find the range of the short circuit threshold values use the following equations.

$$I_{SCP(max)} = \frac{I_{ILIM(max)} \times R_{ILIM} + 50\text{ mV}}{R_{DS(onMIN)}} \text{ A} \quad (9)$$

$$I_{SCP(min)} = \frac{I_{ILIM(min)} \times R_{ILIM} + 10\text{ mV}}{R_{DS(onMAX)}} \text{ A} \quad (10)$$

The TPS40075 provides short-circuit protection only. As such, it is recommended that the minimum short circuit protection level be placed at least 20% above the maximum output current required from the converter. The maximum output of the converter should be the steady state maximum output plus any transient specification that may exist.

The ILIM capacitor maximum value can be found from:

$$C_{ILIM(max)} = \frac{V_{OUT} \times 0.2}{V_{IN} \times R_{ILIM} \times f_{SW}} \text{ (Farads)} \quad (11)$$

Note that this is a recommended maximum value. If a smaller value can be used, it should be to improve protection. For most applications, consider using half the maximum value shown in Equation 11.

BOOST AND DBP BYPASS CAPACITANCE

The BOOST capacitance provides a local, low-impedance flying source for the high-side driver. The BOOST capacitor should be a good quality, high-frequency ceramic capacitor. A minimum value of 100-nF is suggested.

The DBP capacitor has to provide energy storage for switching both the synchronous MOSFET and the high-side MOSFET (via the BOOST capacitor). The suggested value for this capacitor is 1-µF ceramic, minimum.

INTERNAL REGULATORS

The internal regulators are linear regulators that provide controlled voltages for the drivers and the internal circuitry to operate from. The low-side driver operates directly from the 8-V regulator supply while the high-side driver bootstrap capacitor is charged from this supply. The actual voltage delivered to the high-side driver is the voltage on the DBP pin less any drop from the bootstrap diode. If the internal bootstrap diode is used, the drop across that diode is nominally 1.4 V at room temperature. This regulator has two modes of operation. At voltages below 8.5 V on VDD, the regulator is in a low dropout mode of operation and tries to provide as little impedance as possible from VDD to DBP. When VDD is above 10 V, the regulator regulates DBP to 8 V. Between these two voltages, the regulator is in whatever state it was in when VDD entered this region. The LVBP pin is connected to a 4.2-V regulator that supplies power for the internal control circuitry. Small amounts of current can be drawn from these pins for other external circuit functions, as long as power dissipation in the controller chip remains at acceptable levels and junction temperature does not exceed 125°C. Any external load connected to LVBP should be electrically quiet to avoid degrading performance of the TPS40075. Typical output voltages for these two regulators are shown in Figure 23 and Figure 24.

DIFFERENTIAL SENSE AMPLIFIER

The TPS40075 has an on board differential amplifier intended for use as a remote sensing amplifier for the output voltage. Use of this amplifier for remote sensing eliminates load regulation issues due to voltage drops that occur between the converter and the actual point of load. The amplifier is powered from the DBP pin and can be used to monitor output voltages up to 6 V with a DBP voltage of 8 V. For lower DBP voltages, the sense amplifier can be used to monitor output voltages up to 2-V below the DBP voltage. The internal resistors used to configure the amplifier for unity gain match each other closely, but their absolute values can vary as much as 30%, so adding external resistance to alter the gain is not accurate in a production environment.

SYNCHRONIZATION

The SYNC pin accepts logic level signals and is used to synchronize the TPS40075 to an external clock source. Synchronization occurs on the rising edge of the signal at the SYNC pin. There is a fixed delay of approximately 300 ns from the rising edge of the waveform at SYNC to the HDRV output turning on the high-side FET. The pin may be left floating in this function is not used, or it may be connected to GND. The frequency of the external clock must be greater than the free running frequency of the device as set by the resistor on the RT pin (R_{RT}). This pin requires a totem pole drive, or open collector/drain if pull up resistor to either LVBP or a separate supply between 2.5 V and 5 V is used. Synchronization does not affect the modulator gain due to the voltage feed forward circuitry. The programmable UVLO thresholds are affected by synchronization. The thresholds are shifted by the ratio of the sync frequency to the free running frequency of the converter. For example, synchronizing to a frequency 20% higher than the free running frequency results in the programmable UVLO thresholds shifting up 20% from their calculated free run values. The synchronization frequency should be kept less than 1.5 times the free run frequency for best performance, although higher multiples can be used.

POWERGOOD OPERATION

The PGD pin is an open drain output that actively pulls to GND if any of the following conditions are met (assuming that the input voltage is above 4.5 V)

- Soft-start is active (V_{VSS} < 3.5 V)
- V_{FB} < 0.63 V
- V_{FB} > 0.77 V
- Programmable UVLO condition not satisfied (V_{IN} below programmed level)
- Overcurrent condition exists
- Die temperature is greater than 165°C

PRE-BIASED OUTPUTS

Some applications require that the converter not sink current during startup if a pre-existing voltage exists at the output. Since synchronous buck converters inherently sink current some method of overcoming this characteristic must be employed. Applications that require this operation are typically power rails for a multi supply processor or ASIC. The method used in this controller, is to not allow the low side or rectifier FET to turn on until there the output voltage commanded by the start up ramp is higher than the pre-existing output voltage. This is detected by monitoring the internal pulse width modulator (PWM) for its first output pulse. Since this controller uses a closed loop startup, the first output pulse from the PWM does not occur until the output voltage is commanded to be higher than the pre-existing voltage. This effectively limits the controller to sourcing current only during the startup sequence.

If the pre-existing voltage is higher that the intended regulation point for the output of the converter, the converter starts and sinks current when the soft-start time has completed

SHUTDOWN AND SEQUENCING

The TPS40075 can be shut down by pulling the SS pin to a level below 250 mV. Pulling the pin low resets the internal pre-bias circuitry to ensure that the converter does not damage sensitive loads.

Automatic startup sequencing can be accomplished by connecting the PGD pin of a master supply based on the TPS40075 to the SS pin of a slave supply. The master comes up first and release the salve SS pin to allow the slave to come up. Controlled shutdown of sequenced supplies can be accomplished by either pulling the SS pin of the master below the shutdown threshold and letting the PGD pin pull the slave SS pin down, or by pulling down the SS pins of all supplies simultaneously.

TPS40075 POWER DISSIPATION

The power dissipation in the TPS40075 is largely dependent on the MOSFET driver currents and the input voltage. The driver current is proportional to the total gate charge, Qg, of the external MOSFETs. Driver power (neglecting external gate resistance) can be calculated from:

$$P_D = Q_g \times V_{DR} \times f_{SW} \quad \text{(Watts/driver)} \tag{12}$$

where

- V_{DR} is the driver output voltage

The total power dissipation in the TPS40075, assuming the same MOSFET is selected for both the high-side and synchronous rectifier is described in Equation 13.

$$P_T = \left(\frac{2 \times P_D}{V_{DR}} + I_Q\right) \times V_{IN} \quad \text{(Watts)} \tag{13}$$

or

$$P_T = \left(2 \times Q_g \times f_{SW} + I_Q\right) \times V_{IN} \quad \text{(Watts)} \tag{14}$$

where

- I_Q is the quiescent operating current (neglecting drivers)

The maximum power capability of the TPS40075 PowerPAD package is dependent on the layout as well as air flow. The thermal impedance from junction to air ambient assuming 2-oz. copper trace and thermal pad with solder and no air flow is θ_{JA} = 60 °C/W

The maximum allowable package power dissipation is related to ambient temperature by Equation 15.

$$P_T = \frac{T_J - T_A}{\theta_{JA}} \quad \text{(Watts)} \tag{15}$$

Substituting Equation 15 into Equation 14 and solving for f_{SW} yields the maximum operating frequency for the TPS4007x. The result is described in Equation 16.

$$f_{SW} = \frac{\left(\left[\frac{(T_J - T_A)}{(\theta_{JA} \times V_{IN})}\right] - I_Q\right)}{\left(2 \times Q_g\right)} \quad \text{(Hz)} \tag{16}$$

BOOST DIODE

The TPS40075 has internal diodes to charge the boost capacitor connected from SW to BOOST. The drop across this diode is rather large at 1.4-V nominal at room temperature resulting in the drive voltage to the high-side MOSFET being reduced by this amount from the DBP voltage. If this drop is too large for a particular application, an external diode may be connected from DBP (anode) to BOOST (cathode). This provides significantly improved gate drive for the high-side MOSFET, especially at lower input voltages.

GROUNDING AND BOARD LAYOUT

The TPS40075 provides separate signal ground (GND) and power ground (PGND) pins. Care should be given to proper separation of the circuit grounds. Each ground should consist of a plane to minimize its impedance if possible. The high power *noisy* circuits such as the output, synchronous rectifier, MOSFET driver decoupling capacitor (DBP), and the input capacitor should be connected to PGND plane.

Sensitive nodes such as the FB resistor divider and RT should be connected to the GND plane. The GND plane should only make a single point connection to the PGND plane. It is suggested that the GND pin be tied to the copper area for the PowerPAD underneath the chip. Tie the PGND to the PowerPAD copper area as well and make the connection to the power circuit ground from the PGND pin. Reference the output voltage divider to the GND pin.

Component placement should ensure that bypass capacitors (LVPB and DBP) are located as close as possible to their respective power and ground pins. Also, sensitive circuits such as FB, RT and ILIM should not be located near high dv/dt nodes such as HDRV, LDRV, BOOST, and the switch node (SW). Failure to follow careful layout practices results in sub-optimal operation.

SYNCHRONOUS RECTIFIER CONTROL

Table 2 describes the state of the rectifier MOSFET control under various operating conditions.

Table 2. Synchronous Rectifier MOSFET States

SYNCHRONOUS RECTIFIER OPERATION DURING			
SOFT-START	**NORMAL**	**FAULT (FAULT RECOVERY IS SAME AS SOFT-START)**	**OVERVOLTAGE**
Off until first high-side pulse is detected, then on when high-side MOSFET is off	Turns off at the start of a new cycle. Turns on when the high-side MOSFET is turned off	OFF	Turns OFF only at start of next cycle ON if duty cycle is > 0

For proper operation, the total gate charge of the MOSFET connected to LDRV should be less than 50nC.

DESIGN EXAMPLE

1. SPECIFICATIONS

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
INPUT CURRENT						
V_{IN}	Input voltage		10.8	12.0	13.2	V
V_O	Output voltage	I_{OUT} = 10 A		1.5	5	
	Regulation		1.47		1.53	
V_{RIPPLE}	Output ripple voltage	$I_{O(max)}$ = 15 A		30		mV
V_{OVER}	Output overshoot	I_{STEP} = 8 A		50		
V_{UNDER}	Output undershoot	I_{STEP} = 8 A		50		
I_{LOAD}	Output current		0		15	A
I_{SCP}	Short circuit current trip point		16		30	
η	Efficiency	V_{IN} = 12 V, I_{LOAD} = 15 A		85%		
f_{SW}	Switching frequency			400		kHz

2. SCHEMATIC

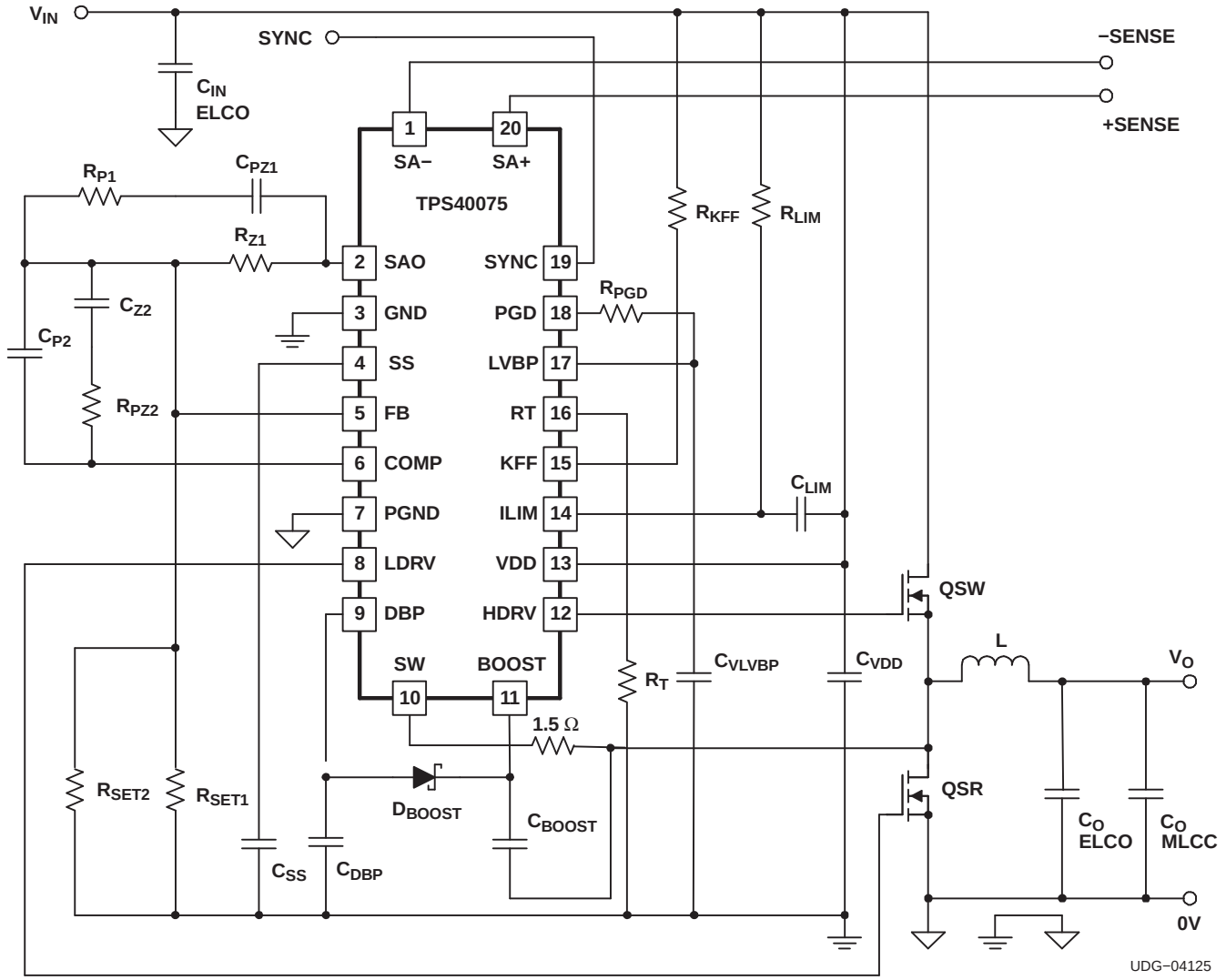


Figure 29. TPS40075 Reference Design Schematic

3. COMPONENT SELECTION

3. 1 Power Train Components

Designers familiar with the buck converter can skip to section ***3.2 Component Selection for TPS40075***.

3.1.1 Output Inductor, L_O

The output inductor is one of the most important components to select. It stores the energy necessary to keep the output regulated when the switch MOSFET is turned off. The value of the output inductor dictates the peak and RMS currents in the converter. These currents are important when selecting other components. Equation 17 can be used to calculate a value for L.

$$L = \frac{V_O}{V_{IN(max)}} \times \frac{\left(V_{IN(max)} - V_O\right)}{f_{SW} \times \Delta I} \tag{17}$$

Δ I is the allowable ripple in the inductor. Selecting ΔI also sets the output current when the converter goes into discontinuous mode (DCM) operation. Since this converter utilizes MOSFETs for the rectifier, DCM is not a major concern. Select ΔI to be between 20% and 30% of maximum I_{LOAD}. For this design, ΔI of 3 A was selected. The calculated L is 1.1 µH. A standard inductor with value of 1.0 µH was chosen. This increases ΔI by about 10% to 3.3 A.

With this ΔI value, calculate the RMS and peak current flowing in L_O. Note this peak current is also seen by the switching MOSFET and synchronous rectifier.

$$I_{LOAD\_RMS} = \sqrt{I_{LOAD}{}^2 + \frac{\Delta I^2}{12}} = 15.03 \text{ A} \tag{18}$$

$$I_{PK} = I_{LOAD} + \frac{\Delta I^2}{2} = 16.65 \text{ A} \tag{19}$$

3.1.2 Output Capacitor, C_O, ELCO and MLCC

Several parameters must be considered when selecting the output capacitor. The capacitance value should be selected based on the output overshoot, V_{OVER}, and undershoot, V_{UNDER}, during a transient load, I_{STEP}, on the converter. The equivalent series resistance (ESR) is chosen to allow the converter meet the output ripple specification, V_{RIPPLE}. The voltage rating must be greater than the maximum output voltage. Other parameters to consider are: equivalent series inductance which is important in fast transient load situations. Also size and technology can be factors when choosing the output capacitor. In this design a large capacitance electrolytic type capacitor, C_O ELCO, is used to meet the overshoot and under shoot specifications. Its ESR is chosen to meet the output ripple specification. While a smaller multiple layer ceramic capacitor, C_O MLCC, is used to filter high frequency noise.

The minimum required capacitance and maximum ESR can be calculated using the equations below.

$$C_O > \frac{L \times I_{STEP}{}^2}{2 \times V_{UNDER} \times D_{MAX} \times \left(V_{IN} - V_O\right)} \tag{20}$$

$$C_O > \frac{L \times I_{STEP}{}^2}{2 \times V_{OVER} \times V_O} \tag{21}$$

$$ESR < \frac{V_{RIPPLE}}{\Delta I} \tag{22}$$

Using Equation 20 through Equation 22, the capacitance for C_O should be greater than 495 µF and its ESR should be less than 9.1mΩ. The 1000 µF/25 V capacitor from Rubycon's MBZ or Panasonic's series EEU-FL was chosen. Its ESR is 19 mΩ, so two in parallel are used. The slightly higher ESR is offset by the four times increase in capacitance. A 2.2 µF/16 V MLCC is also added in parallel to reduce high frequency noise.

3.1.3. Input Capacitor, C_{IN}, ELCO and MLCC

The input capacitor is selected to handle the ripple current of the buck stage. Also a relative large capacitance is used to keep the ripple voltage on the supply line low. This is especially important where the supply line is high impedance. It is recommended that the supply line be kept low impedance. The input capacitor ripple current can be calculated using Equation 23.

$$I_{CAP(RMS)} = \sqrt{\left[\left(I_{LOAD(max)} - I_{IN(avg)}^{2}\right) + \frac{\Delta I^2}{12}\right] \times D + I_{IN(avg)}^{2} \times (1 - D)} \quad (23)$$

where

- $I_{IN(avg)}$ is the average input current

This is calculated simply by multiplying the output DC current by the duty cycle. The ripple current in the input capacitor is 5.05 A. A 1206 MLCC using X7R material has a typical dissipation factor of 5%. For a 2.2 µF capacitor at 400 kHz the ESR is approximately 7.2 mΩ. If two capacitors are used in parallel the power dissipation in each capacitor is less than 46 mW.

A 470 µF/16 V electrolytic capacitor is added to maintain the voltage on the input rail.

3.1.4 Switching MOSFET, QSW

The following key parameters must be met by the selected MOSFET.

- Drain source voltage, V_{DS}, must be able to withstand the input voltage plus spikes that may be on the switching node. For this design a V_{DS} rating of 25 V to 30 V is recommended.
- Drain current, I_D, at 25°C, must be greater than that calculated using Equation 24. For this design, I_D should be greater than 5 A.

$$I_D = \sqrt{\frac{V_O}{V_{IN(min)}} \times \left(I_{LOAD(max)}^{2} + \frac{\Delta I^2}{12}\right)} \quad (24)$$

- Gate source voltage, V_{GS} must be able to withstand the gate voltage from the control device . For the TPS40075 this is 9 V.

Once the above boundary parameters are defined the next step in selecting the switching MOSFET is to select the key performance parameters. Efficiency is the performance characteristic which drives the other selection criteria. Target efficiency for this design is 90%. Based on 1.5-V output and 15 A this equates to a power loss in the converter of 2.5 W. Using this figure a target of 0.5 W dissipated in the switching MOSFET was chosen.

Equation 25 through Equation 28 can be used to calculate the power loss, P_{QSW}, in the switching MOSFET

$$P_{QSW} = P_{QSW(CON)} + P_{QSW(SW)} + P_{QSW(GATE)} \quad (25)$$

$$P_{QSW(CON)} = R_{DS(on)} \times I_D{}^2 = R_{DS(on)} \times \frac{V_O}{V_{IN}} \times \left(I_{LOAD}{}^2 + \frac{\Delta I^2}{12}\right) \quad (26)$$

$$P_{QSW(SW)} = V_{IN} \times f_{SW} \times \left[\frac{\left(I_{LOAD} + \frac{\Delta I}{2}\right) \times \left(Q_{gs1} + Q_{gd}\right)}{I_g} + \frac{Q_{OSS(SW)} + Q_{OSS(SR)}}{2}\right] \quad (27)$$

$$P_{QSW(GATE)} = Q_{g(TOT)} \times V_g \times F_{SW} \quad (28)$$

where

- $P_{QSW(CON)}$ = conduction losses
- $P_{QSW(SW)}$ = switching losses
- $P_{QSW(GATE)}$ = gate drive losses
- Q_{gd} = drain source charge or miller charge
- Q_{gs1} = gate source post threshold charge
- I_g = gate drive current
- $Q_{OSS(SW)}$ = switching MOSFET output charge
- $Q_{OSS(SR)}$ = synchronous MOSFET output charge
- $Qg_{(TOT)}$ = total gate charge from zero volts to the gate voltage
- Vg = gate voltage

If the total estimated loss is split evenly between conduction and switching losses, Equation 25 and Equation 26 yields preliminary values for $R_{DS(on)}$ and $(Q_{gs1} + Q_{gd})$. Note output losses due to Q_{OSS} and gate losses have been ignored here. Once a MOSFET is selected these parameters can be added.

The switching MOSFET for this design should have an $R_{DS(on)}$ of less than 9 mΩ. The sum of Q_{gd} and Q_{gs} should be approximately 4 nC.

It is not always possible to get a MOSFET which meets both these criteria so a comprise may have to be made. Also by selecting different MOSFETs close to this criteria and calculating power loss the final selection can be made. It was found that the PH6325L MOSFET from Philips semiconductor gave reasonable results. This device has an $R_{DS(on)}$ of 6.3 mΩ and a (Qgs1+Qgd) of 5.9 nC. The estimated conduction losses are 0.178 W and the switching losses are 0.270 W. This gives a total estimated power loss of 0.448 W versus 0.5 W for our initial boundary condition. Note this does not include gate losses of approximately 10 mW and output losses of less than 1 mW.

3.1.5 Rectifier MOSFET, QSR

Similar criteria can be used for the rectifier MOSFET. There is one significant difference. Due to the body diode conducting, the rectifier MOSFET switches with near zero voltage across its drain and source so effectively with near zero switching losses. However, there are some losses in the body diode. These are minimized by reducing the delay time between the transition from the switching MOSFET turn off to rectifier MOSFET turn on and vice versa. The TPS40075 incorporates TI's proprietary predictive gate drive which helps reduce this delay to between 10 ns and 20 ns.

The calculations for the losses in the rectifier MOSFET are show in Equation 29 through Equation 32.

$$P_{QSR} = P_{QSR(CON)} + P_{DIODE} + P_{QSR(GATE)} \quad (29)$$

$$P_{QSW(CON)} = R_{DS(on)} \times I_D{}^2 = R_{DS(on)} \times \frac{V_O}{V_{IN}} \times \left(I_{LOAD}{}^2 + \frac{\Delta I^2}{12}\right) \quad (30)$$

$$P_{DIODE} = V_f \times I_{LOAD} \times (t_1 + t_2) \times f_{SW} \quad (31)$$

$$K_{PWM} \cong \frac{V_{UVLO}}{1\ V} \quad (32)$$

where

- P_{DIODE} = body diode losses
- t_1 = body diode conduction prior to turn on of channel = 10 ns for predictive gate drive
- t_2 = body diode conduction after turn off of channel = 10 ns for predictive gate drive
- V_f = body diode forward voltage

Estimating the body diode losses based on a forward voltage of 1.2 V gives 0.142 W. The gate losses are unknown at this time so assume 0.1 W gate losses. This leaves 0.258 W for conduction losses. Using this figure a target $R_{DS(on)}$ of 1.1 mΩ was calculated. This is an extremely low value. It is not possible to meet this without paralleling multiple MOSFETs. Paralleling MOSFETs increases the gate capacitance and slows down switching speeds. This increases body diode and gate losses.

The PH2625L from Philips was chosen. Using the parameters from its data sheet the actual expected power losses were calculated. Conduction loss is 0.527 W, body diode loss is 0.142 W and the gate loss was 0.174 W. This totals 0.843 W associated with the rectifier MOSFET. This is somewhat greater than the initial allowance. Because of this the converter may not hit its efficiency figure at the maximum load.

Two other criteria should be verified before finalizing on the rectifier MOSFET. One is the requirement to ensure that predictive gate drive functions correctly. The maximum turn off delay of the PH2625L is 67 ns. The minimum turn on delay of the PH6325L is 25 ns. These devices easily meet the 100 ns difference requirement.

Secondly the ratio between C_{gs} and C_{gd} should be greater than 1. The C_{gs} of the PH2625L is 2133 pF and the Cgd is 1622 pF, so the C_{gs}:C_{gd} ratio is 1.3:1. This helps reduce the risk of dv/dt induced turn on of the rectifier MOSFET. If this is likely to be a problem a small resistor may be added in series with the boost capacitor, C_{BOOST}.

3.2 Component Selection for TPS40075

3.2.1 Timing Resistor, R_T

The timing resistor is calculated using the following equation.

$$R_T = \frac{1}{f_{SW} \times 17.82 \times 10^{-6}} - 23 \quad (33)$$

This gives a resistor value of 89.2 kΩ. Using the E24 range of resistor values a 118-kΩ resistor was selected. The nominal frequency using this resistor is 398 kHz.

3.2.2 Feed Forward and UVLO Resistor, R_{KFF}

A resistor connected to the KFF pin of the device feeds into the ramp generator. This resistor provides current into the ramp generator proportional to the input voltage. The ramp is then adjusted to compensate for different input voltages. Is provides the voltage feed forward feature of the TPS40075.

The same resistor also sets the under voltage lock out point. The input start voltage should be used to calculate a value for R_{KFF}. For this converter the minimum input voltage is 10.8 V however due to tolerances in the device, a start voltage of 15% less than the minimum input voltage is selected. The start voltage for R_{KFF} calculation is 9.18 V. Using Equation 34 R_{KFF} can be selected.

$$R_{KFF} = \frac{\left(V_{UVLO(on)} - 0.5\right)}{\left(0.018 + \left(\frac{5}{R_T}\right)\right)} \quad (34)$$

This equation gives a R_{KFF} value of 136 kΩ. The closest lower standard value should be selected. For this design and using E24 resistor range 133 kΩ was chosen. This yields a typical start voltage of 8.52 V.

3.2.3 Soft Start Capacitor

It is good practice to limit the rise time of the output voltage. This helps prevent output overshoot and possible damage to the load. The selection of the soft start time is arbitrary, but it must meet one condition; it should be greater than the time constant of the output filter, L and C_O. This time is given by Equation 35

$$t_{START} \geq 2\pi \times \sqrt{L \times C_O} \quad (35)$$

The soft-start time must be greater than 0.281 ms. A time of 1 ms was chosen, this time also helps keep the initial input current during start up low. The value of C_{SS} can be calculated using Equation 36.

$$C_{SS} \geq \frac{12 \times 10^{-6}}{0.7} \times t_{START} \quad (36)$$

C_{SS} should be greater than 17 nF, a 22 nF MLCC was chosen. The calculated start time using this capacitor is 1.28 ms.

3.2.4 Short Circuit Protection, R_{ILIM} and C_{ILIM}

Short circuit protection is programmed using the R_{ILIM} resistor. Selection of this resistor depends on the $R_{DS(on)}$ of the switching MOSFET selected and the required short circuit current trip point, I_{SCP}. The minimum I_{SCP} is limited by the inductor peak current, the output voltage, the output capacitor and the soft start time. Their relationship is given by Equation 37. A short circuit current trip point greater than that calculated by this equation should be used.

$$I_{SCP} \geq \frac{C_O \times V_{OUT}}{t_{START}} + I_{LOAD} \times \frac{\Delta I}{2} \quad (37)$$

The minimum short circuit current trip point for this design is 16.35 A. This value is used in Equation 38 to calculate the minimum R_{ILIM} value.

$$R_{ILIM} \geq \frac{I_{SCP} \times R_{DS(on)MAX} + V_{ILIM(min)}}{I_{SINK(max)}} \quad (38)$$

R_{ILIM} is calculated to be 1.14 kΩ . The closest standard value greater than 1.14 kΩ is chose, this is 1.15 kΩ. To verify that the short circuit current requirements are met the minimum and maximum short circuit current can be calculated using Equation 39 and Equation 40.

$$I_{SCP(min)} = \frac{I_{SINK(min)} \times R_{ILIM(min)} - V_{ILIM(max)}}{R_{DS(on)MIN}} \quad (39)$$

$$I_{SCP(max)} = \frac{I_{SINK(max)} \times R_{ILIM(max)} - V_{ILIM(min)}}{R_{DS(on)MAX}} \quad (40)$$

The minimum I_{SCP} is 17.09 A and the maximum is 29.45 A.

It is recommended to add a small capacitor, C_{ILIM}, across R_{ILIM}. The value of this capacitor should be less than that calculated in Equation 41.

$$C_{ILIM(max)} = \frac{V_O \times 0.2}{V_{IN} \times R_{ILIM} \times f_{SW}} \quad (41)$$

This equation yields a maximum C_{ILIM} of 44 pF. A value half this is chosen, 22 pF.

3.2.5 Voltage Decoupling Capacitors, C_{DBP}, C_{LVBP} and C_{VDD}

Several pins on the TPS40075 have DC voltages. It is recommended to add small decoupling capacitors to these pins. Below is a list of the recommended values.

- C_{DBP} = 1.0 µF
- C_{LVBP} = 0.1 µF
- C_{VDD} = 4.7 µF

3.2.6 Boost Voltage, C_{BOOST} and D_{BOOST} (optional)

A capacitor charge pump or boost circuit is required to drive an N-channel MOSFET in the switch location of a buck converter . The TPS40075 contains the elements for this boost circuit. The designer just has to add a capacitor, C_{BOOST}, from the switch node of the buck power stage to the BOOST pin of the device. Selection of this capacitor is based on the total gate charge of the switching MOSFET and the allowable ripple on the boost voltage, ΔV_{BOOST}. A ripple of 0.15 V is assumed for this design. Using these two parameters and Equation 42 the minimum value for C_{BOOST} can be calculated.

$$C_{BOOST} > \frac{Q_{g(TOTAL)}}{\Delta V_{BOOST}} \tag{42}$$

The total gate charge of the switching MOSFET is 13.3 nC. A minimum C_{BOOST} of 0.089 µF is required. A 0.1 µF capacitor was chosen.

This capacitor must be able to withstand the maximum voltage on DBP (10 V in this instance). A 50 V capacitor is used for expediancy.

To reduce losses in the TPS40075 and to increase the available gate voltage for the switching MOSFET an external diode can be added between the DBP pin and the BOOST pin of the device. A small signal schottky should be used here, such as the BAT54.

3.3 Closing the Feedback Loop, R_{Z1}, R_{P1}, R_{PZ2}, R_{SET1}, R_{SET2}, C_{Z2}, C_{P2} and C_{PZ1}

A graphical method is used to select the compensation components. This is a standard feedforward buck converter. Its PWM gain is shown in Equation 43.

$$K_{PWM} \cong \frac{V_{UVLO}}{1\ V} \tag{43}$$

The gain of the output L-C filter is given by Equation 44

$$K_{LC} = \frac{\left(1 + s \times ESR \times C_O\right)}{1 + s \times \left(\frac{L}{R_{LOAD}}\right) + s^2 \times L \times C_O} \tag{44}$$

The PWM and LC gain is, shown in Equation 45.

$$G_e(s) = K_{PWM} \times K_{LC} = \frac{V_{UVLO}}{1\ V} \times \frac{\left(1 + s \times ESR \times C_O\right)}{1 + s \times \left(\frac{L}{R_{LOAD}}\right) + s^2 \times L \times C_O} \tag{45}$$

To describe this in a Bode plot, the DC gain must be expressed in dB. The DC gain is equal to K_{PWM}. To express this in dB we take its LOG and multiple by 20. For this converter the DC gain is shown in Equation 46.

$$DCGAIN = 20 \times LOG\left(\frac{V_{UVLO}}{1\ V}\right) = 20 \times LOG(8.752) = 18.8\ dB \tag{46}$$

The pole and zero frequencies should be calculated, also. A double pole is associated with the L-C and a zero is associated with the ESR of the output capacitor. The frequency at where these occur can be calculated using the following two equations.

$$f_{LC\_Pole} = \frac{1}{2\pi \times \sqrt{L \times C_O}} = 3559 \text{ Hz} \quad (47)$$

$$f_{ESR\_Zero} = \frac{1}{2\pi \times ESR \times C_O} = 8377 \text{ Hz} \quad (48)$$

The resulting bode plot is shown in Figure 30.

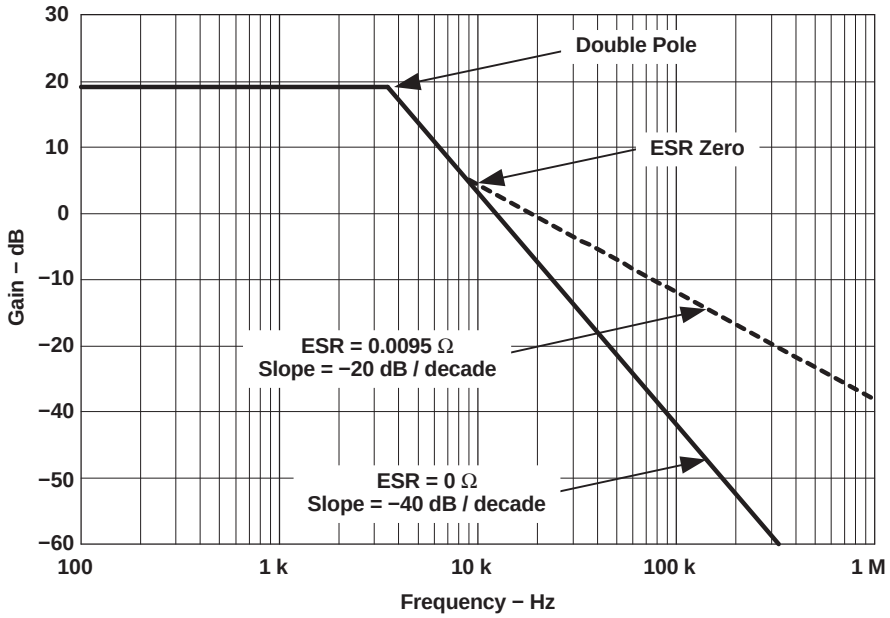


Figure 30. PWM and LC Filter Gain

The next step is to establish the required compensation gain to achieve the desired overall system response. The target response is to have the crossover frequency between 1/10 to 1/4 times the switching frequency. To have a phase margin greater than 45° and a gain margin greater than 6 dB.

A Type III compensation network, as shown in Figure 31, was used for this design. This network gives the best overall flexibility for compensating the converter.

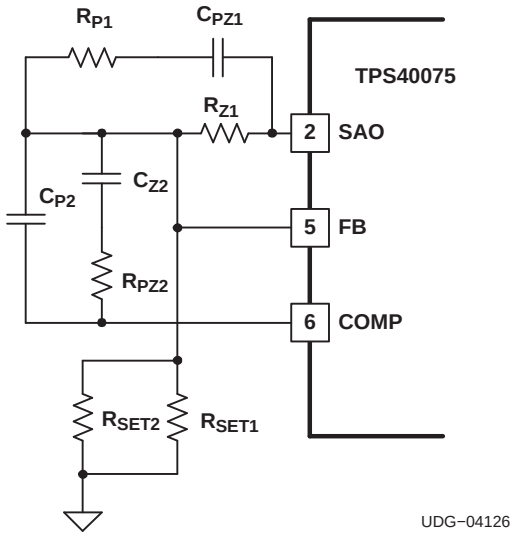


Figure 31. Type III Conpensation with TPS40075

A typical bode plot to this type of compensation network is shown in Figure 32.

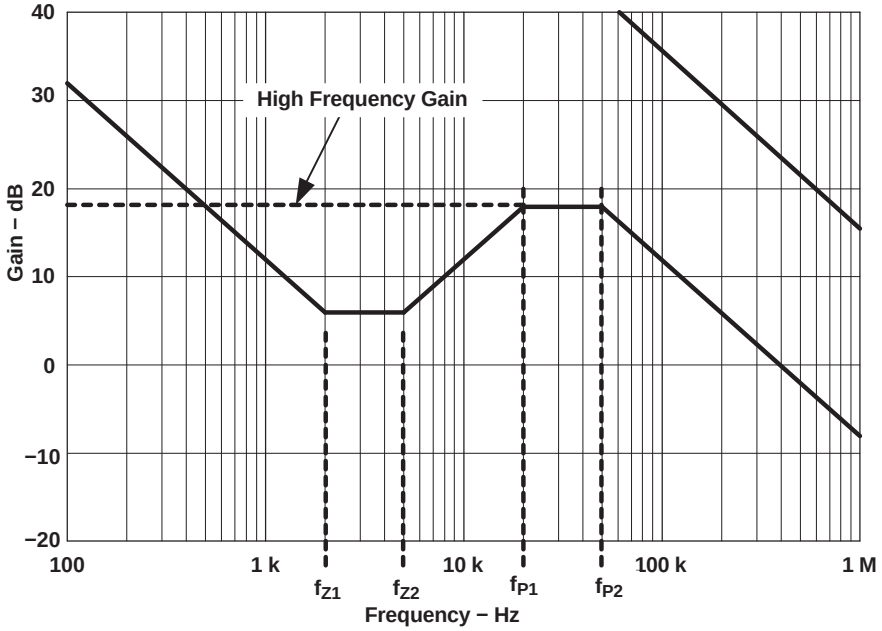


Figure 32. Type III Compensation Bode Plot

The high frequency gain and the break (pole and zero) frequencies are calculated using the following equations.

$$V_O = V_{FB} \times \frac{R_{Z1} + R_{SET}}{R_{SET}} \quad (49)$$

$$R_{SET} = \frac{R_{SET1} \times R_{SET2}}{R_{SET1} + R_{SET2}} \quad (50)$$

$$GAIN = \frac{R_{PZ2}}{\left(\frac{R_{Z1} \times R_{P1}}{R_{Z1} + R_{P1}}\right)} \quad (51)$$

$$f_{P1} = \frac{1}{2\pi \times R_{P1} \times C_{PZ1}} \quad (52)$$

$$f_{P2} = \frac{C_{P2} + C_{Z2}}{2\pi \times R_{PZ2} \times C_{P2} \times C_{Z2}} \cong \frac{1}{2\pi \times R_{PZ2} \times C_{P2}} \quad (53)$$

$$f_{Z1} = \frac{1}{2\pi \times R_{Z1} \times C_{PZ1}} \quad (54)$$

$$f_{Z2} = \frac{1}{2\pi \times \left(R_{PZ2} + R_{P1}\right) \times C_{Z2}} \cong \frac{1}{2\pi \times R_{PZ2} \times C_{Z2}} \quad (55)$$

Using this PWM and L-C bode plot the following actions ensure stability.

1. Place two zero's close to the double pole, i.e. $f_{Z1} = f_{Z2} = 3559$ Hz
2. Place a pole at one octave below the desired crossover frequency. The crossover frequency was selected as one quarter the switching frequency, $f_{CO} = 100$ kHz, $f_{P1} = 50$ kHz
3. Place the second pole about an octave above f_{co}. This ensures that the overall system gain falls off quickly to give good gain margin, $f_{P2} = 200$ kHz
4. The high-frequency gain is sufficient to ensure 0 dB at the required crossover frequency, GAIN = -1 GAIN of PWM and LC at the crossover frequency, GAIN = 17.6 dB, or 7.586

Desired frequency response and resultant overall system response can be seen in Figure 33.

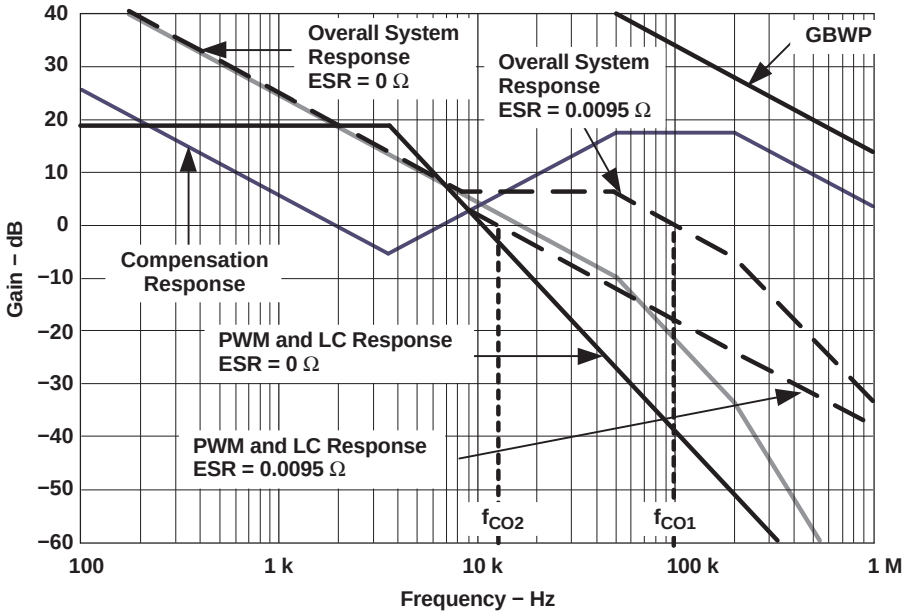


Figure 33. Overall System Bode Plot

Using these values and the equations above the resistors and capacitors around the compensation network can be calculated.

1. Set R_{Z1} = 10 kΩ.
2. Calculate R_{SET} using Equation 49; R_{SET} = 8750 Ω. Two resistors in parallel, R_{SET1} and R_{SET2}, are used to make up R_{SET}. R_{SET1} = 9.53 kΩ, R_{SET2} = 105 kΩ.
3. Using Equation 54 and f_{Z1} = 3559 Hz, C_{PZ1} can be calculated to be 4.47 nF; C_{PZ1}= 4.7 nF.
4. F_{P1} and Equation 52 yields R_{P1} to be 677 Ω, R_{P1} = 680 Ω.
5. The required gain of 17.6 dB (7.586) and Equation 52 sets the value for R_{PZ1}. Note actual gain used for this calculation was 20 dB (10), this ensures that the gain of the transfer function is high enough, R_{PZ1} = 6.2 kΩ.
6. C_{Z2} is calculated using Equation 55 and the desired frequency for the second zero, C_{Z2} = 6.8 nF.
7. C_{P2} is calculated using the second pole frequency and Equation 53, C_{P2} = 150 pF.

Using MathCAD the above values were used to draw the actual Bode plot for gain and phase. From these plots the crossover frequency, phase margin and gain margin can be recorded.

Table 3. Equivalent Series Resistance

ESR (Ω)	CROSSOVER FREQUENCY (kHz)	PHASE MARGIN (°)	GAIN MARGIN (dB)
0	23.1	72	> 46
0.0095	98.6	78.8	> 33

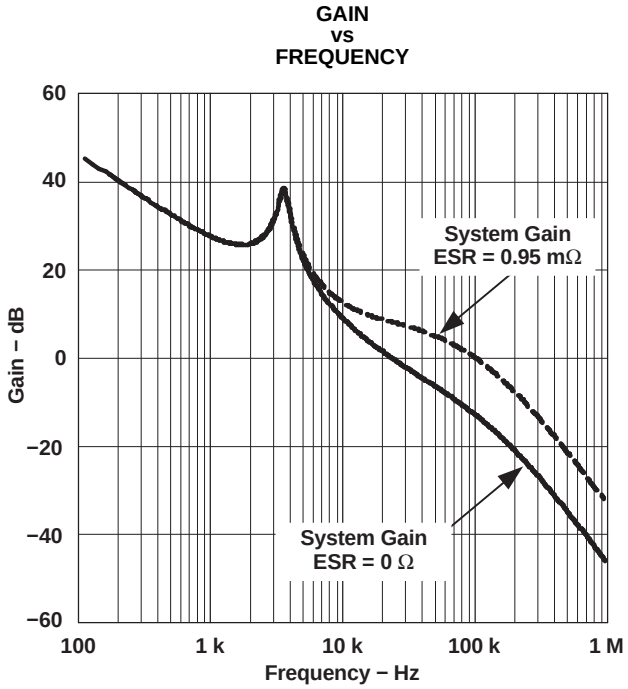


Figure 34.

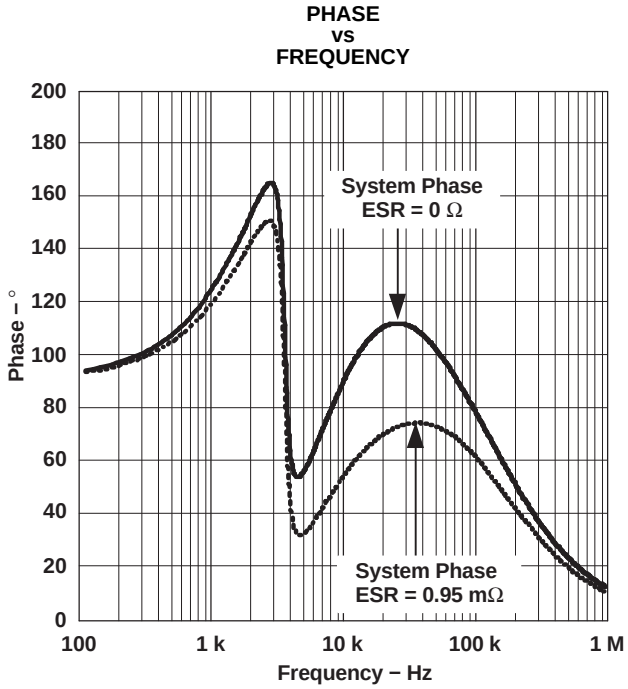
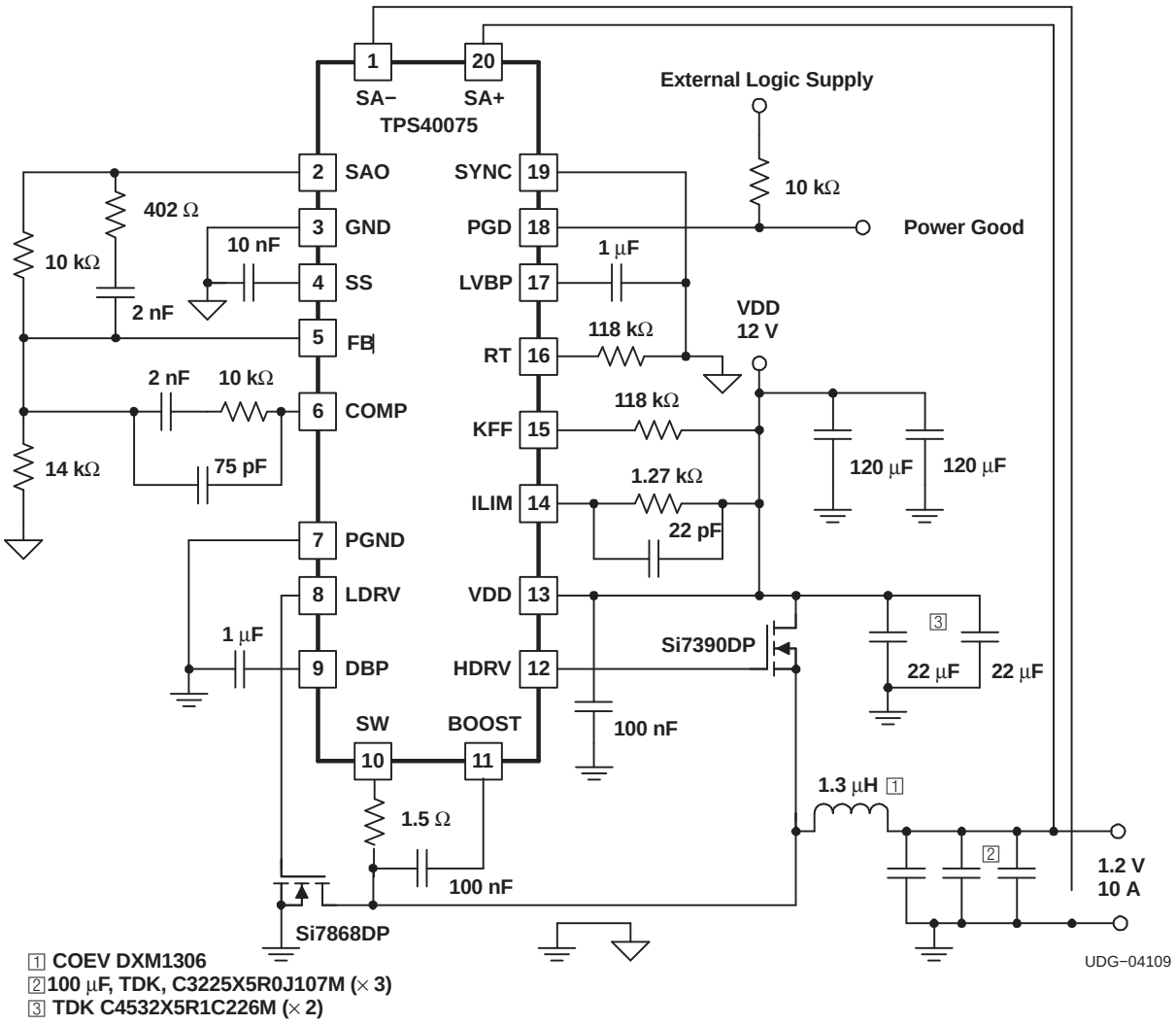


Figure 35.

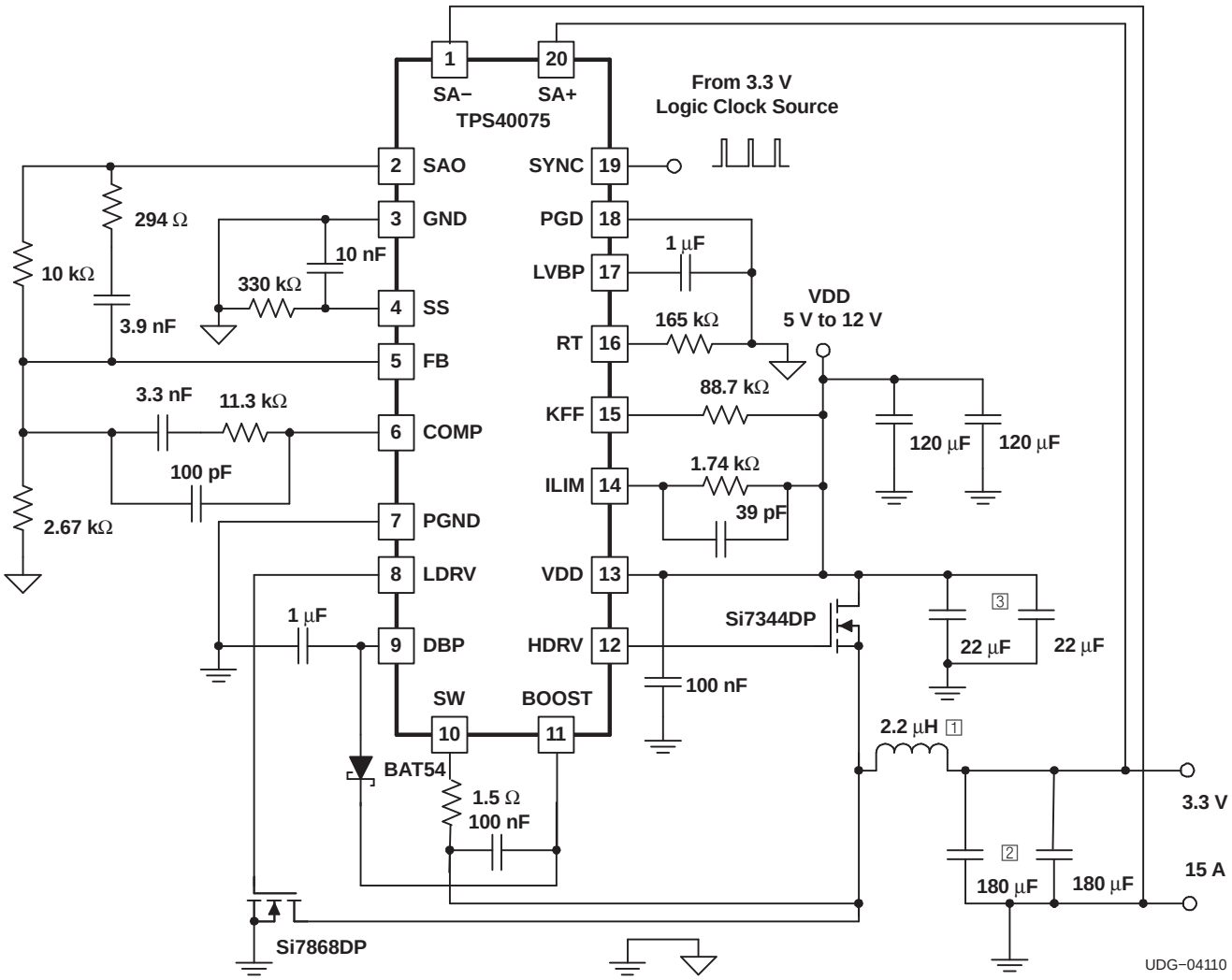
ALTERNATE APPLICATIONS

Some alternative applicaiton diagrams are shown in Figure 36 through Figure 38.



1 COEV DXM1306
2 100 µF, TDK, C3225X5R0J107M (× 3)
3 TDK C4532X5R1C226M (× 2)

Figure 36. 400 kHz, 12 V to 1.2 V Converter with Powergood Indication



1 Coiltronics HC2LP−2R2 or
Vishay IHLP5050FDRZ2R2M01

2 Panasonic EEF−SE0J181R (× 2)

3 TDK C4532X5R1C226M (×2)

Figure 37. 300 kHz Intermediate Bus (5 V to 12 V) to 3.3 V Converter

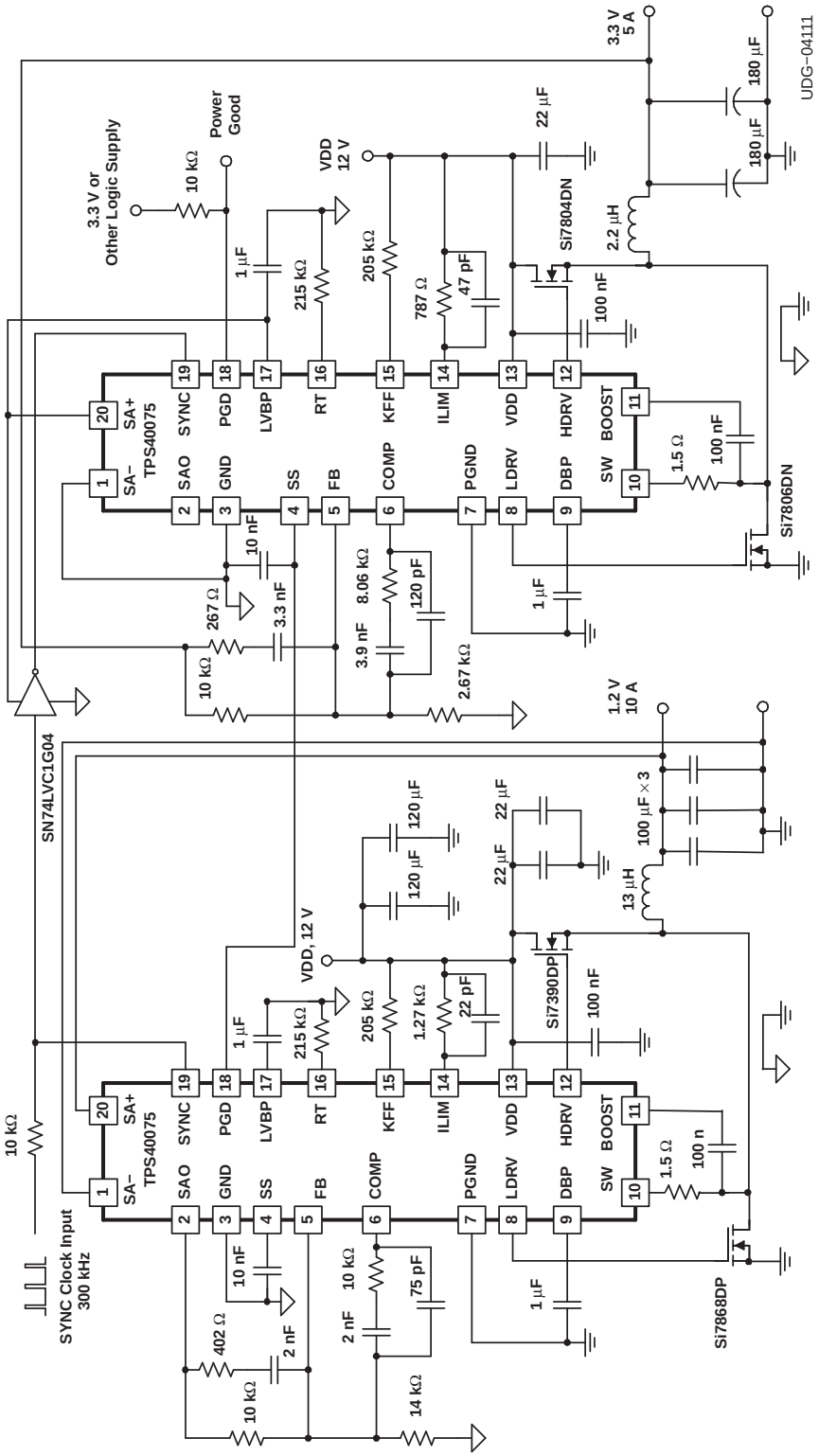


Figure 38. Sequenced Supplies, Synchronized 180° Out of Phase

ADDITIONAL REFERENCES

The following parts are similar to the TPS40075 and may be of interest:

1. TPS40071 Mid Range Input (4.5 V to 28 V) up to 1-MHz Frequency Synchronous Buck Controller
2. TPS40100 Wide Input Range Synchronous Buck Controller for Sequencing
3. TPS40057 Wide Input (8 V to 40 V) up to 1MHz Frequency Synchronous Buck Controller, source/sink with prebias
4. TPS40190 Low Pin Count Synchronous Buck DC/DC Controller

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TPS40075RHLR	Active	Production	VQFN (RHL) | 20	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	40075
TPS40075RHLR.A	Active	Production	VQFN (RHL) | 20	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	40075
TPS40075RHLRG4	Active	Production	VQFN (RHL) | 20	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	40075
TPS40075RHLRG4.A	Active	Production	VQFN (RHL) | 20	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	40075
TPS40075RHLT	Active	Production	VQFN (RHL) | 20	250 | SMALL T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	40075
TPS40075RHLT.A	Active	Production	VQFN (RHL) | 20	250 | SMALL T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	40075
TPS40075RHLTG4	Active	Production	VQFN (RHL) | 20	250 | SMALL T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	40075

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

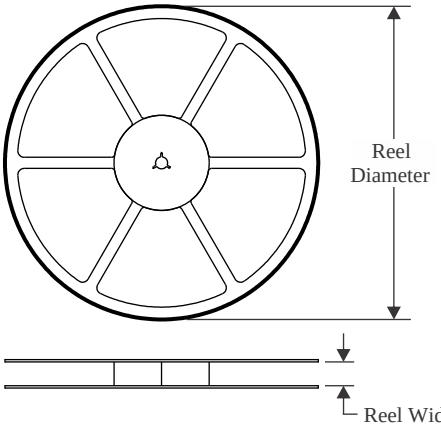
(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

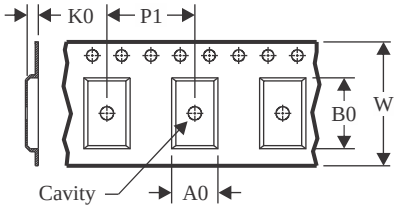
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

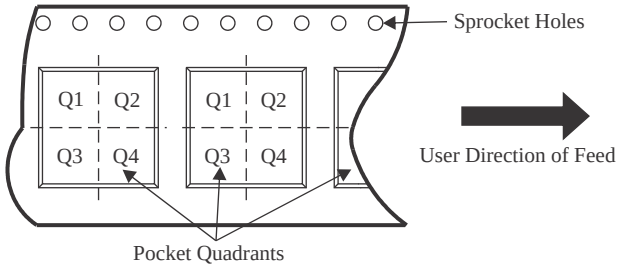


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

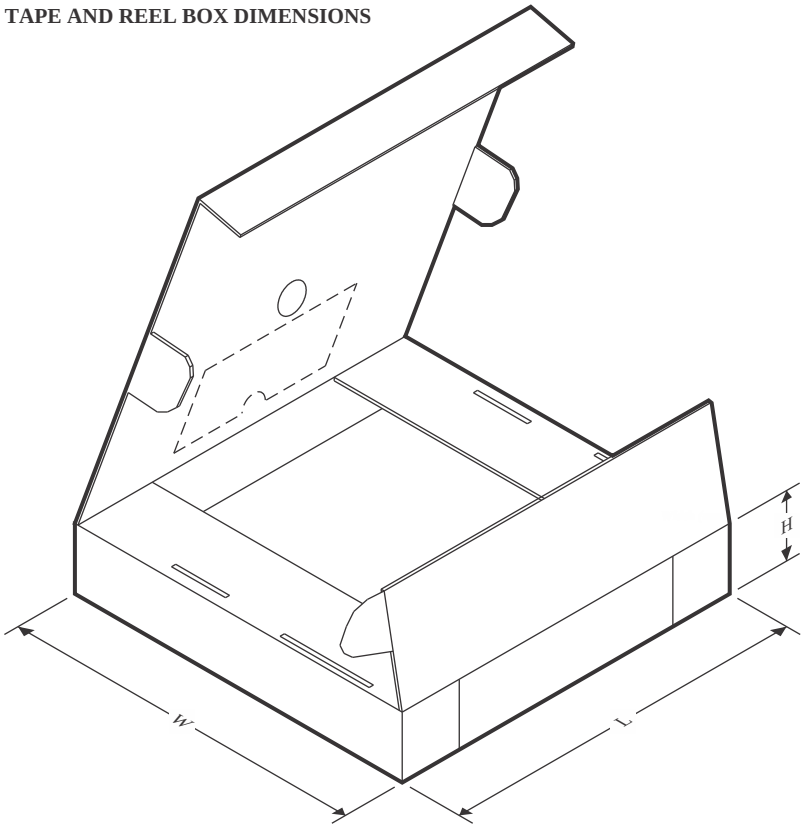
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS40075RHLR	VQFN	RHL	20	3000	330.0	12.4	3.71	4.71	1.1	8.0	12.0	Q1
TPS40075RHLRG4	VQFN	RHL	20	3000	330.0	12.4	3.71	4.71	1.1	8.0	12.0	Q1
TPS40075RHLT	VQFN	RHL	20	250	180.0	12.4	3.71	4.71	1.1	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

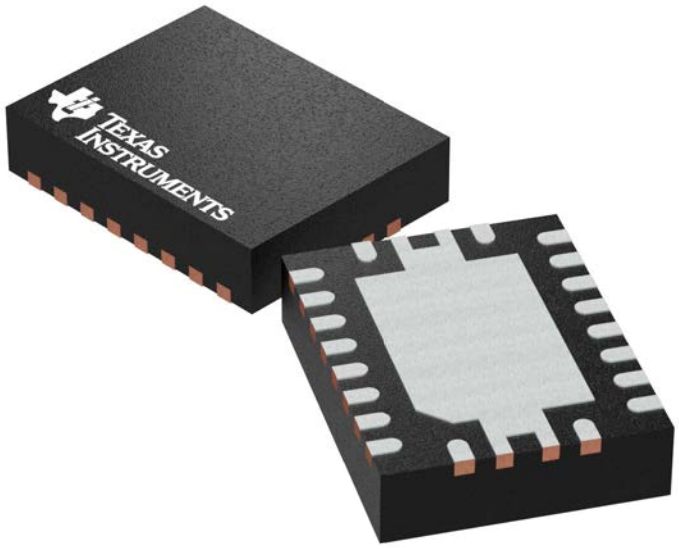
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS40075RHLR	VQFN	RHL	20	3000	353.0	353.0	32.0
TPS40075RHLRG4	VQFN	RHL	20	3000	353.0	353.0	32.0
TPS40075RHLT	VQFN	RHL	20	250	213.0	191.0	35.0

RHL 20

VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD

3.5 x 4.5 mm, 0.5 mm pitch



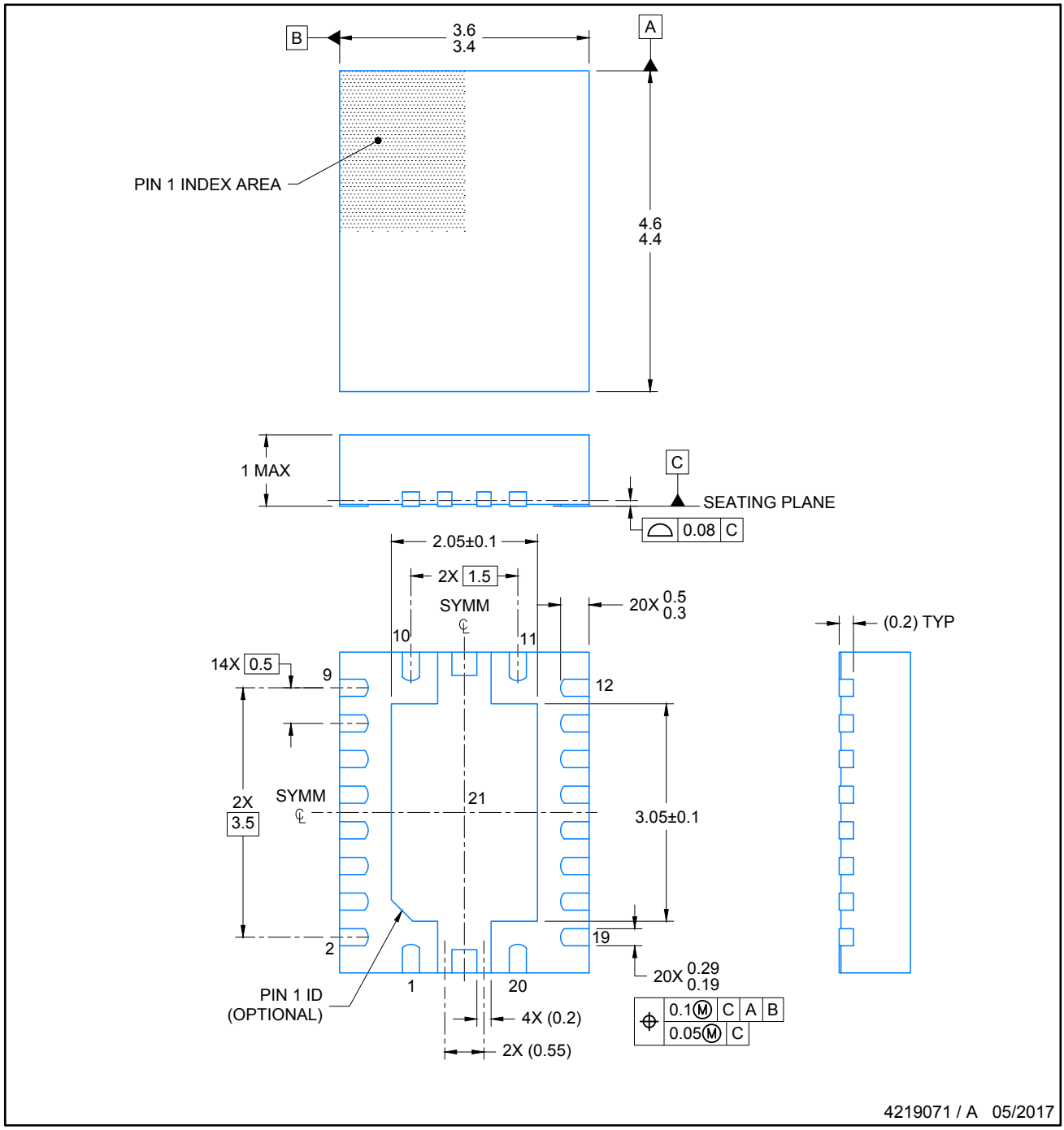
Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

PACKAGE OUTLINE

RHL0020A

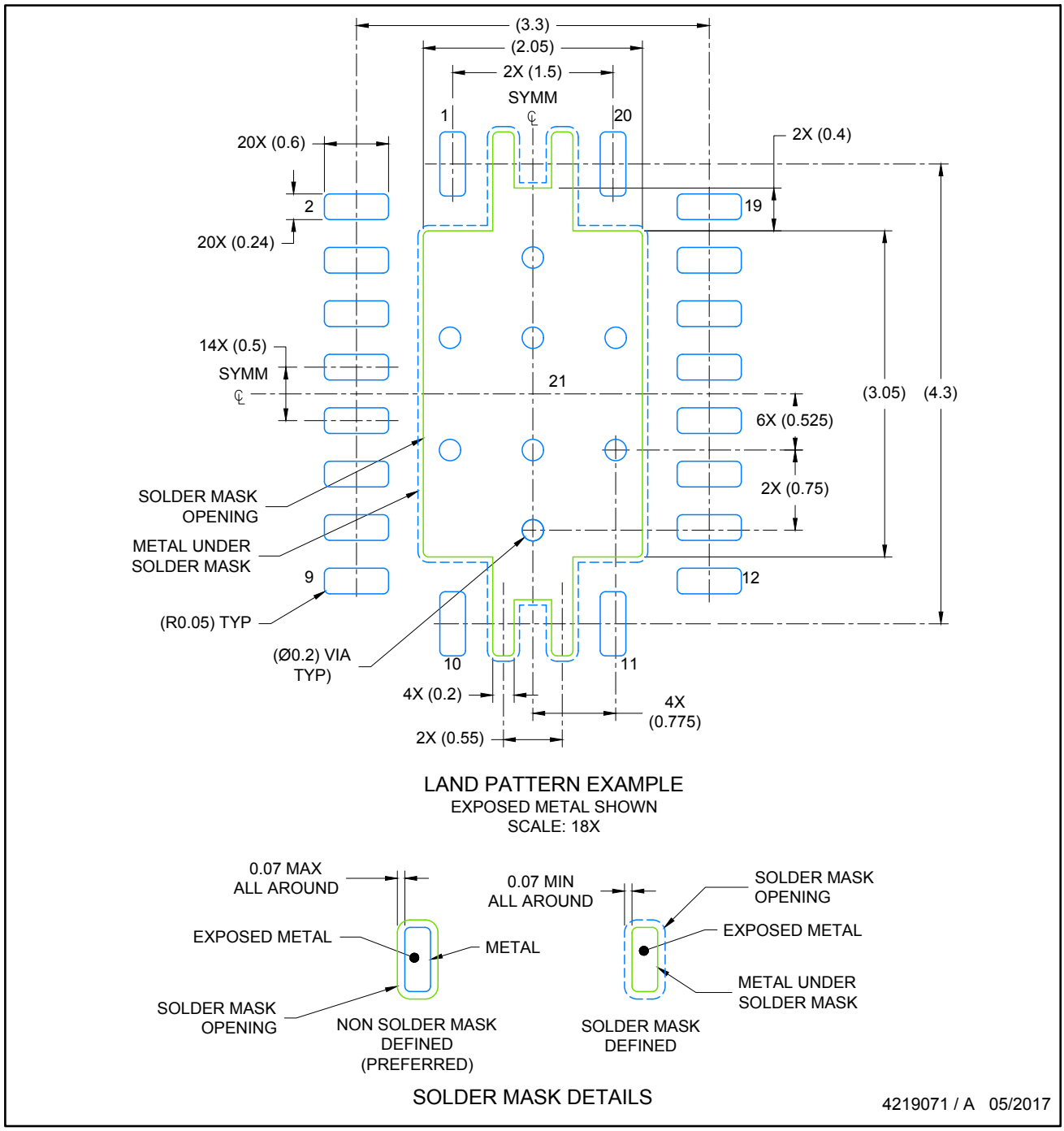
VQFN - 1 mm max height

PLASTIC QUAD FLATPACK- NO LEAD



NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.

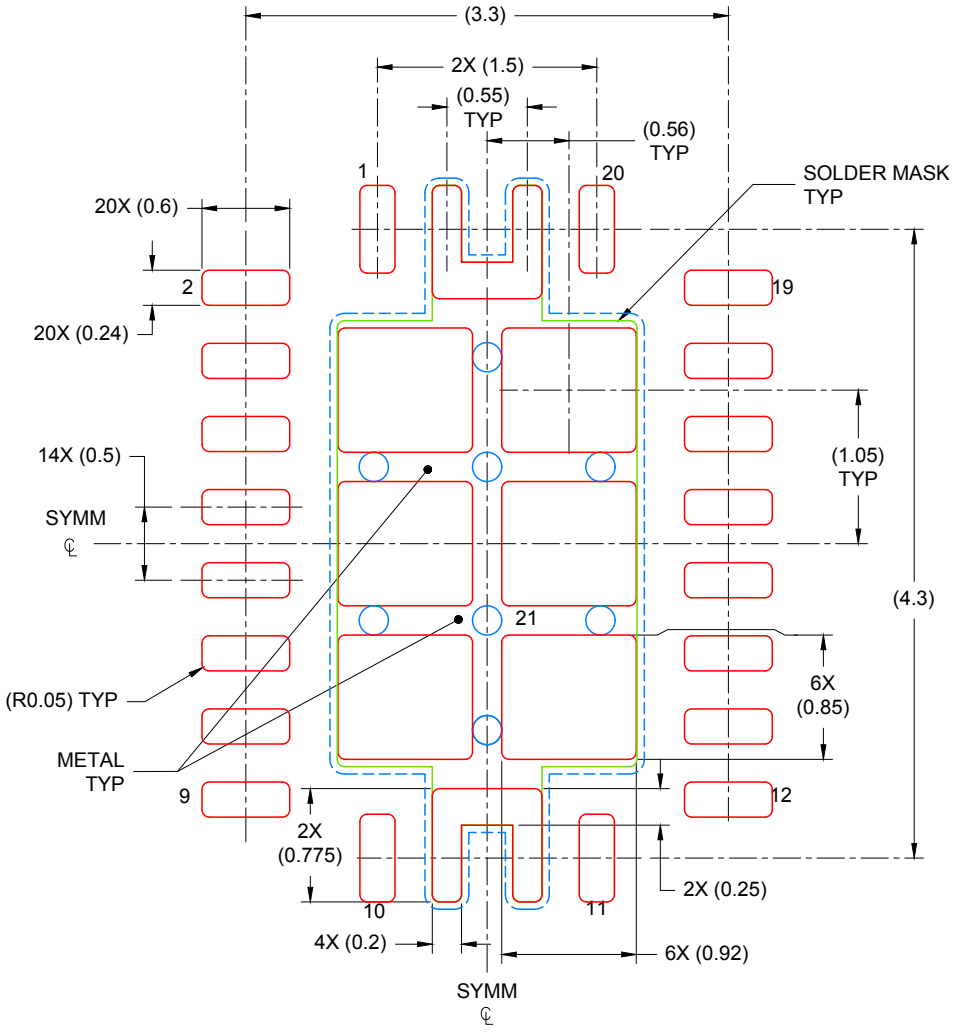


NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
6. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to theri locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.

EXAMPLE STENCIL DESIGN
VQFN - 1 mm max height

PLASTIC QUAD FLATPACK- NO LEAD



SOLDER PASTE EXAMPLE
BASED ON 0.1mm THICK STENCIL

EXPOSED PAD
75% PRINTED COVERAGE BY AREA
SCALE: 20X

4219071 / A 05/2017

NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations..

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Last updated 10/2025