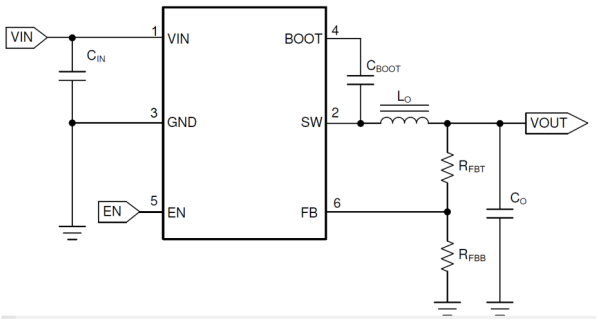
TPS543021 4.5V to 28V, 3A, EMI Friendly, Synchronous Step-Down Converter

1 Features

- Configured for a wide range of applications
  - 4.5V to 28V input voltage range
  - Up to 3A continuous output current
  - –40°C to 150°C junction temperature range
  - 70ns minimum switching on time
  - ±1% tolerance reference voltage (25°C)
  - Supports low drop out mode
  - Precision enable
- High efficiency
  - Integrated 75mΩ and 35mΩ MOSFETs
  - Low 2µA shutdown, 28µA quiescent current
  - Pulse frequency modulation (PFM) for high light load efficiency
- Ease of use
  - Peak current mode control with internal compensation
  - Fixed 400kHz switching frequency
  - Internal 5ms soft start
  - Frequency spread spectrum to reduce EMI
  - Overcurrent protection with hiccup mode
  - Non-latched protection for overtemperature protection (OTP), overcurrent protection (OCP), overvoltage protection (OVP), and undervoltage lockout (UVLO)
  - SOT-563 package
- Create a custom design using the TPS543021 with the WEBENCH® Power Designer

2 Applications

- Industry application
- Audio
- Set-top box (STB), digital television (DTV)
- Printer



TPS543021 Simplified Schematic

3 Description

The TPS543021 is a 4.5V to 28V input voltage range, 3A synchronous buck converter. The device includes two integrated switching FETs, internal loop compensation and 5ms internal soft start to reduce component count.

By integrating the MOSFETs, the TPS543021 achieves the high power density and offers a small footprint on the PCB. TPS543021 has adjustable output by a different FB resistor configuration.

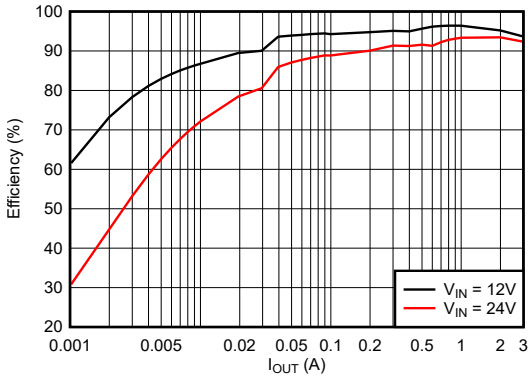
The TPS543021 operates in PFM (pulse frequency modulation) mode for high light load efficiency and reduces the power loss. The device incorporates spread spectrum for Electromagnetic Interference (EMI) reduction.

Cycle-by-cycle current limit in high-side MOSFET protects the converter in an overload condition and is enhanced by a low-side MOSFET freewheeling current limit which prevents current runaway. Hiccup mode protection is triggered if the overcurrent condition has persisted for longer than the preset time.

Package Information

PART NUMBER	PACKAGE(1)	PACKAGE SIZE(2)
TPS543021	DRL (SOT-563, 6)	1.6mm × 1.6mm

(1) For more information, see Section 10.
(2) The package size (length × width) is a nominal value and includes pins, where applicable.



5V_{OUT} Efficiency vs Output Current

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4 Pin Configuration and Functions

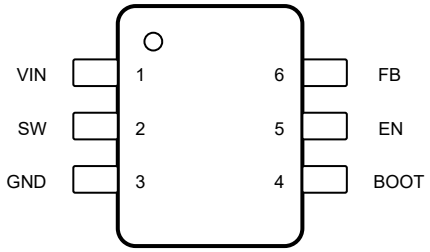


Figure 4-1. 6-Pin SOT-563, DRL Package (Top View)

Table 4-1. Pin Functions

PIN		TYPE[1]	DESCRIPTION
NAME	NO.		
VIN	1	P	Input voltage supply pin. The drain terminal of high-side FET. Connect to the input supply and input bypass capacitors C_{IN}. Input bypass capacitors must be directly connected to this pin and GND.
SW	2	P	Switch node connection between high-side NFET and low-side NFET.
GND	3	G	Ground pin. Source terminal of low-side power NFET as well as the ground terminal for controller circuit. The path to C_{IN} must be as short as possible.
BOOT	4	P	Supply input for the high-side NFET gate drive circuit. Connect a high quality 0.1µF capacitor between BOOT and SW pins.
EN	5	A	This pin is the enable pin. Float the EN pin to enable. Precision enable input allows an adjustable UVLO by an external resistor divider.
FB	6	A	Converter feedback input. Connect to output voltage with feedback resistor divider. Never short this terminal to ground during operation.

(1) A = Analog, P = Power, G = Ground

5 Specifications

5.1 Absolute Maximum Ratings

Over the recommended operating junction temperature range of –40°C to +150°C (unless otherwise noted)(1)

		MIN	MAX	UNIT
Pin voltage	VIN to GND	–0.3	30	V
	SW to GND	–0.3	30	V
	SW to GND less than 10ns transients	–3.5	33	V
	BOOT to SW	–0.3	6	V
	EN to GND	–0.3	7	V
	FB to GND	–0.3	6	V
Operating junction temperature, T_J		–40	150	°C
Storage temperature, T_{stg}		–65	150	°C

(1) Operation outside the Absolute Maximum Ratings may cause permanent device damage. Absolute Maximum Ratings do not imply functional operation of the device at these or any other conditions beyond those listed under Recommended Operating Conditions. If used outside the Recommended Operating Conditions but within the Absolute Maximum Ratings, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.

5.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±2500	V
		Charged device model (CDM), per ANSI/ESDA/ JEDEC JS-002(2)	±1500	

(1) JEDEC document JEP155 states that 500V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250V CDM allows safe manufacturing with a standard ESD control process.

5.3 Recommended Operating Conditions

Over the recommended operating junction temperature range of –40°C to +150°C (unless otherwise noted)(1)

		MIN	MAX	UNIT
V_{IN}	VIN to GND	4.5	28	V
I_{OUT}	Output current	0	3	A
SW	SW to GND	–0.1	28	V
EN	EN to GND	–0.1	6	V
FB	FB to GND	–0.1	5	V
T_J	Operating junction temperature	–40	150	°C

(1) Recommended operating conditionsindicate conditions for which the device is intended to be functional, but do not specify specific performance limits. For specified specifications, see Electrical Characteristics table.

5.4 Thermal Information

THERMAL METRIC(1)		TPS543021 DRL (SOT563) 6 Pins	UNIT
$R_{\theta JA}$ (2)	Junction-to-ambient thermal resistance	131.2	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	52.3	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	23.1	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	2.39	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	21.5	°C/W

5.4 Thermal Information (continued)

THERMAL METRIC[1]		TPS543021 DRL (SOT563) 6 Pins	UNIT
$R_{\theta JA(effective)}$	Junction-to-ambient thermal resistance with TI EVM	64.2	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application note.
(2) The value of $R_{\theta JA}$ given in this table is only valid for comparison with other packages and can not be used for design purposes. These values were simulated on a standard JEDEC board. These values do not represent the performance obtained in an actual application.

5.5 Electrical Characteristics

Limits apply over operating junction temperature (T_J) range of –40°C to +150°C, unless otherwise stated. Minimum and Maximum limits are specified through test, design or statistical correlation. Typical values represent the most likely parametric norm at T_J = 25°C, V_{IN} = 12V, and are provided for reference purposes only. Unless otherwise stated, the following conditions apply: V_{IN} = 4.5V to 28V.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
SUPPLY						
$I_{Q(VIN)}$	VIN quiescent current	Non-switching, V_{IN} = 12V, V_{EN} = 5V, V_{FB} = 1V		28		µA
$I_{SD(VIN)}$	VIN shutdown supply current	V_{IN} = 12V, V_{EN} = 0V		2		µA
UVLO						
$V_{UVLO(R)}$	V_{IN} UVLO rising threshold	V_{IN} rising	3.8	4.1	4.4	V
$V_{UVLO(F)}$	V_{IN} UVLO falling threshold	V_{IN} falling	3.3	3.6	3.9	V
$V_{UVLO(H)}$	V_{IN} UVLO hysteresis		400	480	560	mV
ENABLE						
$V_{EN(R)}$	EN voltage rising threshold	EN rising, enable switching		1.23	1.28	V
$V_{EN(F)}$	EN voltage falling threshold	EN falling, disable switching	1.1	1.16		V
$I_{EN(P)}$	EN pin sourcing current	V_{EN} = 1.0V		0.7		µA
$I_{EN(H)}$	EN pin sourcing current hysteresis	V_{EN} = 1.5V		1.55		µA
REFERENCE VOLTAGE						
V_{FB}	FB voltage	T_J = 25°C	590	596	602	V
V_{FB}	FB voltage	T_J = –40°C to 150°C	582	596	610	V
$I_{FB(LKG)}$	FB input leakage current	V_{IN} = 12V, V_{FB} = 0.6V			0.15	µA
SWITCHING FREQUENCY						
f_{SW}	Centre switching frequency, CCM operation	V_{IN} = 12V	295	400	505	kHz
F_{Dither} (1)	Switching frequency dithering range	Frequency dithering over center frequency		±6%		
POWER STAGE						
$R_{DSON(HS)}$	High-side MOSFET On-resistance	$V_{BOOT-SW}$ = 5V		70		mΩ
$R_{DSON(LS)}$	Low-side MOSFET On-resistance	V_{IN} = 12V		35		mΩ
$t_{ON(min)}$ (1)	Minimum ON pulse width	V_{IN} = 12V, I_{OUT} = 1A		70		ns
$t_{ON(max)}$ (1)	Maximum ON pulse width	V_{IN} = 5V		62		µs
CURRENT LIMITS AND HICCUP						
$I_{HS(OC)}$	High-side peak current limit	Peak current limit on HS MOSFET	4	5	6	A
$I_{LS(OC)}$	Low-side valley current limit	Valley current limit on LS MOSFET	3.1	4	5.5	A
I_{PK_MIN} (1)	Minimum Peak Inductor Current			0.75		A

5.5 Electrical Characteristics (continued)

Limits apply over operating junction temperature (T_J) range of –40°C to +150°C, unless otherwise stated. Minimum and Maximum limits are specified through test, design or statistical correlation. Typical values represent the most likely parametric norm at T_J = 25°C, V_{IN} = 12V, and are provided for reference purposes only. Unless otherwise stated, the following conditions apply: V_{IN} = 4.5V to 28V.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{OC_HICCUP} (1)	Time between current-limit hiccup burst			40		ms
OUTPUT OVP						
V_{OV}	Overvoltage-protection (OVP) threshold voltage	V_{FB} rising		108		%
V_{OV_HYS}	Overvoltage-protection (OVP) hysteresis			4		%
STARTUP						
t_{SS}	Internal fixed soft-start time	From 10% to 90% of target V_{OUT}		5		ms
THERMAL SHUTDOWN						
$T_{J(SD)}$ (1)	Thermal shutdown threshold			160		°C
$T_{J(HYS)}$ (1)	Thermal shutdown hysteresis			10		°C
t_{OT_HICCUP} (1)	Time between over temperature hiccup burst			80		ms

(1) Not production tested. Specified by correlation by design.

5.6 Typical Characteristics

V_{IN} = 12V, T_A = 25°C, unless otherwise specified.

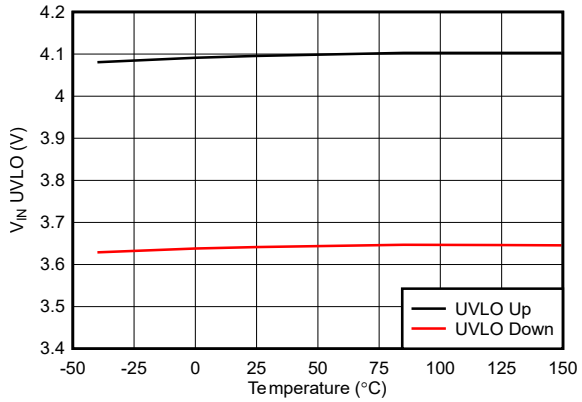


Figure 5-1. V_{IN} UVLO Threshold

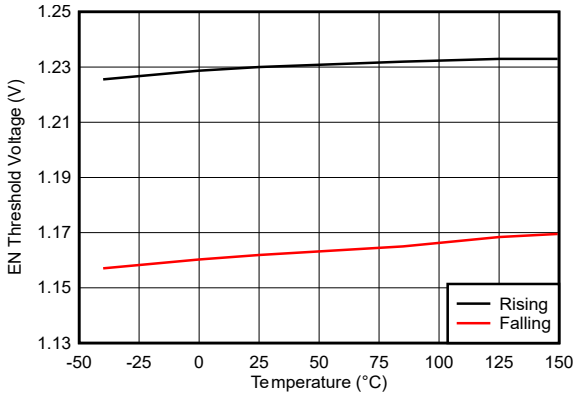


Figure 5-2. EN Threshold

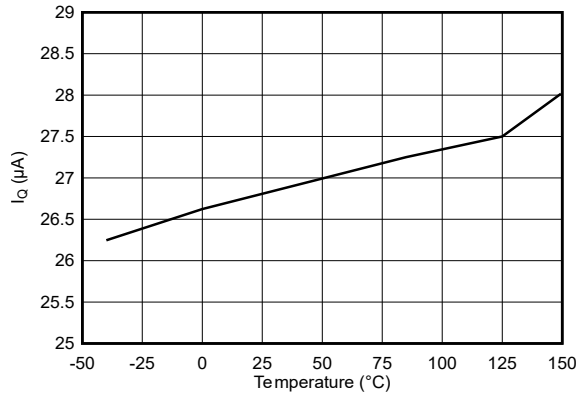


Figure 5-3. Non-Switching I_Q

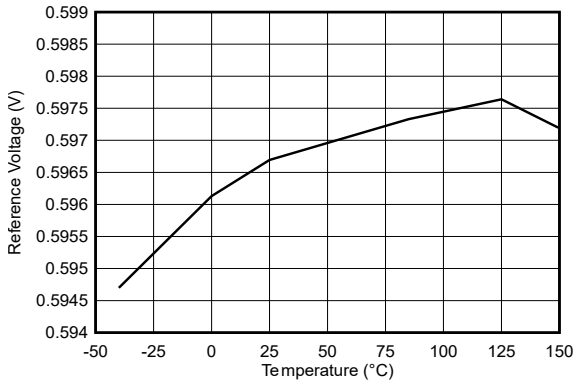


Figure 5-4. Reference Voltage

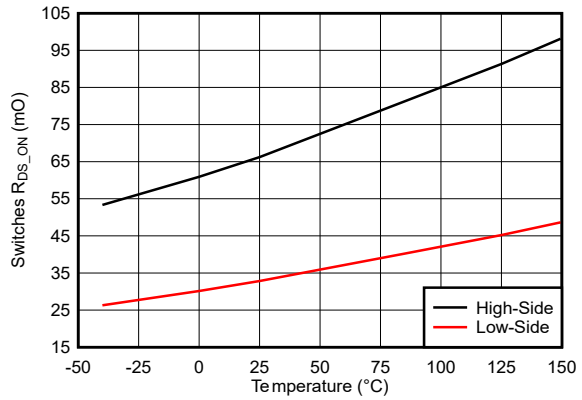


Figure 5-5. High-Side and Low-Side Switches R_{DS_ON}

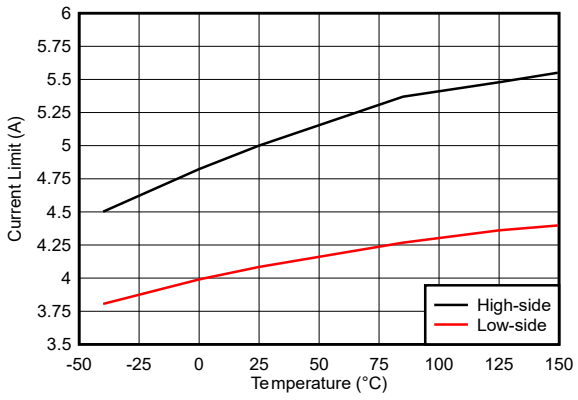


Figure 5-6. High-Side and Low-Side Current Limit

6 Detailed Description

6.1 Overview

The TPS543021 device is a 28V, 3A, synchronous step-down (buck) converter with two integrated N-channel MOSFETs. To improve performance during line and load transients the device implements a constant-frequency, peak current mode control which reduces output capacitance. The optimized internal compensation network minimizes the external component counts and simplifies the control loop design.

The device begins switching at V_{IN} is 4.5V or higher. The operating current is 28µA typically when not switching and under no load. When the device is disabled, the supply current is 2µA typically.

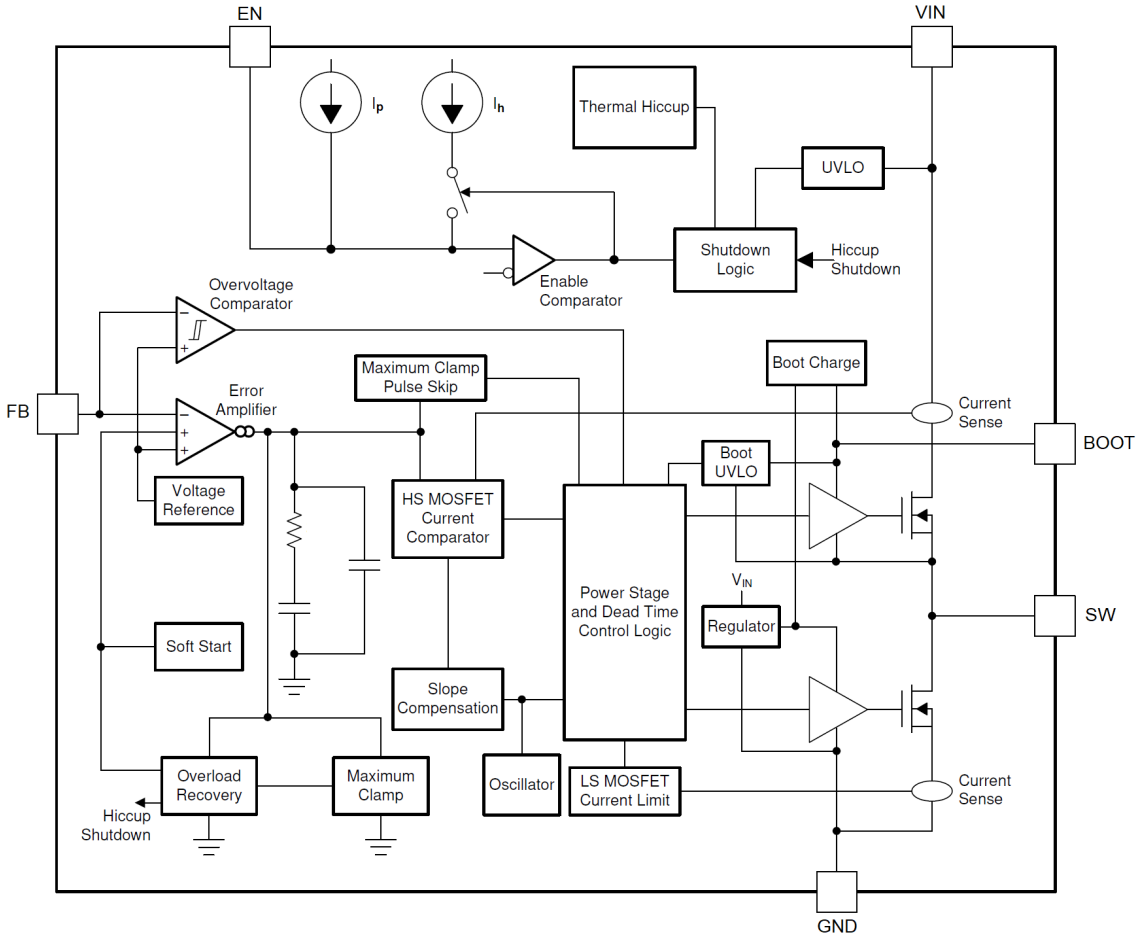
The integrated 70mΩ high-side MOSFET and 35mΩ low-side MOSFET allow for high efficiency power supply designs with continuous output currents up to 3A.

The device reduces the external component count by integrating the boot recharge diode. The bias voltage for the integrated high-side MOSFET is supplied by an external capacitor on the BOOT to SW pins. The boot capacitor voltage is monitored by an UVLO circuit and turns the high-side MOSFET off when the voltage falls below a preset threshold of 2.4V typically.

The device minimizes excessive output overvoltage transients by taking advantage of the overvoltage comparator. When the regulated output voltage is greater than 108% of the nominal voltage, the overvoltage comparator is activated, and the high-side MOSFET is turned off and masked from turning on till the output voltage is lower than 104%.

The device has internal 5ms soft-start time to minimize inrush currents.

6.2 Functional Block Diagram



6.3 Feature Description

6.3.1 Fixed-Frequency PWM Control

The device uses a fixed-frequency, peak current-mode control. The output voltage sensed through external resistors on the FB pin and compared to an internal voltage reference by an error amplifier. An internal oscillator initiates the turn on of the high-side power switch. The error amplifier output is compared to the current of the high-side power switch. When the power-switch current reaches the error amplifier output voltage level, the high side power switch is turned off and the low-side power switch is turned on. The device implements a current-limit by clamping the error amplifier voltage to a maximum level and also implements a minimum clamp for improved transient-response performance.

6.3.2 Light Load Operation

The TPS543021 is designed to operate in pulse frequency modulation (PFM) mode at light load condition to maintain high efficiency operation. When either the minimum high-side switch ON time t_{ON-MIN} or the minimum peak inductor current I_{PEAK_MIN} (typically 750mA) is reached, the switching frequency decreases to maintain regulation. In PFM mode, switching frequency is decreased by the control loop to maintain output voltage regulation when load current reduces. Switching loss is further reduced in PFM operation due to a significant drop in effective switching frequency. Because the integrated current comparator catches the peak inductor current only, the average load current entering pulse frequency mode varies with the applications and external output filters.

6.3.3 Error Amplifier

The device has a transconductance amplifier as the error amplifier. The error amplifier compares the FB voltage to the lower one of the internal soft-start voltage or the internal 0.596V voltage reference. The frequency compensation components are placed internally between the output of the error amplifier and ground.

6.3.4 Slope Compensation and Output Current

The device adds a compensating ramp to the signal of the switch current. This slope compensation prevents sub-harmonic oscillations as the duty cycle increases. The available peak inductor current remains constant over the full duty-cycle range.

6.3.5 Enable and Adjusting Undervoltage Lockout

The EN pin provides electrical on and off control of the device. When the EN pin voltage exceeds the rising threshold voltage, the device begins operation. If the EN pin voltage is pulled below the falling threshold voltage, the regulator stops switching and enters shutdown mode with low quiescent current.

The EN pin has an internal pullup-current source, which allows the user to float the EN pin to enable the device. If an application requires control of the EN pin, use open-drain or open-collector output logic to interface with the pin.

The device implements internal undervoltage-lockout (UVLO) circuitry on the VIN pin. The device is disabled when the VIN pin voltage falls below the internal V_{IN} UVLO threshold. The internal V_{IN} UVLO threshold has a hysteresis of 480mV.

If an application requires a higher UVLO threshold (V_{START} and V_{STOP}) on the VIN pin, then the EN pin can be configured as shown in Figure 6-1. When using the external UVLO function, TI recommends setting the hysteresis at a value greater than 500mV, and EN pin voltage never exceeds 7V at maximum V_{IN} voltage.

The EN pin has a small pullup current, I_p, which sets the default state of the pin to enable when no external components are connected. The pullup current is also used to control the voltage hysteresis for the UVLO function because the pullup current increases by I_h when the EN pin crosses the enable threshold. Use Equation 1 and Equation 2 to calculate the values of R1 and R2 for a specified UVLO threshold.

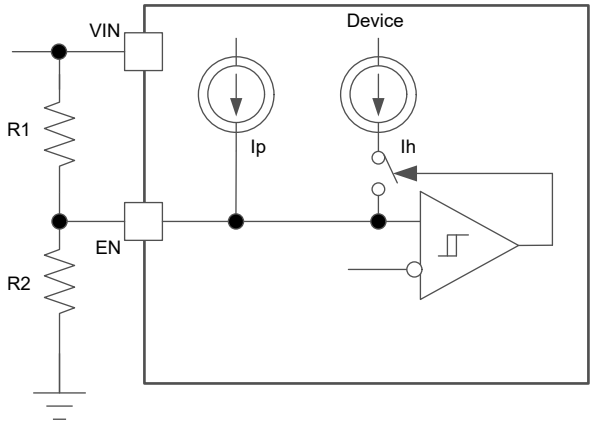


Figure 6-1. Adjustable V_{IN} Undervoltage Lockout

$$R_1 = \frac{\frac{V_{EN(F)}}{V_{EN(R)}} \times V_{START} - V_{STOP}}{I_p \times \left(1 - \frac{V_{EN(F)}}{V_{EN(R)}}\right) + I_h} \quad (1)$$

$$R_2 = \frac{R_1 \times V_{EN(F)}}{V_{STOP} - V_{EN(F)} + \left(I_h + I_p\right) \times R_1} \quad (2)$$

Where:

- I_p = 0.7µA
- I_h = 1.55µA
- $V_{EN(F)}$ = 1.16V
- $V_{EN(R)}$ = 1.23V

6.3.6 Safe Start-Up into Prebiased Outputs

The device has been designed to prevent the low-side MOSFET from discharging a prebiased output. During monotonic prebiased start-up, both high-side and low-side MOSFETs are not allowed to be turned on until the internal soft-start voltage is higher than the FB pin voltage.

6.3.7 Voltage Reference

The voltage reference system produces a precise voltage-reference overtemperature by scaling the output of a temperature stable band-gap circuit. The typical voltage reference is designed at 0.596V.

6.3.8 Adjustable Output Voltage

A precision 0.596V reference voltage (V_{REF}) is used to maintain a tightly regulated output voltage over the entire operating temperature range. The output voltage is set by a resistor divider from V_{OUT} to the FB pin. TI recommends to use 1% tolerance resistors with a low temperature coefficient for the FB divider. Select the bottom-side resistor, R_{FBB}, for the desired divider current and use Equation 3 to calculate the top-side resistor, R_{FBT}. The recommended range for R_{FBT} is 10kΩ to 100kΩ. A lower R_{FBT} value can be used if pre-loading is desired to reduce the V_{OUT} offset in PFM operation. Lower R_{FBT} values reduce efficiency at very light load. Less static current goes through a larger R_{FBT} value and can be more desirable when light-load efficiency is critical. However, TI does not recommend R_{FBT} values larger than 1MΩ because R_{FBT} values larger than 1MΩ make the feedback path more susceptible to noise. Larger R_{FBT} values require a more carefully designed feedback path trace from the feedback resistors to the feedback pin of the device. The tolerance and temperature variation of the resistor divider network affect the output voltage regulation.

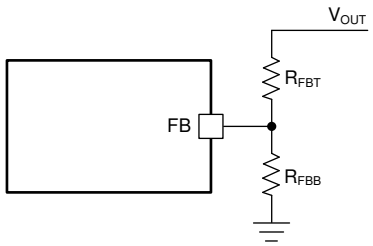


Figure 6-2. Output Voltage Setting

$$R_{FBT} = \frac{(V_{OUT} - V_{REF})}{V_{REF}} \times R_{FBB} \quad (3)$$

6.3.9 Internal Soft Start

The TPS543021 uses the internal soft-start function. The internal soft-start time is set to 5ms typically.

6.3.10 Bootstrap Voltage (BOOT)

The TPS543021 has an integrated boot regulator and requires a 0.1µF ceramic capacitor between the BOOT and SW pins to provide the gate drive voltage for the high-side MOSFET. TI recommends a ceramic capacitor with an X7R or X5R grade dielectric because of the stable characteristics over temperature and voltage. To improve drop out, the device is designed to operate at 100% duty cycle as long as the maximum high-side switch ON time t_{ON-MAX} is reached and BOOT to SW pin voltage is greater than 2.4V typically.

6.3.11 Overcurrent Protection

The device is protected from overcurrent conditions by cycle-by-cycle current limiting on both the high-side MOSFET and the low-side MOSFET.

6.3.11.1 High-Side MOSFET Overcurrent Protection

The device implements current mode control which uses the internal COMP voltage to control the turn off of the high-side MOSFET and the turn on of the low-side MOSFET on a cycle-by-cycle basis. During each cycle, the switch current and the current reference generated by the internal COMP voltage are compared. When the peak switch current intersects the current reference, the high-side switch turns off.

6.3.11.2 Low-Side MOSFET Overcurrent Protection

While the low-side MOSFET is turned on, the conduction current is monitored by the internal circuitry. During normal operation, the low-side MOSFET sources current to the load. At the end of every clock cycle, the low-side MOSFET sourcing current is compared to the internally set low-side sourcing current-limit. If the inductor valley current is exceeded the low-side source current limit $I_{LS(OC)}$, the high-side MOSFET does not turn on and the low-side MOSFET stays on for the next cycle. The high-side MOSFET turns on again when the inductor valley current is below the low-side sourcing current-limit at the start of a cycle. If the current of the low-side switch triggers $I_{LS(OC)}$ for 512 consecutive cycles and hiccup current protection mode is activated, the device shuts down and restarts after the hiccup time of 40ms. The hiccup mode helps to reduce the device power dissipation under severe overcurrent conditions.

6.3.12 Spread Spectrum

TPS543021 introduces frequency spread spectrum to reduce EMI. The modulation frequency is 1/512 of center switching frequency. The dithering range is ±6% over center frequency.

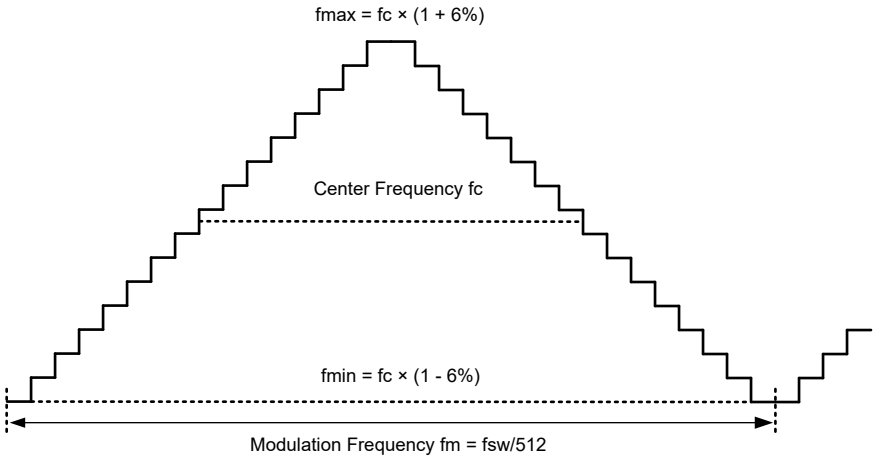


Figure 6-3. Frequency Spread Spectrum Diagram

6.3.13 Output Overvoltage Protection (OVP)

The TPS543021 incorporates an overvoltage protection (OVP) circuit to minimize output voltage overshoot when recovering from output fault conditions or strong unload transients. The OVP circuit includes an overvoltage comparator to compare the FB pin voltage with internal thresholds. When the FB pin voltage goes above 108% × Vref, the high-side MOSFET is forced off. When the FB pin voltage falls below 104% × Vref, the high-side MOSFET enables again.

6.3.14 Thermal Shutdown

The internal thermal-shutdown circuitry forces the device to stop switching if the junction temperature exceeds 160°C typically. When the junction temperature drops below 150°C typically, the internal thermal-hiccup timer begins to count. The device re-initiates the power-up sequence after the thermal hiccup time (t_{OT_HICCUP}) 80ms is over.

6.4 Device Functional Modes

6.4.1 Normal Operation

When the input voltage is above the UVLO threshold, the TPS543021 can operate in the normal switching modes. Normal continuous conduction mode (CCM) occurs when inductor peak current is above 0A. In CCM, the device operates at a fixed frequency.

6.4.2 PFM Mode Operation

The devices are designed to operate in high-efficiency PFM mode under light load conditions. During light load operation, pulse frequency modulation (PFM) mode activates to maintain high efficiency operation. When either the minimum high-side switch ON time t_{ON-MIN} or the minimum peak inductor current I_{PEAK_MIN} (typically 750mA) is reached, the switching frequency decreases to maintain regulation. In PFM mode, switching frequency is decreased by the control loop to maintain output voltage regulation when load current reduces. Switching loss is further reduced in PFM operation due to a significant drop in effective switching frequency.

7 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

7.1 Application Information

The TPS543021 is a step-down DC-to-DC converter to convert a higher input voltage to a lower output DC voltage with a maximum output current of 3A. The following design procedure can be used to select components for the TPS543021. Alternately, the WEBENCH circuit design and selection simulation services software can be used to generate complete designs. When generating a design, the WEBENCH circuit design and selection simulation services software uses iterative design procedure and accesses comprehensive databases of components. See also ti.com.

7.2 Typical Application

7.2.1 TPS543021 6V to 28V Input, 5V Output Converter

The TPS543021 only requires a few external components to convert from a wide voltage range supply to a fixed output voltage. The following figure shows a basic schematic.

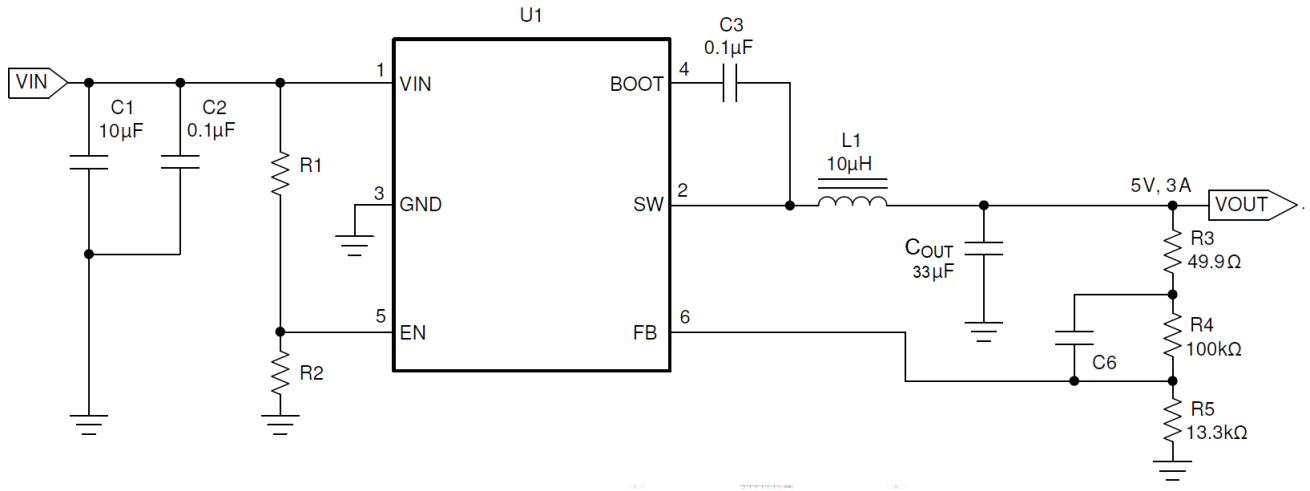


Figure 7-1. 5V, 3A Reference Design

The external components must fulfill the needs of the application and the stability criteria of the control loop of the device. Use Table 7-1 to simplify the output filter component selection.

Table 7-1. Typical External Component Values for 3A Output Current

V_{OUT} (V)	L (µH)	C_{OUT} (µF)(1)	R4 (kΩ)	R5 (kΩ)	C6 (pF)
1.8	4.7	80	100	49.9	47
2.5	5.6	60	100	31.6	47
3.3	6.8	44	100	22.1	56
5	10	30	100	13.3	75

(1) Ceramic capacitor is used in this table. All the C_{OUT} values are after derating.

7.2.2 Design Requirements

For this design example, use the parameters in the following table.

Table 7-2. Design Parameters

PARAMETER	VALUE
Input voltage range	6V to 28V
Output voltage	5V
Output current	3A
Output overshoot, undershoot (1.5A to 3A)	5%
Output voltage ripple	0.5%
Switching frequency	400kHz

7.2.3 Detailed Design Procedure

7.2.3.1 Custom Design With WEBENCH® Tools

Click here to create a custom design using the TPS543021 device with the WEBENCH® Power Designer.

1. Start by entering the input voltage (V_{IN}), output voltage (V_{OUT}), and output current (I_{OUT}) requirements.
2. Optimize the design for key parameters such as efficiency, footprint, and cost using the optimizer dial.
3. Compare the generated design with other possible solutions from Texas Instruments.

The WEBENCH Power Designer provides a customized schematic along with a list of materials with real-time pricing and component availability.

In most cases, these actions are available:

- Run electrical simulations to see important waveforms and circuit performance
- Run thermal simulations to understand board thermal performance
- Export customized schematic and layout into popular CAD formats
- Print PDF reports for the design, and share the design with colleagues

Get more information about WEBENCH tools at www.ti.com/WEBENCH.

7.2.3.2 Output Voltage Setpoint

The output voltage of the TPS543021 device is externally adjustable using a resistor divider network. The divider network is comprised of R4 and R5. Use the following equations to calculate the relationship of the output voltage to the resistor divider.

$$R_5 = \frac{R_4 \times V_{ref}}{V_{OUT} - V_{ref}} \tag{4}$$

$$V_{OUT} = V_{ref} \times \left(\frac{R_4}{R_5} + 1\right) \tag{5}$$

Select a value of R4 to be approximately 100kΩ. Slightly increasing or decreasing R5 can result in closer output voltage matching when using standard value resistors. In this design, R4 = 100kΩ and R5 = 13.3kΩ, which results in a 5V output voltage. The 49.9Ω resistor, R3, is optional for loop stability testing.

7.2.3.3 Input Capacitor Selection

The device requires an input decoupling capacitor, and a bulk capacitor is needed depending on the application. TI recommends a ceramic capacitor over 10µF for the decoupling capacitor. An additional 0.1µF capacitor (C2) from VIN to GND is required for high frequency filtering. The capacitor voltage rating must be greater than the maximum input voltage.

Use the following equation to calculate the input ripple voltage (ΔV_{IN}).

$$\Delta V_{IN} = \frac{I_{OUT(MAX)} \times 0.25}{C_{BULK} \times f_{SW}} + I_{OUT(MAX)} \times ESR_{MAX} \quad (6)$$

where:

- C_{BULK} is the bulk capacitor value
- f_{SW} is the switching frequency
- $I_{OUT(MAX)}$ is the maximum loading current
- ESR_{MAX} is maximum series resistance of the bulk capacitor

The maximum RMS (root mean square) ripple current must also be checked. For worst case conditions, use Equation 7 to calculate $I_{CIN(RMS)}$.

$$I_{CIN(RMS)} = \frac{I_{OUT(MAX)}}{2} \quad (7)$$

The actual input-voltage ripple is greatly affected by parasitic associated with the layout and the output impedance of the voltage source. *Design Requirements* shows the actual input voltage ripple for this circuit, which is larger than the calculated value. The maximum voltage across the input capacitors is VIN (MAX) + ΔVIN/2. The selected bypass capacitor is rated for 50V and the ripple current capacity is greater than 2A. Both values provide ample margin. The maximum ratings for voltage and current must not be exceeded under any circumstance.

7.2.3.4 Bootstrap Capacitor Selection

A 0.1µF ceramic capacitor must be connected between the BOOT to SW pin for proper operation. TI recommends to use a ceramic capacitor rated at 16V or higher. The bootstrap capacitor must be a high-quality ceramic type with X7R or X5R grade dielectric for temperature stability.

7.2.3.5 Undervoltage Lockout Setpoint

The undervoltage lockout (UVLO) setpoint can be adjusted using the external voltage divider network of R1 and R2. R1 is connected between the VIN and EN pins of the TPS543021 device. R2 is connected between the EN and GND pins. The UVLO has two thresholds, one for power up when the input voltage is rising and one for power down or brown outs when the input voltage is falling. Use Equation 1 and Equation 2 to calculate the values for the upper and lower resistor values of R1 and R2.

7.2.3.6 Output Filter Components

Two components must be selected for the output filter, the output inductor (L_O) and C_O.

7.2.3.6.1 Inductor Selection

Use the following equation to calculate the minimum value of the output inductor (L_{MIN}).

$$L_{MIN} = \frac{V_{OUT} \times \left(V_{IN(MAX)} - V_{OUT}\right)}{V_{IN(MAX)} \times K_{IND} \times I_{OUT} \times f_{SW}} \quad (8)$$

Where:

K_{IND} is a coefficient that represents the amount of inductor ripple current relative to the maximum output current.

In general, the value of K_{IND} is at the discretion of the designer; however, the following guidelines can be used. For designs using low-ESR output capacitors, such as ceramics, a reasonable value of K_{IND} must be 20% to 60% of maximum I_{OUT} supported by converter.

For this design example, use K_{IND} = 0.35. The minimum inductor value is calculated as 9.78µH. For this design, a close standard value of 10µH was selected for L_{MIN}.

For the output filter inductor, the RMS current and saturation current ratings must not be exceeded. Use the following equation to calculate the RMS inductor current ($I_{L(RMS)}$).

$$I_{L(MAX)} = \sqrt{I_{OUT(MAX)}^{2} + \frac{1}{12} \times \left(\frac{V_{OUT} \times \left(V_{IN(MAX)} - V_{OUT} \right)}{V_{IN(MAX)} \times L_O \times f_{SW} \times 0.8} \right)^2} \quad (9)$$

Use the following equation to calculate the peak inductor current ($I_{L(PK)}$).

$$I_{L(PK)} = I_{OUT(MAX)} + \frac{V_{OUT} \times \left(V_{IN(MAX)} - V_{OUT} \right)}{V_{IN(MAX)} \times L_O \times f_{SW} \times 1.6} \quad (10)$$

Smaller or larger inductor values can be used depending on the amount of ripple current the designer wants to allow so long as the other design requirements are met. Larger value inductors have lower AC current and result in lower output voltage ripple. Smaller inductor values increase AC current and output voltage ripple.

7.2.3.6.2 Output Capacitor Selection

Consider three primary factors when selecting the value of the output capacitor. The output capacitor determines the modulator pole, the output voltage ripple, and how the regulator responds to a large change in load current. The output capacitance must be selected based on the more stringent of these three criteria.

The desired response to a large change in the load current is the first criterion. The output capacitor must supply the load with current when the regulator cannot. This situation occurs if the desired hold-up times are present for the regulator. In this case, the output capacitor must hold the output voltage above a certain level for a specified amount of time after the input power is removed. The regulator is also temporarily unable to supply sufficient output current if a large, fast increase occurs affecting the current requirements of the load, such as a transition from no load to full load. The regulator usually requires four or more clock cycles for the control loop to notice the change in load current and output voltage and to adjust the duty cycle to react to the change. The output capacitor must be sized to supply the extra current to the load until the control loop responds to the load change. The output capacitance must be large enough to supply the difference in current for four or more clock cycles while only allowing a tolerable amount of drop in the output voltage. Use the following equation to calculate the minimum required output capacitance.

$$C_O = \frac{2 \times \Delta I_{OUT}}{f_{SW} \times \Delta V_{OUT}} \quad (11)$$

where:

- ΔI_{OUT} is the change in output current
- f_{SW} is the switching frequency of the regulator
- $\Delta V_{(OUT)}$ is the allowable change in the output voltage

For this example, the transient load response is specified as a 5% change in the output voltage, V_{OUT}, for a load step of 1.5A. So the ΔI_{OUT} = 1.5A and ΔV_{OUT} = 0.25V. Using these values results in a minimum capacitance of 30µF. This value does not consider the ESR of the output capacitor in the output voltage change. For ceramic capacitors, the ESR is usually small enough to ignore in this calculation.

Equation 12 calculates the minimum output capacitance required to meet the output voltage ripple specification. In this case, the maximum output voltage ripple is 25mV. Under this requirement, Equation 12 yields 13.13µF.

$$C_O = \frac{1}{8 \times f_{SW}} \times \frac{1}{\frac{V_{OUTripple}}{I_{ripple}}} \quad (12)$$

where:

- f_{SW} is the switching frequency
- $V_{(OUTripple)}$ is the maximum allowable output voltage ripple
- $I_{(ripple)}$ is the inductor ripple current

Use Equation 13 to calculate the maximum ESR an output capacitor can have to meet the output-voltage ripple specification. Equation 13 indicates the ESR must be less than 23.8mΩ. In this case, the ESR of the ceramic capacitor is much smaller than 23.8mΩ.

$$R_{ESR} < \frac{V_{OUTripple}}{I_{ripple}} \tag{13}$$

Additional capacitance deratings for aging, temperature, and DC bias must be considered, which increases this minimum value. For this example, three 10uF 16V, X7R ceramic capacitors are used, two 22uF 10V, X7R ceramic capacitors also can used if the total effective capacitance larger than 30uF at $5V_{OUT}$ bias. Capacitors generally have limits to the amount of ripple current the capacitors can handle without failing or producing excess heat. An output capacitor that can support the inductor ripple current must be specified. Some capacitor data sheets specify the RMS value of the maximum ripple current. Use Equation 14 to calculate the RMS ripple current that the output capacitor must support.

$$I_{COUT(RMS)} = \frac{1}{\sqrt{12}} \times \left(\frac{V_{OUT} \times \left(V_{IN(MAX)} - V_{OUT}\right)}{V_{IN(MAX)} \times L_O \times f_{SW} \times N_C} \right) \tag{14}$$

7.2.3.6.3 Feedforward Capacitor

In some cases, a feedforward capacitor can be used across R_{FBT} to improve the load transient response or improve the loop phase margin. This statement is especially true when values of R_{FBT} > 100kΩ are used. Large values of R_{FBT} in combination with the parasitic capacitance at the FB pin can create a small signal pole that interferes with the loop stability. A C_{FF} (C6 in this example) helps mitigate this effect. Use lower values to determine if any advantage is gained by the use of a C_{FF} capacitor.

The Application Report *Optimizing Transient Response of Internally Compensated DC-DC Converters with Feedforward Capacitor* application note is helpful when experimenting with a feedforward capacitor.

7.2.4 Application Curves

Unless otherwise specified the following conditions apply: V_{IN} = 24V, V_{OUT} = 5V, L = 10µH, C_{OUT} = 30µF, T_A = 25°C.

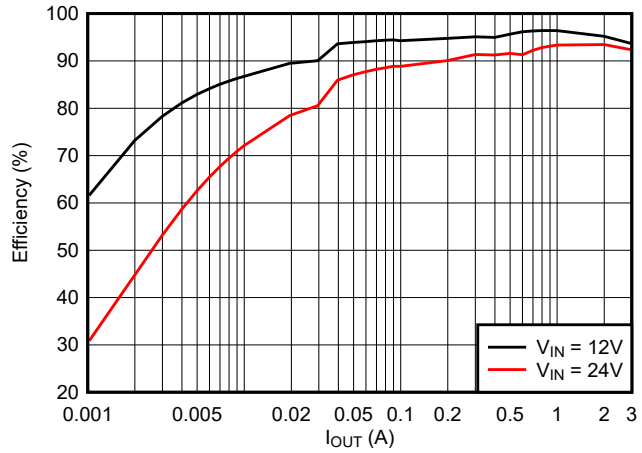


Figure 7-2. 5V_{OUT} Efficiency

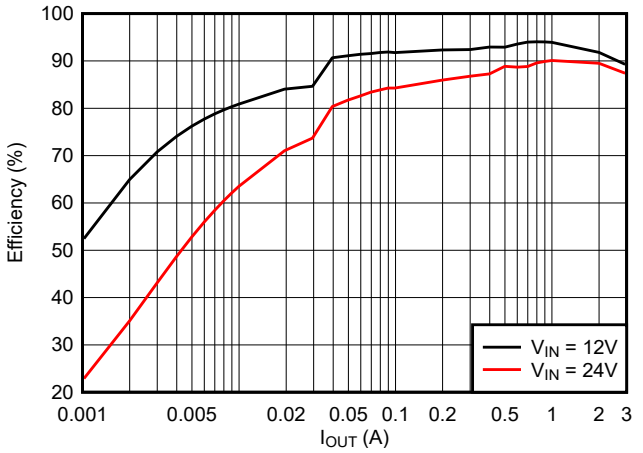


Figure 7-3. 3.3V_{OUT} Efficiency

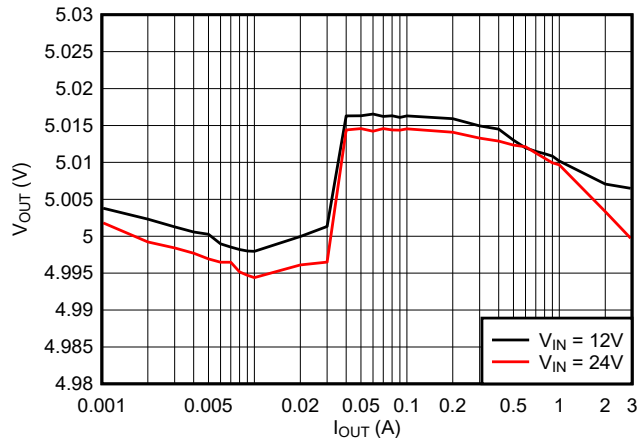


Figure 7-4. Load Regulation

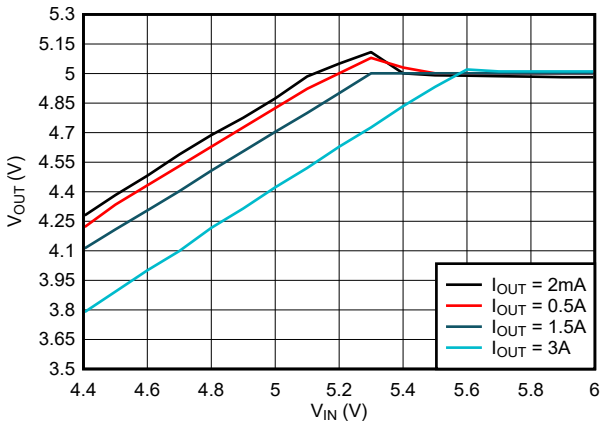


Figure 7-5. Drop Out

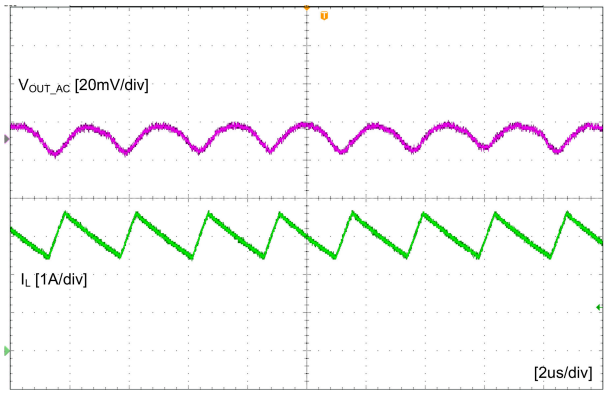


Figure 7-6. Output Voltage Ripple, I_{OUT} = 3A

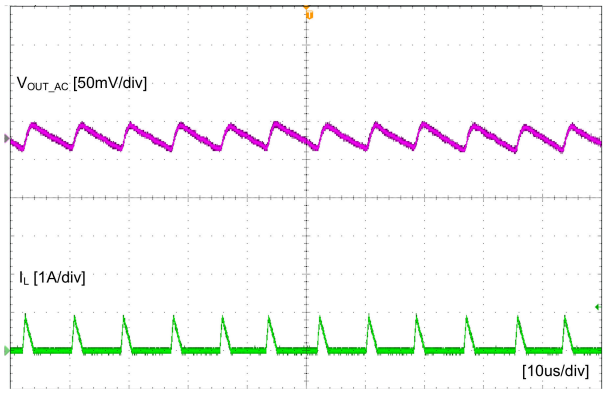


Figure 7-7. Output Voltage Ripple, I_{OUT} = 0.1A

7.2.4 Application Curves (continued)

Unless otherwise specified the following conditions apply: V_{IN} = 24V, V_{OUT} = 5V, L = 10µH, C_{OUT} = 30µF, T_A = 25°C.

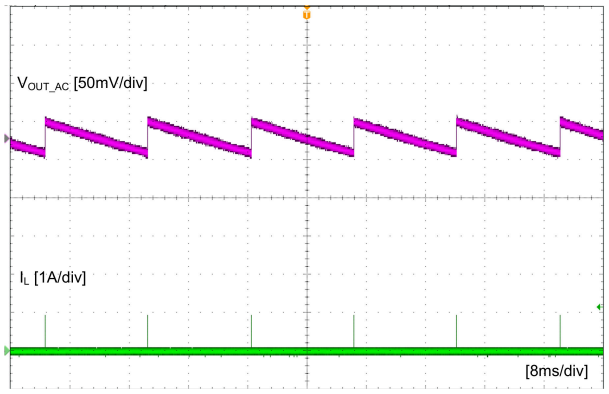


Figure 7-8. Output Voltage Ripple, I_{OUT} = 0A

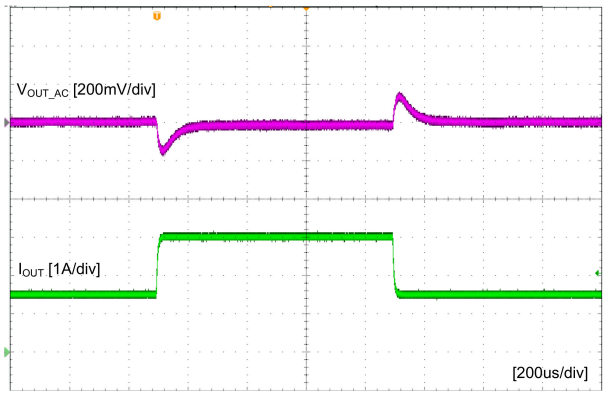


Figure 7-9. Load Transient Response, 1.5A to 3A Load Step

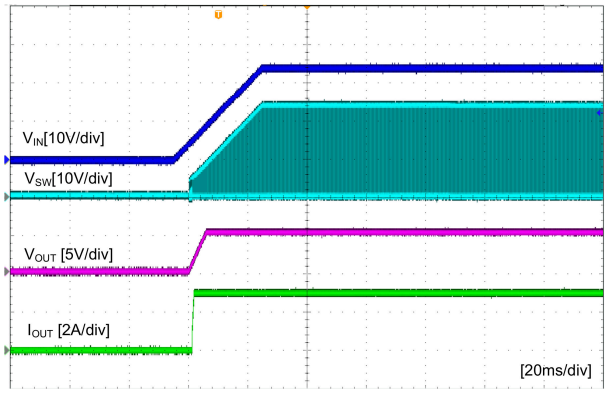


Figure 7-10. Start-Up by V_{IN}

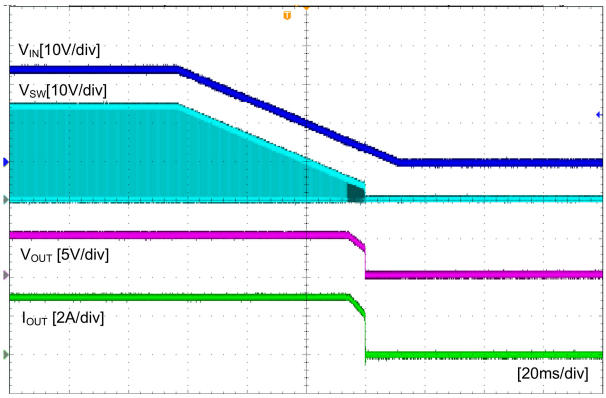


Figure 7-11. Shutdown by V_{IN}

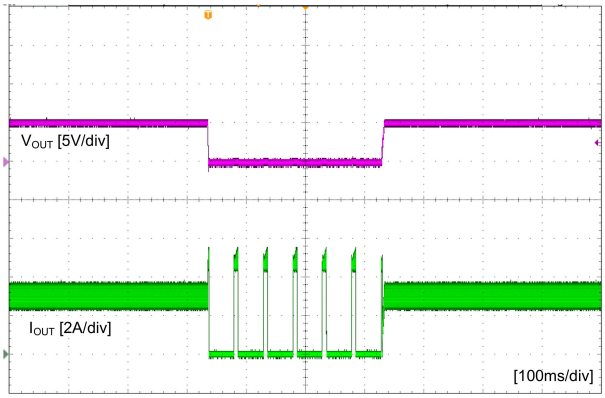


Figure 7-12. Load Transient Response, 0.2A to 1.8A Load Step

7.3 Power Supply Recommendations

The devices are designed to operate from an input voltage supply range between 4.5V and 28V. This input supply must be well regulated. If the input supply is located more than a few inches from the device or converter, additional bulk capacitance can be required in addition to the ceramic bypass capacitors. An electrolytic capacitor with a value of 22µF is a typical choice.

7.4 Layout

7.4.1 Layout Guidelines

- Make VIN and GND traces as wide as possible to reduce trace impedance. The wide areas are also of advantage from the view point of heat dissipation.
- Place the input capacitor and output capacitor as close to the device as possible to minimize trace impedance.
- Provide sufficient vias for the input capacitor and output capacitor.
- Keep the SW trace as physically short and wide as practical to minimize radiated emissions.
- Do not allow switching current to flow under the device.
- Connect a separate VOUT path to the upper feedback resistor.
- Make a Kelvin connection to the GND pin for the feedback path.
- Place the voltage feedback loop away from the high-voltage switching trace, and preferably have ground shield.
- Make the trace of the VFB node as small as possible to avoid noise coupling.
- Make the GND trace between the output capacitor and the GND pin as wide as possible to minimize the trace impedance.

7.4.2 Layout Example

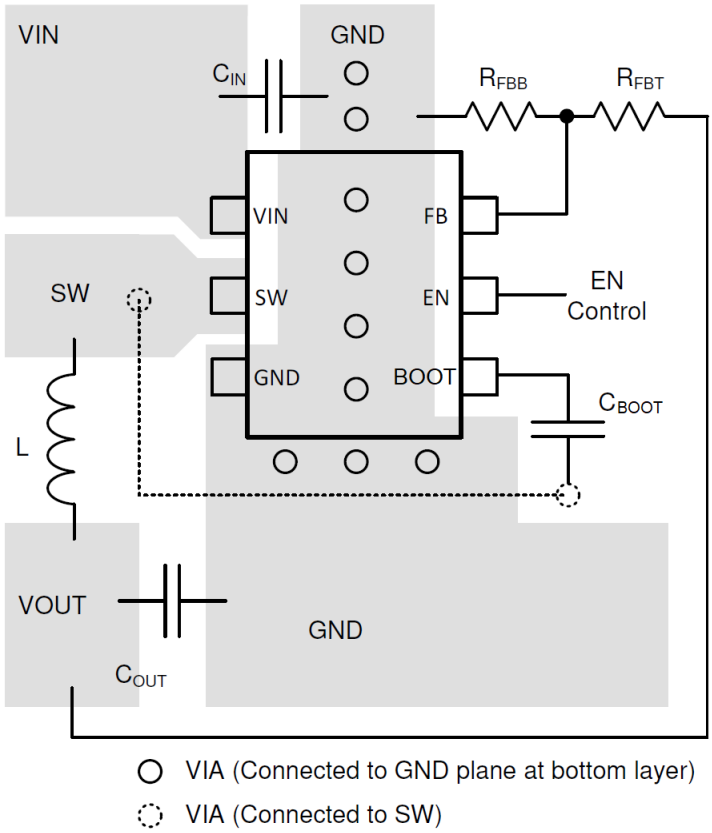


Figure 7-13. Board Layout

8 Device and Documentation Support

8.1 Device Support

8.1.1 Third-Party Products Disclaimer

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8.1.2 Development Support

8.1.2.1 Custom Design With WEBENCH® Tools

Click here to create a custom design using the TPS543021 device with the WEBENCH® Power Designer.

1. Start by entering the input voltage (V_{IN}), output voltage (V_{OUT}), and output current (I_{OUT}) requirements.
2. Optimize the design for key parameters such as efficiency, footprint, and cost using the optimizer dial.
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- Run thermal simulations to understand board thermal performance
- Export customized schematic and layout into popular CAD formats
- Print PDF reports for the design, and share the design with colleagues

Get more information about WEBENCH tools at www.ti.com/WEBENCH.

8.2 Documentation Support

8.2.1 Related Documentation

For related documentation, see the following:

Texas Instruments, *Optimizing Transient Response of Internally Compensated DC-DC Converters with Feedforward Capacitor* application note

8.3 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

8.4 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

8.5 Trademarks

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WEBENCH® is a registered trademark of Texas Instruments.
All trademarks are the property of their respective owners.

8.6 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

8.7 Glossary

TI Glossary This glossary lists and explains terms, acronyms, and definitions.

9 Revision History

Changes from Revision * (July 2025) to Revision A (September 2025)	Page
• Changed document status from Advance Information to Production Data	1

10 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
PTPS543021DRLR	Active	Preproduction	SOT-5X3 (DRL) | 6	4000 | LARGE T&R	-	Call TI	Call TI	-40 to 150	
TPS543021DRLR	Active	Production	SOT-5X3 (DRL) | 6	4000 | LARGE T&R	-	SN	Level-1-260C-UNLIM	-40 to 150	3021

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

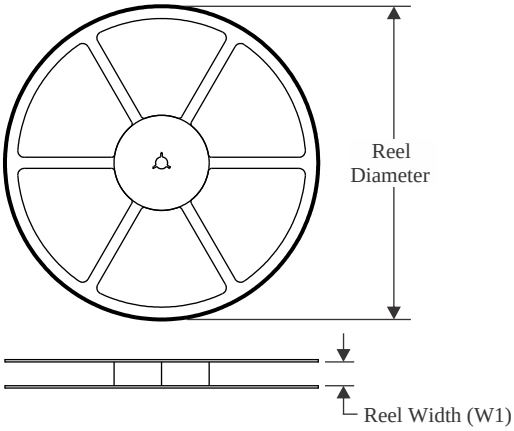
(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

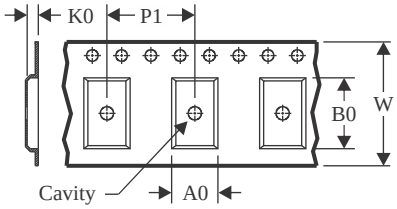
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

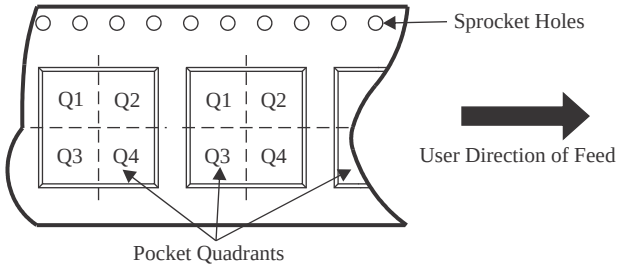


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

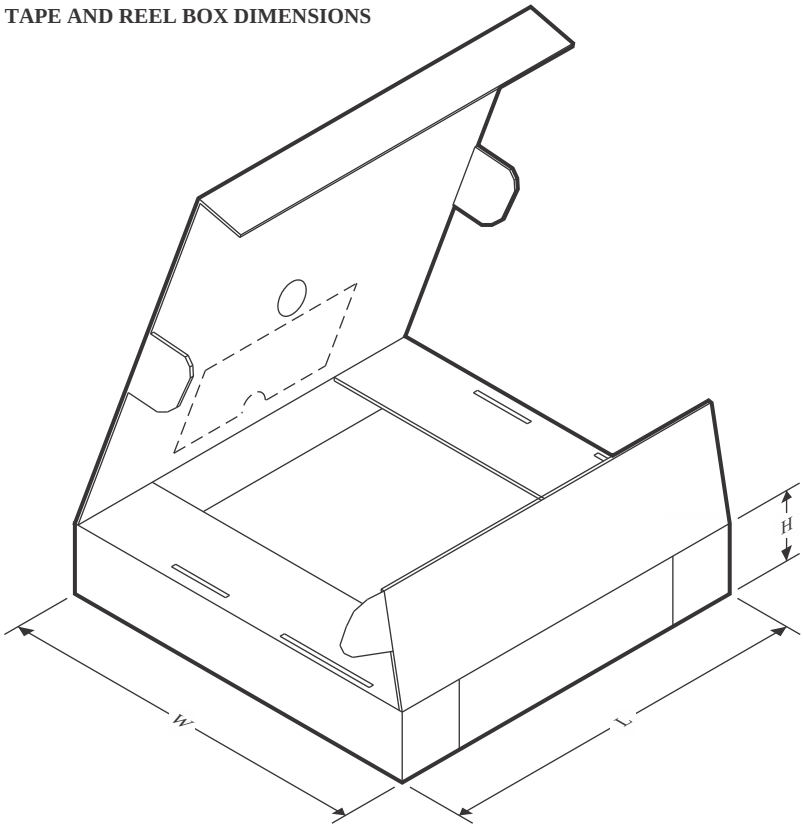
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS543021DRLR	SOT-5X3	DRL	6	4000	180.0	8.4	1.8	1.8	0.75	4.0	8.0	Q3

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

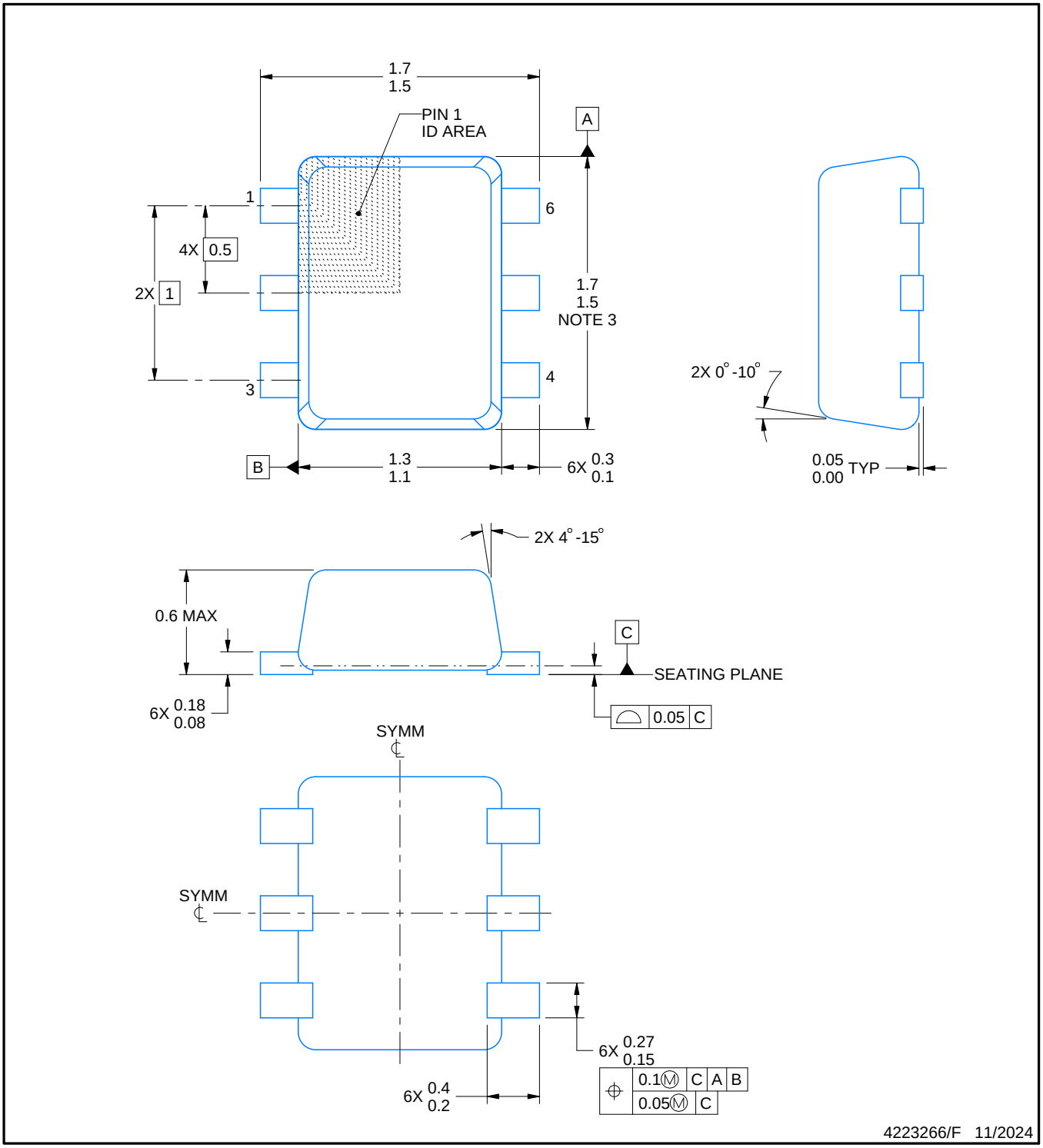
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS543021DRLR	SOT-5X3	DRL	6	4000	210.0	185.0	35.0

PACKAGE OUTLINE

DRL0006A

SOT - 0.6 mm max height

PLASTIC SMALL OUTLINE



NOTES:

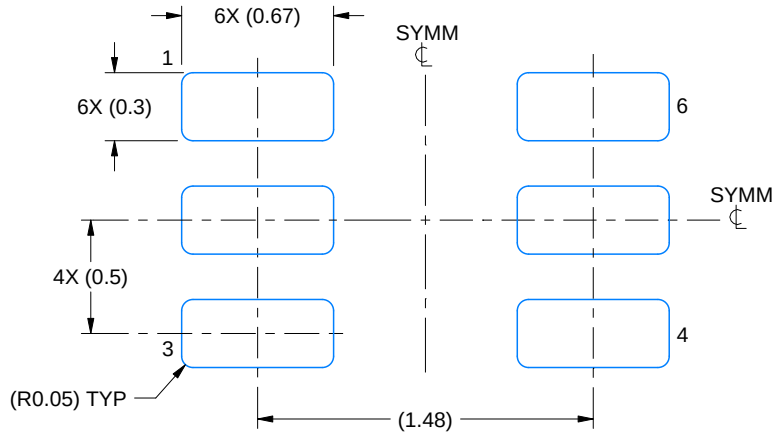
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. Reference JEDEC registration MO-293 Variation UAAD

EXAMPLE BOARD LAYOUT

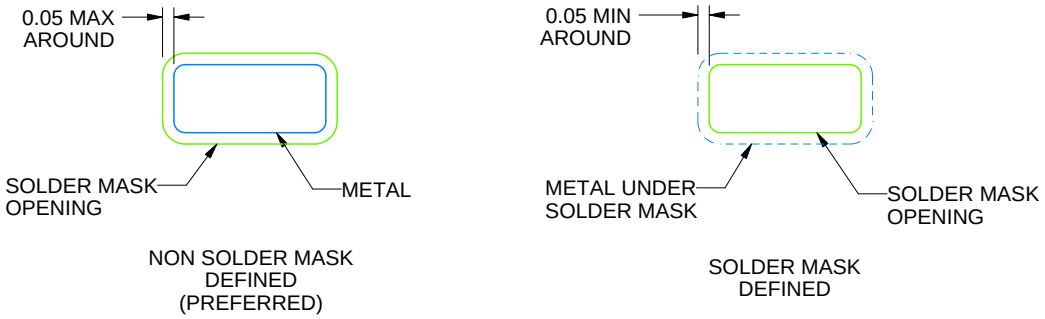
DRL0006A

SOT - 0.6 mm max height

PLASTIC SMALL OUTLINE



LAND PATTERN EXAMPLE
SCALE:30X



SOLDERMASK DETAILS

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NOTES: (continued)

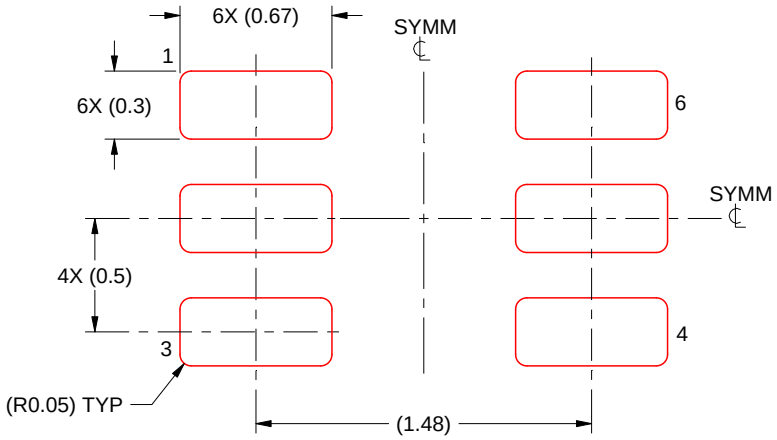
5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
7. Land pattern design aligns to IPC-610, Bottom Termination Component (BTC) solder joint inspection criteria.

EXAMPLE STENCIL DESIGN

DRL0006A

SOT - 0.6 mm max height

PLASTIC SMALL OUTLINE



SOLDER PASTE EXAMPLE
BASED ON 0.1 mm THICK STENCIL
SCALE:30X

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NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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