TPS544B27W 4V to 18V Input, 20A Buck Converter With PMBus® and Telemetry

1 Features

- PMBus® 1.5 interface with NVM for configuration, telemetry (V/I/T), and fault reporting
- Input voltage: 4V to 18V
- Output voltage: 0.25V to 5.5V
- Supports external 5V bias improving efficiency and enabling 2.7V minimum input voltage
- Output current: 20A continuous and 35A peak
- Cycle-by-cycle valley I_{OUT} OCF limit programmable up to 35A
- Input power monitoring (PIN sense)
- Programmable DCM or FCCM operation
- Switching frequency: 400kHz to 2MHz
- Programmable internal loop compensation including droop (DC load line)
- Programmable soft-start time from 0.5ms to 16ms
- Programmable soft-stop time from 0.5ms to 4ms
- Programmable output voltage slew rate: 0.625mV/µs to 25mV/µs
- Programmable V_{IN} UVLO, V_{OUT} OVF/UVF, and OTF
- Safe start-up into prebiased outputs
- Precision voltage reference and differential remote sense for high output accuracy
  - ±0.5% tolerance from 0°C to 85°C junction
  - ±1% tolerance from –40°C to 125°C junction
- Analog output current output pin (IMON)
- D-CAP+™ control topology with fast transient response
- Open-drain power-good output (VRRDY)

2 Applications

- Server and cloud-computing POLs
- Hardware accelerator
- Network interface card
- Broadband, networking, and optical
- Wireless infrastructure

3 Description

The TPS544B27W device is a highly-integrated buck converter with D-CAP+ control topology for fast transient response. All programmable parameters can be configured by the PMBus interface and stored in non-volatile memory (NVM) as the new default values to minimize the external component count. These features make the device well-designed for space-constrained applications.

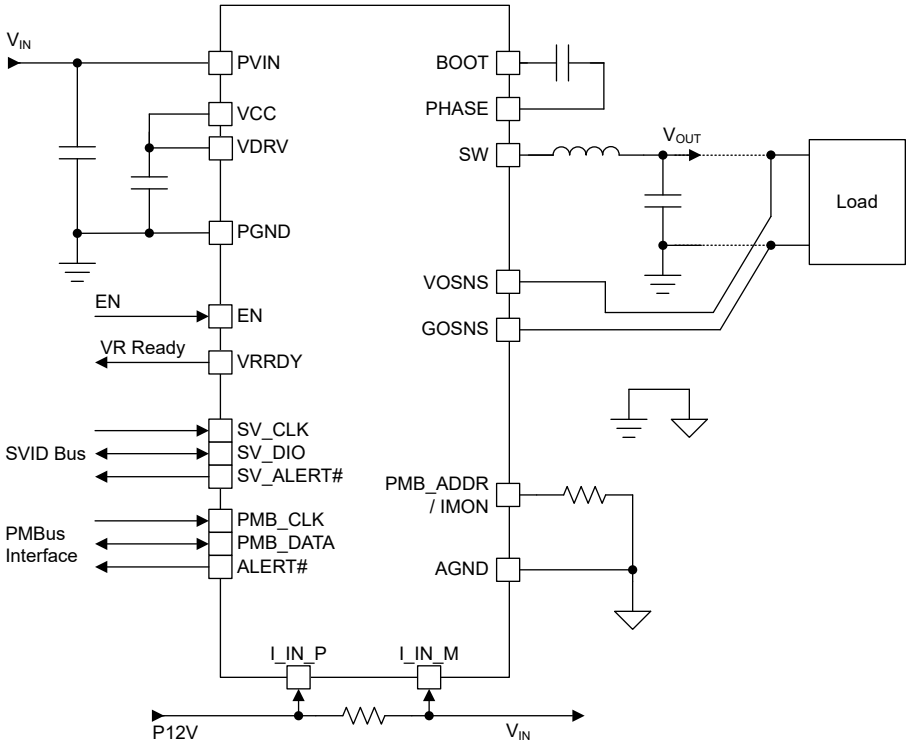
Fault management and status reports for the overcurrent fault (OCF), V_{OUT} overvoltage fault (OVF), undervoltage fault (UVF), and overtemperature fault are provided on the device. The TPS544B27W device provides a full set of telemetry, including output voltage, output current, and device temperature. Additionally, input power monitoring through an external sensing resistor is provided for board-level power management.

TPS544B27W is a lead-free device and is RoHS compliant without exemption.

Package Information

PART NUMBER	PACKAGE(1)	PACKAGE SIZE(2)
TPS544B27W	VBD (WQFN-FCRLF, 33)	5.00mm × 4.00mm

(1) For more information, see Section 11.
(2) The package size (length × width) is a nominal value and includes pins, where applicable.



Simplified Schematic

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4 Pin Configuration and Functions

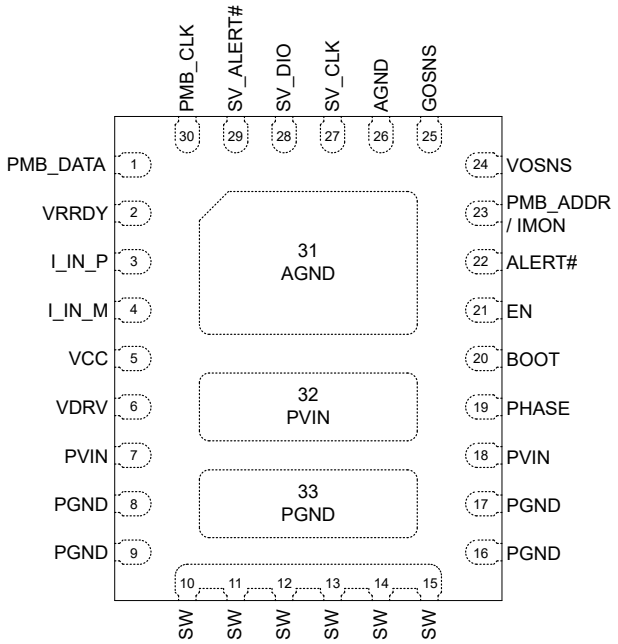


Figure 4-1. 33-Pin VBD, WQFN-FCRLF Package (Top View)

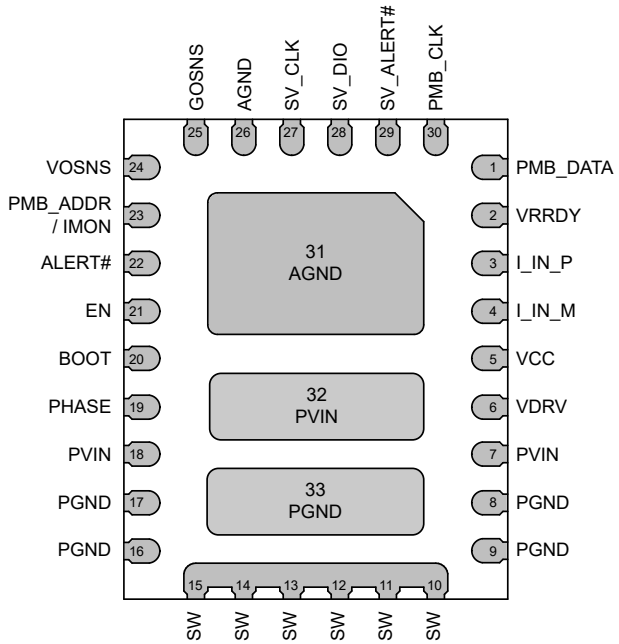


Figure 4-2. 33-Pin VBD, WQFN-FCRLF Package (Bottom View)

Table 4-1. Pin Functions

PIN		TYPE[1]	DESCRIPTION
NAME	NO.		
AGND	26	G	Ground pin, reference point for internal control circuitry
AGND	31	G	Thermal pad internally tied to AGND. Connect this pad to board ground on PCB layout to enhance the thermal performance.
BOOT	20	P	Supply rail for the high-side gate driver (boost terminal). Connect the bootstrap capacitor from this pin to the PHASE pin. A high temperature (X7R) 0.1µF or greater value ceramic capacitor is recommended.
EN	21	I	Enable pin, an active-high input pin that, when asserted high, causes the VR to begin soft-start sequence for the output voltage rail. When de-asserted low, the VR de-asserts VRRDY and begins the shutdown sequence of the output voltage rail and continue to completion.
GOSNS	25	I	Negative input of the differential remote sense circuit, connect to the ground sense point on the load side
I_IN_M	4	I	Negative input of the differential input current sense. Connect to PVIN side of input current sense resistor. If input current sense not used, connect directly to I_IN_P and PVIN.
I_IN_P	3	I	Positive Input of the differential input current sense. Connect to the input side of input current sense resistor. If input current sense not used, connect directly to I_IN_M and PVIN.
PGND	8 – 9, 16 – 17	G	Power ground for the internal power stage
PGND	33	G	Thermal pad internally tied to PGND. Connect this pad to board ground on PCB layout to enhance the thermal performance.
PHASE	19	O	Return for high-side MOSFET driver. Shorted to SW internally. Connect the BOOT pin bypass capacitor to this pin.

Table 4-1. Pin Functions (continued)

PIN		TYPE[1]	DESCRIPTION
NAME	NO.		
PMB_ADDR / IMON	23	I/O	Multipurpose pin. During the device initialization, the PMBus address of the controller is set by tying an external resistor between this pin and AGND. For proper resistor detection, do not load this pin with more than 20pF during the device initialization at VCC power-up. DC_LL, VBOOT, and OFFSET source 0 or 1 are selected as well. After device initialization, this pin can be used as an analog current monitor output. This pin is a current sense of low-side MOSFET. The analog IMON feature is enabled via the EN_AIMON bit in the PMBus (DAh) SVID_IMAX command. When using the IMON feature, do not load this pin with more than 50pF.
PMB_CLK	30	I	PMBus serial clock pin
PMB_DATA	1	I/O	PMBus bi-directional serial data pin
PVIN	7, 18	P	Power input for both the power stage and the analog circuit. PVIN is the input of the internal VCC LDO.
PVIN	32	P	Pad internally tied to PVIN. Connect this pad to the power input voltage in the PCB layout and use vias to connect to internal layers to reduce AC and DC parasitics in the PCB layout.
ALERT#	22	O	Multi-purpose active low open-drain pin. The functionality can be selected through the SEL_ALRT_FN field in the PMBus (D0h) SYS_CFG_USER1 command. 1. SMB_ALERT# 2. PINALRT# 3. CAT_FAULT# 4. VR_HOT#
SV_ALERT#	29	O	SVID active low ALERT# signal. This output is asserted to indicate the status of the VR has changed.
SV_CLK	27	I	SVID clock pin
SV_DIO	28	I/O	SVID bi-directional data pin
SW	10 – 15	O	Output switching terminal of the power converter. Connect these pins to the output inductor.
VCC	5	I	Internal LDO output and bias for internal circuitry. Connect to VDRV or power from same external 5V bias. Bypass to AGND with minimum 1.0µF, 10V ceramic capacitor
VDRV	6	P	Input for gate driver circuit. Connect to VCC for internal bias. An external 5V bias can be connected to this pin to save the power losses on the internal LDO.
VOSNS	24	I	Positive input of the differential remote sense circuit, connect to the Vout sense point on the load side
VRRDY	2	O	Voltage regulator “Ready” output signal. The VRRDY indicator is asserted when the controller is ready to accept SVID commands after EN is asserted. VRRDY is also be de-asserted low when a shutdown fault occurs. This open-drain output requires an external pullup resistor.

(1) I = Input, O = Output, I/O = Input or Output, G = Ground, P = Power.

5 Specifications

5.1 Absolute Maximum Ratings

Over operating junction temperature range (unless otherwise noted) (1)

		MIN	MAX	UNIT
Pin voltage	PVIN	–0.3	19	V
Pin voltage	SW – PGND, DC	–0.3	19	V
Pin voltage	SW – PGND, transient < 10ns	–3	21.5	V
Pin voltage	PVIN – SW, DC	–0.3	19	V
Pin voltage	PVIN – SW, transient < 10ns	–3	25	V
Pin voltage	BOOT – PGND	–0.3	25	V
Pin voltage	BOOT – SW	–0.3	6	V
Pin voltage	I_IN_P, I_IN_M	–0.3	20	V
Pin voltage	EN, VOSNS, PMB_ADDR/IMON, VRRDY	–0.3	5.5	V
Pin voltage	PMB_CLK, PMB_DATA, ALERT#, SV_DIO, SV_CLK, SV_ALRT#	–0.3	5.5	V
Pin voltage	GOSNS – AGND	–0.3	0.3	V
Pin voltage	VCC, VDRV	–0.3	6	V
Sink current	VRRDY		10	mA
Junction temperature	T_J	–40	150	°C
Storage temperature	T_{stg}	–55	150	°C

(1) Operation outside the Absolute Maximum Ratings may cause permanent device damage. Absolute Maximum Ratings do not imply functional operation of the device at these or any other conditions beyond those listed under Recommended Operating Conditions. If used outside the Recommended Operating Conditions but within the Absolute Maximum Ratings, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.

5.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 (1)	±2000	V
		Charged-device model (CDM), per ANSI/ESDA/JEDEC JS-002 (2)	±500	

(1) JEDEC document JEP155 states that 500V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250V CDM allows safe manufacturing with a standard ESD control process.

5.3 Recommended Operating Conditions

Over operating junction temperature range (unless otherwise noted)

			MIN	NOM	MAX	UNIT
V_{OUT}	Output voltage range (programmed through SVID interface)		0.25		3.04	V
V_{OUT}	Output voltage range (programmed through PMBus interface)		0.25		5.5	V
V_{IN}	Input voltage	PVIN when VCC+VDRV is powered by the internal LDO.	4.0		18	V
		PVIN when VCC+VDRV is powered by a valid external bias	2.7		18	V
V_{BIAS}	Input voltage	VCC+VDRV external bias	4.7		5.5	V
I_{OUT}	Output current range		0		35	A
	Pin voltage	I_IN_P, I_IN_M	4		18	V
	Pin voltage	SV_CLK, SV_DIO, SV_ALERT#	–0.1		1.5	V
	Pin voltage	EN, VRRDY, PMB_ADDR/IMON, PMB_CLK, PMB_DATA, ALERT#	–0.1		5.3	V
I_{PG}	Input current capability	VRRDY			10	mA
I_{PMBUS}	Input current capability	PMB_DATA, ALERT#			20	mA
T_J	Operating junction temperature		–40		150	°C

5.4 Thermal Information

THERMAL METRIC[1]		DEVICE		UNIT
		VBD (QFN, JEDEC)	VBD (QFN, TI EVM)	
		33 PINS	33 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	30.5	17.3	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	8.8	n/a [2]	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	10.3	n/a [2]	°C/W
ψ_{JT}	Junction-to-top characterization parameter	2.9	n/a [2]	°C/W
ψ_{JB}	Junction-to-board characterization parameter	10.3	n/a [2]	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance – Power stage to PGND	5.5	n/a [2]	°C/W
	Junction-to-case (bottom) thermal resistance – Power stage to PVIN	8.7	n/a [2]	°C/W
	Junction-to-case (bottom) thermal resistance – Controller to AGND	15.3	n/a [2]	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application note.
(2) The thermal simulation setup is not applicable to a TI EVM layout.

5.5 Electrical Characteristics

T_J = –40°C to +125°C, PVIN = 4V to 18V, V_{VCC} = 4.5V to 5.0V (unless otherwise noted). Typical values are at T_J = 25°C, PVIN = 12V and V_{VCC} = 4.5V.

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
SUPPLY							
$I_{Q(PVIN)}$	PVIN quiescent current	Non-switching, PVIN = 12V, V_{EN} = 0V, no external bias on VCC/VDRV pin			10	13	mA
I_{VCC}	VCC+VDRV external bias current	5 V external bias on VCC+VDRV, regular switching, T_J = 25°C, PVIN = 12V, V_{EN} = 2V, FCCM, I_{OUT} = 0A	V_{OUT} = 0.4V, f_{SW} = 600kHz		21		mA
			V_{OUT} = 1.8V, f_{SW} = 1000kHz		30		mA
			V_{OUT} = 1.8V, f_{SW} = 1500kHz		40		mA
$I_{Q(VCC)}$	VCC+VDRV quiescent current	5V external bias on VCC+VDRV, non-switching. PVIN = 12V, V_{EN} = 0V			10		mA
INPUT UVLO AND OV							
$PVIN_{OV(RISE)}$	PVIN overvoltage threshold (55h) VIN_OV_FAULT_LIMIT	(55h) VIN_OV_FAULT_LIMIT = 16V		16.4	17.0		V
		(55h) VIN_OV_FAULT_LIMIT = 18V		18	18.5		V

5.5 Electrical Characteristics (continued)

T_J = –40°C to +125°C, PVIN = 4V to 18V, V_{VCC} = 4.5V to 5.0V (unless otherwise noted). Typical values are at T_J = 25°C, PVIN = 12V and V_{VCC} = 4.5V.

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
$PVIN_{OV(FALL)}$	PVIN overvoltage falling threshold. PVIN_OVF status bit, once it is set, cannot be cleared unless PVIN falls below this threshold.	PVIN falling			13.5		V
VIN_ON	PVIN turn-on voltage (35h) VIN_ON	PVIN rising	(35h) VIN_ON = 10V		10		V
			(35h) VIN_ON = 9V		9		V
			(35h) VIN_ON = 8V		8		V
			(35h) VIN_ON = 7V		7		V
			(35h) VIN_ON = 6V		6		V
			(35h) VIN_ON = 5V		5		V
			(35h) VIN_ON = 3V		3.8		V
			(35h) VIN_ON = 2V		2.5		V
VIN_OFF	PVIN turn-off voltage (36h) VIN_OFF	PVIN falling	(36h) VIN_OFF = 9V		9.5		V
			(36h) VIN_OFF = 8V		8.5		V
			(36h) VIN_OFF = 7V		7.5		V
			(36h) VIN_OFF = 6V		6.5		V
			(36h) VIN_OFF = 5V		5.5		V
			(36h) VIN_OFF = 4V		4.2		V
			(36h) VIN_OFF = 3V		3.6		V
			(36h) VIN_OFF = 2V		2.3		V
$T_{DGLTCH(ON)}$	VIN_ON deglitch time				50		µs
$T_{DGLTCH(OFF)}$	VIN_OFF deglitch time				5		µs
ENABLE							
$V_{EN(R)}$	EN voltage rising threshold	EN rising, enable switching			1.2	1.3	V
$V_{EN(F)}$	EN voltage falling threshold	EN falling, disable switching		0.9	1.0		V
$V_{EN(H)}$	EN voltage hysteresis				0.2		V
$t_{EN(DGLTCH)}$	EN deglitch time (1)			0.2	0.7		µs
$R_{EN(PD)}$	EN internal pulldown resistor (EN to AGND)	VEN = 2V, EN pin to AGND		110	125	140	kΩ
INTERNAL VCC LDO							
$V_{VCC(LDO)}$	Internal VCC LDO output voltage	PVIN = 4V, $I_{VCC(load)}$ = 5mA		3.925	3.97	4.0	V
		PVIN = 5V to 18V, $I_{VCC(load)}$ = 5mA		4.3	4.5	4.55	V
$V_{VCC(ON)}$	VCC UVLO rising threshold	VCC rising		3.7	3.80	3.86	V
$V_{VCC(OFF)}$	VCC UVLO falling threshold	VCC falling		3.5	3.59	3.65	V
$V_{VCC(DO)}$	VCC LDO dropout voltage	PVIN – V_{VCC}, PVIN = 4V, $I_{VCC(load)}$ = 50mA			140	250	mV
$I_{VCC(SC)}$	VCC LDO short-circuit current limit	PVIN = 12V		250	300		mA
VOUT VOLTAGE							
$V_{DAC(RNG)}$	V_{DAC} range			250		768	mV
$V_{OUT(ACC)}$	Output voltage regulation accuracy	T_J = 0°C to 85°C	V_{OUT} = 0.5V, VOSL = 0.5, V_{VOSNS}–V_{GOSNS}	0.495	0.5	0.505	V
			V_{OUT} = 0.75V, VOSL = 0.5, V_{VOSNS}–V_{GOSNS}	0.744	0.75	0.756	V
			V_{OUT} = 1.536V, VOSL = 0.5, V_{VOSNS}–V_{GOSNS}	1.52832	1.536	1.54368	V
		T_J = –40°C to 125°C	V_{OUT} = 0.5V, VOSL = 0.5, V_{VOSNS}–V_{GOSNS}	0.4925	0.5	0.5075	V
			V_{OUT} = 0.75V, VOSL = 0.5, V_{VOSNS}–V_{GOSNS}	0.7425	0.75	0.7575	V
			V_{OUT} = 1.536V, VOSL = 0.5, V_{VOSNS}–V_{GOSNS}	1.52064	1.536	1.55136	V

5.5 Electrical Characteristics (continued)

T_J = –40°C to +125°C, PVIN = 4V to 18V, V_{VCC} = 4.5V to 5.0V (unless otherwise noted). Typical values are at T_J = 25°C, PVIN = 12V and V_{VCC} = 4.5V.

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
$V_{OUT(ACC)}$	Output voltage regulation accuracy	T_J = 0°C to 85°C	V_{OUT} = 1.2V, VOSL = 0.5, V_{VOSNS}–V_{GOSNS}	1.194	1.2	1.206	V
			V_{OUT} = 1.8V, VOSL = 0.25, V_{VOSNS}–V_{GOSNS}	1.791	1.8	1.809	V
		T_J = –40°C to 125°C	V_{OUT} = 1.2V, VOSL = 0.5,V_{VOSNS}–V_{GOSNS}	1.188	1.2	1.212	V
			V_{OUT} = 1.8V, VOSL = 0.25, V_{VOSNS}–V_{GOSNS}	1.782	1.8	1.818	V
$R_{DCLL(RNG)}$	DC load line programmable range			0		3.1	mΩ
$R_{DCLL(RES)}$	DC load line programmable resolution				0.1		mΩ
I_{VOS}	VOSNS input current	VOSL = 0.25, V_{VOSNS} = 1.8V			120	130	µA
V_{OUTRES}	Resolution of VOUT_COMMAND and VOUT_TRIM				1.953		mV
VOSL	VOUT_SCALE_LOOP internal feedback loop scaling factor	Programmable range, 4 discrete settings		0.125		1	
VOUT_TRIM	Programmable range			–125		123	mV
SR_{FAST}	SVID SetVID-Fast slew rate accuracy (1)	VOUT_TRANSITION_RATE = 10mV/µs		9	10	11	mV/µs
SWITCHING FREQUENCY							
$f_{SW(FCCM)}$	Switching frequency (33h) FREQUENCY_SWITCH	PVIN = 12V, FCCM, V_{OUT} = 1.2V, I_{OUT} = 10A	(33h) FREQUENCY_SWITCH = 0x3803 (400kHz)		400		kHz
			(33h) FREQUENCY_SWITCH = 0x3805 (600kHz)	510	600	660	kHz
			(33h) FREQUENCY_SWITCH = 0x3806 (800kHz)	680	800	920	kHz
			(33h) FREQUENCY_SWITCH = 0x3808 (1000kHz)	850	1000	1150	kHz
			(33h) FREQUENCY_SWITCH = 0x3809 (1200kHz)	1020	1200	1440	kHz
			(33h) FREQUENCY_SWITCH = 0x380B (1500kHz)		1500		kHz
			(33h) FREQUENCY_SWITCH = 0x380E (1800kHz)		1700		kHz
			(33h) FREQUENCY_SWITCH = 0x380F (2000kHz)		1900		kHz
STARTUP AND SHUTDOWN TIMING							
$t_{ON(DLY)}$	Power on sequence delay, (60h) TON_DELAY	V_{VCC} = 4.5V	TON_DELAY = 0ms		0.05	0.1	ms
			TON_DELAY = 0.5ms		0.5	0.55	ms
			TON_DELAY = 1.0ms		1.0	1.1	ms
			TON_DELAY = 2.0ms		2.0	2.2	ms
$t_{ON(Rise)}$	Soft-start time, (61h) TON_RISE	V_{VCC} = 4.5V	TON_RISE = 0.5ms		0.5	0.575	ms
			TON_RISE = 1.0ms		1.0	1.15	ms
			TON_RISE = 2.0ms		2.0	2.3	ms
			TON_RISE = 4.0ms		4.0	4.6	ms
			TON_RISE = 8.0ms		8.0	9.2	ms
			TON_RISE = 16.0ms		16.0	18.4	ms
$t_{OFF(DLY)}$	Power off sequence delay, (64h) TOFF_DELAY	V_{VCC} = 4.5V	TOFF_DELAY = 0ms		0	0.05	ms
			TOFF_DELAY = 1.0ms		1.0	1.1	ms
			TOFF_DELAY = 1.5ms		1.5	1.65	ms
			TOFF_DELAY = 2.0ms		2.0	2.2	ms

5.5 Electrical Characteristics (continued)

T_J = –40°C to +125°C, PVIN = 4V to 18V, V_{VCC} = 4.5V to 5.0V (unless otherwise noted). Typical values are at T_J = 25°C, PVIN = 12V and V_{VCC} = 4.5V.

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
$SR_{(Fall)}$	Soft-stop slew rate, (65h) TOFF_FALL	V_{VCC} = 4.5V, VOSL = 0.5 (5mV VID table), VDACBOOT = 0.55V	TOFF_FALL = 0.5ms		–2.22		mV/µs
			TOFF_FALL = 1ms		–1.11		mV/µs
			TOFF_FALL = 2ms		–0.56		mV/µs
			TOFF_FALL = 4ms		–0.28		mV/µs
		V_{VCC} = 4.5V, VOSL = 0.25 (10mV VID table), VDACBOOT = 0.45V	TOFF_FALL = 0.5ms		–3.64		mV/µs
			TOFF_FALL = 1ms		–1.82		mV/µs
			TOFF_FALL = 2ms		–0.91		mV/µs
			TOFF_FALL = 4ms		–0.46		mV/µs
POWER STAGE							
$R_{DSON(HS)}$	High-side MOSFET on-resistance	T_J = 25°C, PVIN = 12V	$V_{BOOT-PHASE}$ = 4.5V		6.7		mΩ
			$V_{BOOT-PHASE}$ = 5V		6.5		mΩ
$R_{DSON(LS)}$	Low-side MOSFET on-resistance	T_J = 25°C, PVIN = 12V	$V_{VCC/VDRV}$ = internal bias (4.5V)		2.1		mΩ
			$V_{VCC/VDRV}$ = 5V		2.0		mΩ
$t_{ON(min)}$	Minimum ON pulse width	V_{VDRV} = V_{VCC} = internal bias			30		ns
$t_{OFF(min)}$	Minimum OFF pulse width	V_{VDRV} = V_{VCC} = internal bias, I_O =1.5A, V_{OUT} = $V_{OUT(set)}$ – 20mV, SW falling edge to rising edge			210	250	ns
BOOTSTRAP CIRCUIT							
$I_{BOOT(LKG)}$	BOOT leakage current	V_{EN} = 2V, $V_{BOOT-SW}$ = 5V				150	µA
$V_{BT-PH(UV\_F)}$	BOOT-PHASE UVLO falling threshold				3		V
OVERCURRENT PROTECTION							
$I_{LS(OC)}$	Low-side MOSFET valley overcurrent limit, (46h) IOUT_OC_FAULT_LIMIT (1)	IOUT_OC_FAULT_LIMIT = 8A		6.5	8	9.5	A
		IOUT_OC_FAULT_LIMIT = 10A		8.5	10	11.5	A
		IOUT_OC_FAULT_LIMIT = 12A		10.5	12	13.5	A
		IOUT_OC_FAULT_LIMIT = 15A		13.5	15	16.5	A
		IOUT_OC_FAULT_LIMIT = 16A		14.4	16	17.6	A
		IOUT_OC_FAULT_LIMIT = 20A		18	20	22	A
		IOUT_OC_FAULT_LIMIT = 24A		21.6	24	26.4	A
		IOUT_OC_FAULT_LIMIT = 25A		22.5	25	27.5	A
		IOUT_OC_FAULT_LIMIT = 30A		27	30	33	A
		IOUT_OC_FAULT_LIMIT = 32A		28.8	32	35.2	A
		IOUT_OC_FAULT_LIMIT = 35A		31.5	35	38.5	A
$I_{LS(NOC)}$	Low-side MOSFET negative overcurrent limit (1)	≥ 12A	SEL_NOC = 00b		–22.1	–18.6	A
			SEL_NOC = 01b		–17.8	–15.6	A
			SEL_NOC = 10b		–13.9	–12	A
			SEL_NOC = 11b		–6.2	–4.9	A
		≤ 8A	SEL_NOC = 00b		–10.8	–9.2	A
			SEL_NOC = 01b		–8.9	–7.7	A
			SEL_NOC = 10b		–6.9	–5.7	A
			SEL_NOC = 11b		–3.1	–2.0	A
$I_{ZC(CCM)}$	Zero-cross detection current threshold (CCM operation, entering DCM)	V_{IN} = 12V, V_{VCC} = 4.5V	SEL_ZC = 00b		1000		mA
			SEL_ZC = 01b		700		mA
			SEL_ZC = 10b		–250		mA
			SEL_ZC = 11b		–500		mA
OUTPUT OVF/UVF							
V_{OVF}	Vout overvoltage fault (OVF) threshold, (40h) VOUT_OV_FAULT_LIMIT	(VOSNS – GOSNS) rising	VOUT_OV_FAULT_LIMIT = 573d		112%		VOC
			VOUT_OV_FAULT_LIMIT = 594d	113%	116%	119%	VOC
			VOUT_OV_FAULT_LIMIT = 614d	117%	120%	123%	VOC
			VOUT_OV_FAULT_LIMIT = 634d		124%		VOC
$V_{OVF(acc)}$	Vout OVF accuracy	(VOSNS – GOSNS) rising		–3%		3%	VOC
V_{UVF}	Vout undervoltage fault (UVF) threshold, (44h) VOUT_UV_FAULT_LIMIT	(VOSNS – GOSNS) falling	VOUT_UV_FAULT_LIMIT = 430d		84%		VOC
			VOUT_UV_FAULT_LIMIT = 389d	73%	76%	79%	VOC
			VOUT_UV_FAULT_LIMIT = 348d		68%		VOC
			VOUT_UV_FAULT_LIMIT = 307d		60%		VOC

5.5 Electrical Characteristics (continued)

T_J = –40°C to +125°C, PVIN = 4V to 18V, V_{VCC} = 4.5V to 5.0V (unless otherwise noted). Typical values are at T_J = 25°C, PVIN = 12V and V_{VCC} = 4.5V.

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
$V_{OVF(acc)}$	Vout UVF accuracy	(VOSNS – GOSNS) falling		–3%		3%	VOC
	Vout UVF and UVW delay time	(45h) VOUT_UV_FAULT_RESPONSE<2:0> = x00b			1.6		µs
		(45h) VOUT_UV_FAULT_RESPONSE<2:0> = x01b			16		µs
		(45h) VOUT_UV_FAULT_RESPONSE<2:0> = x10b			64		µs
		(45h) VOUT_UV_FAULT_RESPONSE<2:0> = x11b			256		µs
T_{HICCUP}	Hiccup sleep time before a restart. Applicable to all faults with hiccup response option.	(45h) VOUT_UV_FAULT_RESPONSE<5:3> = 111b			56		ms
$V_{OVF(FIX)}$	V_{OUT} fixed OVF protection threshold	VOUT_SCALE_LOOP = 1	OVF_FIXED = 0b		0.75		V
			OVF_FIXED = 1b		0.9		V
		VOUT_SCALE_LOOP = 0.5 (5mV VID table)	OVF_FIXED = 0b	1.44	1.5	1.53	V
			OVF_FIXED = 1b	1.725	1.8	1.83	V
		VOUT_SCALE_LOOP = 0.25 (10mV VID table)	OVF_FIXED = 0b	2.305	2.4	2.45	V
			OVF_FIXED = 1b	2.88	3.0	3.06	V
		VOUT_SCALE_LOOP = 0.125	OVF_FIXED = 0b		4.8		V
			OVF_FIXED = 1b		6.0		V
OUTPUT OVW/UVW							
V_{OVW}	Overvoltage warning (OVW) threshold, (42h) VOUT_OV_WARN_LIMIT	(VOSNS – GOSNS) rising	VOUT_OV_WARN_LIMIT = 532d		104%		VOC
			VOUT_OV_WARN_LIMIT = 553d	105%	108%	111%	VOC
			VOUT_OV_WARN_LIMIT = 573d	109%	112%	115%	VOC
			VOUT_OV_WARN_LIMIT = 594d		116%		VOC
$t_{OVW(DLY)}$	OVW delay time	(VOSNS – GOSNS) > V_{OVW}			2		µs
$V_{UVW(range)}$	Undervoltage warning (UVW) threshold, (43h) VOUT_UV_WARN_LIMIT programmable range	(VOSNS – GOSNS) falling		68%		96%	VOC
$V_{UVW(res)}$	Undervoltage warning (UVW) threshold resolution				4%		VOC
V_{UVW}	Undervoltage warning (UVW) threshold, (43h) VOUT_UV_WARN_LIMIT	(VOSNS – GOSNS) falling	VOUT_UV_WARN_LIMIT = 492d		96%		VOC
			VOUT_UV_WARN_LIMIT = 471d		92%		VOC
			VOUT_UV_WARN_LIMIT = 451d	85%	88%	91%	VOC
			VOUT_UV_WARN_LIMIT = 430d		84%		VOC
			VOUT_UV_WARN_LIMIT = 410d		80%		VOC
			VOUT_UV_WARN_LIMIT = 389d		76%		VOC
			VOUT_UV_WARN_LIMIT = 369d		72%		VOC
			VOUT_UV_WARN_LIMIT = 348d		68%		VOC
VRRDY							
$t_{PG(DLY\_RISE)}$	Power good rising edge delay (soft-start done to high delay time, only occurs during startup)	PGD_DEL = 00b			0		ms
		PGD_DEL = 01b			0.5		ms
		PGD_DEL = 10b			1.0		ms
		PGD_DEL = 11b			2.0		ms
$t_{PG(DLY\_UVF)}$	Power good falling edge delay from UVF (1)				1		µs
$I_{PG(LKG)}$	Power good pin leakage current when open drain output is high	V_{VRRDY} = 5V				5	µA
$V_{OL(PG)}$	Power good pin output low-level voltage	I_{VRRDY} = 10mA, V_{IN} = 12V, V_{VCC} = 4.5V				300	mV
	Minimum VCC for valid power good output	V_{EN} = 0V, R_{pullup} = 10kΩ, V_{VRRDY} ≤ 0.3V				1.2	V
OUTPUT DISCHARGE							
R_{DISCHG}	Output discharge on VOSNS pin	PVIN = 12V, V_{VCC} = 4.5V, V_{VOSNS} = 0.5V, V_{EN} = 0V		1.15	1.47	1.85	kΩ

5.5 Electrical Characteristics (continued)

T_J = –40°C to +125°C, PVIN = 4V to 18V, V_{VCC} = 4.5V to 5.0V (unless otherwise noted). Typical values are at T_J = 25°C, PVIN = 12V and V_{VCC} = 4.5V.

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
THERMAL SHUTDOWN AND TEMPERATURE PROTECTION							
$T_{J(SD)}$	Thermal shutdown threshold (1)	Junction temperature rising	SEL_OTF_BG = 0b011	98	110	122	°C
			SEL_OTF_BG = 0b010	108	120	132	°C
			SEL_OTF_BG = 0b001	118	131	143	°C
			SEL_OTF_BG = 0b000	129	142	154	°C
			SEL_OTF_BG = 0b111	141	154	167	°C
			SEL_OTF_BG = 0b110	153	166	180	°C
$T_{J(HYS)}$	Thermal shutdown hysteresis (1)	SEL_OTF_BG = 0b110			15		°C
TELEMETRY (PMBUS AND SVID)							
$M_{IOUT(rng)}$	Output current measurement range	ICC_MAX = 40A		0		40	A
$M_{IOUT(acc)}$	Output current measurement accuracy (T_J = 0°C to 125°C)	ICC_MAX = 8A, FCCM	0A ≤ I_{OUT} ≤ 8A (1)	–0.45		1.35	A
		ICC_MAX = 20A, FCCM	0A ≤ I_{OUT} ≤ 6A	–0.75		0.75	A
			6A < I_{OUT} ≤ 12A (1)	–0.75		0.75	A
			14A < I_{OUT} ≤ 20A (1)	–6%		6%	
		ICC_MAX = 40A, FCCM	0A ≤ I_{OUT} ≤ 8A (1)	–0.75		0.75	A
			I_{OUT} = 12A (1)	–8%		8%	
			24A < I_{OUT} ≤ 40A (1)	–6%		6%	
$M_{VOUT(rng)}$	Output voltage measurement range			0		6	V
$M_{VOUT(acc)}$	Output voltage measurement accuracy datapoint	VOUT_SCALE_LOOP = 1	V_{OUT} = 0.5V	0.49	0.5	0.51	V
		VOUT_SCALE_LOOP = 0.5	V_{OUT} = 0.75V	0.736	0.75	0.764	V
			V_{OUT} = 1.2V	1.184	1.199	1.213	V
		VOUT_SCALE_LOOP = 0.25	V_{OUT} = 1.5V	1.48	1.5	1.52	V
			V_{OUT} = 1.8V	1.775	1.801	1.824	V
		VOUT_SCALE_LOOP = 0.125	V_{OUT} = 3.3V	3.254	3.301	3.348	V
$M_{PIN(rng)}$	Input power measurement range	PIN_SENSE_RES = 111b (0.25mΩ)		0		640	W
$M_{PVIN(rng)}$	Input voltage measurement range			4		18	V
$M_{PVIN(acc)}$	Input voltage measurement accuracy datapoint	T_J = 25°C	VIN = 8V	7.875	8	8.125	V
			VIN = 12V	11.875	12	12.125	V
			VIN = 16V	15.84375	16	16.15625	V
$M_{IIN(rng)}$	Input current measurement range	PIN_SENSE_RES = 011b (1.0mΩ)		0		40	A
		PIN_SENSE_RES = 101b (0.5mΩ)		0		40	A
$M_{IIN(acc)}$	Input current measurement accuracy datapoint	T_J = 25°C, PIN_SENSE_RES = 011b (1mΩ)	I_{IN} = 15A	14.685	15	15.315	A
			I_{IN} = 20A	19.58	20	20.42	A
			I_{IN} = 25A	24.475	25	25.525	A
		T_J = 25°C, PIN_SENSE_RES = 101b (0.5mΩ)	I_{IN} = 15A	14.685	15	15.315	A
			I_{IN} = 20A	19.58	20	20.42	A
			I_{IN} = 25A	24.475	25	25.525	A
$M_{TSNS(rng)}$	Internal temperature sense range			–40		150	°C
$M_{TSNS(acc)}$	Internal temperature sense accuracy (1)	–40°C ≤ T_J ≤ 125°C		–4		4	°C
ANALOG IMON							
A_{IMON}	Analog IMON output gain	ICC_MAX ≤ 8A			8		A/V
		8A < ICC_MAX ≤ 20A			16		A/V
		ICC_MAX > 20A			32		A/V
$IMON_{(OFF)}$	Analog IMON offset error			–0.1		0.1	V
$IMON_{(GAIN)}$	Analog IMON gain error			–10%		10%	
PMBUS INTERFACE							
$V_{IH(PMBUS)}$	High-level input voltage on PMB_CLK, PMB_DATA			1.35			V
$V_{IL(PMBUS)}$	Low-level input voltage on PMB_CLK, PMB_DATA					0.8	
$I_{IH(PMBUS)}$	Input high level current into PMB_CLK, PMB_DATA			–10		10	µA

5.5 Electrical Characteristics (continued)

T_J = –40°C to +125°C, PVIN = 4V to 18V, V_{VCC} = 4.5V to 5.0V (unless otherwise noted). Typical values are at T_J = 25°C, PVIN = 12V and V_{VCC} = 4.5V.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$V_{OL(PMBUS)}$	Output low level voltage on PMB_DATA and ALERT#	VCC ≥ 4.5V, I_{pin} = 20mA			0.4	V
$I_{OH(PMBUS)}$	Output high level open drain leakage current into PMB_DATA, ALERT#	V_{pin} = 5.5V			10	µA
$I_{OL(PMBUS)}$	Output low level open drain sinking current on PMB_DATA, ALERT# (1)	V_{pin} = 0.4V	20			mA
C_{PIN_PMB}	PMB_CLK and PMB_DATA pin input capactiance (1)	V_{pin} = 0.1V to 1.35V			5	pF
$t_{TIMEOUT}$	Detect clock low timeout (1)		25	30	35	ms
N_{WR_NVM}	Number of NVM writeable cycles (1)	–40°C ≤ T_J ≤ 125°C	1000			cycle

(1) Specified by design

5.6 Timing Requirements

PARAMETER		MIN	NOM	MAX	UNIT
PMBUS INTERFACE					
f_{PMB_CLK}	PMBus operating frequency range	10		1000	kHz
t_{BUF}	Bus free time between a STOP and START condition (1)	0.5			µs
t_{HD_STA}	Hold time for a (repeated) START condition (1)	0.26			µs
t_{SU_STA}	Setup time for a repeated START condition (1)	0.26			µs
t_{SU_STO}	Setup time for a STOP condition (1)	0.26			µs
t_{HD_PMB}	PMB_DATA hold time (1)	0			µs
t_{SU_PMB}	PMB_DATA setup time (1)	50			ns
t_{LOW}	Low period of PMB_CLK (1)	0.5			µs
t_{HIGH}	High period of PMB_CLK (1)	0.26		50	µs
t_{R_PMB}	PMB_CLK and PMB_DATA rise time with f_{PMB_CLK} = 100kHz (1) (2)			1000	ns
	PMB_CLK and PMB_DATA rise time with f_{PMB_CLK} = 400kHz (1) (2)			300	ns
	PMB_CLK and PMB_DATA rise time with f_{PMB_CLK} = 1MHz (1) (2)			120	ns
t_{F_PMB}	PMB_CLK and PMB_DATA fall time with f_{PMB_CLK} = 100kHz or 400kHz (1) (3)			300	ns
	PMB_CLK and PMB_DATA fall time with f_{PMB_CLK} = 1MHz (1) (3)			120	ns

(1) Specified by design.
(2) VIL(MAX) – 150mV to VIH(MIN) + 150mV.
(3) VIH(MIN) + 150mV to VIL(MAX) – 150mV.

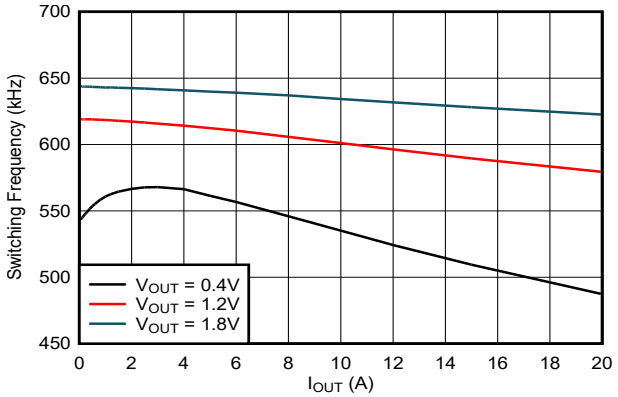
5.7 Switching Characteristics

T_J = –40°C to +125°C, PVIN = 4V to 18V, V_{VCC} = 4.5V to 5.0V (unless otherwise noted). Typical values are at T_J = 25°C, PVIN = 12V and V_{VCC} = 4.5V.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{co_pmb}	VR PMB_CLK falling edge to PMB_DATA delay (1)		65		130	ns

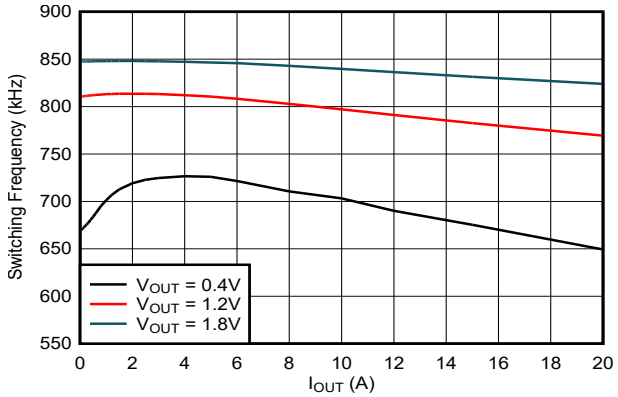
(1) Specified by design

5.8 Typical Characteristics



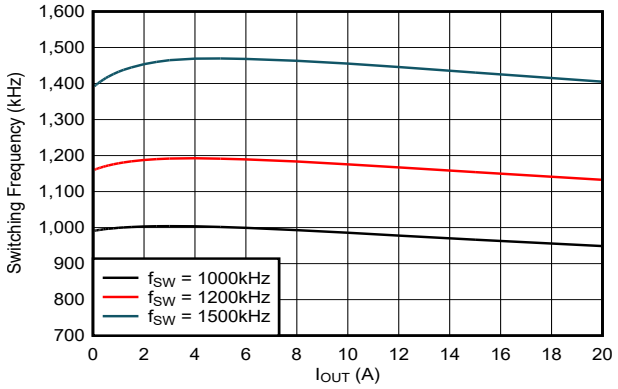
V_{IN} = 12V f_{SW} = 600kHz FCCM
DCLL = 0mΩ

Figure 5-1. 600kHz Switching Frequency versus Output Current



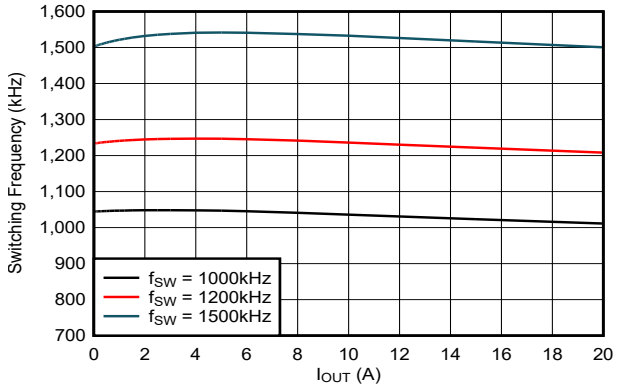
V_{IN} = 12V f_{SW} = 800kHz FCCM
DCLL = 0mΩ

Figure 5-2. 800kHz Switching Frequency versus Output Current



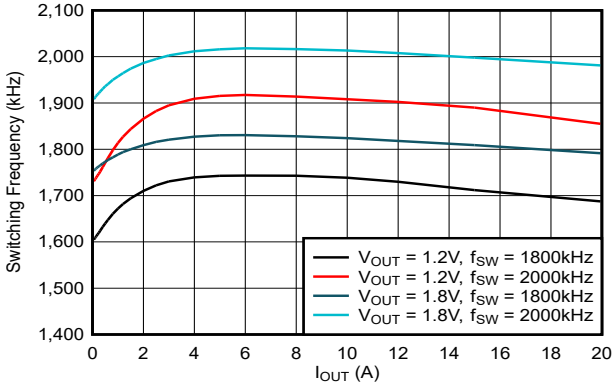
V_{IN} = 12V V_{OUT} = 1.2V FCCM
DCLL = 0mΩ

Figure 5-3. 1.2V Output Switching Frequency versus Output Current



V_{IN} = 12V V_{OUT} = 1.8V FCCM
DCLL = 0mΩ

Figure 5-4. 1.8V Output Switching Frequency versus Output Current



V_{IN} = 12V DCLL = 0mΩ FCCM

Figure 5-5. 1.8V Output Switching Frequency versus Output Current

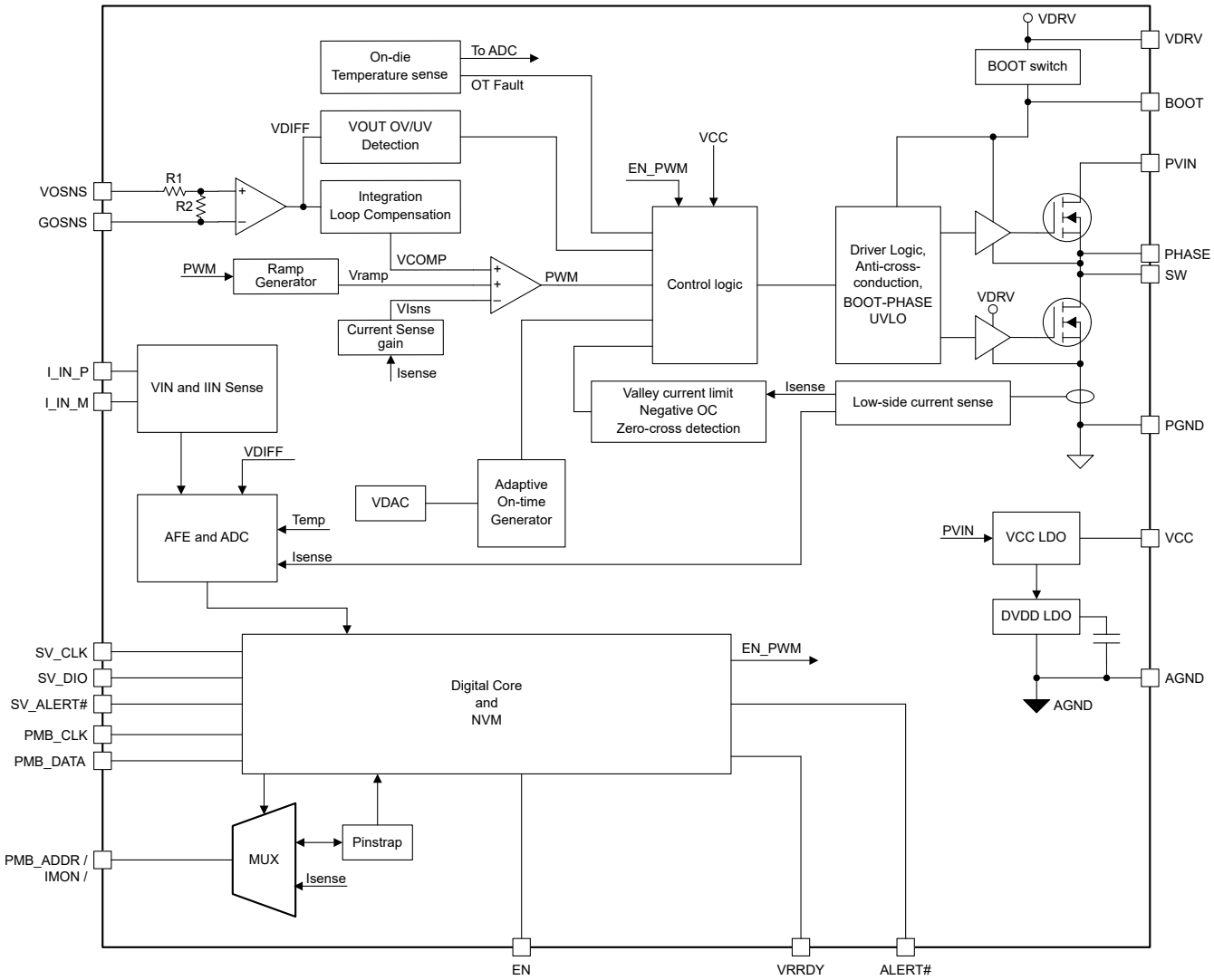
6 Detailed Description

6.1 Overview

The TPS544B27W device is a high-efficiency, highly-integrated, synchronous buck converter with D-CAP+ control topology for fast transient response and reduced output capacitance. D-CAP+ control topology includes programmable droop compensation, also called DC load line (DCLL), for applications requiring adaptive voltage positioning (AVP).

The device is highly configurable by programming through the PMBus interface, and the programmed parameters can be stored in EEPROM as the new default values to minimize the external component count. These features make the device well-designed for space-constrained applications. Overcurrent, overvoltage, and undervoltage, overtemperature protections are provided internally in the device and are programmable. The TPS544B27W device offers a full set of telemetry features including output voltage, output current, device temperature, and input voltage. Optionally, the device can provide input current and input power telemetry by sensing across an external resistor.

6.2 Functional Block Diagram



6.3 Feature Description

6.3.1 Operating Frequency and Mode

The TPS544B27W provides forced continuous conduction mode (FCCM) operation for low output ripple at light-load or discontinuous conduction mode (DCM) with auto-skipping Eco-mode for improved light-load efficiency. The switching frequency and operation mode can be programmed through the PMBus interface using the PMBus (33h) FREQUENCY_SWITCH command and FCCM bit in the PMBus (D0h) SYS_CFG_USER1 command. Changes to PMBus (33h) FREQUENCY_SWITCH take effect immediately, even if the output is enabled. Changes to the FCCM bit do not take effect until the output is disabled through the PMBus (02h) ON_OFF_CONFIG mechanism.

6.3.2 Setting the Output Voltage

The TPS544B27W includes a fully integrated, internal, precision feedback divider. Using both the selectable feedback divider and precision adjustable reference, output voltages up to 5.5V can be obtained. To set the output voltage, the appropriate internal feedback divider gain (VOSL) must be selected through the PMBus interface. The method the internal feedback divider is programmed set by the value in the VOUT_CTRL bits in the PMBus (D0h) SYS_CFG_USER1 command as follows.

- VOUT_CTRL = 00b or 01b: The output voltage is controlled through SVID and the internal feedback divider gain can be programmed to be 0.5 or 0.25 by selecting between the supported PROTOCOL_ID in the PMBus (D1h) SVID_ADDR_CFG_USER command. The PMBus (29h) VOUT_SCALE_LOOP command is read only in this configuration and reflects the active feedback divider gain.
- VOUT_CTRL = 10b: The output voltage is controlled through PMBus and the internal feedback divider can be programmed to divider gains 1, 0.5, 0.25, or 0.125 using the PMBus (29h) VOUT_SCALE_LOOP command.

The valid output voltage range when configured through SVID or PMBus depends upon the feedback divider ratio configured as shown in Table 6-1. Setting the output voltage near the low end of the range can negatively affect VOUT regulation accuracy while setting the output voltage above the recommended range can limit the actual output voltage achieved.

Note

The output must be disabled through the PMBus (02h) ON_OFF_CONFIG mechanism before changing PMBus VOUT_CTRL, (29h) VOUT_SCALE_LOOP and PROTOCOL_ID. VOUT_CTRL and PROTOCOL_ID can be updated while the output is enabled, but the output must be disabled for the change to take effect. The device NACKs attempts to change PMBus (29h) VOUT_SCALE_LOOP while the output is enabled.

Table 6-1. Valid Output Voltage Range

INTERNAL DIVIDER GAIN	VOUT_CTRL	SVID (05h) PROTOCOL_ID	PMBus® (29h) VOUT_SCALE_LOOP	VALID OUTPUT VOLTAGE RANGE(1)
1.0	10b only	N/A	1.0	0.250V to 0.768V
0.5	All values	07h, 09h (5mV VID table) (2)	0.5(3)	0.250V to 1.536V
0.25	All values	04h, 0Ah (10mV VID table)(2)	0.25(3)	0.500V to 3.072V
0.125	10b only	N/A	0.125	1.000V to 5.500V

(1) The valid output voltage range must consider any offset added through PMBus (22h) VOUT_TRIM or OFFSET_1 and margin through PMBus (25h) VOUT_MARGIN_HIGH or PMBus (26h) VOUT_MARGIN_LOW.
(2) The PROTOCOL_ID values are the values in the SVID register. PROTOCOL_ID in the PMBus (D1h) SVID_ADDR_CFG_USER command is a 2-bit field. Refer to the PROTOCOL_ID description in Section 7 on how to select between 5mV or 10mV VID tables, and between VR13 or VR14.
(3) PMBus (29h) VOUT_SCALE_LOOP is read only with VOUT_CTRL = 00b or 01b.

The initial boot up voltage (VBOOT) after the output is enabled is set by either VBOOT_0 in the PMBus (D6h) VBOOT_DCLL command or VBOOT_1 in the PMBus (D7h) VBOOT_OFFSET_1 command. VBOOT_0 or VBOOT_1 is selected by the PMB_ADDR resistor as described in Section 6.3.9.1. VBOOT sets the initial boot

up reference DAC voltage (VDAC_BOOT) and the regulated output voltage is scaled up by the internal feed back divider gain. The possible VBOOT voltages for each VOSL are shown in Table 6-2.

Table 6-2. VBOOT Voltages

VBOOT_0 or VBOOT_1	VDAC_BOOT (V)	VBOOT (V)			
		VOSL = 1	VOSL = 0.5	VOSL = 0.25	VOSL = 0.125
00000b	0(1)	0(1)	0(1)	0(1)	0(1)
00001b	0.3	0.3	0.6	1.2	2.4
00010b	0.3125	0.3125	0.625	1.25	2.5
00011b	0.325	0.325	0.65	1.3	2.6
00100b	0.3375	0.3375	0.675	1.35	2.7
00101b	0.35	0.35	0.7	1.4	2.8
00110b	0.3625	0.3625	0.725	1.45	2.9
00111b	0.375	0.375	0.75	1.5	3
01000b	0.3875	0.3875	0.775	1.55	3.1
01001b	0.4	0.4	0.8	1.6	3.2
01010b	0.4125	0.4125	0.825	1.65	3.3
01011b	0.425	0.425	0.85	1.7	3.4
01100b	0.4375	0.4375	0.875	1.75	3.5
01101b	0.45	0.45	0.9	1.8	3.6
01110b	0.4625	0.4625	0.925	1.85	3.7
01111b	0.475	0.475	0.95	1.9	3.8
10000b	0.4875	0.4875	0.975	1.95	3.9
10001b	0.5	0.5	1	2	4
10010b	0.5125	0.5125	1.025	2.05	4.1
10011b	0.525	0.525	1.05	2.1	4.2
10100b	0.5375	0.5375	1.075	2.15	4.3
10101b	0.55	0.55	1.1	2.2	4.4
10110b	0.5625	0.5625	1.125	2.25	4.5
10111b	0.575	0.575	1.15	2.3	4.6
11000b	0.5875	0.5875	1.175	2.35	4.7
11001b	0.6	0.6	1.2	2.4	4.8
11010b	0.625	0.625	1.25	2.5	5
11011b	0.65	0.65	1.3	2.6	5.2
11100b	0.675	0.675	1.35	2.7	5.4
11101b	0.7	0.7	1.4	2.8	5.5
11110b	0.725	0.725	1.45	2.9	5.5
11111b	0.75	0.75	1.5	3	5.5

(1) VBOOT = 0V results in booting up into the VID0 state.

An offset (VOFFSET) can be added to the output voltage through the PMBus (22h) VOUT_TRIM command or OFFSET_1 located in the PMBus (D7h) VBOOT_OFFSET_1 command. VOFFSET affects the output voltage at startup and after start-up. The VBOOT voltage including VOFFSET can be calculated with Equation 1. How VOFFSET is applied to the output voltage depends on VOUT_CTRL as follows.

- VOUT_CTRL = 00b: Selection between PMBus (22h) VOUT_TRIM and OFFSET_1 is enabled and the VOFFSET used is selected by the PMB_ADDR resistor as described in Section 6.3.9.1. The register value in the PMBus (22h) VOUT_TRIM command or OFFSET_1 field are loaded directly to the SVID (33h) OFFSET register. As a result, the step size of the VOFFSET added follows the 5mV or 10mV SVID VID table selected through PROTOCOL_ID. The VOFFSET added through PMBus (22h) VOUT_TRIM does not follow the PMBus (20h) VOUT_MODE format.
- VOUT_CTRL = 01b or 10b: VOFFSET can only be added through the PMBus (22h) VOUT_TRIM command and the offset follows the PMBus (20h) VOUT_MODE format.

$$V_{BOOT} = \frac{V_{DAC\_BOOT}}{VOUT\_SCALE\_LOOP} + V_{OFFSET} \quad (1)$$

Table 6-3 gives an example on how to set the VBOOT voltage to 1.110V for each VOUT_CTRL setting. This table assumes Option 0 is selected through the PMB_ADDR resistor.

Table 6-3. Setting the VBOOT Voltage Example

VOUT_CTRL	INTERNAL DIVIDER GAIN		VBOOT_0 FIELD VALUE	PMBus® (22h) VOUT_TRIM COMMAND VALUE
	COMMAND OR FIELD	VALUE		
00b	PROTOCOL_ID in PMBus (D1h) SVID_ADDR_CFG_USER	10b (VR14, 5mV)	10101b	0002h
01b	PROTOCOL_ID in PMBus (D1h) SVID_ADDR_CFG_USER	10b (VR14, 5mV)	10101b	000Ah
10b	PMBus (29h) VOUT_SCALE_LOOP	E804h	10101b	000Ah

After start-up, the output voltage can be programmed to a different voltage through either the SVID interface or the PMBus interface, depending upon the value of VOUT_CTRL. When the output is controlled through the SVID interface, the device follows the SVID VID table. When the output voltage is controlled through PMBus, the device follows the PMBus (20h) VOUT_MODE format. If the output is disabled then re-enabled, the output voltage ramps up to VBOOT programmed in the active VBOOT register.

Table 6-4 summarizes the methods possible to program the output voltage.

Table 6-4. VOUT Control Methods

VOUT_CTRL	METHOD	START-UP		AFTER STERT-UP	
		V_{OUT}	V_{OFFSET}	V_{OUT}	V_{OFFSET}
00b(1)	SVID	VBOOT_0 or VBOOT_1	PMBus (22h) VOUT_TRIM or OFFSET_1	SVID commands (such as SetVID and SetWP)	SVID register (33h) OFFSET
01b(2)	SVID+PMBus	VBOOT_0 or VBOOT_1	PMBus (22h) VOUT_TRIM	SVID commands (such as SetVID and SetWP)	Cannot be changed after start-up
10b(3)	PMBus	VBOOT_0 or VBOOT_1	PMBus (22h) VOUT_TRIM	PMBus (21h) VOUT_COMMAND	PMBus (22h) VOUT_TRIM

(1) Writes to PMBus (21h) VOUT_COMMAND are allowed but do not affect the output voltage.
(2) Writes to PMBus (21h) VOUT_COMMAND and SVID (33h) OFFSET register are allowed but do not affect the output voltage.
(3) Writes through the SVID interface are allowed but do not affect the output voltage.

There is no minimum programming limit to the voltage that can be programmed through either the SVID interface or the PMBus interface. The maximum output voltage that can be programmed is limited by either SVID VIDO_MAX field (located in SVID registers 09h and 0Ah) or PMBus (24h) VOUT_MAX command depending on the value of VOUT_CTRL as follows.

- VOUT_CTRL = 00b: The output voltage is programmed only through the SVID interface, so the output voltage plus offset is limited by the SVID VIDO_MAX field.
- VOUT_CTRL = 01b: The output voltage programmed through the SVID interface (such as with SetVID or SetWP commands) are limited by SVID VIDO_MAX field. The offset programmed through PMBus (22h) VOUT_TRIM is not limited.
- VOUT_CTRL = 10b: The output voltage is programmed only through the PMBus interface, so the output voltage plus offset is limited by PMBus (24h) VOUT_MAX command.

6.3.3 DC Load Line

The TPS544B27W device supports adaptive voltage positioning (AVP) also called DC Load Line (DCLL). Using a non-zero DCLL causes the output voltage to decrease proportionally to the output current. Using a non-zero DCLL is optional. A suggested DCLL setting is typically given in the requirements for the rail being powered by

the device. If no droop is suggested, TI recommends setting DCLL to 0mΩ to avoid violating the V_{OUT} tolerance band specification.

DCLL provides two potential benefits:

- Reduces the total peak-to-peak output voltage excursion during transient load steps, allowing for reduced output capacitance and can compensate for the resistance in the system between the regulator and the load.
- Reduces power consumption in the system when load current is high by automatically decreasing the output voltage.

The DCLL setting is configured through the DCLL_0 and DCLL_1 bit fields in the VBOOT_DCLL command. PMB_ADDR pinstrap selects between the two options. The active DCLL setting can be read through the VOUT_DROOP command.

6.3.4 Fault Management

Table 6-5 summarizes the fault protection in the TPS544B27W and how the device responds to them. All faults can assert SMB_ALERT# can be masked through the SMBALERT_MASK command.

Table 6-5. Fault Protection Summary

FAULT OR WARNING	PMBUS® COMMAND	ACTIVE DURING t_{ON_RISE}	FAULT RESPONSE SETTING	POWER MOSFET BEHAVIOR	VRRDY STATUS
Thermal Shutdown	OT_FAULT_RESPONSE	Yes	Latch-off	Both MOSFETs off	Low
			Restart	Both MOSFETs off; restart after hiccup delay	
Low-side OC fault	IOUT_OC_FAULT_LIMIT	Yes	Continue operation while limiting current	Low-side MOSFET stays on until current drops below limit. High-side MOSFET on-time controlled by PWM.	High
OC warning	IOUT_OC_WARN_LIMIT	Yes	N/A	MOSFETS controlled by PWM	High
Negative OC fault	SEL_NOC in (D0h) SYS_CFG_USER1	Yes	N/A	Turn off low-side MOSFET	High
V_{OUT} OV fault (tracking)	VOUT_OV_FAULT_LIMIT, VOUT_OV_FAULT_RESPONSE	No	Latch-off	Low-side MOSFET latched on and protected by negative OC; high-side MOSFET off.	Low
			Restart	Low-side MOSFET latched on and protected by negative OC; high-side MOSFET off; restart after hiccup delay.	
			Ignore	MOSFETS controlled by PWM	High
V_{OUT} OV fault (fixed)	SEL_FIX_OVF and EN_FIX_OVF in (D0h) SYS_CFG_USER1, VOUT_OV_FAULT_RESPONSE	Yes	Latch-off	Low-side MOSFET latched on and protected by negative OC; high-side MOSFET off.	Low
			Restart	Low-side MOSFET latched on and protected by negative OC; high-side MOSFET off; restart after hiccup delay.	
			Ignore	MOSFETS controlled by PWM	High
V_{OUT} OV warning (tracking)	VOUT_OV_WARN_LIMIT	No	N/A	MOSFETS controlled by PWM	High
V_{OUT} UV fault (tracking)	VOUT_UV_FAULT_LIMIT, VOUT_UV_FAULT_RESPONSE	No	Latch-off	Both MOSFETs off	Low
			Restart	Both MOSFETs off; restart after hiccup delay	
			Ignore	MOSFETS controlled by PWM	High
V_{OUT} UV warning (tracking)	VOUT_UV_WARN_LIMIT	No	N/A	MOSFETS controlled by PWM	High
PVIN UVLO	VIN_ON, VIN_OFF	Yes	Shutdown	Both MOSFETs off	Low
PVIN OV fault	VIN_OV_FAULT_LIMIT	Yes	Latch-off	Both MOSFETs off	Low

6.3.5 Current Sense and Positive Overcurrent Protection

For a buck converter, the switch current increases at a linear rate determined by input voltage, output voltage, and the output inductor value during the high-side MOSFET on-time (ON time). During the on-time of the low-side MOSFET (OFF time), this current decreases linearly determined by the output voltage and the output inductor value. The average value of the switch current is the load current I_{OUT}. The inductor during the OFF time, even with a negative slew rate, usually flows from the device SW node to the load the device which is said to be sourcing current and the output current is declared to be positive.

The output overcurrent limit (OCL) in the TPS544B27W is implemented to clamp low-side *valley current* on a cycle-by-cycle basis. The inductor current is monitored during the OFF time by sensing the current flowing through the low-side MOSFET. When the sensed low-side MOSFET current remains above the selected OCL threshold, the low-side MOSFET stays ON until the sensed current level becomes lower than the selected OCL threshold. This operation extends the OFF time and pushes the next ON time (where the high-side MOSFET turns on) out. During an overcurrent event, the current sunk by the load (I_{OUT}) exceeds the current sourced by the device to the output capacitors, thus, the output voltage tends to decrease. Eventually, when the output voltage falls below the undervoltage-protection threshold, the UVP comparator detects undervoltage and after a delay time set in the PMBus (45h) VOUT_UV_FAULT_RESPONSE command responds to the fault. Through the same PMBus (45h) VOUT_UV_FAULT_RESPONSE command, the device response and retry setting can be configured to retry after a hiccup delay time, remain latched off state (both high-side and low-side MOSFETs are latched off) or continue operation without interruption. If configured for latch off, a reset of VCC or a re-toggling of the EN pin is required to leave the latched off state.

If an OCL condition occurs during start-up the device still has cycle-by-cycle current limit based on the sensed low-side valley current. This operation can limit the energy charged into the output capacitors thus the output voltage typically ramps up slower than the desired soft-start slew rate. During the soft start, the VOUT Tracking UVF comparator is disabled thus the device does not respond to a UVF event. Upon the completion of soft-start the device responds to the UVF event, which is caused by the OCL event.

The OCL feature in the device is implemented by detecting the low-side valley current through analog circuitries and has no relationship with the integrated Analog-to-Digital converter (ADC). The telemetry analog-front-end gets an input from the low-side current sense circuit and average low-side MOSFET current from the start to the end of each low-side MOSFET on time. By this method, the telemetry sub-system reports the load current (I_{OUT}) which is the average value of the inductor current but not peak or valley values

6.3.6 Negative Overcurrent Limit

The TPS544B27W device is a synchronous buck converter, thus current can flow from the device to the load or from the load into the device through the SW node. When current flows from the SW node to the load, the device sources current (positive output current). When current flows from the load into the SW node, the device sinks current (negative output current).

The device features a programmable, cycle-by-cycle negative overcurrent (NOC) protection limit, configurable through the SEL_NOC bits in the SYS_CFG_USER1 command. Similar to positive overcurrent protection, the device monitors inductor current during the low-side MOSFET ON period to limit the valley inductor current. When detected current exceeds the selected NOC limit, the device turns off the low-side MOSFET to prevent excessive negative current that can damage the device. Following NOC turning off the low-side MOSFET as a protective action, the high-side MOSFET turns on for the duration set by the adaptive on-time generator, which is based on input voltage (V_{IN}), sensed output voltage (V_{OUT}), and the selected switching frequency (f_{SW}).

NOC protection typically activates after an overvoltage event but can also engage during VOUT step-down transitions with fast slew rates.

CAUTION

Avoid selecting an NOC limit less than half the worst-case peak-to-peak inductor ripple current. Setting too low a limit causes the device to restrict valley inductor current during light-load or no-load conditions in normal operation. When negative inductor current becomes limited, the low-side ON period shortens and volt-second balance across the inductor is disrupted. This imbalance causes the output voltage to drift upward until the volt-seconds during high-side on-time equals the volt-seconds during high-side off-time. To avoid this behavior, TI recommends selecting the highest NOC limit by setting SEL_NOC = 00b and ICC_MAX ≥ 010b.

6.3.7 Zero-Crossing Detection

The TPS544B27W device uses a zero-crossing (ZC) circuit to perform the zero inductor current detection during skip-mode operation. The ZC threshold is set to a small positive value before the low-side MOSFET is turned off to compensate for delay in the ZC detection circuit, entering discontinuous conduction mode (DCM) operation. After entering DCM, the ZC threshold hysteresis increases the threshold to a higher postive value. As a result, the device delivers better light-load efficiency. The low-side MOSFET body diode can conduct for a short period depending on the input voltage, inductor value, switching frequency, and output voltage.

6.3.8 Overtemperature Protection

The TPS544B27W device implements three overtemperature protection (OTP) mechanisms for comprehensive thermal safety. For all mechanisms switching stops when the sensed IC temperature goes beyond the respective threshold. The device responds to all mechanisms as configured through the OT_FAULT_RESPONSE PMBus command.

The controller monitors the temperature via an on-die temperature sensor. This sensed temperature is compared to the threshold selected through SEL_OTF_BG with an analog comparator.

The power stage die employs a separate temperature sensor for OTP with a fixed threshold of 166°C typical (rising).

Note

The third OTP mechanism, the user programmable OTP selected through the OT_FAULT_LIMIT, is not functional. If the device temperature monitored through READ_TEMPERATURE_1 telemetry is greater than OT_FAULT_LIMIT, the device does not respond. The device also does not respond to READ_TEMPERATURE_1 greater than the programmed OT_WARN_LIMIT.

6.3.9 PMBus® Interface

6.3.9.1 Setting the PMBus® Address

The TPS544B27W offers selectable PMBus address either through a resistor from the PMB_ADDR pin to AGND or programmable address by writing an address value into the PMB_ADDR field located in the PMBus (D2h) PMB_ADDR command. The resistor value is detected at VCC power-on. To use the address programmed into the PMBus (D2h) PMB_ADDR command, the OVRD_PMB_ADDR bit also located in the PMBus (D2h) PMB_ADDR command must be set and the VCC must be reset before the device responds to the programmed address.

The PMB_ADDR preconfigured PMBus addresses selected with the resistor to AGND are shown in Table 6-6. A resistor with ±1% tolerance and temperature coefficient of ±100ppm/°C or better is required. Up to 8 different addresses can be selected. The bits marked with an X in Table 6-6 are programmed by the SEL_PSTR_ADDR_BASE located in the PMBus (D2h) PMB_ADDR command.

In addition to setting the PMBus address, the PMB_ADDR pin resistor value selects between two sources for the SVID registers VBOOT, OFFSET, and DC_LL . The two sources selected from are called option 0 and 1. Table 6-7 summarizes the sources for option 0 and 1. Because the resistor value at PMB_ADDR is detected at VCC power-on, VCC must be reset to change between option 0 and 1.

Table 6-6. PMB_ADDR Pin Resistor Selected Values

R_{ADDR} (kΩ)	PMBUS® ADDRESS (bin)	PMBUS® ADDRESS WITH SEL_PSTR_ADDR_BASE = 1110b		VBOOT, OFFSET, DCLL
		binary	hex	
≤1.78 (SHORT)	XXXX001	1110001	71	1
2.21	XXXX000	1110000	70	
2.74	XXXX010	1110010	72	
3.32	XXXX011	1110011	73	
4.02	XXXX001	1110001	71	0
4.87	XXXX000	1110000	70	
5.9	XXXX010	1110010	72	
7.32	XXXX011	1110011	73	
9.09	XXXX111	1110111	77	1
11.3	XXXX110	1110110	76	
14.3	XXXX101	1110101	75	
18.2	XXXX100	1110100	74	
22.1	XXXX011	1110011	73	
26.7	XXXX010	1110010	72	
33.2	XXXX001	1110001	71	
40.2	XXXX000	1110000	70	
49.9	XXXX111	1110111	77	0
60.4	XXXX110	1110110	76	
76.8	XXXX101	1110101	75	
102	XXXX100	1110100	74	
137	XXXX011	1110011	73	
174	XXXX010	1110010	72	
243	XXXX001	1110001	71	
≥412 (FLOAT)	XXXX000	1110000	70	

Table 6-7. Option 0 and 1 selection through PMB_ADDR pin

OPTION	PMBUS® SOURCE FOR SVID REGISTER		
	SVID (23h) DC_LL	SVID (26h) VBOOT	SVID (33h) OFFSET
0	DCLL_0 field in PMBus (D6h) VBOOT_DCLL	VBOOT_0 field in PMBus (D6h) VBOOT_DCLL	PMBus (22h) VOUT_TRIM
1	DCLL_1 field in PMBus (D6h) VBOOT_DCLL	VBOOT_1 field in PMBus (D7h) VBOOT_OFFSET_1	OFFSET_1 field in PMBus (D7h) VBOOT_OFFSET_1

6.3.9.2 SMBus Alert Response Address

The TPS544B27W supports the SMB_ALERT# response protocol through the Alert Response Address (ARA). The ARA response protocol is a mechanism by which the target device can alert the bus host about important information. The host can process this event and simultaneously accesses all target devices on the bus that support the protocol through the alert response address. All target devices asserting SMB_ALERT# acknowledge this request with the respective PMBus Address.

When a target device responds to the ARA, the device deasserts SMB_ALERT# but retains the offending status bits. After this successful notification, handling the interrupt becomes the responsibility of the host. The bus controller performs a modified receive byte operation to get the address of the target device, then uses the PMBus status commands to query the target device that caused the alert.

If multiple devices are asserting SMB_ALERT# low, the target device with the lowest address wins communication rights. If the SMB_ALERT# pin remains asserted after a successful receive byte operation using ARA, the host can query the ARA again to determine the next offending device.

To re-enable SMB_ALERT# triggering for initial fault sources (including any that occurred between SMB_ALERT# assertion and the ARA response), the original faults in the TPS544B27W must be cleared. This can be done by either:

- Writing to the CLEAR_FAULTS command
- Re-enabling the output via the method configured in ON_OFF_CONFIG
- Writing 1b to the asserted status bits
- Performing a power reset

Note that new fault sources that become active after the device's response to the ARA immediately trigger SMB_ALERT# again.

For more information on the SMBus alert response protocol, see the system management bus (SMBus) specification.

6.4 Device Functional Modes

6.4.1 Forced Continuous-Conduction Mode

When the operation mode is set to FCCM through the FCCM bit in the PMBus (D0h) SYS_CFG_USER1 command, the controller operates in continuous conduction mode (CCM) during light-load conditions. During CCM, the switching frequency maintained to an almost constant level over the entire load range which is designed for applications requiring tight control of the switching frequency at the cost of lower efficiency at light loads.

When FCCM is selected, the TPS544B27W device operates at CCM during the whole soft-start period as well as the nominal operation.

6.4.2 DCM Light Load Operation

When the operation mode is set to DCM, the device automatically reduces the switching frequency at light-load conditions to maintain high efficiency. This section describes the operation mode in detail.

As the output current decreases from heavy load condition, the inductor current also decreases until the rippled valley of the inductor current touches zero level. Zero level is the boundary between the continuous-conduction and discontinuous-conduction modes. The synchronous MOSFET turns off when this zero inductor current is detected. As the load current decreases further, the converter runs into discontinuous-conduction mode (DCM).

The on-time is maintained to a level approximately the same as during continuous-conduction mode operation, and as a result, discharging the output capacitor with a smaller load current to the level of the reference voltage requires more time. The transition point to the DCM light-load operation mode ($I_{OUT(LL)}$) is calculated as shown in Equation 2.

$$I_{OUT(LL)} = \frac{1}{2 \times L \times f_{SW}} \times \frac{(V_{IN} - V_{OUT}) \times V_{OUT}}{V_{IN}} \quad (2)$$

Where

- f_{SW} is the nominal CCM switching frequency.

The reduced switching frequency ($f_{SW(LL)}$) at load currents less than $I_{OUT(LL)}$ when in DCM is calculated as shown in Equation 3.

$$f_{SW(LL)} = f_{SW} \times \frac{I_{OUT}}{I_{OUT(LL)}} \quad (3)$$

The output voltage peak to peak ripple increases in load operation, reaching up to 4 × the continuous conduction ripple voltage at no load. TI recommends using low ESR capacitors (such as ceramic capacitor) for skip mode.

6.5 Programming

6.5.1 PMBus® Command NVM Defaults

Table 6-8 lists the default for the bit behavior and register values. Word command values are in big endian format (high byte to low byte) and Block command values are given in little endian format (low byte to high byte).

Table 6-8. PMBus® Command Default Values

COMMAND CODE	COMMAND NAME	DEFAULT VALUE	DEFAULT BEHAVIOR
0x01	OPERATION	0x04	ON bit set to 0 and margin off
0x02	ON_OFF_CONFIG	0x17	Turn ON/OFF by EN pin only. When turning off use TOFF_DELAY and TOFF_FALL.
0x0E	PASSKEY	0x00B661	Passkey unset and unlocked. NVM CHECKSUM = 0xB661.
0x10	WRITE_PROTECT	0x00	All commands are writable.
0x19	CAPABILITY	0xD0	Read only. See command description.
0x1B78	ALERT_MASK_BYTE	0xC8	All supported bits unmasked.
0x1B79	ALERT_MASK_WORD	0x0D	All supported bits unmasked.
0x1B7A	ALERT_MASK_VOUT	0x07	All supported bits unmasked.
0x1B7B	ALERT_MASK_IOUT	0x4F	All supported bits unmasked.
0x1B7C	ALERT_MASK_INPUT	0x76	All supported bits unmasked.
0x1B7D	ALERT_MASK_TEMPERATURE	0x3F	All supported bits unmasked.
0x1B7E	ALERT_MASK_CML	0x0D	All supported bits unmasked.
0x1B7F	ALERT_MASK_OTHER	0x7F	All supported bits unmasked.
0x1B80	ALERT_MASK_MFR_SPECIFIC	0x84	All supported bits unmasked.
0x1BCE	ALERT_MASK_PULSE_CATCHER	0xFA	All supported bits unmasked.
0x20	VOUT_MODE	0x97	Read only. See command description.
0x21	VOUT_COMMAND	0x00CE	0.4125V
0x22	VOUT_TRIM	0x0009	+0.018V
0x24	VOUT_MAX	0x0226	1.07421875V
0x25	VOUT_MARGIN_HIGH	0x0210	103.125%
0x26	VOUT_MARGIN_LOW	0x01F0	96.875%
0x27	VOUT_TRANSITION_RATE	0xE850	10mV/µs
0x28	VOUT_DROOP	0x0019	2.5mΩ
0x29	VOUT_SCALE_LOOP	0xE808	1V/V
0x33	FREQUENCY_SWITCH	0x3804	600kHz
0x35	VIN_ON	0x0009	9V
0x36	VIN_OFF	0x0007	7.5V
0x40	VOUT_OV_FAULT_LIMIT	0x0266	120%
0x41	VOUT_OV_FAULT_RESPONSE	0x80	Latch off
0x42	VOUT_OV_WARN_LIMIT	0x0252	116%
0x43	VOUT_UV_WARN_LIMIT	0x01C3	88%
0x44	VOUT_UV_FAULT_LIMIT	0x0185	76%
0x45	VOUT_UV_FAULT_RESPONSE	0x42	Latch off, 64µs delay
0x46	IOUT_OC_FAULT_LIMIT	0x0018	24A
0x47	IOUT_OC_FAULT_RESPONSE	0x00	Continue operation without interruption with the valley current limiting the output current.
0x4A	IOUT_OC_WARN_LIMIT	0x1005	20A

Table 6-8. PMBus® Command Default Values (continued)

COMMAND CODE	COMMAND NAME	DEFAULT VALUE	DEFAULT BEHAVIOR
0x4F	OT_FAULT_LIMIT	0x1026	150°C (READ_TEMP based OTF does not assert in the TPS544B27W. Use SEL_OTF_BG for adjustable OTF.)
0x50	OT_FAULT_RESPONSE	0x80	Latch off
0x51	OT_WARN_LIMIT	0x101F	125°C (OTW does not assert in the TPS544B27W)
0x55	VIN_OV_FAULT_LIMIT	0x0808	16.5V
0x60	TON_DELAY	0xF801	0.5ms
0x61	TON_RISE	0xF801	0.5ms
0x64	TOFF_DELAY	0xF800	0ms
0x65	TOFF_FALL	0xF801	0.5ms
0x6B	PIN_OP_WARN_LIMIT	0x105A	360W
0x78	STATUS_BYTE	0x41	Current status
0x79	STATUS_WORD	0x0841	Current status
0x7A	STATUS_VOUT	0x00	Current status
0x7B	STATUS_IOUT	0x00	Current status
0x7C	STATUS_INPUT	0x00	Current status
0x7D	STATUS_TEMPERATURE	0x00	Current status
0x7E	STATUS_CML	0x00	Current status
0x7F	STATUS_OTHER	0x00	Current status
0x80	STATUS_MFR_SPECIFIC	0x00	Current status
0x88	READ_VIN	n/a	Sensed input voltage
0x89	READ_IIN	n/a	Sensed input current
0x8B	READ_VOUT	n/a	Sensed output voltage
0x8C	READ_IOUT	n/a	Sensed output current
0x8D	READ_TEMPERATURE_1	n/a	Sensed controller die temperature
0x97	READ_PIN	n/a	Sensed input power
0x98	PMBUS_REVISION	0x55	PMBus 1.4
0x99	MFR_ID	0x5449	ASCII for "TI"
0x9A	MFR_MODEL	0x0057	ASCII for "0W"
0x9B	MFR_REVISION	0x0000	All zeroes
0xAD	IC_DEVICE_ID	0x5449544B2700	IC part number
0xAE	IC_DEVICE_REV	0x32	IC revision
0xC7	EXTENDED_WRITE_PROTECT	0x0000	All commands are writable.
0xC8	DIE_ID	0x0000	Always 0
0xCD	NVM_PATCH_SPACE	0x0000000000	All zeroes
0xCF	CLOUD_OPTIONS	0x00	No write protection and no offset.
0xD0	SYS_CFG_USER1	0xC003	FCCM, PMBus control, SMB_ALERT#, Fixed OVF enabled with 0.9V threshold.
0xD1	SVID_ADDR_CFG_USER	0xC01B	SVID interface configuration options.
0xD2	PMBUS_ADDR	0x770E	PMB_ADDR set by pinstrap with pinstrap address bits 6:3 = 1110b.
0xD4	IMON_CAL	0x78	No calibration.
0xD5	COMP	0x5894540000	See command description.
0xD6	VBOOT_DCLL	0x19190A	Option 0 VDAC_BOOT = 0.4125V; SEL_OTF_BG set to 142°C; Option 0 and Option 1 DCLL = 2.5mΩ.
0xD7	VBOOT_OFFSET_1	0x000A	Option 1 VDAC_BOOT = 0.4125V.
0xD8	IIN_CAL	0x78	No calibration.

Table 6-8. PMBus® Command Default Values (continued)

COMMAND CODE	COMMAND NAME	DEFAULT VALUE	DEFAULT BEHAVIOR
0xDA	SVID_IMAX	0x8004	ICC_MAX = 20A, READ_IOUT exponent = -5d, PIN_SENSE_RES = 1mΩ
0xDB	SVID_EXT_CAPABILITY_VIDOMAX	0x0D7E	VIDO_MAX = 0x17E (1.077V)

7 Register Maps

7.1 PMBus® Transaction Types

Support for the following SMBus transaction types is mandatory. The use of PEC is optional.

Note that the Process Call and SMBus Block Write-Block Read Process Call transaction type contains a repeated start condition, which can not be compatible with all I^2C Controller device IP.

- Write Byte / Read Byte
- Write Word / Read Word
- Write Block / Read Block
- Send Byte / Receive Byte
- Block Write-Block Read Process Call (SMBALERT_MASK command for example)
- Process Call (SECURITY_BYTE command for example)

7.2 Conventions for Documenting Block Commands

According to the SMBus specification, block commands are transmitted across the PMBus interface in ascending order. The description below shows the convention this document follows for documenting block commands.

When block values are listed as register map tables, the block values are listed in byte order from top to bottom starting with Byte N and ending with Byte 1.

- Byte 1 (first byte sent) corresponds to bits 7:0.
- Byte 2 (second byte sent) corresponds to bits 15:8.
- Byte 3 (third byte sent) corresponds to bits 23:16.
- … and so on.

When block values are listed as text in hexadecimal, block values are listed in byte order, from left to right, starting with Byte N and ending with Byte 1 with a space between each byte of the value. For example, in block , the byte order returned in response to a Block Read is:

- Byte 1, bits 7:0 = 54h
- Byte 2, bits 15:8 = 49h
- Byte 3, bits 23:16 = 54h
- Byte 4, bits 31:24 = 4Bh
- Byte 5, bits 39:32 = 27h
- Byte 6, bits 47:40 = 00h

Figure 7-1. Block Command Byte Ordering

47	46	45	44	43	42	41	40
RW	RW	RW	RW	RW	RW	RW	RW
Byte N							
39	38	37	36	35	34	33	32
RW	RW	RW	RW	RW	RW	RW	RW
Byte …							
31	30	29	28	27	26	25	24
RW	RW	RW	RW	RW	RW	RW	RW
Byte 4							
23	22	21	20	19	18	17	16
RW	RW	RW	RW	RW	RW	RW	RW
Byte 3							
15	14	13	12	11	10	9	8

Figure 7-1. Block Command Byte Ordering (continued)

RW	RW	RW	RW	RW	RW	RW	RW
Byte 2							
7	6	5	4	3	2	1	0
RW	RW	RW	RW	RW	RW	RW	RW
Byte 1							

LEGEND: R/W = Read/Write; R = Read only

7.3 PMBus Commands

Section 7.3 lists the memory-mapped registers for the PMBus Command Map registers. All register offset addresses not listed in Section 7.3 should be considered as reserved locations and the register contents should not be modified.

Table 7-1. PMBus Commands

Address	Acronym	Register Name	Write Transaction	Read Transaction	Section
01h	OPERATION		Write Byte	Read Byte	Go
02h	ON_OFF_CONFIG		Write Byte	Read Byte	Go
03h	CLEAR_FAULTS		Send Byte	N/A	Go
0Eh	PASSKEY		Block Write	Block Read	Go
10h	WRITE_PROTECT		Write Byte	Read Byte	Go
15h	STORE_USER_ALL		Send Byte	N/A	Go
16h	RESTORE_USER_ALL		Send Byte	N/A	Go
19h	CAPABILITY		N/A	Read Byte	Go
1Bh	SMBALERT_MASK		Write Word	Block Write-Block Read Process Call	Go
20h	VOUT_MODE		N/A	Read Byte	Go
21h	VOUT_COMMAND		Write Word	Read Word	Go
22h	VOUT_TRIM		Write Word	Read Word	Go
24h	VOUT_MAX		N/A	Read Word	Go
25h	VOUT_MARGIN_HIGH		Write Word	Read Word	Go
26h	VOUT_MARGIN_LOW		Write Word	Read Word	Go
27h	VOUT_TRANSITION_RATE		Write Word	Read Word	Go
28h	VOUT_DROOP		N/A	Read Word	Go
29h	VOUT_SCALE_LOOP		Write Word	Read Word	Go
33h	FREQUENCY_SWITCH		Write Word	Read Word	Go
35h	VIN_ON		Write Word	Read Word	Go
36h	VIN_OFF		Write Word	Read Word	Go
40h	VOUT_OV_FAULT_LIMIT		Write Word	Read Word	Go
41h	VOUT_OV_FAULT_RESPONSE		Write Byte	Read Byte	Go
42h	VOUT_OV_WARN_LIMIT		Write Word	Read Word	Go
43h	VOUT_UV_WARN_LIMIT		Write Word	Read Word	Go
44h	VOUT_UV_FAULT_LIMIT		Write Word	Read Word	Go
45h	VOUT_UV_FAULT_RESPONSE		Write Byte	Read Byte	Go
46h	IOUT_OC_FAULT_LIMIT		Write Word	Read Word	Go
47h	IOUT_OC_FAULT_RESPONSE		N/A	Read Byte	Go
4Ah	IOUT_OC_WARN_LIMIT		Write Word	Read Word	Go
4Fh	OT_FAULT_LIMIT		Write Word	Read Word	Go
50h	OT_FAULT_RESPONSE		Write Byte	Read Byte	Go
51h	OT_WARN_LIMIT		Write Word	Read Word	Go
55h	VIN_OV_FAULT_LIMIT		Write Word	Read Word	Go
60h	TON_DELAY		Write Word	Read Word	Go
61h	TON_RISE		Write Word	Read Word	Go
64h	TOFF_DELAY		Write Word	Read Word	Go
65h	TOFF_FALL		Write Word	Read Word	Go

Table 7-1. PMBus Commands (continued)

Address	Acronym	Register Name	Write Transaction	Read Transaction	Section
6Bh	PIN_OP_WARN_LIMIT		Write Word	Read Word	Go
78h	STATUS_BYTE		N/A	Read Byte	Go
79h	STATUS_WORD		N/A	Read Word	Go
7Ah	STATUS_VOUT		Write Byte	Read Byte	Go
7Bh	STATUS_IOUT		Write Byte	Read Byte	Go
7Ch	STATUS_INPUT		Write Byte	Read Byte	Go
7Dh	STATUS_TEMPERATURE		Write Byte	Read Byte	Go
7Eh	STATUS_CML		Write Byte	Read Byte	Go
7Fh	STATUS_OTHER		Write Byte	Read Byte	Go
80h	STATUS_MFR_SPECIFIC		Write Byte	Read Byte	Go
88h	READ_VIN		N/A	Read Word	Go
89h	READ_IIN		N/A	Read Word	Go
8Bh	READ_VOUT		N/A	Read Word	Go
8Ch	READ_IOUT		N/A	Read Word	Go
8Dh	READ_TEMPERATURE_1		N/A	Read Word	Go
97h	READ_PIN		N/A	Read Word	Go
98h	PMBUS_REVISION		N/A	Read Byte	Go
99h	MFR_ID		N/A	Block Read	Go
9Ah	MFR_MODEL		Block Write	Block Read	Go
9Bh	MFR_REVISION		Block Write	Block Read	Go
ADh	IC_DEVICE_ID		N/A	Block Read	Go
AEh	IC_DEVICE_REV		N/A	Block Read	Go
C7h	EXTENDED_WRITE_PROTECT		Write Word	Read Word	Go
CDh	NVM_PATCH_SPACE		Block Write	Block Read	Go
CFh	CLOUD_OPTIONS		Write Byte	Read Byte	Go
D0h	SYS_CFG_USER1		Write Word	Read Word	Go
D1h	SVID_ADDR_CFG_USER		Write Word	Read Word	Go
D2h	PMBUS_ADDR		Write Word	Read Word	Go
D4h	IMON_CAL		Write Byte	Read Byte	Go
D5h	COMP		Block Write	Block Read	Go
D6h	VBOOT_DCLL		Block Write	Block Read	Go
D7h	VBOOT_OFFSET_1		Write Word	Read Word	Go
D8h	IIN_CAL		Write Byte	Read Byte	Go
DAh	SVID_IMAX		Write Word	Read Word	Go
DBh	SVID_EXT_CAPABILITY_VIDOMAX		Write Word	Read Word	Go
FCh	FUSION_ID0		N/A	Read Word	Go
FDh	FUSION_ID1		N/A	Block Read	Go

Complex bit access types are encoded to fit into small table cells. Section 7.3 shows the codes that are used for access types in this section.

Table 7-2. PMBus Command Map Access Type Codes

Access Type	Code	Description
Read Type		
R	R	Read
Write Type		
W	W	Write
W1C	W 1C	Write 1 to clear
Reset or Default Value		

Table 7-2. PMBus Command Map Access Type Codes (continued)

Access Type	Code	Description
-n		Value after reset or the default value

7.3.1 OPERATION (Address = 01h)

OPERATION is shown in Figure 7-2 and described in Table 7-3.

Return to the Summary Table.

Write Transaction: Write Byte
Read Transaction: Read Byte
Data Format: Unsigned Binary (1 byte)
NVM Back-up: No
Updates: On-the-fly

The OPERATION command is used to turn the device output on or off, in conjunction with the input from the EN pin, according to the configuration of the ON_OFF_CONFIG command. It is also used to set the output voltage to the upper or lower MARGIN levels, and select soft-stop when turned off through OPERATION.

Data Validity: Attempts to write 0b11XX, 0b0100, 0b0111, 0b1000, 0b1011 to MARGIN[3:0] or to write 1 to OPERATION[1] are considered as invalid data or unsupported data (ivd) and the device responds as described in the IVD bit in STATUS_CML.

Figure 7-2. OPERATION

7	6	5	4	3	2	1	0
ON	OFF	MARGIN[3:0]				OPERATION[1:0]	
R/W-0h	R/W-0h	R/W-1h				R-0h	

Table 7-3. OPERATION Field Descriptions

Bit	Field	Type	Reset	Description
7	ON	R/W	0h	Turn the device output on or off when the ON_OFF_CONFIG command is configured with its CMD bit high. There can be several other requirements that must be satisfied before the power conversion can begin. The input voltages must be above their UVLO thresholds and, if the CPR bit in ON_OFF_CONFIG is high, the enable pin must be high. 0h = The device output is off 1h = The device output is on
6	OFF	R/W	0h	Sets the turn-off behavior when commanding the device output off via OPERATION[7] (the ON bit transitions from 1 to 0) and when the ON_OFF_CONFIG command is configured with its CMD bit high. If the ON bit is 1, then the OFF bit is ignored. 0h = Immediately turn the device output off forcing the power stage to a high-Z state, not honoring the programmed TOFF_DELAY and programmed TOFF_FALL, when commanded off via OPERATION[7]. 1h = Soft off. Use the programmed turn-off delay in TOFF_DELAY and ramp down in TOFF_FALL when commanded off via OPERATION[7].
5:2	MARGIN[3:0]	R/W	1h	Sets the margin state, independent of the OPERATION[7] bit value. Values other than those listed below are invalid/unsupported data. If margin is off, the output voltage source is VOUT_COMMAND and OV/UV faults behave normally as programmed in their respective fault response registers. 0h = Margin off and faults behave as programmed. 1h = Margin off and faults behave as programmed. 2h = Margin off and faults behave as programmed. 3h = Margin off and faults behave as programmed. 5h = Margin low (Ignore fault). Output voltage target uses VOUT_MARGIN_LOW. UV faults are ignored and do not trigger shut-down, but will trigger STATUS updates. 6h = Margin low (Act on fault). Output voltage target uses VOUT_MARGIN_LOW. OV/UV faults trigger per their respective fault response settings. 9h = Margin high (Ignore fault). Output voltage target uses VOUT_MARGIN_HIGH. OV faults are ignored and do not trigger shut-down, but will trigger STATUS updates. Ah = Margin high (Act on fault). Output voltage target uses VOUT_MARGIN_HIGH. OV/UV faults trigger per their respective fault response settings.
1:0	OPERATION[1:0]	R	0h	Reserved.

7.3.2 ON_OFF_CONFIG (Address = 02h)

ON_OFF_CONFIG is shown in Figure 7-3 and described in Table 7-4.

Return to the Summary Table.

Write Transaction: Write Byte
Read Transaction: Read Byte
Data Format: Unsigned Binary (1 byte)
NVM Back-up: EEPROM
Updates: On-the-fly

The ON_OFF_CONFIG command configures the combination of enable pin input and serial bus commands needed to turn the device output on and off. This includes how the unit responds when power is applied to VIN. For the purposes of ON_OFF_CONFIG, the device EN pin is the CONTROL pin.

Data Validity: Attempts to write any unsupported values (e.g. ON_OFF_CONFIG[7:5] != 3b000 or POL = 0) are considered as invalid data or unsupported data (ivd) and the device responds as described in the IVD bit in STATUS_CML.

Figure 7-3. ON_OFF_CONFIG

7	6	5	4	3	2	1	0
RESERVED	RESERVED	RESERVED	PU	CMD	CPR	POL	CPA
R-0h	R-0h	R-0h	R/W-Xh	R/W-Xh	R/W-Xh	R-1h	R/W-Xh

Table 7-4. ON_OFF_CONFIG Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R	0h	
6	RESERVED	R	0h	
5	RESERVED	R	0h	
4	PU	R/W	X	Sets the default to either turn on the device output any time power is present, or for the device output on and off to be controlled by the CONTROL pin and/or the OPERATION command. 0h = Device output turns on any time sufficient input power is present regardless of state of the CONTROL pin or OPERATION command. 1h = Device output does not turn on until commanded by the CONTROL pin and/or OPERATION command as programmed in bits [3:0] of the ON_OFF_CONFIG command.
3	CMD	R/W	X	The CMD bit sets how the device responds to the OPERATION command. 0h = Device ignores the ON bit in the OPERATION command. 1h = Device responds to the ON bit being set high in the OPERATION command (and the CONTROL pin if configured by CPR) to enable the device output.
2	CPR	R/W	X	The CPR bit sets the CONTROL pin response. 0h = Device ignores the CONTROL pin to enable its output. 1h = The device output responds to the CONTROL pin.
1	POL	R	1h	The POL bit sets the polarity of the CONTROL pin. 1h = The CONTROL pin has active high polarity.
0	CPA	R/W	X	The CPA bit sets the CONTROL pin action when the device output is turned off with the CONTROL pin. The device must be configured to respond to the CONTROL pin through the CPR bit. 0h = When the output is turned off by the CONTROL pin, continue regulating for the time programmed into TOFF_DELAY and ramp down in the time programmed into TOFF_FALL. 1h = When the output is turned off by the CONTROL pin, immediately turn off the output.

7.3.3 CLEAR_FAULTS (Address = 03h)

Return to the Summary Table.

CMD Address	03h
Write Transaction:	Send Byte
Read Transaction:	N/A
Format:	Data-less
NVM Back-up:	No
Updates:	On-the-fly

CLEAR_FAULTS is a command used to clear all bits in all status registers and deassert the SMB_ALERT# signal if currently asserted. This write-only command requires no data byte.

The CLEAR_FAULTS command does not restart a unit that has latched off due to a fault condition. If a fault condition persists after clearing, the device immediately re-sets the corresponding fault bit and notifies the host through the configured notification method.

Note

Read operations to command address 03h (such as Read Byte) will also trigger a CLEAR_FAULTS operation.

7.3.4 PASSKEY (Address = 0Eh)

PASSKEY is shown in Figure 7-4 and described in Table 7-5.

Return to the Summary Table.

Write Transaction: Block Write
Read Transaction: Block Read
Data Format: Writes Unsigned Binary (4 bytes); Reads Unsigned Binary (3 bytes)
NVM Back-up: EEPROM
Updates: On-the-fly. STORE_USER_ALL then power on reset required for the PASSKEY to be locked.

The PMBus 1.5 standard command PASSKEY provides a customer with the ability to lock access to (C7h) EXTENDED_WRITE_PROTECT with a user programmed up to 32-bit passkey. PASSKEY will accept fewer or more bytes on a write without NACKing or an invalid data response.

Writing a non-zero value using PASSKEY will lock write access to EXT_WRITE_PROTECT only after sending a STORE_USER_ALL command and performing a power on reset, or sending a RESTORE_USER_ALL command.

In any PASSKEY state the user can read a total of 3 bytes from PASSKEY, with the 2 additional bytes being a user option reporting a NVM_CHECKSUM value based on the contents of the non-volatile memory.

Data Validity: Writes between 2 and 8 bytes will be acknowledged. Any other number of bytes are considered as invalid data. Additionally when the PASSKEY is set but unlocked, writes to PASSKEY other than all bytes 00h or the current PASSKEY are considered as invalid data. In both cases the device responds as described in the IVD bit in STATUS_CML.

Figure 7-4. PASSKEY

23	22	21	20	19	18	17	16
NVM_CHECKSUM[15:0]							
R-0h							
15	14	13	12	11	10	9	8
NVM_CHECKSUM[15:0]							
R-0h							
7	6	5	4	3	2	1	0
RESERVED	RESERVED	RESERVED	PASSKEY_LOCK	PASSKEY_ATTEMPTS[3:0]			
R-0h	R-0h	R-0h	R-0h	R-0h			

Table 7-5. PASSKEY Field Descriptions

Bit	Field	Type	Reset	Description
23:8	NVM_CHECKSUM[15:0]	R	0h	NVM_CHECKSUM reports the CRC-16 (polynomial 0x8005) checksum for the current NVM settings. The PASSKEY NVM bits are excluded from the checksum to prevent a malicious actor from reading the device configuration and repeatedly setting PASSKEY values in an attempt to discover the PASSKEY value.
7	RESERVED	R	0h	
6	RESERVED	R	0h	
5	RESERVED	R	0h	
4	PASSKEY_LOCK	R	0h	This bit reflects the lock status if the PASSKEY. 0h = PASSKEY is unlocked or set. 1h = PASSKEY is locked. Writes to EXTENDED_WRITE_PROTECT are blocked by the PASSKEY.
3:0	PASSKEY_ATTEMPTS[3:0]	R	0h	This bit returns the number of invalid PASSKEY write attempts to unlock PASSKEY. After 3 invalid attempts a power on reset is required for further attempts. 0h = No invalid attempts 1h = One invalid attempt 2h = Two invalid attempts Fh = Three or more invalid attempts

7.3.5 WRITE_PROTECT (Address = 10h)

WRITE_PROTECT is shown in Figure 7-5 and described in Table 7-6.

Return to the Summary Table.

Write Transaction: Write Byte
Read Transaction: Read Byte
Data Format: unsigned binary (1 byte)
NVM Back-up: EEPROM
Updates: On-the-fly

The WRITE_PROTECT command is used to control writing to the PMBus device. The intent of this command is to provide protection against accidental changes. This command is not intended to provide protection against deliberate or malicious changes to a device's configuration or operation. Supported commands may have their parameters read regardless of the WRITE_PROTECT settings, with one exception. Commands using a Process Call or Block Write-Block Read Process call to read their parameters cannot have their parameters read. The write portion of these transactions is blocked preventing their parameters from being read.

Data Validity: Attempts to write values not specified or attempts to enable write protection through both PROTECTION and PROTECTION_MFR at the same time are considered as invalid data or unsupported data (ivd) and the device responds as described in the IVD bit in STATUS_CML. The only valid values are 0x00, 0x02, 0x03, 0x20, 0x40 and 0x80.

Figure 7-5. WRITE_PROTECT

7	6	5	4	3	2	1	0
PROTECTION[2:0]			RESERVED	RESERVED	RESERVED	PROTECTION_MFR[1:0]	
R/W-Xh			R-0h	R-0h	R-0h	R/W-0h	

Table 7-6. WRITE_PROTECT Field Descriptions

Bit	Field	Type	Reset	Description
7:5	PROTECTION[2:0]	R/W	X	This bit field sets PMBus standard write protection levels. 0h = No write protection. 1h = Disable all writes except for the WRITE_PROTECT, STORE_USER_ALL, OPERATION, ON_OFF_CONFIG, and VOUT_COMMAND commands. 2h = Disable all writes except for the WRITE_PROTECT, STORE_USER_ALL, and OPERATION commands. 4h = Disable all writes except for the WRITE_PROTECT and STORE_USER_ALL commands.
4	RESERVED	R	0h	
3	RESERVED	R	0h	
2	RESERVED	R	0h	
1:0	PROTECTION_MFR[1:0]	R/W	0h	0h = No manufacturer specific write protection. 2h = Disables writes to all PMBus commands except VOUT_COMMAND (requires power-cycle to restore write access) 3h = Disables writes to all PMBus commands (requires power-cycle to restore write access)

7.3.6 STORE_USER_ALL (Address = 15h)

Return to the Summary Table.

CMD Address	15h
Write Transaction:	Send Byte
Read Transaction:	N/A
Format:	Data-less
NVM Back-up:	No
Updates:	Not recommended for on-the-fly-use, but not explicitly blocked

The STORE_USER_ALL command instructs the PMBus device to copy the entire contents of the Operating Memory to the matching locations in the non-volatile User Store Memory. Any items in Operating Memory that do not have matching locations in the User Store Memory are ignored.

CAUTION

NVM store operations are not recommended while the output is enabled. Although not explicitly prevented, interruption during this process can result in corrupted NVM data. TI recommends disabling regulation and waiting a minimum of 125ms after issuing NVM store operations before continuing with other operations. EEPROM programming faults due to corrupted NVM will cause the device to assert STATUS_CML[1].

Note

Read operations to command address 15h (such as Read Byte) will also trigger a STORE_USER_ALL operation.

7.3.7 RESTORE_USER_ALL (Address = 16h)

Return to the Summary Table.

CMD Address	16h
Write Transaction:	Send Byte
Read Transaction:	N/A
Format:	Data-less
NVM Back-up:	No
Updates:	Not recommended for on-the-fly-use, but not explicitly blocked

The RESTORE_USER_ALL command instructs the PMBus device to copy the entire contents of the non-volatile User Store Memory to the matching locations in the Operating Memory.

While technically permitted, using the RESTORE_USER_ALL command when output is enabled can lead to unpredictable, undesirable, or even catastrophic results. TI strongly recommends turning the device output off (using the method programmed into ON_OFF_CONFIG) before issuing this command.

Note

1. RESTORE_USER_ALL while the output is enabled causes the device will NACK the next write attempt. Until receiving one write attempt, the device will NACK reads to most commands. After one write attempt, normal operation resumes for all writes and reads.
2. Read operations to command address 16h (such as Read Byte) will also trigger an NVM restore operation.
3. RESTORE_USER_ALL causes the device to assert STATUS_INPUT[3] (LOW_VIN) and STATUS_MFR_SPECIFIC[5] (PS_FAULT).

7.3.8 CAPABILITY (Address = 19h)

CAPABILITY is shown in Figure 7-6 and described in Table 7-7.

Return to the Summary Table.

Write Transaction: N/A
Read Transaction: Read Byte
Data Format: unsigned binary (1 byte)
NVM Back-up: No
Updates: N/A

This command provides a way for the host to determine the capabilities of this PMBus device. This command is read-only and has one data byte formatted as below.

Figure 7-6. CAPABILITY

7	6	5	4	3	2	1	0
PEC	SPD[1:0]		ALRT	FORMAT	AVS	RESERVED	RESERVED
R-1h	R-2h		R-1h	R-0h	R-0h	R-0h	R-0h

Table 7-7. CAPABILITY Field Descriptions

Bit	Field	Type	Reset	Description
7	PEC	R	1h	1h = Packet Error Checking is supported.
6:5	SPD[1:0]	R	2h	2h = Maximum supported bus speed is 1MHz.
4	ALRT	R	1h	1h = This device has an SMB_ALERT# pin and supports the SMBus Alert Response Protocol.
3	FORMAT	R	0h	0h = Numeric format is LINEAR11, ULINEAR16, SLINEAR16, or DIRECT format.
2	AVS	R	0h	0h = AVSBus is NOT supported.
1	RESERVED	R	0h	
0	RESERVED	R	0h	

7.3.9 SMBALERT_MASK (Address = 1Bh)

Return to the Summary Table.

CMD Address:	1Bh
Write Transaction:	Write Word
Read Transaction:	Block Write-Block Read Process Call
Format:	Write: Unsigned Binary (2 bytes) Read: Unsigned Binary (1 byte)
NVM Back-up:	EEPROM
Updates:	On-the-fly

The SMBALERT_MASK command can be used to prevent a warning or fault condition from asserting the SMB_ALERT# signal. Setting a MASK bit does not prevent the associated bit in the STATUS_x command from being set, but prevents the associated bit in the STATUS_x command from asserting SMB_ALERT#. The following register descriptions describe the individual mask bits available.

SMBALERT_MASK write transaction is Write Word with the following:

- CMD Address = 1Bh
- Write Data Byte Low = STATUS_x COMMAND CODE
- Write Data Byte High = STATUS_x MASK

SMBALERT_MASK read transaction is a Block Write-Block Read Process Call with the following:

- CMD Address = 1Bh
- Byte Count = 1
- Write Data Byte = STATUS_x COMMAND CODE
- Byte Count = 1
- Read Data Byte = STATUS_x MASK

Please refer to the PMBus 1.3.1 Part II specification, section 15.38 SMBALERT_MASK Command for further details on this command, and the SMBus 3.1 specification, section 6.5.8 Block Write-Block Read Process Call for further details on the process call transaction.

7.3.10 SMBALERT_MASK Registers

Section 7.3.10 lists the memory-mapped registers for the SMBALERT_MASK registers. All register offset addresses not listed in Section 7.3.10 should be considered as reserved locations and the register contents should not be modified.

Table 7-8. SMBALERT_MASK Registers

Address	Acronym	Register Name	Section
78h	ALERT_MASK_BYTE		Go
79h	ALERT_MASK_WORD		Go
7Ah	ALERT_MASK_VOUT		Go
7Bh	ALERT_MASK_IOUT		Go
7Ch	ALERT_MASK_INPUT		Go
7Dh	ALERT_MASK_TEMPERATURE		Go
7Eh	ALERT_MASK_CML		Go
7Fh	ALERT_MASK_OTHER		Go
80h	ALERT_MASK_MFR_SPECIFIC		Go
CEh	ALERT_MASK_PULSE_CATCHER		Go

Complex bit access types are encoded to fit into small table cells. Section 7.3.10 shows the codes that are used for access types in this section.

Table 7-9. SMBALERT_MASK Access Type Codes

Access Type	Code	Description
Read Type		

Table 7-9. SMBALERT_MASK Access Type Codes (continued)

Access Type	Code	Description
R	R	Read
Write Type		
W	W	Write
Reset or Default Value		
-n		Value after reset or the default value

7.3.10.1 ALERT_MASK_BYTE (Address = 78h) [Reset = C8h]

ALERT_MASK_BYTE is shown in Figure 7-7 and described in Table 7-10.

Return to the Summary Table.

Figure 7-7. ALERT_MASK_BYTE

7	6	5	4	3	2	1	0
UNSUPPORTED_7	UNSUPPORTED_6	MASK_STS_OVF	MASK_STS_OCF	UNSUPPORTED_3	MASK_STS_OTFW	MASK_STS_CML	MASK_STS_OTH
R-1b	R-1b	R/W-0b	R/W-0b	R-1b	R/W-0b	R/W-0b	R/W-0b

Table 7-10. ALERT_MASK_BYTE Field Descriptions

Bit	Field	Type	Reset	Description
7	UNSUPPORTED_7	R	1b	Unsupported so always masked.
6	UNSUPPORTED_6	R	1b	Unsupported so always masked.
5	MASK_STS_OVF	R/W	0b	
4	MASK_STS_OCF	R/W	0b	
3	UNSUPPORTED_3	R	1b	Unsupported so always masked.
2	MASK_STS_OTFW	R/W	0b	
1	MASK_STS_CML	R/W	0b	
0	MASK_STS_OTH	R/W	0b	

7.3.10.2 ALERT_MASK_WORD (Address = 79h) [Reset = 0Dh]

ALERT_MASK_WORD is shown in Figure 7-8 and described in Table 7-11.

Return to the Summary Table.

Figure 7-8. ALERT_MASK_WORD

7	6	5	4	3	2	1	0
MASK_STS_VFW	MASK_STS_OCFW	MASK_STS_INPUT	MASK_STS_MFR	UNSUPPORTED_3	UNSUPPORTED_2	MASK_STS_OTHER	UNSUPPORTED_0
R/W-0b	R/W-0b	R/W-0b	R/W-0b	R-1b	R-1b	R/W-0b	R-1b

Table 7-11. ALERT_MASK_WORD Field Descriptions

Bit	Field	Type	Reset	Description
7	MASK_STS_VFW	R/W	0b	
6	MASK_STS_OCFW	R/W	0b	
5	MASK_STS_INPUT	R/W	0b	
4	MASK_STS_MFR	R/W	0b	
3	UNSUPPORTED_3	R	1b	Unsupported so always masked.
2	UNSUPPORTED_2	R	1b	Unsupported so always masked.
1	MASK_STS_OTHER	R/W	0b	
0	UNSUPPORTED_0	R	1b	Unsupported so always masked.

7.3.10.3 ALERT_MASK_VOUT (Address = 7Ah) [Reset = XXh]

ALERT_MASK_VOUT is shown in Figure 7-9 and described in Table 7-12.

Return to the Summary Table.

Figure 7-9. ALERT_MASK_VOUT

7	6	5	4	3	2	1	0
MASK_OVF	MASK_OVW	MASK_UVW	MASK_UVF	MASK_VO_MAX_MIN_W	UNSUPPORTED_2	UNSUPPORTED_1	UNSUPPORTED_0
R/W-xb	R/W-xb	R/W-xb	R/W-xb	R/W-xb	R-1b	R-1b	R-1b

Table 7-12. ALERT_MASK_VOUT Field Descriptions

Bit	Field	Type	Reset	Description
7	MASK_OVF	R/W	xb	On reset the value will be determined by NVM.
6	MASK_OVW	R/W	xb	On reset the value will be determined by NVM.
5	MASK_UVW	R/W	xb	On reset the value will be determined by NVM.
4	MASK_UVF	R/W	xb	On reset the value will be determined by NVM.
3	MASK_VO_MAX_MIN_W	R/W	xb	On reset the value will be determined by NVM.
2	UNSUPPORTED_2	R	1b	Unsupported so always masked.
1	UNSUPPORTED_1	R	1b	Unsupported so always masked.
0	UNSUPPORTED_0	R	1b	Unsupported so always masked.

7.3.10.4 ALERT_MASK_IOUT (Address = 7Bh) [Reset = XFh]

ALERT_MASK_IOUT is shown in Figure 7-10 and described in Table 7-13.

Return to the Summary Table.

Figure 7-10. ALERT_MASK_IOUT

7	6	5	4	3	2	1	0
MASK_OCF	MASK_OCUV	MASK_OCW	MASK_UCF	UNSUPPORTED_3	UNSUPPORTED_2	UNSUPPORTED_1	UNSUPPORTED_0
R/W-xb	R-1b	R/W-xb	R/W-xb	R-1b	R-1b	R-1b	R-1b

Table 7-13. ALERT_MASK_IOUT Field Descriptions

Bit	Field	Type	Reset	Description
7	MASK_OCF	R/W	xb	On reset the value will be determined by NVM.
6	MASK_OCUV	R	1b	
5	MASK_OCW	R/W	xb	On reset the value will be determined by NVM.
4	MASK_UCF	R/W	xb	On reset the value will be determined by NVM.
3	UNSUPPORTED_3	R	1b	Unsupported so always masked.
2	UNSUPPORTED_2	R	1b	Unsupported so always masked.
1	UNSUPPORTED_1	R	1b	Unsupported so always masked.
0	UNSUPPORTED_0	R	1b	Unsupported so always masked.

7.3.10.5 ALERT_MASK_INPUT (Address = 7Ch) [Reset = XXh]

ALERT_MASK_INPUT is shown in Figure 7-11 and described in Table 7-14.

Return to the Summary Table.

Figure 7-11. ALERT_MASK_INPUT

7	6	5	4	3	2	1	0
MASK_PVIN_OVF	UNSUPPORTED_6	UNSUPPORTED_5	UNSUPPORTED_4	MASK_LOW_VIN	UNSUPPORTED_2	UNSUPPORTED_1	MASK_PIN_OPW
R/W-xb	R-1b	R-1b	R-1b	R/W-xb	R-1b	R-1b	R/W-xb

Table 7-14. ALERT_MASK_INPUT Field Descriptions

Bit	Field	Type	Reset	Description
7	MASK_PVIN_OVF	R/W	xb	On reset the value will be determined by NVM.
6	UNSUPPORTED_6	R	1b	Unsupported so always masked.
5	UNSUPPORTED_5	R	1b	Unsupported so always masked.
4	UNSUPPORTED_4	R	1b	Unsupported so always masked.
3	MASK_LOW_VIN	R/W	xb	On reset the value will be determined by NVM.
2	UNSUPPORTED_2	R	1b	Unsupported so always masked.
1	UNSUPPORTED_1	R	1b	Unsupported so always masked.
0	MASK_PIN_OPW	R/W	xb	On reset the value will be determined by NVM.

7.3.10.6 ALERT_MASK_TEMPERATURE (Address = 7Dh) [Reset = XFh]

ALERT_MASK_TEMPERATURE is shown in Figure 7-12 and described in Table 7-15.

Return to the Summary Table.

Figure 7-12. ALERT_MASK_TEMPERATURE

7	6	5	4	3	2	1	0
MASK_OT_PROG	MASK_OTW_PROG	UNSUPPORTED_5	UNSUPPORTED_4	UNSUPPORTED_3	UNSUPPORTED_2	UNSUPPORTED_1	UNSUPPORTED_0
R/W-xb	R/W-xb	R-1b	R-1b	R-1b	R-1b	R-1b	R-1b

Table 7-15. ALERT_MASK_TEMPERATURE Field Descriptions

Bit	Field	Type	Reset	Description
7	MASK_OT_PROG	R/W	xb	On reset the value will be determined by NVM.
6	MASK_OTW_PROG	R/W	xb	On reset the value will be determined by NVM.
5	UNSUPPORTED_5	R	1b	Unsupported so always masked.
4	UNSUPPORTED_4	R	1b	Unsupported so always masked.
3	UNSUPPORTED_3	R	1b	Unsupported so always masked.
2	UNSUPPORTED_2	R	1b	Unsupported so always masked.
1	UNSUPPORTED_1	R	1b	Unsupported so always masked.
0	UNSUPPORTED_0	R	1b	Unsupported so always masked.

7.3.10.7 ALERT_MASK_CML (Address = 7Eh) [Reset = XXh]

ALERT_MASK_CML is shown in Figure 7-13 and described in Table 7-16.

Return to the Summary Table.

Figure 7-13. ALERT_MASK_CML

7	6	5	4	3	2	1	0
MASK_IVC	MASK_IVD	MASK_PEC	MASK_MEM	UNSUPPORTED_3	UNSUPPORTED_2	MASK_OTH	UNSUPPORTED_0
R/W-xb	R/W-xb	R/W-xb	R/W-xb	R-1b	R-1b	R/W-xb	R-1b

Table 7-16. ALERT_MASK_CML Field Descriptions

Bit	Field	Type	Reset	Description
7	MASK_IVC	R/W	xb	On reset the value will be determined by NVM.
6	MASK_IVD	R/W	xb	On reset the value will be determined by NVM.
5	MASK_PEC	R/W	xb	On reset the value will be determined by NVM.
4	MASK_MEM	R/W	xb	On reset the value will be determined by NVM.
3	UNSUPPORTED_3	R	1b	Unsupported so always masked.
2	UNSUPPORTED_2	R	1b	Unsupported so always masked.
1	MASK_OTH	R/W	xb	On reset the value will be determined by NVM.
0	UNSUPPORTED_0	R	1b	Unsupported so always masked.

7.3.10.8 ALERT_MASK_OTHER (Address = 7Fh) [Reset = XFh]

ALERT_MASK_OTHER is shown in Figure 7-14 and described in Table 7-17.

Return to the Summary Table.

Figure 7-14. ALERT_MASK_OTHER

7	6	5	4	3	2	1	0
MASK_ACT_CMPLT	UNSUPPORTED_6	UNSUPPORTED_5	UNSUPPORTED_4	UNSUPPORTED_3	UNSUPPORTED_2	UNSUPPORTED_1	UNSUPPORTED_0
R/W-xb	R-1b	R-1b	R-1b	R-1b	R-1b	R-1b	R-1b

Table 7-17. ALERT_MASK_OTHER Field Descriptions

Bit	Field	Type	Reset	Description
7	MASK_ACT_CMPLT	R/W	xb	On reset the value will be determined by NVM.
6	UNSUPPORTED_6	R	1b	Unsupported so always masked.
5	UNSUPPORTED_5	R	1b	Unsupported so always masked.
4	UNSUPPORTED_4	R	1b	Unsupported so always masked.
3	UNSUPPORTED_3	R	1b	Unsupported so always masked.
2	UNSUPPORTED_2	R	1b	Unsupported so always masked.
1	UNSUPPORTED_1	R	1b	Unsupported so always masked.
0	UNSUPPORTED_0	R	1b	Unsupported so always masked.

7.3.10.9 ALERT_MASK_MFR_SPECIFIC (Address = 80h) [Reset = XXh]

ALERT_MASK_MFR_SPECIFIC is shown in Figure 7-15 and described in Table 7-18.

Return to the Summary Table.

Figure 7-15. ALERT_MASK_MFR_SPECIFIC

7	6	5	4	3	2	1	0
UNSUPPORTED_7	MASK_OTF_BG	MASK_PS_FLT	MASK_PS_COMM_WRN	MASK_PC	UNSUPPORTED_2	MASK_PS_OT	MASK_VDRV_UV
R-1b	R/W-xb	R/W-xb	R/W-xb	R/W-1b	R-1b	R/W-xb	R/W-xb

Table 7-18. ALERT_MASK_MFR_SPECIFIC Field Descriptions

Bit	Field	Type	Reset	Description
7	UNSUPPORTED_7	R	1b	Unsupported so always masked.
6	MASK_OTF_BG	R/W	xb	On reset the value will be determined by NVM.
5	MASK_PS_FLT	R/W	xb	On reset the value will be determined by NVM.
4	MASK_PS_COMM_WRN	R/W	xb	On reset the value will be determined by NVM.
3	MASK_PC	R/W	1b	
2	UNSUPPORTED_2	R	1b	Unsupported so always masked.
1	MASK_PS_OT	R/W	xb	On reset the value will be determined by NVM.
0	MASK_VDRV_UV	R/W	xb	On reset the value will be determined by NVM.

7.3.10.10 ALERT_MASK_PULSE_CATCHER (Address = CEh) [Reset = FXh]

ALERT_MASK_PULSE_CATCHER is shown in Figure 7-16 and described in Table 7-19.

Return to the Summary Table.

Figure 7-16. ALERT_MASK_PULSE_CATCHER

7	6	5	4	3	2	1	0
UNSUPPORTED_7	UNSUPPORTED_6	UNSUPPORTED_5	UNSUPPORTED_4	MASK_CH3_INT	MASK_CH2_INT	MASK_CH1_INT	MASK_CH0_INT
R-1b	R-1b	R-1b	R-1b	R/W-1b	R/W-xb	R/W-1b	R/W-xb

Table 7-19. ALERT_MASK_PULSE_CATCHER Field Descriptions

Bit	Field	Type	Reset	Description
7	UNSUPPORTED_7	R	1b	Unsupported so always masked.
6	UNSUPPORTED_6	R	1b	Unsupported so always masked.
5	UNSUPPORTED_5	R	1b	Unsupported so always masked.
4	UNSUPPORTED_4	R	1b	Unsupported so always masked.
3	MASK_CH3_INT	R/W	1b	
2	MASK_CH2_INT	R/W	xb	On reset the value will be determined by NVM.
1	MASK_CH1_INT	R/W	1b	
0	MASK_CH0_INT	R/W	xb	On reset the value will be determined by NVM.

7.3.11 VOUT_MODE (Address = 20h)

VOUT_MODE is shown in Figure 7-17 and described in Table 7-20.

Return to the Summary Table.

Write Transaction: N/A
Read Transaction: Read Byte
Data Format: unsigned binary (1 byte)
NVM Back-up: No
Updates: N/A

The data byte for the VOUT_MODE command sets the data format for VOUT related commands.

Data Validity: Attempts to write the VOUT_MODE command are considered as invalid data or unsupported data (ivd) and the device responds as described in the IVD bit in STATUS_CML.

Figure 7-17. VOUT_MODE

7	6	5	4	3	2	1	0
VOUT_MODE[2:0]			VOUT_EXPONENT[4:0]				
R-4h			R-17h				

Table 7-20. VOUT_MODE Field Descriptions

Bit	Field	Type	Reset	Description
7:5	VOUT_MODE[2:0]	R	4h	Bit 2 value of 1 indicates relative data format for VOUT related commands, such as VOUT_OV_FAULT_LIMIT and VOUT_UV_FAULT_LIMIT. Bits 1:0 indicate linear format (ULINEAR16, SLINEAR16)
4:0	VOUT_EXPONENT[4:0]	R	17h	Specifies the exponent to use with output voltage related commands in two's complement format. Value is fixed at -9 (1.953mV/LSB).

7.3.12 VOUT_COMMAND (Address = 21h)

VOUT_COMMAND is shown in Figure 7-18 and described in Table 7-21.

Return to the Summary Table.

Write Transaction: Write Word
Read Transaction: Read Word
Data Format: Direct 1mV LSB
NVM Back-up: No
Updates: On-the-fly

When the PMBus interface is in control of the output, writes to VOUT_COMMAND cause the device to set its output voltage to the commanded value. Output voltage changes due to VOUT_COMMAND occur at the rate specified by VOUT_TRANSITION_RATE.

This command can be written during soft-start or soft-stop. However, the output will continue to ramp up/down to the original target (VBOOT) at the rate programmed into TON_RISE/TOFF_FALL. After soft-start completes (and if VOUT_COMMAND is different from the VBOOT value), the device will immediately transition from the VBOOT value to the latest written VOUT_COMMAND at the programmed VOUT_TRANSITION_RATE. Writes to VOUT_COMMAND during soft-stop will be acknowledged, however, no transition will occur and VOUT_COMMAND will get automatically updated back to VBOOT at the conclusion of soft-stop.

During regulation, preemptive writes to VOUT_COMMAND are allowed even if the output is still slewing to a previously programmed VOUT_COMMAND. The device will immediately start slewing to the new target at the rate programmed into VOUT_TRANSITION_RATE.

Figure 7-18. VOUT_COMMAND

15	14	13	12	11	10	9	8
RESERVED	RESERVED	RESERVED	VOUT_COMMAND[12:0]				
R-0h	R-0h	R-0h	R/W-XXXh				
7	6	5	4	3	2	1	0
VOUT_COMMAND[12:0]							
R/W-XXXh							

Table 7-21. VOUT_COMMAND Field Descriptions

Bit	Field	Type	Reset	Description
15	RESERVED	R	0h	
14	RESERVED	R	0h	
13	RESERVED	R	0h	
12:0	VOUT_COMMAND[12:0]	R/W	X	The VOUT_COMMAND reset value is determined by VOUT_SCALE_LOOP and VBOOT_0 or VBOOT_1. Note two important details: when writing to VOUT_COMMAND, the LSB does not match the VOUT_MODE setting and instead uses Direct format with a 1mV LSB, and the reset read value uses a 2mV LSB resulting in the device returning half the actual VBOOT voltage value upon a read. After the command is written to, a read of VOUT_COMMAND returns the value written.

7.3.13 VOUT_TRIM (Address = 22h)

VOUT_TRIM is shown in Figure 7-19 and described in Table 7-22.

Return to the Summary Table.

Write Transaction: Write Word
Read Transaction: Read Word
Data Format: VOUT_CTRL = 0b00, signed 5mV LSB; VOUT_CTRL = 0b01 or 0b10, SLINEAR16 1.953mV LSB per VOUT_MODE
NVM Back-up: EEPROM
Updates: VOUT_CTRL = 0b00 or 0b01, output must be disabled to take effect; VOUT_CTRL = 0b10, On-the-fly

The VOUT_TRIM command is used to apply a fixed offset voltage to the output voltage command value. It is typically used by the end user to trim the output voltage at the time the PMBus device is assembled into the end user's system. Output voltage changes due to VOUT_TRIM occur at the rate specified by VOUT_TRANSITION_RATE.

Data Validity: Attempts to write the read-only bits (VOUT_TRIM[15:7]) to a different value than the sign bit (VOUT_TRIM[6]) are considered as invalid data or unsupported data (ivd) and the device responds as described in the IVD bit in STATUS_CML. The signed value of the full 16 bits is being validated.

Figure 7-19. VOUT_TRIM

15	14	13	12	11	10	9	8
VOUT_TRIM_SIGN_EXT[8:0]							
R-0h							
7	6	5	4	3	2	1	0
VOUT_TRIM_SIGN_EXT[8:0]	VOUT_TRIM[6:0]						
R-0h	R/W-Xh						

Table 7-22. VOUT_TRIM Field Descriptions

Bit	Field	Type	Reset	Description
15:7	VOUT_TRIM_SIGN_EXT[8:0]	R	0h	The 9 MSBs are read only limiting the range of VOUT_TRIM that can be programmed. Their value is set through sign extension of bit 6. Writes to the VOUT_TRIM command must set VOUT_TRIM_SIGN_EXT to the same value as bit 6.
6:0	VOUT_TRIM[6:0]	R/W	X	Output voltage offset. If VOUT_CTRL = 0b00, this functions as OFFSET_0 selected through PMB_ADDR pinstrap and the binary value directly sets the SVID register OFFSET resulting in a 5mV or 10mV LSB depending on the PROTOCOL_ID selected in the configuration. If VOUT_CTRL = 0b01 or 0b10, VOUT_TRIM always adds offset to the output with an LSB determined by VOUT_MODE.

7.3.14 VOUT_MAX (Address = 24h)

VOUT_MAX is shown in Figure 7-20 and described in Table 7-23.

Return to the Summary Table.

Write Transaction: N/A
Read Transaction: Read Word
Data Format: ULINEAR16 1.953mV LSB per VOUT_MODE
NVM Back-up: No
Updates: N/A

The VOUT_MAX command sets an upper limit on the output voltage the unit can be commanded through PMBus via any combination of VOUT_COMMAND, VOUT_TRIM, VOUT_MARGIN_HIGH, and VOUT_SCALE_LOOP. The intent of this command is to provide a safeguard against a user accidentally setting the output voltage to a possibly destructive level. When a write to a command attempts to set the output voltage above the VOUT_MAX limit the command's data is still updated as written. This limit is also applies to the startup voltage level VBOOT.

While conversion is enabled, any output voltage change that causes the new target voltage to be greater than the current value of VOUT_MAX will cause the VOUT_MAX_MIN_WARNING condition. This result causes the device to:

- Set to the output voltage to current value of VOUT_MAX at the slew rate defined by VOUT_TRANSITION_RATE.
- Set the STS_MISC bit in the STATUS_BYTE.
- Set the STS_VFW bit in the STATUS_WORD.
- Set the VO_MAX_MIN_W bit in STATUS_VOUT.

The status bits persist until the combined output voltage is less than VOUT_MAX.

Data Validity: Attempts to write to VOUT_MAX are considered as invalid data or unsupported data (ivd) and the device responds as described in the IVD bit in STATUS_CML.

Figure 7-20. VOUT_MAX

15	14	13	12	11	10	9	8
RESERVED	RESERVED	RESERVED	RESERVED	VOUT_MAX[11:0]			
R-0h	R-0h	R-0h	R-0h	R/W-B7Fh			
7	6	5	4	3	2	1	0
VOUT_MAX[11:0]							
R/W-B7Fh							

Table 7-23. VOUT_MAX Field Descriptions

Bit	Field	Type	Reset	Description
15	RESERVED	R	0h	
14	RESERVED	R	0h	
13	RESERVED	R	0h	
12	RESERVED	R	0h	
11:0	VOUT_MAX[11:0]	R/W	B7Fh	The VOUT_MAX value is determined by VIDO_MAX in the SVID_EXT_CAPABILITY_VIDOMAX command. This limit does not apply to output voltage programming that is attempted via SVID, for which SVID registers VID_MAX and VIDO_MAX set the limit.

The read-only contents of this command are set by the value of the VIDO_MAX field in the command SVID_EXT_CAPABILITY_VIDOMAX. VOUT_MAX is calculated from VIDO_MAX as shown in Equation 4.

$$VOUT\_MAX = (VIDO\_MAX \times SCALAR + OFFSET) \times \frac{1mV}{1.953mV} \quad (4)$$

The value for the SCALAR and OFFSET depend on the internal divide ratio and are given in Table 7-24.

Table 7-24. Variables used to set VOUT_MAX from VIDO_MAX

VOUT_SCALE_LOOP (V/V)	SCALAR	OFFSET
0.125(1)	20	980
0.25	10	490
0.5	5	245
1(2)	2.5	122

(1) If VOSL = 0.125V/V the calculation can result in a value that exceeds the maximum value supported by the VOUT_MAX register, so the maximum recommended value for VIDO_MAX in this case is 0EFh.
(2) If VOSL = 1V/V the calculation does not result in an integer value so the calculation result is rounded down to set VOUT_MAX.

7.3.15 VOUT_MARGIN_HIGH (Address = 25h)

VOUT_MARGIN_HIGH is shown in Figure 7-21 and described in Table 7-25.

Return to the Summary Table.

Write Transaction: Write Word
Read Transaction: Read Word
Data Format: ULINEAR16 relative 1.953m LSB per VOUT_MODE
NVM Back-up: EEPROM
Updates: On-the-fly

This command is used to increase the value of the regulated voltage when the OPERATION command is set to Margin High. Since the VOUT format is set to relative in VOUT_MODE[7], the commanded output voltage will increase by the multiplicative factor indicated in this command.

Data Validity: Attempts to change the read-only bits (VOUT_MARGIN_HIGH[15:11]) are considered as invalid data or unsupported data (ivd) and the device responds as described in the IVD bit in STATUS_CML.

Figure 7-21. VOUT_MARGIN_HIGH

15	14	13	12	11	10	9	8
RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	VOUT_MARGIN_HIGH[10:0]		
R-0h	R-0h	R-0h	R-0h	R-0h	R/W-XXh		
7	6	5	4	3	2	1	0
VOUT_MARGIN_HIGH[10:0]							
R/W-XXh							

Table 7-25. VOUT_MARGIN_HIGH Field Descriptions

Bit	Field	Type	Reset	Description
15	RESERVED	R	0h	
14	RESERVED	R	0h	
13	RESERVED	R	0h	
12	RESERVED	R	0h	
11	RESERVED	R	0h	
10:0	VOUT_MARGIN_HIGH[10:0]	R/W	X	Margin High output voltage. Written value are mapped to a resolution of 1.5625%. Additionally those values are mapped to only two options in NVM. See the following table for more details.

Table 7-26. VOUT_MARGIN_HIGH Enumeration

VOUT_MARGIN_HIGH (decimal)		% Margin	Restore value(1)
≥	<		
0	524	101.5625	528d (103.125%)
524	532	103.125	
532	540	104.6875	536d (104.6875%)
540	548	106.25	
548	556	107.8125	
556	564	109.375	
564	572	110.9375	
572	2048	112.5	

(1) The bits in this register do not have direct NVM backup and are instead mapped to one of two settings when storing to NVM.

7.3.16 VOUT_MARGIN_LOW (Address = 26h)

VOUT_MARGIN_LOW is shown in Figure 7-22 and described in Table 7-27.

Return to the Summary Table.

Write Transaction: Write Word
Read Transaction: Read Word
Data Format: ULINEAR16 relative 1.953m LSB per VOUT_MODE
NVM Back-up: EEPROM
Updates: On-the-fly

This command is used to decrease the value of the regulated voltage when the OPERATION command is set to Margin Low. Since the Vout format is set to relative in VOUT_MODE[7], the commanded output voltage will increase by the multiplicative factor indicated in this command.

Data Validity: Attempts to change the read-only bits (VOUT_MARGIN_LOW[15:10]) are considered as invalid data or unsupported data (ivd) and the device responds as described in the IVD bit in STATUS_CML.

Figure 7-22. VOUT_MARGIN_LOW

15	14	13	12	11	10	9	8
RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	VOUT_MARGIN_LOW[9:0]	
R-0h	R-0h	R-0h	R-0h	R-0h	R-0h	R/W-XXh	
7	6	5	4	3	2	1	0
VOUT_MARGIN_LOW[9:0]							
R/W-XXh							

Table 7-27. VOUT_MARGIN_LOW Field Descriptions

Bit	Field	Type	Reset	Description
15	RESERVED	R	0h	
14	RESERVED	R	0h	
13	RESERVED	R	0h	
12	RESERVED	R	0h	
11	RESERVED	R	0h	
10	RESERVED	R	0h	
9:0	VOUT_MARGIN_LOW[9:0]	R/W	X	Margin Low output voltage. Written value are mapped to a resolution of 1.5625%. Additionally those values are mapped to only two options in NVM. See the following table for more details.

Table 7-28. VOUT_MARGIN_LOW Enumeration

VOUT_MARGIN_LOW (decimal)		% Margin	Restore value(1)
≥	<		
0	452	87.5	488d (95.3125%)
452	460	89.0625	
460	468	90.625	
468	476	92.1875	
476	484	93.75	
484	492	95.3125	
492	500	96.875	496d (96.875%)
500	1024	98.4375	

(1) The bits in this register do not have direct NVM backup and are instead mapped to one of two settings when storing to NVM.

7.3.17 VOUT_TRANSITION_RATE (Address = 27h)

VOUT_TRANSITION_RATE is shown in Figure 7-23 and described in Table 7-29.

Return to the Summary Table.

Write Transaction: Write Word
Read Transaction: Read Word
Data Format: LINEAR11
NVM Back-up: EEPROM
Updates: On-the-fly

This command sets the slew rate in mV/us at which any output voltage changes during normal power conversion occur. This commanded rate of change does not apply when the unit is commanded to turn on or to turn off.

Data Validity: Attempts to change the exponent or the upper bits of the mantissa (VOUT_TRANSITION_RATE[10:8]) are considered as invalid data or unsupported data (ivd) and the device responds as described in the IVD bit in STATUS_CML.

Figure 7-23. VOUT_TRANSITION_RATE

15	14	13	12	11	10	9	8
EXPONENT[4:0]					RESERVED	RESERVED	RESERVED
R-1Dh					R-0h	R-0h	R-0h
7	6	5	4	3	2	1	0
VOUT_TRANSITION_RATE[7:0]							
R/W-XXh							

Table 7-29. VOUT_TRANSITION_RATE Field Descriptions

Bit	Field	Type	Reset	Description
15:11	EXPONENT[4:0]	R	1Dh	Linear format two's complement exponent. Fixed exponent of -3 resulting in a 0.125mV/us LSB.
10	RESERVED	R	0h	
9	RESERVED	R	0h	
8	RESERVED	R	0h	
7:0	VOUT_TRANSITION_RATE[7:0]	R/W	X	Linear format mantissa. See the following table for details on the available settings.

Table 7-30. VOUT_TRANSITION_RATE Enumeration

VOUT_TRANSITION_RATE mantissa (decimal)		VOUT_TRANSITION_RATE (mV/µs)	SVID (24h) SR_FAST register value (hex)	Restore value (decimal) (1)
≥	<			
0	8	0.625	00h	5
8	15	1.25	01h	10
15	30	2.5	02h	20
30	42	5	05h	40
42	62	5.56	05h	44
62	84	10	0Ah	80
84	144	11.11	0Ah	89
144	256	25	19h	200

(1) The bits in this register do not have direct NVM backup and are instead restored to a fixed value based on the selected slew rate.

7.3.18 VOUT_DROOP (Address = 28h)

VOUT_DROOP is shown in Figure 7-24 and described in Table 7-31.

Return to the Summary Table.

Write Transaction: N/A
Read Transaction: Read Word
Data Format: Direct (0.1mOhm/LSB)
NVM Back-up: No
Updates: N/A

The VOUT_DROOP command sets the rate, in mV/A (mOhm) at which the output voltage decreases with increasing output current for use with adaptive voltage positioning. This may also be referred to as the DC Load Line (DCLL).

Figure 7-24. VOUT_DROOP

15	14	13	12	11	10	9	8
RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED
R-0h	R-0h	R-0h	R-0h	R-0h	R-0h	R-0h	R-0h
7	6	5	4	3	2	1	0
RESERVED	RESERVED	RESERVED	VOUT_DROOP[4:0]				
R-0h	R-0h	R-0h	R-0h				

Table 7-31. VOUT_DROOP Field Descriptions

Bit	Field	Type	Reset	Description
15	RESERVED	R	0h	
14	RESERVED	R	0h	
13	RESERVED	R	0h	
12	RESERVED	R	0h	
11	RESERVED	R	0h	
10	RESERVED	R	0h	
9	RESERVED	R	0h	
8	RESERVED	R	0h	
7	RESERVED	R	0h	
6	RESERVED	R	0h	
5	RESERVED	R	0h	
4:0	VOUT_DROOP[4:0]	R	0h	Output voltage droop. This field reflects the active DCLL setting, DCLL_0 or DCLL_1. DCLL_0 or DCLL_1 are selected through PMB_ADDR pinstrap.

7.3.19 VOUT_SCALE_LOOP (Address = 29h)

VOUT_SCALE_LOOP is shown in Figure 7-25 and described in Table 7-32.

Return to the Summary Table.

Write Transaction: Write Word
Read Transaction: Read Word
Data Format: LINEAR11
NVM Back-up: EEPROM
Updates: VOUT_CTRL = 10b and output disabled, read/write; VOUT_CTRL = 10b and output enabled, read only; VOUT_CTRL = 00b or 01b, read only

VOUT_SCALE_LOOP allows PMBus devices to map between the commanded voltage and the voltage at the control circuit input. The VOUT_SCALE_LOOP also programs an internal precision resistor divider so no external divider is required.

Data Validity: Attempts to change the read-only bits (VOUT_SCALE_LOOP[15:4]), attempts to write this command when the output is enabled by the ON_OFF_CONFIG mechanism or attempts to write this command when SVID is controlling the output (VOUT_CTRL is 00b or 01b) are considered as invalid data or unsupported data (ivd) and the device responds as described in the IVD bit in STATUS_CML.

Figure 7-25. VOUT_SCALE_LOOP

15	14	13	12	11	10	9	8
EXPONENT[4:0]					RESERVED	RESERVED	RESERVED
R-1Dh					R-0h	R-0h	R-0h
7	6	5	4	3	2	1	0
RESERVED	RESERVED	RESERVED	RESERVED	VOUT_SCALE_LOOP[3:0]			
R-0h	R-0h	R-0h	R-0h	R/W-Xh			

Table 7-32. VOUT_SCALE_LOOP Field Descriptions

Bit	Field	Type	Reset	Description
15:11	EXPONENT[4:0]	R	1Dh	Linear format two's complement exponent. Fixed exponent of -3 resulting in a 0.125 LSB.
10	RESERVED	R	0h	
9	RESERVED	R	0h	
8	RESERVED	R	0h	
7	RESERVED	R	0h	
6	RESERVED	R	0h	
5	RESERVED	R	0h	
4	RESERVED	R	0h	
3:0	VOUT_SCALE_LOOP[3:0]	R/W	X	Linear format mantissa. Attempting to write a value unequal to one of these four options will cause the device to automatically select the nearest supported option per the table below. If VOUT_CTRL is 00b or 01b, the value is determined by the PROTOCOL_ID setting in SVID_ADDR_CFG_USER. 1h = VOUT_SCALE_LOOP of 0.125 V/V. 2h = VOUT_SCALE_LOOP of 0.25 V/V. If VOUT_CTRL is 00b or 01b, this is the value selected when PROTOCOL_ID is selecting the 10mV VID table. 4h = VOUT_SCALE_LOOP of 0.5 V/V. If VOUT_CTRL is 00b or 01b, this is the value selected when PROTOCOL_ID is selecting the 5mV VID table. 8h = VOUT_SCALE_LOOP of 1.00 V/V.

Table 7-33. VOUT_SCALE_LOOP Enumeration

VOUT_SCALE_LOOP mantissa (decimal)		VOUT_SCALE_LOOP (V/V)	Restore value (decimal)(1)
≥	<		
0	2	0.125	1
2	4	0.25	2
4	8	0.5	4

Table 7-33. VOUT_SCALE_LOOP Enumeration (continued)

VOUT_SCALE_LOOP mantissa (decimal)		VOUT_SCALE_LOOP (V/V)	Restore value (decimal)(1)
≥	<		
8	16	1	8

(1) The bits in this register do not have direct NVM backup and are instead restored to a fixed value based on the selected internal divider gain.

7.3.20 FREQUENCY_SWITCH (Address = 33h)

FREQUENCY_SWITCH is shown in Figure 7-26 and described in Table 7-34.

Return to the Summary Table.

Write Transaction: Write Word
Read Transaction: Read Word
Data Format: LINEAR11
NVM Back-up: EEPROM
Updates: On-the-fly

This command sets the switching frequency of the regulator in kHz.

Data Validity: Attempts to change the read-only bits (FREQUENCY_SWITCH[15:4]) are considered as invalid data or unsupported data (ivd) and the device responds as described in the IVD bit in STATUS_CML.

Figure 7-26. FREQUENCY_SWITCH

15	14	13	12	11	10	9	8
EXPONENT[4:0]					RESERVED	RESERVED	RESERVED
R-7h					R-0h	R-0h	R-0h
7	6	5	4	3	2	1	0
RESERVED	RESERVED	RESERVED	RESERVED	FREQUENCY_SWITCH[3:0]			
R-0h	R-0h	R-0h	R-0h	R/W-Xh			

Table 7-34. FREQUENCY_SWITCH Field Descriptions

Bit	Field	Type	Reset	Description
15:11	EXPONENT[4:0]	R	7h	Linear format two's complement exponent. Fixed exponent of 7 resulting in a 128kHz LSB.
10	RESERVED	R	0h	
9	RESERVED	R	0h	
8	RESERVED	R	0h	
7	RESERVED	R	0h	
6	RESERVED	R	0h	
5	RESERVED	R	0h	
4	RESERVED	R	0h	
3:0	FREQUENCY_SWITCH[3:0]	R/W	X	Linear format mantissa. See the following table for details on the available settings.

Table 7-35. FREQUENCY_SWITCH Enumeration

FREQUENCY_SWITCH mantissa (decimal)		FREQUENCY_SWITCH (kHz)
≥	<	
0	4	400
4	6	600
6	7	800
7	9	1000
9	11	1200
11	14	1500
14	15	1800
15	16	2000

7.3.21 VIN_ON (Address = 35h)

VIN_ON is shown in Figure 7-27 and described in Table 7-36.

Return to the Summary Table.

Write Transaction: Write Word
Read Transaction: Read Word
Data Format: LINEAR11
NVM Back-up: EEPROM
Updates: On-the-fly

The VIN_ON command sets the value of the input voltage at the PVIN pin, in volts, at which the device should start power conversion, assuming all other conditions are met.

Data Validity: Attempts to change the read-only bits (VIN_ON[15:4]) are considered as invalid data or unsupported data (ivd) and the device responds as described in the IVD bit in STATUS_CML.

Figure 7-27. VIN_ON

15	14	13	12	11	10	9	8
EXPONENT[4:0]					RESERVED	RESERVED	RESERVED
R-0h					R-0h	R-0h	R-0h
7	6	5	4	3	2	1	0
RESERVED	RESERVED	RESERVED	RESERVED	VIN_ON[3:0]			
R-0h	R-0h	R-0h	R-0h	R/W-Xh			

Table 7-36. VIN_ON Field Descriptions

Bit	Field	Type	Reset	Description
15:11	EXPONENT[4:0]	R	0h	Linear format two's complement exponent. Fixed exponent of 0 resulting in a 1V LSB.
10	RESERVED	R	0h	
9	RESERVED	R	0h	
8	RESERVED	R	0h	
7	RESERVED	R	0h	
6	RESERVED	R	0h	
5	RESERVED	R	0h	
4	RESERVED	R	0h	
3:0	VIN_ON[3:0]	R/W	X	Linear format mantissa. See the following table for details on the available settings.

Table 7-37. VIN_ON Enumeration

VIN_ON mantissa (decimal)		VIN_ON (V)
≥	<	
0	3	2.5
3	5	3.8
5	6	5
6	7	6
7	8	7
8	9	8
9	10	9
10	16	10

7.3.22 VIN_OFF (Address = 36h)

VIN_OFF is shown in Figure 7-28 and described in Table 7-38.

Return to the Summary Table.

Write Transaction: Write Word
Read Transaction: Read Word
Data Format: LINEAR11
NVM Back-up: EEPROM
Updates: On-the-fly

The VIN_OFF command sets the value of the input voltage at the PVIN pin, in volts, at which the device should stop power conversion.

Data Validity: Attempts to change the read-only bits (VIN_OFF[15:4]) are considered as invalid data or unsupported data (ivd) and the device responds as described in the IVD bit in STATUS_CML.

Figure 7-28. VIN_OFF

15	14	13	12	11	10	9	8
EXPONENT[4:0]					RESERVED	RESERVED	RESERVED
R-0h					R-0h	R-0h	R-0h
7	6	5	4	3	2	1	0
RESERVED	RESERVED	RESERVED	RESERVED	VIN_OFF[3:0]			
R-0h	R-0h	R-0h	R-0h	R/W-Xh			

Table 7-38. VIN_OFF Field Descriptions

Bit	Field	Type	Reset	Description
15:11	EXPONENT[4:0]	R	0h	Linear format two's complement exponent. Fixed exponent of 0 resulting in a 1V LSB.
10	RESERVED	R	0h	
9	RESERVED	R	0h	
8	RESERVED	R	0h	
7	RESERVED	R	0h	
6	RESERVED	R	0h	
5	RESERVED	R	0h	
4	RESERVED	R	0h	
3:0	VIN_OFF[3:0]	R/W	X	Linear format mantissa. See the following table for details on the available settings.

Table 7-39. VIN_OFF Enumeration

VIN_OFF mantissa (decimal)		VIN_OFF (V)
≥	<	
0	3	2.3
3	4	3.6
4	5	4.2
5	6	5.5
6	7	6.5
7	8	7.5
8	9	8.5
9	16	9.5

7.3.23 VOUT_OV_FAULT_LIMIT (Address = 40h)

VOUT_OV_FAULT_LIMIT is shown in Figure 7-29 and described in Table 7-40.

Return to the Summary Table.

Write Transaction: Write Word
Read Transaction: Read Word
Data Format: ULINEAR16 relative 1.953m LSB per VOUT_MODE
NVM Back-up: EEPROM
Updates: On-the-fly

The VOUT_OV_FAULT_LIMIT command sets the value, in volts, of the output voltage sensed at the (VOSNS - GOSNS) pins that causes an output overvoltage fault. Since the VOUT format is set to relative in VOUT_MODE[7], the threshold set in this command is a multiplicative factor of the current commanded output voltage. This function is activated after the soft-start ramp completes.

Following an overvoltage fault condition, the device responds according to VOUT_OV_FAULT_RESPONSE command.

Data Validity: Attempts to change the read-only bits (VOUT_OV_FAULT_LIMIT[15:11]) are considered as invalid data or unsupported data (ivd) and the device responds as described in the IVD bit in STATUS_CML.

Figure 7-29. VOUT_OV_FAULT_LIMIT

15	14	13	12	11	10	9	8
RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	VOUT_OV_FAULT_LIMIT[10:0]		
R-0h	R-0h	R-0h	R-0h	R-0h	R/W-XXh		
7	6	5	4	3	2	1	0
VOUT_OV_FAULT_LIMIT[10:0]							
R/W-XXh							

Table 7-40. VOUT_OV_FAULT_LIMIT Field Descriptions

Bit	Field	Type	Reset	Description
15	RESERVED	R	0h	
14	RESERVED	R	0h	
13	RESERVED	R	0h	
12	RESERVED	R	0h	
11	RESERVED	R	0h	
10:0	VOUT_OV_FAULT_LIMIT[10:0]	R/W	X	These bits set the output overvoltage fault threshold. Format is per VOUT_MODE. See the following table for details on the available settings.

Table 7-41. VOUT_OV_FAULT_LIMIT Enumeration

VOUT_OV_FAULT_LIMIT (decimal)		VOUT_OV_FAULT_LIMIT	Restore value (decimal)(1)
≥	<		
0	584	112%	573
584	604	116%	594
604	624	120%	614
624	2048	124%	634

(1) The bits in this register do not have direct NVM backup and are instead restored to a fixed value based on the selected threshold.

7.3.24 VOUT_OV_FAULT_RESPONSE (Address = 41h)

VOUT_OV_FAULT_RESPONSE is shown in Figure 7-30 and described in Table 7-42.

Return to the Summary Table.

Write Transaction: Write Byte
Read Transaction: Read Byte
Data Format: unsigned binary (1 byte)
NVM Back-up: EEPROM
Updates: On-the-fly

The VOUT_OV_FAULT_RESPONSE command instructs the device on what action to take in response to an output overvoltage fault. This includes both the fault limit programmed into (40h) VOUT_OV_FAULT_LIMIT and the fixed OVF selected in (D0h) SYS_CFG_USER1. Upon triggering the fault the device also:

- Sets the STS_OVF bit in STATUS_BYTE
- Sets the STS_VFW bit in STATUS_WORD
- Sets the OVF bit in STATUS_VOUT

Data Validity: Values that may be programmed into this command are 0x00 or 0x3F for ignore, 0xBF for hiccup, and 0x80 for latch off. Any value other than will not be accepted and such an attempt are considered as invalid data or unsupported data (ivd) and the device responds as described in the IVD bit in STATUS_CML.

Figure 7-30. VOUT_OV_FAULT_RESPONSE

7	6	5	4	3	2	1	0
IGNRZ_OV	RESERVED	RS_OV	RESERVED	RESERVED	TD_OV[2:0]		
R/W-Xh	R-0h	R/W-Xh	R-0h	R-0h	R-0h		

Table 7-42. VOUT_OV_FAULT_RESPONSE Field Descriptions

Bit	Field	Type	Reset	Description
7	IGNRZ_OV	R/W	X	Output overvoltage response setting. 0h = The device continues operation (i.e., ignores the fault) without interruption. OVF is also blocked from pulling VRRDY/PGOOD low. 1h = The device shuts down (disables the output) and responds according to the retry setting in bits RS_OV below.
6	RESERVED	R	0h	
5	RS_OV	R/W	X	Output overvoltage retry setting. 0h = Latch-off after the fault. A VCC power cycle or output enable toggle through the ON_OFF_CONFIG mechanism is required to restart power conversion. 7h = Automatically restart after the retry time delay setting without limitation on the number of restart attempts.
4	RESERVED	R	0h	
3	RESERVED	R	0h	
2:0	TD_OV[2:0]	R	0h	Output overvoltage retry time delay setting. 0h = The device does not delay a restart. This is only supported when restart is disabled by setting RS_OV to 0b000. The output remains disabled until the fault is cleared as noted in RS_OV. 7h = The device waits 52ms before going through a normal startup. This is only supported when restart is enabled by setting RS_OV to 0b111.

7.3.25 VOUT_OV_WARN_LIMIT (Address = 42h)

VOUT_OV_WARN_LIMIT is shown in Figure 7-31 and described in Table 7-43.

Return to the Summary Table.

Write Transaction: Write Word
Read Transaction: Read Word
Data Format: ULINEAR16 relative 1.953m LSB per VOUT_MODE
NVM Back-up: EEPROM
Updates: On-the-fly

The VOUT_OV_WARN_LIMIT command sets the value, in volts, of the output voltage sensed at the (VOSNS - GOSNS) pins that causes an output overvoltage warning. This value is typically less than the VOUT_OV_FAULT_LIMIT as it will not trigger a fault. Since the VOUT format is set to relative in VOUT_MODE[7], the threshold set in this command is a multiplicative factor of the current commanded output voltage. This function is activated after the soft-start ramp completes.

Upon triggering the warning the device:

- Sets the STS_MISC bit in STATUS_BYTE
- Sets the STS_VFW bit in STATUS_WORD
- Sets the OVW bit in STATUS_VOUT

Data Validity: Attempts to change the read-only bits (VOUT_OV_WARN_LIMIT[15:11]) are considered as invalid data or unsupported data (ivd) and the device responds as described in the IVD bit in STATUS_CML.

Figure 7-31. VOUT_OV_WARN_LIMIT

15	14	13	12	11	10	9	8
RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	VOUT_OV_WARN_LIMIT[10:0]		
R-0h	R-0h	R-0h	R-0h	R-0h	R/W-XXh		
7	6	5	4	3	2	1	0
VOUT_OV_WARN_LIMIT[10:0]							
R/W-XXh							

Table 7-43. VOUT_OV_WARN_LIMIT Field Descriptions

Bit	Field	Type	Reset	Description
15	RESERVED	R	0h	
14	RESERVED	R	0h	
13	RESERVED	R	0h	
12	RESERVED	R	0h	
11	RESERVED	R	0h	
10:0	VOUT_OV_WARN_LIMIT[10:0]	R/W	X	These bits set the output overvoltage warning threshold. Format is per VOUT_MODE. See the following table for details on the available settings.

Table 7-44. VOUT_OV_WARN_LIMIT Enumeration

VOUT_OV_WARN_LIMIT (decimal)		VOUT_OV_WARN_LIMIT	Restore value (decimal)(1)
≥	<		
0	544	104%	532
544	560	108%	553
560	584	112%	573
584	2048	116%	594

(1) The bits in this register do not have direct NVM backup and are instead restored to a fixed value based on the selected threshold.

7.3.26 VOUT_UV_WARN_LIMIT (Address = 43h)

VOUT_UV_WARN_LIMIT is shown in Figure 7-32 and described in Table 7-45.

Return to the Summary Table.

Write Transaction: Write Word
Read Transaction: Read Word
Data Format: ULINEAR16 relative 1.953m LSB per VOUT_MODE
NVM Back-up: EEPROM
Updates: On-the-fly

The VOUT_UV_WARN_LIMIT command sets the value, in volts, of the output voltage sensed at the (VOSNS - GOSNS) pins that causes an output undervoltage warning. This value is typically greater than the VOUT_UV_FAULT_LIMIT as it will not trigger a fault. Since the VOUT format is set to relative in VOUT_MODE[7], the threshold set in this command is a multiplicative factor of the current commanded output voltage. This function is activated after the soft-start ramp completes.

Upon triggering the warning the device:

- Sets the STS_MISC bit in STATUS_BYTE
- Sets the STS_VFW bit in STATUS_WORD
- Sets the UVW bit in STATUS_VOUT

Data Validity: Attempts to change the read-only bits (VOUT_UV_WARN_LIMIT[15:10]) are considered as invalid data or unsupported data (ivd) and the device responds as described in the IVD bit in STATUS_CML.

Figure 7-32. VOUT_UV_WARN_LIMIT

15	14	13	12	11	10	9	8
RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	VOUT_UV_WARN_LIMIT[9:0]	
R-0h	R-0h	R-0h	R-0h	R-0h	R-0h	R/W-XXh	
7	6	5	4	3	2	1	0
VOUT_UV_WARN_LIMIT[9:0]							
R/W-XXh							

Table 7-45. VOUT_UV_WARN_LIMIT Field Descriptions

Bit	Field	Type	Reset	Description
15	RESERVED	R	0h	
14	RESERVED	R	0h	
13	RESERVED	R	0h	
12	RESERVED	R	0h	
11	RESERVED	R	0h	
10	RESERVED	R	0h	
9:0	VOUT_UV_WARN_LIMIT[9:0]	R/W	X	These bits set the output undervoltage warning threshold. Format is per VOUT_MODE. See the following table for details on the available settings.

Table 7-46. VOUT_UV_WARN_LIMIT Enumeration

VOUT_UV_WARN_LIMIT (decimal)		VOUT_UV_WARN_LIMIT	Restore value (decimal)[1]
≥	<		
0	360	68%	348
360	384	72%	369
384	400	76%	389
400	416	80%	410
416	440	84%	430
440	464	88%	451
464	480	92%	471

Table 7-46. VOUT_UV_WARN_LIMIT Enumeration (continued)

VOUT_UV_WARN_LIMIT (decimal)		VOUT_UV_WARN_LIMIT	Restore value (decimal)(1)
≥	<		
480	1024	96%	492

(1) The bits in this register do not have direct NVM backup and are instead restored to a fixed value based on the selected threshold.

7.3.27 VOUT_UV_FAULT_LIMIT (Address = 44h)

VOUT_UV_FAULT_LIMIT is shown in Figure 7-33 and described in Table 7-47.

Return to the Summary Table.

Write Transaction: Write Word
Read Transaction: Read Word
Data Format: ULINEAR16 relative 1.953m LSB per VOUT_MODE
NVM Back-up: EEPROM
Updates: On-the-fly

The VOUT_UV_FAULT_LIMIT command sets the value, in volts, of the output voltage sensed at the (VOSNS - GOSNS) pins that causes an output undervoltage fault. Since the VOUT format is set to relative in VOUT_MODE[7], the threshold set in this command is a multiplicative factor of the current commanded output voltage. This function is activated after the soft-start ramp completes.

Data Validity: Attempts to change the read-only bits (VOUT_UV_FAULT_LIMIT[15:10]) are considered as invalid data or unsupported data (ivd) and the device responds as described in the IVD bit in STATUS_CML.

Figure 7-33. VOUT_UV_FAULT_LIMIT

15	14	13	12	11	10	9	8
RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	VOUT_UV_FAULT_LIMIT[9:0]	
R-0h	R-0h	R-0h	R-0h	R-0h	R-0h	R/W-XXh	
7	6	5	4	3	2	1	0
VOUT_UV_FAULT_LIMIT[9:0]							
R/W-XXh							

Table 7-47. VOUT_UV_FAULT_LIMIT Field Descriptions

Bit	Field	Type	Reset	Description
15	RESERVED	R	0h	
14	RESERVED	R	0h	
13	RESERVED	R	0h	
12	RESERVED	R	0h	
11	RESERVED	R	0h	
10	RESERVED	R	0h	
9:0	VOUT_UV_FAULT_LIMIT[9:0]	R/W	X	These bits set the output undervoltage fault threshold. Format is per VOUT_MODE. See the following table for details on the available settings.

Table 7-48. VOUT_UV_FAULT_LIMIT Enumeration

VOUT_UV_FAULT_LIMIT (decimal)		VOUT_UV_FAULT_LIMIT	Restore value (decimal)(1)
≥	<		
0	328	60%	307
328	369	68%	348
369	410	76%	389
410	1024	84%	430

(1) The bits in this register do not have direct NVM backup and are instead restored to a fixed value based on the selected threshold.

7.3.28 VOUT_UV_FAULT_RESPONSE (Address = 45h)

VOUT_UV_FAULT_RESPONSE is shown in Figure 7-34 and described in Table 7-49.

Return to the Summary Table.

Write Transaction: Write Byte
Read Transaction: Read Byte
Data Format: unsigned binary (1 byte)
NVM Back-up: EEPROM
Updates: On-the-fly

The VOUT_UV_FAULT_RESPONSE command instructs the device on what action to take in response to an output under-voltage fault. Upon triggering the fault the device also:

- Sets the STS_VFW bit in STATUS_WORD
- Sets the UVF bit in STATUS_VOUT

Data Validity: Values that may be programmed into this command are 0x00 - 0x03 or 0x38 - 0x3B for ignore, 0x78 - 0x7B for hiccup, and 0x40 - 0x43 for latch off. Any value other than will not be accepted and such an attempt are considered as invalid data or unsupported data (ivd) and the device responds as described in the IVD bit in STATUS_CML.

Figure 7-34. VOUT_UV_FAULT_RESPONSE

7	6	5	4	3	2	1	0
RESERVED	IGNRZ_UV	RS_UV	RESERVED	RESERVED	RESERVED	TD_UV[1:0]	
R-0h	R/W-Xh	R/W-Xh	R-0h	R-0h	R-0h	R/W-Xh	

Table 7-49. VOUT_UV_FAULT_RESPONSE Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R	0h	
6	IGNRZ_UV	R/W	X	Output under voltage response setting. 0h = The device continues operation (i.e., ignores the fault) without interruption. UVF_EARLY is also blocked from pulling VRRDY/PGOOD low. 1h = The device continues to operate for the delay time specified by TD_UV. If the fault condition is still present at the end of the delay time, the unit responds as programmed in RS_UV.
5	RS_UV	R/W	X	Output voltage under voltage retry setting. 0h = Latch-off after the fault. A VCC power cycle or output enable toggle through the ON_OFF_CONFIG mechanism is required to restart power conversion. 7h = Automatically restart after the retry time delay setting without limitation on the number of restart attempts.
4	RESERVED	R	0h	
3	RESERVED	R	0h	
2	RESERVED	R	0h	
1:0	TD_UV[1:0]	R/W	X	Output undervoltage response delay and restart delay selection. If the fault condition goes away before the response delay counter expires, then the response delay counter is reset to zero. If RS_UV is set to restart, the restart delay (hiccup duration) is also configured. 0h = 2us response delay, 52ms restart delay 1h = 16us response delay, 52ms restart delay 2h = 64us response delay, 52ms restart delay 3h = 256us response delay, 52ms restart delay

7.3.29 IOUT_OC_FAULT_LIMIT (Address = 46h)

IOUT_OC_FAULT_LIMIT is shown in Figure 7-35 and described in Table 7-50.

Return to the Summary Table.

Write Transaction: Write Word
Read Transaction: Read Word
Data Format: LINEAR11
NVM Back-up: EEPROM
Updates: On-the-fly

The IOUT_OC_FAULT_LIMIT command sets the value of the output current, in amps, that causes the overcurrent detector to indicate an overcurrent fault condition. The thresholds selected here are compared to valley inductor current sensed through the low-side MOSFET.

Data Validity: Attempts to change the read-only bits (IOUT_OC_FAULT_LIMIT[15:6]) will be considered invalid/unsupported data (ivd) and the device responds as described in the IVD bit in STATUS_CML.

Figure 7-35. IOUT_OC_FAULT_LIMIT

15	14	13	12	11	10	9	8
EXPONENT[4:0]					RESERVED	RESERVED	RESERVED
R-0h					R-0h	R-0h	R-0h
7	6	5	4	3	2	1	0
RESERVED	RESERVED	IOUT_OC_FAULT_LIMIT[5:0]					
R-0h	R-0h	R/W-Xh					

Table 7-50. IOUT_OC_FAULT_LIMIT Field Descriptions

Bit	Field	Type	Reset	Description
15:11	EXPONENT[4:0]	R	0h	Linear format two's complement exponent. Fixed exponent of 0 resulting in a 1A LSB.
10	RESERVED	R	0h	
9	RESERVED	R	0h	
8	RESERVED	R	0h	
7	RESERVED	R	0h	
6	RESERVED	R	0h	
5:0	IOUT_OC_FAULT_LIMIT[5:0]	R/W	X	Linear format mantissa. These bits select the inductor valley current limit threshold. See the following table for details on the available settings.

Table 7-51. IOUT_OC_FAULT_LIMIT Enumeration

IOUT_OC_FAULT_LIMIT (decimal)		IOUT_OC_FAULT_LIMIT (A)	Restore value (decimal)(1)
≥	<		
0	9	8	8
9	11	10	10
11	13	12	12
13	16	15	15
16	17	16	16
17	21	20	20
21	25	24	24
25	26	25	25
26	31	30	30
31	33	32	32

Table 7-51. IOUT_OC_FAULT_LIMIT Enumeration (continued)

IOUT_OC_FAULT_LIMIT (decimal)		IOUT_OC_FAULT_LIMIT (A)	Restore value (decimal)(1)
≥	<		
33	64	35	35

(1) The bits in this register do not have direct NVM backup and are instead restored to a fixed value based on the selected threshold.

7.3.30 IOUT_OC_FAULT_RESPONSE (Address = 47h)

IOUT_OC_FAULT_RESPONSE is shown in Figure 7-36 and described in Table 7-52.

Return to the Summary Table.

Write Transaction: N/A
Read Transaction: Read Byte
Data Format: unsigned binary (1 byte)
NVM Back-up: No
Updates: N/A

The IOUT_OC_FAULT_RESPONSE commands instructs the device on what action to take in response to an output overcurrent fault. Upon triggering the fault the device also:

- Sets the STS_OCF bit in STATUS_BYTE
- Sets the STS_OCFW bit in STATUS_WORD
- Sets the OCF bit in STATUS_IOUT

Data Validity: This command is read only. Attempts to write to this command will not be accepted and such an attempt are considered as invalid data or unsupported data (ivd) and the device responds as described in the IVD bit in STATUS_CML.

Figure 7-36. IOUT_OC_FAULT_RESPONSE

7	6	5	4	3	2	1	0
OCF_RESP[1:0]		OCF_RETRY[2:0]			OCF_TD[2:0]		
R-0h		R-0h			R-0h		

Table 7-52. IOUT_OC_FAULT_RESPONSE Field Descriptions

Bit	Field	Type	Reset	Description
7:6	OCF_RESP[1:0]	R	0h	Read-only bits indicating the rail's output overcurrent response setting. 0h = The device continues operation (i.e., ignores the fault) without interruption with the device's valley current limiting the output current.
5:3	OCF_RETRY[2:0]	R	0h	Read-only bits indicating the rail's output overcurrent retry setting after responding to an overcurrent condition. With RESP_OC fixed at 00b, the value of these bits do not impact the expected device behavior.
2:0	OCF_TD[2:0]	R	0h	Read-only bits indicating the rail's output overcurrent response delay and restart delay setting. With RESP_OC fixed at 00b, the value of these bits do not impact the expected device behavior.

7.3.31 IOUT_OC_WARN_LIMIT (Address = 4Ah)

IOUT_OC_WARN_LIMIT is shown in Figure 7-37 and described in Table 7-53.

Return to the Summary Table.

Write Transaction: Write Word
Read Transaction: Read Word
Data Format: LINEAR11
NVM Back-up: EEPROM
Updates: On-the-fly

The IOUT_OC_WARN_LIMIT command sets the average value of the output current, in amps, that causes the overcurrent detector to indicate an overcurrent warn condition. This is implemented in the internal telemetry system by performing a digital comparison of the output of the READ_IOUT telemetry to the warning threshold.

Upon triggering the warning the device:
- Sets the STS_MISC bit in STATUS_BYTE
- Sets the STS_OCFW bit in STATUS_WORD
- Sets the OCW bit in STATUS_IOUT

Data Validity: Attempts to change the read-only bits (IOUT_OC_WARN_LIMIT[15:4]) are considered as invalid data or unsupported data (ivd) and the device responds as described in the IVD bit in STATUS_CML.

Figure 7-37. IOUT_OC_WARN_LIMIT

15	14	13	12	11	10	9	8
EXPONENT[4:0]					RESERVED	RESERVED	RESERVED
R-2h					R-0h	R-0h	R-0h
7	6	5	4	3	2	1	0
RESERVED	RESERVED	RESERVED	RESERVED	IOUT_OC_WARN_LIMIT[3:0]			
R-0h	R-0h	R-0h	R-0h	R/W-Xh			

Table 7-53. IOUT_OC_WARN_LIMIT Field Descriptions

Bit	Field	Type	Reset	Description
15:11	EXPONENT[4:0]	R	2h	Linear format two's complement exponent. Fixed exponent of 2 resulting in a 4A LSB.
10	RESERVED	R	0h	
9	RESERVED	R	0h	
8	RESERVED	R	0h	
7	RESERVED	R	0h	
6	RESERVED	R	0h	
5	RESERVED	R	0h	
4	RESERVED	R	0h	
3:0	IOUT_OC_WARN_LIMIT[3:0]	R/W	X	Linear format mantissa. These bits select the average IOUT warning threshold. All programmable mantissa values of 0 to 15 are available, resulting in an IOUT_OC_WARN_LIMIT of 0A to 60A with a 4A resolution.

7.3.32 OT_FAULT_LIMIT (Address = 4Fh)

OT_FAULT_LIMIT is shown in Figure 7-38 and described in Table 7-54.

Return to the Summary Table.

Write Transaction: Write Word
Read Transaction: Read Word
Data Format: LINEAR11
NVM Back-up: EEPROM
Updates: On-the-fly

The OT_FAULT_LIMIT command sets the temperature, in degrees Celsius, of the device that causes an overtemperature fault condition. This is implemented in the internal telemetry system by performing a digital comparison of the output of the READ_TEMPERATURE_1 telemetry to the warning threshold.

Data Validity: Attempts to change the read-only bits (OT_FAULT_LIMIT[15:6]) are considered as invalid data or unsupported data (ivd) and the device responds as described in the IVD bit in STATUS_CML.

Figure 7-38. OT_FAULT_LIMIT

15	14	13	12	11	10	9	8
EXPONENT[4:0]					RESERVED	RESERVED	RESERVED
R-2h					R-0h	R-0h	R-0h
7	6	5	4	3	2	1	0
RESERVED	RESERVED	OT_FAULT_LIMIT[5:0]					
R-0h	R-0h	R/W-Xh					

Table 7-54. OT_FAULT_LIMIT Field Descriptions

Bit	Field	Type	Reset	Description
15:11	EXPONENT[4:0]	R	2h	Linear format two's complement exponent. Fixed exponent of 2 resulting in a 4 deg C LSB.
10	RESERVED	R	0h	
9	RESERVED	R	0h	
8	RESERVED	R	0h	
7	RESERVED	R	0h	
6	RESERVED	R	0h	
5:0	OT_FAULT_LIMIT[5:0]	R/W	X	Linear format mantissa. These bits select the over-temperature fault threshold in the controller die, based on the precision temperature sensor in the telemetry system. See the following table for details on the available settings.

Table 7-55. OT_FAULT_LIMIT Enumeration

OT_FAULT_LIMIT mantissa (decimal)		OT_FAULT_LIMIT (°C)	Restore value (decimal)(1)
≥	<		
0	30	115	29
30	31	120	30
31	32	125	31
32	34	130	33
34	35	135	34
35	36	140	35
36	37	145	36
37	64	150	38

(1) The bits in this register do not have direct NVM backup and are instead restored to a fixed value based on the selected threshold.

7.3.33 OT_FAULT_RESPONSE (Address = 50h)

OT_FAULT_RESPONSE is shown in Figure 7-39 and described in Table 7-56.

Return to the Summary Table.

Write Transaction: Write Byte
Read Transaction: Read Byte
Data Format: unsigned binary (1 byte)
NVM Back-up: EEPROM
Updates: On-the-fly

The OT_FAULT_RESPONSE command instructs the device on what action to take in response to an over temperature fault. This includes over temperature faults from the controller through READ_TEMP telemetry or OTF_BG and from the power stage through PS_OT. For READ_TEMP telemetry based OTF only, upon triggering the fault the device also:

Sets the STS_OTFW bit in STATUS_BYTE

Sets the OTF_PROG bit in STATUS_TEMPERATURE

Data Validity: Values that may be programmed into this command are 0xBF for hiccup and 0x80 for latch off. Any value other than will not be accepted and such an attempt are considered as invalid data or unsupported data (ivd) and the device responds as described in the IVD bit in STATUS_CML.

Figure 7-39. OT_FAULT_RESPONSE

7	6	5	4	3	2	1	0
RESERVED	RESERVED	RS_OT	RESERVED	RESERVED	TD_OT[2:0]		
R-1h	R-0h	R/W-Xh	R-0h	R-0h	R-0h		

Table 7-56. OT_FAULT_RESPONSE Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R	1h	
6	RESERVED	R	0h	
5	RS_OT	R/W	X	Over temperature retry setting. 0h = Latch-off after the fault. A VCC power cycle or output enable toggle through the ON_OFF_CONFIG mechanism is required to restart power conversion. 7h = Automatically restart after the retry time delay setting without limitation on the number of restart attempts.
4	RESERVED	R	0h	
3	RESERVED	R	0h	
2:0	TD_OT[2:0]	R	0h	Over temperature retry time delay setting. 0h = The device does not delay a restart. This is only supported when restart is disabled by setting RS_OT to 0b000. The output remains disabled until the fault is cleared as noted in RS_OT. 7h = The device waits 52ms before going through a normal startup. This is only supported when restart is enabled by setting RS_OT to 0b111.

7.3.34 OT_WARN_LIMIT (Address = 51h)

OT_WARN_LIMIT is shown in Figure 7-40 and described in Table 7-57.

Return to the Summary Table.

Write Transaction: Write Word
Read Transaction: Read Word
Data Format: LINEAR11
NVM Back-up: EEPROM
Updates: On-the-fly

The OT_WARN_LIMIT command sets the temperature, in degrees Celsius, of the device that causes an overtemperature warning condition. This is implemented in the internal telemetry system by performing a digital comparison of the output of the READ_TEMPERATURE_1 telemetry to the warning threshold.

Upon triggering the warning the device:
- Sets the STS_OTFW bit in STATUS_BYTE
- Sets the OTW_PROG bit in STATUS_TEMPERATURE

Data Validity: Attempts to change the read-only bits (OT_WARN_LIMIT[15:6]) are considered as invalid data or unsupported data (ivd) and the device responds as described in the IVD bit in STATUS_CML.

Figure 7-40. OT_WARN_LIMIT

15	14	13	12	11	10	9	8
EXPONENT[4:0]					RESERVED	RESERVED	RESERVED
R-2h					R-0h	R-0h	R-0h
7	6	5	4	3	2	1	0
RESERVED	RESERVED	OT_WARN_LIMIT[5:0]					
R-0h	R-0h	R/W-Xh					

Table 7-57. OT_WARN_LIMIT Field Descriptions

Bit	Field	Type	Reset	Description
15:11	EXPONENT[4:0]	R	2h	Linear format two's complement exponent. Fixed exponent of 2 resulting in a 4 deg C LSB.
10	RESERVED	R	0h	
9	RESERVED	R	0h	
8	RESERVED	R	0h	
7	RESERVED	R	0h	
6	RESERVED	R	0h	
5:0	OT_WARN_LIMIT[5:0]	R/W	X	Linear format mantissa. See the following table for details on the available settings.

Table 7-58. OT_WARN_LIMIT Enumeration

OT_WARN_LIMIT mantissa (decimal)		OT_WARN_LIMIT (°C)	SVID (22h) TEMP_MAX register value (hex)	Restore value (decimal) (1)
≥	<			
0	25	95	5Fh	24
25	26	100	64h	25
26	27	105	69h	26
27	29	110	6Eh	28
29	30	115	73h	29
30	31	120	78h	30
31	32	125	7Dh	31
32	64	130	82h	33

(1) The bits in this register do not have direct NVM backup and are instead restored to a fixed value based on the selected threshold.

7.3.35 VIN_OV_FAULT_LIMIT (Address = 55h)

VIN_OV_FAULT_LIMIT is shown in Figure 7-41 and described in Table 7-59.

Return to the Summary Table.

Write Transaction: Write Word
Read Transaction: Read Word
Data Format: LINEAR11
NVM Back-up: EEPROM
Updates: On-the-fly

The VIN_OV_FAULT_LIMIT command sets the value of the input voltage at the PVIN pin, in volts, when an input overvoltage fault is declared. VIN_OV_FAULT_LIMIT is typically used to stop switching in the event of excessive input voltage, which can result in over-stress damage to the power FETs due to ringing on the SW node. The response is fixed to latch-off so there is no VIN_OV_FAULT_RESPONSE register.

Upon triggering the fault the device also:

- Sets the STS_MISC bit in STATUS_BYTE
- Sets the STS_INPUT bit in STATUS_WORD
- Sets the PVIN_OVF bit in STATUS_INPUT

Data Validity: Attempts to change the read-only bits (VIN_OV_FAULT_LIMIT[15:4]) are considered as invalid data or unsupported data (ivd) and the device responds as described in the IVD bit in STATUS_CML.

Figure 7-41. VIN_OV_FAULT_LIMIT

15	14	13	12	11	10	9	8
EXPONENT[4:0]					RESERVED	RESERVED	RESERVED
R-1h					R-0h	R-0h	R-0h
7	6	5	4	3	2	1	0
RESERVED	RESERVED	RESERVED	RESERVED	VIN_OV_FAULT_LIMIT[3:0]			
R-0h	R-0h	R-0h	R-0h	R/W-Xh			

Table 7-59. VIN_OV_FAULT_LIMIT Field Descriptions

Bit	Field	Type	Reset	Description
15:11	EXPONENT[4:0]	R	1h	Linear format two's complement exponent. Fixed exponent of 1 resulting in a 2V LSB.
10	RESERVED	R	0h	
9	RESERVED	R	0h	
8	RESERVED	R	0h	
7	RESERVED	R	0h	
6	RESERVED	R	0h	
5	RESERVED	R	0h	
4	RESERVED	R	0h	
3:0	VIN_OV_FAULT_LIMIT[3:0]	R/W	X	Linear format mantissa. These bits select the VIN over-voltage threshold. See the following table for details on the available settings.

Table 7-60. VIN_OV_FAULT_LIMIT Enumeration

VIN_OV_FAULT_LIMIT mantissa (decimal)		VIN_OV_FAULT_LIMIT (V)	Restore value (decimal)(1)
≥	<		
0	9	16.5	8
9	16	18.5	9

(1) The bits in this register do not have direct NVM backup and are instead restored to a fixed value based on the selected threshold.

7.3.36 TON_DELAY (Address = 60h)

TON_DELAY is shown in Figure 7-42 and described in Table 7-61.

Return to the Summary Table.

Write Transaction: Write Word
Read Transaction: Read Word
Data Format: LINEAR11
NVM Back-up: EEPROM
Updates: On-the-fly

The TON_DELAY command sets the time, in milliseconds, from when a start condition is received (as programmed by the ON_OFF_CONFIG command) until the output voltage starts to rise.

Data Validity: Attempts to change the read-only bits (TON_DELAY[15:3]) are considered as invalid data or unsupported data (ivd) and the device responds as described in the IVD bit in STATUS_CML.

Figure 7-42. TON_DELAY

15	14	13	12	11	10	9	8
EXPONENT[4:0]					RESERVED	RESERVED	RESERVED
R-1Fh					R-0h	R-0h	R-0h
7	6	5	4	3	2	1	0
RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	TON_DELAY[2:0]		
R-0h	R-0h	R-0h	R-0h	R-0h	R/W-Xh		

Table 7-61. TON_DELAY Field Descriptions

Bit	Field	Type	Reset	Description
15:11	EXPONENT[4:0]	R	1Fh	Linear format two's complement exponent. Fixed exponent of -1 resulting in a 0.5ms LSB.
10	RESERVED	R	0h	
9	RESERVED	R	0h	
8	RESERVED	R	0h	
7	RESERVED	R	0h	
6	RESERVED	R	0h	
5	RESERVED	R	0h	
4	RESERVED	R	0h	
3	RESERVED	R	0h	
2:0	TON_DELAY[2:0]	R/W	X	Linear format mantissa. These bits select the turn-on delay. Possible values are below. When an unsupported value is written, an adjacent available option will be selected. Note: A minimum turn-on delay of approximately 50us is always enforced, even when selecting the minimum setting. 0h = 0.05ms 1h = 0.5ms 2h = 1ms 4h = 2ms

Table 7-62. TON_DELAY Enumeration

TON_DELAY mantissa (decimal)		TON_DELAY (ms)	Restore value (decimal)(1)
≥	<		
0	1	0.05	0
1	2	0.5	1
2	3	1	2
3	8	2	4

(1) The bits in this register do not have direct NVM backup and are instead restored to a fixed value based on the selected threshold.

7.3.37 TON_RISE (Address = 61h)

TON_RISE is shown in Figure 7-43 and described in Table 7-63.

Return to the Summary Table.

Write Transaction: Write Word
Read Transaction: Read Word
Data Format: LINEAR11
NVM Back-up: EEPROM
Updates: On-the-fly

The TON_RISE command sets the time, in milliseconds, from when the output starts to rise until the voltage has entered regulation. A combination of the value programmed into this command and the VBOOT value sets the DAC slew rate to achieve the target soft-start time.

Data Validity: Attempts to change the read-only bits (TON_RISE[15:6]) are considered as invalid data or unsupported data (ivd) and the device responds as described in the IVD bit in STATUS_CML.

Figure 7-43. TON_RISE

15	14	13	12	11	10	9	8
EXPONENT[4:0]					RESERVED	RESERVED	RESERVED
R-1Fh					R-0h	R-0h	R-0h
7	6	5	4	3	2	1	0
RESERVED	RESERVED	TON_RISE[5:0]					
R-0h	R-0h	R/W-Xh					

Table 7-63. TON_RISE Field Descriptions

Bit	Field	Type	Reset	Description
15:11	EXPONENT[4:0]	R	1Fh	Linear format two's complement exponent. Fixed exponent of -1 resulting in a 0.5ms LSB.
10	RESERVED	R	0h	
9	RESERVED	R	0h	
8	RESERVED	R	0h	
7	RESERVED	R	0h	
6	RESERVED	R	0h	
5:0	TON_RISE[5:0]	R/W	X	Linear format mantissa. Possible values are below. When an unsupported value is written, an adjacent available option will be selected. 1h = 0.5ms 2h = 1ms 4h = 2ms 8h = 4ms 10h = 8ms 20h = 16ms 3Eh = 16ms 3Fh = 16ms

7.3.38 TOFF_DELAY (Address = 64h)

TOFF_DELAY is shown in Figure 7-44 and described in Table 7-64.

Return to the Summary Table.

Write Transaction: Write Word
Read Transaction: Read Word
Data Format: LINEAR11
NVM Back-up: EEPROM
Updates: On-the-fly

The TOFF_DELAY command sets the time, in milliseconds, from when a stop condition is received (as programmed by the ON_OFF_CONFIG command) until the output voltage starts to fall. Refer to the OPERATION and ON_OFF_CONFIG command descriptions for details on when the TOFF_DELAY period is used upon receiving a stop condition.

Data Validity: Attempts to change the read-only bits (TOFF_DELAY[15:3]) are considered as invalid data or unsupported data (ivd) and the device responds as described in the IVD bit in STATUS_CML.

Figure 7-44. TOFF_DELAY

15	14	13	12	11	10	9	8
EXPONENT[4:0]					RESERVED	RESERVED	RESERVED
R-1Fh					R-0h	R-0h	R-0h
7	6	5	4	3	2	1	0
RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	TOFF_DELAY[2:0]		
R-0h	R-0h	R-0h	R-0h	R-0h	R/W-Xh		

Table 7-64. TOFF_DELAY Field Descriptions

Bit	Field	Type	Reset	Description
15:11	EXPONENT[4:0]	R	1Fh	Linear format two's complement exponent. Fixed exponent of -1 resulting in a 0.5ms LSB.
10	RESERVED	R	0h	
9	RESERVED	R	0h	
8	RESERVED	R	0h	
7	RESERVED	R	0h	
6	RESERVED	R	0h	
5	RESERVED	R	0h	
4	RESERVED	R	0h	
3	RESERVED	R	0h	
2:0	TOFF_DELAY[2:0]	R/W	X	Linear format mantissa. These bits select the turn off delay time. Possible values are below. When an unsupported value is written, an adjacent available option will be selected. 0h = 0ms 2h = 1ms 3h = 1.5ms 4h = 2ms

7.3.39 TOFF_FALL (Address = 65h)

TOFF_FALL is shown in Figure 7-45 and described in Table 7-65.

Return to the Summary Table.

Write Transaction: Write Word
Read Transaction: Read Word
Data Format: LINEAR11
NVM Back-up: EEPROM
Updates: On-the-fly

The TOFF_FALL command sets the time, in milliseconds, from when a stop condition is received (as programmed by the ON_OFF_CONFIG command) until the output voltage starts to fall. Refer to the OPERATION and ON_OFF_CONFIG command descriptions for details on when the TOFF_FALL period is used upon receiving a stop condition.

A combination of the value programmed into this command and the VBOOT value sets the DAC slew rate to achieve the target soft-stop time. Switching stops and the output voltage stops slewing down when the regulated VOUT reaches 0.2V nominal, however the time programmed into this command is based on the output voltage slewing to 0V. As a result the observed TOFF_FALL time to 0V may different than the value programmed into this command, and is dependent on how long it takes the load to discharge the remaining 0.2V output.

Data Validity: Attempts to change the read-only bits (TOFF_FALL[15:4]) are considered as invalid data or unsupported data (ivd) and the device responds as described in the IVD bit in STATUS_CML.

Figure 7-45. TOFF_FALL

15	14	13	12	11	10	9	8
EXPONENT[4:0]					RESERVED	RESERVED	RESERVED
R-1Fh					R-0h	R-0h	R-0h
7	6	5	4	3	2	1	0
RESERVED	RESERVED	RESERVED	RESERVED	TOFF_FALL[3:0]			
R-0h	R-0h	R-0h	R-0h	R/W-Xh			

Table 7-65. TOFF_FALL Field Descriptions

Bit	Field	Type	Reset	Description
15:11	EXPONENT[4:0]	R	1Fh	Linear format two's complement exponent. Fixed exponent of -1 resulting in a 0.5ms LSB.
10	RESERVED	R	0h	
9	RESERVED	R	0h	
8	RESERVED	R	0h	
7	RESERVED	R	0h	
6	RESERVED	R	0h	
5	RESERVED	R	0h	
4	RESERVED	R	0h	
3:0	TOFF_FALL[3:0]	R/W	X	Linear format mantissa. These bits select the soft-stop time. Possible values are below. When an unsupported value is written, an adjacent available option will be selected. 1h = 0.5ms 2h = 1ms 4h = 2ms 8h = 4ms

7.3.40 PIN_OP_WARN_LIMIT (Address = 6Bh)

PIN_OP_WARN_LIMIT is shown in Figure 7-46 and described in Table 7-66.

Return to the Summary Table.

Write Transaction: Write Word
Read Transaction: Read Word
Data Format: LINEAR11
NVM Back-up: EEPROM
Updates: On-the-fly

The PIN_OP_WARN_LIMIT command sets the input power, in watts, that causes the input power detector to indicate an input power warn condition. This is implemented in the internal telemetry system by performing a digital comparison of the output of the READ_PIN telemetry to the warning threshold. This command also sets the value in the SVID register (2Eh) PIN_MAX.

Upon triggering the warning the device:

- Sets the STS_MISC bit in STATUS_BYTE
- Sets the STS_INPUT bit in STATUS_WORD
- Sets the PIN_OPW bit in STATUS_INPUT

Data Validity: Attempts to change the read-only bits (PIN_OP_WARN_LIMIT[15:8]) are considered as invalid data or unsupported data (ivd) and the device responds as described in the IVD bit in STATUS_CML.

Figure 7-46. PIN_OP_WARN_LIMIT

15	14	13	12	11	10	9	8
EXPONENT[4:0]					RESERVED	RESERVED	RESERVED
R-2h					R-0h	R-0h	R-0h
7	6	5	4	3	2	1	0
PIN_OP_WARN_LIMIT[7:0]							
R/W-XXh							

Table 7-66. PIN_OP_WARN_LIMIT Field Descriptions

Bit	Field	Type	Reset	Description
15:11	EXPONENT[4:0]	R	2h	Linear format two's complement exponent. Fixed exponent of 2 resulting in a 4W LSB.
10	RESERVED	R	0h	
9	RESERVED	R	0h	
8	RESERVED	R	0h	
7:0	PIN_OP_WARN_LIMIT[7:0]	R/W	X	Linear format mantissa. These bits select the input over-power warning threshold. Possible values are below. When an unsupported value is written, an adjacent available option will be selected. 1Eh = 120W 2Dh = 180W 3Ch = 240W 4Bh = 300W 5Ah = 360W 69h = 420W 78h = 480W A0h = 640W

7.3.41 STATUS_BYTE (Address = 78h)

STATUS_BYTE is shown in Figure 7-47 and described in Table 7-67.

Return to the Summary Table.

Write Transaction: N/A
Read Transaction: Read Byte
Data Format: unsigned binary (1 byte)
NVM Back-up: No
Updates: N/A

The STATUS_BYTE command returns one byte of information with a summary of the most critical faults, including overvoltage, overcurrent and overtemperature. The following table describes the bits the device supports in STATUS_BYTE. In the event of a fault or warning, the bits in STATUS_BYTE are asserted to indicate which other status registers should be checked for further information. The bits in STATUS_BYTE cannot be cleared through writes to STATUS_BYTE. Instead, clearing the bits must be done in through writes to the other corresponding status registers.

Data Validity: Attempts to write STATUS_BYTE are considered as invalid data or unsupported data (ivd) and the device responds as described in the IVD bit in STATUS_CML.

Figure 7-47. STATUS_BYTE

7	6	5	4	3	2	1	0
RESERVED	STS_OFF	STS_OVF	STS_OCF	RESERVED	STS_OTFW	STS_CML	STS_MISC
R-0h	R-1h	R-0h	R-0h	R-0h	R-0h	R-0h	R-1h

Table 7-67. STATUS_BYTE Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R	0h	
6	STS_OFF	R	1h	LIVE (unlatched) status bit, indicating if the device output is disabled. 0h = Device output enabled. 1h = Device output disabled due to fault or external configuration (e.g. disabled through the ON_OFF_CONFIG mechanism).
5	STS_OVF	R	0h	This bit indicates if an output overvoltage fault has occurred. This bit directly reflects the state of STATUS_VOUT[7] - OVF. 0h = No output overvoltage fault. 1h = An output overvoltage fault has occurred.
4	STS_OCF	R	0h	This bit indicates if an output overcurrent fault has occurred. It directly reflects the state of STATUS_IOUT[7] - OCF. 0h = No output overcurrent fault. 1h = An output overcurrent fault has occurred.
3	RESERVED	R	0h	
2	STS_OTFW	R	0h	This bit indicates if an overtemperature fault or warning has occurred. It is an OR of the OTF_PROG and OTW_PROG bits located at STATUS_TEMPERATURE[7:6]. 0h = No overtemperature fault or warning. 1h = An overtemperature fault or warning has occurred. The host should check STATUS_TEMPERATURE for more information.
1	STS_CML	R	0h	This bit indicates that a communications, memory or logic fault has occurred in STATUS_CML. 0h = No communications, memory or logic fault. 1h = A communications, memory or logic fault has occurred. The host should check STATUS_CML for more information.
0	STS_MISC	R	1h	This bit is used to flag faults and warnings not covered with the other bits in STATUS_BYTE. 0h = No fault other than those listed above. 1h = A fault other than those listed above has occurred. The host should check STATUS_WORD for more information.

7.3.42 STATUS_WORD (Address = 79h)

STATUS_WORD is shown in Figure 7-48 and described in Table 7-68.

Return to the Summary Table.

Write Transaction: N/A
Read Transaction: Read Word
Data Format: unsigned binary (2 bytes)
NVM Back-up: No
Updates: N/A

The STATUS_WORD command returns a two-byte value summarizing fault and warning conditions in the device. The following table describes the bits the device supports in STATUS_WORD. The low byte of this command duplicates the information provided by the STATUS_BYTE command, while the high byte provides additional context.

When a fault or warning occurs, these bits are asserted to identify which status registers should be read for further information. These bits cannot be cleared through writes to STATUS_WORD. Instead, clearing the bits must be done in through writes to the other corresponding status registers.

Data Validity: Attempts to write STATUS_WORD are considered as invalid data or unsupported data (ivd) and the device responds as described in the IVD bit in STATUS_CML.

Figure 7-48. STATUS_WORD

15	14	13	12	11	10	9	8
STS_VFW	STS_OCFW	STS_INPUT	STS_MFR	STS_PGOOD_Z	RESERVED	OTHER	RESERVED
R-0h	R-0h	R-1h	R-0h	R-1h	R-0h	R-0h	R-0h
7	6	5	4	3	2	1	0
RESERVED	STS_OFF	STS_OVF	STS_OCF	RESERVED	STS_OTFW	STS_CML	STS_MISC
R-0h	R-1h	R-0h	R-0h	R-0h	R-0h	R-0h	R-1h

Table 7-68. STATUS_WORD Field Descriptions

Bit	Field	Type	Reset	Description
15	STS_VFW	R	0h	This bit indicates if an output voltage fault or warning in STATUS_VOUT has occurred. 0h = No output voltage fault or warning. 1h = An output voltage fault or warning has occurred. The host should check STATUS_VOUT for more information.
14	STS_OCFW	R	0h	This bit indicates if an output current fault or warning in STATUS_IOUT has occurred. 0h = No output current fault or warning. 1h = An output current fault or warning has occurred. The host should check STATUS_IOUT for more information.
13	STS_INPUT	R	1h	This bit indicates if an input fault or warning in STATUS_INPUT has occurred. 0h = No input fault or warning. 1h = An input fault or warning has occurred. The host should check STATUS_INPUT for more information.
12	STS_MFR	R	0h	This bit indicates if a fault or warning in STATUS_MFR_SPECIFIC has occurred, with the exception of bit 7 DCM. 0h = No manufacturer-defined fault or warning. 1h = A manufacturer-defined fault or warning has occurred. The host should check STATUS_MFR_SPECIFIC for more information.
11	STS_PGOOD_Z	R	1h	LIVE (unlatched) status bit indicating if the power good signal is low. The power good signal goes low when the output is off or upon the output voltage exceeding the threshold programmed into the VOUT_OV_FAULT_LIMIT command or the VOUT_UV_FAULT_LIMIT command. Although this signal is unlatched, the faults which assert PGOOD low are latched. This bit cannot be cleared by a PMBus write and this bit cannot trigger SMB_ALERT#. 0h = The power good signal is high. 1h = The power good signal is low, indicating the output is off or a fault condition caused the output voltage to exceed the set thresholds.
10	RESERVED	R	0h	
9	OTHER	R	0h	This bit indicates if a fault or warning in STATUS_OTHER has occurred. 0h = No fault or warning in STATUS_OTHER. 1h = A fault or warning in STATUS_OTHER has occurred. The host should check STATUS_OTHER for more information.
8	RESERVED	R	0h	
7	RESERVED	R	0h	
6	STS_OFF	R	1h	

Table 7-68. STATUS_WORD Field Descriptions (continued)

Bit	Field	Type	Reset	Description
5	STS_OVF	R	0h	
4	STS_OCF	R	0h	
3	RESERVED	R	0h	
2	STS_OTFW	R	0h	
1	STS_CML	R	0h	
0	STS_MISC	R	1h	

7.3.43 STATUS_VOUT (Address = 7Ah)

STATUS_VOUT is shown in Figure 7-49 and described in Table 7-69.

Return to the Summary Table.

Write Transaction: Write Byte
Read Transaction: Read Byte
Data Format: unsigned binary (1 byte)
NVM Back-up: No
Updates: On-the-fly

The STATUS_VOUT command returns one byte of information relating to the status of the converter's output voltage related faults and warnings as follows. The status bits remain latched even after the fault or warning condition is resolved. The bits can be cleared by:

- CLEAR_FAULTS command
- Writing 1b to the target bit
- Toggling the ON_OFF_CONFIG mechanism of the rail
- Power cycle to reset the device

The STS_VFW bit in STATUS_WORD represents an ORing of the bits in this command. When any of the event occurs that sets a bit in this command, the STS_VFW bit is also set. Similarly, if all of the bits in this command are cleared, STS_VFW is also cleared.

All bits which can trigger SMB_ALERT# have a corresponding mask bit in the SMBALERT_MASK command.

Figure 7-49. STATUS_VOUT

7	6	5	4	3	2	1	0
OVF	OVW	UVW	UVF	VO_MAX_MIN_W	RESERVED	RESERVED	RESERVED
R/W1C-0h	R/W1C-0h	R/W1C-0h	R/W1C-0h	R/W1C-0h	R-0h	R-0h	R-0h

Table 7-69. STATUS_VOUT Field Descriptions

Bit	Field	Type	Reset	Description
7	OVF	R/W1C	0h	This latched bit is set if the output voltage exceeds either the relative threshold configured with the VOUT_OV_FAULT_LIMIT command or the absolute threshold selected with the SEL_FIX_OVF bit field in the SYS_CFG_USER1 command. 0h = No output overvoltage fault. 1h = An output overvoltage fault has occurred.
6	OVW	R/W1C	0h	This latched bit is set if the output voltage exceeds the relative threshold as configured with the VOUT_OV_WARN_LIMIT command. 0h = No output overvoltage warning. 1h = An output overvoltage warning has occurred.
5	UVW	R/W1C	0h	This latched bit is set if the output voltage goes below the relative threshold as configured with the VOUT_UV_WARN_LIMIT command. This bit will also be set in the event of a UVF. 0h = No output undervoltage warning. 1h = An output undervoltage warning has occurred.
4	UVF	R/W1C	0h	This latched bit is set if the output voltage goes below the relative threshold as configured with the VOUT_UV_FAULT_LIMIT command. 0h = No output undervoltage warning. 1h = An output undervoltage warning has occurred.
3	VO_MAX_MIN_W	R/W1C	0h	This latched bit is set if an attempt to set the output voltage through the PMBus interface is limited by the VOUT_MAX command. Refer to the VOUT_MAX command description for more details. 0h = No output voltage maximum or minimum warning. 1h = An output voltage maximum or minimum warning has occurred.
2	RESERVED	R	0h	
1	RESERVED	R	0h	
0	RESERVED	R	0h	

7.3.44 STATUS_IOUT (Address = 7Bh)

STATUS_IOUT is shown in Figure 7-50 and described in Table 7-70.

Return to the Summary Table.

Write Transaction: Write Byte
Read Transaction: Read Byte
Data Format: unsigned binary (1 byte)
NVM Back-up: No
Updates: On-the-fly

The STATUS_IOUT command returns one byte of information relating to the status of the converter's output current related faults and warnings as follows. The status bits remain latched even after the fault or warning condition is resolved. The bits can be cleared by:

- CLEAR_FAULTS command
- Writing 1b to the target bit
- Toggling the ON_OFF_CONFIG mechanism of the rail
- Power cycle to reset the device

The STS_OCFW bit in STATUS_WORD represents an ORing of the bits in this command. When any of the event occurs that sets a bit in this command, the STS_OCFW bit is also set. Similarly, if all of the bits in this command are cleared, STS_OCFW is also cleared.

All bits which can trigger SMB_ALERT# have a corresponding mask bit in the SMBALERT_MASK command.

Figure 7-50. STATUS_IOUT

7	6	5	4	3	2	1	0
OCF	OCUV	OCW	UCF	RESERVED	RESERVED	RESERVED	RESERVED
R/W1C-0h	R-0h	R/W1C-0h	R/W1C-0h	R-0h	R-0h	R-0h	R-0h

Table 7-70. STATUS_IOUT Field Descriptions

Bit	Field	Type	Reset	Description
7	OCF	R/W1C	0h	This latched bit is set if the maximum valley inductor current is being limited by the device to the threshold configured with the IOUT_OC_FAULT_LIMIT command. 0h = No output overcurrent fault. 1h = An output overcurrent fault has occurred.
6	OCUV	R	0h	This bit is a logical AND of the OCF bit and the UVF bit in STATUS_VOUT. This bit cannot be cleared directly by writing 1b to it. Instead clearing this bit requires clearing either the OCF or UVF bits. Additionally, this bit does not have separate SMB_ALERT# masking. Instead this bit is also masked if the UVF bit in STATUS_VOUT is masked.
5	OCW	R/W1C	0h	This latched bit is set if the READ_IOUT telemetry exceeds the threshold as configured with the IOUT_OC_WARN_LIMIT command. 0h = No output overcurrent warning. 1h = An output overcurrent warning has occurred.
4	UCF	R/W1C	0h	This latched bit is set if the minimum valley inductor current is being limited by the device to the threshold configured with the SEL_NOC bit field in the SYS_CFG_USER1 command. 0h = No output undercurrent fault. 1h = An output undercurrent fault has occurred.
3	RESERVED	R	0h	
2	RESERVED	R	0h	
1	RESERVED	R	0h	
0	RESERVED	R	0h	

7.3.45 STATUS_INPUT (Address = 7Ch)

STATUS_INPUT is shown in Figure 7-51 and described in Table 7-71.

Return to the Summary Table.

Write Transaction: Write Byte
Read Transaction: Read Byte
Data Format: unsigned binary (1 byte)
NVM Back-up: No
Updates: On-the-fly

The STATUS_INPUT command returns one byte of information relating to the status of the converter's input related faults and warnings as follows. The status bits remain latched even after the fault or warning condition is resolved. The bits can be cleared by:

- CLEAR_FAULTS command
- Writing 1b to the target bit
- Toggling the ON_OFF_CONFIG mechanism of the rail
- Power cycle to reset the device

The STS_INPUT bit in STATUS_WORD represents an ORing of the bits in this command. When any of the event occurs that sets a bit in this command, the STS_INPUT bit is also set. Similarly, if all of the bits in this command are cleared, STS_INPUT is also cleared.

All bits which can trigger SMB_ALERT# have a corresponding mask bit in the SMBALERT_MASK command.

Figure 7-51. STATUS_INPUT

7	6	5	4	3	2	1	0
PVIN_OVF	RESERVED	RESERVED	RESERVED	LOW_VIN	RESERVED	RESERVED	PIN_OPW
R/W1C-0h	R-0h	R-0h	R-0h	R/W1C-1h	R-0h	R-0h	R/W1C-0h

Table 7-71. STATUS_INPUT Field Descriptions

Bit	Field	Type	Reset	Description
7	PVIN_OVF	R/W1C	0h	This latched bit is set if the input voltage exceeds the threshold as configured with the VIN_OV_FAULT_LIMIT command. 0h = No input overvoltage fault. 1h = An input overvoltage fault has occurred.
6	RESERVED	R	0h	
5	RESERVED	R	0h	
4	RESERVED	R	0h	
3	LOW_VIN	R/W1C	1h	This bit is initially set during power-up and remains set until the power input voltage (PVIN) exceeds both the VIN_OFF and VIN_ON thresholds. During the initial power-up, the LOW_VIN bit is LIVE (unlatched) and does not trigger SMB_ALERT#. Upon PVIN exceeding the VIN_ON threshold for the first time, subsequent PVIN drops below the VIN_OFF threshold will result in a latched LOW_VIN bit and it will trigger SMB_ALERT# if unmasked. 0h = PVIN is greater than VIN_ON and VIN_OFF 1h = PVIN is less than VIN_OFF
2	RESERVED	R	0h	
1	RESERVED	R	0h	
0	PIN_OPW	R/W1C	0h	This latched bit is set if the READ_PIN telemetry exceeds the threshold as configured with the PIN_OP_WARN_LIMIT command. 0h = No input overpower warning. 1h = An input overpower warning has occurred.

7.3.46 STATUS_TEMPERATURE (Address = 7Dh)

STATUS_TEMPERATURE is shown in Figure 7-52 and described in Table 7-72.

Return to the Summary Table.

Write Transaction: Write Byte
Read Transaction: Read Byte
Data Format: unsigned binary (1 byte)
NVM Back-up: No
Updates: On-the-fly

The STATUS_TEMPERATURE command returns one byte of information relating to the status of the converter's temperature related faults and warnings as follows. The status bits remain latched even after the fault or warning condition is resolved. The bits can be cleared by:

- CLEAR_FAULTS command
- Writing 1b to the target bit
- Toggling the ON_OFF_CONFIG mechanism of the rail
- Power cycle to reset the device

The STS_OTFW bit in STATUS_BYTE represents an ORing of the bits in this command. When any of the event occurs that sets a bit in this command, the STS_OTFW bit is also set. Similarly, if all of the bits in this command are cleared, STS_OTFW is also cleared.

All bits which can trigger SMB_ALERT# have a corresponding mask bit in the SMBALERT_MASK command.

Figure 7-52. STATUS_TEMPERATURE

7	6	5	4	3	2	1	0
OTF_PROG	OTW_PROG	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED
R/W1C-0h	R/W1C-0h	R-0h	R-0h	R-0h	R-0h	R-0h	R-0h

Table 7-72. STATUS_TEMPERATURE Field Descriptions

Bit	Field	Type	Reset	Description
7	OTF_PROG	R/W1C	0h	This latched bit is set if the READ_TEMPERATURE_1 telemetry exceeds the threshold as configured with the OT_FAULT_LIMIT command. 0h = No overtemperature fault. 1h = An overtemperature fault has occurred.
6	OTW_PROG	R/W1C	0h	This latched bit is set if the READ_TEMPERATURE_1 telemetry exceeds the threshold as configured with the OT_WARN_LIMIT command. 0h = No overtemperature warning. 1h = An overtemperature warning has occurred.
5	RESERVED	R	0h	
4	RESERVED	R	0h	
3	RESERVED	R	0h	
2	RESERVED	R	0h	
1	RESERVED	R	0h	
0	RESERVED	R	0h	

7.3.47 STATUS_CML (Address = 7Eh)

STATUS_CML is shown in Figure 7-53 and described in Table 7-73.

Return to the Summary Table.

Write Transaction: Write Byte
Read Transaction: Read Byte
Data Format: unsigned binary (1 byte)
NVM Back-up: No
Updates: On-the-fly

The STATUS_CML command returns one byte with contents relating to communications, logic, and memory as follows. The status bits remain latched even after the fault or warning condition is resolved. The bits can be cleared by:

- CLEAR_FAULTS command
- Writing 1b to the target bit
- Toggling the ON_OFF_CONFIG mechanism of the rail
- Power cycle to reset the device

The STS_CML bit in STATUS_BYTE represents an ORing of the bits in this command. When any of the event occurs that sets a bit in this command, the STS_CML bit is also set. Similarly, if all of the bits in this command are cleared, STS_CML is also cleared.

All bits which can trigger SMB_ALERT# have a corresponding mask bit in the SMBALERT_MASK command.

Figure 7-53. STATUS_CML

7	6	5	4	3	2	1	0
IVC	IVD	PEC_FAIL	MEM	RESERVED	RESERVED	OTH_COMM	RESERVED
R/W1C-0h	R/W1C-0h	R/W1C-0h	R/W1C-0h	R-0h	R-0h	R/W1C-0h	R-0h

Table 7-73. STATUS_CML Field Descriptions

Bit	Field	Type	Reset	Description
7	IVC	R/W1C	0h	This latched bit is set when an invalid command is detected and the device responds as follows: • NACK the unsupported command code and all data bytes • Ignore the received command code and any received data • Set the STS_CML bit in STATUS_BYTE • Set the IVC bit in STATUS_CML 0h = No invalid or unsupported command. 1h = Invalid or unsupported command received.
6	IVD	R/W1C	0h	This latched bit is set when invalid or unsupported data is detected and the device responds as follows: • NACK the invalid or unsupported data bytes • Ignore the received command code and any received data • Set the STS_CML bit in STATUS_BYTE • Set the IVD bit in STATUS_CML 0h = No invalid or unsupported data. 1h = Invalid or unsupported data received.
5	PEC_FAIL	R/W1C	0h	
4	MEM	R/W1C	0h	This latched bit is set when a fault with the internal memory is detected. The source of the fault could be one of the following sources: • Parity check failure during or after STORE_USER_ALL. • During reset RESTORE (i.e. EEPROM restore at boot-up), either a mismatch between the EEPROM contents and the register contents OR a failure to pass parity checks. • When the user issues a RESTORE_USER_ALL command, a failure to pass parity checks. • Failure during the EEPROM programming sequence. 0h = No Memory faults. 1h = Memory fault detected.

Table 7-73. STATUS_CML Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3	RESERVED	R	0h	
2	RESERVED	R	0h	
1	OTH_COMM	R/W1C	0h	This latched bit is set if a communication fault other than the ones covered by bits [7:5] is detected. The source of the fault could be one of the following sources: • SMBus Clock Low Timeout. • Failure to communicate with the power-stage through the internal interface. 0h = No other communication fault. 1h = Other communication fault detected.
0	RESERVED	R	0h	

7.3.48 STATUS_OTHER (Address = 7Fh)

STATUS_OTHER is shown in Figure 7-54 and described in Table 7-74.

Return to the Summary Table.

Write Transaction: Write Byte
Read Transaction: Read Byte
Data Format: unsigned binary (1 byte)
NVM Back-up: No
Updates: On-the-fly

The STATUS_OTHER command returns one byte containing miscellaneous status information not covered by the other standard STATUS bytes. The status bits remain latched even after the fault or warning condition is resolved. The bits can be cleared by:

- CLEAR_FAULTS command
- Writing 1b to the target bit
- Toggling the ON_OFF_CONFIG mechanism of the rail
- Power cycle to reset the device

The OTHER bit in STATUS_WORD represents an ORing of the bits in this command. When any of the event occurs that sets a bit in this command, the OTHER bit is also set. Similarly, if all of the bits in this command are cleared, OTHER is also cleared.

All bits which can trigger SMB_ALERT# have a corresponding mask bit in the SMBALERT_MASK command.

Figure 7-54. STATUS_OTHER

7	6	5	4	3	2	1	0
SEC_ACT_CMPLT	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	FIRST_TO_ALERT
R/W1C-0h	R-0h	R-0h	R-0h	R-0h	R-0h	R-0h	R/W1C-0h

Table 7-74. STATUS_OTHER Field Descriptions

Bit	Field	Type	Reset	Description
7	SEC_ACT_CMPLT	R/W1C	0h	This latched bit is set upon completion of a security action, if enabled through the PMBus status alert triggering Security Action. 0h = No completed security action. 1h = A security action is complete.
6	RESERVED	R	0h	
5	RESERVED	R	0h	
4	RESERVED	R	0h	
3	RESERVED	R	0h	
2	RESERVED	R	0h	
1	RESERVED	R	0h	
0	FIRST_TO_ALERT	R/W1C	0h	This latched bit is set if the device asserted the SMB_ALERT# signal while the SMB_ALERT# signal was high. 0h = The device is not asserting SMB_ALERT# or the SMB_ALERT# signal was low when the device asserted SMB_ALERT#. 1h = The SMB_ALERT# signal was high when the device asserted SMB_ALERT#.

7.3.49 STATUS_MFR_SPECIFIC (Address = 80h)

STATUS_MFR_SPECIFIC is shown in Figure 7-55 and described in Table 7-75.

Return to the Summary Table.

Write Transaction: Write Byte
Read Transaction: Read Byte
Data Format: unsigned binary (1 byte)
NVM Back-up: No
Updates: On-the-fly

The STATUS_MFR_SPECIFIC command returns one byte containing manufacturer defined status information. The status bits remain latched even after the fault or warning condition is resolved. The bits can be cleared by:

- CLEAR_FAULTS command
- Writing 1b to the target bit
- Toggling the ON_OFF_CONFIG mechanism of the rail
- Power cycle to reset the device

The STS_MFR bit in STATUS_WORD represents an ORing of the bits in this command. When any of the event occurs that sets a bit in this command, the STS_MFR bit is also set. Similarly, if all of the bits in this command are cleared, STS_MFR is also cleared.

All bits which can trigger SMB_ALERT# have a corresponding mask bit in the SMBALERT_MASK command.

Figure 7-55. STATUS_MFR_SPECIFIC

7	6	5	4	3	2	1	0
DCM	OTF_BG	PS_FLT	PS_COMM_WRN	PC	RESERVED	PS_OT	PS_UV
R-0h	R/W1C-0h	R/W1C-0h	R/W1C-0h	R-0h	R-0h	R/W1C-0h	R/W1C-0h

Table 7-75. STATUS_MFR_SPECIFIC Field Descriptions

Bit	Field	Type	Reset	Description
7	DCM	R	0h	This LIVE (unlatched) bit is set to indicate discontinuous conduction mode. This bit does not trigger SMB_ALERT# nor assert the STS_MFR bit in STATUS_WORD or the STS_OTH in STATUS_BYTE as DCM is not a fault or warning condition. Instead, it provides information on the device's current operating mode. 0h = The device is operating in CCM 1h = The device is operating in DCM
6	OTF_BG	R/W1C	0h	This latched bit is set upon detection of controller's fixed bandgap overtemperature fault. 0h = No fixed controller overtemperature fault. 1h = A fixed controller overtemperature fault has occurred.
5	PS_FLT	R/W1C	0h	This latched bit is set upon detection of a power-stage fault. Power-stage faults which can set this bit includes: • VDRV voltage input to the power stage is insufficient (PS_UV). • Power-stage temperature exceeds the power-stage's fixed thermal shutdown (PS_OT). 0h = No power-stage faults. 1h = A power-stage fault has occurred.
4	PS_COMM_WRN	R/W1C	0h	This latched bit is set upon detection of a communications error with the power-stage. 0h = No power-stage communication fault. 1h = A power-stage communication fault has occurred.
3	PC	R	0h	This bit when set indicates a pulse-catcher warning in STATUS_PULSE_CATCHER. All bits in STATUS_PULSE_CATCHER must be cleared before this bit can be cleared. 0h = A pulse-catcher warning has not occurred. 1h = A pulse-catcher warning has occurred. The host should check STATUS_PULSE_CATCHER for more information.
2	RESERVED	R	0h	
1	PS_OT	R/W1C	0h	This latched bit is set upon detection of power-stage's fixed overtemperature fault. 0h = No fixed power-stage overtemperature fault. 1h = A fixed power-stage overtemperature fault has occurred.
0	PS_UV	R/W1C	0h	This LIVE (unlatched) bit is set upon detection of a power-stage undervoltage fault at the VDRV pin. 0h = No power-stage VDRV undervoltage fault. 1h = A power-stage VDRV undervoltage fault is present.

7.3.50 READ_VIN (Address = 88h)

READ_VIN is shown in Figure 7-56 and described in Table 7-76.

Return to the Summary Table.

Write Transaction: N/A
Read Transaction: Read Word
Data Format: LINEAR11
NVM Back-up: No
Updates: N/A
Update Rate: 380us
Supported Range: 4V - 31.96875V

The READ_VIN command returns input voltage in volts.

Figure 7-56. READ_VIN

15	14	13	12	11	10	9	8
EXPONENT[4:0]					RESERVED	READ_VIN[9:0]	
R-1Bh					R-0h	R-0h	
7	6	5	4	3	2	1	0
READ_VIN[9:0]							
R-0h							

Table 7-76. READ_VIN Field Descriptions

Bit	Field	Type	Reset	Description
15:11	EXPONENT[4:0]	R	1Bh	Linear format two's complement exponent. Fixed exponent of -5 resulting in a 0.03125V LSB.
10	RESERVED	R	0h	
9:0	READ_VIN[9:0]	R	0h	Linear format mantissa.

7.3.51 READ_IIN (Address = 89h)

READ_IIN is shown in Figure 7-57 and described in Table 7-77.

Return to the Summary Table.

Write Transaction: N/A
Read Transaction: Read Word
Data Format: LINEAR11
NVM Back-up: No
Updates: N/A
Update Rate: 95us
Supported Range: 0A - 63.9375A

The READ_IIN command returns input current in amps, sensed differentially across an external resistor between the I_IN_P and I_IN_M pins. For correct telemetry, configure PIN_SENSE_RES in the SVID_IMAX command to match the external sense resistance.

Figure 7-57. READ_IIN

15	14	13	12	11	10	9	8
EXPONENT[4:0]					READ_IIN[10:0]		
R-1Ch					R-0h		
7	6	5	4	3	2	1	0
READ_IIN[10:0]							
R-0h							

Table 7-77. READ_IIN Field Descriptions

Bit	Field	Type	Reset	Description
15:11	EXPONENT[4:0]	R	1Ch	Linear format two's complement exponent. Fixed exponent of -4 resulting in a 0.0625A LSB.
10:0	READ_IIN[10:0]	R	0h	Linear format two's complement mantissa.

7.3.52 READ_VOUT (Address = 8Bh)

READ_VOUT is shown in Figure 7-58 and described in Table 7-78.

Return to the Summary Table.

Write Transaction: N/A
Read Transaction: Read Word
Data Format: ULINEAR16 1.953mV LSB per VOUT_MODE
NVM Back-up: No
Updates: N/A
Update Rate: 190us
Supported Range: 0V - 6V

The READ_VOUT command returns output voltage in volts, sensed differentially between the VOSNS and GOSNS pins.

Figure 7-58. READ_VOUT

15	14	13	12	11	10	9	8
RESERVED	RESERVED	RESERVED	READ_VOUT[12:0]				
R-0h	R-0h	R-0h	R-0h				
7	6	5	4	3	2	1	0
READ_VOUT[12:0]							
R-0h							

Table 7-78. READ_VOUT Field Descriptions

Bit	Field	Type	Reset	Description
15	RESERVED	R	0h	
14	RESERVED	R	0h	
13	RESERVED	R	0h	
12:0	READ_VOUT[12:0]	R	0h	Linear format mantissa.

7.3.53 READ_IOUT (Address = 8Ch)

READ_IOUT is shown in Figure 7-59 and described in Table 7-79.

Return to the Summary Table.

Write Transaction: N/A
Read Transaction: Read Word
Data Format: LINEAR11
NVM Back-up: No
Updates: N/A
Update Rate: 95us
Supported Range: -64A - 63.9375A

The READ_IOUT command returns output current in amps.

Figure 7-59. READ_IOUT

15	14	13	12	11	10	9	8
EXPONENT_IOUT[4:0]					READ_IOUT[10:0]		
R-Xh					R-0h		
7	6	5	4	3	2	1	0
READ_IOUT[10:0]							
R-0h							

Table 7-79. READ_IOUT Field Descriptions

Bit	Field	Type	Reset	Description
15:11	EXPONENT_IOUT[4:0]	R	X	Linear format two's complement exponent. The exponent and resulting LSB depend on the value programmed to ICC_MAX in the SVID_IMAX command.
10:0	READ_IOUT[10:0]	R	0h	Linear format two's complement mantissa.

7.3.54 READ_TEMPERATURE_1 (Address = 8Dh)

READ_TEMPERATURE_1 is shown in Figure 7-60 and described in Table 7-80.

Return to the Summary Table.

Write Transaction: N/A
Read Transaction: Read Word
Data Format: LINEAR11
NVM Back-up: No
Updates: N/A
Update Rate: 380us
Supported Range: -256 deg C - 255.75 deg C

The READ_TEMPERATURE_1 command returns the controller's die temperature in degrees Celsius.

Figure 7-60. READ_TEMPERATURE_1

15	14	13	12	11	10	9	8
EXPONENT[4:0]					READ_TEMP1[10:0]		
R-1Eh					R-0h		
7	6	5	4	3	2	1	0
READ_TEMP1[10:0]							
R-0h							

Table 7-80. READ_TEMPERATURE_1 Field Descriptions

Bit	Field	Type	Reset	Description
15:11	EXPONENT[4:0]	R	1Eh	Linear format two's complement exponent. Fixed exponent of -2 resulting in a 0.25 deg C LSB.
10:0	READ_TEMP1[10:0]	R	0h	Linear format two's complement mantissa.

7.3.55 READ_PIN (Address = 97h)

READ_PIN is shown in Figure 7-61 and described in Table 7-81.

Return to the Summary Table.

Write Transaction: N/A
Read Transaction: Read Word
Data Format: LINEAR11
NVM Back-up: No
Updates: N/A
Update Rate: 95us
Supported Range: 0W - 1023W

The READ_PIN command returns input power in watts, which is calculated from the READ_VIN and READ_IIN telemetry.

Figure 7-61. READ_PIN

15	14	13	12	11	10	9	8
EXPONENT[4:0]					READ_PIN[10:0]		
R-0h					R-0h		
7	6	5	4	3	2	1	0
READ_PIN[10:0]							
R-0h							

Table 7-81. READ_PIN Field Descriptions

Bit	Field	Type	Reset	Description
15:11	EXPONENT[4:0]	R	0h	Linear format two's complement exponent. Fixed exponent of 0 resulting in a 1W LSB.
10:0	READ_PIN[10:0]	R	0h	Linear format two's complement mantissa.

7.3.56 PMBUS_REVISION (Address = 98h)

PMBUS_REVISION is shown in Figure 7-62 and described in Table 7-82.

Return to the Summary Table.

Write Transaction: N/A
Read Transaction: Read Byte
Data Format: unsigned binary (1 byte)
NVM Back-up: No
Updates: N/A

The PMBUS_REVISION command returns the revision of the PMBus specification to which the device is compliant.

Data Validity: Attempts to write PMBUS_REVISION are considered as invalid data or unsupported data (ivd) and the device responds as described in the IVD bit in STATUS_CML.

Figure 7-62. PMBUS_REVISION

7	6	5	4	3	2	1	0
PMBUS_REVISION[7:0]							
R-55h							

Table 7-82. PMBUS_REVISION Field Descriptions

Bit	Field	Type	Reset	Description
7:0	PMBUS_REVISION[7:0]	R	55h	Compliant to PMBus specification revision 1.4 Part I and Part II.

7.3.57 MFR_ID (Address = 99h)

MFR_ID is shown in Figure 7-63 and described in Table 7-83.

Return to the Summary Table.

Write Transaction: N/A
Read Transaction: Block Read
Data Format: unsigned binary (2 bytes)
NVM Back-up: No
Updates: N/A

The MFR_ID command provides a location to program the device with data identifying the manufacturer. This typically occurs during manufacturing.

Data Validity: Attempts to write MFR_ID are considered as invalid data or unsupported data (ivd) and the device responds as described in the IVD bit in STATUS_CML.

Figure 7-63. MFR_ID

15	14	13	12	11	10	9	8
MFR_ID[15:0]							
R-4954h							
7	6	5	4	3	2	1	0
MFR_ID[15:0]							
R-4954h							

Table 7-83. MFR_ID Field Descriptions

Bit	Field	Type	Reset	Description
15:0	MFR_ID[15:0]	R	4954h	2-bytes of read only data with specific byte values of Byte 1 = 54h and Byte 2 = 49h, which corresponds to the ASCII code for "TI".

7.3.58 MFR_MODEL (Address = 9Ah)

MFR_MODEL is shown in Figure 7-64 and described in Table 7-84.

Return to the Summary Table.

Write Transaction: Block Write
Read Transaction: Block Read
Data Format: unsigned binary (2 bytes)
NVM Back-up: EEPROM
Updates: On-the-fly

The MFR_MODEL command provides a location to program the device with data identifying the device model. This typically occurs during manufacturing.

Data Validity: Attempts to send a MFR_MODEL command for a Block Write with a byte count not equal to 2 bytes are considered as invalid data or unsupported data (ivd) and the device responds as described in the IVD bit in STATUS_CML.

Figure 7-64. MFR_MODEL

15	14	13	12	11	10	9	8
MFR_MODEL[15:0]							
R/W-XXXXh							
7	6	5	4	3	2	1	0
MFR_MODEL[15:0]							
R/W-XXXXh							

Table 7-84. MFR_MODEL Field Descriptions

Bit	Field	Type	Reset	Description
15:0	MFR_MODEL[15:0]	R/W	X	2-bytes of arbitrarily writable user-storable NVM for manufacturer model information.

7.3.59 MFR_REVISION (Address = 9Bh)

MFR_REVISION is shown in Figure 7-65 and described in Table 7-85.

Return to the Summary Table.

Write Transaction: Block Write
Read Transaction: Block Read
Data Format: unsigned binary (2 bytes)
NVM Back-up: EEPROM
Updates: On-the-fly

The MFR_REVISION command provides a location to program the device with data identifying the device's revision. This typically occurs during manufacturing.

Data Validity: Attempts to send a MFR_REVISION command for a Block Write with a byte count not equal to 2 bytes are considered as invalid data or unsupported data (ivd) and the device responds as described in the IVD bit in STATUS_CML.

Figure 7-65. MFR_REVISION

15	14	13	12	11	10	9	8
MFR_REVISION[15:0]							
R/W-XXXXh							
7	6	5	4	3	2	1	0
MFR_REVISION[15:0]							
R/W-XXXXh							

Table 7-85. MFR_REVISION Field Descriptions

Bit	Field	Type	Reset	Description
15:0	MFR_REVISION[15:0]	R/W	X	2-bytes of arbitrarily writable user-storable NVM for manufacturer revision information. This field's NVM is also used to set the value for the PMBus configuration file version located a Security byte addresses 04h and 05h. Additionally, the NVM for MFR_REVISION<7:0> is used to set the value for SVID register 1Eh CFG_FILE_ID.

7.3.60 IC_DEVICE_ID (Address = ADh)

IC_DEVICE_ID is shown in Figure 7-66 and described in Table 7-86.

Return to the Summary Table.

Write Transaction: N/A
Read Transaction: Block Read
Data Format: unsigned binary (6 bytes)
NVM Back-up: No
Updates: N/A

The IC_DEVICE_ID command is used to read the type of device or part number of the device that is connected to the PMBus interface.

Figure 7-66. IC_DEVICE_ID

47	46	45	44	43	42	41	40
PART_NUMBER_EXTENSION[7:0]							
R-0h							
39	38	37	36	35	34	33	32
PART_NUMBER_5[3:0]				PART_NUMBER_6[3:0]			
R-2h				R-7h			
31	30	29	28	27	26	25	24
PART_NUMBER_3[3:0]				PART_NUMBER_4[3:0]			
R-4h				R-Bh			
23	22	21	20	19	18	17	16
PART_NUMBER_1[3:0]				PART_NUMBER_2[3:0]			
R-5h				R-4h			
15	14	13	12	11	10	9	8
ASCII_I[7:0]							
R-49h							
7	6	5	4	3	2	1	0
ASCII_T[7:0]							
R-54h							

Table 7-86. IC_DEVICE_ID Field Descriptions

Bit	Field	Type	Reset	Description
47:40	PART_NUMBER_EXTENSION[7:0]	R	0h	
39:36	PART_NUMBER_5[3:0]	R	2h	
35:32	PART_NUMBER_6[3:0]	R	7h	
31:28	PART_NUMBER_3[3:0]	R	4h	
27:24	PART_NUMBER_4[3:0]	R	Bh	
23:20	PART_NUMBER_1[3:0]	R	5h	
19:16	PART_NUMBER_2[3:0]	R	4h	
15:8	ASCII_I[7:0]	R	49h	
7:0	ASCII_T[7:0]	R	54h	

7.3.61 IC_DEVICE_REV (Address = AEh)

IC_DEVICE_REV is shown in Figure 7-67 and described in Table 7-87.

Return to the Summary Table.

Write Transaction: N/A
Read Transaction: Block Read
Data Format: unsigned binary (1 byte)
NVM Back-up: No
Updates: N/A

The IC_DEVICE_REV command is used to read the revision of the device that is connected to the PMBus interface.

Figure 7-67. IC_DEVICE_REV

7	6	5	4	3	2	1	0
RESERVED	PS_IC[2:0]			DEVICE_REVISION[3:0]			
R-0h	R-3h			R-2h			

Table 7-87. IC_DEVICE_REV Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R	0h	
6:4	PS_IC[2:0]	R	3h	
3:0	DEVICE_REVISION[3:0]	R	2h	

7.3.62 EXTENDED_WRITE_PROTECT (Address = C7h)

EXTENDED_WRITE_PROTECT is shown in Figure 7-68 and described in Table 7-88.

Return to the Summary Table.

Write Transaction: Write Word
Read Transaction: Read Word
Data Format: Unsigned Binary (2 bytes)
NVM Back-up: EEPROM
Updates: On-the-fly

The EXTENDED_WRITE_PROTECT command configures additional register write protection beyond the standard PMBus write protection WRITE_PROTECT.

Figure 7-68. EXTENDED_WRITE_PROTECT

15	14	13	12	11	10	9	8
RESERVED	WPL	TRIML	VOCL	VOFCL	WRNL	IO_TEMP_FCL	MRGNL
R-0h	R/W-Xh	R/W-Xh	R/W-Xh	R/W-Xh	R/W-Xh	R/W-Xh	R/W-Xh
7	6	5	4	3	2	1	0
OPL	CFGL	VIFCL	SQNCL	MFRDL	PSKYL	RNVML	SNVML
R/W-Xh	R/W-Xh	R/W-Xh	R/W-Xh	R/W-Xh	R/W-Xh	R/W-Xh	R/W-Xh

Table 7-88. EXTENDED_WRITE_PROTECT Field Descriptions

Bit	Field	Type	Reset	Description
15	RESERVED	R	0h	
14	WPL	R/W	X	Write Protect Lock. Blocks writes to the standard WRITE_PROTECT, and controls writing of bits in EXTENDED_WRITE_PROTECT based on the setting in bit 2 PSKYL. An intended effect of the WPL bit is that once it is set, it cannot be cleared. Command List: WRITE_PROTECT, EXTENDED_WRITE_PROTECT 0h = WRITE_PROTECT and EXTENDED_WRITE_PROTECT commands are writable to any value. The value of PSKYL has no effect on access to either command. 1h = WRITE_PROTECT command is read only and access to EXTENDED_WRITE_PROTECT is determined by the value of the PSKYL bit. If PSKYL is set to 0, EXTENDED_WRITE_PROTECT is writable, but bits set to 1 cannot be cleared by writing a 0 to that bit. After a write to EXTENDED_WRITE_PROTECT, the value of EXTENDED_WRITE_PROTECT will be the bit-wise OR of the value prior to the write and the value written. If PSKYL is set to 1, EXTENDED_WRITE_PROTECT is read only.
13	TRIML	R/W	X	Trim Lock. Blocks writes to trim related commands, including commands which set the base output voltage and are typically set to a fixed value for the devices configuration. Command List: VOUT_TRIM, IMON_CAL, IIN_CAL, VOUT_SCALE_LOOP, VOUT_DROOP, VBOOT_DCLL, VBOOT_OFFSET_1 0h = Commands are writable unless write protected by WRITE_PROTECT 1h = Commands are read only
12	VOCL	R/W	X	Vout Command Lock. Blocks writes to commands related to setting the base output voltage and may be changed dynamically in the application. Command List: VOUT_MODE, VOUT_COMMAND 0h = Commands are writable unless write protected by WRITE_PROTECT 1h = Commands are read only
11	VOFCL	R/W	X	Vout Fault Configuration Lock. Blocks writes to commands related to configuration of output voltage faults. Command List: VOUT_MAX, VOUT_OV_FAULT_LIMIT, VOUT_OV_FAULT_RESPONSE, VOUT_UV_FAULT_LIMIT, VOUT_UV_FAULT_RESPONSE, VOUT_MIN 0h = Commands are writable unless write protected by WRITE_PROTECT 1h = Commands are read only
10	WRNL	R/W	X	Warnings Lock. Blocks writes to commands related to configuration of warnings, including masking which faults or warnings can assert SMB_ALERT#. Command List: SMBALERT_MASK VOUT_OV_WARN_LIMIT, VOUT_UV_WARN_LIMIT, IOUT_OC_WARN_LIMIT, OT_WARN_LIMIT, PIN_OP_WARN_LIMIT, ADV_TEL_BYTE (CH0_NM, CH2_NM restore value) There is one command this provides write protection to which warrants special clarification. The protection provided to ADV_TEL_BYTE is to provide the initial reset or restore value for the No More write protection for the NVM backed pulse-catcher channels. This effectively turns the No More write protection into Never Again write protection. As a result for this bit to take effect on the ADV_TEL_BYTE, a reset or restore to enable write protection. 0h = Commands are writable unless write protected by WRITE_PROTECT 1h = Commands are read only (ADV_TEL_BYTE requires a reset or restore)
9	IO_TEMP_FCL	R/W	X	Iout and Temperature Fault Configuration Lock. Blocks writes to commands related to configuration of output current and temperature faults. Command List: IOUT_OC_FAULT_LIMIT, IOUT_OC_FAULT_RESPONSE, OT_FAULT_LIMIT, OT_FAULT_RESPONSE 0h = Commands are writable unless write protected by WRITE_PROTECT 1h = Commands are read only

Table 7-88. EXTENDED_WRITE_PROTECT Field Descriptions (continued)

Bit	Field	Type	Reset	Description
8	MRGNL	R/W	X	Margin Lock. Blocks writes to commands related to margining the output voltage. Command List: VOUT_MARGIN_HIGH, VOUT_MARGIN_LOW, VOUT_TRANSITION_RATE 0h = Commands are writable unless write protected by WRITE_PROTECT 1h = Commands are read only
7	OPL	R/W	X	Operation Lock. Blocks writes to the OPERATION command. Command List: OPERATION 0h = Commands are writable unless write protected by WRITE_PROTECT 1h = Commands are read only
6	CFGL	R/W	X	Configuration Lock. Blocks writes to commands related to setting the device's configuration. Command List: FREQUENCY_SWITCH, NVM_PATCH_SPACE, CLOUD_OPTIONS, SYS_CFG_USER1, SVID_ADDR_CFG_USER, PMB_ADDR, COMP, SVID_IMAX, SVID_EXT_CAPABILITY_VIDOMAX 0h = Commands are writable unless write protected by WRITE_PROTECT 1h = Commands are read only
5	VIFCL	R/W	X	Vin Fault Configuration Lock. Blocks writes to commands related to configuration of input voltage faults. Command List: VIN_OV_FAULT_LIMIT 0h = Commands are writable unless write protected by WRITE_PROTECT 1h = Commands are read only
4	SQNCL	R/W	X	Sequence Lock. Blocks writes to commands related to configuration of sequencing. Command List: TON_DELAY, TON_RISE, TOFF_DELAY, TOFF_FALL, and ON_OFF_CONFIG, VIN_ON, VIN_OFF 0h = Commands are writable unless write protected by WRITE_PROTECT 1h = Commands are read only
3	MFRDL	R/W	X	Manufacturer Data Lock. Blocks writes to manufacturer data commands. Command List: MFR_ID, MFR_MODEL, MFR_REVISION 0h = Commands are writable unless write protected by WRITE_PROTECT 1h = Commands are read only
2	PSKYL	R/W	X	Passkey Lock. Blocks writes to the PASSKEY command. This is meant to prevent accidental or malicious attempts to set a PASSKEY on a device without one. If the PASSKEY is set but not locked, this bit will also prevent unsetting the PASSKEY. Command List: PASSKEY 0h = Commands are writable unless write protected by WRITE_PROTECT 1h = Commands are read only
1	RNVML	R/W	X	Restore NVM Lock. Blocks writes to the RESTORE_USER_ALL command. Command List: RESTORE_USER_ALL 0h = Commands are writable unless write protected by WRITE_PROTECT 1h = Commands are read only
0	SNVML	R/W	X	Store NVM Lock. Blocks writes to the STORE_USER_ALL command. This bit only blocks writes if set at power on reset or after a restore. To take effect, this bit must be stored to NVM followed by a power on reset or restore. Command List: STORE_USER_ALL 0h = Commands are writable unless write protected by WRITE_PROTECT 1h = Commands are read only after a power on reset or restore.

7.3.63 NVM_PATCH_SPACE (Address = CDh)

NVM_PATCH_SPACE is shown in Figure 7-69 and described in Table 7-89.

Return to the Summary Table.

Figure 7-69. NVM_PATCH_SPACE

39	38	37	36	35	34	33	32
RESERVED							
R/W-X							
31	30	29	28	27	26	25	24
RESERVED							
R/W-X							
23	22	21	20	19	18	17	16
RESERVED	RESERVED						
R-0h	R/W-X						
15	14	13	12	11	10	9	8
RESERVED							
R/W-X							
7	6	5	4	3	2	1	0
RESERVED	RESERVED						
R-0h	R/W-X						

Table 7-89. NVM_PATCH_SPACE Field Descriptions

Bit	Field	Type	Reset	Description
39:32	RESERVED	R/W	X	
31:24	RESERVED	R/W	X	
23	RESERVED	R	0h	
22:16	RESERVED	R/W	X	
15:8	RESERVED	R/W	X	
7	RESERVED	R	0h	
6:0	RESERVED	R/W	X	

7.3.64 CLOUD_OPTIONS (Address = CFh)

CLOUD_OPTIONS is shown in Figure 7-70 and described in Table 7-90.

Return to the Summary Table.

Figure 7-70. CLOUD_OPTIONS

7	6	5	4	3	2	1	0
RESERVED	RESERVED	RESERVED	RESERVED				
R/W-X	R-0h	R-0h	R/W-X				

Table 7-90. CLOUD_OPTIONS Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R/W	X	
6	RESERVED	R	0h	
5	RESERVED	R	0h	
4:0	RESERVED	R/W	X	

7.3.65 SYS_CFG_USER1 (Address = D0h)

SYS_CFG_USER1 is shown in Figure 7-71 and described in Table 7-91.

Return to the Summary Table.

Write Transaction: Write Word
Read Transaction: Read Word
Data Format: Unsigned binary (2 bytes)
NVM Back-up: EEPROM
Updates: On-the-fly. Some fields require the output to be disabled to take effect.

This register contains miscellaneous bits for system configuration.

Figure 7-71. SYS_CFG_USER1

15	14	13	12	11	10	9	8
FCCM	VOUT_CTRL[1:0]		EN_SS_DCM	PGD_DEL[1:0]		SEL_NOC[1:0]	
R/W-Xh	R/W-Xh		R/W-Xh	R/W-Xh		R/W-Xh	
7	6	5	4	3	2	1	0
SEL_ALRT_FN[1:0]		RESERVED		RESERVED		SEL_FIX_OVF	EN_FIX_OVF
R/W-Xh		R/W-X		R/W-X		R/W-Xh	R/W-Xh

Table 7-91. SYS_CFG_USER1 Field Descriptions

Bit	Field	Type	Reset	Description
15	FCCM	R/W	X	This bit selects between forced continuous mode conduction (FCCM) and discontinuous cooduction mode (DCM). PMBus writes are always accepted and the data is updated; however, in order for this bit to take effect, the output must be disabled. 0h = DCM operation is enabled and automatically entered or exited based on zero-crossing detection of the low-side MOSFET sensed current. 1h = FCCM.
14:13	VOUT_CTRL[1:0]	R/W	X	These bits determines how the output voltage of the rail is controlled. PMBus writes are always accepted and the data is updated; however, in order for this bit to take effect, the output must be disabled. 0h = SVID control 1h = SVID control and PMBus control 2h = PMBus control
12	EN_SS_DCM	R/W	X	This bit forces DCM during soft start. 0h = FCCM bit determines operation during soft start. 1h = The device operates in DCM during soft start, overriding the setting in the FCCM bit during softstart.
11:10	PGD_DEL[1:0]	R/W	X	These bits set a delay time from soft start completion to the PGOOD/VRRDY pin going high. This delay time is included only once per startup of the rail. 0h = 0.0015ms delay 1h = 0.5ms delay 2h = 1ms delay 3h = 2ms delay
9:8	SEL_NOC[1:0]	R/W	X	These bits select the under current fault (UCF) threshold that limits the low-side MOSFET sinking current. The threshold depends on ICC_MAX as shown in the following table.
7:6	SEL_ALRT_FN[1:0]	R/W	X	These bits select the functionality of the ALERT pin. 0h = SMB_ALERT#. All PMBus STATUS registers and their masking are used to determine assertion of the pin. 1h = PINALERT#. When the power measured by the SVID PIN telemetry (SVID registers PIN_H and PIN_L) is greater than the SVID register PIN_ALERT_TH, the pin asserts low and holds low for 100 ms. 2h = CAT_FAULT#. The pin asserts low if the device detects PS_FLT, OTF, UVF, or OVF statuses. Upon detection of UVF, this pin waits for a fixed delay time of 2 us and ignores the response delay programmed into TD_UV. Once a fault causes the CAT_FAULT# pin to assert low, the fault must be cleared for the pin to be released, such as through CLEAR_FAULTS or turning the output off and on through the ON_OFF_CONFIG mechanism. 3h = VR_HOT#.
5:4	RESERVED	R/W	X	
3:2	RESERVED	R/W	X	
1	SEL_FIX_OVF	R/W	X	This bit is used to select the fixed output voltage OVF threshold. The threshold at the output also depends VOUT_SCALE_LOOP as shown in the following table. 0h = Low threshold 1h = High threshold
0	EN_FIX_OVF	R/W	X	This bit is used to enable the fixed output voltage OVF threshold.

Table 7-92. SEL_NOC Enumeration Table

SEL_NOC	Sinking current limit	
	ICC_MAX < 0b010	ICC_MAX ≥ 0b010
0b00	-12	-24
0b01	-10	-20
0b10	-8	-16
0b11	-4	-8

Table 7-93. SEL_FIX_OVF Enumeration Table

VOUT_SCALE_LOOP	SEL_FIX_OVF	Fixed OVF threshold (V)
1	0	0.75
	1	0.9
0.5	0	1.5
	1	1.8
0.25	0	2.4
	1	3.0
0.125	0	4.8
	1	6.0

7.3.66 SVID_ADDR_CFG_USER (Address = D1h)

SVID_ADDR_CFG_USER is shown in Figure 7-72 and described in Table 7-94.

Return to the Summary Table.

Write Transaction: Write Word
Read Transaction: Read Word
Data Format: Unsigned binary (2 bytes)
NVM Back-up: EEPROM
Updates: On-the-fly. PMBus writes are always accepted and the data is updated; however, in order for this bit to take effect, the output must be disabled.

This register contains the bits to configure SVID address and other SVID settings.

Figure 7-72. SVID_ADDR_CFG_USER

15	14	13	12	11	10	9	8
PROTOCOL_ID[1:0]		RESERVED		RESERVED			
R/W-Xh		R/W-X		R/W-X			
7	6	5	4	3	2	1	0
RESERVED		RESERVED		RESERVED		RESERVED	
R/W-X		R/W-X		R/W-X		R/W-X	

Table 7-94. SVID_ADDR_CFG_USER Field Descriptions

Bit	Field	Type	Reset	Description
15:14	PROTOCOL_ID[1:0]	R/W	X	These bits set the Protocol ID in SVID register 05h. 0h = Protocol ID set to 04h (VR13, 10mV) 1h = Protocol ID set to 07h (VR13, 5mV) 2h = Protocol ID set to 09h (VR14, 5mV) 3h = Protocol ID set to 0Ah (VR14, 10mV)
13:12	RESERVED	R/W	X	
11:8	RESERVED	R/W	X	
7:6	RESERVED	R/W	X	
5:4	RESERVED	R/W	X	
3:2	RESERVED	R/W	X	
1:0	RESERVED	R/W	X	

7.3.67 PMBUS_ADDR (Address = D2h)

PMBUS_ADDR is shown in Figure 7-73 and described in Table 7-95.

Return to the Summary Table.

Write Transaction: Write Word
Read Transaction: Read Word
Data Format: Unsigned Binary (2 bytes)
NVM Back-up: EEPROM
Updates: On-the-fly. STORE_USER_ALL then power on reset required for the device to respond to a new PMBus address.

This command contains bits for setting the PMBus address for the device and other configuration settings for the PMB_ADDR pin.

Figure 7-73. PMBUS_ADDR

15	14	13	12	11	10	9	8
RESERVED	PMB_ADDR[6:0]						
R-0h	R/W-Xh						
7	6	5	4	3	2	1	0
OVRD_PMB_ADDR	SEL_PMB_DAT_DEL[1:0]		RESERVED	SEL_PSTR_ADDR_BASE[3:0]			
R/W-Xh	R/W-Xh		R-0h	R/W-Xh			

Table 7-95. PMBUS_ADDR Field Descriptions

Bit	Field	Type	Reset	Description
15	RESERVED	R	0h	
14:8	PMB_ADDR[6:0]	R/W	X	This 7-bit code determines the PMBus address of the part. After power on reset, the value readback from this field are the address the device responds to. Refer to the PMB_ADDR Pinstrap section for details on how pinstrapping affects this field.
7	OVRD_PMB_ADDR	R/W	X	This bit determines if the PMBus address is from pinstrap or from NVM setting. Setting this bit does not override the selection between option 0 and option 1 described in the PMB_ADDR Pinstrap section. In order for this bit to take effect, the user has to write this bit, store to EEPROM, and power-cycle the part. 0h = PMBus address set by PMB_ADDR pinstrap pin. 1h = PMBus address set by NVM bits in the PMB_ADDR field in within this command.
6:5	SEL_PMB_DAT_DEL[1:0]	R/W	X	This bit field enables the addition of internal delay to the PMBus data input. This delay affects only incoming data and does not delay data out of the device. Adding internal delay may be necessary if a PMBus controller is designed to transition the data line simultaneously with the clock falling edge. Without appropriate delay, differences in fall times between data and clock lines can cause the device to detect the data falling edge before the clock falling edge, incorrectly interpreting it as a START condition. However, excessive delay settings can cause issues with PMBus controllers that transition data lines near the minimum data setup time (50ns for 1 MHz Class). TI does not recommend adding internal delay when using such controllers. These configuration bits take effect immediately after the PMBus transaction completes, without requiring a STORE-RESTORE cycle. 0h = No delay 1h = Short delay (100ns) 2h = Medium delay (200ns) 3h = Long delay (300ns)
4	RESERVED	R	0h	
3:0	SEL_PSTR_ADDR_BASE[3:0]	R/W	X	The bit field sets bits 6:3 of the PMBus address set through the PMB_ADDR pinstrap. For changes to take effect, the user must write the new value, store to EEPROM, and power-cycle the device. The new pinstrapped PMBus address becomes active only after a complete power cycle.

7.3.68 IMON_CAL (Address = D4h)

IMON_CAL is shown in Figure 7-74 and described in Table 7-96.

Return to the Summary Table.

Write Transaction: Write Byte
Read Transaction: Read Byte
Data Format: Unsigned Binary (1 byte)
NVM Back-up: EEPROM
Updates: On-the-fly

This register contains the bits for PMBus READ_IOUT and SVID IOUT_H/L calibration.

Figure 7-74. IMON_CAL

7	6	5	4	3	2	1	0
IMON_GAIN_CAL[3:0]				IMON_OFS_CAL[3:0]			
R/W-Xh				R/W-Xh			

Table 7-96. IMON_CAL Field Descriptions

Bit	Field	Type	Reset	Description
7:4	IMON_GAIN_CAL[3:0]	R/W	X	These bits contains the PMBus READ_IOUT and SVID IOUT_H/L gain calibration. 0h = -3.52% 1h = -3.13% 2h = -2.34% 3h = -1.95% 4h = -1.56% 5h = -1.17% 6h = -0.39% 7h = 0.00% 8h = 0.39% 9h = 1.17% Ah = 1.56% Bh = 1.95% Ch = 2.34% Dh = 3.13% Eh = 3.52% Fh = 3.91%
3:0	IMON_OFS_CAL[3:0]	R/W	X	These bits contains the PMBus READ_IOUT and SVID IOUT_H/L offset calibration. This register gives flexibility to change nominal reporting by +/-5A the maximum supported ICC_MAX. 0h = -2.00A 1h = -1.75A 2h = -1.50A 3h = -1.25A 4h = -1.00A 5h = -0.75A 6h = -0.50A 7h = -0.25A 8h = 0.00A 9h = 0.25A Ah = 0.50A Bh = 0.75A Ch = 1.00A Dh = 1.25A Eh = 1.50A Fh = 1.75A

7.3.69 COMP (Address = D5h)

COMP is shown in Figure 7-75 and described in Table 7-97.

Return to the Summary Table.

Write Transaction: Block Write
Read Transaction: Block Read
Data Format: Unsigned Binary (5 bytes)
NVM Back-up: EEPROM
Updates: On-the-fly

This register contains feedback compensation settings for the regulated rail.

Figure 7-75. COMP

39	38	37	36	35	34	33	32
RESERVED				RESERVED			
R-0h				R-0h			
31	30	29	28	27	26	25	24
RESERVED		RESERVED		RESERVED		RESERVED	
R-0h		R-0h		R-0h		R-0h	
23	22	21	20	19	18	17	16
SEL_VCM	SEL_RAMP_SAT[1:0]		COMP_CLMP[1:0]		RAMP[2:0]		
R/W-Xh	R/W-Xh		R/W-Xh		R/W-Xh		
15	14	13	12	11	10	9	8
AC_GAIN[3:0]				ACLL[3:0]			
R/W-Xh				R/W-Xh			
7	6	5	4	3	2	1	0
INT_GAIN[1:0]		INT_TIME[2:0]			RESERVED	SEL_CSRISE[1:0]	
R/W-Xh		R/W-Xh			R-0h	R/W-Xh	

Table 7-97. COMP Field Descriptions

Bit	Field	Type	Reset	Description
39:36	RESERVED	R	0h	
35:32	RESERVED	R	0h	
31:30	RESERVED	R	0h	
29:27	RESERVED	R	0h	
26	RESERVED	R	0h	
25:24	RESERVED	R	0h	
23	SEL_VCM	R/W	X	This bit sets the common mode voltage (VCM) for the control loop. 0h = Recommended setting 1h = VCM increased by 50mV
22:21	SEL_RAMP_SAT[1:0]	R/W	X	These bits determine the ramp saturation level. Lower ramp saturation level may result in lower ramp amplitude. 0h = 1x 1h = 1.1x 2h = 1.25x (recommended) 3h = 1.5x
20:19	COMP_CLMP[1:0]	R/W	X	These bits set an internal clamp threshold. 0h = Disabled 1h = Disabled 2h = 700mV (recommended) 3h = 800mV
18:16	RAMP[2:0]	R/W	X	These bits determine the ramp amplitude in mV. 0h = 40mV 1h = 60mV 2h = 80mV 3h = 100mV 4h = 120mV 5h = 160mV 6h = 200mV 7h = 240mV

Table 7-97. COMP Field Descriptions (continued)

Bit	Field	Type	Reset	Description
15:12	AC_GAIN[3:0]	R/W	X	These bits determine the AC gain setting. 0h = 0.3 1h = 0.5 2h = 1 3h = 1.5 4h = 2 5h = 2.5 6h = 3 7h = 3.5 8h = 4 9h = 5 Ah = 6 Bh = 7
11:8	ACLL[3:0]	R/W	X	These bits determine the AC load-line setting in mOhm. 0h = 0.5mOhm 1h = 1mOhm 2h = 1.5mOhm 3h = 2mOhm 4h = 2.5mOhm 5h = 3mOhm 6h = 3.5mOhm 7h = 4mOhm 8h = 5mOhm 9h = 6mOhm Ah = 7mOhm Bh = 9mOhm Ch = 10mOhm Dh = 12mOhm Eh = 13mOhm Fh = 15mOhm
7:6	INT_GAIN[1:0]	R/W	X	These bits determine the integrator gain. 0h = 2 1h = 1.5 2h = 1 3h = 0.5
5:3	INT_TIME[2:0]	R/W	X	These bits determine the integrator time constant in us. 0h = 0.25us 1h = 1us 2h = 3us 3h = 4.5us 4h = 6.25us 5h = 8us 6h = 10us 7h = 20us
2	RESERVED	R	0h	
1:0	SEL_CSRISE[1:0]	R/W	X	Set these bits based on the output inductor value for the current sensing circuit as shown in the following table. Round the inductance value up to the nearest supported value.

Table 7-98. Recommended SEL_CSRISE for selected inductor values

Inductor Value (nH)(1)			Suggested SEL_CSRISE
VOUT_SCALE_LOOP = 1V/V or 0.5V/V	VOUT_SCALE_LOOP = 0.25V/V	VOUT_SCALE_LOOP = 0.125V/V	
100	200	400	0b00
200	400	800	0b01
300	600	1200	0b10
400	800	1600	0b11

(1) Round selected inductance value up to the nearest available setting.

7.3.70 VBOOT_DCLL (Address = D6h)

VBOOT_DCLL is shown in Figure 7-76 and described in Table 7-99.

Return to the Summary Table.

Write Transaction: Block Write
Read Transaction: Block Read
Data Format: Unsigned Binary (3 bytes)
NVM Back-up: EEPROM
Updates: On-the-fly

This register contains the VBOOT option 0 setting, DCLL option 0 and 1 settings, and other configuration bits for the device.

Figure 7-76. VBOOT_DCLL

23	22	21	20	19	18	17	16
ALLOW_RSVD_DEV_ADDR	RESERVED		VBOOT_0[4:0]				
R/W-Xh	R-0h		R/W-Xh				
15	14	13	12	11	10	9	8
SEL_OTF_BG[2:0]			DCLL_0[4:0]				
R/W-X			R/W-Xh				
7	6	5	4	3	2	1	0
RESERVED		RESERVED	DCLL_1[4:0]				
R-0h		R/W-0h	R/W-Xh				

Table 7-99. VBOOT_DCLL Field Descriptions

Bit	Field	Type	Reset	Description
23	ALLOW_RSVD_DEV_ADDR	R/W	X	This bit determines whether the device responds to reserved PMBus addresses 0x28, 0x37, and 0x61. 0h = Device does not respond when configured for reserved addresses. 1h = Device acknowledges when configured for reserved addresses.
22:21	RESERVED	R	0h	
20:16	VBOOT_0[4:0]	R/W	X	These bits contains VBOOT option 0 setting that is used for the VREF DAC target for soft-start purposes. With the VBOOT value is setting the VREF DAC target, the appropriate VOUT_SCALE_LOOP or PROTOCOL_ID must be programmed to set the internal divider gain and achieve the desired output voltage. Setting the VREF DAC target directly multiplies the number of available VBOOT voltages by the number of internal gain settings. VBOOT_0 or VBOOT_1 are selected through the PMB_ADDR pin to determine the effective VBOOT voltage. There is nothing preventing the VBOOT_0 (or VBOOT_1) value from being updated in any state. If the active VBOOT is updated while in the soft-start state, the output voltage will slew to the updated VBOOT setting.
15:13	SEL_OTF_BG[2:0]	R/W	X	These bits to select different OTF_BG thresholds. TI does not recommend setting this to 0b100 or 0b101. 0h = 142degC Rise, 128degC Fall 1h = 131degC Rise, 118degC Fall 2h = 120degC Rise, 107degC Fall 3h = 110degC Rise, 98degC Fall 4h = 192degC Rise, 177degC Fall 5h = 178degC Rise, 163degC Fall 6h = 166degC Rise, 151degC Fall 7h = 154degC Rise, 140degC Fall
12:8	DCLL_0[4:0]	R/W	X	These bits select the DC load-line with a format of 0.1mOhm/LSB, resulting in a DCLL range of 0mOhm to 3.1mOhm in 0.1mOhm increments. DCLL_0 or DCLL_1 are selected through the PMB_ADDR pin.
7:6	RESERVED	R	0h	
5	RESERVED	R/W	0h	
4:0	DCLL_1[4:0]	R/W	X	These bits set the option 1 DCLL selected through the PMB_ADDR pin. Refer to the DCLL_0 description for more details.

7.3.71 VBOOT_OFFSET_1 (Address = D7h)

VBOOT_OFFSET_1 is shown in Figure 7-77 and described in Table 7-100.

Return to the Summary Table.

Write Transaction: Write Word
Read Transaction: Read Word
Data Format: Unsigned Binary (2 bytes)
NVM Back-up: EEPROM
Updates: On-the-fly

This command contains the information for the second option (option 1) for the boot-up voltage VBOOT and SVID register OFFSET (33h).

Figure 7-77. VBOOT_OFFSET_1

15	14	13	12	11	10	9	8
RESERVED	RESERVED	PSTR_RESULT_OPT	OFFSET_1[4:0]				
R-0h	R-0h	R-0h	R/W-Xh				
7	6	5	4	3	2	1	0
RESERVED	RESERVED	RESERVED	VBOOT_1[4:0]				
R/W-X	R/W-X	R-0h	R/W-Xh				

Table 7-100. VBOOT_OFFSET_1 Field Descriptions

Bit	Field	Type	Reset	Description
15	RESERVED	R	0h	
14	RESERVED	R	0h	
13	PSTR_RESULT_OPT	R	0h	This read only bit indicates if option 0 or option 1 was selected through pinstrap of the PMB_ADDR pin. 0h = Option 0 1h = Option 1
12:8	OFFSET_1[4:0]	R/W	X	These bits set the option 1 OFFSET selected through the PMB_ADDR pin. They are mapped directly to the SVID (33h) OFFSET register, with the MSB sign extended for negative offsets.
7	RESERVED	R/W	X	
6	RESERVED	R/W	X	
5	RESERVED	R	0h	
4:0	VBOOT_1[4:0]	R/W	X	These bits set the option 1 VBOOT selected through the PMB_ADDR pin. Refer to the VBOOT_0 description for more details.

7.3.72 IIN_CAL (Address = D8h)

IIN_CAL is shown in Figure 7-78 and described in Table 7-101.

Return to the Summary Table.

Write Transaction: Write Byte
Read Transaction: Read Byte
Data Format: Unsigned Binary (2 bytes)
NVM Back-up: EEPROM
Updates: On-the-fly

This register contains the bits for PMBus READ_IIN and SVID IIN_H/L calibration.

Figure 7-78. IIN_CAL

7	6	5	4	3	2	1	0
IIN_GAIN_CAL[3:0]				IIN_OFS_CAL[3:0]			
R/W-Xh				R/W-Xh			

Table 7-101. IIN_CAL Field Descriptions

Bit	Field	Type	Reset	Description
7:4	IIN_GAIN_CAL[3:0]	R/W	X	These bits contains the PMBus READ_IIN and SVID IIN_H/L gain calibration. 0h = -3.52% 1h = -3.13% 2h = -2.34% 3h = -1.95% 4h = -1.56% 5h = -1.17% 6h = -0.39% 7h = 0.00% 8h = 0.39% 9h = 1.17% Ah = 1.56% Bh = 1.95% Ch = 2.34% Dh = 3.13% Eh = 3.52% Fh = 3.91%
3:0	IIN_OFS_CAL[3:0]	R/W	X	These bits contains the PMBus READ_IIN and SVID IIN_H/L offset calibration. This register gives flexibility to change nominal reporting by +/-2A. 0h = -2.00A 1h = -1.75A 2h = -1.50A 3h = -1.25A 4h = -1.00A 5h = -0.75A 6h = -0.50A 7h = -0.25A 8h = 0.00A 9h = 0.25A Ah = 0.50A Bh = 0.75A Ch = 1.00A Dh = 1.25A Eh = 1.50A Fh = 1.75A

7.3.73 SVID_IMAX (Address = DAh)

SVID_IMAX is shown in Figure 7-79 and described in Table 7-102.

Return to the Summary Table.

Write Transaction: Write Word
Read Transaction: Read Word
Data Format: Unsigned Binary (2 bytes)
NVM Back-up: EEPROM
Updates: On-the-fly

This register contains the bits for ICC_MAX and input current sensing configurations.

Figure 7-79. SVID_IMAX

15	14	13	12	11	10	9	8
ICC_MAX[2:0]			RESERVED	PEC_REQ	EN_AIMON	SEL_ZC[1:0]	
R/W-Xh			R/W-0h	R/W-Xh	R/W-Xh	R/W-Xh	
7	6	5	4	3	2	1	0
RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	PIN_SENSE_RES[2:0]		
R-0h	R-0h	R-0h	R/W-X	R-0h	R/W-Xh		

Table 7-102. SVID_IMAX Field Descriptions

Bit	Field	Type	Reset	Description
15:13	ICC_MAX[2:0]	R/W	X	These bits set the ICC_MAX setting in the SVID register 21h and the READ_IOUT exponent as shown in the following table. Additionally these bits set the internal telemetry gain. If the SVID interface is not being used, TI recommends using ICC_MAX >= 0b010.
12	RESERVED	R/W	0h	
11	PEC_REQ	R/W	X	This bit determines how the device handles transactions without PEC bytes. 0h = Accept commands without PEC; validate PEC when provided. 1h = Reject all commands without PEC as invalid PEC.
10	EN_AIMON	R/W	X	This bit enables the analog IMON output function on the PMB_ADDR/IMON pin. 0h = Analog IMON output disabled 1h = Analog IMON output enabled. Additionally, for this function to be enabled, the PMB_ADDR resistor to ground must be 11.3kOhm or larger.
9:8	SEL_ZC[1:0]	R/W	X	This bit field selects the zero crossing thresholds. 0h = 1200mA Enter DCM, 1500mA Exit DCM 1h = 900mA Enter DCM, 1200mA Exit DCM 2h = 0mA Enter DCM, 300mA Exit DCM 3h = -300mA Enter DCM, 0mA Exit DCM
7	RESERVED	R	0h	
6	RESERVED	R	0h	
5	RESERVED	R	0h	
4	RESERVED	R/W	X	
3	RESERVED	R	0h	
2:0	PIN_SENSE_RES[2:0]	R/W	X	Set these bits based on the external sensing resistor used for input current/power measurement as shown in the following table.

Table 7-103. ICC_MAX Enumeration Table

ICC_MAX	ICC_MAX (A)	READ_IOUT exponent
0b000	6	-6
0b001	8	
0b010	12	-5
0b011	16	
0b100	20	
0b101	24	-4
0b110	32	
0b111	40	

Table 7-104. PIN_SENSE_RES Enumeration Table

External R_{SENSE} (mΩ)	PIN_SENSE_RES	Internal Gain (V/V)	Maximum input current sensed (A)
4	0b000	12.5	16
3	0b001	12.5	21.3
2	0b010	25	16
1	0b011	20	40
1	0b100	25	32
0.5	0b101	40	40
0.5	0b110	50	32
0.25	0b111	50	64

7.3.74 SVID_EXT_CAPABILITY_VIDOMAX (Address = DBh)

SVID_EXT_CAPABILITY_VIDOMAX is shown in Figure 7-80 and described in Table 7-105.

Return to the Summary Table.

Write Transaction: Write Word
Read Transaction: Read Word
Data Format: Unsigned Binary (2 bytes)
NVM Back-up: EEPROM
Updates: On-the-fly

This register consists of 2 parts. The first part, bits 15:9, containing direct copy of the bits 7:1 in the SVID (09h) VIDO_MAX_H_CAPA register indicating feature capabilities of the device. The second part, bits 8:0, set VIDO_MAX value for the SVID interface. In the SVID interface this is split across two registers: bit 0 of (09h) VIDO_MAX_H_CAPA and bits 7:0 of (0Ah) VIDO_MAX_L.

Data Validity: Changes through this command are only allowed when the output is disabled. When the output is enabled attempts to write will result in a NACK of the unsupported data and the received value will be ignored. The CML bit in the STATUS_BYTE and the IVD bit in the (7Eh) STATUS_CML registers will be set.

Figure 7-80. SVID_EXT_CAPABILITY_VIDOMAX

15	14	13	12	11	10	9	8
PSYS_WARN	IMON_CAL	DFDS	DFDV	HI_PRES	ICC_IN_MAX	RESERVED	VIDO_MAX[8:0]
R-0h	R-0h	R-0h	R-0h	R-1h	R-1h	R-0h	R/W-XXh
7	6	5	4	3	2	1	0
VIDO_MAX[8:0]							
R/W-XXh							

Table 7-105. SVID_EXT_CAPABILITY_VIDOMAX Field Descriptions

Bit	Field	Type	Reset	Description
15	PSYS_WARN	R	0h	When 1, this indicates that PsysWarn is supported in SVID. PsysWarn is NOT supported.
14	IMON_CAL	R	0h	When 1, this indicates that SVID IMON calibration is supported. SVID IMON_CAL is NOT supported.
13	DFDS	R	0h	When 1, this indicates that Design for Debug SVID_logs is supported. DFDS is NOT supported.
12	DFDV	R	0h	When 1, this indicates that Design for Debug VR_event_logs is supported. DFDV is NOT supported.
11	HI_PRES	R	1h	When 1, this indicates that high precision telemetry is supported. HI_PRES is supported.
10	ICC_IN_MAX	R	1h	This bit indicates if IIN telemetry is reported as a fraction of IccInMax is supported. 0h = The device does NOT support IIN telemetry reported as a fraction of IccInMax. 1h = The device supports IIN telemetry reported as a fraction of IccInMax.
9	RESERVED	R	0h	
8:0	VIDO_MAX[8:0]	R/W	X	This field sets the maximum value of VID+Offset allowed via SVID. Exceeding VIDO_MAX with (VID+Offset) will cause a REJ for individual rails requests and a NACK for all-call requests.

7.3.75 FUSION_ID0 (Address = FCh)

FUSION_ID0 is shown in Figure 7-81 and described in Table 7-106.

Return to the Summary Table.

Figure 7-81. FUSION_ID0

15	14	13	12	11	10	9	8
FUSION_ID0[15:0]							
R-2C0h							
7	6	5	4	3	2	1	0
FUSION_ID0[15:0]							
R-2C0h							

Table 7-106. FUSION_ID0 Field Descriptions

Bit	Field	Type	Reset	Description
15:0	FUSION_ID0[15:0]	R	2C0h	

7.3.76 FUSION_ID1 (Address = FDh)

FUSION_ID1 is shown in Figure 7-82 and described in Table 7-107.

Return to the Summary Table.

Figure 7-82. FUSION_ID1

47	46	45	44	43	42	41	40
FUSION_ID1[47:0]							
R-4B434F4C4954h							
39	38	37	36	35	34	33	32
FUSION_ID1[47:0]							
R-4B434F4C4954h							
31	30	29	28	27	26	25	24
FUSION_ID1[47:0]							
R-4B434F4C4954h							
23	22	21	20	19	18	17	16
FUSION_ID1[47:0]							
R-4B434F4C4954h							
15	14	13	12	11	10	9	8
FUSION_ID1[47:0]							
R-4B434F4C4954h							
7	6	5	4	3	2	1	0
FUSION_ID1[47:0]							
R-4B434F4C4954h							

Table 7-107. FUSION_ID1 Field Descriptions

Bit	Field	Type	Reset	Description
47:0	FUSION_ID1[47:0]	R	4B434F4C4954h	

8 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

8.1 Application Information

The TPS544B27W device is a highly-integrated, synchronous, step-down DC/DC converter. The TPS544B27W has a simple design procedure where programmable parameters can be configured by PMBus and stored to non-volatile memory (NVM) to minimize external component count.

8.2 Typical Application

8.2.1 Application

This design describes a 1.8V application.

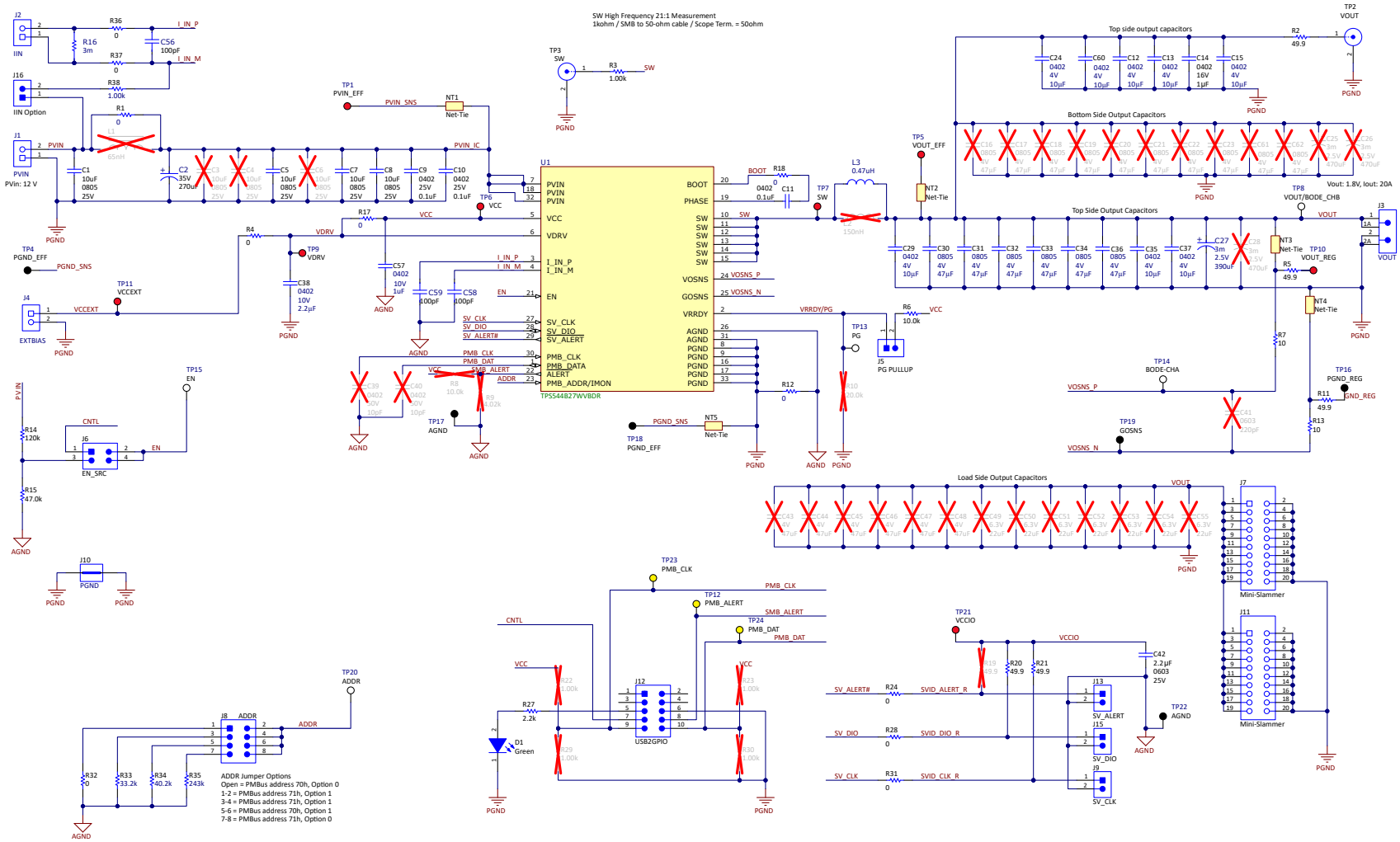


Figure 8-1. 1.8V Output Application

8.2.2 Design Requirements

This design uses the parameters listed in the following table.

Table 8-1. Design Parameters

PARAMETER	VALUE
Input voltage	10.8V – 13.2V
Output voltage	1.8V
Output current	20A
Switching frequency	800kHz
DC load line	0mΩ
PMBus address	70h

8.2.3 Detailed Design Procedure

This design example leverages the requirements for a 1.8V rail in a server platform. The following steps illustrate how to select key components.

8.2.3.1 Inductor Selection

The inductor must be selected such that the transient performance and ripple requirements are balanced for a particular design. In general, a small inductance increases loop bandwidth leading to be better transient response at the expense of high current and voltage ripple. In this example, a 470nH, 4.2mΩ inductor is used per Intel Oak Stream reference design.

8.2.3.2 Input Capacitor Selection

Input capacitors must be selected to provide reduction in input voltage ripple and high-frequency bypassing, which in return reduces switching stress on the power stage MOSFETs internal to the device. In this example, two 0.1µF, 25V, 0402 must be placed as close as possible to pin 7 and pin 18 of the device on the same layer as the IC on the PCB. In addition, 4 × 10µF or 4 × 22µF ceramic capacitors are used. A 270µF, 35V bulk capacitor can also be added to represent bulk input capacitance that is typically on a server mother board.

8.2.3.3 Output Capacitor Selection

To meet the output voltage ripple and load transient requirements, use a 1µF and 4 × 47µF/4V/X6S/0805 ceramic capacitors and 390µF Aluminum polymer capacitor local to the output of inductor of the regulator. Additionally, use 8 × 10µF/4V/X6S /0402 and 2 × 47µF/4V/X6S /0805 near the load.

8.2.3.4 VCC/VDRV Bypass Capacitor

Use a minimum of 1µF, 10V rated capacitor for bypassing of the VDRV pin to PGND. Use a minimum 1µF, 10V rated capacitor for bypassing of the VCC pin to AGND. TI recommends connecting the VCC bypass capacitor to AGND, but this is not required. The VDRV bypass capacitor must refer to PGND to minimize the length of high-frequency gate drive current path. In total, two 1µF capacitors or a single 2.2µF capacitor is required for bypassing VCC and VDRV.

8.2.3.5 BOOT Capacitor Selection

Use a minimum of a 0.1µF capacitor connected from BOOT (pin 20) to PHASE (pin 19). An optional series boot resistor of 0Ω to 2.2Ω can be added.

8.2.3.6 RSENSE Selection

In applications which require the input current or input power telemetry feature, a 3mΩ resistor can be selected to sense the input current on a 12V bus. The sensed input current and the sensed input voltage on I_IN_M Pin 4 are used to calculate the total input power. The input power information can be read through telemetry registers and used for power management.

If input current and input power sensing are not used, connect the I_IN_M and I_IN_P pins together so that the reported current is always 0. Also connect them to the PVIN input rail for input voltage telemetry.

8.2.3.7 I_IN_P and I_IN_M Capacitor Selection

Use a 100pF/25V/0402 ceramic capacitor referenced to PGND on both the I_IN_P Pin 3 and I_IN_M Pin 4. Place another 100pF/25V/0402 ceramic capacitor between Pin 3 and Pin 4. These decoupling capacitors minimize the impact from switching noise on the 12V bus and thus help the device to achieve high accuracy on input current reporting.

8.2.3.8 VRRDY Pullup Resistor Selection

The VRRDY output is an open-drain output and must be pulled up externally through a pullup resistor. Place a pullup resistor, within a 1kΩ to 100kΩ range at the VRRDY Pin 2. In this example, VRRDY is pulled up to VCC/VDRV with a 10kΩ resistor.

8.2.3.9 PMBus® Address Resistor Selection

See also Table 6-6 for the list of PMBus addresses selectable by an external resistor. A resistor between the PMB_ADDR pin 23 and AGND sets the preconfigured PMBus address in the memory map. In this application, a resistor selects a PMBus address of 70h.

8.2.4 Application Curves

Figure 8-2 through Figure 8-21 present typical performance curves for TPS544B27EVM. The input voltage is 12V and output voltage is 1.8V, unless otherwise noted

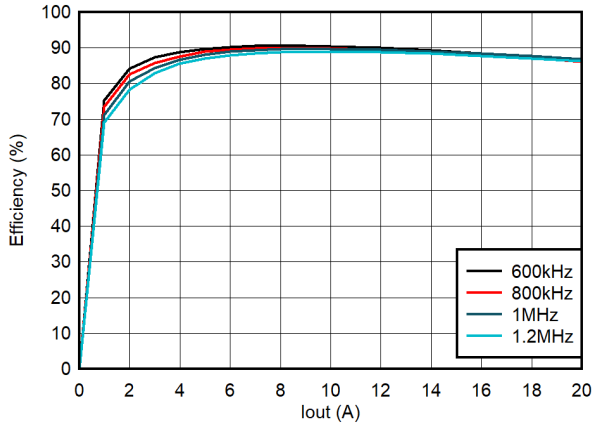


Figure 8-2. Efficiency, FCCM, Internal LDO

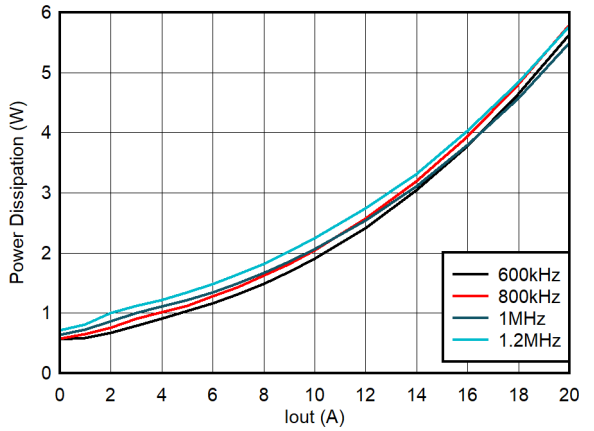


Figure 8-3. Power Dissipation, FCCM, Internal LDO

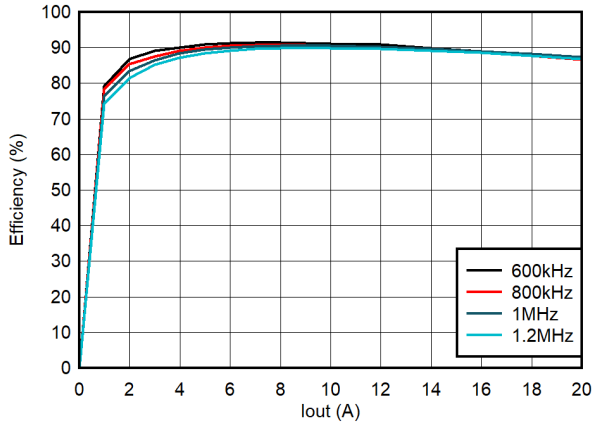


Figure 8-4. Efficiency, FCCM, External 5V Bias

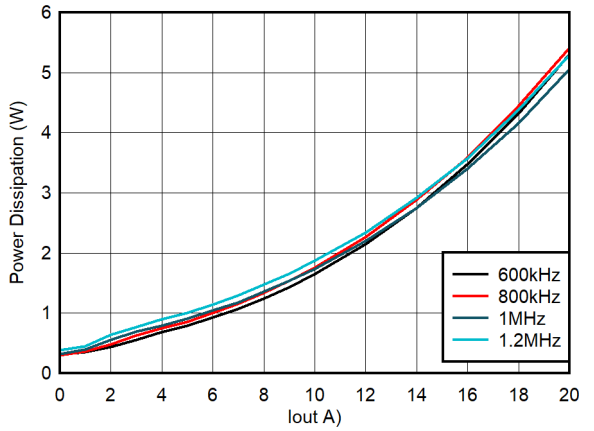


Figure 8-5. Power Dissipation, FCCM, External 5V Bias

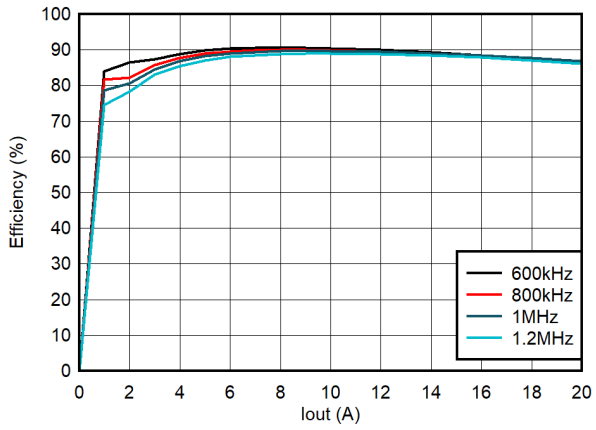


Figure 8-6. Efficiency, DCM, Internal LDO

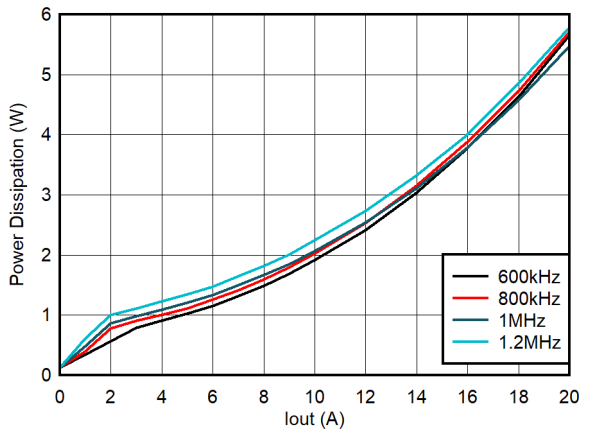


Figure 8-7. Power Dissipation, DCM, Internal LDO

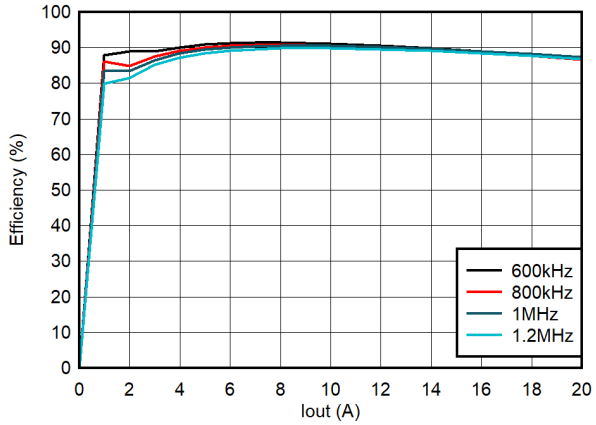


Figure 8-8. Efficiency, DCM, External 5V Bias

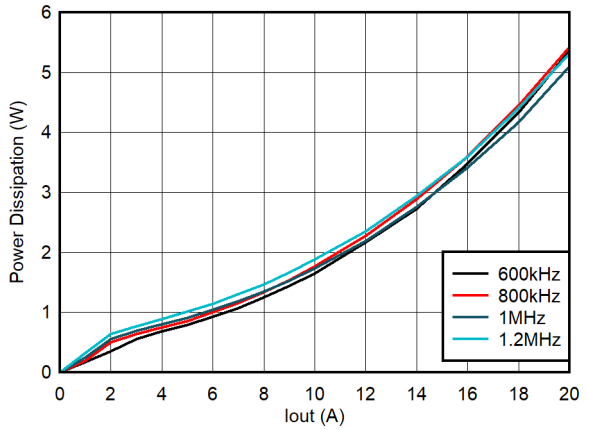


Figure 8-9. Power Dissipation, DCM, External 5V Bias

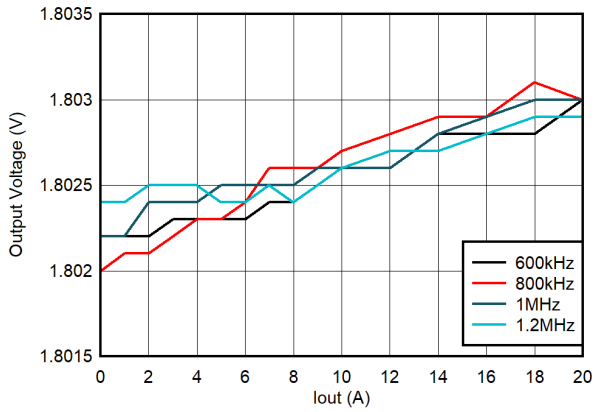


Figure 8-10. Load Regulation, FCCM, Internal LDO

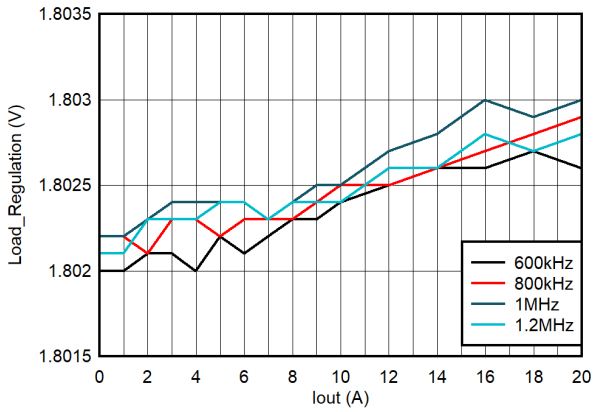


Figure 8-11. Load Regulation, FCCM, External 5V Bias

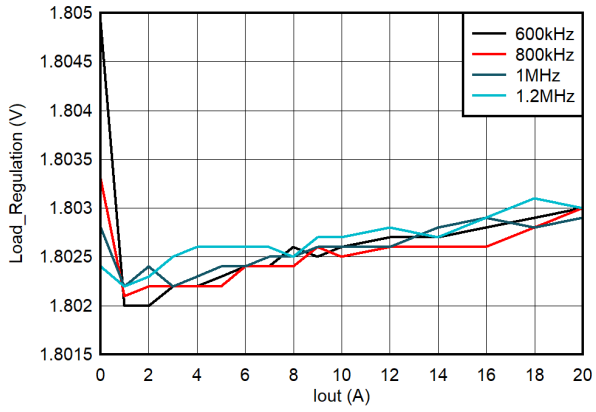


Figure 8-12. Load Regulation, DCM, Internal LDO

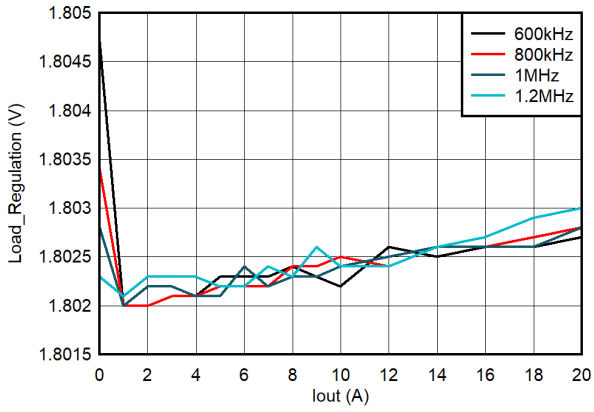


Figure 8-13. Load Regulation, DCM, External 5V Bias

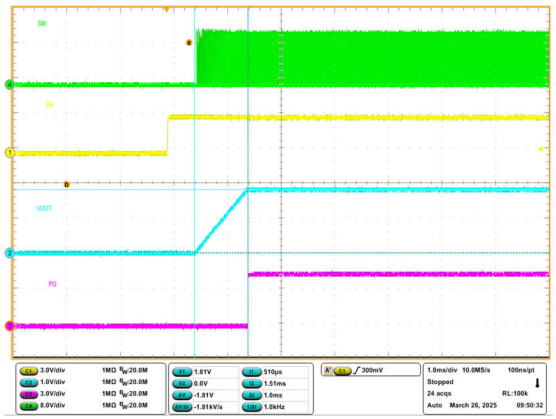


Figure 8-14. ENABLE Start-Up, 800kHz, FCCM, 20A Load

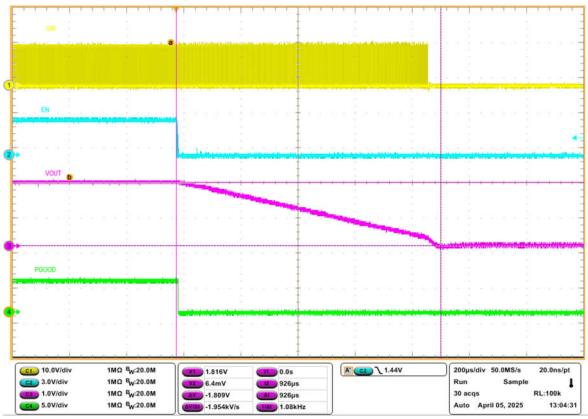


Figure 8-15. ENABLE Shutdown, 800kHz, FCCM, 15A Load, Soft-Off

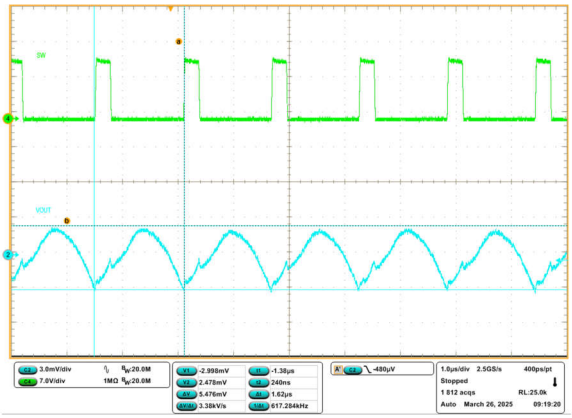


Figure 8-16. Output Voltage Ripple, 600kHz, FCCM, 20A Load

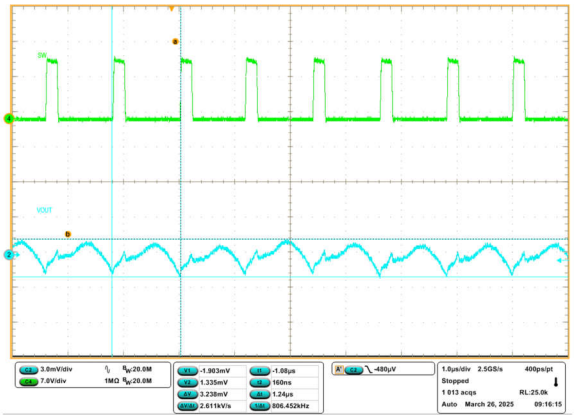


Figure 8-17. Output Voltage Ripple, 800kHz, FCCM, 20A Load

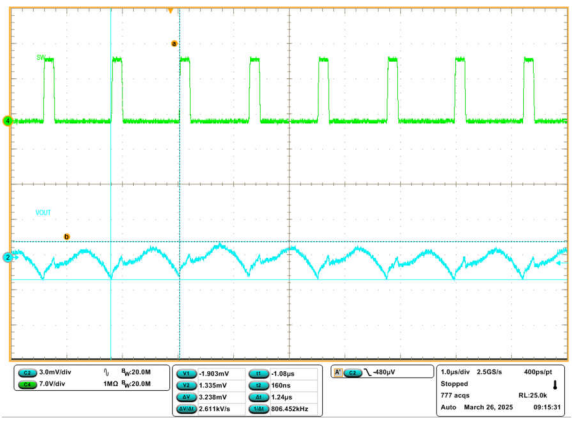


Figure 8-18. Output Voltage Ripple, 800kHz, FCCM, 1A Load

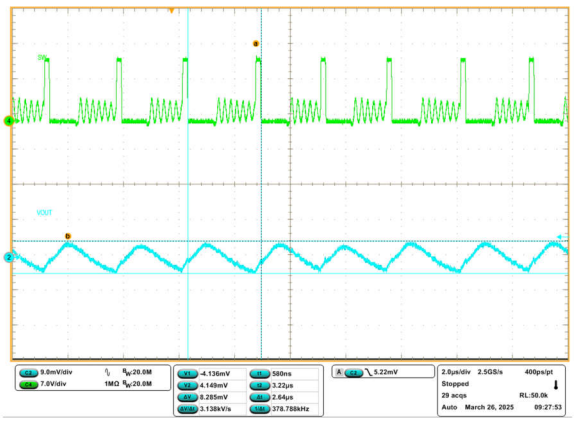


Figure 8-19. Output Voltage Ripple, 800kHz, DCM, 1A Load

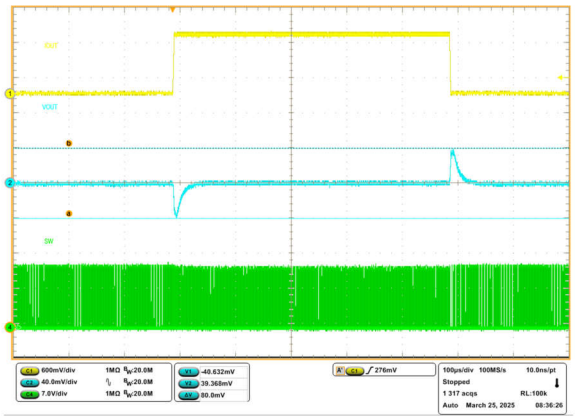


Figure 8-20. Load Transient, FCCM, 0A to 10A, 5A/us Slew Rate

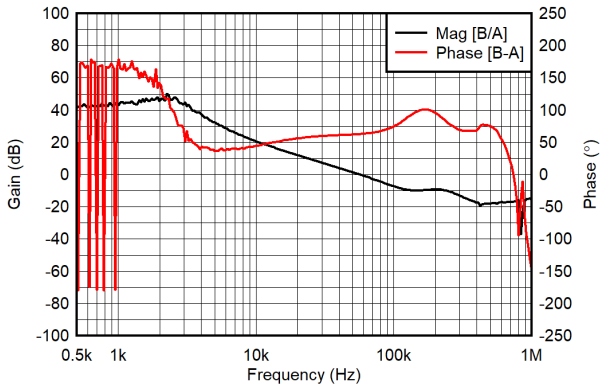


Figure 8-21. Bodeplot, 800kHz, FCCM, 20A Load

8.2.4.1 Thermal Performance

The following are thermal results captured on TPS544B27EVM with PVIN = 12V, VOUT = 1.8V, 20A Load, No airflow, soak 10 minutes.

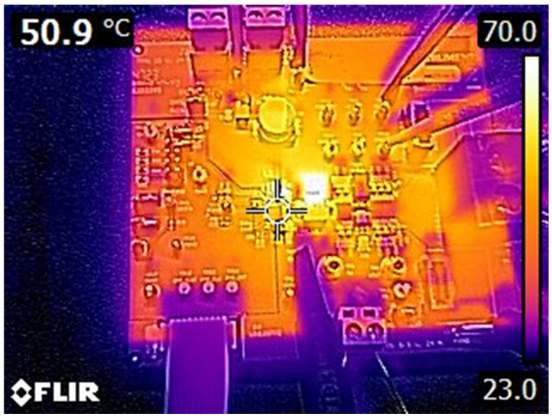


Figure 8-22. Thermal Characteristics, 600kHz, FCCM, Internal LDO

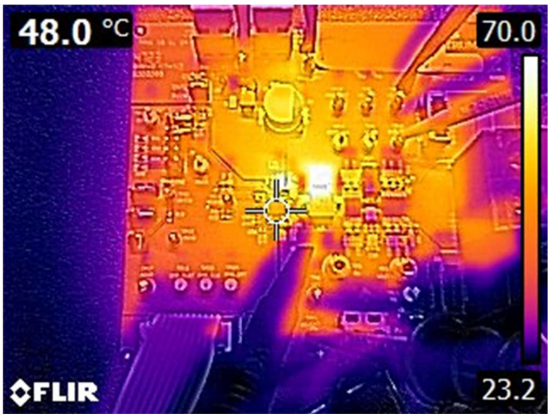


Figure 8-23. Thermal Characteristics, 600kHz, FCCM, External 5V Bias

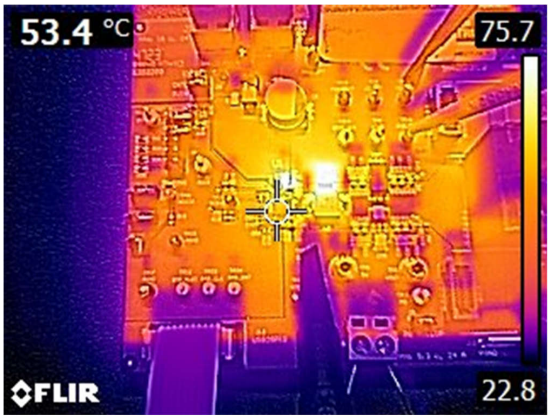


Figure 8-24. Thermal Characteristics, 800kHz, FCCM, Internal LDO

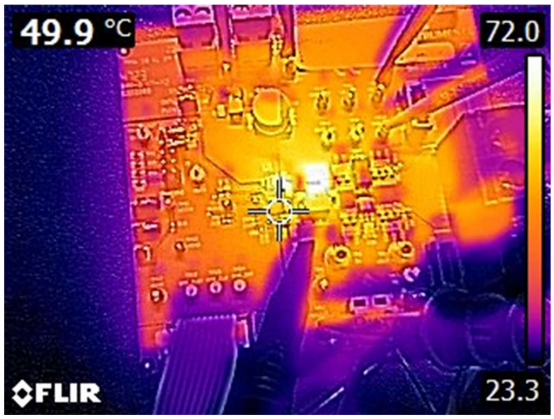


Figure 8-25. Thermal Characteristics, 800kHz, FCCM, External 5V Bias

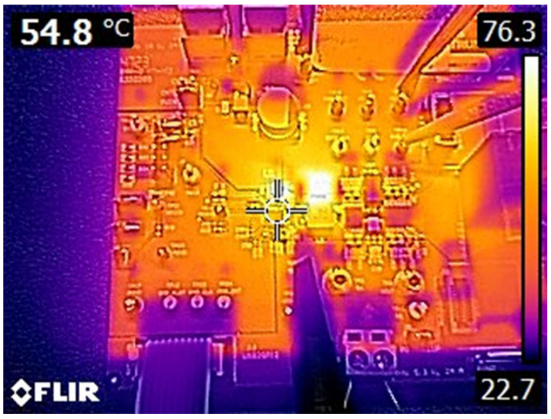


Figure 8-26. Thermal Characteristics, 1MHz, FCCM, Internal LDO

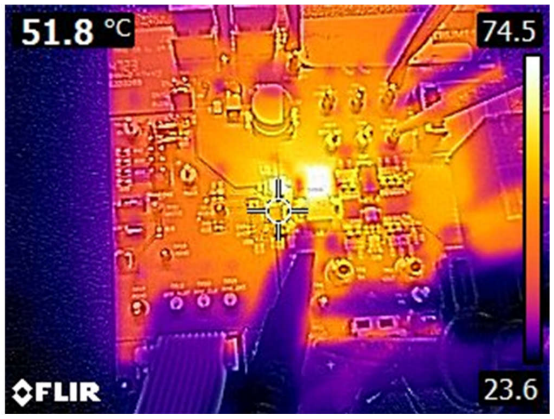


Figure 8-27. Thermal Characteristics, 1MHz, FCCM, External 5V Bias

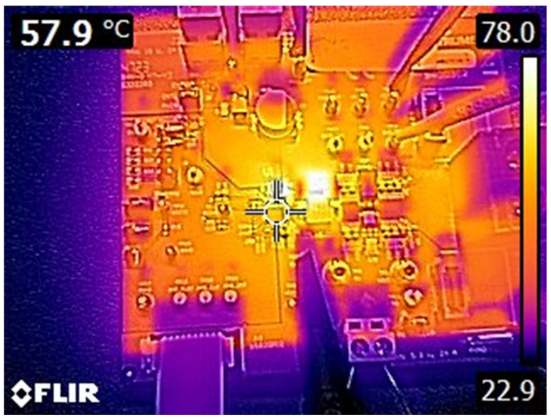


Figure 8-28. Thermal Characteristics, 1.2MHz, FCCM, Internal LDO

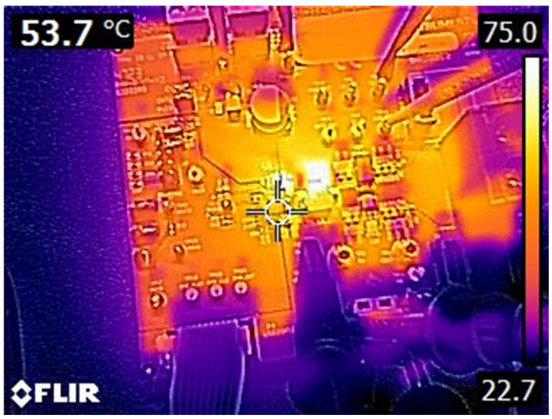


Figure 8-29. Thermal Characteristics, 1.2MHz, FCCM, External 5V Bias

8.3 Power Supply Recommendations

The device is designed to operate from a wide input voltage supply range between 4V to 18V when the VCC/VDRV pins are powered by an external bias ranging from 4.75V to 5.3V. Both PVIN and VCC/VDRV bias must be well regulated. Proper bypassing of input supplies (PVIN and VCC/VDRV) is also critical for noise performance, as are PCB layout and grounding scheme. See the recommendation in Section 8.4.1.

8.4 Layout

8.4.1 Layout Guidelines

Layout is critical for good power-supply design. Following these guidelines helps make sure of optimal performance, thermal management, and noise immunity. Figure 8-30 shows the recommended PCB layout configuration.

- **Power Component Placement and Routing:**
  - Place all power components (input and output capacitors, inductor, and the IC) on the top side of the PCB. To shield and isolate sensitive small signal traces from noisy power lines, insert at least one solid ground inner plane on layer 2.
  - Make the switch node as short and wide as possible. The PCB trace connecting the SW pin and high-voltage side of the inductor is defined as the switch node.
- **Decoupling Capacitors:**
  - PVIN to PGND decoupling capacitors are critical for MOSFET robustness and minimizing switching noise. Place two 0.1µF/25V/X7R/0402 (or similar) ceramic capacitors as close as possible to PVIN pins 7 and 8, connecting each capacitor to the adjacent PGND pin on the top layer. These capacitors bypass high frequency current in the PVIN and PGND loop. While TI recommends a 25V rating, this can be reduced to 16V for applications with a tightly regulated 12V input bus.
  - Place a 1µF 0402 ceramic capacitor (10V, X7S) from VDRV (pin 6) to PGND to bypass the gate drive and another from VCC (pin 5) to AGND to bypass the control loop. While the VCC capacitor can connect to PGND instead, an AGND connection is preferred. Use a voltage rating between 6.3V and 10V for these bypass capacitors to minimize ESR and ESL. Keep decoupling loops small and use wide routing traces (TI recommends 12 mil minimum) to reduce impedance.
  - Place the BOOT capacitor as close as possible to the BOOT and PHASE pins, using traces with a width of 12mil or wider.
- **Via Placement:**
  - For PVIN to PGND decoupling capacitors placed on the opposite side of the board, use at least two vias per pad for both PVIN and PGND connections to make sure of low impedance.
  - Place at least 4 PGND vias near both PGND pins 8-9 and pins 16-17 (8 vias total). These are in addition to the vias recommended beneath PGND pad pin 33. This arrangement minimizes ground bounce and improves thermal dissipation.
  - In addition to the 3 vias beneath the PVIN pad (pin 32), place vias near all PVIN pins to create low-impedance connections to input voltage planes on internal layers.
  - The AGND pin 26 to the PGND plane using two vias placed close to the pin. On the bottom layer, connect the AGND trace to the PGND thermal pad (underneath IC) using either a net-tie or a 0Ω resistor.
  - Connect the AGND pad, pin 31 to internal PGND ground planes through multiple vias to minimize thermal resistance and improve thermal performance.
- **Output Voltage Sensing:**
  - **Remote sensing:** Route VOSNS/GOSNS connections as a differential pair to the remote location. Implement Kelvin sensing across a high-frequency bypass capacitor (0.1µF or higher). Connect the ground side to GOSNS and the VOUT side to VOSNS. Keep these traces away from noise sources (inductor, SW node, clock lines) and shield them with PGND planes above and below.
  - **Single-ended sensing:** Connect the VOSNS pin to a high frequency local bypass capacitor of 0.1µF or higher, and short GOSNS to AGND using the shortest possible trace.
- **Input Current and Power Monitoring:**
  - When using input monitoring to achieve high accuracy and minimize switching noise interference, place 100pF/25V/0402 bypass capacitors from each of I_IN_P and I_IN_M pins to PGND. Add another 100pF/25V/0402 bypass capacitor between I_IN_P and I_IN_M. Position these capacitors as close as possible to the respective pins.
  - When not using input monitoring to enable the device to report PVIN voltage:
    1. Connect I_IN_P (Pin 3) directly to I_IN_M (Pin 4)
    2. Place a 0.1µF ceramic bypass capacitor between I_IN_M (Pin 4) and PGND

3. Connect I_IN_M (Pin 4) to the PVIN node of the TPS544B27W.

- Place the PMB_ADDR (pin 23) to AGND resistor close to the pin to minimize noise coupling. Minimize the trace length from the resistor to the device pins so that trace capacitance is minimized. Excess capacitance can lead to an incorrect detection of the resistor.

8.4.2 Layout Example

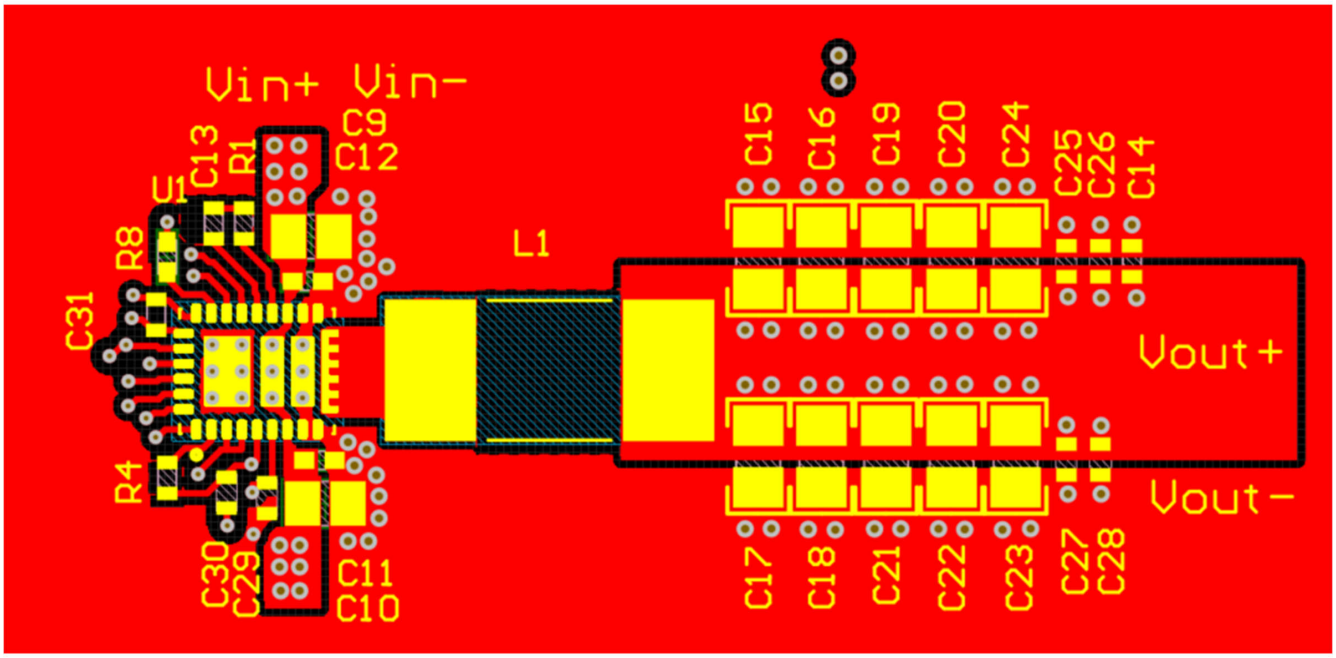


Figure 8-30. Layout Example

9 Device and Documentation Support

9.1 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

9.2 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

9.3 Trademarks

D-CAP+™ and TI E2E™ are trademarks of Texas Instruments.
PMBus® is a registered trademark of System Management Interface Forum, Inc..
All trademarks are the property of their respective owners.

9.4 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

9.5 Glossary

TI Glossary — This glossary lists and explains terms, acronyms, and definitions.

10 Revision History

DATE	REVISION	NOTES
December 2025	*	Initial Release

11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TPS544B27WVBDR	Active	Production	WQFN-FCRLF (VBD) | 33	3000 | LARGE T&R	-	SNAGCU	Level-2-260C-1 YEAR	-	T544B27W

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

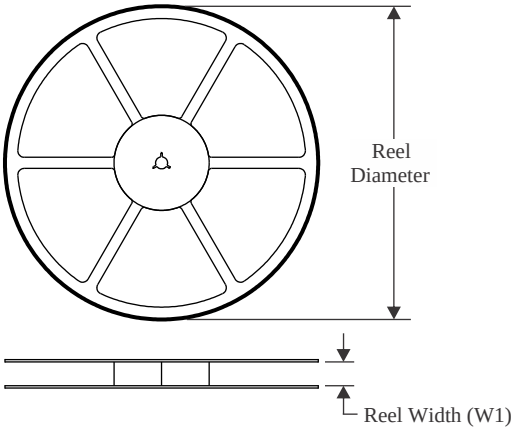
(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

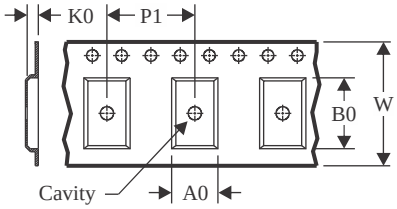
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

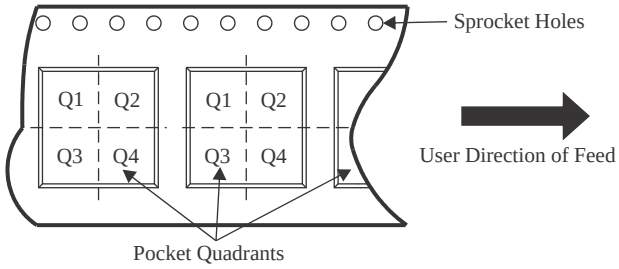


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

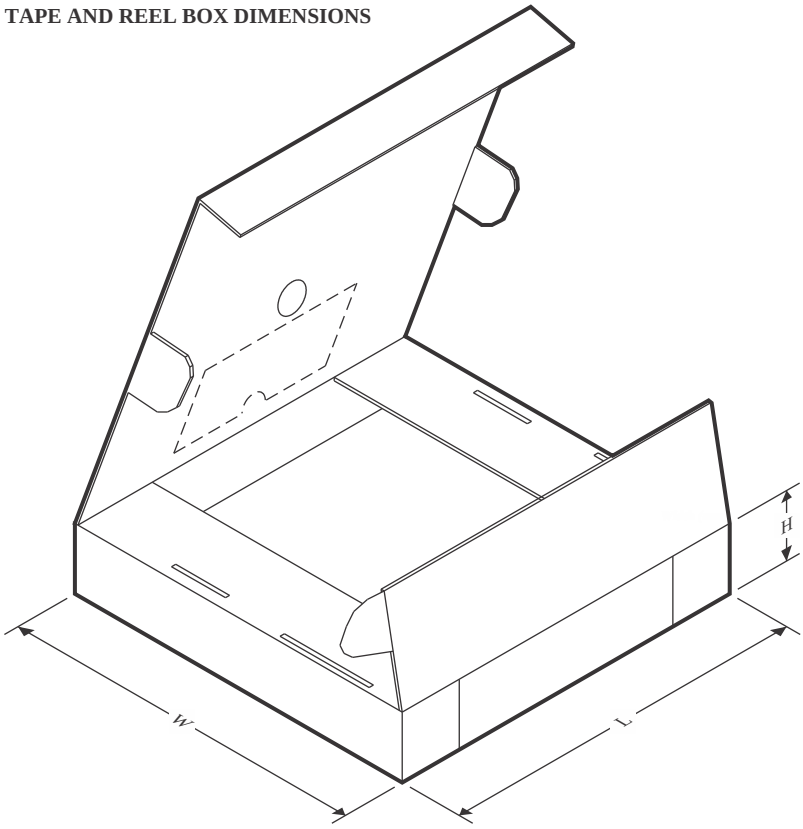
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS544B27WVBDR	WQFN-FCRLF	VBD	33	3000	330.0	12.4	4.3	5.3	1.3	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

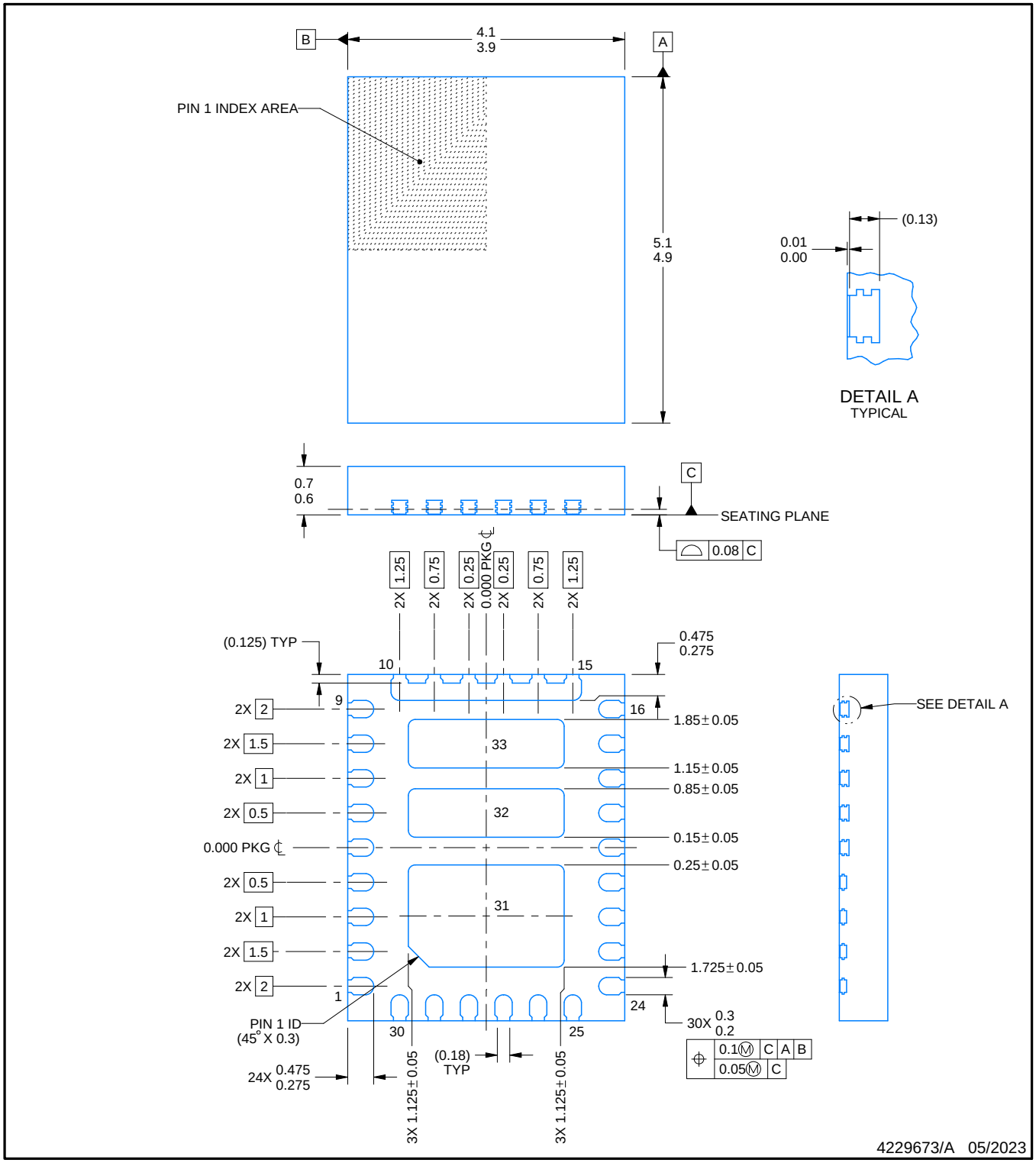
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS544B27WVBDR	WQFN-FCRLF	VBD	33	3000	367.0	367.0	35.0

PACKAGE OUTLINE

VBD0033A

WQFN-FCRLF - 0.7 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



NOTES:

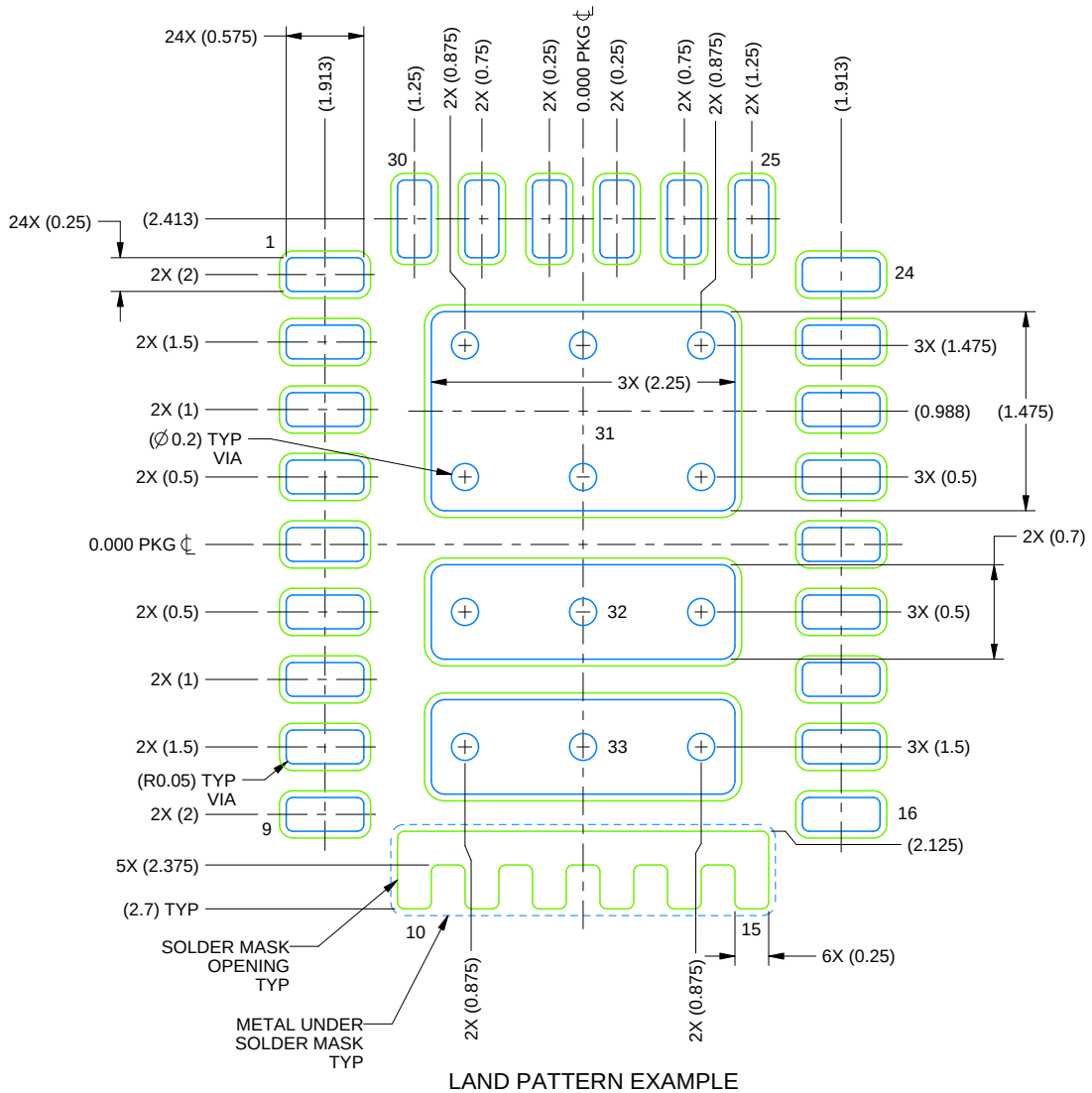
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pads must be soldered to the printed circuit board for optimal thermal and mechanical performance.

EXAMPLE BOARD LAYOUT

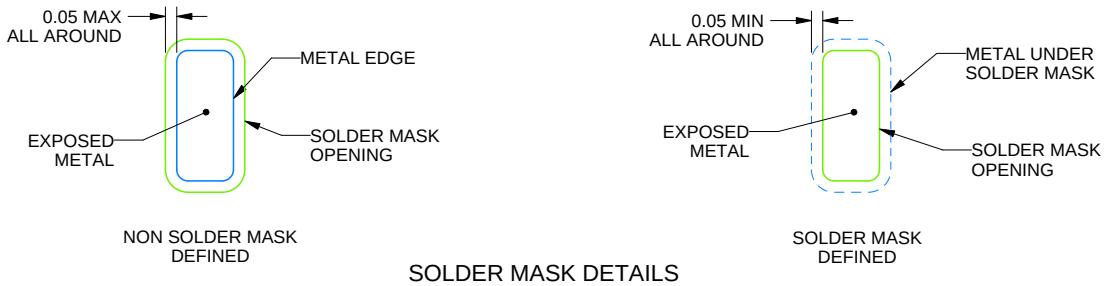
VBD0033A

WQFN-FCRLF - 0.7 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



LAND PATTERN EXAMPLE
SCALE: 18X



SOLDER MASK DETAILS

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NOTES: (continued)

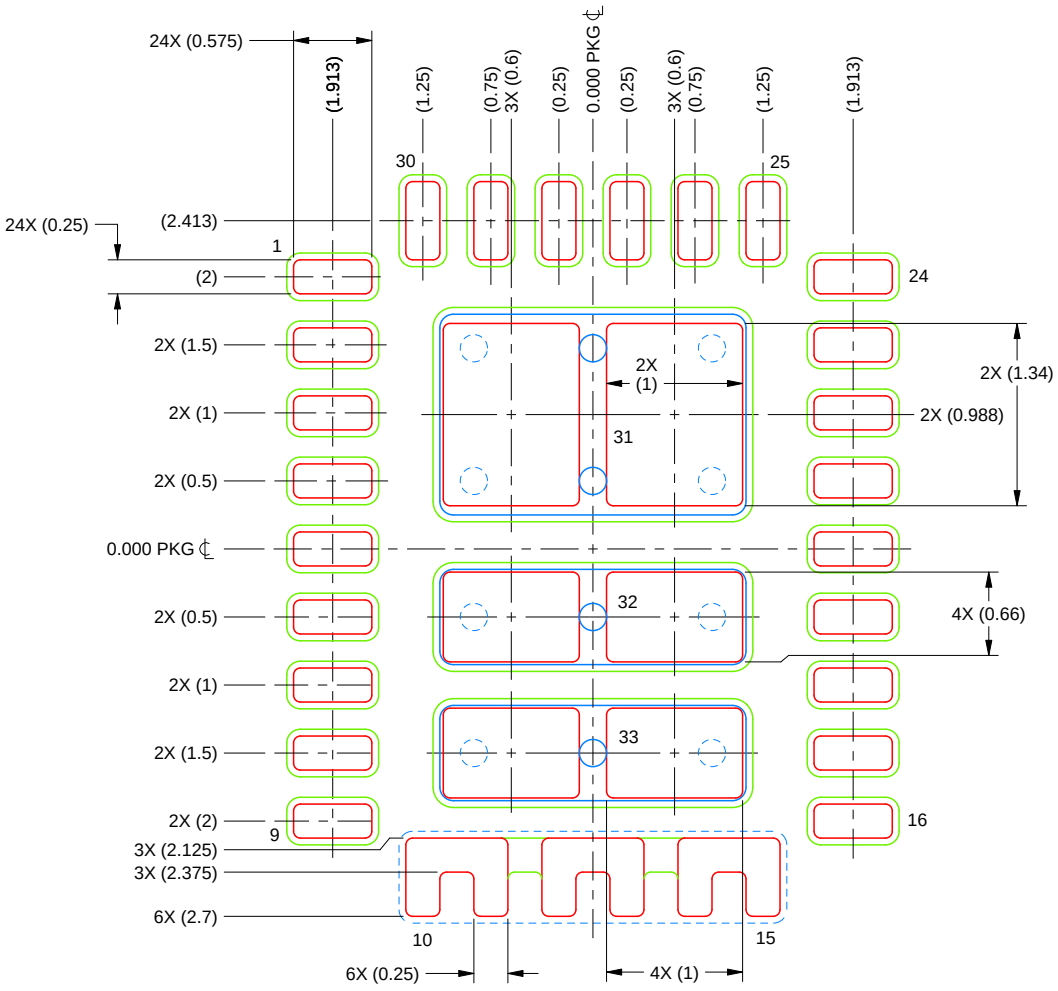
4. This package is designed to be soldered to thermal pads on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).

EXAMPLE STENCIL DESIGN

VBD0033A

WQFN-FCRLF - 0.7 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 18X

PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
PAD NUMBERED 10-15: 89%
PAD 31: 81%
PADS 32 & 33: 84%

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NOTES: (continued)

5. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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