

## TPS546D24 2.95-V to 16-V, 40-A, up to 4x Stackable, PMBus® Buck Converter

## 1 Features

- Split Rail Support: 2.95-V to 16-V PVIN; 2.95-V to 18-V AVIN (4-V<sub>IN</sub> VDD5 for Switching)
- Integrated 4.5-mΩ/0.9-mΩ MOSFETs
- Average Current Mode Control With Selectable Internal Compensation
- 2x, 3x, 4x Stackable With Current Sharing up to 160 A, Supporting a Single Address per Output
- Selectable 0.6-V to 5.5-V Output via Pin Strap or 0.25-V to 5.5-V via PMBus VOUT\_COMMAND
- Extensive PMBus Command Set With Telemetry for V<sub>OUT</sub>, I<sub>OUT</sub> and Internal Die Temperature
- Differential Remote Sensing With Internal FB Divider for < 1% V<sub>OUT</sub> Error –40°C to +150°C T<sub>J</sub>
- AVS and Margining Capabilities Through PMBus
- MSEL Pins Pin Programming PMBus Defaults
- 12 Selectable Switching Frequencies from 225 kHz to 1.5 MHz (8 Pin-Strap Options)
- Frequency Sync In/Sync Out
- Supports Prebiased Output
- Supports Strongly Coupled Inductor
- 7 mm × 5 mm × 1.5 mm, 40-pin QFN, Pitch = 0.5 mm
- Create a Custom Design Using the TPS546D24 With [WEBENCH® Power Designer](#)

## 2 Applications

- Data Center Switches, Rack Servers
- Active Antenna System, Remote Radio and Baseband Unit
- Automated Test Equipment, CT, PET, and MRI
- ASIC, SoC, FPGA, DSP Core, and I/O Voltage

### 3 Description

The TPS546D24 is a highly integrated, non-isolated DC/DC converter capable of high frequency operation and 40-A current output from a 7-mm x 5-mm package. Two, three, and four TPS546D24 devices can be interconnected to provide up to 160 A on a single output. The device has an option to overdrive the internal 5-V LDO with an external 5-V supply via the VDD5 pin to improve efficiency and reduce power dissipation of the converter.

The TPS546D24 uses a proprietary fixed-frequency current-mode control with input feedforward and selectable internal compensation components for minimal size and stability over a wide range of output capacitances.

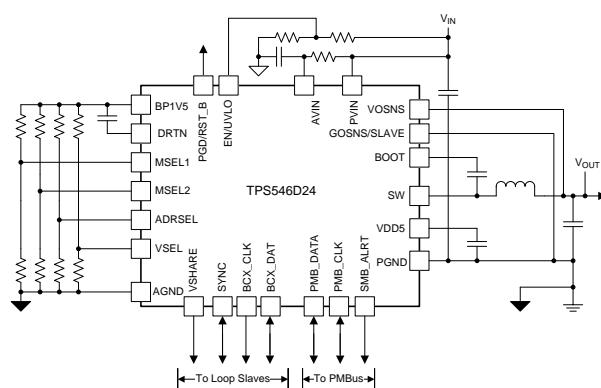
The PMBus interface with 1-MHz clock support gives a convenient, standardized digital interface for converter configuration as well as monitoring of key parameters including output voltage, output current, and internal die temperature. Response to fault conditions can be set to restart, latch off, or ignore, depending on system requirements. Back-channel communication between stacked devices enables all TPS546D24 converters powering a single output rail to share a single address to simplify system software/firmware design. Key parameters including output voltage, switching frequency, soft-start time, and overcurrent fault limits can also be configured through BOM selection without PMBus communication to support program free power-up.

## Device Information<sup>(1)</sup>

PART NUMBER	PACKAGE	BODY SIZE (NOM)
TPS546D24	LQFN-CLIP (40)	7.00 mm x 5.00 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

## Simplified Application



## Table of Contents

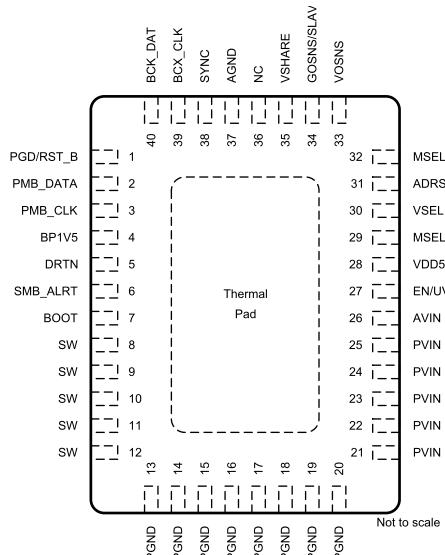
<b>1</b>	<b>Features</b> .....	<b>1</b>
<b>2</b>	<b>Applications</b> .....	<b>1</b>
<b>3</b>	<b>Description</b> .....	<b>1</b>
<b>4</b>	<b>Revision History</b> .....	<b>2</b>
<b>5</b>	<b>Pin Configuration and Functions</b> .....	<b>3</b>
<b>6</b>	<b>Device and Documentation Support</b> .....	<b>5</b>
6.1	Device Support.....	5
<b>7</b>	<b>Mechanical, Packaging, and Orderable Information</b> .....	<b>6</b>
6.2	Receiving Notification of Documentation Updates....	5
6.3	Community Resources.....	6
6.4	Trademarks .....	6
6.5	Electrostatic Discharge Caution .....	6
6.6	Glossary .....	6

## 4 Revision History

Changes from Original (November 2018) to Revision A	Page
• First release of production-data data sheet .....	1

## 5 Pin Configuration and Functions

**RVF Package**  
**40-Pin LQFN-CLIP With Exposed Thermal Pad**  
**Top View**



### Pin Functions

PIN		I/O	DESCRIPTION
NO.	NAME		
1	PGD/RST_B	I/O	Open-drain power good or reset#, As determined by user accessible bit (See in PMBUS Command detailed descriptions) . The default pin function is an open drain power-good indicator.
2	PMB_DATA	I/O	PMBus DATA pin. See PMBus specification.
3	PMB_CLK	I	PMBus CLK pin. See PMBus specification.
4	BP1V5	O	Output of the 1.5-V internal regulator. This regulator powers the digital circuitry and should be bypassed with a minimum of 1 $\mu$ F to DRTN. BP1V5 is not designed to power external circuit.
5	DRTN	—	Digital bypass return for bypass capacitor for BP1V5. Internally Connected to AGND. Do not Connect to PGND or AGND.
6	SMB_ALRT	O	SMBus alert pin. See SMBus specification.
7	BOOT	I	Bootstrap pin for the internal flying high side driver. Connect a typical 100 nF from this pin to SW. To reduce the voltage spike at SW, an optional BOOT resistor of up to 8 $\Omega$ may be placed in series with the BOOT capacitor to slow down turn-on of the high-side FET.
8	SW	I/O	Switched power output of the device. Connect the output averaging filter and bootstrap to this group of pins.
9			
10			
11			
12			
13	PGND	—	Power stage ground return. These pins are internally connected to the thermal pad.
14			
15			
16			
17			
18			
19			
20			

**Pin Functions (continued)**

PIN		I/O	DESCRIPTION
NO.	NAME		
21	PVIN	I	Input power to the power stage. Low-impedance bypassing of these pins to PGND is critical.
22			
23			
24			
25			
26	AVIN	I	Input power to the controller. Bypass with a minimum 1- $\mu$ F ceramic capacitor to PGND. If AVIN is connected to the same input as PVIN or VDD5, a minimum 10- $\mu$ s R-C filter is recommended to reduce switching noise on AVIN.
27	EN/UVLO	I	Enable switching as the PMBus CONTROL pin. EN/UVLO can also be connected to a resistor divider to program input voltage UVLO.
28	VDD5	O	Output of the 5-V internal regulator. This regulator powers the driver stage of the controller and should be bypassed with a minimum of 4.7 $\mu$ F to PGND at the thermal pad. Low impedance bypassing of this pin to PGND is critical.
29	MSEL2	I	Connect this pin to a resistor divider between BP1V5 and AGND for different options of soft-start time, overcurrent fault limit, and multi-phase information. See section
30	VSEL	I	Connect this pin to a resistor divider between BP1V5 and AGND for different options of internal voltage feedback divider and default output voltage. See section.
31	ADRSEL	I	Connect this pin to a resistor divider between BP1V5 and AGND for different options of PMBus addresses and frequency sync (including determination of SYNC pin as SYNC IN or SYNC OUT function). See section.
32	MSEL1	I	Connect this pin to a resistor divider between BP1V5 and AGND for different options of switching frequency and internal compensation parameters. See section.
33	VOSNS	I	The positive input of the remote sense amplifier. For a standalone device or the loop master device in a multi-phase configuration, connect VOSNS pin to the output voltage at the load. For the loop slave device in a multi-phase configuration, the remote sense amplifier is not required for output voltage sensing or regulation, this pin can be left floating.
34	GOSNS/SLAVE	I	The negative input of the remote sense amplifier for loop master device or should be pulled up high to indicate loop slave. For standalone device or the loop master device in a multi-phase configuration, connect GOSNS pin to the ground at the load. For the loop slave device in a multi-phase configuration, the GOSNS pin must be pulled up to BP1V5 to indicate the device a loop slave.
35	VSHARE	I/O	Voltage sharing signal for multi-phase operation. For stand-alone device, the VSHARE pin must be left floating.
36	NC	-	Not internally connected. Pin can be left floating or connected to PGND at the thermal pad.
37	AGND	-	Analog ground return for controller. Connect the AGND pin directly to the thermal pad on the PCB board.
38	SYNC	I/O	For frequency synchronization, can be programmed as SYNC IN or SYNC OUT pin by ADRSEL pin or the PMBus Command. The SYNC pin can be left floating when not used.
39	BCX_CLK	I/O	Clock for back-channel communications between stacked devices.
40	BCX_DAT	I/O	Data for back-channel communications between stacked devices.
—	Thermal pad	—	Package thermal pad, internally connected to PGND. The thermal pad must have adequate solder coverage for proper operation.

## 6 Device and Documentation Support

### 6.1 Device Support

#### 6.1.1 Third-Party Products Disclaimer

TI'S PUBLICATION OF INFORMATION REGARDING THIRD-PARTY PRODUCTS OR SERVICES DOES NOT CONSTITUTE AN ENDORSEMENT REGARDING THE SUITABILITY OF SUCH PRODUCTS OR SERVICES OR A WARRANTY, REPRESENTATION OR ENDORSEMENT OF SUCH PRODUCTS OR SERVICES, EITHER ALONE OR IN COMBINATION WITH ANY TI PRODUCT OR SERVICE.

#### 6.1.2 Development Support

##### 6.1.2.1 *Custom Design With WEBENCH® Tools*

[Click here](#) to create a custom design using the TPS546D24 device with the WEBENCH® Power Designer.

1. Start by entering the input voltage ( $V_{IN}$ ), output voltage ( $V_{OUT}$ ), and output current ( $I_{OUT}$ ) requirements.
2. Optimize the design for key parameters such as efficiency, footprint, and cost using the optimizer dial.
3. Compare the generated design with other possible solutions from Texas Instruments.

The WEBENCH Power Designer provides a customized schematic along with a list of materials with real-time pricing and component availability.

In most cases, these actions are available:

- Run electrical simulations to see important waveforms and circuit performance
- Run thermal simulations to understand board thermal performance
- Export customized schematic and layout into popular CAD formats
- Print PDF reports for the design, and share the design with colleagues

Get more information about WEBENCH tools at [www.ti.com/WEBENCH](http://www.ti.com/WEBENCH).

##### 6.1.2.2 *Texas Instruments Fusion Digital Power Designer*

The TPS546D24 devices are supported by Texas Instruments Digital Power Designer. Fusion Digital Power Designer is a graphical user interface (GUI) which can be used to configure and monitor the devices via PMBus using a Texas Instruments USB-to-GPIO adapter.

Click this link to download the Texas Instruments [Fusion Digital Power Designer](#) software package.

### 6.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on [ti.com](http://ti.com). In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

## 6.3 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's [Terms of Use](#).

**TI E2E™ Online Community** *TI's Engineer-to-Engineer (E2E) Community.* Created to foster collaboration among engineers. At [e2e.ti.com](http://e2e.ti.com), you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

**Design Support** *TI's Design Support* Quickly find helpful E2E forums along with design support tools and contact information for technical support.

## 6.4 Trademarks

E2E is a trademark of Texas Instruments.

WEBENCH is a registered trademark of Texas Instruments.

PMBus is a registered trademark of System Management Interface Forum, Inc..

All other trademarks are the property of their respective owners.

## 6.5 Electrostatic Discharge Caution



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

## 6.6 Glossary

[SLYZ022](#) — *TI Glossary.*

This glossary lists and explains terms, acronyms, and definitions.

## 7 Mechanical, Packaging, and Orderable Information

The following pages include mechanical packaging and orderable information. This information is the most current data available for the designated devices. These data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

**PACKAGING INFORMATION**

Orderable part number	Status (1)	Material type (2)	Package   Pins	Package qty   Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TPS546D24RVFR	Active	Production	LQFN-CLIP (RVF)   40	2500   LARGE T&R	ROHS Exempt	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	TPS546D24
TPS546D24RVFR.A	Active	Production	LQFN-CLIP (RVF)   40	2500   LARGE T&R	ROHS Exempt	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	TPS546D24
TPS546D24RVFT	Active	Production	LQFN-CLIP (RVF)   40	250   SMALL T&R	ROHS Exempt	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	TPS546D24
TPS546D24RVFT.A	Active	Production	LQFN-CLIP (RVF)   40	250   SMALL T&R	ROHS Exempt	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	TPS546D24

<sup>(1)</sup> **Status:** For more details on status, see our [product life cycle](#).

<sup>(2)</sup> **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

<sup>(3)</sup> **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

<sup>(4)</sup> **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

<sup>(5)</sup> **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

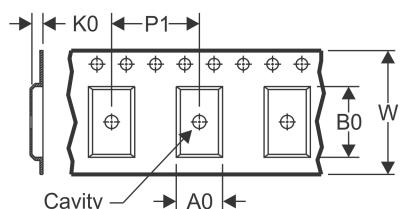
<sup>(6)</sup> **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

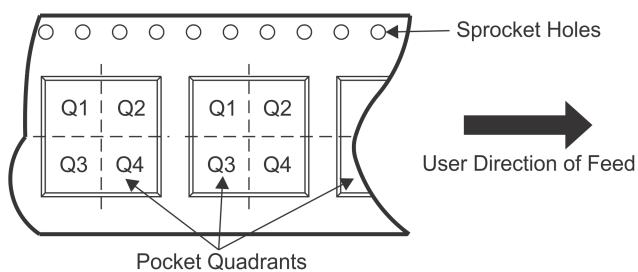
**Important Information and Disclaimer:** The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

**TAPE AND REEL INFORMATION**
**REEL DIMENSIONS**

**TAPE DIMENSIONS**


A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS546D24RVFR	LQFN-CLIP	RVF	40	2500	330.0	16.4	5.35	7.35	1.7	8.0	16.0	Q1
TPS546D24RVFT	LQFN-CLIP	RVF	40	250	180.0	16.4	5.35	7.35	1.7	8.0	16.0	Q1

**TAPE AND REEL BOX DIMENSIONS**


\*All dimensions are nominal

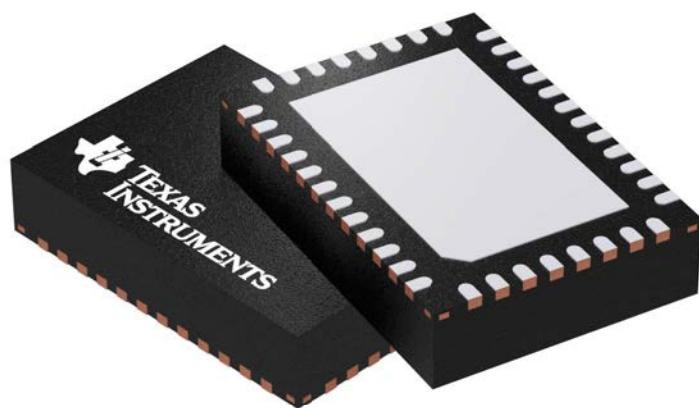
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS546D24RVFR	LQFN-CLIP	RVF	40	2500	367.0	367.0	38.0
TPS546D24RVFT	LQFN-CLIP	RVF	40	250	210.0	185.0	35.0

## GENERIC PACKAGE VIEW

**RVF 40**

**LQFN-CLIP - 1.52 mm max height**

PLASTIC QUAD FLATPACK - NO LEAD



Images above are just a representation of the package family, actual package may vary.  
Refer to the product data sheet for package details.

4211383/D

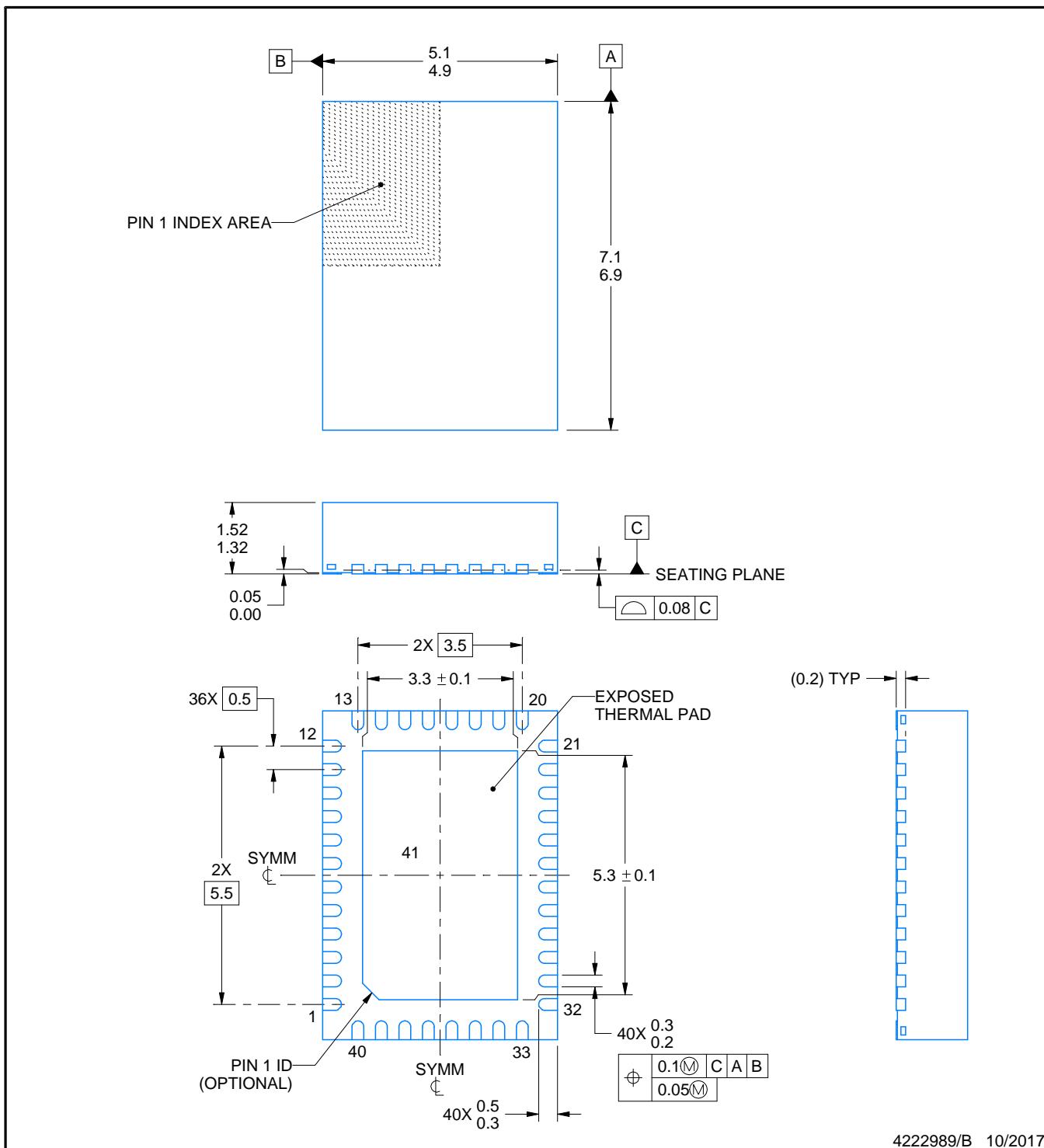


# PACKAGE OUTLINE

**RVF0040A**

**LQFN-CLIP - 1.52 mm max height**

PLASTIC QUAD FLATPACK - NO LEAD



4222989/B 10/2017

**NOTES:**

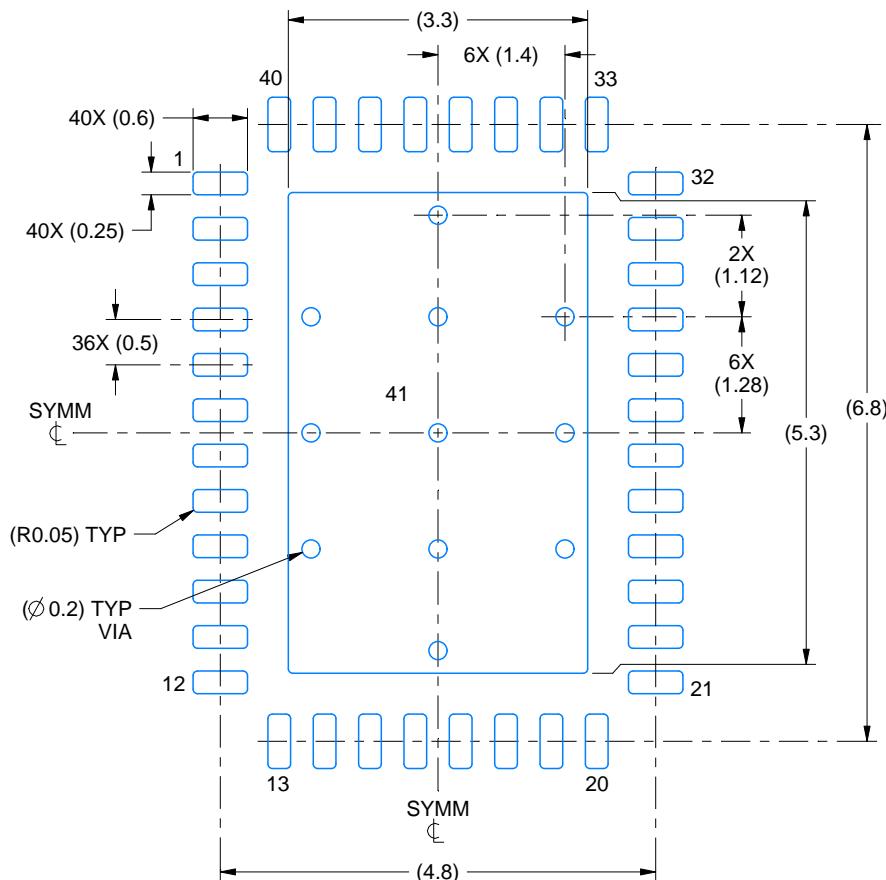
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.
4. Reference JEDEC registration MO-220.

## EXAMPLE BOARD LAYOUT

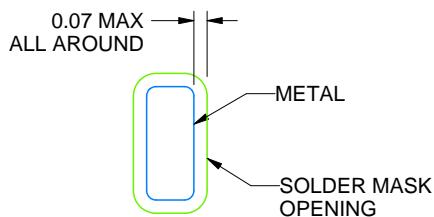
**RVF0040A**

## LQFN-CLIP - 1.52 mm max height

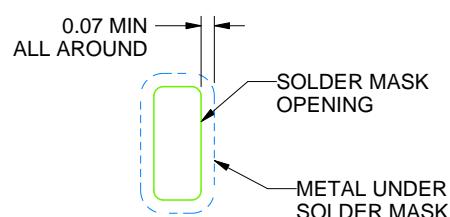
#### PLASTIC QUAD FLATPACK - NO LEAD



## LAND PATTERN EXAMPLE



NON SOLDER MASK  
DEFINED  
(PREFERRED)



## SOLDER MASK DEFINED

## SOLDER MASK DETAILS

4222989/B 10/2017

#### NOTES: (continued)

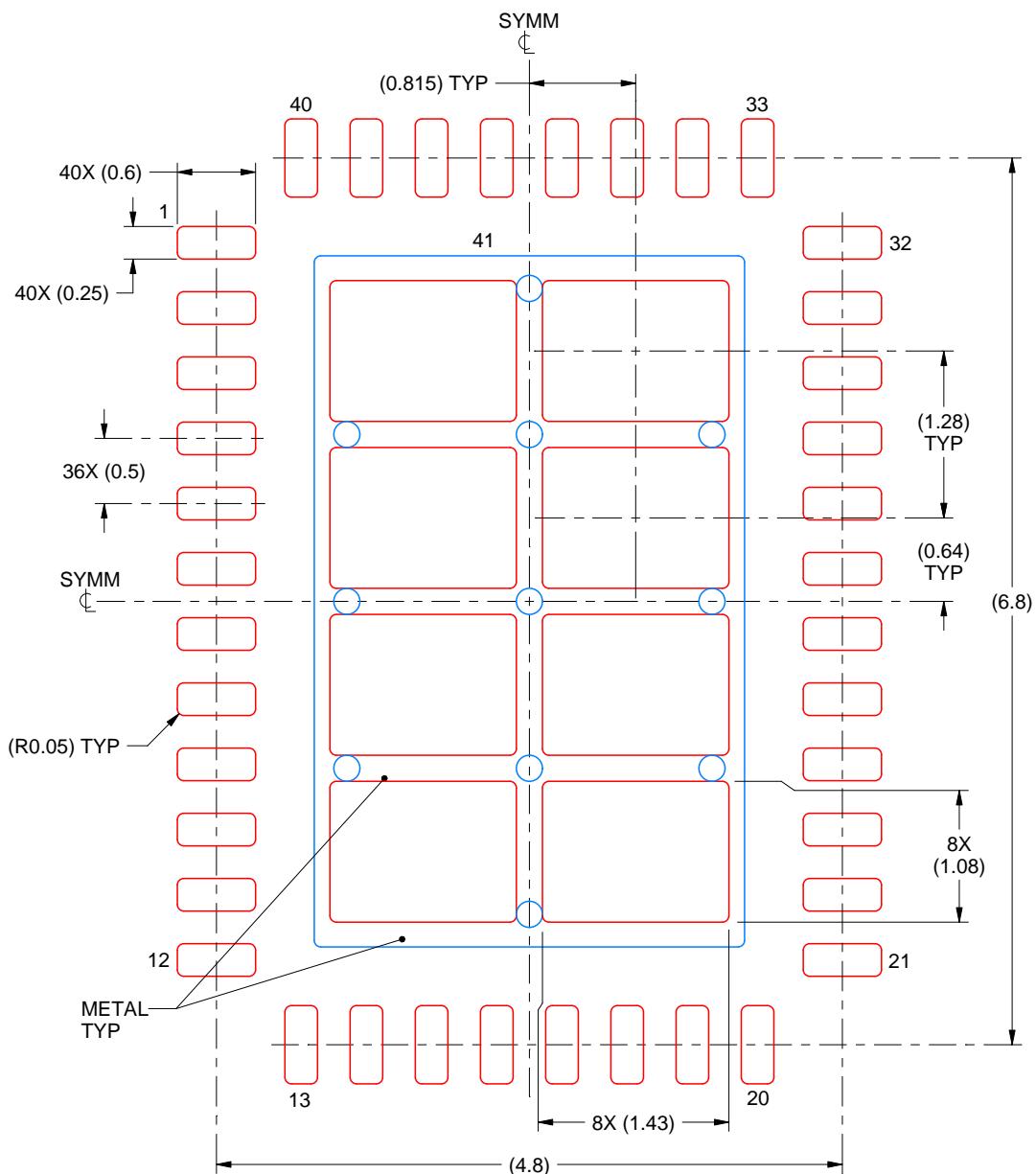
5. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 ([www.ti.com/lit/slua271](http://www.ti.com/lit/slua271)).

## EXAMPLE STENCIL DESIGN

**RVF0040A**

## LQFN-CLIP - 1.52 mm max height

## PLASTIC QUAD FLATPACK - NO LEAD



## SOLDER PASTE EXAMPLE BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD  
71% PRINTED SOLDER COVERAGE BY AREA  
SCALE:18X

4222989/B 10/2017

#### NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

## IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATASHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES "AS IS" AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, regulatory or other requirements.

These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you fully indemnify TI and its representatives against any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI's products are provided subject to [TI's Terms of Sale](#), [TI's General Quality Guidelines](#), or other applicable terms available either on [ti.com](#) or provided in conjunction with such TI products. TI's provision of these resources does not expand or otherwise alter TI's applicable warranties or warranty disclaimers for TI products. Unless TI explicitly designates a product as custom or customer-specified, TI products are standard, catalog, general purpose devices.

TI objects to and rejects any additional or different terms you may propose.

Copyright © 2026, Texas Instruments Incorporated

Last updated 10/2025