

TPS560200-Q1 4.5V to 17V Input, 500mA, Automotive, Synchronous Step-Down Converter With Advanced Eco-mode

1 Features

- AEC-Q100 qualified for automotive applications
 - Temperature range: grade 1 -40°C to 125°C
 - HBM ESD Classification: H2
 - CDM ESD Classification: C4B
- Integrated monolithic 0.95Ω high-side and 0.33Ω low-side MOSFETs
- 500mA continuous output current
- Output voltage range: 0.8V to 6.5V
- 0.8V voltage reference with $\pm 1.3\%$ accuracy over temperature
- Auto-skip advanced Eco-mode for high efficiency at light loads
- D-CAP2™ control scheme enables fast transient responses
- No external compensation needed
- 600kHz switching frequency
- 2ms internal soft start
- Safe start-up into prebiased VOUT
- Thermal shutdown
- -40°C to 125°C operating junction temperature range
- Available in 8-pin MSOP package

2 Applications

- Electric vehicle (EV) charging station
- Infotainment system

3 Description

The TPS560200-Q1 is an 17V, 500mA, low-I_q, adaptive on-time D-CAP2 control scheme mode synchronous monolithic buck converter with integrated MOSFETs in easy-to-use 8-pin MSOP package.

The TPS560200-Q1 lets system designers complete the suite of various end-equipment power bus regulators with a cost-effective, low component count and low standby current design. The main control loop for the device uses the D-CAP2 control scheme that provides a fast transient response with no external compensation components. The adaptive on-time control supports seamless transition between PWM mode at higher load conditions and advanced Eco-mode operation at light loads.

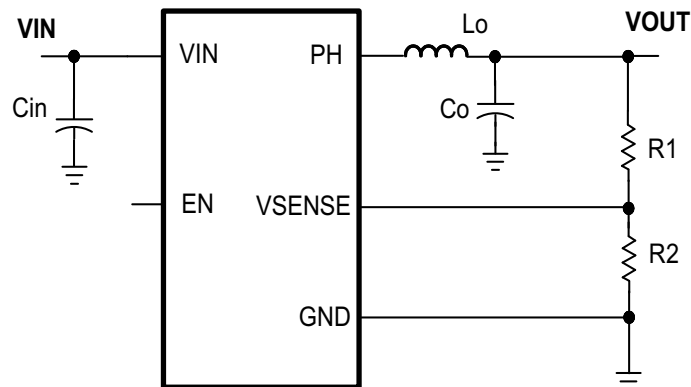
The TPS560200-Q1 also has a proprietary circuit that enables the device to adapt to both low equivalent series resistance (ESR) output capacitors, such as POSCAP or SP-CAP, and ultra-low ESR ceramic capacitors. The device operates from 4.5V to 17V VIN input. The output voltage can be programmed between 0.8V and 6.5V. The device also features a fixed 2ms soft-start time. The device is available in the 8-pin MSOP package.

Package Information

PART NUMBER	PACKAGE ⁽¹⁾	PACKAGE SIZE ⁽²⁾
TPS560200-Q1	DGK (VSSOP, 8)	3mm × 4.9mm

(1) For more information, see [Section 10](#).

(2) The package size (length × width) is a nominal value and includes pins, where applicable.



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Simplified Schematic



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4 Pin Configuration and Functions

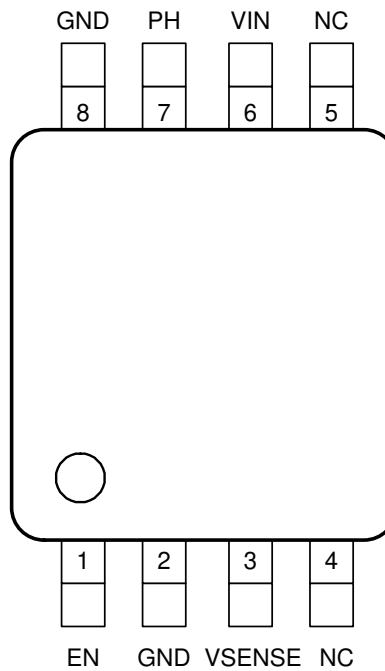


Figure 4-1. DGK Package 8-Pin VSSOP (Top View)

Table 4-1. Pin Functions

PIN		TYPE ⁽¹⁾	DESCRIPTION
NAME	NO.		
EN	1	I	Enable pin. Float to enable
GND	2, 8	—	Return for control circuitry and low-side power MOSFET
VSENSE	3	I	Converter feedback input. Connect to output voltage with feedback resistor divider
NC	4, 5	—	No connection inside, can be connected to any node or can be floating
VIN	6	I	Supplies the control circuitry of the power converter
PH	7	O	The switch node

(1) I = input, O = output

5 Specifications

5.1 Absolute Maximum Ratings

See (1)

		MIN	MAX	UNIT
Input voltage	VIN	-0.3	19	V
	EN	-0.3	7	V
	VSENSE	-0.3	3	V
Output voltage	PH	-0.6	19	V
	PH 10ns transient	-2	21	V
Source current	EN		±100	µA
	PH		Current limit	A
Sink current	PH		Current limit	A
Operating junction temperature		-40	150	°C
Storage temperature, T _{stg}		-65	150	

- (1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

5.2 ESD Ratings

		VALUE	UNIT
V _(ESD) Electrostatic discharge	Human-body model (HBM), per AEC Q100-002, all -2000, 2000 pins ⁽¹⁾	±2000	V
	Charged-device model (CDM), per AEC Q100-011, all pins	±500	

- (1) AEC Q100-002 indicates that HBM stressing must be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

5.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
V _I	Input voltage range	4.5	17	V
T _J	Operating junction temperature	-40	125	°C

5.4 Thermal Information

THERMAL METRIC ⁽¹⁾		TPS560200-Q1	UNIT
		DGK (VSSOP)	
		8 Pins	
R _{θJA}	Junction-to-ambient thermal resistance	184.7	°C/W
R _{θJC(top)}	Junction-to-case (top) thermal resistance	76.8	°C/W
R _{θJB}	Junction-to-board thermal resistance	106.0	°C/W
Ψ _{JT}	Junction-to-top characterization parameter	14.4	°C/W
Ψ _{JB}	Junction-to-board characterization parameter	104.3	°C/W
R _{θJC(bot)}	Junction-to-case (bottom) thermal resistance	N/A	°C/W

- (1) For more information about traditional and new thermal metrics, see the [Semiconductor and IC Package Thermal Metrics](#) application note.

5.5 Electrical Characteristics

$T_J = -40^{\circ}\text{C}$ to 125°C , $V_{IN} = 4.5\text{V}$ to 17V (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
SUPPLY VOLTAGE (VIN PIN)					
VIN Operating input voltage		4.5		17	V
VIN Internal UVLO wakeup	VIN Rising		4.35	4.5	V
VIN Internal UVLO shutdown	VIN Falling	3.9	4.15		V
VIN Shutdown supply current	EN = 0V, $V_{IN} = 12\text{V}$	2.0	3.7	9	μA
VIN Operating – non switching supply current	VSENSE = 850mV, $V_{IN} = 12\text{V}$	35	60	95	μA
ENABLE (EN PIN)					
Enable threshold	Rising		1.16	1.29	V
	Falling	1.05	1.13		V
Internal Soft-Start	VSENSE ramps from 0V to 0.8V		2		ms
OUTPUT VOLTAGE					
Voltage reference	25°C, $V_{IN} = 12\text{V}$, $V_{OUT} = 1.05\text{V}$, $I_{OUT} = 5\text{mA}$, Pulse-Skipping	0.796	0.804	0.812	V
	25°C, $V_{IN} = 12\text{V}$, $V_{OUT} = 1.05\text{V}$, $I_{OUT} = 100\text{mA}$, Continuous current mode	0.792	0.800	0.808	V
	$V_{IN} = 12\text{V}$, $V_{OUT} = 1.05\text{V}$, $I_{OUT} = 100\text{mA}$, Continuous current mode	0.789	0.800	0.811	V
MOSFET					
High-side switch resistance ⁽¹⁾	$V_{IN} = 12\text{V}$	0.50	0.95	1.50	Ω
Low-side switch resistance ⁽¹⁾	$V_{IN} = 12\text{V}$	0.20	0.33	0.55	Ω
CURRENT LIMIT					
Low-side switch sourcing current limit	$L_{OUT} = 10\mu\text{H}$, Valley current, $V_{OUT} = 1.05\text{V}$	570	670	795	mA
THERMAL SHUTDOWN					
Thermal shutdown			160		$^{\circ}\text{C}$
Thermal shutdown hysteresis			10		$^{\circ}\text{C}$
ON-TIME TIMER CONTROL					
On time	$V_{IN} = 12\text{V}$ ⁽¹⁾	130	165	200	ns
Minimum off time	25°C, VSENSE = 0.5V		250	400	ns
OUTPUT UNDERVOLTAGE PROTECTION					
Output UVP threshold	Falling	56	63	69	%VREF
Hiccup time			15		ms

(1) Not production tested

5.6 Typical Characteristics

$V_{IN} = 12V$, $T_A = 25^\circ C$ (unless otherwise noted).

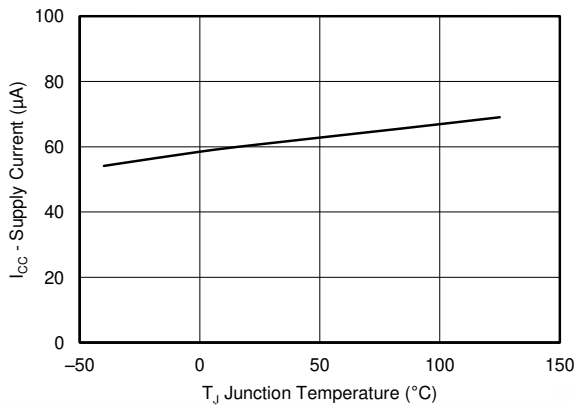


Figure 5-1. Supply Current vs Junction Temperature

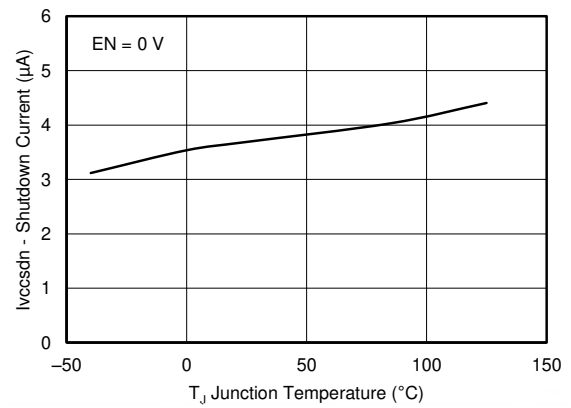


Figure 5-2. Shutdown Current vs Junction Temperature

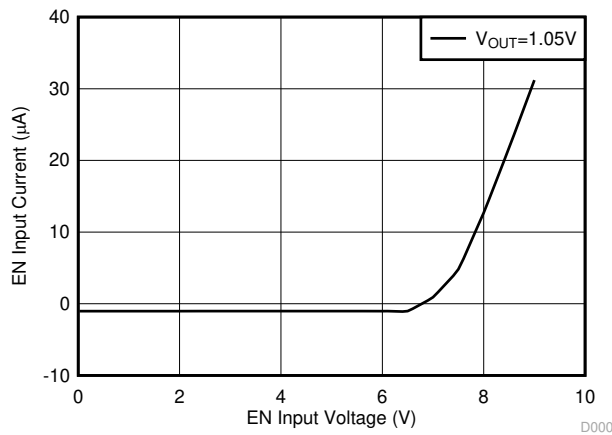


Figure 5-3. EN Input Current vs EN Input Voltage

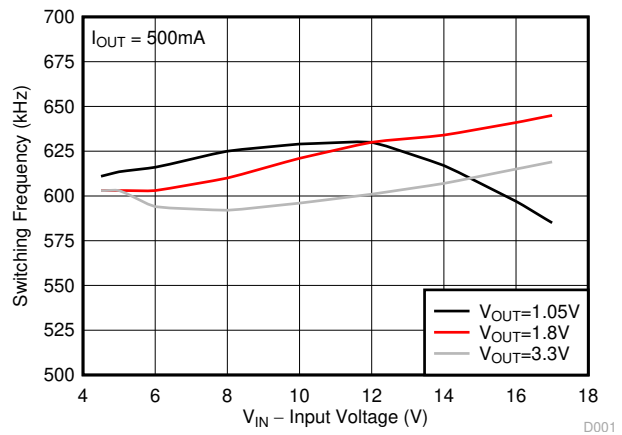


Figure 5-4. Switching Frequency vs Input Voltage

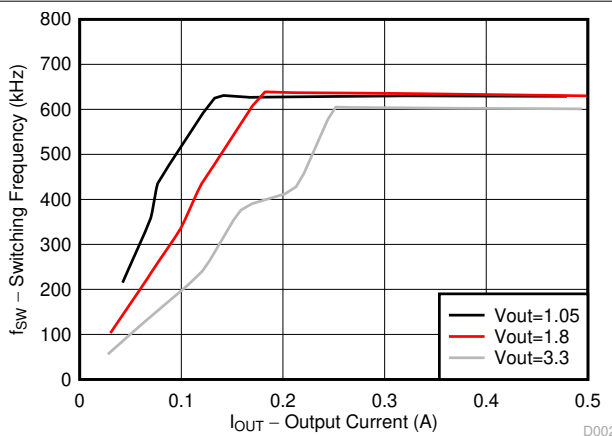


Figure 5-5. Switching Frequency vs Output Current

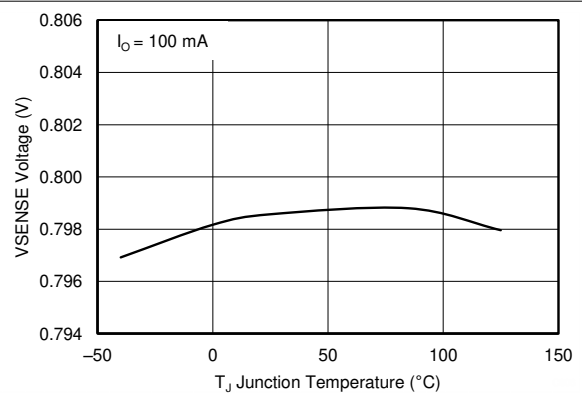


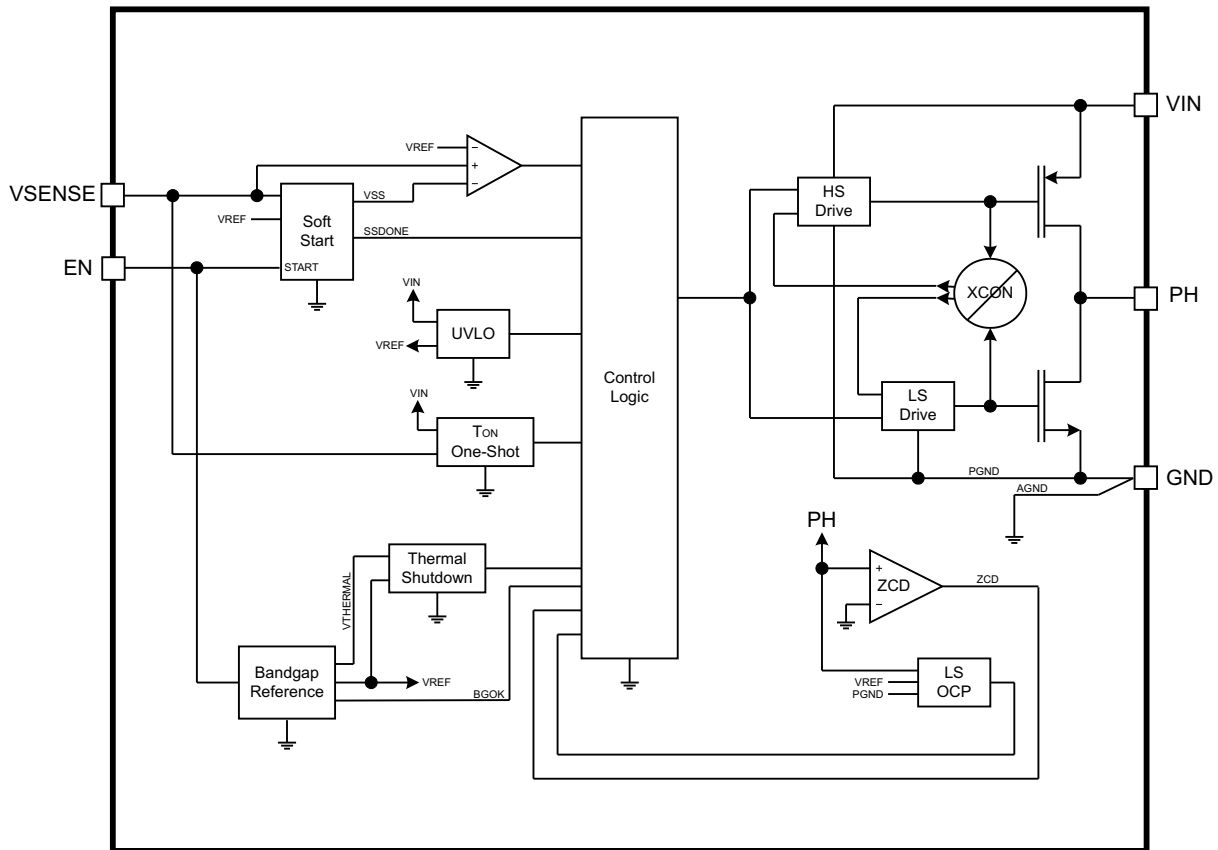
Figure 5-6. VSENSE Voltage vs Junction Temperature

6 Detailed Description

6.1 Overview

The TPS560200-Q1 is a 500mA, synchronous step-down (buck) converter with two integrated N-channel MOSFETs. The device operates using D-CAP2 control scheme. The fast transient response of D-CAP2 control scheme reduces the output capacitance required to meet a specific level of performance. Proprietary internal circuitry allows the use of low-ESR output capacitors including ceramic and special polymer types.

6.2 Functional Block Diagram



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6.3 Feature Description

6.3.1 PWM Operation

The main control loop of the TPS560200-Q1 is an adaptive on-time pulse width modulation (PWM) controller that supports a proprietary D-CAP2 control scheme. D-CAP2 control scheme combines constant on-time control with an internal compensation circuit for pseudo-fixed frequency and low external component count configuration with both low-ESR and ceramic output capacitors. D-CAP2 control scheme is stable even with virtually no ripple at the output.

At the beginning of each cycle, the high-side MOSFET is turned on. This MOSFET is turned off after internal one-shot timer expires. This one shot is set by the converter input voltage, V_{IN} , and the output voltage, V_{OUT} , to maintain a pseudo-fixed frequency over the input voltage range, therefore called adaptive on-time control. The one-shot timer is reset and the high-side MOSFET is turned on again when the feedback voltage falls below the reference voltage. An internal ramp is added to reference voltage to simulate output ripple, eliminating the need for ESR induced output ripple from D-CAP2 control scheme.

6.3.2 PWM Frequency and Adaptive On-Time Control

TPS560200-Q1 uses an adaptive on-time control scheme and does not have a dedicated on board oscillator. The TPS560200-Q1 runs with a pseudo-constant frequency of 600kHz by using the input voltage and output voltage to set the on-time, one-shot timer. The on-time is inversely proportional to the input voltage and proportional to the output voltage; therefore, when the duty ratio is V_{OUT}/V_{IN} , the frequency is constant.

6.3.3 Advanced Auto-Skip Eco-mode Control

The TPS560200-Q1 is designed with advanced auto-skip Eco-mode to increase higher light-load efficiency. As the output current decreases from heavy-load condition, the inductor current is also reduced. If the output current is reduced enough, the inductor current ripple valley reaches the zero level, which is the boundary between continuous conduction and discontinuous conduction modes. The rectifying low-side MOSFET is turned off when the zero inductor current is detected. As the load current further decreases the converter run into discontinuous conduction mode. The on-time is kept approximately the same as is in continuous conduction mode. The off-time increases as it takes more time to discharge the output capacitor to the level of the reference voltage with smaller load current. The transition point to the light load operation $I_{OUT(LL)}$ current can be calculated in [Equation 1](#).

$$I_{OUT(LL)} = \frac{1}{2 \times L_{OUT} \times f_{sw}} \times \frac{(V_{IN} - V_{OUT}) \times V_{OUT}}{V_{IN}} \quad (1)$$

6.3.4 Soft Start and Prebiased Soft Start

The TPS560200-Q1 has an internal 2ms soft start. When the EN pin becomes high, internal soft-start function begins ramping up the reference voltage to the PWM comparator.

The TPS560200-Q1 contains a unique circuit to prevent current from being pulled from the output during start-up if the output is prebiased. When the soft start commands a voltage higher than the prebias level (internal soft start becomes greater than feedback voltage V_{VSENSE}), the controller slowly activates synchronous rectification by starting the first low-side FET gate driver pulses with a narrow on-time. It then increments that on-time on a cycle-by-cycle basis until coinciding with the time dictated by $(1/D)$, where D is the duty cycle of the converter. This scheme prevents the initial sinking of the prebias output, and ensure that the out voltage (V_{OUT}) starts and ramps up smoothly into regulation and the control loop is given time to transition from prebiased start-up to normal mode operation.

6.3.5 Current Protection

The output overcurrent protection (OCP) is implemented using a cycle-by-cycle valley detect control circuit. The switch current is monitored by measuring the low-side FET switch voltage between the PH pin and GND. This voltage is proportional to the switch current. To improve accuracy, the voltage sensing is temperature compensated.

During the on-time of the high-side FET switch, the switch current increases at a linear rate determined by V_{IN} , V_{OUT} , the on-time and the output inductor value. During the on time of the low-side FET switch, this current decreases linearly. The average value of the switch current is the load current I_{out} . The TPS560200-Q1 constantly monitors the low-side FET switch voltage, which is proportional to the switch current, during the low-side on-time. If the measured voltage is above the voltage proportional to the current limit, an internal counter is incremented per each switching cycle and the converter maintains the low-side switch on until the measured voltage is below the voltage corresponding to the current limit at which time the switching cycle is terminated and a new switching cycle begins. In subsequent switching cycles, the on-time is set to a fixed value and the current is monitored in the same manner.

There are some important considerations for this type of overcurrent protection. The peak current is the average load current plus one half of the peak-to-peak inductor current. The valley current is the average load current minus one half of the peak-to-peak inductor current. Because the valley current is used to detect the overcurrent threshold, the load current is higher than the overcurrent threshold. Also, when the current is being limited, the output voltage tends to fall as the demanded load current can be higher than the current available from the

converter. This protection is non-latching. When the VSENSE voltage becomes lower than 63% of the target voltage, the UVP comparator detects the VSENSE voltage. After 7 μ s detecting the UVP voltage, device shuts down and re-starts after hiccup time.

When the overcurrent condition is removed, the output voltage returns to the regulated value.

6.3.6 Thermal Shutdown

TPS560200-Q1 monitors the temperature of TPS560200-Q1. If the temperature exceeds the threshold value (typically 160°C), the device is shut off. This is non-latch protection.

6.4 Device Functional Modes

6.4.1 Normal Operation

When the input voltage is above the UVLO threshold and the EN voltage is above the enable threshold, the TPS560200-Q1 can operate in the normal switching modes. Normal continuous conduction mode (CCM) occurs when the minimum switch current is above 0A. In CCM, the TPS560200-Q1 operates at a quasi-fixed frequency of 600kHz.

6.4.2 Eco-mode Operation

When the TPS560200-Q1 is in the normal CCM operating mode and the switch current falls to 0A, the TPS560200-Q1 begins operating in pulse-skipping Eco-mode. Each switching cycle is followed by a period of energy-saving sleep time. The sleep time ends when the VFB voltage falls below the Eco-mode threshold voltage. As the output current decreases the perceived time between switching pulses increases.

6.4.3 Standby Operation

When the TPS560200-Q1 is operating in either normal CCM or Eco-mode, TPS560200-Q1 can be placed in standby by asserting the EN pin low.

7 Application and Implementation

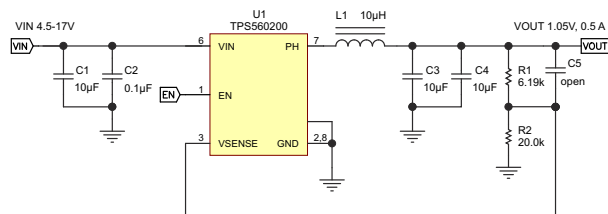
Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

7.1 Application Information

The TPS560200-Q1 is used as a step-down converter which converts a voltage of 4.5V to 17V to a lower voltage.

7.2 Typical Application



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Figure 7-1. Typical Application Schematic

7.2.1 Design Requirements

For this design example, refer to the application parameters shown in [Table 7-1](#).

Table 7-1. Design Parameters

PARAMETER	VALUES
Input voltage range	4.5V to 17V
Output voltage	1.05V
Output current	500mA
Output voltage ripple	30 mV/pp

7.2.2 Detailed Design Procedure

7.2.2.1 Output Voltage Resistors Selection

The output voltage is set with a resistor divider from the output node to the VFB pin. TI recommends using 1% tolerance or better divider resistors. Start by using [Equation 2](#) to calculate V_{OUT} .

To improve efficiency at light loads, consider using larger value resistors, high resistance is more susceptible to noise, and the voltage errors from the VSENSE input current are more noticeable.

$$R2 = \frac{R1 \times 0.8 \text{ V}}{V_{OUT} - 0.8 \text{ V}} \quad (2)$$

7.2.2.2 Output Filter Selection

The output filter used with the TPS560200-Q1 is an LC circuit. This LC filter has double pole at:

$$F_P = \frac{1}{2\pi\sqrt{L_{OUT} \times C_{OUT}}} \quad (3)$$

At low frequencies, the overall loop gain is set by the output set-point resistor divider network and the internal gain of the TPS560200-Q1. The low frequency phase is 180 degrees. At the output filter pole frequency, the gain rolls off at a –40dB per decade rate and the phase drops rapidly. D-CAP2 control scheme introduces a high frequency zero that reduces the gain roll off to –20dB per decade and increases the phase to 90 degrees one decade above the zero frequency. The inductor and capacitor selected for the output filter must be selected so that the double pole of Equation 3 is located below the high frequency zero but close enough that the phase boost provided by the high frequency zero provides adequate phase margin for a stable circuit. To meet this requirement use the values recommended in Table 7-2.

Table 7-2. Recommended Component Values

Output Voltage (V)	R1 (kΩ)	R2 (kΩ)	C5 (pF)	L1 (μH)			C3 + C4 (μF)
				MIN	TYP	MAX	
1.0	4.99	20.0			10		10 + 10
1.05	6.19	20.0			10		10 + 10
1.2	10.0	20.0			10		10 + 10
1.5	17.4	20.0			10		10 + 10
1.8	24.9	20.0	optional		10		10 + 10
2.5	42.2	20.0	optional		10		10 + 10
3.3	61.9	20.0	optional		10		10 + 10
5.0	105	20.0	optional		10		10 + 10

Because the DC gain is dependent on the output voltage, the required inductor value increases as the output voltage increases. Additional phase boost can be achieved by adding a feed-forward capacitor (C5) in parallel with R1. The feed-forward capacitor is most effective for output voltages at or above 1.8V.

The inductor peak-to-peak ripple current, peak current, and RMS current are calculated using Equation 4, Equation 5, and Equation 6. The inductor saturation current rating must be greater than the calculated peak current and the RMS or heating current rating must be greater than the calculated RMS current. Use 600kHz for f_{SW} .

Use 600kHz for f_{SW} . Make sure the chosen inductor is rated for the peak current of Equation 5 and the RMS current of Equation 6.

$$I_{LPP} = \frac{V_{OUT}}{V_{IN(max)}} \times \frac{V_{IN(max)} - V_{OUT}}{L_{OUT} \times f_{sw}} \quad (4)$$

$$I_{LPEAK} = I_{OUT} + \frac{I_{LPP}}{2} \quad (5)$$

$$I_{L_{OUT}(RMS)} = \sqrt{I_{OUT}^2 + \frac{1}{12} I_{LPP}^2} \quad (6)$$

For this design example, the calculated peak current is 0.582A and the calculated RMS current is 0.502A. The inductor used is a Würth 744777910 with a peak current rating of 2.6A and an RMS current rating of 2A.

The capacitor value and ESR determines the amount of output voltage ripple. The TPS560200-Q1 is intended for use with ceramic or other low-ESR capacitors. The recommended values are given in Table 7-2. Use Equation 7 to determine the required RMS current rating for the output capacitor.

$$I_{C_{OUT}(RMS)} = \frac{V_{OUT} \times (V_{IN} - V_{OUT})}{\sqrt{12} \times V_{IN} \times L_{OUT} \times f_{sw}} \quad (7)$$

For this design, two MuRata GRM32DR61E106KA12L 10 μ F output capacitors are used. The typical ESR is 2m Ω each. The calculated RMS current is 0.047A and each output capacitor is rated for 3A.

7.2.2.3 Input Capacitor Selection

The TPS560200-Q1 requires an input decoupling capacitor and a bulk capacitor is needed depending on the application. A ceramic capacitor over 10 μ F is recommended for the decoupling capacitor. An additional 0.1- μ F capacitor (C2) from pin 6 to ground is optional to provide additional high frequency filtering. The capacitor voltage rating must be greater than the maximum input voltage.

7.2.3 Application Curves

$V_{IN} = 12V$, $V_{OUT} = 1.05V$, $T_A = 25^\circ C$ (unless otherwise noted).

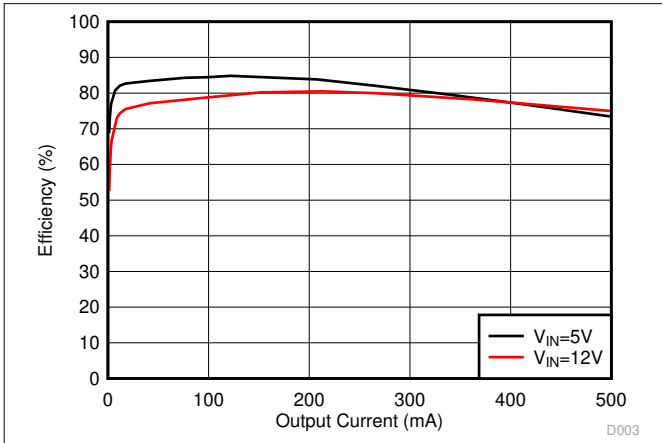


Figure 7-2. Efficiency

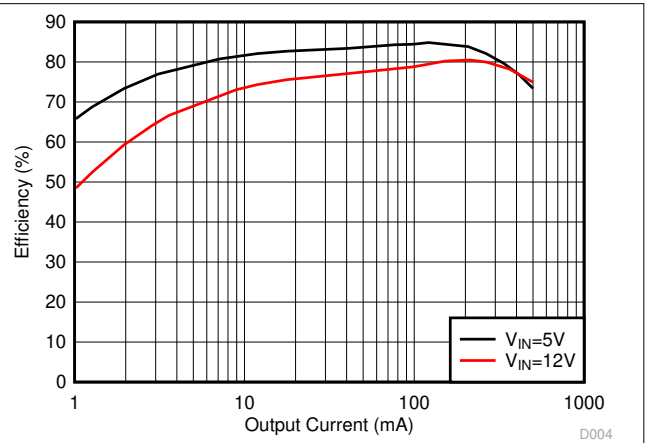


Figure 7-3. Light-Load Efficiency

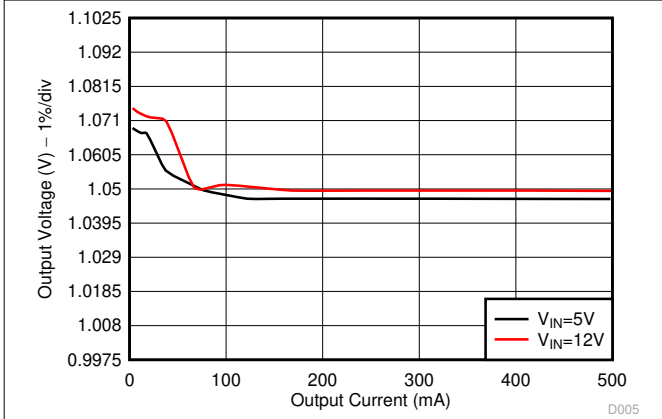


Figure 7-4. Load Regulation

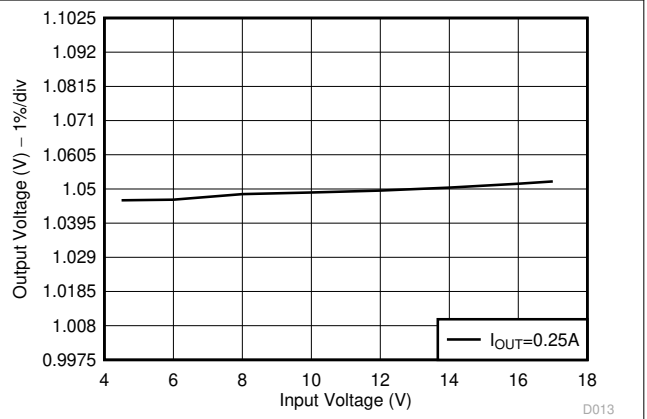


Figure 7-5. Line Regulation

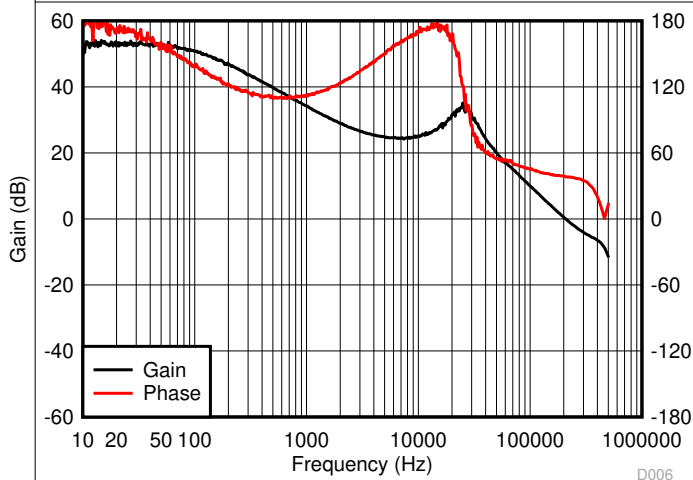


Figure 7-6. Loop Response, $I_{OUT} = 0.25A$

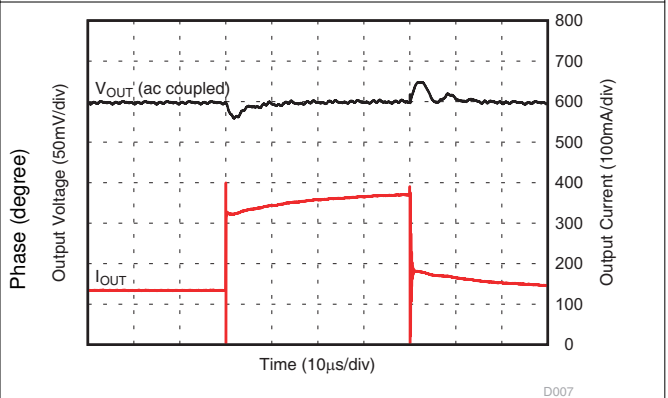


Figure 7-7. Transient Response, 25% to 75% Load Step

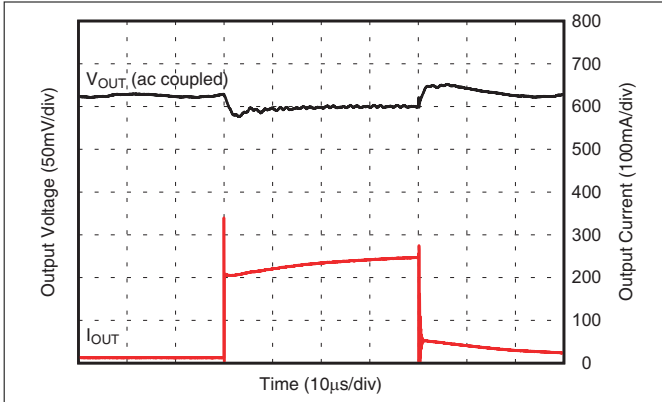


Figure 7-8. Transient Response, 2% to 50% Load Step

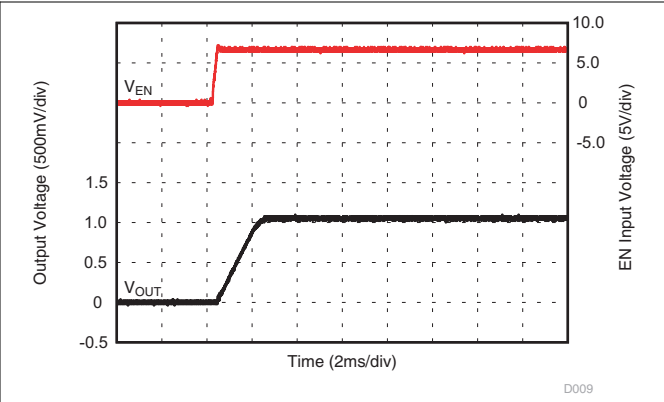


Figure 7-9. Start-Up Relative to EN

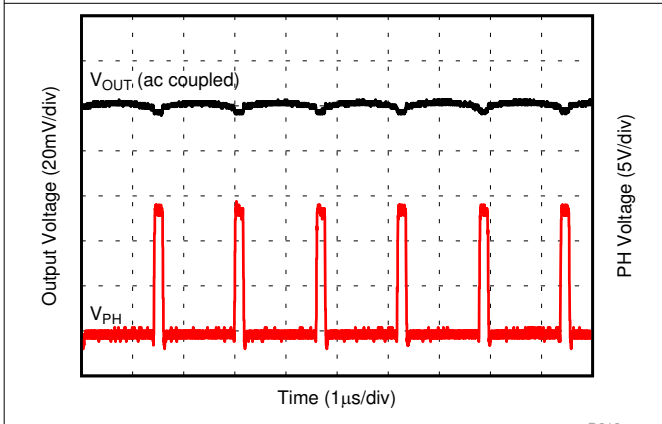


Figure 7-10. Output Ripple, I_{OUT} = 500mA

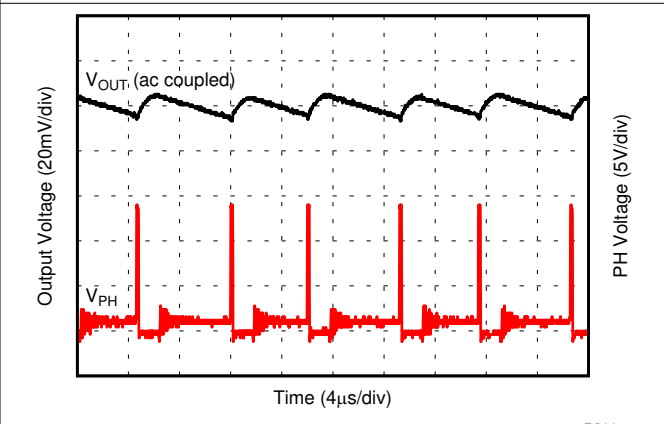


Figure 7-11. Output Ripple, I_{OUT} = 30mA

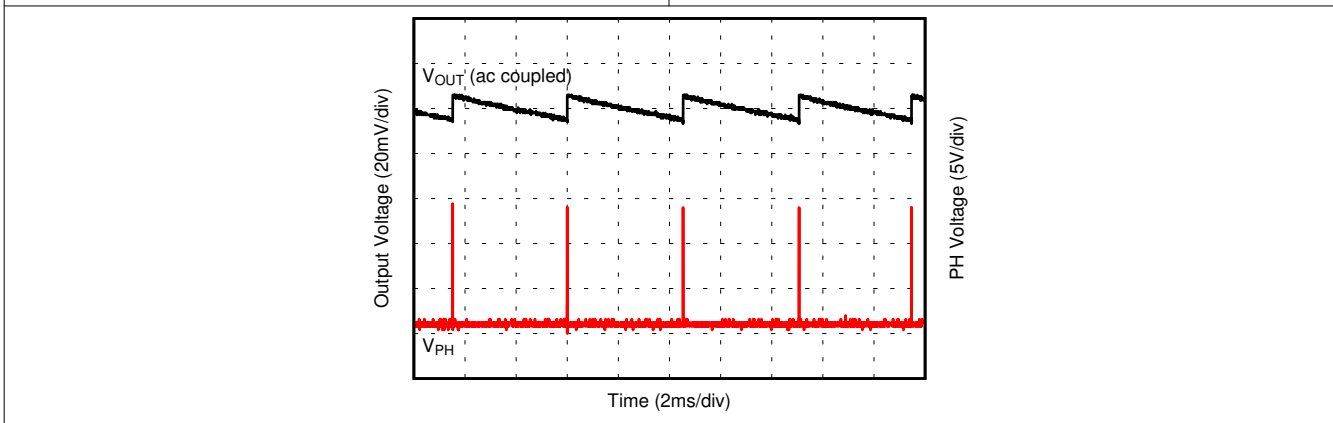


Figure 7-12. Output Ripple, I_{OUT} = 0mA

7.3 Power Supply Recommendations

The TPS560200-Q1 is designed to operate from input supply voltage in the range of 4.5V to 17V. Buck converters require the input voltage to be higher than the output voltage for proper operation. The maximum recommended operating duty cycle is 75%. Using that criteria, the minimum recommended input voltage is $V_O / 0.75$.

7.4 Layout

7.4.1 Layout Guidelines

The VIN pin must be bypassed to ground with a low-ESR ceramic bypass capacitor. Take care to minimize the loop area formed by the bypass capacitor connection, the VIN pin, and the GND pin of the IC. The typical recommended bypass capacitance is 10 μ F ceramic with a X5R or X7R dielectric and the optimum placement is closest to the VIN and GND pins of the device. An additional high-frequency bypass capacitor can be added. See [Figure 7-13](#) for a PCB layout example. The GND pin must be tied to the PCB ground plane at the pin of the IC. The PH pin must be routed to a small copper area directly adjacent to the pin. Make the circulating loop from PH to the output inductor, output capacitors and back to GND as tight as possible while preserving adequate etch width to reduce conduction losses in the copper. Use vias adjacent to the IC to tie top-side ground copper plane to the internal or bottom layer ground planes. The additional external components can be placed approximately as shown. Obtaining acceptable performance with alternate layout schemes can be possible; however, this layout produced good results and is intended as a guideline.

7.4.2 Layout Example

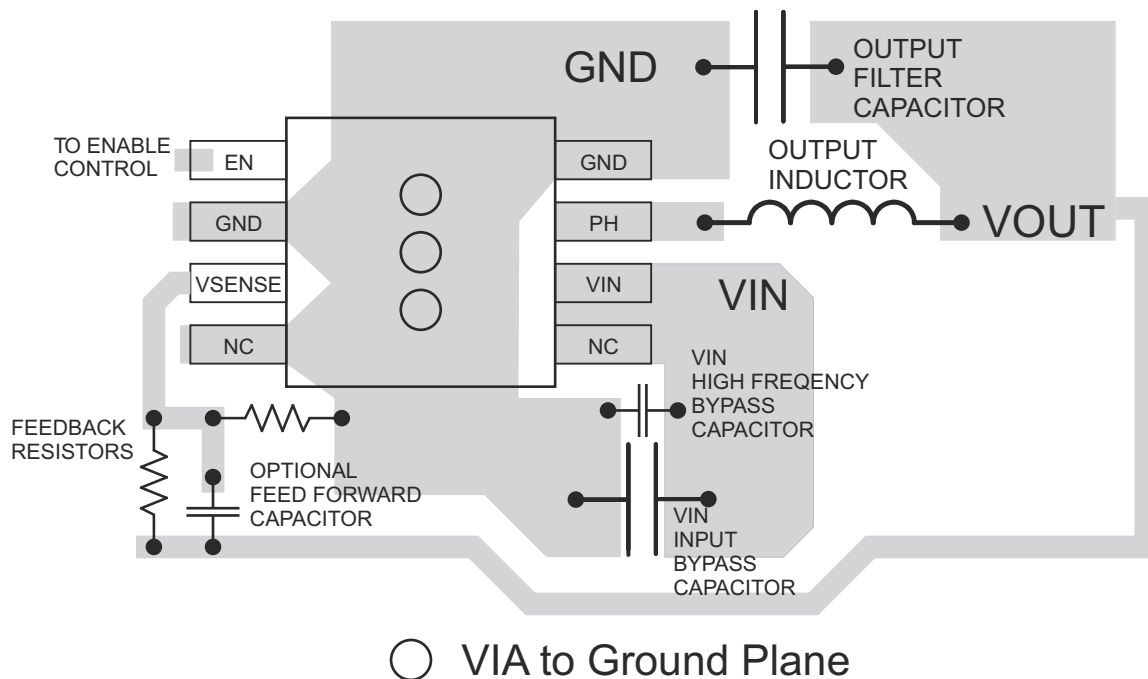


Figure 7-13. Layout Schematic

8 Device and Documentation Support

8.1 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

8.2 Support Resources

[TI E2E™ support forums](#) are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's [Terms of Use](#).

8.3 Trademarks

D-CAP2™ and TI E2E™ are trademarks of Texas Instruments.

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8.4 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

8.5 Glossary

[TI Glossary](#) This glossary lists and explains terms, acronyms, and definitions.

9 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision B (May 2019) to Revision C (June 2026)	Page
• Updated the numbering format for tables, figures, and cross-references throughout the document.....	1
• Added <i>Automotive</i> to the datasheet title.....	1
• Deleted the trademark symbol from Eco-mode throughout the document.....	1
• Added <i>control scheme</i> after D-CAP2 trademark throughout the document.....	1
• Changed from ANSI/ESDA/JEDEC JS-001 to AEC Q100-002 in the <i>ESD Ratings</i> table.....	4
• Updated table note 1 in the <i>ESD Ratings</i> table to comply with automotive standards.....	4
• Added link to table note 1 to the On Time spec in the <i>Electrical Characteristics</i> table.....	5
• Deleted WEBENCH reference in <i>Application Information</i>	10
<hr/>	
Changes from Revision A (May 2016) to Revision B (May 2019)	Page
• Editorial updates only; no technical changes	1
<hr/>	
Changes from Revision * (April 2016) to Revision A (May 2016)	Page
• Changed the device status From: Preview To: Production	1

10 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package Pins	Package qty Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TPS560200QDGKRQ1	Active	Production	VSSOP (DGK) 8	2500 LARGE T&R	Yes	NIPDAU NIPDAUAG	Level-2-260C-1 YEAR	-40 to 125	ZDNK
TPS560200QDGKRQ1.A	Active	Production	VSSOP (DGK) 8	2500 LARGE T&R	Yes	NIPDAUAG	Level-2-260C-1 YEAR	-40 to 125	ZDNK
TPS560200QDGKRQ1.B	Active	Production	VSSOP (DGK) 8	2500 LARGE T&R	Yes	NIPDAUAG	Level-2-260C-1 YEAR	-40 to 125	ZDNK
TPS560200QDGKTQ1	Active	Production	VSSOP (DGK) 8	250 SMALL T&R	Yes	NIPDAU NIPDAUAG	Level-2-260C-1 YEAR	-40 to 125	ZDNK
TPS560200QDGKTQ1.A	Active	Production	VSSOP (DGK) 8	250 SMALL T&R	Yes	NIPDAUAG	Level-2-260C-1 YEAR	-40 to 125	ZDNK
TPS560200QDGKTQ1.B	Active	Production	VSSOP (DGK) 8	250 SMALL T&R	Yes	NIPDAUAG	Level-2-260C-1 YEAR	-40 to 125	ZDNK

(1) **Status:** For more details on status, see our [product life cycle](#).

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

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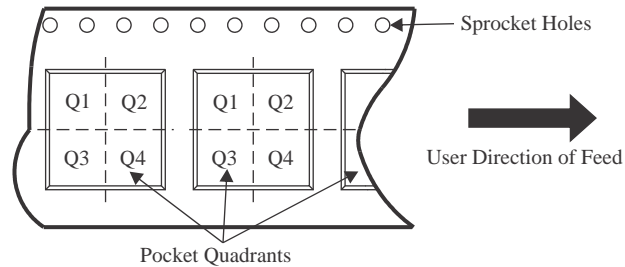
OTHER QUALIFIED VERSIONS OF TPS560200-Q1 :

- Catalog : [TPS560200](#)

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product

TAPE AND REEL INFORMATION

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE


*All dimensions are nominal

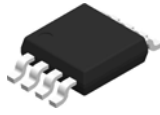
Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS560200QDGKRQ1	VSSOP	DGK	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
TPS560200QDGKTQ1	VSSOP	DGK	8	250	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
TPS560200QDGKTQ1	VSSOP	DGK	8	250	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS560200QDGKRQ1	VSSOP	DGK	8	2500	353.0	353.0	32.0
TPS560200QDGKTQ1	VSSOP	DGK	8	250	353.0	353.0	32.0
TPS560200QDGKTQ1	VSSOP	DGK	8	250	366.0	364.0	50.0

DGK0008A



PACKAGE OUTLINE

VSSOP - 1.1 mm max height

SMALL OUTLINE PACKAGE



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NOTES:

PowerPAD is a trademark of Texas Instruments.

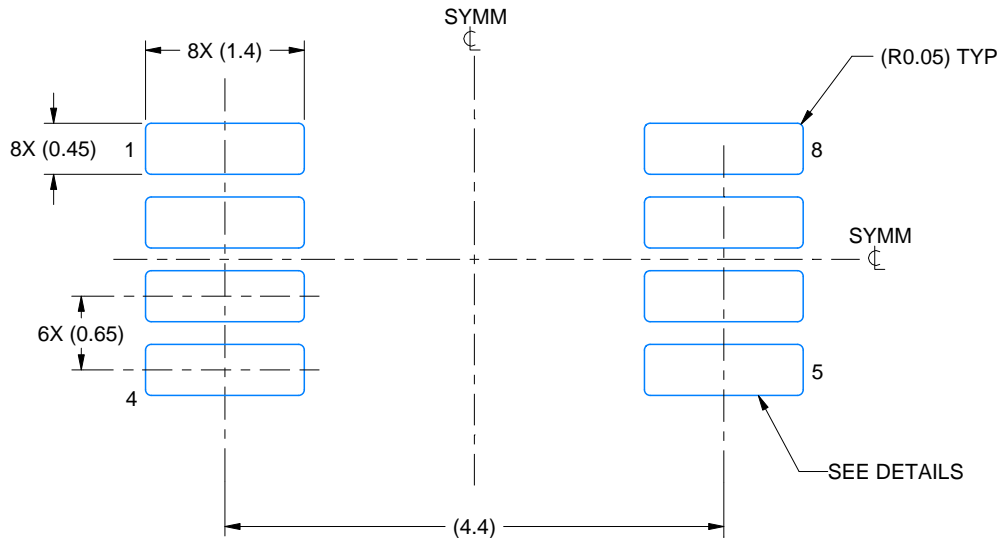
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-187.

EXAMPLE BOARD LAYOUT

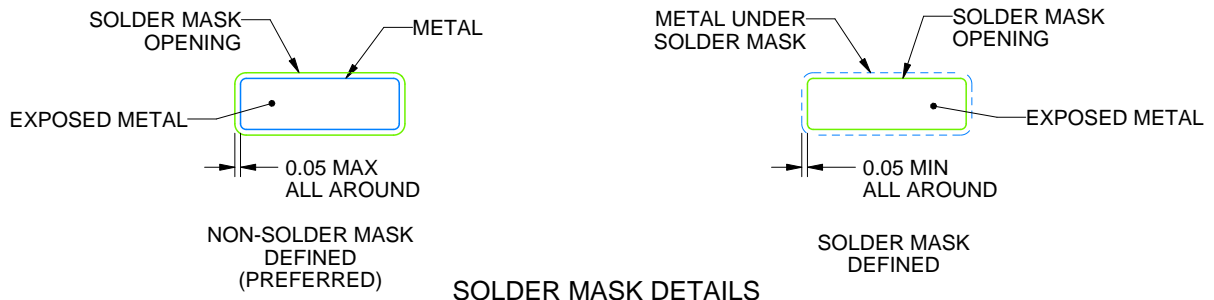
DGK0008A

™ VSSOP - 1.1 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 15X



SOLDER MASK DETAILS

4214862/A 04/2023

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.
9. Size of metal pad may vary due to creepage requirement.

EXAMPLE STENCIL DESIGN

DGK0008A

TM VSSOP - 1.1 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE
SCALE: 15X

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NOTES: (continued)

11. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
12. Board assembly site may have different recommendations for stencil design.

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