TPS61129-Q1 5.5V, 3.5A Isw Automotive Boost Converter With Clock Synchronization

1 Features

- AEC-Q100 qualified for automotive applications
  - Device temperature grade 1: –40°C to 125°C ambient operating temperature range
- Input voltage range: 0.9V to 5.5V
- Output voltage range: 2.6V to 5.5V
  - Fixed 5V or adjustable Vout: TPS61129-Q1
  - Fixed 3.85V Vout: TPS611291-Q1
  - Fixed 5.15V Vout: TPS611292-Q1
  - 275Ω output discharge resistance at EN = 0
- Typical 5µA quiescent current into VOUT pin
- Typical 0.01µA quiescent current into VIN pin
- Typical 100nA shutdown current
- Peak switching current limit: 3.5A typical
- Integrated LS / HS FET: 125mΩ / 145mΩ
- Switching frequency:
  - 2.2MHz for TPS61129-Q1
  - 2.0MHz for TPS611291-Q1
- ±6% spread spectrum modulation (SSEN enable)
- Auto PFM, forced PWM mode, SYNC selectable
- Down mode operation when Vin is close to or higher than Vout
- Windowed power good (PGOOD)
- True disconnect during shutdown
- OVP and thermal shutdown protections
- Output short-circuit protection
- 3mm × 3mm VSON-11 wettable flank package

2 Applications

- Automotive point of load
- Tablet (multimedia)
- Smart speaker
- Optical Module

3 Description

The TPS61129-Q1 provides a power supply design for portable equipment and smart devices, powered by various batteries and other power supplies. The TPS61129-Q1 has a 3.5A (typical) peak switch current limit. The TPS61129-Q1 employs peak current mode control with a fixed switching frequency of 2.2MHz. Under moderate to heavy load conditions, the TPS61129-Q1 operates in pulse width modulation (PWM) mode. At light load, the device has two operating modes that can be selected through the MODE pin. One is pulse frequency modulation (auto PFM) mode to improve light-load efficiency, and the other is forced PWM mode to avoid audible noise and to improve light load ripple performance. The switching frequency can also be synchronized to an external clock. The TPS61129-Q1 implements spread spectrum modulation on the internal clock signal, significantly enhancing electromagnetic interference (EMI) performance when operating in Forced PWM mode. In addition, there is an internal soft-start time to limit the inrush current during start-up.

During shutdown, the output load is fully isolated from the input power source, and the TPS61129-Q1 only consumes a 0.1µA current to achieve long battery life.

The TPS61129-Q1 output voltage can be programmed by an external resistor divider, or is available with fixed 5.15V, 5.0V, and 3.85V options internally on the chip.

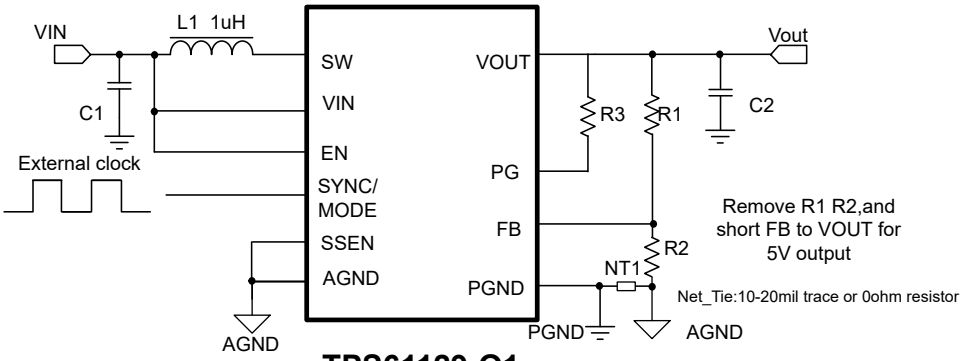
The TPS61129-Q1 offers a very small design size with a 3.0mm × 3.0mm wettable flank VSON package.

Device Information

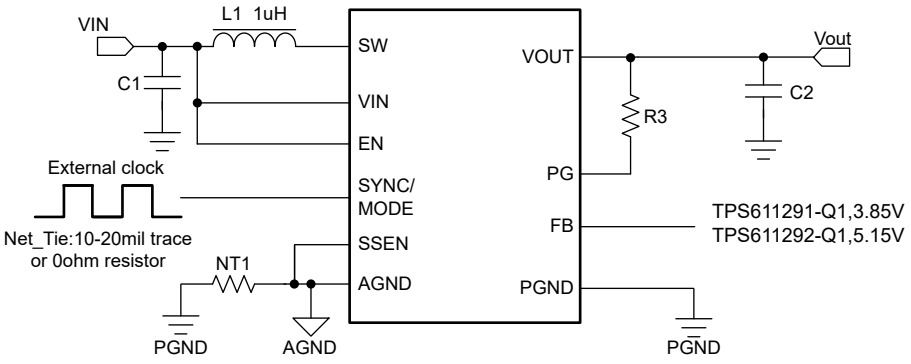
PART NUMBER(3)	PACKAGE(1)	PACKAGE SIZE(2)
TPS61129-Q1	DRC (VSON, 11)	3mm × 3mm
TPS611291-Q1(4)		
TPS611292-Q1(4)		

(1) For more information, see Section 11.
(2) The package size (length × width) is a nominal value and includes pins, where applicable.
(3) See the *Device Comparison Table*.
(4) Product Preview (not Advance Information).

ADVANCE INFORMATION



TPS61129-Q1 Typical Schematic for Fixed 5V or Adjustable Output



TPS611291-Q1, TPS611292-Q1 Typical Schematic for Fixed Output

ADVANCE INFORMATION

Table of Contents

ADVANCE INFORMATION

ADVANCE INFORMATION

4 Device Comparison Table

PART NUMBER	OUTPUT VOLTAGE
TPS61129QDRCRQ1	Adjustable or fixed 5V when FB pin is connected to VOUT pin
TPS611291QDRCRQ1(1)	Fixed 3.85V
TPS611292QDRCRQ1(1)	Fixed 5.15V

(1) Product Preview (not Advance Information).

5 Pin Configuration and Functions

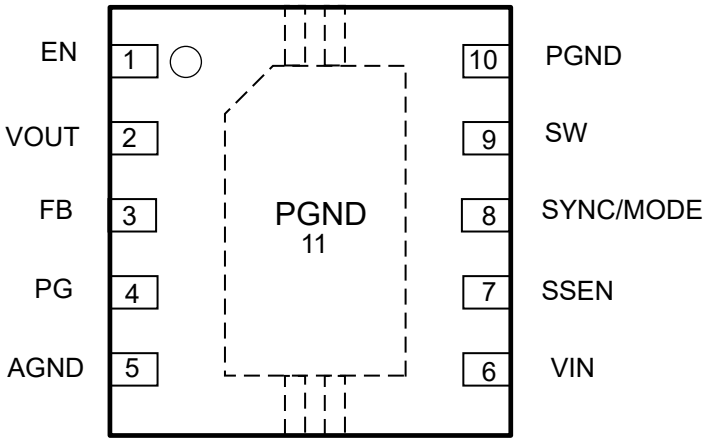


Figure 5-1. DRC Package, VSON 11 Pin (Top View)

Table 5-1. Pin Functions

PIN		TYPE(1)	DESCRIPTION
NAME	NO.		
EN	1	I	Device enable logic input (High enabled, Low disabled). This pin must not be left floating and must be terminated.
VOUT	2	PWR	Boost converter output
FB	3	I	Voltage feedback of adjustable versions. Connect to the center tap of a resistor divider to program the output voltage or connect to VOUT pin directly for fixed 5Vout. Leaves floating for TPS611291-Q1 and TPS611292-Q1.
PG	4	O	Power-good indicator and open drain output
AGND	5	PWR	Analog ground of the IC
VIN	6	I	Supply voltage
SSEN	7	I	Spread spectrum modulation control pin. SSEN = high, Spread spectrum modulation enable. SSEN = low, Spread spectrum modulation disable. This pin must not be left floating and must be terminated.
SYNC/MODE	8	I	Mode selection pin. MODE = high, forced PWM mode. MODE = low or floating, auto PFM mode. This pin can also be used to synchronize the external clock.
SW	9	PWR	The switching node pin of the converter
PGND	10, 11	PWR	Power ground of the IC

(1) I = input, O = output, PWR = power

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
Voltage	Input voltage on SW, VOUT, EN, FB, PG, VIN, SSEN, SYNC/MODE	–0.3	7	V
	SW spike at 10ns	–0.7	8	V
	SW spike at 1ns	–0.7	10	V
T_{stg}	Storage temperature	–65	150	°C
T_J	Operating Junction Temperature	–40	150	°C

(1) Operation outside the Absolute Maximum Ratings may cause permanent device damage. Absolute Maximum Ratings do not imply functional operation of the device at these or any other conditions beyond those listed under Recommended Operating Conditions. If used outside the Recommended Operating Conditions but within the Absolute Maximum Ratings, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per AEC Q100-002(1), all pins(1)	±2000	V
		Charged device model (CDM), per AEC Q100-011, all pins	±500	

(1) AEC Q100-002 indicates that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
V_{IN}	Input voltage	0.9		5.5	V
V_{OUT}	Boost output voltage	2.6		5.5	V
T_J	Operating junction temperature(1)	–40		150	°C
L	Effective inductance	0.7	1.0		µH
C_{OUT}	Effective output capacitance at the VOUT pin	10	22		µF
C_{IN}	Effective input capacitance at the VIN pin	4.7			µF

(1) High junction temperatures degrade operating lifetimes. Operating lifetime is derated for junction temperatures greater than 125°C

6.4 Thermal Information

THERMAL METRIC(1)		DRC VSON 11PINS Standard	All 11PINS EVM(2)	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	67	61.4	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	45	NA	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	19.4	NA	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	5.0	4.0	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	23	22.4	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	NA	NA	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application note.
(2) Measured on TPS61129Q1EVM.

ADVANCE INFORMATION

ADVANCE INFORMATION

6.5 Electrical Characteristics

T_J = –40°C to 150°C, V_{IN} = 3.3V and V_{OUT} = 5.0V. Typical values are at T_J = 25°C, unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
POWER SUPPLY						
V_{IN}	Input voltage range		0.9		5.5	V
V_{IN_UVLO}	Undervoltage lockout threshold	V_{IN} rising		0.7	0.9	V
I_Q	Quiescent current into VIN pin	IC enabled, no load, no switching, VIN = 0.9V to 5.5V, VFB = VREF + 0.01V, T_J up to 125°C		0.01	0.3	µA
I_Q	Quiescent current into VOUT pin	IC enabled, no load, no switching, VOUT = 2.6V to 5.5V, VFB = VREF + 0.015V, T_J up to 125°C		5	10	µA
I_Q	Quiescent current into VOUT pin fixed 5Vout	IC enabled, no load, no switching, VOUT = VFB = 5V+0.15V, T_J up to 125°C		5	10	µA
I_{SD}	Shutdown current into VIN pin	EN = LOW, VOUT = 0V, T_J = 25°C		0.1	0.2	µA
I_{SD}	Shutdown current into VIN pin	EN = LOW, VOUT = 0V, T_J = 125°C		0.1	1.2	µA
I_{SW_LKG}	Leakage current into SW pin (from SW pin to GND pin)	V_{SW} = 3.3V, V_{OUT} = 0V,T_J up to 125°C			3	µA
I_{FB_LKG}	Leakage current at FB pin	T_J up to 125°C		4	30	nA
OUTPUT						
V_O	Output voltage range		2.6		5.5	V
V_{FB}	Feedback voltage	TPS61129-Q1, Forced PWM Mode	492.5	500	507.5	mV
V_{FB}	Feedback voltage	TPS61129-Q1, Auto PFM Mode		505		mV
V_O	Fixed output voltage	TPS61129-Q1, Forced PWM Mode, FB connected to V_{OUT}	4.9	5	5.1	V
V_O	Fixed output voltage	TPS611291-Q1, Forced PWM Mode, FB floating	3.77	3.85	3.93	V
V_{OVP}	Output overvoltage protection	V_{OUT} rising	5.6	5.75	6.0	V
R_{DIS}	Output discharge resistor	VIN = 0.9V to 5.5V		275		Ω
t_{ss}	Soft start-up time	Internal SS ramp time		1.0		ms
V_{down_mode}	Enter down mode threshold for TPS61129	V_{IN} > V_{OUT} - V_{down_mode}		235		mV
V_{down_mode}	Exit down mode threshold for TPS61129	V_{IN} < V_{OUT} - V_{down_mode}		285		mV
V_{down_mode}	Enter down mode threshold for TPS611291(V_{OUT} = 3.85V)	V_{IN} > V_{OUT} - V_{down_mode}		143		mV
V_{down_mode}	Exit down mode threshold for TPS611291(V_{OUT} = 3.85V)	V_{IN} < V_{OUT} - V_{down_mode}		199		mV
POWER SWITCH						
f_{SW}	Switching frequency for TPS61129		1.9	2.2	2.5	MHz
f_{SW}	Switching frequency for TPS611291		1.8	2.0	2.2	MHz
I_{SW}	Peak current limit	V_{OUT} = 5V	3.0	3.5		A
$R_{DS(on)}$	High-side MOSFET on resistance	V_{OUT} = 3.85V		180		mΩ
$R_{DS(on)}$	Low-side MOSFET on resistance	V_{OUT} = 3.85V		150		mΩ
$R_{DS(on)}$	High-side MOSFET on resistance	V_{OUT} = 5V		145		mΩ
$R_{DS(on)}$	Low-side MOSFET on resistance	V_{OUT} = 5V		125		mΩ
t_{OFF_min}	Minimum off time	V_{OUT} = 5V		77		ns

6.5 Electrical Characteristics (continued)

T_J = –40°C to 150°C, V_{IN} = 3.3V and V_{OUT} = 5.0V. Typical values are at T_J = 25°C, unless otherwise noted.

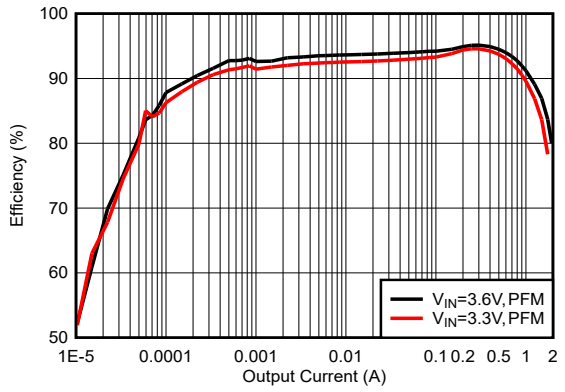
PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{ON_min}	Minimum on time	V_{OUT} = 5V		70		ns
t_{OFF_min}	Minimum off time	V_{OUT} = 3.85V		85		ns
t_{ON_min}	Minimum on time	V_{OUT} = 3.85V		80		ns
f_{SYNC} minimum	Minimum sync frequency			1.5		MHz
f_{SYNC} maximum	Maximum sync frequency			3.3		MHz
f_{SPREAD}	Spread of internal oscillator with spread spectrum enabled			±6		%
$f_{PATTERN}$	Frequency of the frequency dithering pattern			9		kHz
t_{SYNC_MIN}	Minimum sync clock pulse width		50			ns
LOGIC INTERFACE						
V_{SSEN_H}	SSEN logic high threshold	V_{IN} <1.05 V			0.8 × V_{IN}	V
V_{SSEN_L}	SSEN logic low threshold	V_{IN} <1.05 V	0.2 × V_{IN}			V
V_{SSEN_H}	SSEN logic high threshold	V_{IN}>= 1.05V			0.84	V
V_{SSEN_L}	SSEN logic low threshold	V_{IN} >= 1.05V	0.36			V
V_{EN}	EN logic high threshold	V_{IN} < 1.05V			0.8×V_{IN}	V
V_{EN}	EN logic low threshold	V_{IN} < 1.05V	0.2 × V_{IN}			V
V_{EN}	EN logic high threshold	V_{IN} >= 1.05V			0.84	V
V_{EN}	EN logic low threshold	V_{IN} >= 1.05V	0.36			V
I_{EN}	Leakage current into EN pin			5	100	nA
I_{SS_LKG}	Leakage current into SSEN pin			1.2	110	nA
$R_{EN/SS}$	Active EN pin pulldown resistor	EN=low		100		kΩ
$V_{SYNC/MODE\_H}$	SYNC/MODE logic high threshold				1.2	V
$V_{SYNC/MODE\_L}$	SYNC/MODE logic low threshold		0.4			V
$R_{SYNC/MODE}$	Active SYNC/MODE pin pulldown resistor			100		kΩ
POWER GOOD						
PGD_{OV}	PGOOD upper threshold, rising	% of nominal output	104	107	110	%
PGD_{UV}	PGOOD lower threshold, falling	% of nominal output	90	93	96	%
PGDHYS	PGOOD hysteresis	% of nominal output		2.0		%
$t_{PGFLT(rise)}$	Delay time to PGOOD high signal			0.45		ms
$t_{PGFLT(fall)}$	Glitch filter time of PGOOD			33		µs
R_{PG_LOW}	PGOOD pulldown resistor	Sinking 2mA			50	Ω
PROTECTION						
T_{SD}	Thermal shutdown threshold	T_J rising		175		°C
T_{SD}	Thermal shutdown threshold	T_J falling		155		°C
T_{SD_HYS}	Thermal shutdown hysteresis	T_J falling below T_{SD}		20		°C

ADVANCE INFORMATION

ADVANCE INFORMATION

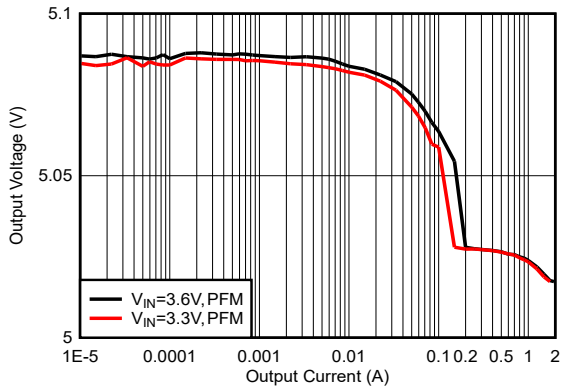
6.6 Typical Characteristics

Based on TPS61129Q1-EVM, T_J = 25°C, unless otherwise noted.



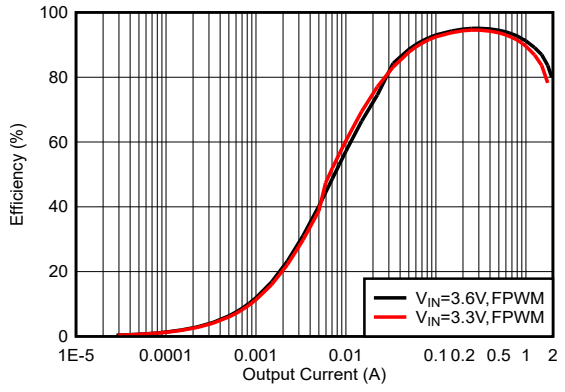
V_{IN} = 3.3V, 3.6V V_{OUT} = 5V SYNC/MODE = Low

Figure 6-1. Efficiency vs Output Current, Auto PFM Mode



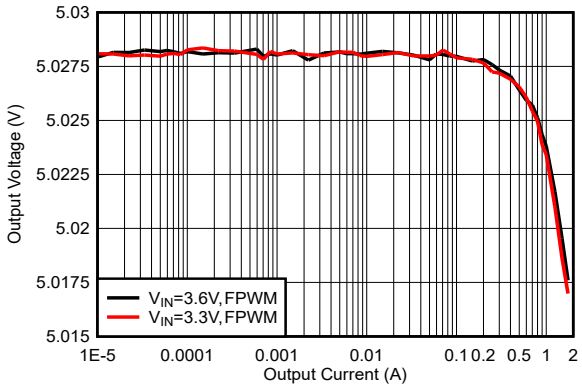
V_{IN} = 3.3V, 3.6V V_{OUT}= 5V SYNC/MODE = Low

Figure 6-2. Output regulation vs Output Current, Auto PFM Mode



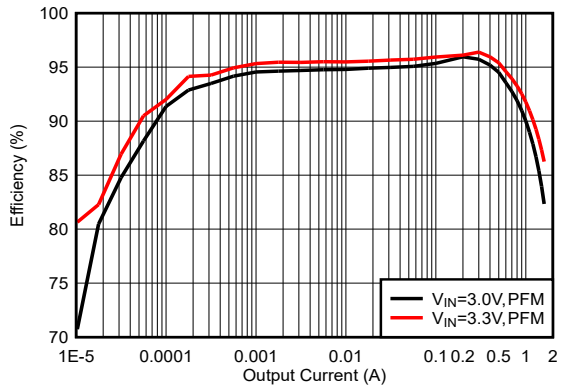
V_{IN} = 3.3V, 3.6V V_{OUT} = 5V SYNC/MODE = High

Figure 6-3. Efficiency vs Output Current, Forced PWM Mode



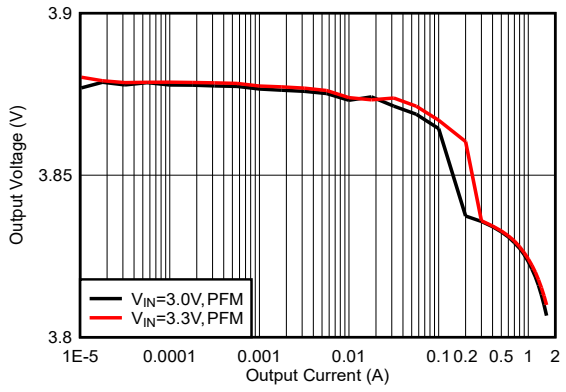
V_{IN} = 3.3V, 3.6V V_{OUT} = 5V SYNC/MODE = High

Figure 6-4. Output regulation vs Output Current, Forced PWM Mode



V_{IN} = 3.0V, 3.3V V_{OUT} = 3.85V SYNC/MODE = Low

Figure 6-5. Efficiency vs Output Current, Auto PFM Mode

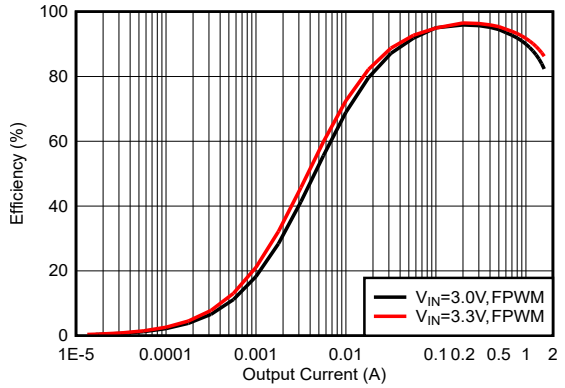


V_{IN} = 3.0V, 3.3V V_{OUT} = 3.85V SYNC/MODE = Low

Figure 6-6. Output regulation vs Output Current, Auto PFM Mode

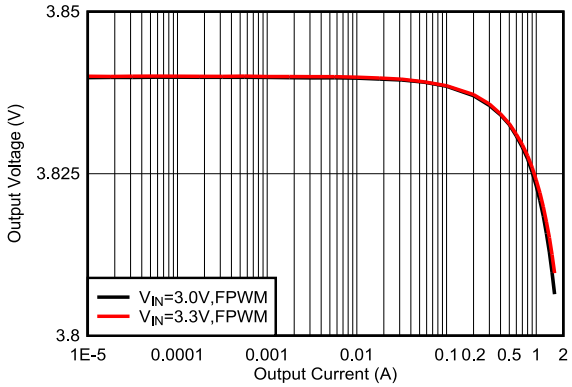
6.6 Typical Characteristics (continued)

Based on TPS61129Q1-EVM, T_J = 25°C, unless otherwise noted.



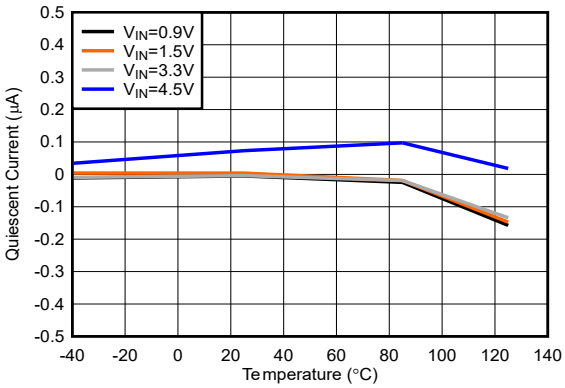
V_{IN} = 3.0V, 3.3V V_{OUT} = 3.85V SYNC/MODE = High

Figure 6-7. Efficiency vs Output Current, Forced PWM Mode



V_{IN} = 3.0V, 3.3V V_{OUT} = 3.85V SYNC/MODE = High

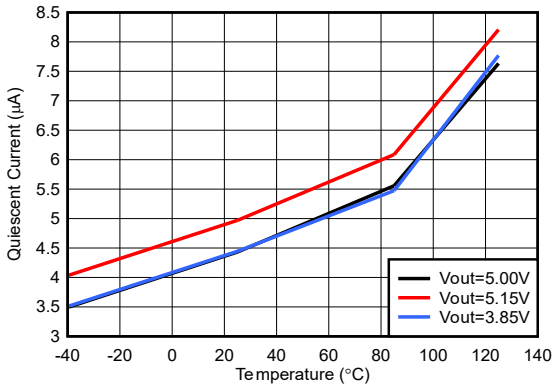
Figure 6-8. Output regulation vs Output Current, Forced PWM Mode



V_{IN} = 0.9V, 1.5V, 3.3V, 4.5V

V_{OUT} = 5V T_J = –40°C to +125°C, No switching

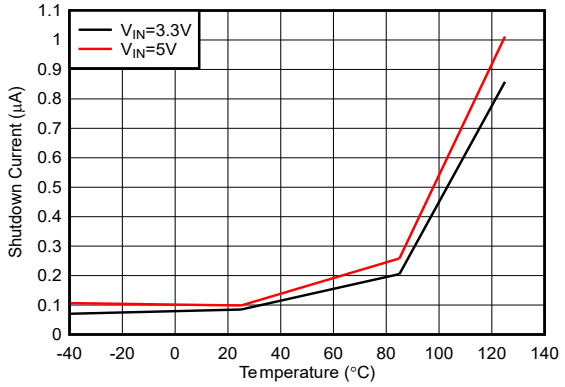
Figure 6-9. Quiescent Current into VIN vs Temperature



V_{IN} = 3.3V, V_{OUT} = 3.85V, 5V, 5.15V

T_J = –40°C to +125°C, No switching

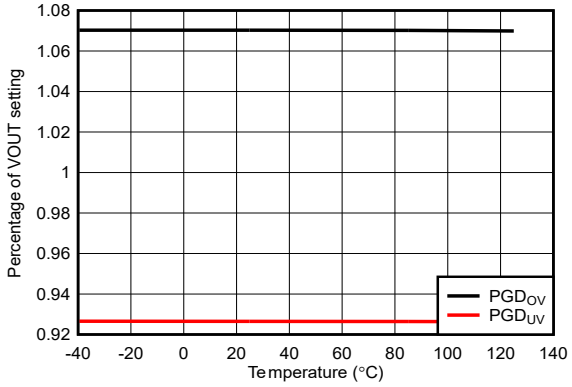
Figure 6-10. Quiescent Current into VOUT vs Temperature



V_{IN} = VSW = 3.3V, 5V, EN=0V

V_{OUT}= 0V, T_J = –40°C to +125°C

Figure 6-11. Shutdown Current vs Temperature



V_{IN} = 3.3V, V_{OUT} = 5V

T_J = –40°C to +125°C

Figure 6-12. PGOOD threshold vs Temperature

ADVANCE INFORMATION

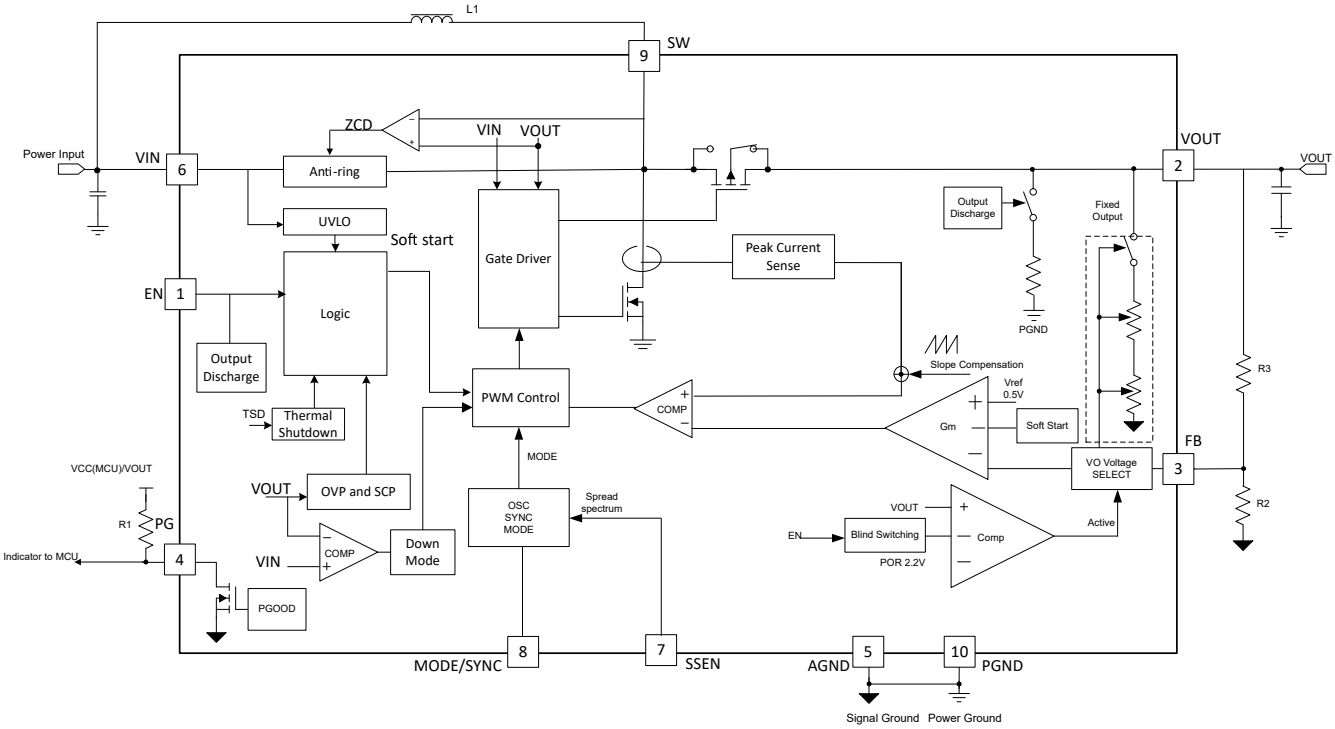
ADVANCE INFORMATION

7 Detailed Description

7.1 Overview

The TPS61129-Q1 delivers power supply designs for portable and smart devices, compatible with various power sources. With a 3.5A typical peak switch current limit, the device operates at a fixed 2.2MHz switching frequency using peak current mode control. The device functions in forced PWM mode under moderate to heavy loads, while offering two selectable light-load modes through the MODE pin: auto PFM mode for improved efficiency and forced PWM mode for reduced audible noise and better ripple performance. The switching frequency can be synchronized with an external clock. In forced PWM mode, spread spectrum technology enhances EMI performance. An internal soft-start time is implemented to limit the inrush current.

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 Synchronous Rectifier and True Shutdown

The device integrates an N-Channel and a P-Channel MOSFET transistor to realize a synchronous rectifier. Because the commonly used discrete Schottky rectifier is replaced with a low RDS(ON) PMOS switch, the power conversion efficiency is high. To avoid ground shift due to the high currents in the NMOS switch, two separate ground pins are used. The reference for all control functions is the AGND pin. The source of the NMOS switch is connected to PGND. Both grounds must be connected on the PCB at only one point close to the AGND pin. A special circuit is applied to disconnect the load from the input during shutdown of the converter. In conventional synchronous rectifier circuits, the back gate diode of the high-side PMOS is forward biased in shutdown and allows current flowing from the battery to the output. This device, however, uses a special circuit, which takes the cathode of the back gate diode of the high-side PMOS and disconnects the cathode from the source when the device is not enabled (EN = low).

The benefit of this feature for the system design is that the battery is not depleted during shutdown of the converter. No additional components have to be added to the design to make sure that the battery is disconnected from the output of the converter.

7.3.2 Device Enable

The device is put into operation when EN is set high. The device is put into a shutdown mode when EN is set to GND. In shutdown mode, the regulator stops switching, all internal control circuitry is switched off, and the load is isolated from the input (as described in the *Synchronous Rectifier and True Shutdown* section). This action also means that the output voltage can drop below the input voltage during shutdown. During start-up of the converter, the duty cycle and the peak current are limited to avoid high peak currents drawn from the battery.

During soft start, when Vout ramps to 2.2V, the reserved OTP is read, to detect whether the device is a fixed output or FB adjustable version.

For the fixed version, such as TPS611291-Q1 and TPS611292-Q1, when Vout rises to 2.2V, the variant version is read and the Vout ramps to the target, such as 3.85V or 5.15V. There is no electrical connection between the internal circuit and the FB pin.

For the adjustable version TPS61129-Q1, when Vout rises to 2.2V, the FB voltage is compared with the internal reference, 0.5V. Therefore, the loop works and output can be regulated to the target voltage.

7.3.3 Down Mode Threshold

In general, a boost converter only regulates output voltages which are higher than the input voltage. This device operates differently. If the input voltage reaches or exceeds the V_{OUT} – 235mV (typical), the converter enters to the down mode. In this mode, the control circuit adjusts the rectifying PMOS so that the voltage drop rises as needed to regulate VOUT. This action means the power losses in the converter increase. This increase must be taken into account for thermal considerations. When the input voltage drops below the output voltage minus 285mV (typical), the down mode automatically deactivates.

7.3.4 SYNC/MODE Configuration

The SYNC/MODE pin can be used to select different operation modes. To enable auto PFM, SYNC/MODE must be set low. Auto PFM mode is used to improve efficiency at light load. In auto PFM mode, the converter only operates when the output voltage trips below a set threshold voltage. The converter ramps up the output voltage with one or several pulses and goes again into auto PFM mode after the output voltage exceeds the set threshold voltage. This auto PFM mode can be disabled by connecting the SYNC/MODE pin to logic high, therefore the device works in forced PWM mode.

The SYNC/MODE pin can also be used to synchronize the device switching frequency with an external clock signal from 1.5MHz to 3.3MHz.

7.3.5 Output Discharge

The TPS61129-Q1 provides a resistive path to quickly discharge output when the EN pin is logic low. With this function, the VOUT is connected to ground through an internal resistor with typical resistance of 275Ω, preventing the output from “floating” or entering into an undetermined state. The output-discharge function smooths power-on and power-off sequencing. Pay attention to the output discharge function when using this device in applications such as power multiplexing, because the output discharge circuitry creates a constant current path between the multiplexer output and the ground.

7.3.6 Soft Start and Short-Circuit Protection

When the input voltage is above the UVLO threshold and the EN pin is pulled high, the TPS61129-Q1 is enabled. To limit the inrush current and power dissipation on the high-side FET, the peak switching current limit is gradually released from 500mA to the normal current limit of 3.5A (typical), based on the voltage at the VOUT pin and working mode. There are a total of three phases during start-up, as summarized in the Table 7-1.

Under abnormal operating conditions, such as when the VOUT pin is shorted to the GND, the device behaves exactly as described in PHASE I .

ADVANCE INFORMATION

Table 7-1. Peak Switching Current Limit in Different Work Conditions, With VIN = 3.3V, VOUT = 5V

PHASE NUMBER	V_{IN} and V_{OUT} CONDITIONS	TYPICAL PEAK SWITCHING CURRENT LIMIT
I	V_{OUT} < 2.2V	0.5A
II	(Down mode) 2.4V < V_{OUT} < V_{IN} + V_{down_mode} (1)	1.5A
III	(Boost mode) V_{IN} + V_{down_mode} < V_{OUT} (1)	3.5A

(1) V_{down_mode} = 235mV for down mode entering, V_{down_mode} = 285mV for down mode existence.

7.3.7 Power-Good Indicator

The TPS61129-Q1 integrates a power-good indicator to simplify sequencing and supervision. The power-good output consists of an open-drain NMOS, requiring an external pullup resistor connected to a suitable voltage supply. The PG pin goes high with a typical 0.45ms delay time after VOUT is between 93% (typical) and 107% (typical) of the target output voltage. When the output voltage is out of the target output voltage window, the PG pin immediately goes low with a 33µs deglitch filter delay. This deglitch filter also prevents any false pulldown of the PGOOD due to transients. When EN is low, PG is forced low after a 33µs deglitch delay. Note that the PG indicator is invalid when the device works in pause mode, when the device switches for several pulses and then snoozes after the output voltage exceeds the set threshold voltage. If not used, the PG pin can be left floating or connected to GND.

7.3.8 Spread Spectrum Frequency Modulation

The TPS61129-Q1 uses a triangle waveform to spread the switching frequency with ±6% of normal frequency. This means, with the normal 2.2MHz switching frequency, the spread spectrum function modulates the switching frequency in the range of 2.07MHz to 2.33MHz in a triangle behavior with a 9kHz rate.

The spread spectrum function is controlled by the SSEN pin.

- When SSEN is high, spread spectrum function is enabled.
- When SSEN is low, spread spectrum function is disabled.

7.4 Device Functional Modes

7.4.1 Undervoltage Lockout

An undervoltage lockout function prevents device start-up if the supply voltage on VIN is lower than approximately 0.9V. When in operation and the battery is being discharged, the device automatically enters the shutdown mode if the voltage on VIN drops below approximately 0.7V. This undervoltage lockout function is implemented to prevent the malfunctioning of the converter.

7.5 Programming

7.5.1 Programming the Output Voltage

The output voltage of the TPS61129-Q1 can be adjusted with an external resistor divider. The typical value of the voltage at the FB pin is 500mV. The maximum recommended value for the output voltage is 5.5V. The output voltage is set by an external resistor divider (R1, R2 in the *TPS61129-Q1 Typical Schematic for Fixed 5V or Adjustable Output* figure). When the output voltage is regulated, the typical voltage at the FB pin is V_{REF}. Therefore, use Equation 1 to calculate the resistor divider.

$$R1 = \left(\frac{V_{OUT}}{V_{REF}} - 1 \right) \times R2 \quad (1)$$

where

- V_{OUT} is the regulated output voltage
- V_{REF} is the internal reference voltage at the FB pin, 0.5V typically

The current through the resistive divider must be about 100 times greater than the current into the FB pin. The typical current into the FB pin is 4nA, and the voltage across R2 is typically 500mV. For the best accuracy, keep R2 smaller than 300kΩ to make sure the current flowing through R2 is at least 100 times larger than the FB pin

ADVANCE INFORMATION

leakage current. Changing R2 toward a lower value increases the immunity against noise injection. Changing the R2 toward a higher value reduces the quiescent current for achieving highest efficiency at low load currents.

8 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

8.1 Application Information

The devices are designed to operate from an input voltage supply range between 0.9V (Vin rising UVLO is 0.9V) and 5.5V with a peak switching current limit up to 3.5A (typical). The TPS61129-Q1 employs peak current mode control with a fixed switching frequency of 2.2MHz. The device works in fixed frequency PWM operation in medium to heavy loads. There are two optional modes in light load by configuring the MODE pin: auto PFM mode and forced PWM to balance the efficiency and noise immunity in light load. The switching frequency can also be synchronized to an external clock. The TPS61129-Q1 uses the spread spectrum of the internal clock to be more EMI friendly at forced PWM mode. In addition, there is an internal soft-start time to limit the inrush current.

8.2 Typical Application

Figure 8-1 shows a typical application of TPS61129-Q1 with 2.7V to 4.2V input range and 5V, 1A output current.

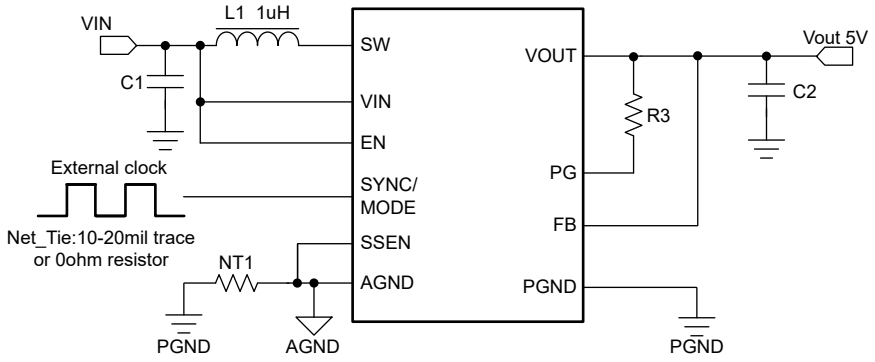


Figure 8-1. Typical Application Circuit for Adjustable Output Voltage Option, 5V Output Voltage

8.2.1 Design Requirements

The TPS61129-Q1 DC-DC converters are intended for systems powered by a single up to triple cell Alkaline, NiCd, NiMH battery with a typical terminal voltage between 0.9V and 5.5V. The devices can also be used in systems powered by one-cell Li-Ion or Li-Polymer with a typical voltage between 2.5V and 4.2V. Additionally, any other voltage source with a typical output voltage between 0.9V and 5.5V can power systems where the TPS61129-Q1 is used.

Table 8-1 lists the design parameters.

Table 8-1. Design Requirements

PARAMETERS	VALUES
Input voltage	2.7V to 4.3V
Output voltage	5V
Output current	1A
Output voltage ripple	± 100mV

ADVANCE INFORMATION

8.2.2 Detailed Design Procedure

8.2.2.1 Inductor Selection

A boost converter normally requires two main passive components for storing energy during the conversion. A boost inductor and a storage capacitor at the output are required. To select the boost inductor, TI recommends to keep the possible peak inductor current below the current limit threshold of the power switch in the chosen configuration. For example, the current limit threshold of the TPS61129-Q1 switch is 3.5A (peak current) at an output voltage of 5V. The highest peak current through the inductor and the switch depends on the output load, the input (VIN), and the output voltage (V_{OUT}). The TPS61129-Q1 is designed to work with inductor of 1µH typical value. Use Equation 2 to estimate the maximum average inductor current:

$$I_{L(DC)} = \frac{V_{OUT} \times I_{OUT}}{V_{IN} \times \eta} \quad (2)$$

where

- V_{OUT} is the output voltage of the boost converter
- I_{OUT} is the output current of the boost converter
- V_{IN} is the input voltage of the boost converter
- η is the power conversion efficiency, use 90% for most applications

Therefore, the inductor ripple current is calculated by

$$\Delta I_{L(P-P)} = \frac{V_{IN} \times D}{L \times f_{SW}} \quad (3)$$

- D is the duty cycle
- L is the inductance value of the inductor, 1µH typically
- f_{SW} is the switching frequency
- V_{IN} is the input voltage of the boost converter

Therefore, Equation 4 calculates the inductor peak current.

$$I_{L(P)} = I_{L(DC)} + \frac{\Delta I_{L(P-P)}}{2} \quad (4)$$

With this calculated value and the calculated currents, selecting a suitable inductor is possible. Normally, TI advises to work with an inductor peak-to-peak current of less than 40% of the average inductor current for maximum output current. A smaller ripple from a larger valued inductor reduces the magnetic hysteresis losses in the inductor and EMI. But in the same way, load transient response time is increased. The saturation current of the inductor must be higher than the calculated peak inductor current.

The following inductor series from different suppliers have been used with the TPS61129-Q1 converters:

Table 8-2. List of Inductors

PART NUMBER	L (µH)	DCR MAX (mΩ)	SATURATION CURRENT (A)	SIZE (L × W × H)	VENDOR
XGL4030-102MEC	1	7.2	4.8	4.0 × 4.0 × 3.0	Coilcraft
XGL4020-102MEC	1	9	3.8	4.0 × 4.0 × 2.0	Coilcraft

8.2.2.2 Input Capacitor Selection

Multilayer X5R or X7R ceramic capacitors are an excellent choices for the input decoupling of the step-up converter as multilayer X5R or X7R ceramic capacitors have extremely low ESR and are available in small footprints. Input capacitors must be located as close as possible to the device. While a 10µF input capacitor is sufficient for most applications, larger values can be used to reduce input current ripple without limitations. Take care when using only ceramic input capacitors. When a ceramic capacitor is used at the input and the power is being supplied through long wires, a load step at the output can induce ringing at the VIN pin. This ringing can couple to the output and be mistaken as loop instability or can even damage the part. In this circumstance, place additional bulk capacitance (tantalum or aluminum electrolytic capacitor) between ceramic input capacitor and the power source to reduce ringing that can occur between the inductance of the power source leads and ceramic input capacitor.

8.2.2.3 Output Capacitor Selection

The output capacitor is mainly selected to meet the requirements for output ripple and loop stability. The ripple voltage is related to capacitor capacitance and the equivalent series resistance (ESR). Assuming a ceramic capacitor with zero ESR, use Equation 5 to calculate the minimum capacitance needed for a given ripple voltage.

$$C_{OUT} = \frac{I_{OUT} \times D_{MAX}}{f_{SW} \times V_{RIPPLE}} \quad (5)$$

where

- D_{MAX} is the maximum switching duty cycle.
- V_{RIPPLE} is the peak-to-peak output ripple voltage.
- I_{OUT} is the maximum output current.
- f_{SW} is the switching frequency.

The ESR impact on the output ripple must be considered if tantalum or aluminum electrolytic capacitors are used. Use Equation 6 to calculate the output peak-to-peak ripple voltage caused by the ESR of the output capacitors.

$$V_{RIPPLE(ESR)} = I_{L(P)} \times R_{ESR} \quad (6)$$

Take care when evaluating the derating of a ceramic capacitor under DC bias voltage, aging, and AC signal. For example, the DC bias voltage can significantly reduce capacitance. A ceramic capacitor can lose more than 50% of the capacitance at the rated voltage. Therefore, always leave margin on the voltage rating to make sure there is adequate capacitance at the required output voltage. Increasing the output capacitor makes the output ripple voltage smaller in forced PWM mode.

TI recommends using the X5R or X7R ceramic output capacitor in the range of 10µF to 1000µF effective capacitance. The 22µF effective capcaitance is typically utilized in middle load conditions. The output capacitor affects the small signal control loop stability of the boost regulator. If the output capacitor is below the recommended range, the boost regulator can potentially become unstable.

ADVANCE INFORMATION

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8.2.3 Application Curves

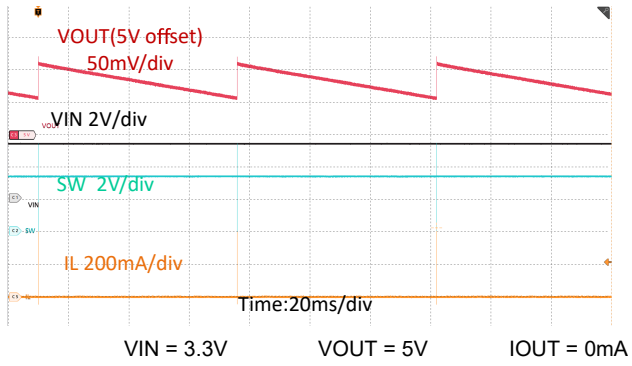

Figure 8-2. Switching Waveform at Open Load, Auto PFM Mode

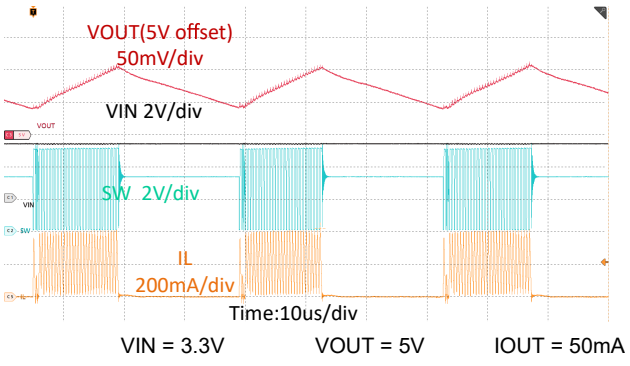

Figure 8-3. Switching Waveform at Medium Load, Auto PFM Mode

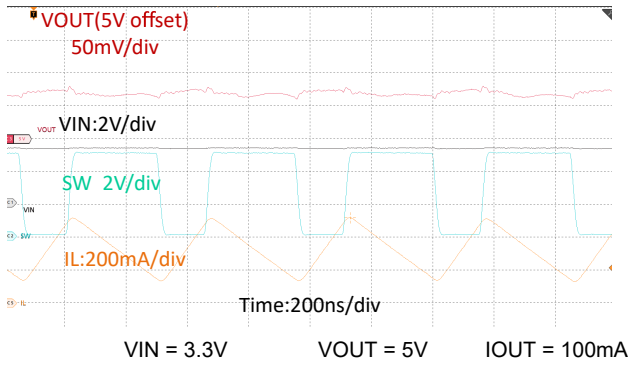

Figure 8-4. Switching Waveform at Heavy Load, Auto PFM Mode

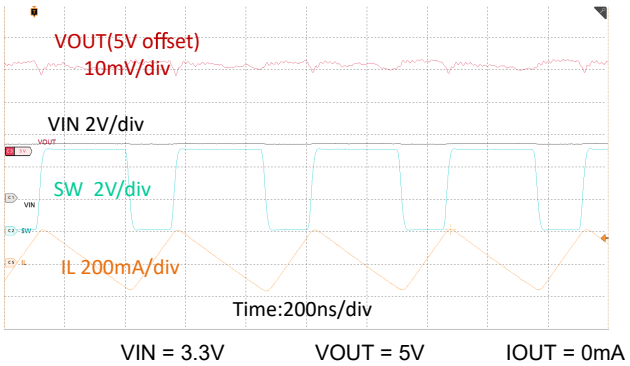

Figure 8-5. Switching Waveform at Open Load, Forced PWM Mode

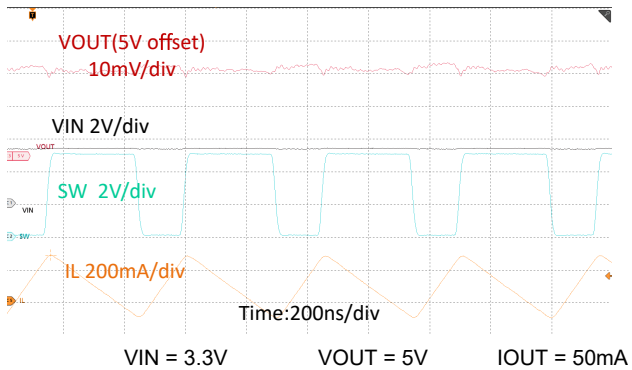

Figure 8-6. Switching Waveform at Medium Load, Forced PWM Mode

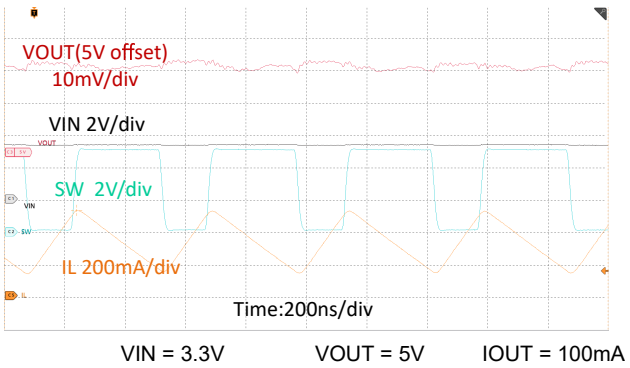

Figure 8-7. Switching Waveform at Heavy Load, Forced PWM Mode

8.2.3 Application Curves (continued)

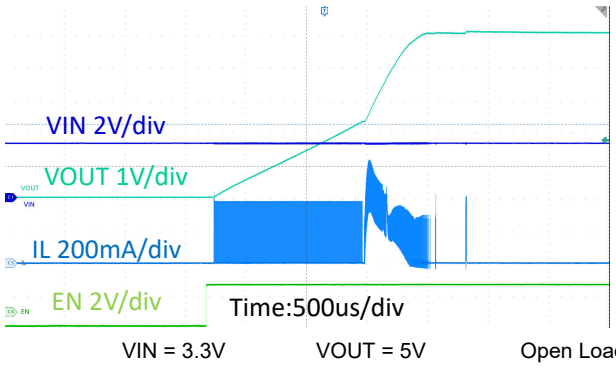

Figure 8-8. Start-Up by EN, Auto PFM Mode

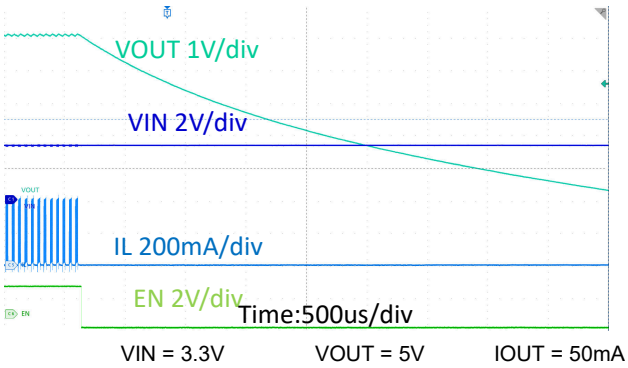

Figure 8-9. Shut-down by EN, Auto PFM Mode

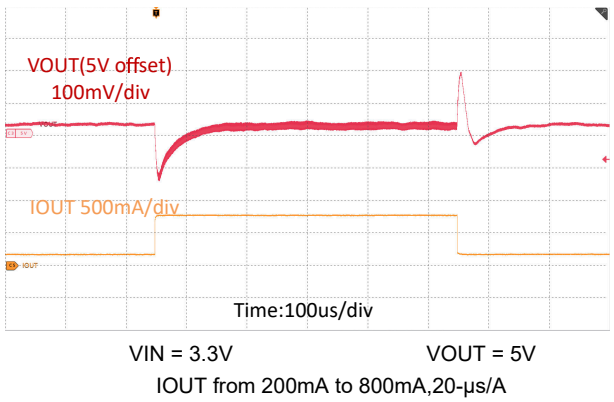

Figure 8-10. Load Transient , Auto PFM Mode

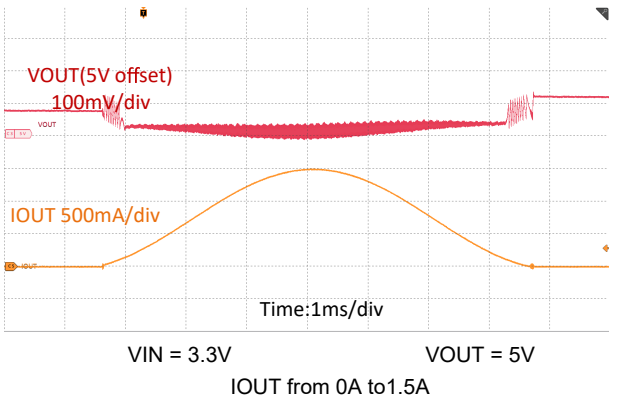

Figure 8-11. Load Sweep, Auto PFM Mode

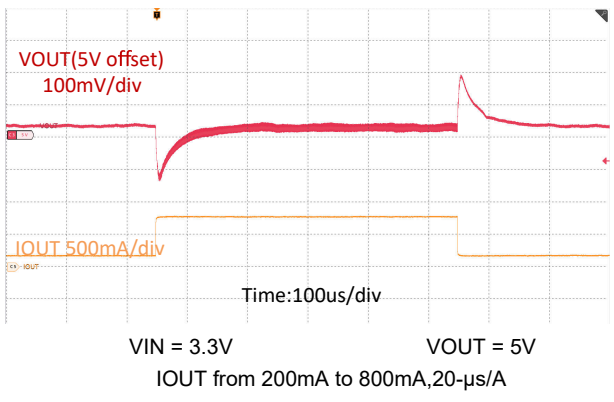

Figure 8-12. Load Transient, Forced PWM Mode

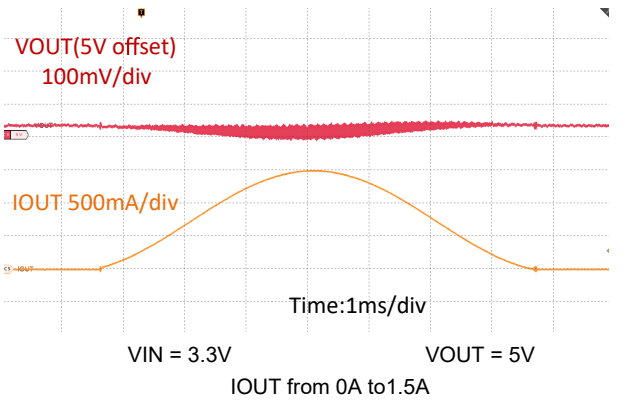

Figure 8-13. Load Sweep, Forced PWM Mode

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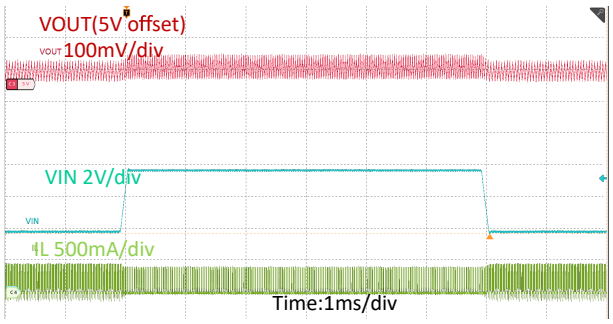
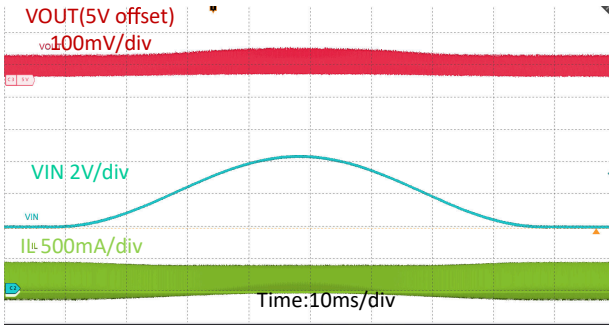
8.2.3 Application Curves (continued)



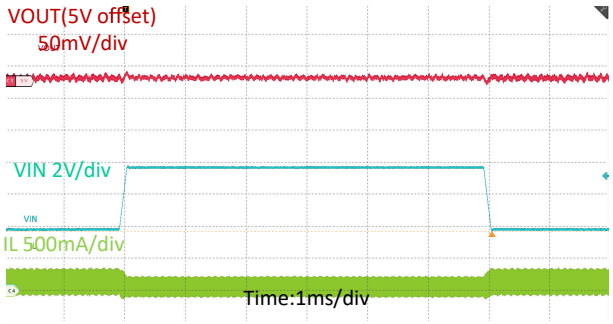
VIN from 2V to 4V, 100µs/V
VOUT = 5V IOUT = 50mA

Figure 8-14. Line Transient, Auto PFM Mode



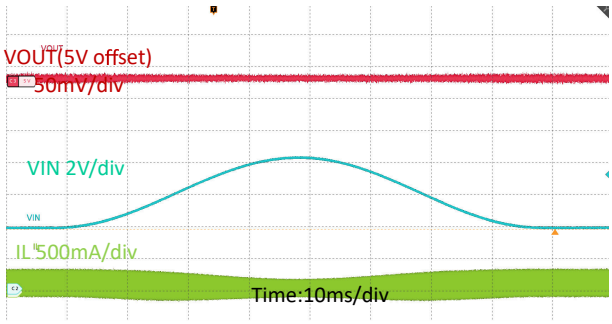
VIN from 2V to 4.3V
VOUT = 5V IOUT = 50mA

Figure 8-15. Line Sweep, Auto PFM Mode



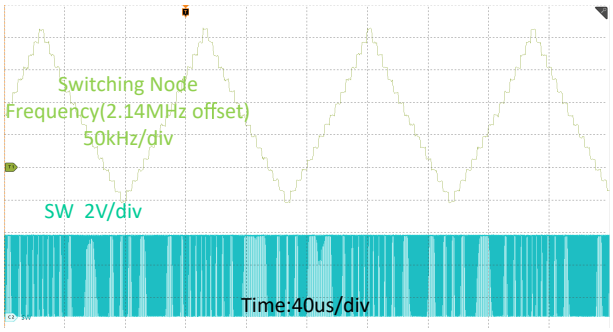
VIN from 2V to 4V, 100µs/V
VOUT = 5V IOUT = 50mA

Figure 8-16. Line Transient, Forced PWM Mode



VIN from 2V to 4.3V
VOUT = 5V IOUT = 50mA

Figure 8-17. Line Sweep, Forced PWM Mode



VIN = 3.3V
IOUT = 50mA

VOUT = 5V, Forced PWM Mode
SSEN = 3.3V

Figure 8-18. Spectrum Frequency

8.3 Power Supply Recommendations

This input supply must be well regulated with the rating of TPS61129-Q1. If the input supply is located more than a few inches from the device, additional bulk capacitance can be required in addition to the ceramic bypass capacitors. An electrolytic or tantalum capacitor with a value of 47µF is a typical choice.

8.4 Layout

8.4.1 Layout Guidelines

As for all switching power supplies, the layout is an important step in the design, especially at high peak currents and high switching frequencies. If the layout is not carefully done, the regulator can show stability problems as well as EMI problems. Therefore, use wide, short traces for the main current path and for power-ground tracks. Use a common ground node for power ground (PGND) and a different one for control ground (AGND) to minimize the effects of ground noise. Connect the ground nodes close to any IC ground pin; the net-tie is used in the example. Enable signal, SYNC/MODE signal and SSEN signal, FB signal must refer to the AGND, other power rail such as power Vin , power Vout and SW snubber must refer to PGND. The most critical current path for all boost converters is from the switching FET, through the synchronous FET, then the output capacitors, and back to ground of the switching FET. Therefore, both output capacitors and the traces must be placed on the same board layer as close as possible between the IC VOUT and PGND pin. Especially at output voltages above 4.5V, adding an RC snubber from the SW pin to PGND pin can assist in further reducing the parasitic inductance impact of this critical current path. See also *Minimizing Ringing at the Switch Node of a Boost Converter* application note for details of implementing a snubber. In addition, the input capacitor must be placed as close as possible between the IC VIN and PGND pin. Placing the inductor close to the SW pin with a wide but short trace helps to improve efficiency and minimize EMI. To lay out the control ground, TI recommends to use short traces as well, separated from the power ground traces. This action avoids ground shift problems that can occur due to superimposition of power ground current and control ground current. The recommended layout is shown in *Layout Example*.

8.4.2 Layout Example

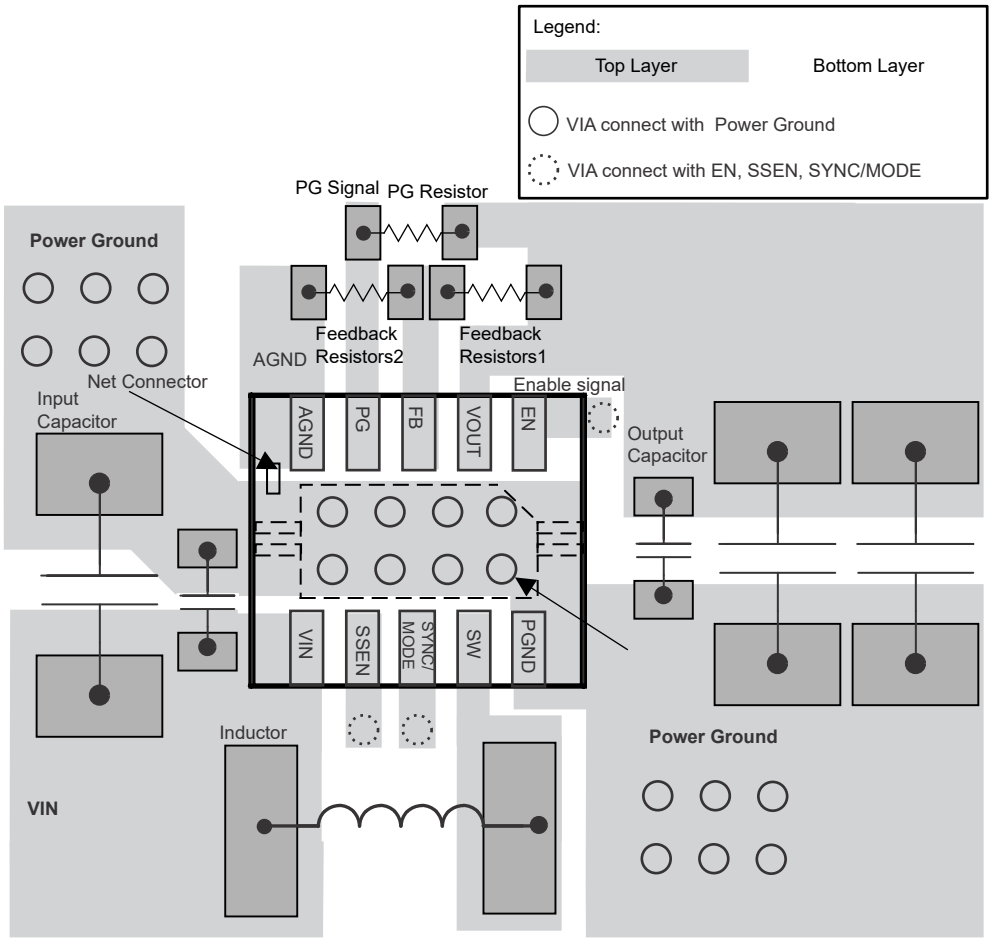


Figure 8-19. PCB Layout Recommendation

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9 Device and Documentation Support

9.1 Device Support

9.1.1 Third-Party Products Disclaimer

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9.2 Documentation Support

9.2.1 Related Documentation

For related documentation, see the following:

Texas Instruments, *Minimizing Ringing at the Switch Node of a Boost Converter* application note

9.3 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

9.4 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

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9.5 Trademarks

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9.6 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

9.7 Glossary

TI Glossary	This glossary lists and explains terms, acronyms, and definitions.

10 Revision History

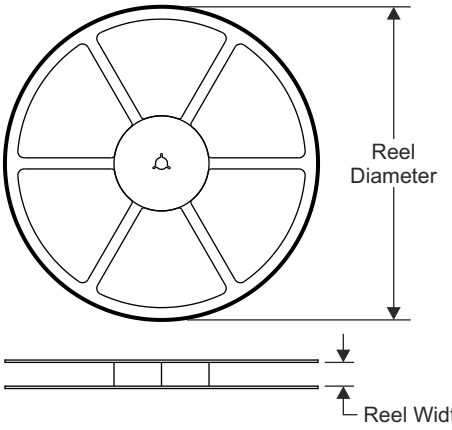
DATE	REVISION	NOTES
May 2026	*	Initial Release

11 Mechanical, Packaging, and Orderable Information

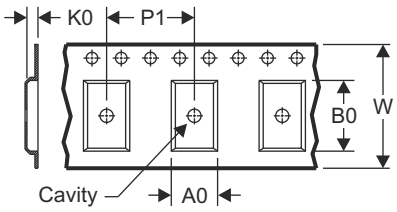
The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

11.1 Tape and Reel Information

REEL DIMENSIONS

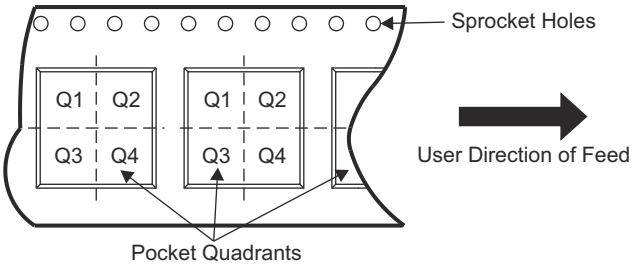


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS61129QDRCRQ1	VSON	DRC	11	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2

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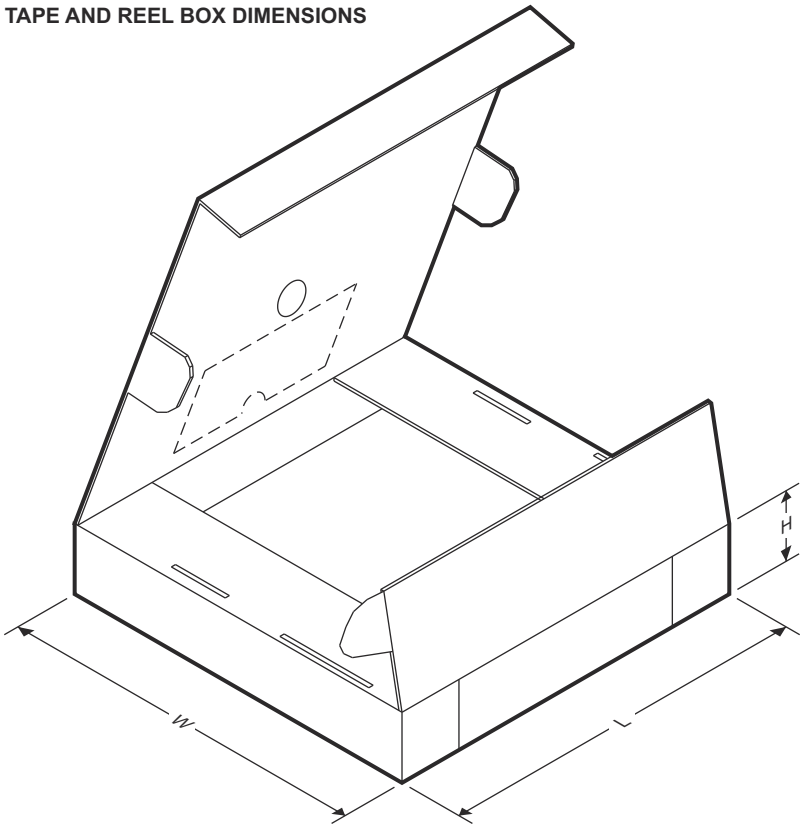
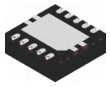
ADVANCE INFORMATION

TAPE AND REEL BOX DIMENSIONS



Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS61129QDRCRQ1	VSON	DRC	11	3000	346	346	33

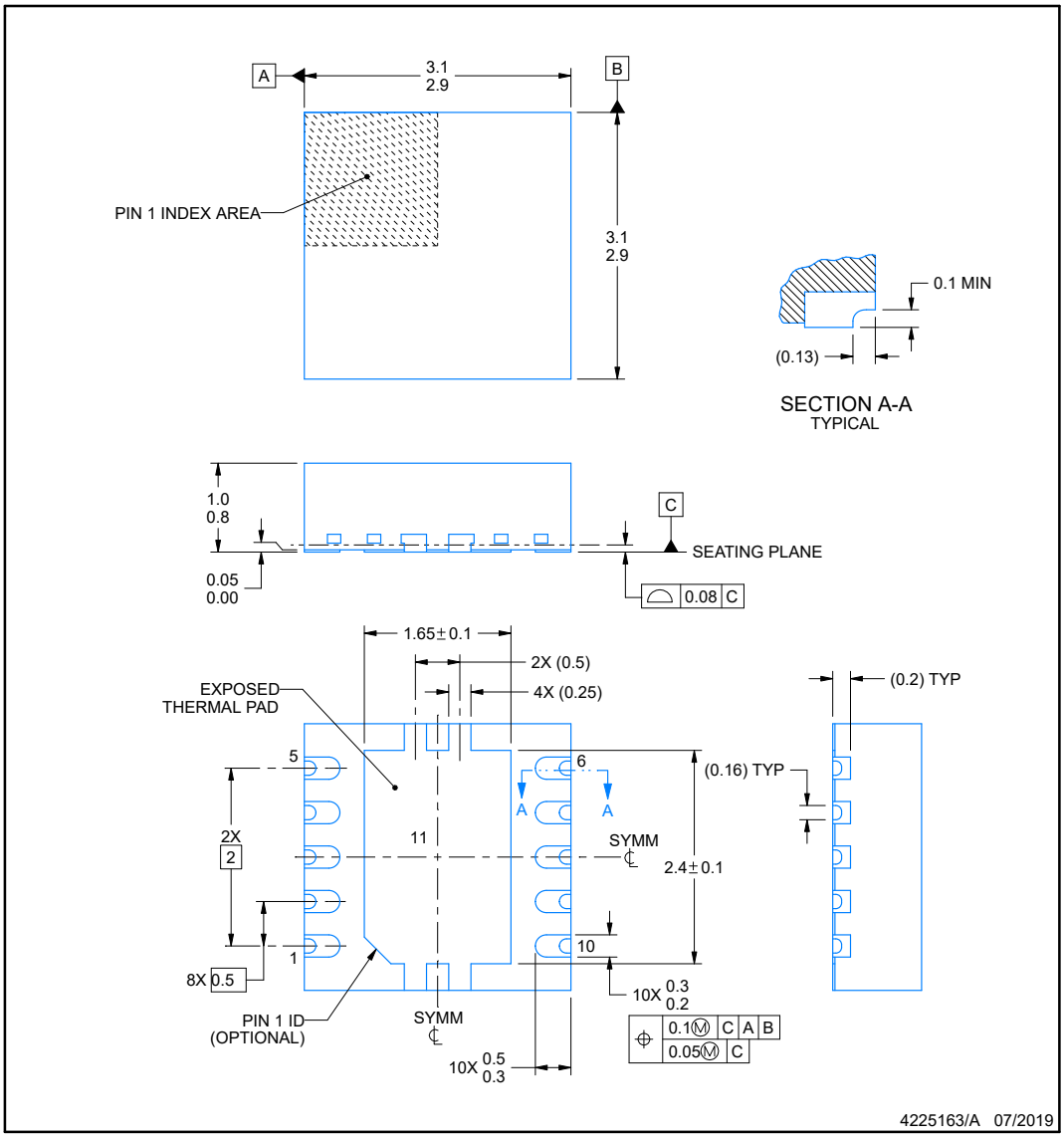


PACKAGE OUTLINE

DRC0010U

VSON - 1 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for optimal thermal and mechanical performance.

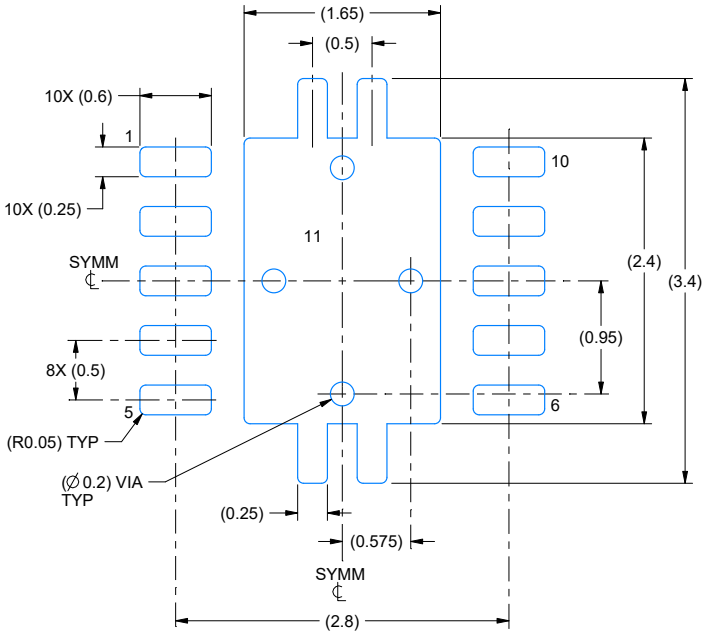
ADVANCE INFORMATION

EXAMPLE BOARD LAYOUT

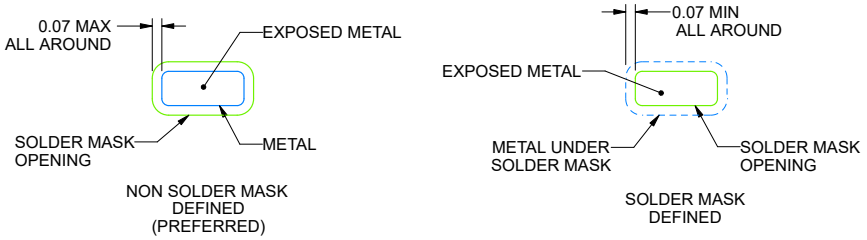
DRC0010U

VSON - 1 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:20X



SOLDER MASK DETAILS

4225163/A 07/2019

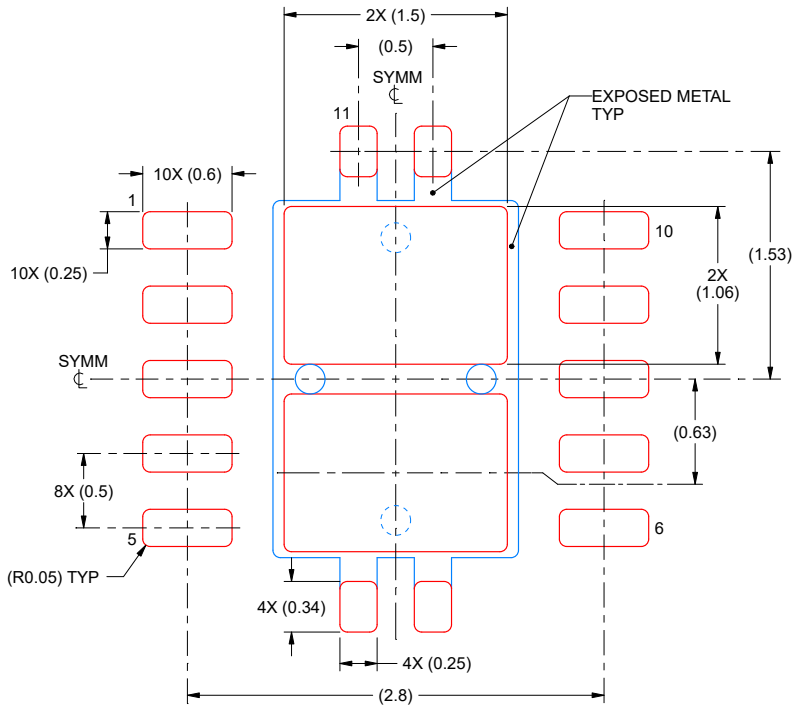
NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.

EXAMPLE STENCIL DESIGN

DRC0010U — **VSON - 1 mm max height**

PLASTIC SMALL OUTLINE - NO LEAD



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD 11:
80% PRINTED SOLDER COVERAGE BY AREA
SCALE:25X

4225163/A 07/2019

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

ADVANCE INFORMATION

GENERIC PACKAGE VIEW

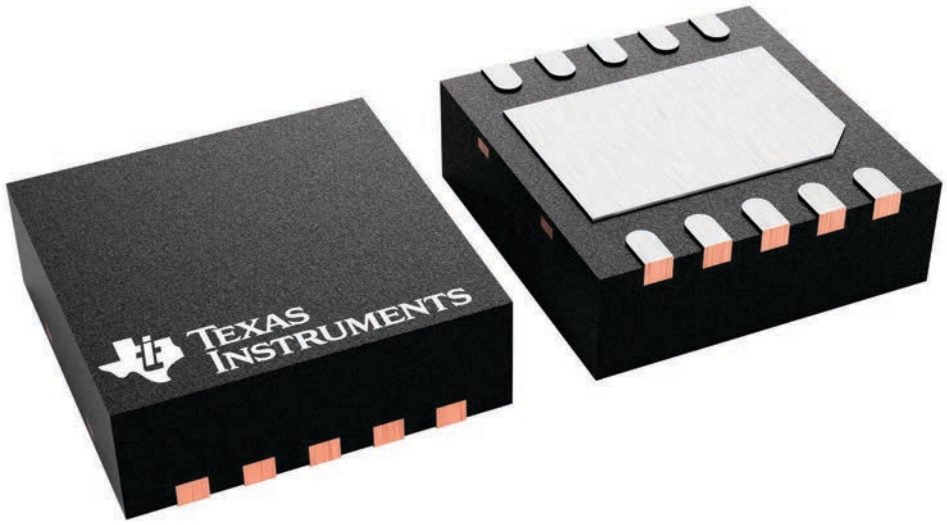
DRC 10

VSON - 1 mm max height

3 x 3, 0.5 mm pitch

PLASTIC SMALL OUTLINE - NO LEAD

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



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