TPS63901 1.8-V to 5.5-V, 75-nA I_Q Buck-Boost Converter with Input Current Limit and DVS in a WCSP Package

1 Features

- 1.8-V to 5.5-V input voltage range
- 1.8-V to 5-V output voltage range (100-mV steps)
  - Programmable with external resistors
  - SEL pin to toggle between two output voltage presets
- > 400-mA output current for $V_I \geq 2.0$ V, $V_O = 3.3$ V
  - Stackable: parallel multiple devices for higher output current
- > 90% efficiency at 10-µA load current
  - 75-nA quiescent current
  - 60-nA shutdown current
- Single-mode operation
  - Eliminates mode transitions between buck, buck-boost and boost operation
  - Low output ripple
  - Excellent transient performance
- Robust operation features
  - Integrated soft start
  - Programmable input current limit with eight settings (1 mA to 100 mA and unlimited)
  - Output short-circuit and overtemperature protection
- Tiny solution size
  - Small 2.2-µH inductor, single 22-µF output capacitor
  - 12-ball, 1.5-mm × 1.15-mm, 0.35-mm pitch WCSP package

2 Applications

- Smart watch
- Smart tracker
- Wearable electronics
- Medical sensor patches and patient monitors
- Smart meters and sensor nodes
- Electronic smart locks
- Industrial IoT (smart sensors) and NB-IoT

3 Description

The TPS63901 device is a high-efficiency synchronous buck-boost converter with an extremely low quiescent current (75 nA typical). The device has 32 user-programmable output voltage settings from 1.8 V to 5 V.

A dynamic voltage-scaling feature lets applications switch between two output voltages during operation; for example, to save power by using a lower system supply voltage during standby operation.

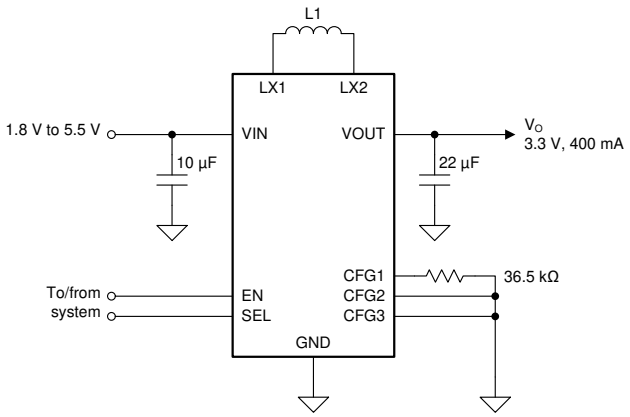
With its wide supply voltage range and programmable input current limit (1 mA to 100 mA and unlimited), the device is ideal for use with a wide range of primary like 3S Alkaline, 1S Li-MnO_2 or 1S Li-$SOCl_2$, and secondary battery types.

The high-output current capability supports commonly-used RF standards like sub-1-GHz, BLE, LoRa, wM-Bus, and NB-IoT.

Device Information

Part Number(1)	Package	Body Size (NOM)
TPS63901	WCSP (12)	1.50 mm × 1.15 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.



Simplified Schematic

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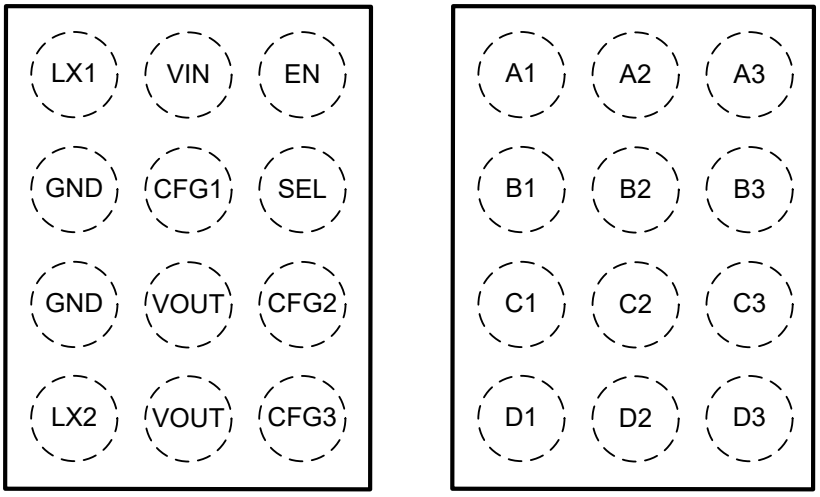


Figure 4-1. 12-Ball WCSP Package (Top View)

Table 4-1. Pin Functions

Pin		Type	Description
Name	No.		
LX1	A1	—	Switching node of the buck stage
VIN	A2	—	Supply voltage
EN	A3	I	Device enable. A high level applied to this pin enables the device and a low level disables it. It must not be left open.
GND	B1,C1	—	Ground
CFG1	B2	I	Configuration pin 1. Connect a resistor between this pin and ground to set $V_{O(2)}$ and input current limit. Must not be left open.
SEL	B3	I	Output voltage select. Selects $V_{O(2)}$ when a high level is applied to this pin. Selects $V_{O(1)}$ when a low level is applied to this pin. It must not be left open.
VOUT	C2,D2	—	Output voltage. The C2 and D2 pins must be connected together.
CFG2	C3	I	Configuration pin 2. Connect a resistor between this pin and ground to set $V_{O(2)}$ and input current limit. Must not be left open.
LX2	D1	—	Switching node of the boost stage
CFG3	D3	I	Configuration pin 3. Connect a resistor between this pin and ground to set $V_{O(1)}$. Must not be left open.

5 Specifications

5.1 Absolute Maximum Ratings

over operating junction temperature range (unless otherwise noted) (1)

		MIN	MAX	UNIT
V_I	Input voltage (VIN, LX1, LX2, VOUT, EN, CFG1, CFG2, CFG3, SEL) (2)	–0.3	5.9	V
T_J	Operating junction temperature	–40	150	°C
T_{stg}	Storage temperature	–65	150	°C

(1) Operation outside the *Absolute Maximum Ratings* may cause permanent device damage. *Absolute Maximum Ratings* do not imply functional operation of the device at these or any other conditions beyond those listed under *Recommended Operating Conditions*. If used outside the *Recommended Operating Conditions* but within the *Absolute Maximum Ratings*, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.
(2) All voltage values are with respect to network ground terminal, unless otherwise noted.

5.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±2000	V
		Charged device model (CDM), per ANSI/ESDA/JEDEC JS-002(2)	±750	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

5.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

			MIN	NOM	MAX	UNIT
V_I	Supply voltage		1.8		5.5	V
V_O	Output voltage		1.8		5.0	V
C_I	Input capacitance (V_I = 2.5 V to 5 V, V_O = 3.3 V, I_O = 0.4 A)(1)		5			µF
C_O	Output capacitance (V_I = 2.5 V to 5 V, V_O = 3.3 V, I_O = 0.4 A)(1)		10			µF
$C_{(CFG)}$	Capacitance (CFG1, CFG2, CFG3)				10	pF
L	Inductance			2.2		µH
I_{SAT}	Inductor saturation current rating	Unlimited current setting	2			A
		≤ 100-mA current settings	1			
T_A	Operating ambient temperature		–40		85	°C
T_J	Operating junction temperature		–40		125	°C

(1) Effective capacitance after DC bias effects have been considered.

5.4 Thermal Information

THERMAL METRIC(1)		YCJ (WCSP) 12 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	102.4	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	0.6	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	26.1	°C/W
ψ_{JT}	Junction-to-top characterization parameter	0.3	°C/W
ψ_{JB}	Junction-to-board characterization parameter	26.1	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

5.5 Electrical Characteristics

T_J = –40°C to 125°C, V_I = 3.0 V, V_O = 2.5 V . Typical values are at T_J = 25°C (unless otherwise noted).

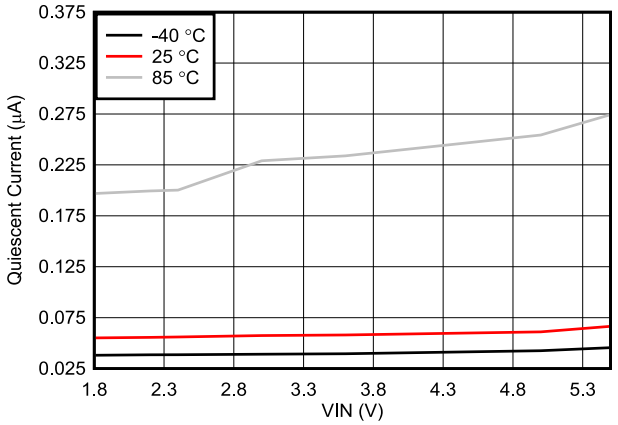
PARAMETER			TEST CONDITIONS		MIN	TYP	MAX	UNIT
SUPPLY								
I_Q	Quiescent current into VIN		V(EN) = 3 V, no load, not switching, "unlimited" current setting; T_J = –40°C to 85°C			0.075	1	µA
I_{SD}	Shutdown current into VIN		V(EN) = 0 V ; T_J = –40°C to 85°C			60		nA
$V_{IT+(UVLO)}$	Positive-going UVLO threshold voltage				1.73	1.75	1.77	V
$V_{hys(UVLO)}$	UVLO threshold voltage hysteresis				90	100	110	mV
$V_{IT+(POR)}$	Positive-going POR threshold voltage				1.37		1.74	V
I/O SIGNALS								
V_{IH}	High-level input voltage (EN, SEL)						1.2	V
V_{IL}	Low-level input voltage (EN, SEL)				0.4			V
	Input current (EN, SEL)		$V_{(EN)}$, $V_{(SEL)}$ = 1.8 V or 0 V			±1	±10	nA
POWER SWITCH								
$r_{DS(on)}$	On-state resistance	Q1	V_I = 3 V, V_O = 5 V, test current = 1 A			140		mΩ
		Q2	V_I = 3 V, V_O = 3 V, test current = 1 A			95		
		Q3	V_I = 3 V, V_O = 3 V, test current = 1 A			95		
		Q4	V_I = 5 V, V_O = 3 V, test current = 1 A			140		
CURRENT LIMIT								
	Peak current limit during start-up (Q1)		V_I = 3.6 V, unlimited current limit setting		0.35		0.83	A
	Peak current limit (Q1)		V_I = 1.8 V, V_O = 3.6 V, unlimited current limit setting		1.33	1.45	1.6	A
			V_I = 3.6 V, V_O = 3.3 V, 100-mA current limit setting		0.15	0.29	0.51	
	Average input current limit		T_J = –40°C to 85°C	1-mA setting		1		mA
				2.5-mA setting		2.5		
				5-mA setting		5		
				10-mA settting		10		
				25-mA setting		25		
				50-mA setting		50		
				100-mA setting		100		
OUTPUT								
	Output voltage DC accuracy		I_O = 1 mA, $C_{O(eff)}$ = 10 µF, $L_{(eff)}$ = 2.2 µH				±1.5%	
CONTROL								
	Internal reference resistor					33		kΩ

5.5 Electrical Characteristics (continued)

T_J = –40°C to 125°C, V_I = 3.0 V, V_O = 2.5 V . Typical values are at T_J = 25°C (unless otherwise noted).

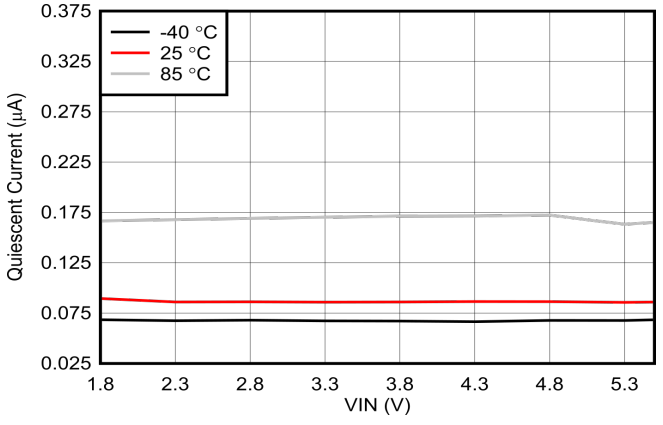
PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
R_{CFG}	R2D setting #0			0	0.1	kΩ
	R2D setting #1		–3%	0.511	+3%	
	R2D setting #2		–3%	1.15	+3%	
	R2D setting #3		–3%	1.87	+3%	
	R2D setting #4		–3%	2.74	+3%	
	R2D setting #5		–3%	3.83	+3%	
	R2D setting #6		–3%	5.11	+3%	
	R2D setting #7		–3%	6.49	+3%	
	R2D setting #8		–3%	8.25	+3%	
	R2D setting #9		–3%	10.5	+3%	
	R2D setting #10		–3%	13.3	+3%	
	R2D setting #11		–3%	16.2	+3%	
	R2D setting #12		–3%	20.5	+3%	
	R2D setting #13		–3%	24.9	+3%	
	R2D setting #14		–3%	30.1	+3%	
	R2D setting #15		–3%	36.5	+3%	
PROTECTION FEATURES						
	Thermal shutdown threshold temperature		140	150	160	°C
	Thermal shutdown hysteresis		15	20	25	°C
TIMING PARAMETERS						
$t_{d(POR)}$	POR signal delay after reaching POR threshold			3.8		ms
$t_{d(EN)}$	Delay between a rising edge on the EN pin and the start of the output voltage ramp	Supply voltage stable before EN pin goes high			1.5	ms
$t_{w(SS)}$	Soft-start step duration	V_O > 1.8 V	100	125	150	µs
$t_{d(SEL)}$	Delay between a change in the state of the SEL pin and the first step change in the output voltage			30	40	µs
$t_{w(DVS)}$	Dynamic voltage scaling step duration		100	125	150	µs
$t_{d(RESTART)}$	Restart delay after protection			10	11	ms

5.6 Typical Characteristics



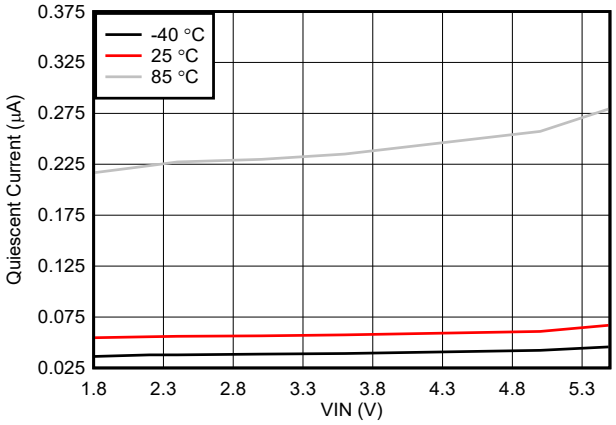
V_O = 5.1 V EN = HIGH I_O = 0 mA, device not switching

Figure 5-1. Quiescent Current into VIN vs Input Voltage



V_O = 5.1 V EN = HIGH I_O = 0 mA, device not switching

Figure 5-2. Quiescent Current into VOUT vs Input Voltage



V_O = 5.1 V EN = LOW

Figure 5-3. Shutdown Current vs Input Voltage

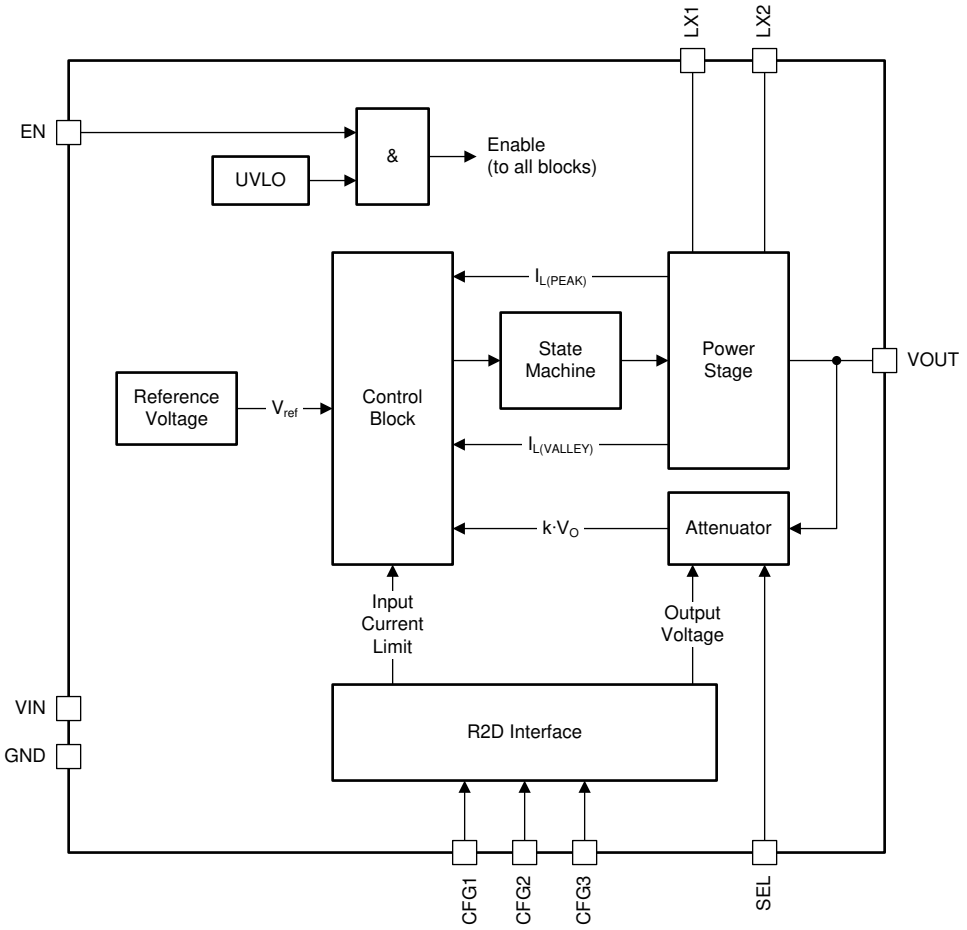
6 Detailed Description

6.1 Overview

The TPS63901 device is a four-switch synchronous buck-boost converter with a maximum output current of 400 mA. The device has a single-mode operation that allows the device to regulate the output voltage to a level above, below, or equal to the input voltage without displaying the mode-switching transients and unpredictable inductor current ripple from which many other buck-boost devices suffer.

The switching frequency of the TPS63901 device varies with the operating conditions: it is lowest when I_O is low and increases smoothly as I_O increases.

6.2 Functional Block Diagram



6.3 Feature Description

6.3.1 Trapezoidal Current Control

Figure 6-1 shows a simplified block diagram of the power stage of the device. Inductor current is sensed in series with Q1 (the peak current) and Q4 (the valley current).

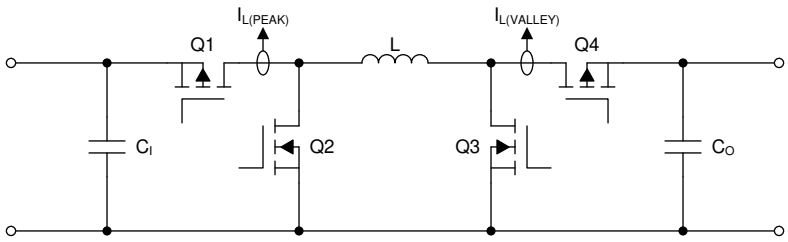


Figure 6-1. Power Stage Simplified Block Diagram

The device uses a trapezoidal inductor current to regulate its output under all operating conditions. Thus, the device only has one operating mode and does not display any of the mode-change transients or unpredictable switching displayed by many other buck-boost devices.

There are four phases of operation:

- Phase A – Q1 and Q3 are on and Q2 and Q4 are off.
- Phase B – Q1 and Q4 are on and Q2 and Q3 are off.
- Phase C – Q2 and Q4 are on and Q1 and Q3 are off.
- Phase D – Q2 and Q3 are on and Q1 and Q4 are off.

Figure 6-2 shows the inductor current waveform when $V_I > V_O$, Figure 6-3 shows the current waveform when $V_I = V_O$, and Figure 6-4 shows the current waveform when $V_I < V_O$.

Figure 6-2 through Figure 6-4 show the typical waveforms during continuous conduction mode (CCM) switching for three operating conditions. During discontinuous conduction mode (DCM), the typical inductor current waveforms look similar to CCM with Phase D at 0-A inductor current. In deep boost mode, where $V_I << V_O$, Phase C length gradually decreases to zero until the switching waveform becomes triangular.

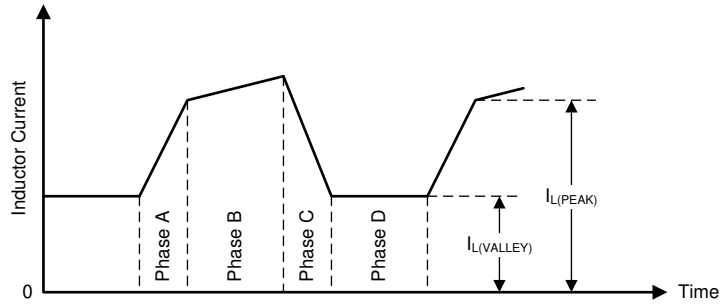


Figure 6-2. Inductor Current Waveform when $V_I > V_O$ (CCM)

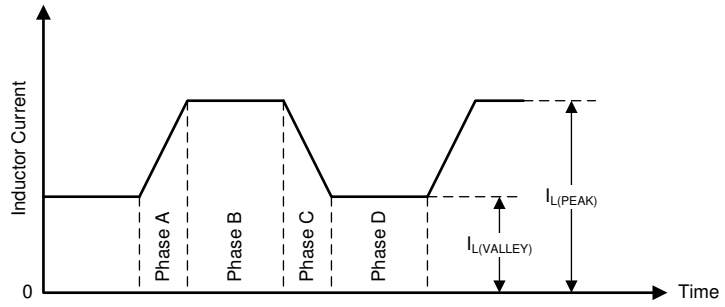


Figure 6-3. Inductor Current Waveform when $V_I = V_O$ (CCM)

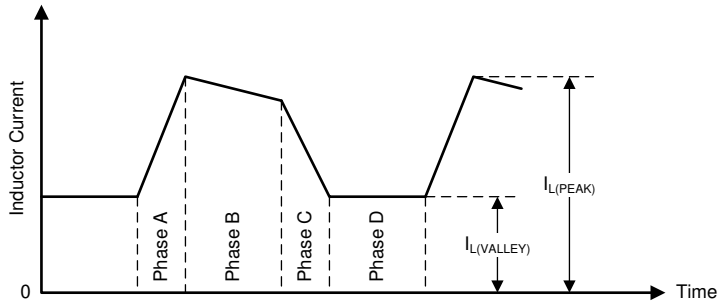


Figure 6-4. Inductor Current Waveform when $V_I < V_O$ (CCM)

The ideal relationship between V_I and V_O (that is, assuming no losses) is:

$$V_O = V_I \left(\frac{t_{w(A)} + t_{w(B)}}{t_{w(B)} + t_{w(C)}} \right) \quad (1)$$

where

- V_I is the input voltage.
- V_O is the output voltage.
- $t_{w(A)}$ is the duration of phase A.
- $t_{w(B)}$ is the duration of phase B.
- $t_{w(C)}$ is the duration of phase C.

By varying relative duration of each phase, the device can regulate V_O to be less than, equal to, or greater than V_I.

6.3.2 Device Enable and Disable

The device turns on when *all* of the following conditions are true:

- The supply voltage is greater than the positive-going undervoltage lockout (UVLO) threshold.
- The EN pin is high.

The device turns off when *at least one* of the following conditions is true:

- The supply voltage is less than the negative-going UVLO threshold.
- The EN pin is low.

Figure 6-13 shows a complete state diagram.

After the device turns on, the internal reference system starts, then the trimming information and the CFG pins are read out. The device ignores any further changes to the CFG pins during device operation.

Figure 6-5 shows the internal start-up sequence.

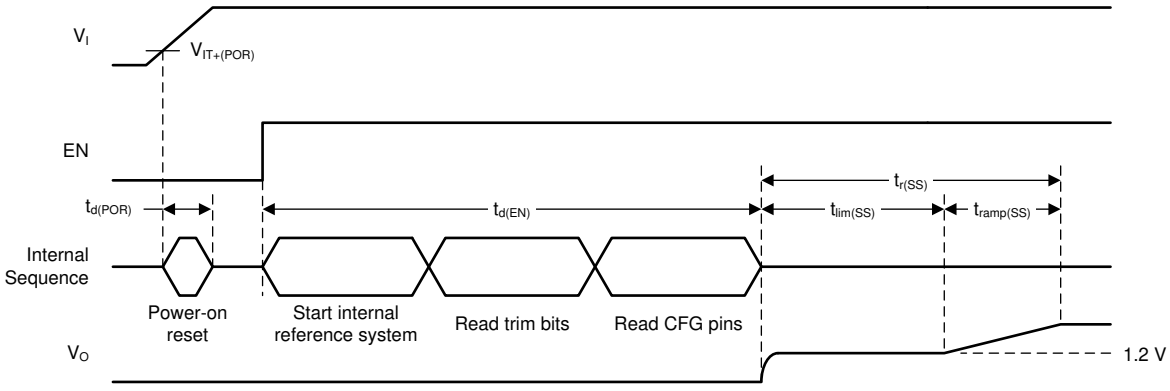


Figure 6-5. Internal Start-Up Sequence

6.3.3 Soft Start

The device has a soft-start feature that starts the device typically with 500-mA peak current limit until V_O = 1.8 V and 500 µs elapsed when the input current limit is set to unlimited (see Section 6.3.4). Afterward, the output voltage ramps in a series of discrete steps (see Figure 6-6).

- When $V_O \leq 1.8$ V, peak current is limited to 500 mA typical for 500 µs.
- When $V_O > 1.8$ V, each step is 100 mV high and has a duration of 125 µs.

The total soft-start ramp-up time can be calculated with Equation 2.

$$t_{r(SS)} = V_O \times 1.25 \left[ms/V\right] - 1.75[ms] \quad (2)$$

where

- $t_{r(SS)}$ is the rise time of the output voltage in milliseconds.
- V_O is the output voltage in volts.

Figure 6-6 shows a typical start-up case.

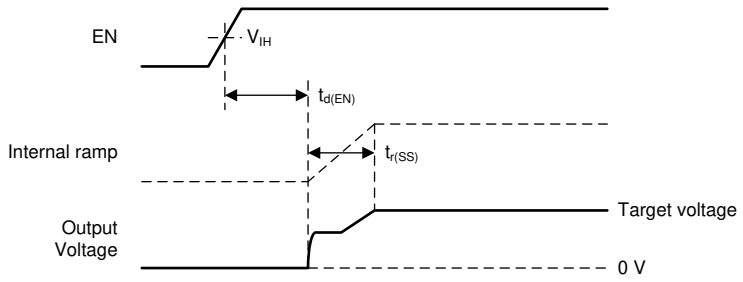


Figure 6-6. Start-Up Behavior

Figure 6-7 illustrates the start-up step size behavior.

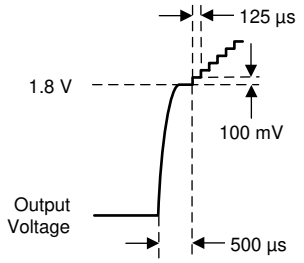


Figure 6-7. Typical Soft-Start Ramp Step Size

Table 6-1 shows the typical start-up time for a number of standard output voltages.

Table 6-1. Typical Start-Up Times

Output Voltage	Soft-Start Ramp-Up Time ($t_{r(SS)}$)	Start-Up Time ($t_{d(EN)}$ + $t_{r(SS)}$)
1.8 V	0.5 ms	2 ms
2.5 V	1.375 ms	2.875 ms
3.3 V	2.375 ms	3.875 ms
5 V	4.5 ms	6 ms

If the output is prebiased – that is, the initial output voltage is not zero – the start-up behavior is as follows:

- If the prebias voltage is *lower* than the target voltage, the device does not start switching until the ramping output voltage is greater than the prebias voltage (see Figure 6-8).
- If the prebias voltage is *higher* than the target voltage, the device does not start to switch until the output voltage has decreased to the target voltage (see Figure 6-9). The device cannot actively discharge the output to the target voltage and relies on the load current to discharge the output capacitor and decrease the output voltage to the target value.

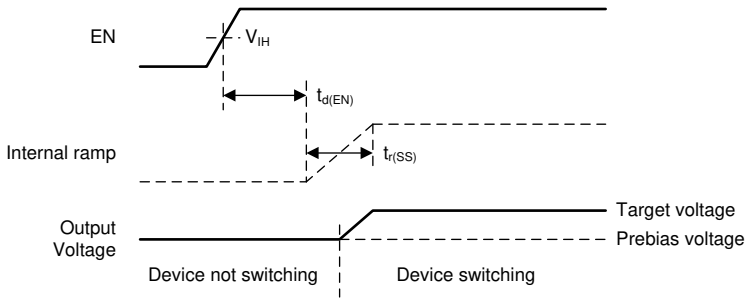


Figure 6-8. Start-Up Behavior into Prebiased (Low) Output

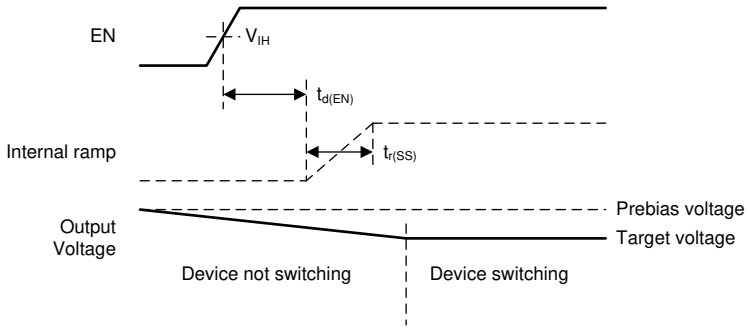


Figure 6-9. Start-Up Behavior into Prebiased (High) Output

6.3.4 Input Current Limit

The device can limit the current drawn from its supply, so that it can be used with batteries that do not support high peak currents. The input current limit is active during normal operation and at start-up to avoid high inrush current. The device has eight current limit settings:

- 1 mA
- 2.5 mA
- 5 mA
- 10 mA
- 25 mA
- 50 mA
- 100 mA
- Unlimited

CFG1 and CFG2 pins select which setting is active (see Section 6.3.6).

6.3.5 Dynamic Voltage Scaling

The device has a dynamic voltage scaling function to switch between the two output voltage settings. When the SEL pin changes state, the output voltage ramps to the new value in 100-mV steps. The duration of each step is 125 µs (see Figure 6-10).

The device does not actively discharge the output capacitor when the output voltage ramps to a lower level. This leads to a longer output voltage settling time when light load is applied (see Figure 6-11). The settling time can be calculated with Equation 3.

$$t_{settle} = C_O \times \frac{V_{O(HIGH)} - V_{O(LOW)}}{I_O} \quad (3)$$

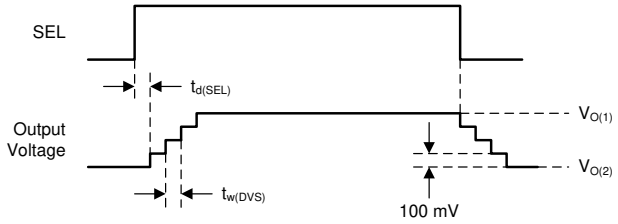


Figure 6-10. Dynamic Voltage Scaling with High Load

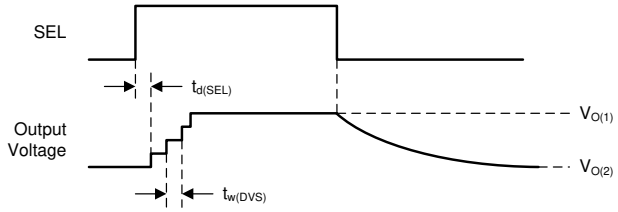


Figure 6-11. Dynamic Voltage Scaling with Light Load

6.3.6 Device Configuration (Resistor-to-Digital Interface)

The device has three configuration pins (CFG1, CFG2, and CFG3) that control its operation. When the device starts up, a resistor-to-digital (R2D) interface reads the values of the configuration resistors on the CFG pins and transfers the setting to an internal configuration register (see Figure 6-12).

- CFG1 and CFG2 set $V_{O(2)}$ level and the input current limit.
- CFG3 sets $V_{O(1)}$ level.

To reduce power consumption, the device reads the value of the resistors connected to the configuration pins during start-up and then disables these pins. Once the device has started to operate, changes to the configuration pins have no effect.

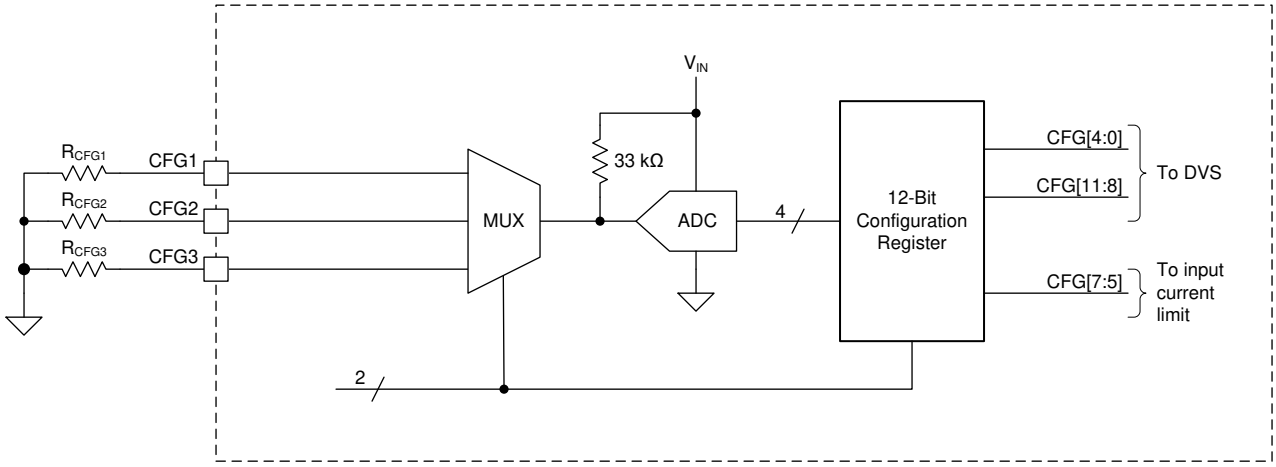


Figure 6-12. Resistor-to-Digital Interface Block Diagram

Table 6-2 summarizes the resistor values needed to configure the device for different input current limit and output voltage (SEL = high) settings. For correct operation, use resistors with a tolerance of ±1% or better and a temperature coefficient of ±200 ppm or better.

Note

For correct operation, TI recommends that the total RMS error of the configuration resistors – including initial tolerance, temperature drift, and aging – is less than ±3%.

Table 6-2. Input Current Limit and Output Voltage (SEL = High) Settings

Output Voltage – $V_{O(2)}$ (SEL = HIGH)		Input Current Limit							
		UNLIMITED	100 mA	50 mA	25 mA	10 mA	5 mA	2.5 mA	1 mA
1.8 V	R_{CFG1}	0 Ω							
	R_{CFG2}	0 Ω	511 Ω	1.15 kΩ	1.87 kΩ	2.74 kΩ	3.83 kΩ	5.11 kΩ	6.49 kΩ
1.9 V	R_{CFG1}	511 Ω							
	R_{CFG2}	0 Ω	511 Ω	1.15 kΩ	1.87 kΩ	2.74 kΩ	3.83 kΩ	5.11 kΩ	6.49 kΩ

Table 6-2. Input Current Limit and Output Voltage (SEL = High) Settings (continued)

Output Voltage – $V_{O(2)}$ (SEL = HIGH)		Input Current Limit							
		UNLIMITED	100 mA	50 mA	25 mA	10 mA	5 mA	2.5 mA	1 mA
2.0 V	R_{CFG1}	1.15 kΩ							
	R_{CFG2}	0 Ω	511 Ω	1.15 kΩ	1.87 kΩ	2.74 kΩ	3.83 kΩ	5.11 kΩ	6.49 kΩ
2.1 V	R_{CFG1}	1.87 kΩ							
	R_{CFG2}	0 Ω	511 Ω	1.15 kΩ	1.87 kΩ	2.74 kΩ	3.83 kΩ	5.11 kΩ	6.49 kΩ
2.2 V	R_{CFG1}	2.74 kΩ							
	R_{CFG2}	0 Ω	511 Ω	1.15 kΩ	1.87 kΩ	2.74 kΩ	3.83 kΩ	5.11 kΩ	6.49 kΩ
2.3 V	R_{CFG1}	3.83 kΩ							
	R_{CFG2}	0 Ω	511 Ω	1.15 kΩ	1.87 kΩ	2.74 kΩ	3.83 kΩ	5.11 kΩ	6.49 kΩ
2.4 V	R_{CFG1}	5.11 kΩ							
	R_{CFG2}	0 Ω	511 Ω	1.15 kΩ	1.87 kΩ	2.74 kΩ	3.83 kΩ	5.11 kΩ	6.49 kΩ
2.5 V	R_{CFG1}	6.49 kΩ							
	R_{CFG2}	0 Ω	511 Ω	1.15 kΩ	1.87 kΩ	2.74 kΩ	3.83 kΩ	5.11 kΩ	6.49 kΩ
2.6 V	R_{CFG1}	8.25 kΩ							
	R_{CFG2}	0 Ω	511 Ω	1.15 kΩ	1.87 kΩ	2.74 kΩ	3.83 kΩ	5.11 kΩ	6.49 kΩ
2.7 V	R_{CFG1}	10.5 kΩ							
	R_{CFG2}	0 Ω	511 Ω	1.15 kΩ	1.87 kΩ	2.74 kΩ	3.83 kΩ	5.11 kΩ	6.49 kΩ
2.8 V	R_{CFG1}	13.3 kΩ							
	R_{CFG2}	0 Ω	511 Ω	1.15 kΩ	1.87 kΩ	2.74 kΩ	3.83 kΩ	5.11 kΩ	6.49 kΩ
2.9 V	R_{CFG1}	16.2 kΩ							
	R_{CFG2}	0 Ω	511 Ω	1.15 kΩ	1.87 kΩ	2.74 kΩ	3.83 kΩ	5.11 kΩ	6.49 kΩ
3.0 V	R_{CFG1}	20.5 kΩ							
	R_{CFG2}	0 Ω	511 Ω	1.15 kΩ	1.87 kΩ	2.74 kΩ	3.83 kΩ	5.11 kΩ	6.49 kΩ
3.1 V	R_{CFG1}	24.9 kΩ							
	R_{CFG2}	0 Ω	511 Ω	1.15 kΩ	1.87 kΩ	2.74 kΩ	3.83 kΩ	5.11 kΩ	6.49 kΩ
3.2 V	R_{CFG1}	30.1 kΩ							
	R_{CFG2}	0 Ω	511 Ω	1.15 kΩ	1.87 kΩ	2.74 kΩ	3.83 kΩ	5.11 kΩ	6.49 kΩ
3.3 V	R_{CFG1}	36.5 kΩ							
	R_{CFG2}	0 Ω	511 Ω	1.15 kΩ	1.87 kΩ	2.74 kΩ	3.83 kΩ	5.11 kΩ	6.49 kΩ
3.4 V	R_{CFG1}	0 Ω							
	R_{CFG2}	8.25 kΩ	10.5 kΩ	13.3 kΩ	16.2 kΩ	20.5 kΩ	24.9 kΩ	30.1 kΩ	36.5 kΩ
3.5 V	R_{CFG1}	511 Ω							
	R_{CFG2}	8.25 kΩ	10.5 kΩ	13.3 kΩ	16.2 kΩ	20.5 kΩ	24.9 kΩ	30.1 kΩ	36.5 kΩ
3.6 V	R_{CFG1}	1.15 kΩ							
	R_{CFG2}	8.25 kΩ	10.5 kΩ	13.3 kΩ	16.2 kΩ	20.5 kΩ	24.9 kΩ	30.1 kΩ	36.5 kΩ
3.7 V	R_{CFG1}	1.87 kΩ							
	R_{CFG2}	8.25 kΩ	10.5 kΩ	13.3 kΩ	16.2 kΩ	20.5 kΩ	24.9 kΩ	30.1 kΩ	36.5 kΩ
3.8 V	R_{CFG1}	2.74 kΩ							
	R_{CFG2}	8.25 kΩ	10.5 kΩ	13.3 kΩ	16.2 kΩ	20.5 kΩ	24.9 kΩ	30.1 kΩ	36.5 kΩ
3.9 V	R_{CFG1}	3.83 kΩ							
	R_{CFG2}	8.25 kΩ	10.5 kΩ	13.3 kΩ	16.2 kΩ	20.5 kΩ	24.9 kΩ	30.1 kΩ	36.5 kΩ
4.0 V	R_{CFG1}	5.11 kΩ							
	R_{CFG2}	8.25 kΩ	10.5 kΩ	13.3 kΩ	16.2 kΩ	20.5 kΩ	24.9 kΩ	30.1 kΩ	36.5 kΩ
4.1 V	R_{CFG1}	6.49 kΩ							
	R_{CFG2}	8.25 kΩ	10.5 kΩ	13.3 kΩ	16.2 kΩ	20.5 kΩ	24.9 kΩ	30.1 kΩ	36.5 kΩ

Table 6-2. Input Current Limit and Output Voltage (SEL = High) Settings (continued)

Output Voltage – $V_{O(2)}$ (SEL = HIGH)		Input Current Limit							
		UNLIMITED	100 mA	50 mA	25 mA	10 mA	5 mA	2.5 mA	1 mA
4.2 V	R_{CFG1}	8.25 kΩ							
	R_{CFG2}	8.25 kΩ	10.5 kΩ	13.3 kΩ	16.2 kΩ	20.5 kΩ	24.9 kΩ	30.1 kΩ	36.5 kΩ
4.3 V	R_{CFG1}	10.5 kΩ							
	R_{CFG2}	8.25 kΩ	10.5 kΩ	13.3 kΩ	16.2 kΩ	20.5 kΩ	24.9 kΩ	30.1 kΩ	36.5 kΩ
4.4 V	R_{CFG1}	13.3 kΩ							
	R_{CFG2}	8.25 kΩ	10.5 kΩ	13.3 kΩ	16.2 kΩ	20.5 kΩ	24.9 kΩ	30.1 kΩ	36.5 kΩ
4.5 V	R_{CFG1}	16.2 kΩ							
	R_{CFG2}	8.25 kΩ	10.5 kΩ	13.3 kΩ	16.2 kΩ	20.5 kΩ	24.9 kΩ	30.1 kΩ	36.5 kΩ
4.6 V	R_{CFG1}	20.5 kΩ							
	R_{CFG2}	8.25 kΩ	10.5 kΩ	13.3 kΩ	16.2 kΩ	20.5 kΩ	24.9 kΩ	30.1 kΩ	36.5 kΩ
4.7 V	R_{CFG1}	24.9 kΩ							
	R_{CFG2}	8.25 kΩ	10.5 kΩ	13.3 kΩ	16.2 kΩ	20.5 kΩ	24.9 kΩ	30.1 kΩ	36.5 kΩ
4.8 V	R_{CFG1}	30.1 kΩ							
	R_{CFG2}	8.25 kΩ	10.5 kΩ	13.3 kΩ	16.2 kΩ	20.5 kΩ	24.9 kΩ	30.1 kΩ	36.5 kΩ
5.0 V	R_{CFG1}	36.5 kΩ							
	R_{CFG2}	8.25 kΩ	10.5 kΩ	13.3 kΩ	16.2 kΩ	20.5 kΩ	24.9 kΩ	30.1 kΩ	36.5 kΩ

Table 6-3 summarizes the resistor values needed to configure the device for different output voltage (SEL = low) settings. For correct operation, use resistors with a tolerance of ±1% or better and a temperature coefficient of better than ±200 ppm.

Table 6-3. Output Voltage (SEL Pin = Low) Settings

Output Voltage – $V_{O(1)}$ (SEL = LOW)	R_{CFG3}
1.8 V	0 Ω
2.0 V	511 Ω
2.1 V	1.15 kΩ
2.2 V	1.87 kΩ
2.3 V	2.74 kΩ
2.4 V	3.83 kΩ
2.5 V	5.11 kΩ
2.6 V	6.49 kΩ
2.7 V	8.25 kΩ
2.8 V	10.5 kΩ
3.0 V	13.3 kΩ
3.3 V	16.2 kΩ
3.6 V	20.5 kΩ
4.0 V	24.9 kΩ
4.5 V	30.1 kΩ
5.0 V	36.5 kΩ

6.3.7 SEL Pin

The SEL pin selects which configuration bits control the output voltage.

- When SEL = high, the output voltage $V_{O(2)}$ is set.
- When SEL = low, the output voltage $V_{O(1)}$ is set.

6.3.8 Short-Circuit Protection

6.3.8.1 Current Limit Setting = 'Unlimited'

The device has a built-in short circuit protection function to limit the current through Q1. The maximum current that flows is limited by the peak current limit. The output voltage decreases if the load is higher than the peak current limit. If the output voltage falls below 1.25 typically, the short circuit protection is activated. With short circuit protection activated, the input current is limited to 26 mA on average.

The device automatically restarts to normal operation after the short condition is removed.

6.3.8.2 Current Limit Setting = 1 mA to 100 mA

The input current limiting function automatically limits current during a short-circuit condition. The device regulates the average input current for as long as the short-circuit condition exists. If the output voltage falls below 1.25 V typically, the short circuit protection is activated. For input current limit settings of 100 mA, 50 mA, and 25 mA, the short circuit protection limits the input current to 26 mA on average. For input current limit setting of 10 mA, 5 mA, 2.5 mA, and 1 mA, the short circuit protection limits the input current to slightly above the typical values for each setting. Table 6-4 shows the typical short circuit currents for each input current limit setting.

The device automatically restarts to previous operation after the short condition is removed.

Table 6-4. Typical Input Current During Short Circuit Condition (V_O < 1.25 V Typically) for All Input Current Limit Settings

Input Current Limit Setting	Typical Short Circuit Input Current
1 mA	1.2 mA
2.5 mA	2.8 mA
5 mA	5.2 mA
10 mA	12 mA
25 mA	26 mA
50 mA	26 mA
100 mA	26 mA
Unlimited	26 mA

6.3.9 Thermal Shutdown

The device has a thermal shutdown function that disables the device if it gets too hot for correct operation. When the device cools down, it automatically restarts operation after a typical delay of $t_{d(RESTART)}$ = 10 ms. The device starts with the soft-start feature (see Section 6.3.3) and keeps the previously read CFG pin setting.

6.4 Device Functional Modes

The device has two functional modes: on and off. The device enters on mode when the voltage on the VIN pin is higher than the UVLO threshold and a high logic level is applied to the EN pin. The device enters off mode when the voltage on the VIN pin is lower than the UVLO threshold or a low logic level is applied to the EN pin.

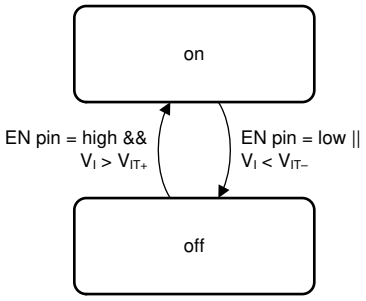


Figure 6-13. Device Functional Modes

7 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

7.1 Application Information

The TPS63901 is a high-efficiency, non-inverting buck-boost converter with an extremely low quiescent current, suitable for applications that need a regulated output voltage from an input supply that can be higher or lower than the output voltage. The input current limit and output voltage are set through resistors connected to the three CFGx pins.

7.2 Typical Application

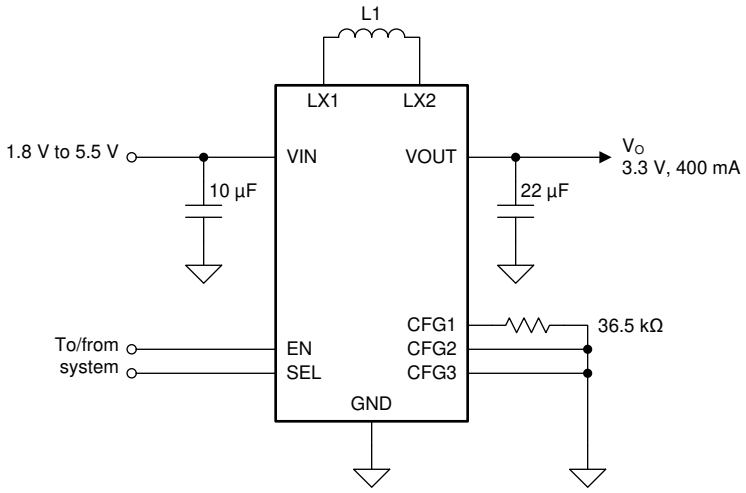


Figure 7-1. 3.3-V_{OUT} Typical Application

7.2.1 Design Requirements

The design guideline provides a component selection to operate the device within the *Recommended Operating Conditions* .

Table 7-1. Matrix of Output Capacitor and Inductor Combinations

Nominal Inductor Value [µH](1)	Nominal Output Capacitor Value [µF](2)				
	10	22	47	100	≥ 300
2.2	+(3)	+ (4)	+	+	+(5)

(1) Inductor tolerance and current derating is anticipated. The effective inductance can vary by 20% and –30%.
(2) Capacitance tolerance and DC bias voltage derating is anticipated. The effective capacitance can vary by 20% and –50%.
(3) Output voltage ripple increases versus typical application.
(4) Typical application. Other check marks indicate possible filter combinations.
(5) Start-up time increased

7.2.2 Detailed Design Procedure

The first step is the selection of the output filter components. To simplify this process, the *Recommended Operating Conditions* outlines minimum and maximum values for inductance and capacitance. Tolerance and derating must be taken into account when selecting nominal inductance and capacitance.

7.2.2.1 Inductor Selection

The inductor selection is affected by several parameters such as inductor ripple current, output voltage ripple, transition point into power save mode, and efficiency. See Table 7-2 for typical inductors.

For high efficiencies, the inductor must have a low DC resistance to minimize conduction losses. Especially at high-switching frequencies, the core material has a high impact on efficiency. When using small chip inductors, the efficiency is reduced mainly due to higher inductor core losses, which needs to be considered when selecting the appropriate inductor. The inductor value determines the inductor ripple current. The larger the inductor value, the smaller the inductor ripple current and the lower the core and conduction losses of the converter. Conversely, larger inductor values cause a slower load transient response. To avoid saturation of the inductor, the peak current for the inductor in steady state operation is calculated using Equation 5. Only the equation that defines the switch current in boost mode is shown because this provides the highest value of current and represents the critical current value for selecting the right inductor.

$$\text{Duty Cycle Boost} \qquad D = \frac{V_{OUT} - V_{IN}}{V_{OUT}} \tag{4}$$

$$I_{PEAK} = \frac{Iout}{\eta \times (1 - D)} + \frac{Vin \times D}{2 \times f \times L} \tag{5}$$

where

- D is duty cycle in boost mode.
- *f* is the converter switching frequency.
- L is the inductor value.
- η is the estimated converter efficiency (use the number from the efficiency curves or 0.9 as an assumption).

Note

The calculation must be done for the minimum input voltage in boost mode.

Calculating the maximum inductor current using the actual operating conditions gives the minimum saturation current of the inductor needed. TI recommends choosing an inductor with a saturation current 20% higher than the value calculated using Equation 5. Possible inductors are listed in Table 7-2.

Table 7-2. List of Recommended Inductors

Inductor Value [µH](1)	Saturation Current [A]	DCR [mΩ]	Part Number	Manufacturer	Size (L × W × H mm)
2.2	3.5	21	XFL4020-222ME	Coilcraft	4 × 4 × 2
2.2	1.7	72	SRN3015TA-2R2M	Bourns	3 × 3 × 1.5
2.2	3.3	82	DFE252012F-2R2M	Murata	2.5 × 2 × 1.2
2.2	2.4	116	DFE201612E-2R2M	Murata	2.0 × 1.6 × 1.2
2.2	2.0	190	DFE201210U-2R2M	Murata	2.0 × 1.2 × 1.0

(1) See the *Third-party Products Disclaimer* .

7.2.2.2 Output Capacitor Selection

For the output capacitor, use of small ceramic capacitors placed as close as possible to the VOUT and GND pins of the IC is recommended. The recommended nominal output capacitor value is a single 22 µF. If, for any reason, the application requires the use of large capacitors, which cannot be placed close to the IC, use a smaller ceramic capacitor in parallel to the large capacitor. The small capacitor must be placed as close as possible to the VOUT and GND pins of the IC.

It is important that the effective capacitance is given according to the recommended value in the *Recommended Operating Conditions*. In general, consider DC bias effects resulting in less effective capacitance. The choice of the output capacitance is mainly a trade-off between size and transient behavior as higher capacitance reduces

transient response overshoot and undershoot and increases transient response time. Possible output capacitors are listed in Table 7-3.

There is no upper limit for the output capacitance value.

At light load currents, the output voltage ripple is dependent on the output capacitor value. Larger output capacitors reduce the output voltage ripple. The leakage current of the output capacitor adds to the overall quiescent current.

Table 7-3. List of Recommended Capacitors

Capacitor Value [µF](1)	Voltage Rating [V]	Part Number	Manufacturer	Size (Metric)
22	6.3	GRM187R60J226ME15	Murata	0603 (1608)
22	6.3	GRM219R60J476ME44	Murata	0805 (3210)
47	6.3	GRM188R60J476ME15	Murata	0603 (1608)

(1) See the *Third-party Products Disclaimer* .

7.2.2.3 Input Capacitor Selection

A 10-µF input capacitor is recommended to improve line transient behavior of the regulator and EMI behavior of the total power supply circuit. An X5R or X7R ceramic capacitor placed as close as possible to the VIN and GND pins of the IC is recommended. This capacitance can be increased without limit. If the input supply is located more than a few inches from the TPS63901 converter, additional bulk capacitance can be required in addition to the ceramic bypass capacitors. An electrolytic or tantalum capacitor with a value of 47 µF is a typical choice.

When operating from a high impedance source, a larger input buffer capacitor is recommended to avoid voltage drops during start-up and load transients.

The input capacitor can be increased without any limit for better input voltage filtering. The leakage current of the input capacitor adds to the overall quiescent current.

Table 7-4. List of Recommended Capacitors

Capacitor Value [µF](1)	Voltage Rating [V]	Part Number	Manufacturer	Size (Metric)
10	6.3	GRM188R60J106ME47	Murata	0603 (1608)
10	10	GRM188R61A106ME69	Murata	0603 (1608)
22	6.3	GRM187R60J226ME15	Murata	0603 (1608)

(1) See the *Third-party Products Disclaimer* .

7.2.2.4 Setting The Output Voltage

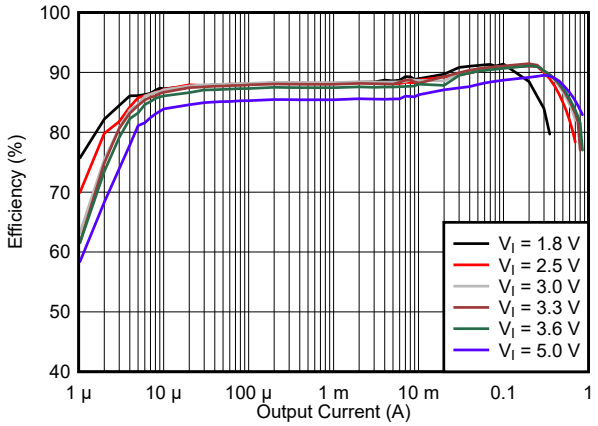
The output voltage is set with the CFGx pins (see Section 6.3.6).

7.2.3 Application Curves

Table 7-5. Components for Application Characteristic Curves for V_{OUT} = 3.3 V

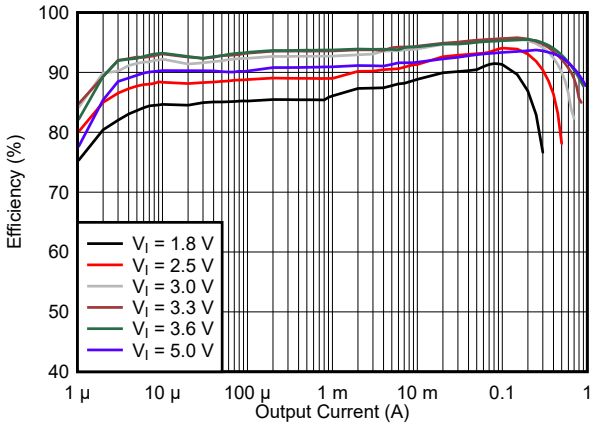
Reference(1)	Description(2)	Part Number	Manufacturer
U1	400-mA ultra low I_Q buck-boost converter (1.5 mm × 1.15 mm)	TPS63901YCJ	Texas Instruments
L1	2.2 µH, 2.5 mm × 2 mm 3.3 A, 82 mΩ	DFE252012F-2R2M	Murata
C1	10 µF, 0603, ceramic capacitor, ±20%, 6.3 V	GRM188R60J106ME47	Murata
C2	22 µF, 0603, ceramic capacitor, ±20%, 6.3 V	GRM187R60J226ME15	Murata
CFG1	36.5 kΩ, 0603 resistor, 1%, 100 mW	Standard	Standard
CFG2	0 Ω, 0603 resistor, 1%, 100 mW	Standard	Standard
CFG3	0 Ω, 0603 resistor, 1%, 100 mW	Standard	Standard

(1) See the *Third-Party Products Discalimer*
(2) For other output voltages, refer to Table 7-1 for resistor values.



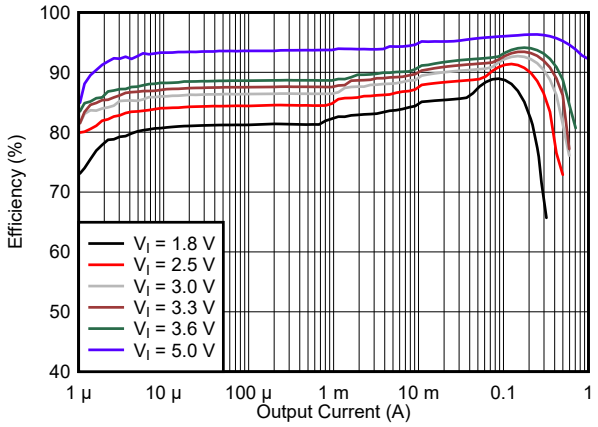
V_O = 1.8 V T_A = 25°C

Figure 7-2. Efficiency vs Output Current



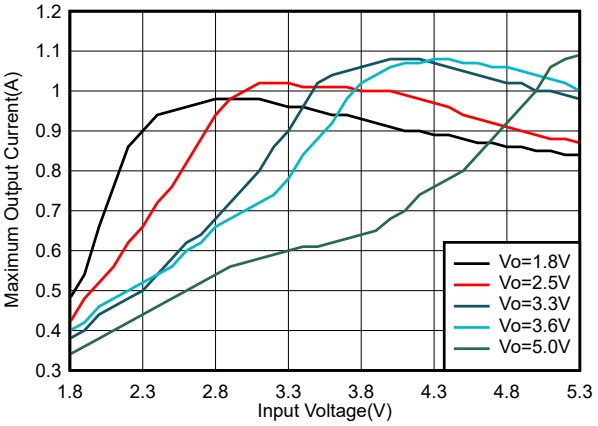
V_O = 3.3 V T_A = 25°C

Figure 7-3. Efficiency vs Output Current



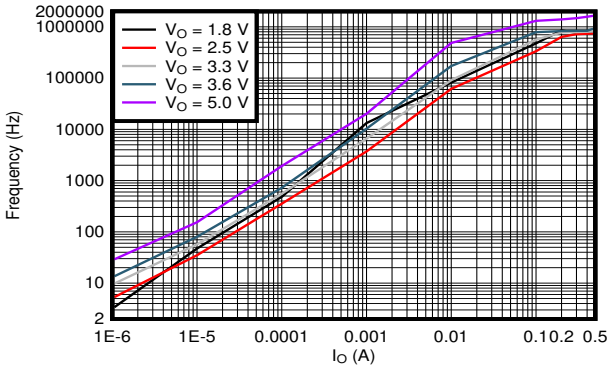
V_O = 5.0 V T_A = 25°C

Figure 7-4. Efficiency vs Output Current



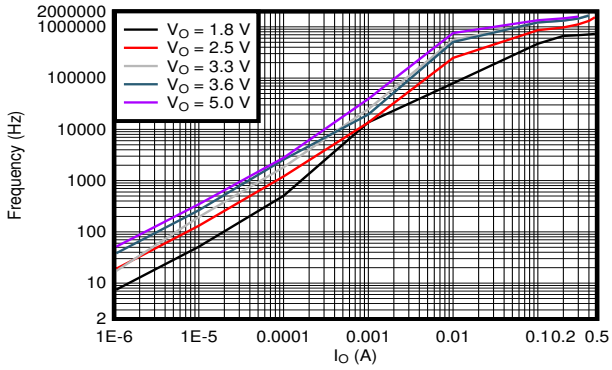
T_A = 25°C

Figure 7-5. Typical Output Current Capability vs Input Voltage



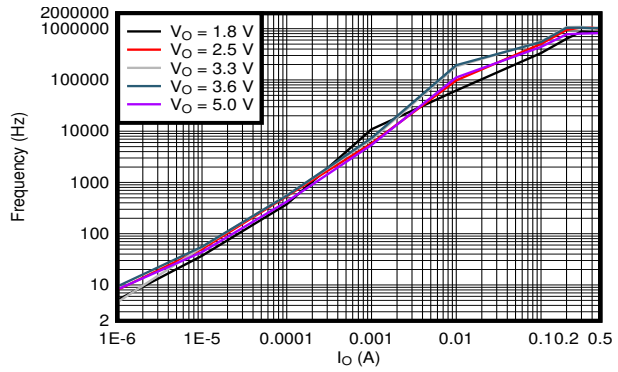
V_I = 3.3 V T_A = 25°C

Figure 7-6. Typical Burst Switching Frequency vs Output Current



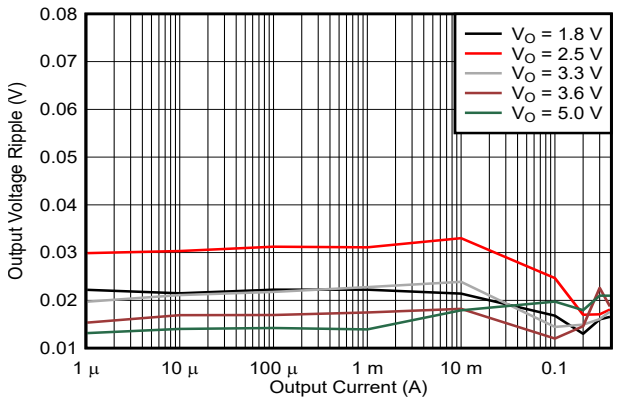
V_I = 2.0 V T_A = 25°C

Figure 7-7. Typical Burst Switching Frequency vs Output Current



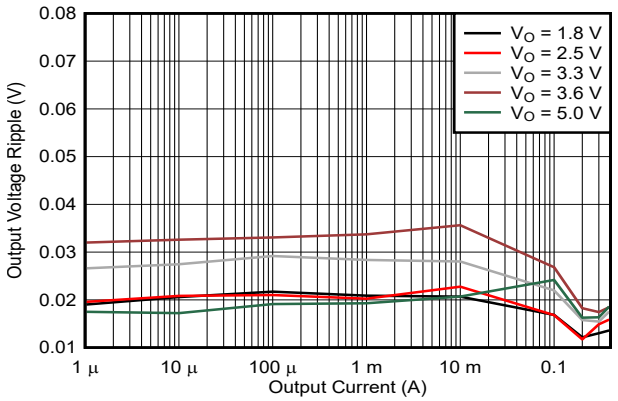
V_I = 5.2 V T_A = 25°C

Figure 7-8. Typical Burst Switching Frequency vs Output Current



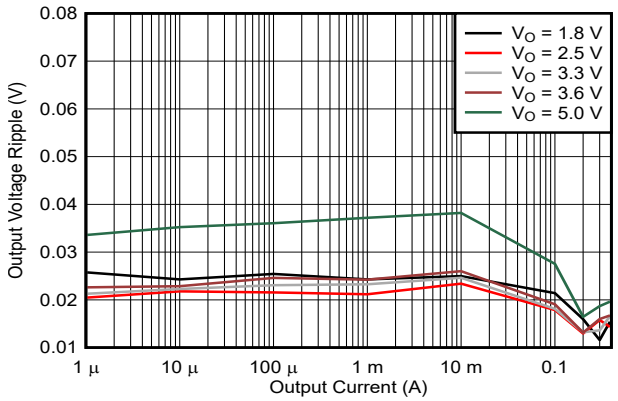
V_I = 3.3 V T_A = 25°C

Figure 7-9. Output Voltage Ripple



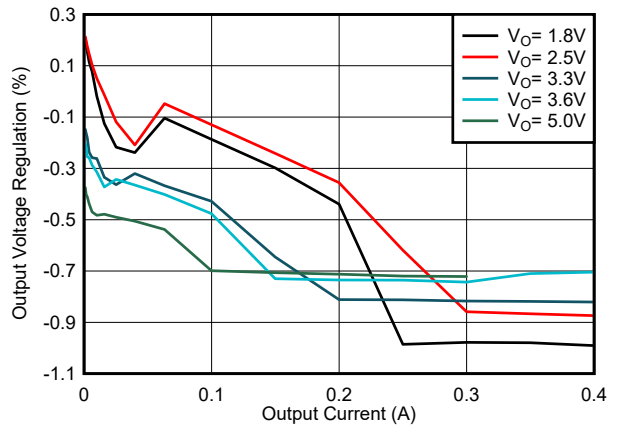
V_I = 4.4 V T_A = 25°C

Figure 7-10. Output Voltage Ripple



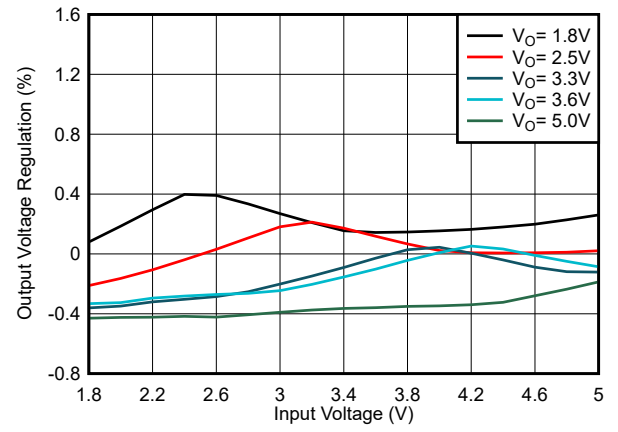
V_I = 5.2 V T_A = 25°C

Figure 7-11. Output Voltage Ripple



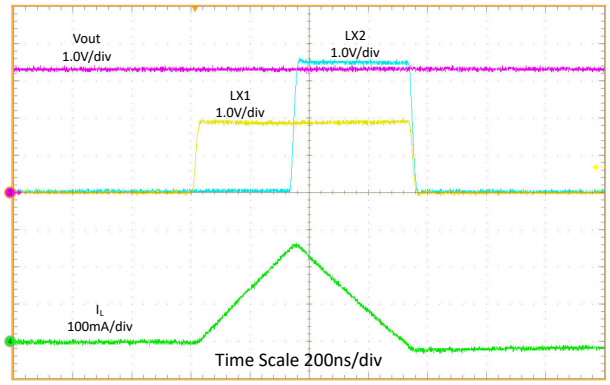
V_I = 3.3 V T_A = 25°C

Figure 7-12. Load Regulation



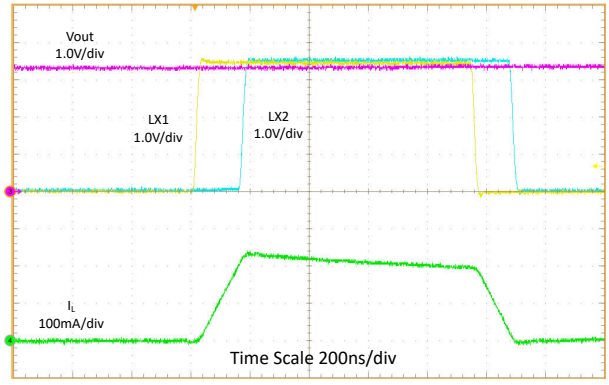
V_I = 1.8 V to 5.0 V Load = 1 mA, T_A = 25°C

Figure 7-13. Line Regulation



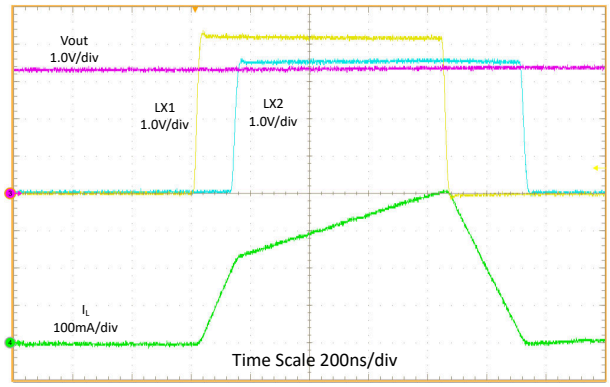
V_I = 1.8 V, V_O = 3.3 V No load

Figure 7-14. Switching Waveforms, Boost Operation



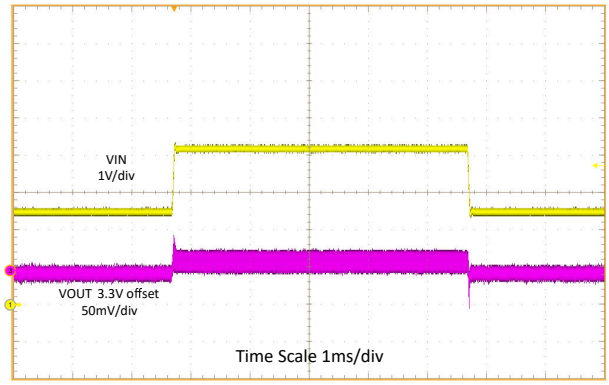
V_I = 3.3 V, V_O = 3.3 V No load

Figure 7-15. Switching Waveforms, Buck-Boost Operation



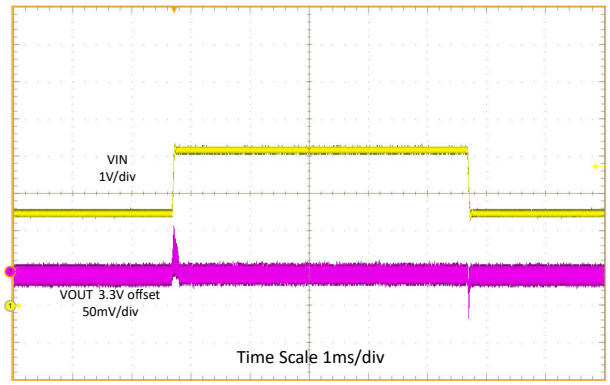
V_I = 4.0 V, V_O = 3.3 V No load

Figure 7-16. Switching Waveforms, Buck Operation



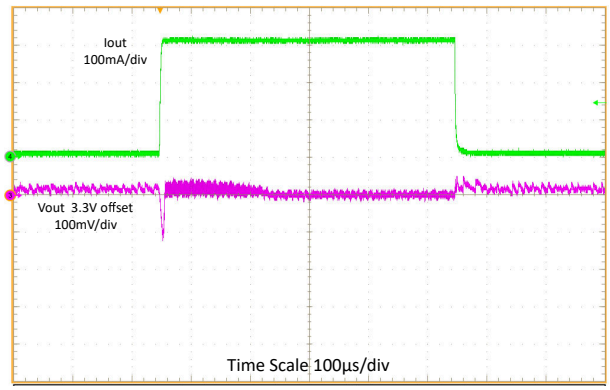
V_I = 2.5 V to 4.2 V, V_O = 3.3 V Load = 200-mA resistive load

Figure 7-17. Line Transient, 200-mA Load



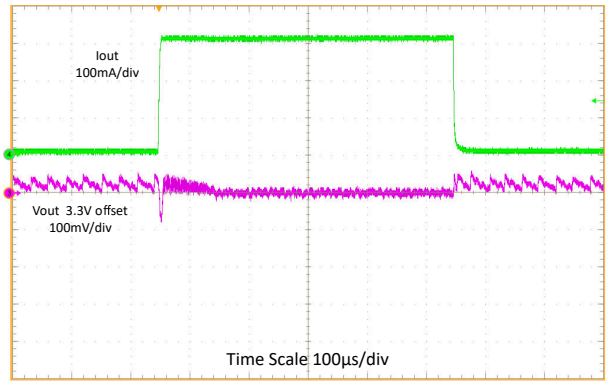
V_I = 2.5 V to 4.2 V, V_O = 3.3 V Load = 400-mA resistive load

Figure 7-18. Line Transient, 400-mA Load



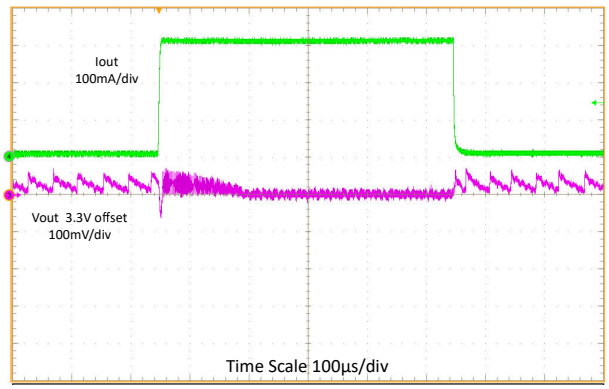
V_I = 2.7 V, V_O = 3.3 V Load = 0 mA to 300 mA, t_r/t_f = 2 µs

Figure 7-19. Load Transient, 300-mA Step



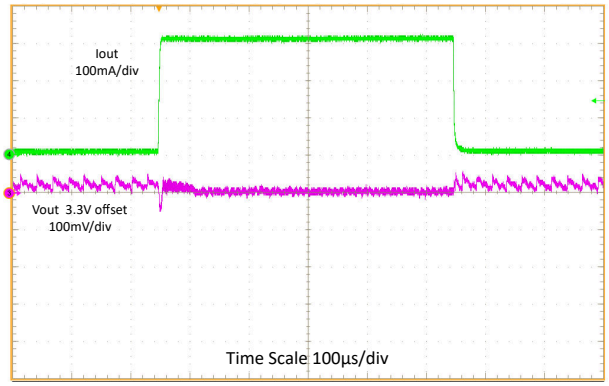
V_I = 3.3 V, V_O = 3.3 V Load = 0 mA to 300 mA, t_r/t_f = 2 µs

Figure 7-20. Load Transient, 300-mA Step



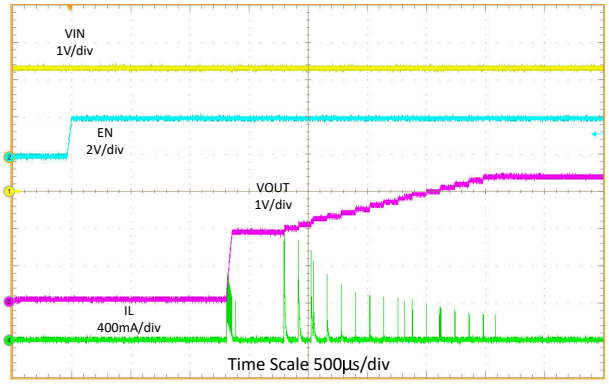
V_I = 4.2 V, V_O = 3.3 V Load = 0 mA to 300 mA, t_r/t_f = 2 µs

Figure 7-21. Load Transient, 300-mA Step



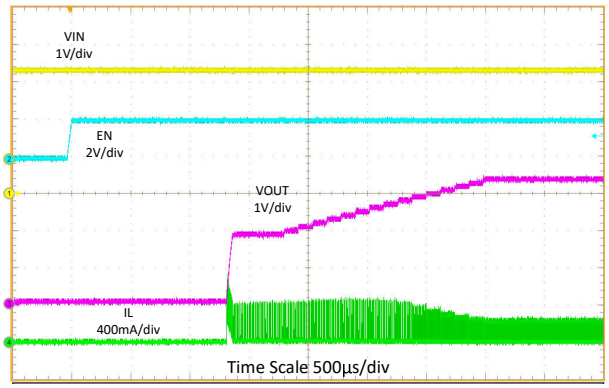
V_I = 5.5 V, V_O = 3.3 V Load = 0 mA to 300 mA, t_r/t_f = 2 µs

Figure 7-22. Load Transient, 300-mA Step



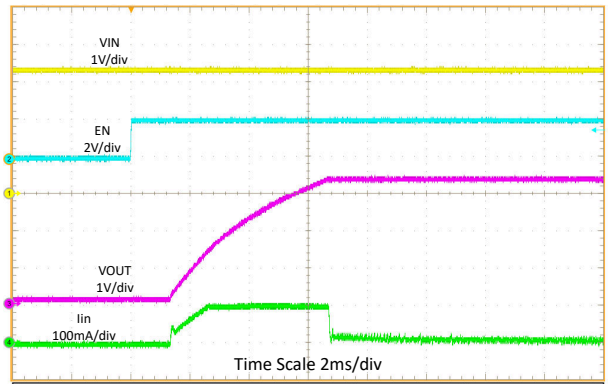
V_I = 3.3 V, V_O = 3.3 V 10-µA resistive load

Figure 7-23. Start-Up Behavior from Rising Enable



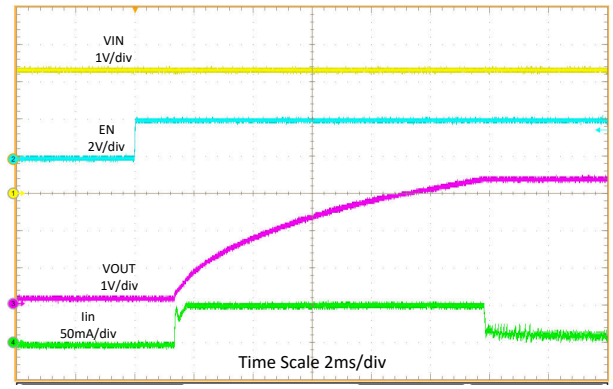
V_I = 3.3 V, V_O = 3.3 V 100-mA resistive load

Figure 7-24. Start-Up Behavior from Rising Enable



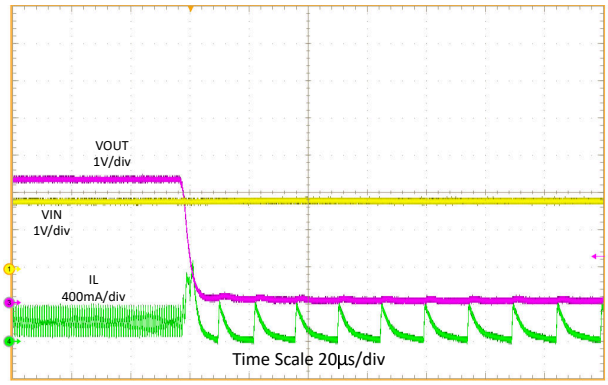
V_I = 3.3 V, V_O = 3.3 V C_I = 32 µF, C_O = 300 µF

Figure 7-25. Start-Up with 100-mA ICL



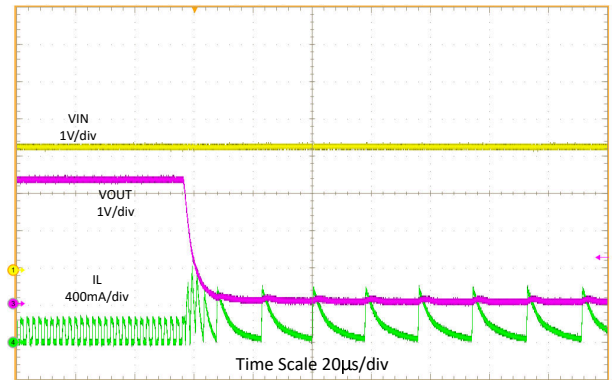
V_I = 3.3 V, V_O = 3.3 V C_I = 32 µF, C_O = 300 µF

Figure 7-26. Start-Up with 50-mA ICL



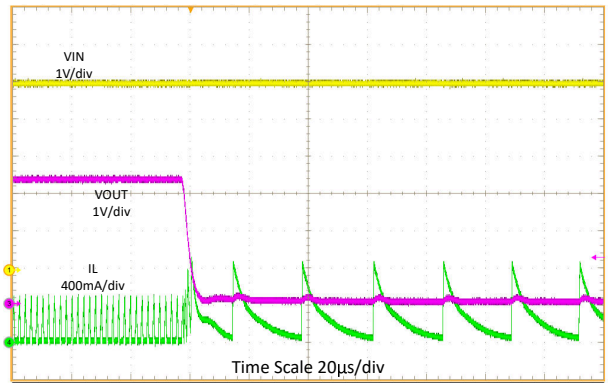
V_I = 1.8 V, V_O = 3.3 V T_A = 25°C

Figure 7-27. Short Circuit Behavior



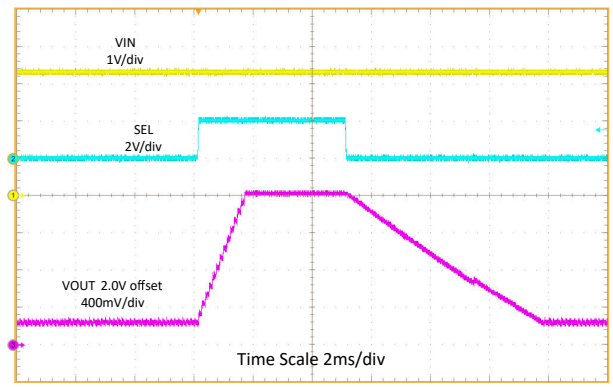
V_I = 3.3 V, V_O = 3.3 V T_A = 25°C

Figure 7-28. Short Circuit Behavior



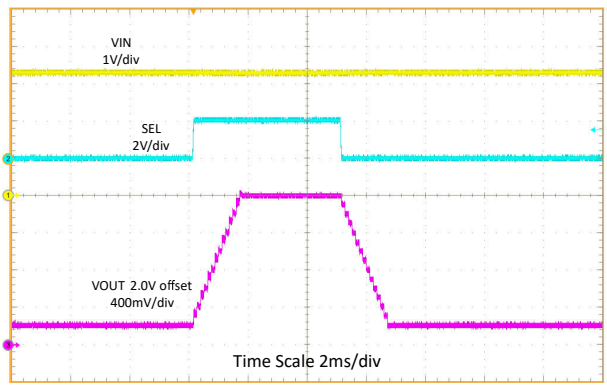
V_I = 5.0 V, V_O = 3.3 V T_A = 25°C

Figure 7-29. Short Circuit Behavior



V_I = 3.3 V, $V_{O(1)}$ = 2.2 V, $V_{O(2)}$ = 3.6 V 0.1-mA resistive load

Figure 7-30. DVS Behavior at Light Load



V_I = 3.3 V, $V_{O(1)}$ = 2.2 V, $V_{O(2)}$ = 3.6 V 400-mA resistive load

Figure 7-31. DVS Behavior at High Load

8 Power Supply Recommendations

The TPS63901 device is designed to operate with input supplies from 1.8 V to 5.5 V. The input supply must be stable and free of noise to achieve the full performance of the device. If the input supply is located more than a few centimeters away from the device, additional bulk capacitance can be required. The input capacitance shown in the application schematics in this data sheet is sufficient for typical applications.

9 Layout

9.1 Layout Guidelines

PCB layout is an important part of any switching power supply design. A poor layout can cause unstable operation, load regulation problems, increased ripple and noise, and EMI issues.

The following PCB layout design guidelines are recommended:

- Place the input and output capacitors close to the device.
- Minimize the area of the input loop, and use short, wide traces on the top layer to connect the input capacitor to the VIN and GND pins.
- Minimize the area of the output loop, and use short, wide traces on the top layer to connect the output capacitor to the VOUT and GND pins.
- The location of the inductor on the PCB is less important than the location of the input and output capacitors. Place the inductor after the input and output capacitors have been placed close to the device. Route the traces to the inductor on an inner layer if necessary.

9.2 Layout Example

Figure 9-1 shows an example of a PCB layout that follows the recommendations of the previous section.

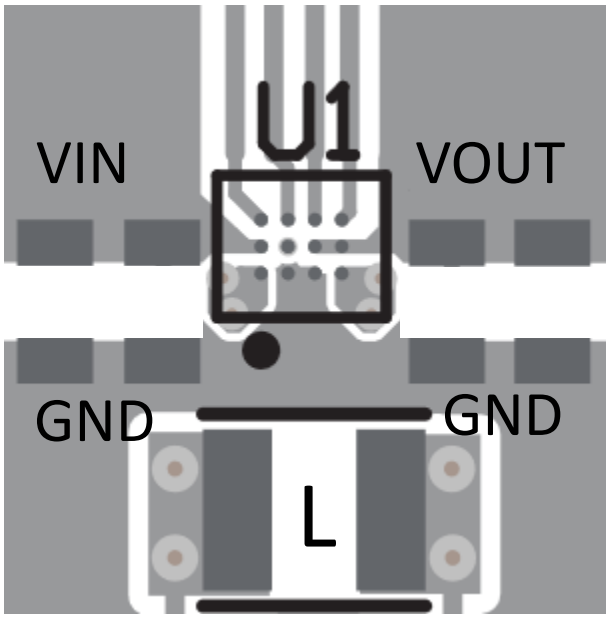


Figure 9-1. PCB Layout Example

10 Device and Documentation Support

10.1 Device Support

10.1.1 Third-Party Products Disclaimer

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OR A WARRANTY, REPRESENTATION OR ENDORSEMENT OF SUCH PRODUCTS OR SERVICES, EITHER ALONE OR IN COMBINATION WITH ANY TI PRODUCT OR SERVICE.

10.2 Documentation Support

10.2.1 Related Documentation

For related documentation see the following:

Texas Instruments, *TPS63901 EVM User Guide*

10.3 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

10.4 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

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10.6 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

10.7 Glossary

TI Glossary	This glossary lists and explains terms, acronyms, and definitions.

11 Revision History

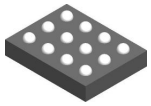
NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision A (June 2022) to Revision B (August 2024)	Page
• Added YCJ0012-C02 packaging information	27

Changes from Revision * (December 2021) to Revision A (June 2022)	Page
• Changed document status from Advance Information to Production Data	1

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

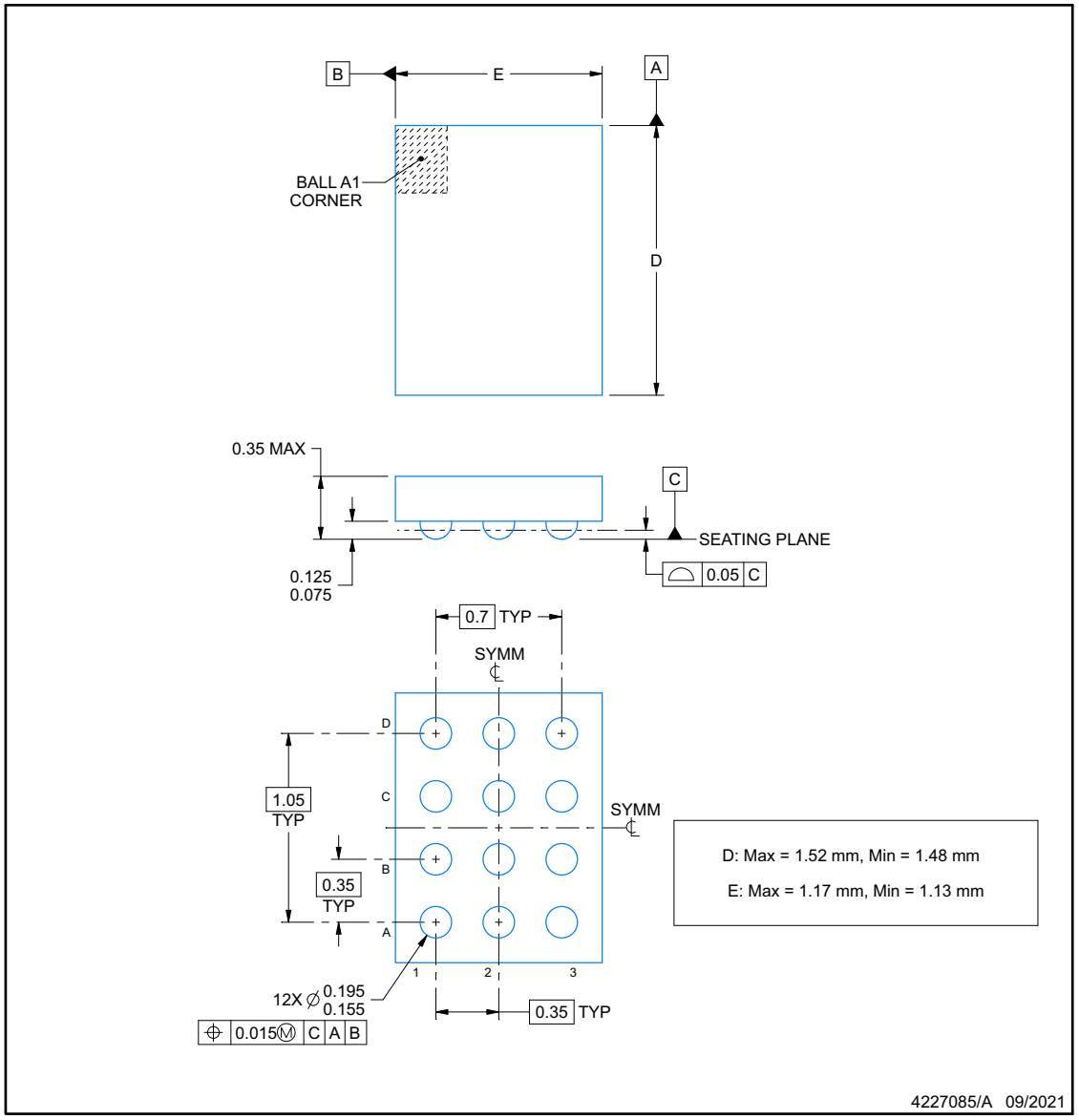


PACKAGE OUTLINE

YCJ0012-C02

DSBGA - 0.35 mm max height

DIE SIZE BALL GRID ARRAY



NOTES:

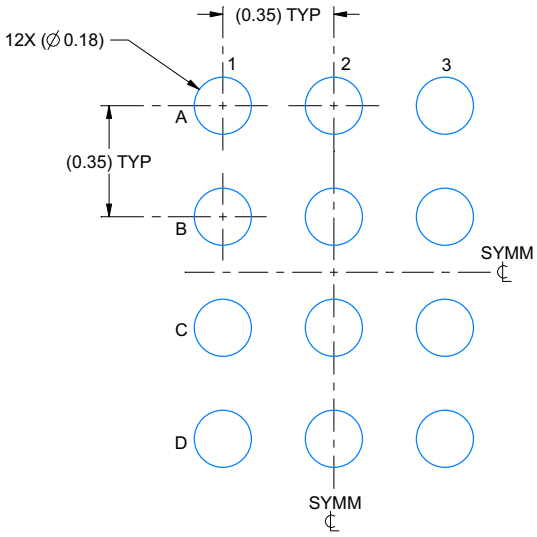
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.

EXAMPLE BOARD LAYOUT

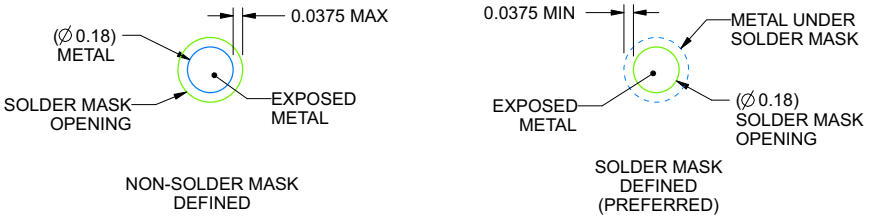
YCJ0012-C02

DSBGA - 0.35 mm max height

DIE SIZE BALL GRID ARRAY



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 50X



SOLDER MASK DETAILS
NOT TO SCALE

4227085/A 09/2021

NOTES: (continued)

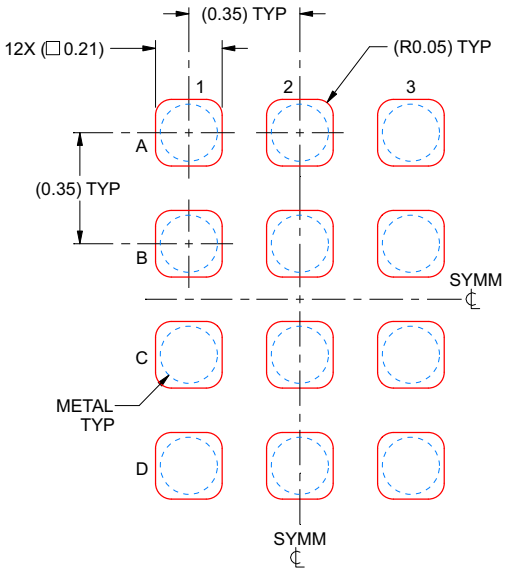
3. Final dimensions may vary due to manufacturing tolerance considerations and also routing constraints.
   See Texas Instruments Literature No. SNVA009 (www.ti.com/lit/snva009).

EXAMPLE STENCIL DESIGN

YCJ0012-C02

DSBGA - 0.35 mm max height

DIE SIZE BALL GRID ARRAY



SOLDER PASTE EXAMPLE
BASED ON 0.075 mm THICK STENCIL
SCALE: 50X

4227085/A 09/2021

NOTES: (continued)

4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPS63901YCJR	ACTIVE	DSBGA	YCJ	12	3000	RoHS & Green	SNAGCU	Level-1-260C-UNLIM	-40 to 125	3901	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

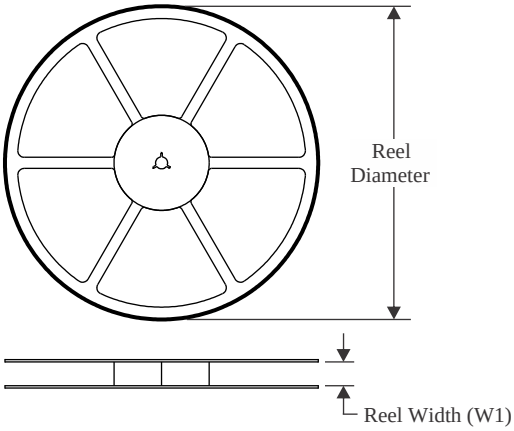
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

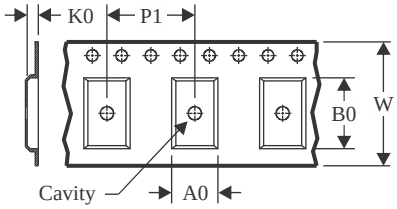
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

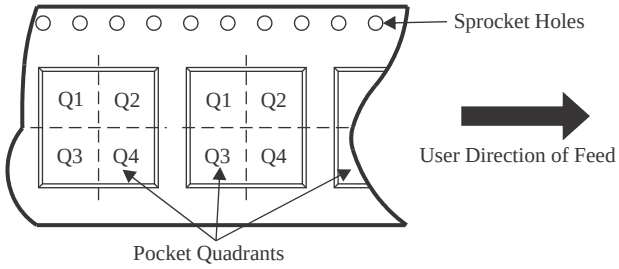


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

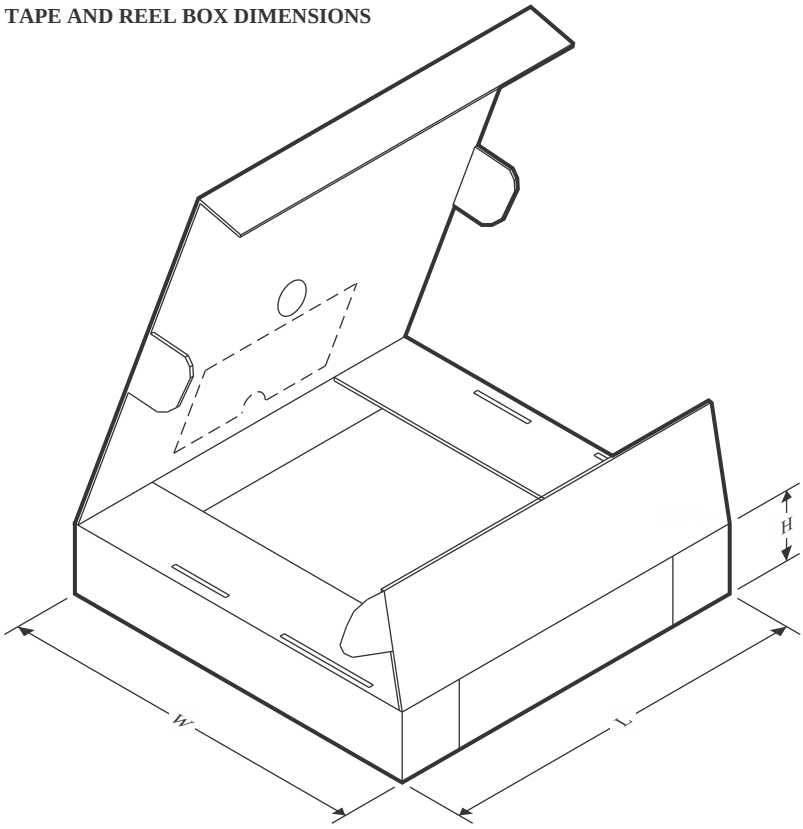
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS63901YCJR	DSBGA	YCJ	12	3000	180.0	8.4	1.26	1.65	0.43	4.0	8.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS63901YCJR	DSBGA	YCJ	12	3000	182.0	182.0	20.0

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