TPS65051-Q1 6-Channel Power Management IC With 2 Step-Down Converters and 4 Low-Input-Voltage LDOs

1 Features

- Qualified for Automotive Applications
- AEC-Q100 Qualified With the Following Results:
  - Device Temperature Grade 1: –40°C to +125°C Ambient Operating Temperature Range
  - Device HBM ESD Classification Level H2
  - Device CDM ESD Classification Level C3B
- Up To 95% Efficiency
- Output Current for DC-DC Converter: DCDC1 = 1 A; DCDC2 = 0.6 A
- Externally Adjustable Output Voltage for DC-DC Converter
- V_I Range for DC-DC Converters From 2.5 V to 6 V
- 2.25-MHz Fixed-Frequency Operation
- Power-Save Mode at Light Load Current
- 180° Out-of-Phase Operation
- Output-Voltage Accuracy in PWM Mode ±1%
- Low-Ripple PFM Mode
- Total Typical 32-µA Quiescent Current for Both DC-DC Converters
- 100% Duty Cycle for Lowest Dropout
- Two General-Purpose 400-mA, High-PSRR LDOs
- Two General-Purpose 200-mA, High-PSRR LDOs
- V_I Range for LDOs from 1.5 V to 6.5 V
- Digital Voltage Selection for the LDOs
- Available in a 4-mm × 4-mm 32-Pin VQFN Package

2 Applications

Automotive Infotainment
Automotive Cluster
Automotive Digital Radio

3 Description

The TPS65051-Q1 device is an integrated power-management IC for applications powered by one Li-Ion or Li-Polymer cell, which requires multiple power rails. The TPS65051-Q1 device provides two efficient, 2.25-MHz step-down converters targeted at providing the core voltage and I/O voltage in a processor-based system. Both step-down converters enter a low-power mode at light load for maximum efficiency across the widest possible range of load currents. For low-noise applications, the user can force the devices into fixed-frequency PWM mode by pulling the MODE pin high. Operating in the shutdown mode reduces the current consumption to less than 1 µA. The devices allow the use of small inductors and capacitors to achieve a small solution size. The TPS65051-Q1 device provides an output current of up to 1 A (DCDC1) and 0.6 A (DCDC2). The TPS65051-Q1 device also integrates two 400-mA LDO and two 200-mA LDO voltage regulators, which one can turn on or off using separate enable pins on each LDO. Each LDO operates with an input voltage range between 1.5 V and 6.5 V, allowing the supply to be from one of the step-down converters or directly from the main battery.

The LDO voltage of the TPS65051-Q1 device is adjustable using external resistor dividers.

Device Information[(1)]

PART NUMBER	PACKAGE	BODY SIZE (NOM)
TPS65051-Q1	VQFN (32)	4.00 mm × 4.00 mm

(1) For all available packages, see the orderable addendum at the end of the datasheet.

Block Diagram

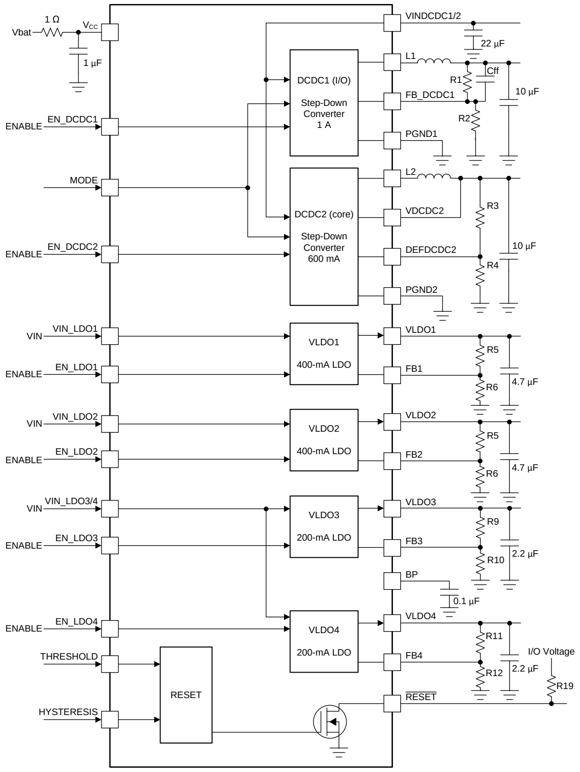


Table of Contents

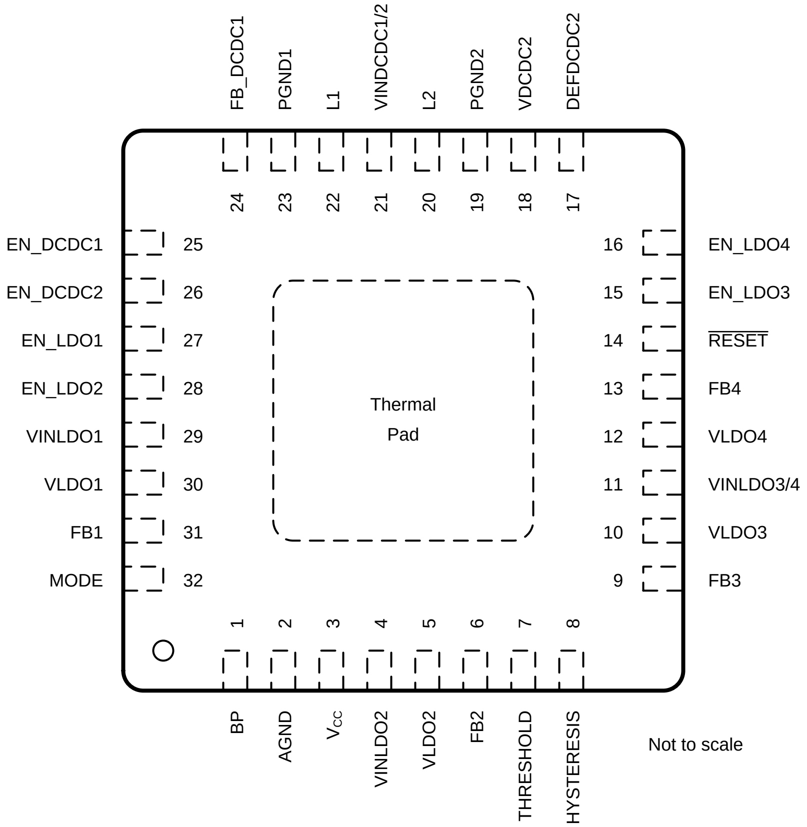
4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision A (November 2012) to Revision B	Page
• Added *Pin Configuration and Functions* section, *ESD Ratings* table, *Feature Description* section, *Device Functional Modes*, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section	1
• Deleted all references to TPS65050-Q1, TPS65052-Q1, TPS65054-Q1, and TPS65056-Q1 part numbers	1
• Deleted the *Ordering Information* table	3
• Changed the resistor labels of R3, R4, and R5 to R13, R14, and R15 in the $\overline{RESET}$ section	20
• Added the *Receiving Notification of Documentation Updates* section	25
• Changed the electrostatic discharge statement	25

5 Pin Configuration and Functions

RSM Package
32-Pin VQFN With Exposed Thermal Pad
Top View



Pin Functions

PIN		I/O	DESCRIPTION
NAME	NO.		
AGND	2	I	Analog GND, connect to PGND and thermal pad
BP	1	I	Input for bypass capacitor for internal reference
DEFDCDC2	17	I	Feedback pin for converter 2. Connect DEFDCDC2 to the center of the external resistor divider.
EN_DCDC1	25	I	Enable input for converter 1, active-high
EN_DCDC2	26	I	Enable input for converter 2, active-high
EN_LDO1	27	I	Enable input for LDO1. Logic high enables the LDO, logic low disables the LDO.
EN_LDO2	28	I	Enable input for LDO2. Logic high enables the LDO, logic low disables the LDO.
EN_LDO3	15	I	Enable input for LDO3. Logic high enables the LDO, logic low disables the LDO.
EN_LDO4	16	I	Enable input for LDO4. Logic high enables the LDO, logic low disables the LDO.
FB1	31	I	Feedback input for the external voltage divider
FB2	6	I	Feedback input for the external voltage divider
FB3	9	I	Feedback input for the external voltage divider
FB4	13	I	Feedback input for the external voltage divider
FB_DCDC1	24	I	Input to adjust output voltage of converter 1 between 0.6 V and V_I. Connect an external resistor divider between VOUT1, this pin, and GND.
HYSTERESIS	8	I	Input for hysteresis on reset threshold
L1	22	O	Switch pin of converter 1. Connected to inductor
L2	20	O	Switch pin of converter 2. Connected to inductor

Pin Functions (continued)

PIN		I/O	DESCRIPTION
NAME	NO.		
MODE	32	I	Select between power-safe mode and forced-PWM mode for DCDC1 and DCDC2. In power-safe mode, the device uses PFM at light loads, PWM for higher loads. Setting this pin to high level selects forced-PWM mode. If this pin has low level, then the device operates in power-safe mode.
PGND1	23	I	GND for converter 1
PGND2	19	I	GND for converter 2
$\overline{\text{RESET}}$	14	O	Open-drain active-low reset output, 100-ms reset-delay time
THRESHOLD	7	I	Reset input
V_{CC}	3	I	Power supply for digital and analog circuitry of DCDC1, DCDC2 and LDOs. Connect this pin to the same voltage supply as VINDCDC1/2.
VDCDC2	18	I	Feedback voltage-sense input, connect directly to the output of converter 2.
VINDCDC1/2	21	I	Input voltage for VDCDC1 and VDCDC2 step-down converters. Connect this pin to the same voltage supply as V_{CC}.
VINLDO1	29	I	Input voltage for LDO1
VINLDO2	4	I	Input voltage for LDO2
VINLDO3/4	11	I	Input voltage for LDO3 and LDO4
VLDO1	30	O	Output voltage of LDO1
VLDO2	5	O	Output voltage of LDO2
VLDO3	10	O	Output voltage of LDO3
VLDO4	12	O	Output voltage of LDO4
Thermal pad		—	Connect to GND

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
V_I	Input voltage on all pins except AGND, PGND, and EN_LDO1 pins with respect to AGND	–0.3	7	V
	Input voltage range on EN_LDO1 pins with respect to AGND	–0.3	V_{CC} + 0.5	
I_I	Current at VINDCDC1/2, L1, PGND1, L2, PGND2		1800	mA
	Current at all other pins		1000	mA
V_O	Output voltage for LDO1, LDO2, LDO3, and LDO4	–0.3	4	V
	Continuous total power dissipation	See the *Thermal Information*		
T_A	Operating free-air temperature	–40	125	°C
T_{stg}	Storage temperature	–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per AEC Q100-002(1)	2000	V
		Charged-device model (CDM), per AEC Q100-011	750	V

(1) AEC Q100-002 indicates that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
V_I	Input voltage for step-down converters, VINDCDC1/2	2.5		6	V
V_O	Output voltage for step-down converter, VDCDC1	0.6		VINDCDC1/2	V
	Output voltage for step-down converter, VDCDC2	0.6		VINDCDC1/2	V
V_I	Input voltage for LDOs, VINLDO1, VINLDO2, VINLDO3/4	1.5		6.5	V
V_O	Output voltage for LDO1 and LDO2	1		3.6	V
	Output voltage for LDO3 and LDO4	1		3.6	V
I_O	Output current at L1 (DCDC1)			1000	mA
	Output current at L2 (DCDC2)			600	mA
	Output current at VLDO1, VLDO2			400	mA
	Output current at VLDO3, VLDO4			200	mA
	Inductor at L1, L2 (1)	1.5	2.2		μH
C_O	Output capacitor at VDCDC1, VDCDC2 (1)	10	22		μF
	Output capacitor at VLDO1, VLDO2, VLDO3, VLDO4 (1)	2.2			μF
C_I	Input capacitor at VCC (1)	1			μF
	Input capacitor at VINLDO1, VINLDO2 (1)	2.2			μF
	Input capacitor at VINLDO3/4 (1)	2.2			μF
T_A	Operating ambient temperature	–40		125	°C
	Resistor from battery voltage to V_{CC} used for filtering (2)		1	10	Ω

(1) See the *Application Information* section of this data sheet for more details.
(2) Up to 2 mA can flow into V_{CC}; when both converters are running in PWM, this resistor causes the UVLO threshold to shift accordingly.

6.4 Thermal Information

THERMAL METRIC (1)		TPS65051-Q1 RSM (VQFN) 32 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	37.2	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	30.1	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	7.8	°C/W
ψ_{JT}	Junction-to-top characterization parameter	0.4	°C/W
ψ_{JB}	Junction-to-board characterization parameter	7.6	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	2.3	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

6.5 Electrical Characteristics

V_{CC} = VINDCDC1/2 = 3.6 V, EN = V_{CC}, MODE = GND, L = 2.2 μH, C_O = 10 μF, T_A = –40°C to 125°C, typical values are at T_A = 25°C (unless otherwise noted).

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
SUPPLY CURRENT							
V_I	Input voltage range at VINDCDC1/2			2.5		6	V
I_Q	Operating quiescent current Total current into V_{CC}, VINDCDC1/2, VINLDO1, VINLDO2, VINLDO3/4	One converter, I_O = 0 mA. PFM mode enabled (Mode = GND) device not switching, EN_DCDC1 = V_I OR EN_DCDC2 = V_I; EN_LDO1= EN_LDO2 = EN_LDO3 = EN_LDO = GND			20	30	μA
		Two converters, I_O = 0 mA PFM mode enabled (Mode = 0) device not switching, EN_DCDC1 = V_I AND EN_DCDC2 = V_I; EN_LDO1 = EN_LDO2 = EN_LDO3 = EN_LDO4 = GND			32	40	μA
		One converter, I_O = 0 mA. PFM mode enabled (Mode = GND) device not switching, EN_DCDC1 = V_I OR EN_DCDC2 = V_I; EN_LDO1 = EN_LDO2 = EN_LDO3 = EN_LDO4 = V_I			180	250	μA
I_Q	Operating quiescent current into V_{CC}	One converter, I_O = 0 mA. Switching with no load (Mode = V_I), PWM operation EN_DCDC1 = V_I OR EN_DCDC2 = V_I; EN_LDO1 = EN_LDO2 = EN_LDO3 = EN_LDO = GND			0.85		mA
		Two converters, I_O = 0 mA Switching with no load (Mode = V_I), PWM operation EN_DCDC1 = V_I AND EN_DCDC2 = V_I; EN_LDO1 = EN_LDO2 = EN_LDO3 = EN_LDO = GND			1.25		mA
$I_{(SD)}$	Shutdown current	EN_DCDC1 = EN_DCDC2 = GND EN_LDO1 = EN_LDO2 = EN_LDO3 = EN_LDO4 = GND			9	12	μA
$V_{(UVLO)}$	Undervoltage lockout threshold for DC-DC converters and LDOs	Voltage at V_{CC}			1.8	2	V
EN_DCDC1, EN_DCDC2, DEFDCDC2, DEFLDO1, DEFLDO2, DEFLDO3, DEFLDO4, EN_LDO1, EN_LDO2, EN_LDO3, EN_LDO4							
V_{IH}	High-level input voltage	MODE, EN_DCDC1, EN_DCDC2, DEFDCDC2, DEFLDO1, DEFLDO2, DEFLDO3, DEFLDO4, EN_LDO1, EN_LDO2, EN_LDO3, EN_LDO4		1.2		V_{CC}	V
V_{IL}	Low-level input voltage	MODE, EN_DCDC1, EN_DCDC2, DEFLDO1, DEFLDO2, DEFLDO3, DEFLDO4, EN_LDO1, EN_LDO2, EN_LDO3, EN_LDO4, DEFDCDC2		0		0.4	V
I_{IB}	Input bias current	MODE = GND or V_I MODE, EN_DCDC1, EN_DCDC2, DEFDCDC2, DEFLDO1, DEFLDO2, DEFLDO3, DEFLDO4, EN_LDO1, EN_LDO2, EN_LDO3, EN_LDO4			0.01	1	μA
		V_FB_LDOx = 1 V, FB_LDO1, FB_LDO2, FB_LDO3, FB_LDO4				100	nA
POWER SWITCH							
$r_{DS(on)}$	P-channel MOSFET on-resistance	DCDC1	VINDCDC1/2 = 3.6 V		280	630	mΩ
			VINDCDC1/2 = 2.5 V		400		
		DCDC2	VINDCDC1/2 = 3.6 V		280	630	
			VINDCDC1/2 = 2.5 V		400		
I_{lkg}	P-channel leakage current	VDCDCx = $V_{(DS)}$ = 6 V				1	μA
$r_{DS(on)}$	N-channel MOSFET on-resistance	DCDC1	VINDCDC1/2 = 3.6 V		220	450	mΩ
			VINDCDC1/2 = 2.5 V		320		
		DCDC2	VINDCDC1/2 = 3.6 V		220	450	
			VINDCDC1/2 = 2.5 V		320		
I_{lkg}	N-channel leakage current	VDCDCx = $V_{(DS)}$ = 6 V			7	10	μA
$I_{(LIMF)}$	Forward current limit PMOS (high side) and NMOS (low side)	DCDC1, 2.5 V ≤ VINDCDC1/2 ≤ 6 V		1.19	1.4	1.65	A
		DCDC2, 2.5 V ≤ VINDCDC1/2 ≤ 6 V		0.85	1	1.15	
	Thermal shutdown	Increasing junction temperature			150		°C
	Thermal shutdown hysteresis	Decreasing junction temperature			20		°C
OUTPUT							
V_O	Output-voltage range for DCDC1, DCDC2			0.6		VINDCDC1/2	V
V_{ref}	Reference voltage				600		mV

Electrical Characteristics (continued)

V_{CC} = VINDCDC1/2 = 3.6 V, EN = V_{CC}, MODE = GND, L = 2.2 μH, C_O = 10 μF, T_A = –40°C to 125°C, typical values are at T_A = 25°C (unless otherwise noted).

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_O	DC output-voltage accuracy, DCDC1, DCDC2[1]	VINDCDC1/2 = 2.5 V to 6 V, 0 mA < I_O = < I_O(maximum) MODE = GND, PFM operation	–2%	0	2%	
		VINDCDC1/2 = 2.5 V to 6 V, 0 mA < I_O = < I_O(maximum) MODE = V_I, PWM operation	–1%	0	1%	
ΔV_O	Power-save-mode ripple voltage[2]	I_O = 1 mA, MODE = GND, V_O = 1.3 V, bandwith = 20 MHz		25		mV_{PP}
V_{OL}	$\overline{\text{RESET}}$, PB_OUT output low voltage	I_{OL} = 1 mA, Vhysteresis < 1 V, Vthreshold < 1 V			0.2	V
I_{OL}	$\overline{\text{RESET}}$, PB_OUT sink current			1		mA
	$\overline{\text{RESET}}$, PB_OUT output leakage current	After PB_IN has been pulled high once; Vthreshold > 1 V and Vhysteresis > 1 V, V_{OH} = 6 V		10		nA
V_{th}	Vthreshold, Vhysteresis threshold		0.98	1	1.02	V
VLDO1, VLDO2, VLDO3 AND VLDO4 LOW-DROPOUT REGULATORS						
V_I	Input-voltage range for LDO1, LDO2, LDO3, LDO4		1.5		6.5	V
$V_{(FB)}$	Feedback voltage for FB_LDO1, FB_LDO2, FB_LDO3, and FB_LDO4			1		V
I_O	Maximum output current for LDO1, LDO2		400			mA
	Maximum output current for LDO3, LDO4		200			
$I_{(SC)}$	LDO1 short-circuit current limit	VLDO1 = GND			750	mA
	LDO2 short-circuit current limit	VLDO2 = GND			850	
	LDO3 and LDO4 short-circuit current limit	VLDO3 = GND, VLDO4 = GND			420	
	Dropout voltage at LDO1	I_O = 400 mA, VINLDO = 3.4 V			400	mV
	Dropout voltage at LDO2	I_O = 400 mA, VINLDO = 1.8 V			280	
	Dropout voltage at LDO3, LDO4	I_O = 200 mA, VINLDO = 1.8 V			280	
I_{lkg}	Leakage current from VinLDOx to VLDOx	LDO enabled, VINLDO = 6.5 V, V_O = 1 V at T_A = 140°C		3		μA
V_O	Output voltage accuracy for LDO1, LDO2, LDO3, LDO4	I_O = 10 mA	–2%		1%	
	Line regulation for LDO1, LDO2, LDO3, LDO4	VINLDO1,2 = VLDO1,2 + 0.5 V (minimum 2.5 V) to 6.5 V, VINLDO3,4 = VLDO3,4 + 0.5 V (minimum 2.5 V) to 6.5 V, I_O = 10 mA	–1%		1%	
	Load regulation for LDO1, LDO2, LDO3, LDO4	I_O = 0 mA to 400 mA for LDO1, LDO2 I_O = 0 mA to 200 mA for LDO3, LDO4	–1%		1%	
PSRR	Power-supply rejection ratio	f = 10 kHz; I_O = 50 mA; V_I = V_O + 1 V		70		dB
$R_{(DIS)}$	Internal discharge resistor at VLDO1, VLDO2, VLDO3, VLDO4	Active when LDO is disabled		350		Ω
	Thermal shutdown	Increasing junction temperature		140		°C
	Thermal shutdown hysteresis	Decreasing junction temperature		20		°C

(1) Output voltage specification does not include tolerance of external voltage-programming resistors.
(2) In power-save mode, device typically enters operation at $I_{PSM} = V_I / 32\ \Omega$.

6.6 Switching Characteristics

V_{CC} = VINDCDC1/2 = 3.6 V, EN = V_{CC}, MODE = GND, L = 2.2 µH, C_O = 10 µF, T_A = –40°C to 125°C, typical values are at T_A = 25°C (unless otherwise noted).

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
OSCILLATOR						
f_{SW}	Oscillator frequency		2.025	2.25	2.475	MHz
OUTPUT						
t_{Start}	Start-up time	Time from active EN to start switching		170		µs
t_{Ramp}	VOUT ramp-up time	Time to ramp from 5% to 95% of V_O		750		µs
	$\overline{\text{RESET}}$ delay time	Input voltage at threshold pin rising	80	100	120	ms
	PB-ONOFF debounce time		26	32	38	ms
VLDO1, VLDO2, VLDO3 AND VLDO4 LOW-DROPOUT REGULATORS						
	Regulation time for LDO1, LDO2, LDO3, LDO4	Load change from 10% to 90%		10		µs

6.7 Typical Characteristics

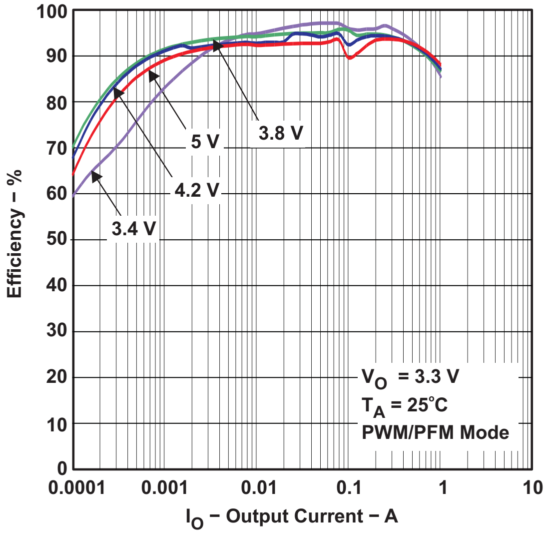


Figure 1. Efficiency vs Output Current

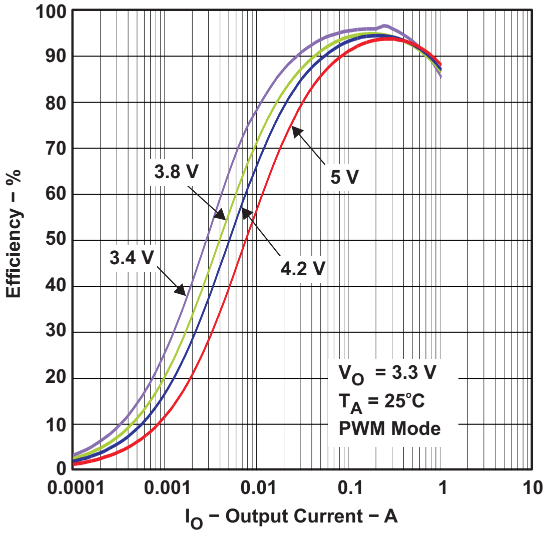


Figure 2. Efficiency vs Output Current

Typical Characteristics (continued)

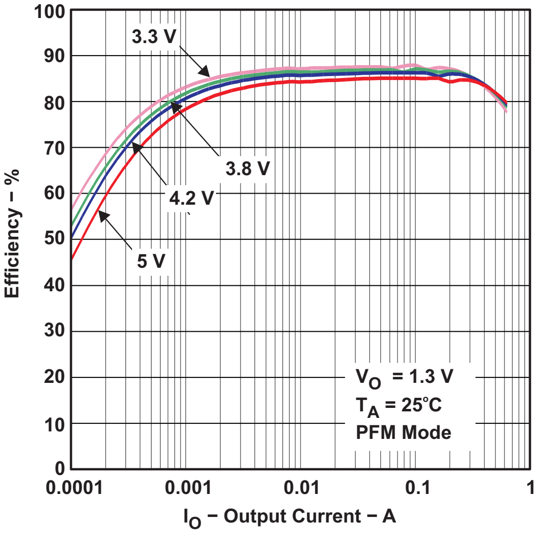


Figure 3. Efficiency vs Output Current

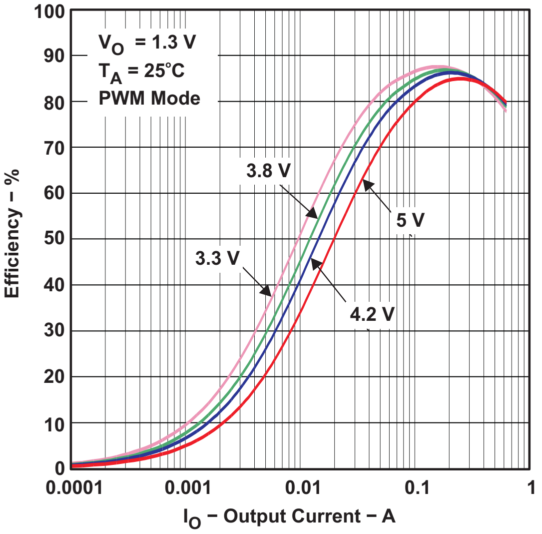


Figure 4. Efficiency vs Output Current

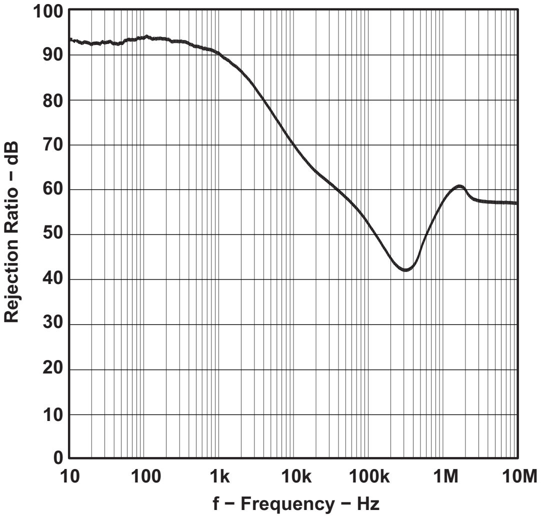


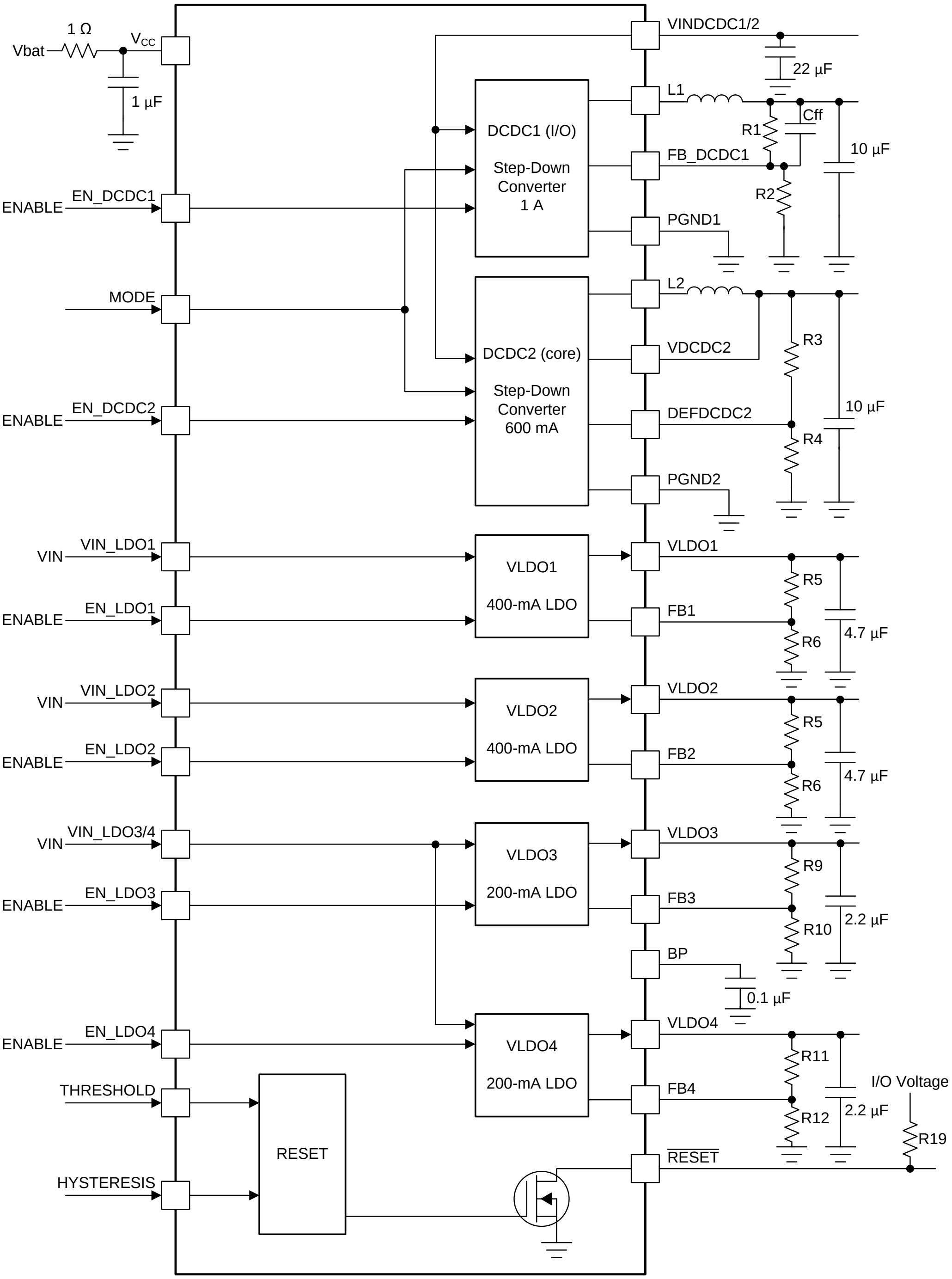
Figure 5. Power-Supply Rejection Ratio vs Frequency

7 Detailed Description

7.1 Overview

The TPS65051-Q1 device has 2 DC-DC buck converters and 4 LDOs. Each DC-DC and LDO has enable pins, allowing external sequence control of the PMU rails. The device also has a RESET feature that is generated from a THRESHOLD comparator. This RESET signal can be used to reset or warn of power shutdown to the embedded mircocontroller or processor. The TPS65051-Q1 device makes power-system integration easy for a variety of embedded processors or FPGAs.

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 Operation

The TPS65051-Q1 device has two synchronous step-down converters. The converters operate with 2.25-MHz (typical) fixed-frequency pulse-width modulation (PWM) at moderate to heavy load currents. At light load currents, the converters automatically enter power-save mode and operate with PFM (pulse-frequency modulation).

During PWM operation, the converters use a unique fast-response voltage-mode controller scheme with input voltage feed-forward to achieve good line and load regulation, allowing the use of small ceramic input and output capacitors. At the beginning of each clock cycle initiated by the clock signal, the P-channel MOSFET switch turns on, the inductor current ramps up until the current comparator trips, and the control logic turns off the switch. The current-limit comparator turns off the switch if the current exceeds the limit of the P-channel switch. After the adaptive dead time, which prevents shoot-through current, the N-channel MOSFET rectifier turns on, and the inductor current ramps down. The clock signal turning off the N-channel rectifier and turning on the on the P-channel switch initiates the next cycle.

The two DC-DC converters operate synchronized to each other, with converter 1 as the master. A 180° phase shift between converter 1 and converter 2 decreases the input rms current, allowing the use of smaller input capacitors.

7.3.2 DCDC1 Converter

An external resistor divider connected to FB_DCDC1 pin sets the converter 1 output voltage. See the *Converter 1 (DCDC1)* section for more details. The maximum output current is 1 A.

7.3.3 DCDC2 Converter

Connect the VDCDC2 pin directly to the DCDC2 converter output voltage. The DEFDCDC2 pin selects the DCDC2 converter output voltage. See the *Converter 2 (DCDC2)* section for more details. The maximum output current is 600 mA.

An external resistor divider sets the output voltage. Connect the DEFDCDC2 pin to the external resistor divider.

7.3.4 Dynamic Voltage Positioning

This feature reduces the voltage under- and overshoots at load steps from light to heavy load and vice versa. It is activated In the power-save mode of operation, running the converter in PFM mode activates dynamic voltage positioning. Dynamic voltage positioning provides more headroom for both the voltage drop at a load step and the voltage increase at a load throw-off, thereby improving load-transient behavior.

At light loads, in which the converters operate in PFM mode, the typical output-voltage regulation is 1% higher than the nominal value. In the event of a load transient from light load to heavy load, the output voltage drops until it reaches the skip-comparator-low threshold, set to 1% below the nominal value, and enters PWM mode. During a release from heavy load to light load, active regulation turning on the N-channel switch minimizes the voltage overshoot.

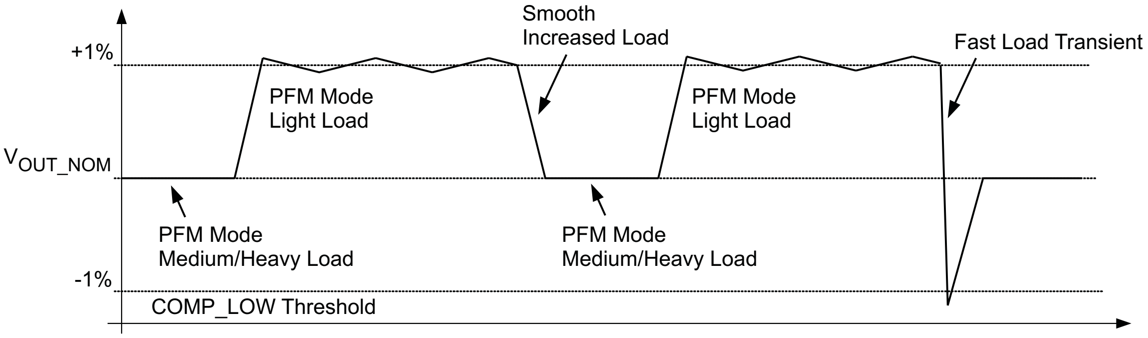


Figure 6. Dynamic Voltage Positioning

Feature Description (continued)

7.3.5 Soft Start

The two converters have an internal soft-start circuit that limits the inrush current during start-up. During soft start, control of the output-voltage ramp-up is as shown in Figure 7.

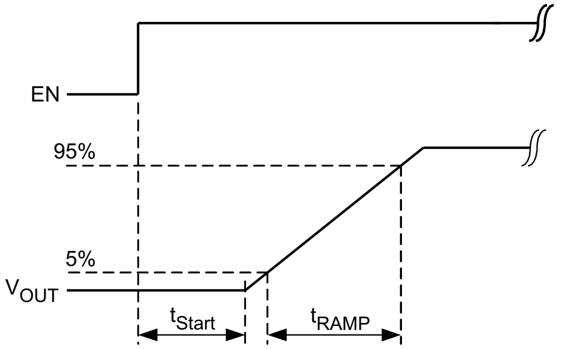


Figure 7. Soft Start

7.3.6 100% Duty-Cycle Low-Dropout Operation

The converters offer a low input-to-output voltage difference while still maintaining operation with the use of the 100% duty-cycle mode. In this mode, the P-channel switch is constantly on. This operational mode is useful in battery-powered applications to achieve longest operation time by taking full advantage of the whole battery voltage range, (that is, the minimum input voltage to maintain regulation depends on the load current and output voltage) and can be calculated as:

$$V_I\,(\text{min}) = V_O\,(\text{max}) + I_O\,(\text{max}) \times (r_{DS(on)}\,(\text{max}) + R_L)$$

where

- I_O max = maximum output current plus inductor ripple current
- $r_{DS(on)}$ max = maximum P-channel switch $r_{DS(on)}$
- R_L = dc resistance of the inductor
- V_O (max) = nominal output voltage plus maximum output-voltage tolerance (1)

7.3.7 Undervoltage Lockout

The undervoltage-lockout circuit prevents the device from malfunctioning at low input voltages and from excessive discharge of the battery, and disables all internal circuitry. The undervoltage-lockout threshold, sensed at the V_{CC} pin, is typically 1.8 V, maximum 2 V.

7.3.8 Mode Selection

The MODE pin allows mode selection between forced PWM mode and power-save mode for both converters. Connecting this pin to GND enables the automatic PWM and power-save mode of operation. The converters operate in fixed-frequency PWM mode at moderate-to-heavy loads and in the PFM mode during light loads, maintaining high efficiency over a wide load-current range.

Pulling the MODE pin high forces both converters to operate constantly in the PWM mode even at light load currents. The advantage is the converters operate with a fixed frequency that allows simple filtering of the switching frequency for noise-sensitive applications. In this mode, the efficiency is lower compared to the power-save mode during light loads. For additional flexibility, it is possible to switch from power-save mode to forced-PWM mode during operation. This allows efficient power management by adjusting the operation of the converters to the specific system requirements.

7.3.9 Enable

To start up each converter independently, the device has a separate enable pin for each DC-DC converter and for each LDO. If EN_DCDC1, EN_DCDC2, EN_LDO1, EN_LDO2, EN_LDO3, or EN_LDO4 is set to high, the corresponding converter starts up with soft start as previously described.

Feature Description (continued)

Pulling the enable pin low forces the device into shutdown, with a shutdown quiescent current as defined in the electrical characteristics. In this mode, the P- and N-Channel MOSFETs turn off, and the entire internal control circuitry switches off. If disabled, internal 350-Ω resistors pull the outputs of the LDOs low, actively discharging the output capacitor. Proper operation requires termination of the enable pins. Do not leave them unconnected.

7.3.10 $\overline{\text{RESET}}$

The device contains circuitry that can generate a reset pulse for a processor with a 100-ms delay time. The device senses the input voltage for a comparator at the THRESHOLD pin. When the voltage exceeds the threshold, the output goes high with a 100-ms delay time. An external resistor connected to the HYSTERESIS input defines the hysteresis. This circuitry is functional as soon as the supply voltage at V_{CC} exceeds the undervoltage-lockout threshold. The TPS65051-Q1 device has a shutdown current (all DC-DC converters and LDOs are off) of 9 μA.

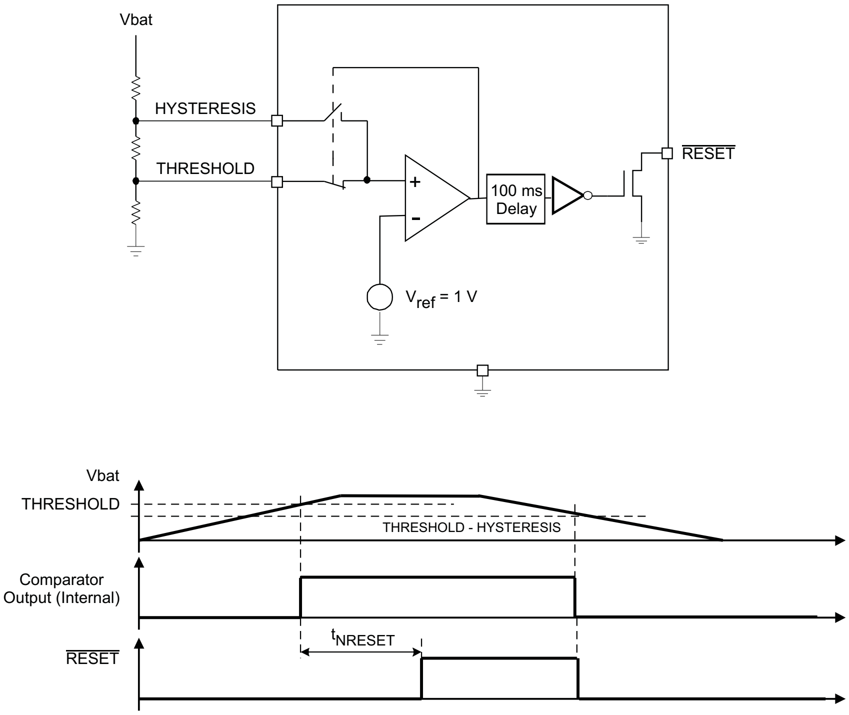


Figure 8. $\overline{\text{RESET}}$ Pulse Circuit

7.3.11 Short-Circuit Protection

All outputs are short-circuit protected with a maximum output current as defined in the *Electrical Characteristics*.

7.3.12 Thermal Shutdown

As soon as the junction temperature, T_J, exceeds 150°C (typically) for the DC-DC converters, the device goes into thermal shutdown. In this mode, the P- and N-channel MOSFETs turn off. The device continues its operation when the junction temperature falls below the thermal shutdown hysteresis again. A thermal shutdown for one of the DC-DC converters disables both converters simultaneously.

The thermal shutdown temperature for the LDOs is typically 140°C. Therefore, an LDO used to power an external voltage never heats up the chip high enough to turn off the DC-DC converters. If one LDO exceeds the thermal shutdown temperature, all LDOs turn off simultaneously.

Feature Description (continued)

7.3.13 Low Dropout Voltage Regulators

The design of the low-dropout voltage regulators allows them to operate well with small ceramic input and output capacitors. They operate with input voltages down to 1.5 V. The LDOs offer a maximum dropout voltage of 400 mV (LDO1) and 280 mV (LDO2, LDO3, and LDO4) at rated output current. Each LDO supports a current-limit feature. The EN_LDO1, ENLDO2, EN_LDO3, and EN_LDO4 pins enable the LDOs. The use of external resistor dividers sets the output voltage of the LDOs.

7.4 Device Functional Modes

7.4.1 Power-Save Mode

The TPS65051-Q1 device is either in the ON or the OFF mode. The OFF mode is entered when the voltage on V_{CC} is below the UVLO threshold of 1.8 V (typically). When the voltage at the V_{CC} pin is higher than UVLO, the device enters ON mode. In the ON mode, the converters and LDOs are available for use.

Setting the MODE pin to 0 enables the power-save mode. If the load current decreases, the converters enter the power-save mode of operation automatically. During power-save mode, the converters operate with reduced switching frequency in PFM mode, and with a minimum quiescent current to maintain high efficiency. The converters position the output voltage 1% above the nominal output voltage. This voltage-positioning feature minimizes voltage drops caused by a sudden load step.

To optimize the converter efficiency at light load, the TPS65051-Q1 device monitors average current. If in PWM mode, the inductor current remains below a certain threshold, then the device enters power-save mode. Use Equation 2 to calculate the average output current threshold to enter PFM mode. Use Equation 3 to calculate the average output current threshold to leave PFM mode.

$$I_{(PFM\_enter)} = \frac{VINDCDC}{32\ \Omega} \tag{2}$$

$$I_{(PSMDCDC\_leave)} = \frac{VINDCDC}{24\ \Omega} \tag{3}$$

During power-save mode, a comparator monitors the output voltage. As the output voltage falls below the skip-comparator (skip comp) threshold, the P-channel switch turns on, and the converter effectively delivers a constant current. If the load is below the delivered current, the output voltage rises until it crosses the skip comp threshold again; then all switching activity ceases, reducing the quiescent current to a minimum until the output voltage has dropped below the threshold. If the load current is greater than the delivered current, the output voltage falls until it crosses the skip-comparator-low (skip comp low) threshold set to 1% below nominal V_O; then the device exits power-save mode, and the converter returns to the PWM mode.

These control methods reduce the quiescent current to 12 µA per converter and the switching frequency to a minimum, achieving the highest converter efficiency. The PFM mode operates with low output-voltage ripple. The ripple depends on the comparator delay and the size of the output capacitor; increasing capacitor value decreases the output ripple voltage.

Disable the power-save mode by driving the MODE pin high. In forced-PWM mode, both converters operate with fixed-frequency PWM mode regardless of the load.

8 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

This device integrates two step-down converters and four LDOs, which can be used to power the voltage rails needed by a processor or any other application. The power management IC (PMIC) can be controlled through the ENABLE and MODE pins or sequenced from the VIN using RC delay circuits. A logic output (RESET) provides the application processor or load a logic signal indicating power good or reset.

8.2 Typical Application

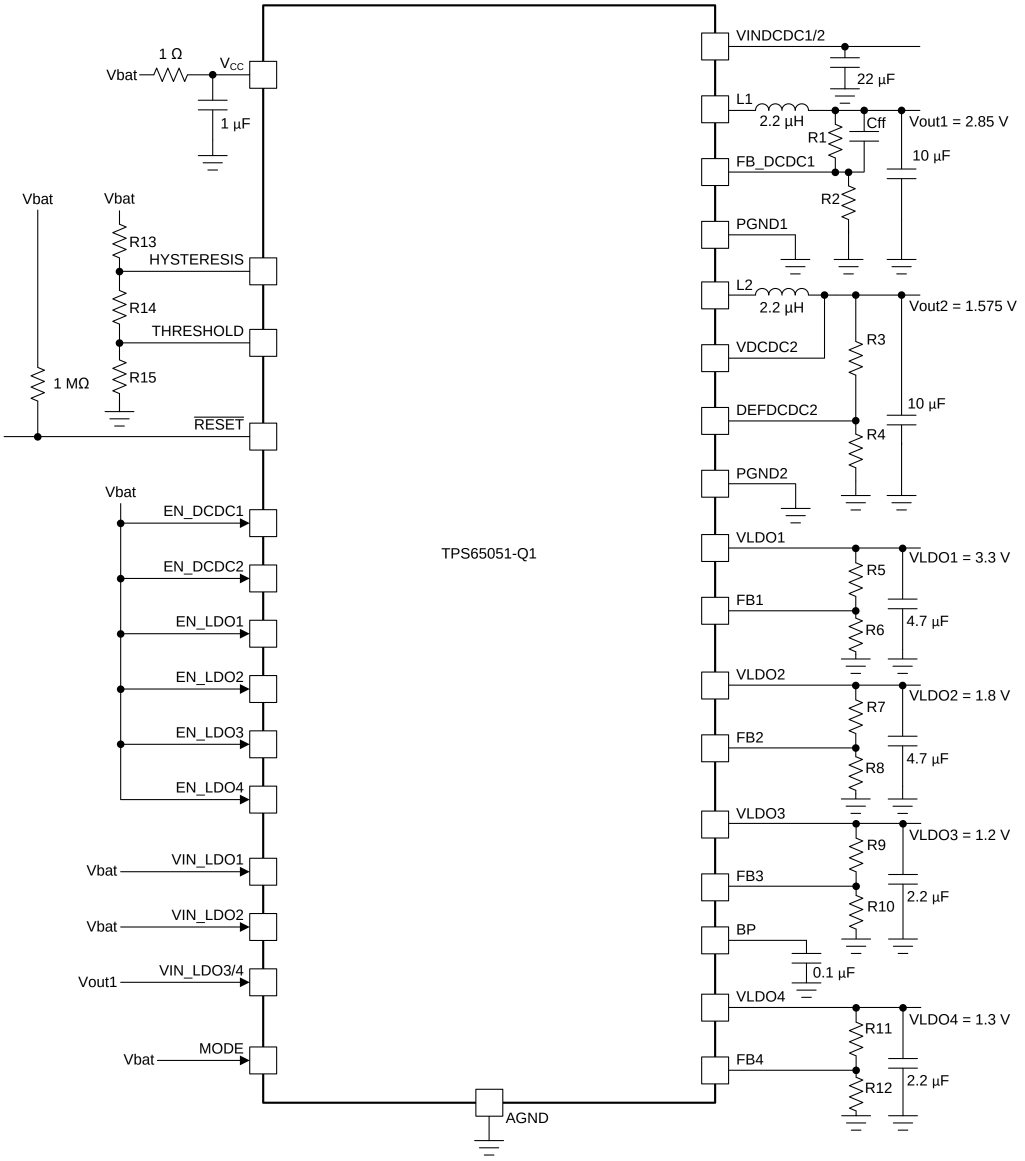


Figure 9. Typical Application Schematic

Typical Application (continued)

8.2.1 Design Requirements

Table 1 lists the design requirements for this example.

Table 1. Design Parameters

PARAMETER	VALUE
DCDC1 and DCDC2 input voltage	2.5 V to 6 V
DCDC1 output voltage	2.85 V
DCDC1 output current	1 A
DCDC2 output voltage	1.575 V
DCDC2 output current	600 mA
LDO1 output voltage	3.3 V
LDO1 output current	400 mA
LDO2 output voltage	1.8 V
LDO2 output current	400 mA
LDO3 output voltage	1.2 V
LDO3 output current	200 mA
LDO4 output voltage	1.3 V
LDO4 output current	200 mA

8.2.2 Detailed Design Procedure

8.2.2.1 Output-Voltage Setting

8.2.2.1.1 Converter 1 (DCDC1)

An external resistor network can set the output voltage of converter 1. Calculate the output voltage using Equation 4,

$$V_O = V_{ref} \times \left(1 + \frac{R1}{R2}\right)$$

where

- the internal reference voltage, V_{ref}, is 0.6 V (4)

TI recommends setting the total resistance of R1 + R2 to less than 1 MΩ. The resistor network connects to the input of the feedback amplifier, therefore requiring a small feed-forward capacitor in parallel with R1. A typical value of 47 pF is sufficient.

8.2.2.1.2 Converter 2 (DCDC2)

The adjustable output voltage is defined with external resistor network on the DEFDCDC2 pin.

Calculation of the adjustable output voltage is similar to that for the DCDC1 converter. TI recommends setting the total resistance of R3 + R4 to less than 1 MΩ. Route the DEFDCDC2 line separate from noise sources, such as the inductor or the L2 line. Connect the VDCDC2 line directly to the output capacitor. As VDCDC2 is the sense pin for the output of L2, there is no need for a feedforward capacitor in conjunction with R3.

Use an external resistor divider at DEFDCDC2 as shown in Figure 10.

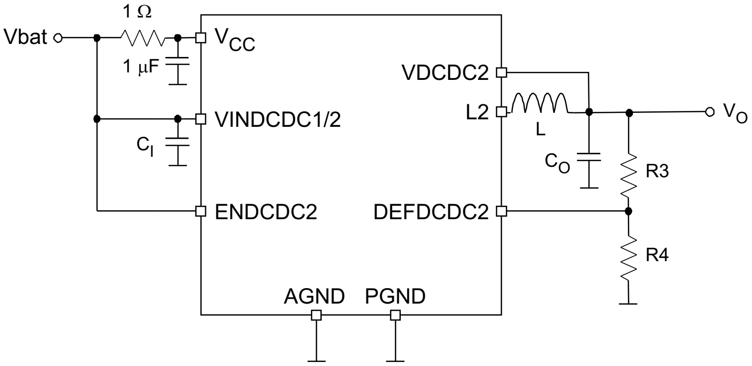


Figure 10. External Resistor Divider

$V_{(DEFDCDC2)} = 0.6\ V$

$$V_O = V_{(DEFDCDC2)} \times \frac{R3 + R4}{R4} \qquad R3 = R4 \times \left(\frac{V_O}{V_{(DEFDCDC2)}} \right) - R4 \tag{5}$$

See Table 2 for typical resistor values:

Table 2. Typical Resistor Values

OUTPUT VOLTAGE	R3	R4	NOMINAL VOLTAGE	Typical CFF
3.3 V	680 kΩ	150 kΩ	3.32 V	47 pF
3 V	510 kΩ	130 kΩ	2.95 V	47 pF
2.85 V	560 kΩ	150 kΩ	2.84 V	47 pF
2.5 V	510 kΩ	160 kΩ	2.51 V	47 pF
1.8 V	300 kΩ	150 kΩ	1.8 V	47 pF
1.6 V	200 kΩ	120 kΩ	1.6 V	47 pF
1.5 V	300 kΩ	200 kΩ	1.5 V	47 pF
1.2 V	330 kΩ	330 kΩ	1.2 V	47 pF

8.2.2.2 Output Filter Design (Inductor and Output Capacitor)

8.2.2.2.1 Inductor Selection

The two converters operate with a 2.2-µH output inductor. A designer can use larger or smaller inductor values to optimize the performance of the device for specific operation conditions. The selected inductor must be rated for its dc resistance and saturation current. The dc resistance of the inductance directly influences the efficiency of the converters. Therefore, select an inductor with lowest dc resistance for highest efficiency. The minimum inductor value is 1.5 µH, but the circuit requires an output capacitor of 22 µF minimum in this case. For an output voltage above 2.8 V, TI recommends an inductor value of 3.3 µH minimum. Lower values result in an increased output-voltage ripple in PFM mode.

Equation 6 calculates the maximum inductor current under static load conditions. The saturation-current rating of the inductor should be higher than the maximum inductor current as calculated with Equation 6. This recommendation is because during heavy load transient the inductor current rises above the calculated value.

$$\Delta I_L = V_O \times \frac{1 - \frac{V_O}{V_I}}{L \times f} \qquad I_L(\text{max}) = I_O(\text{max}) + \frac{\Delta I_L}{2}$$

where

- f = Switching frequency (2.25-MHz typical)
- L = Inductor value
- Δ I_L= Peak-to-peak inductor ripple current
- $I_L$max = Maximum inductor current (6)

The highest inductor current occurs at maximum V_I. Open-core inductors have a soft saturation characteristic, and they can normally handle higher inductor currents versus a comparable shielded inductor.

A more-conservative approach is to select the inductor current rating just for the maximum switch current of the corresponding converter. Give consideration to the difference in the core material from inductor to inductor, which has an impact on the efficiency, especially at high switching frequencies. See Table 3 and the typical applications for possible inductors.

Table 3. Tested Inductors

INDUCTOR TYPE	INDUCTOR VALUE	SUPPLIER
LPS3010	2.2 µH	Coilcraft
LPS3015	3.3 µH	Coilcraft
LPS4012	2.2 µH	Coilcraft
VLF4012	2.2 µH	TDK

8.2.2.2.2 Output-Capacitor Selection

The advanced fast-response voltage-mode control scheme of the two converters allows the use of small ceramic capacitors with a value of 22-µF (typical), without having large output-voltage undershoots and overshoots during heavy load transients. TI recommends ceramic capacitors having low ESR values, which result in the lowest output-voltage ripple.

If ceramic output capacitors are used, the capacitor RMS ripple current rating always meets the application requirements. For completeness, the RMS ripple current is calculated as:

$$I_{(RMSCout)} = V_O \times \frac{1 - \frac{V_O}{V_I}}{L \times f} \times \frac{1}{2 \times \sqrt{3}} \tag{7}$$

At nominal load current, the inductive converters operate in PWM mode, and the overall output voltage ripple is the sum of the voltage spike caused by the output-capacitor ESR plus the voltage ripple caused by charging and discharging the output capacitor:

$$\Delta V_O = V_O \times \frac{1 - \frac{V_O}{V_I}}{L \times f} \times \left(\frac{1}{8 \times C_O \times f} + ESR \right) \tag{8}$$

where the highest output voltage ripple occurs at the highest input voltage V_I.

At light load currents, the converters operate in power-save mode and the output-voltage ripple depends on the output-capacitor value. The internal comparator delay and the external capacitor set the output-voltage ripple. The typical output-voltage ripple is less than 1% of the nominal output voltage.

8.2.2.2.3 Input-Capacitor Selection

The nature of the buck converters having a pulsating input current requires a low-ESR input capacitor for best input-voltage filtering and minimizing the interference with other circuits caused by high input-voltage spikes. The converters require a ceramic input capacitor of 10 µF. Increase the input capacitor as desired for better input-voltage filtering, without any limit.

Table 4. Possible Capacitors

CAPACITOR VALUE	SIZE	SUPPLIER	TYPE
2.2 µF	0805	TDK C2012X5R0J226MT	Ceramic
2.2 µF	0805	Taiyo Yuden JMK212BJ226MG	Ceramic
10 µF	0805	Taiyo Yuden JMK212BJ106M	Ceramic
10 µF	0805	TDK C2012X5R0J106M	Ceramic
10 µF	0603	Taiyo Yuden JMK107BJ106MA	Ceramic

8.2.2.3 Low-Dropout Voltage Regulators (LDOs)

An external resistor network sets the output voltage of all four LDOs. Calculate the output voltage using Equation 9:

$$V_O = V_{ref} \times \left(1 + \frac{R5}{R6}\right)$$

where

- the internal reference voltage, V_{ref}, is 1 V (typical). (9)

TI recommends setting the total resistance of R5 + R6 to less than 1 MΩ. Typically, there is no feedforward capacitor needed at the voltage dividers for the LDOs.

$$V_O = V_{(FB\_LDOs)} \times \frac{R5 + R6}{R6} \qquad R5 = R6 \times \left(\frac{V_O}{V_{(FB\_LDOs)}}\right) - R6 \tag{10}$$

Typical resistor values:

Table 5. Typical Resistor Values

OUTPUT VOLTAGE	R5	R6	NOMINAL VOLTAGE
3.3 V	300 kΩ	130 kΩ	3.31 V
3 V	300 kΩ	150 kΩ	3 V
2.85 V	240 kΩ	130 kΩ	2.85 V
2.8 V	360 kΩ	200 kΩ	2.8 V
2.5 V	300 kΩ	200 kΩ	2.5 V
1.8 V	240 kΩ	300 kΩ	1.8 V
1.5 V	150 kΩ	300 kΩ	1.5 V
1.3 V	36 kΩ	120 kΩ	1.3 V
1.2 V	100 kΩ	510 kΩ	1.19 V
1.1 V	33 kΩ	330 kΩ	1.1 V

8.2.2.4 $\overline{\text{RESET}}$

The device contains a comparator for supervising a voltage connected to an external voltage divider, and generating a reset signal if the voltage is lower than the threshold. The rising-edge delay is 100 ms at the open-drain $\overline{\text{RESET}}$ output. Calculate the values for the external resistors R13 to R15 as follows:

V_L = lower voltage threshold

V_H = higher voltage threshold

V_{REF} = reference voltage (1 V)

Example:

- V_L = 3.3 V
- V_H = 3.4 V

  Set R15 = 100 kΩ

  → R13 + R14 = 240 kΩ

  → R14 = 3.03 kΩ

  → R13 = 237 kΩ

$$R13 + R14 = R15 \times \left(\frac{V_H}{V_{ref}} - 1 \right)$$

$$R14 = R15 \times \frac{V_H - V_L}{V_L} \tag{11}$$

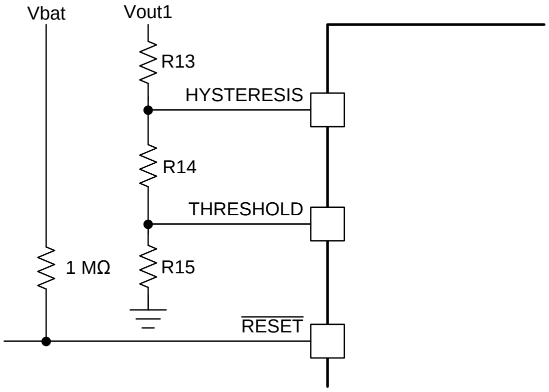


Figure 11. $\overline{\text{RESET}}$ Circuit

8.2.3 Application Curves

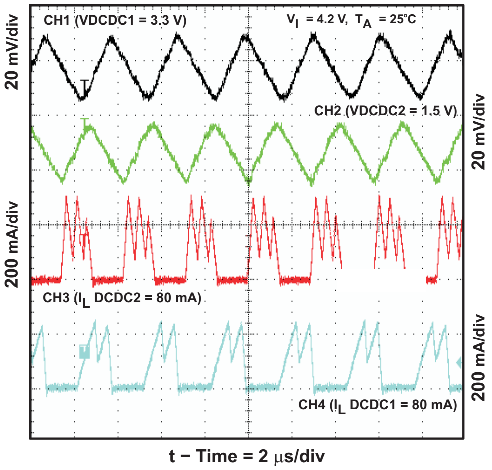


Figure 12. Output Voltage Ripple PWM or PFM MODE = LOW

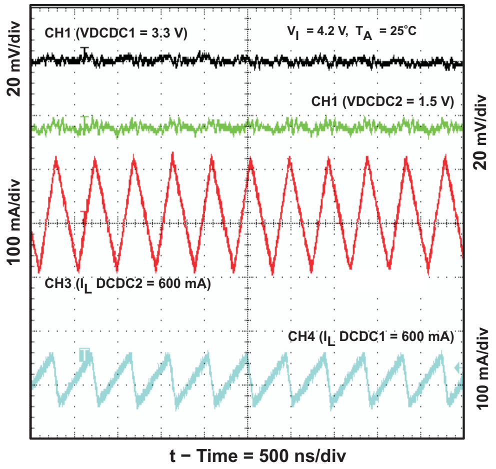


Figure 13. Output Voltage Ripple PWM MODE = HIGH

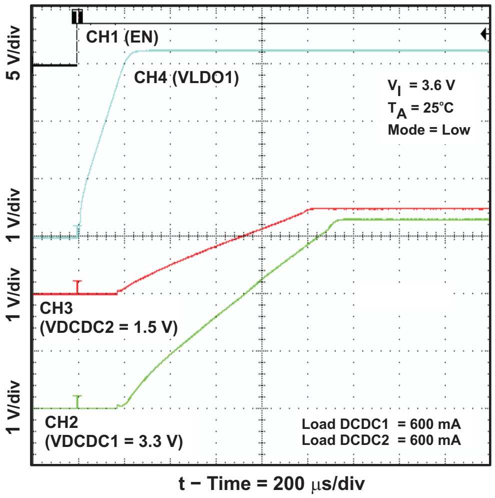


Figure 14. DCDC1 Startup Timing

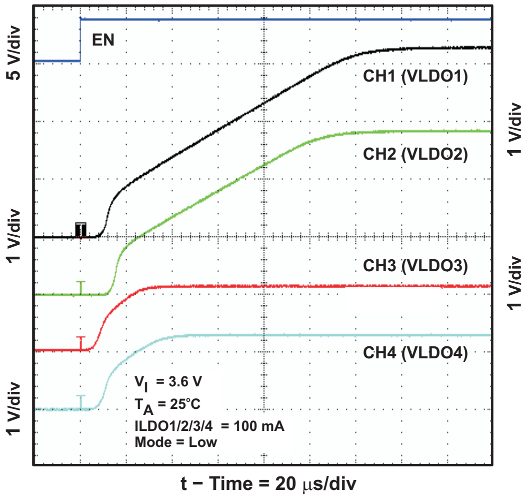


Figure 15. LDO1 to LDO4 Startup Timing

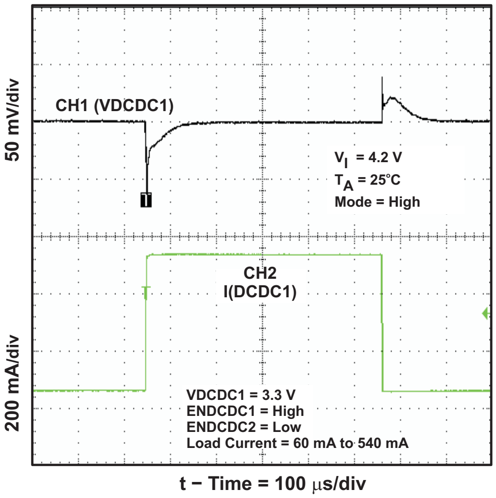


Figure 16. DCDC1 Load Transient Response

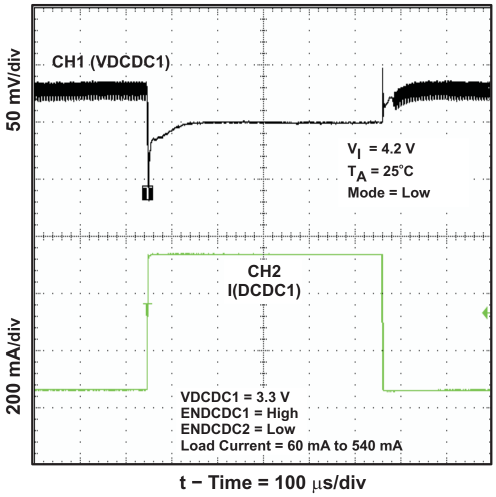


Figure 17. DCDC1 Load Transient Response

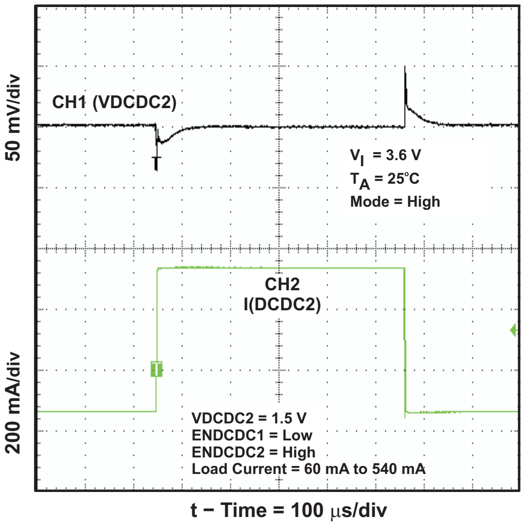


Figure 18. DCDC2 Load Transient Response

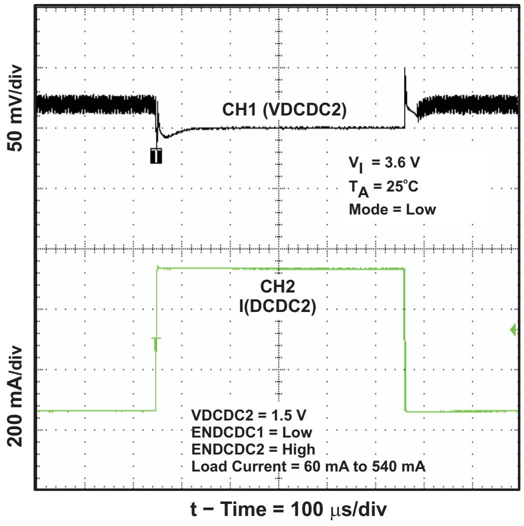


Figure 19. DCDC2 Load Transient Response

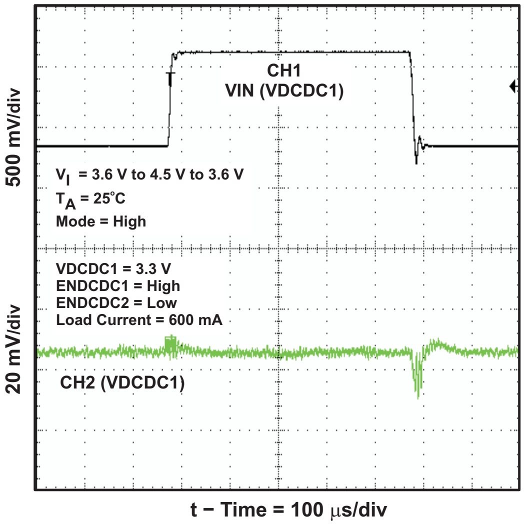


Figure 20. DCDC1 Line Transient Response

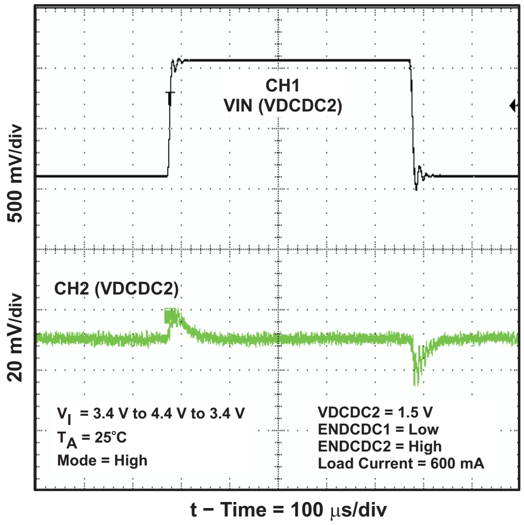


Figure 21. DCDC2 Line Transient Response

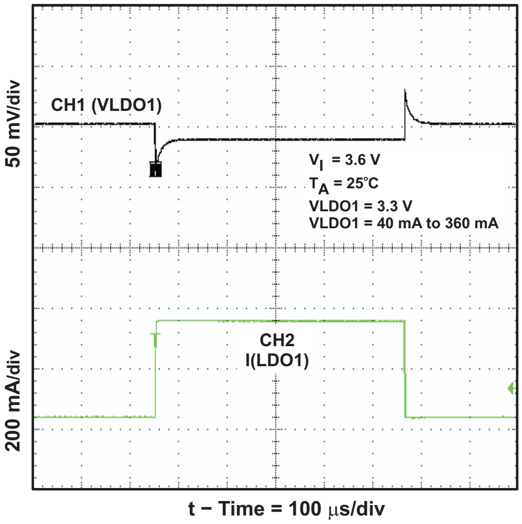


Figure 22. LDO1 Load Transient Response

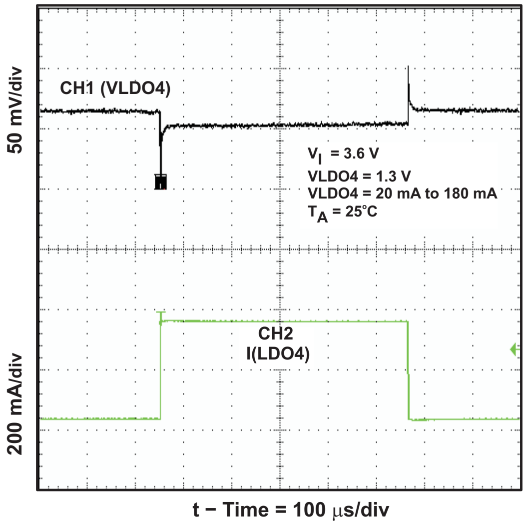


Figure 23. LDO4 Load Transient Response

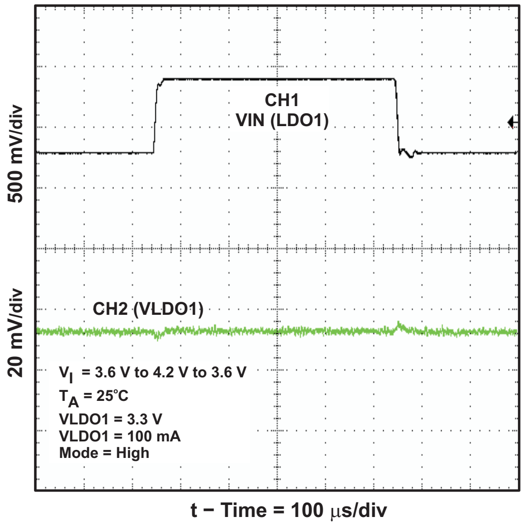


Figure 24. LDO1 Line Transient Response

9 Power Supply Recommendations

In addition to the values listed in the *Recommended Operating Conditions* table, additional recommendations for the power supply are as follows:

- 1-µF bypass capacitor on V_{CC}, located as close as possible to the V_{CC} pin to ground.
- V_{CC} and VINDCDC1/2 must be connected to the same voltage supply with minimal voltage difference.
- Input capacitors must be present on the VINDCDC1/2, VIN_LDO1, VINLDO2, and VIN_LDO3/4 supplies if used.
- Output inductor and capacitors must be used on the outputs of the DC-DC converters if used.
- Output capacitors must be used on the outputs of the LDOs if used.

10 Layout

10.1 Layout Guidelines

- The input capacitors for the DC-DC converters should be placed as close as possible to the VINDCDC1/2 pin and the PGND1 and PGND2 pins.
- The inductor of the output filter should be placed as close as possible to the device to provide the shortest switch node possible, reducing the noise emitted into the system and increasing the efficiency.
- Sense the feedback voltage from the output at the output capacitors to ensure the best DC accuracy. Feedback should be routed away from noisy sources such as the inductor. If possible route on the opposing side as the switch node and inductor and place a GND plane between the feedback and the noisy sources or keep out underneath them entirely.
- Place the output capacitors as close as possible to the inductor to reduce the feedback loop as much as possible. This will ensure best regulation at the feedback point.
- Place the device as close as possible to the most demanding or sensitive load. The output capacitors should be placed close to the input of the load. This will ensure the best AC performance possible.
- The input and output capacitors for the LDOs should be placed close to the device for best regulation performance.
- TI recommends using the common ground plane for the layout of this device. The AGND can be separated from the PGND but, a large low parasitic PGND is required to connect the PGNDx pins to the CIN and external PGND connections. If the AGND and PGND planes are separated, have one connection point to reference the grounds together. Place this connection point close to the IC.

10.2 Layout Example

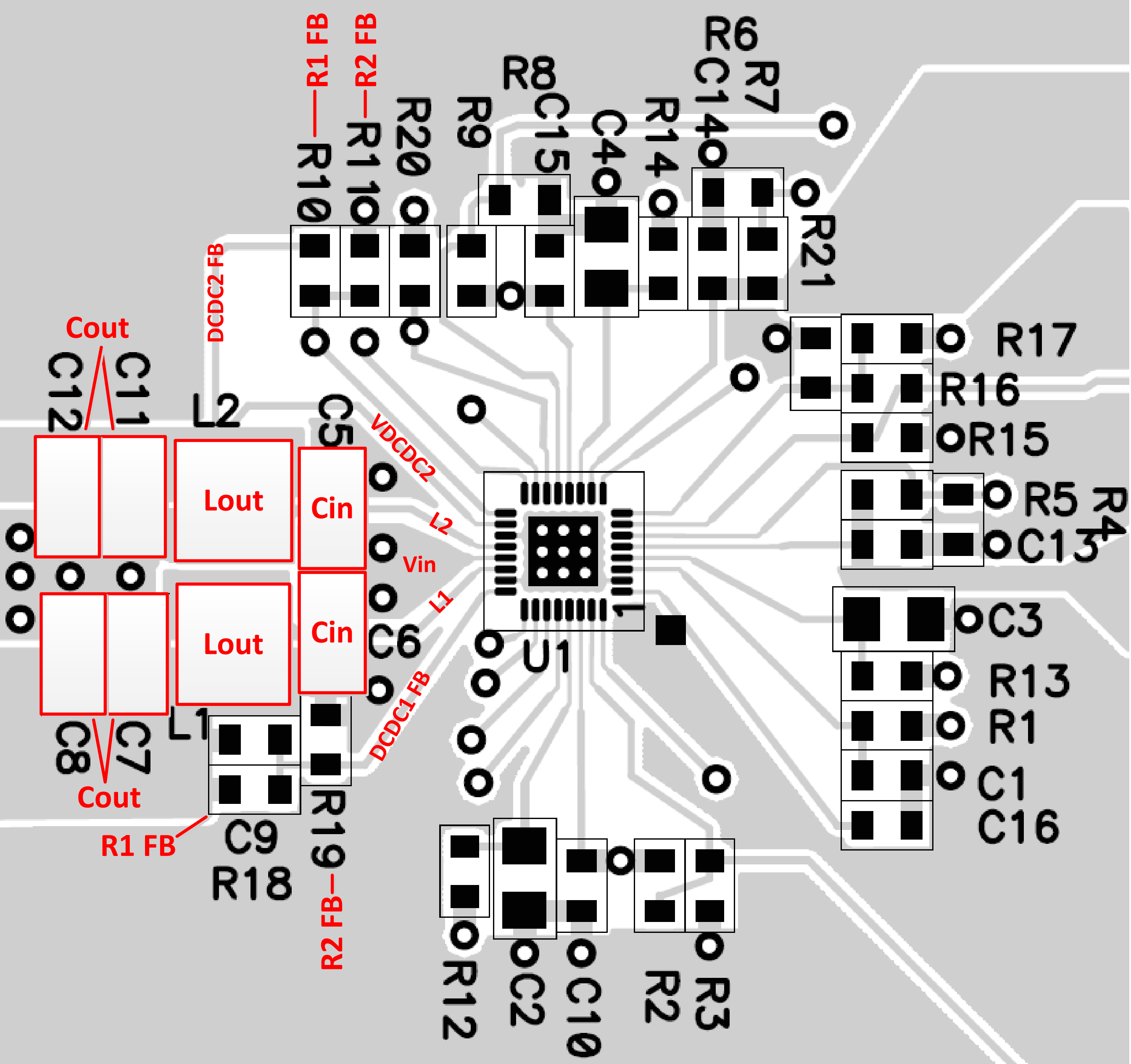


Figure 25. Layout Example from EVM for TPS65051-Q1

11 Device and Documentation Support

11.1 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

11.2 Community Resource

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

11.3 Trademarks

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11.4 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

11.5 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPS65051QRSMRQ1	ACTIVE	VQFN	RSM	32	3000	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-40 to 125	TPS 65051Q	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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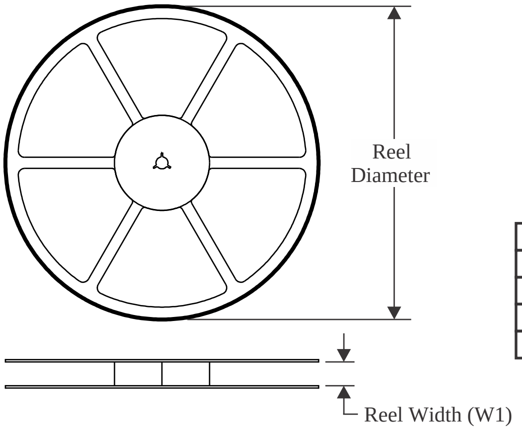
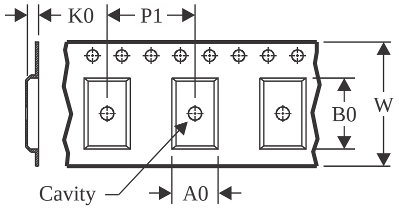
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

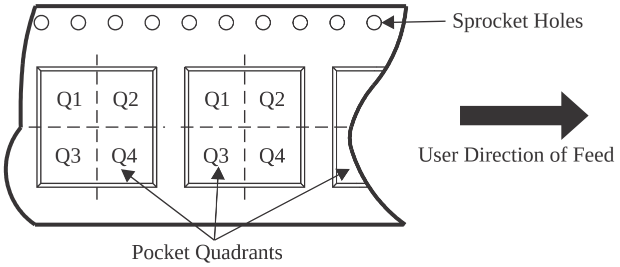


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

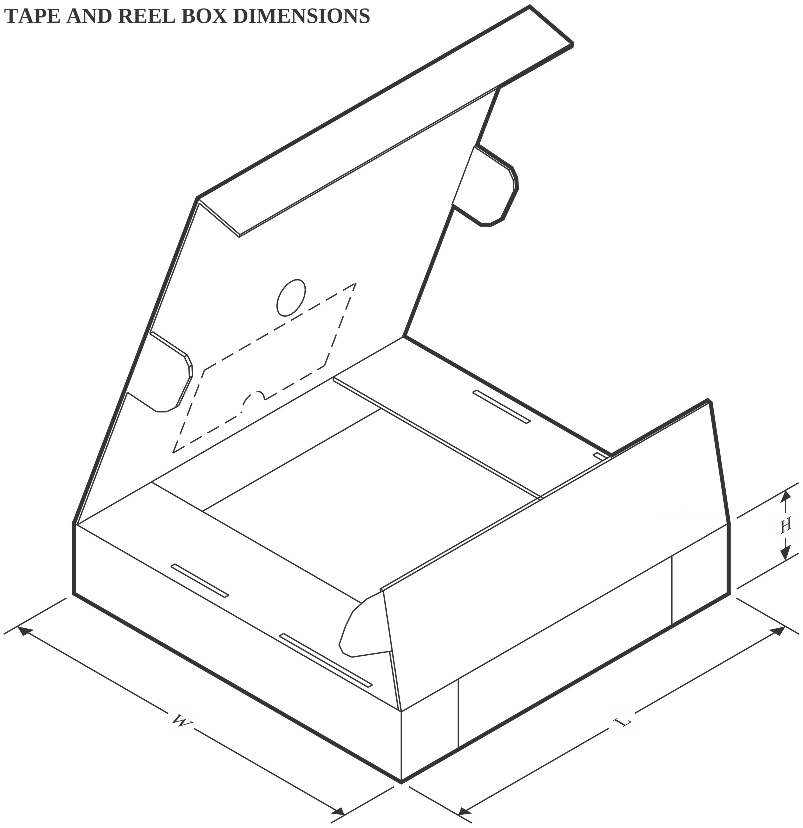
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS65051QRSMRQ1	VQFN	RSM	32	3000	330.0	12.4	4.25	4.25	1.15	8.0	12.0	Q2

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS65051QRSMRQ1	VQFN	RSM	32	3000	356.0	356.0	35.0

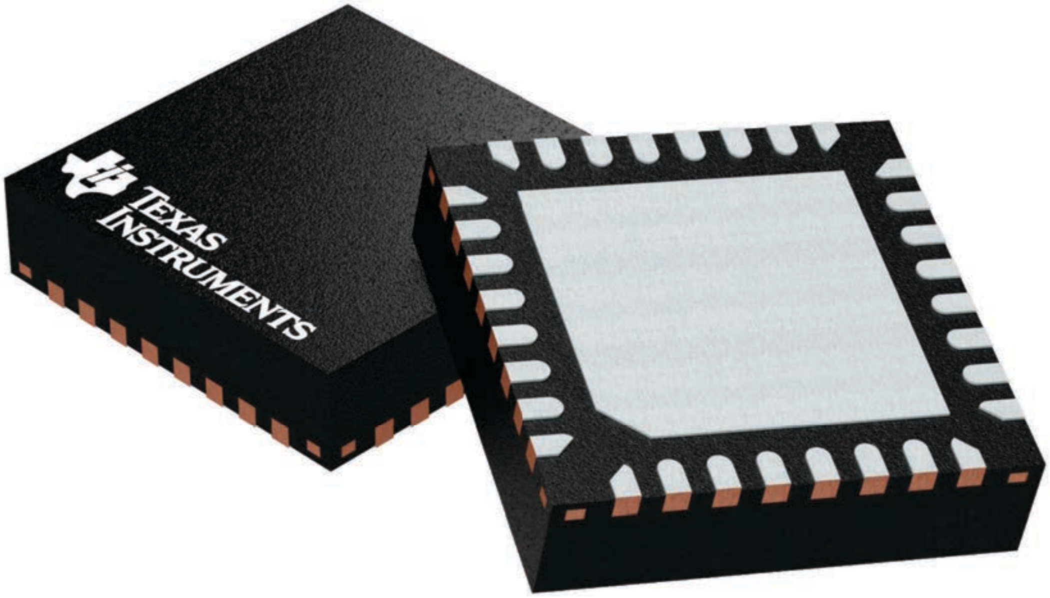
RSM 32

VQFN - 1 mm max height

4 x 4, 0.4 mm pitch

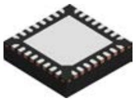
PLASTIC QUAD FLATPACK - NO LEAD

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



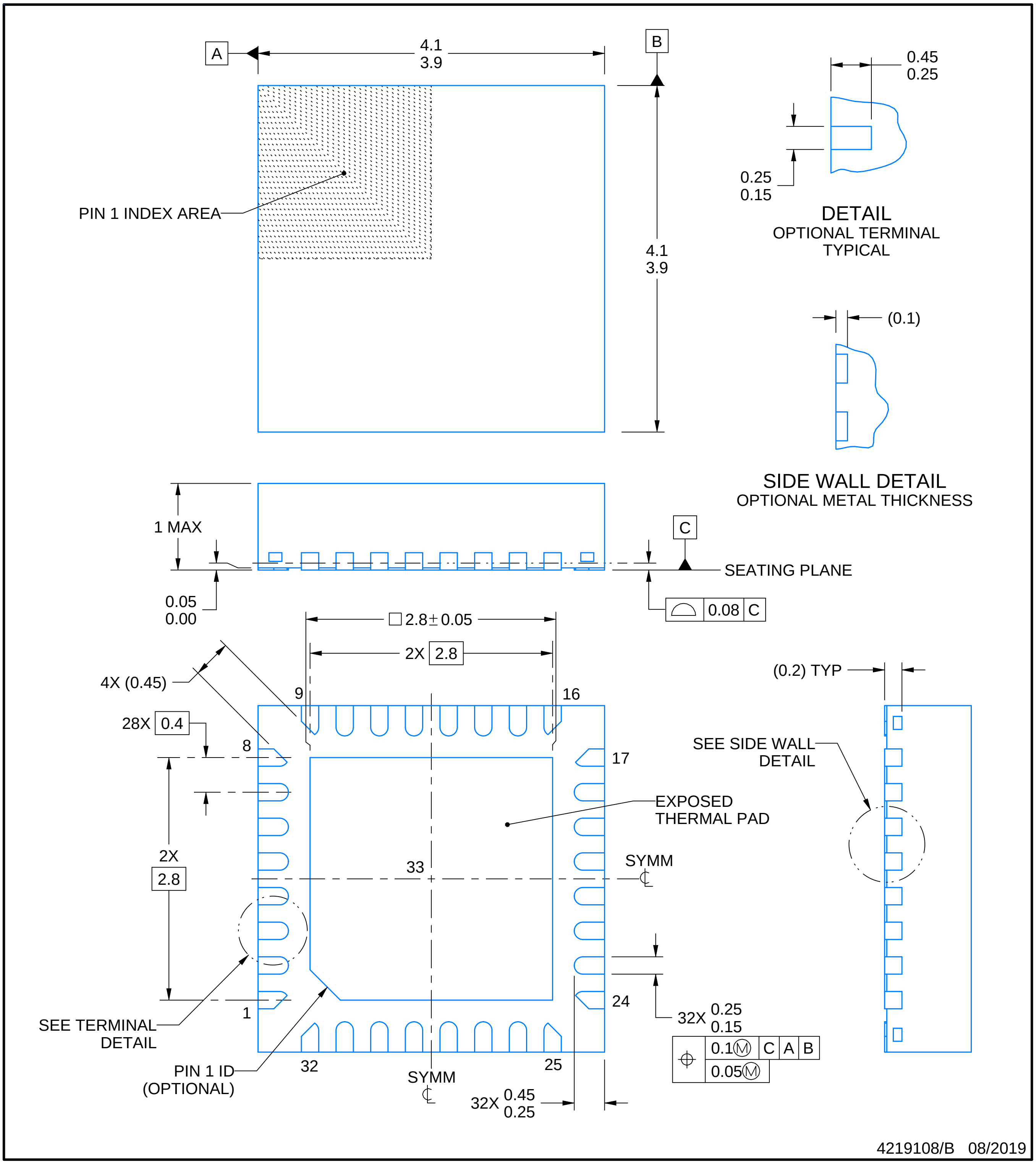
PACKAGE OUTLINE

RSM0032B



VQFN - 1 mm max height

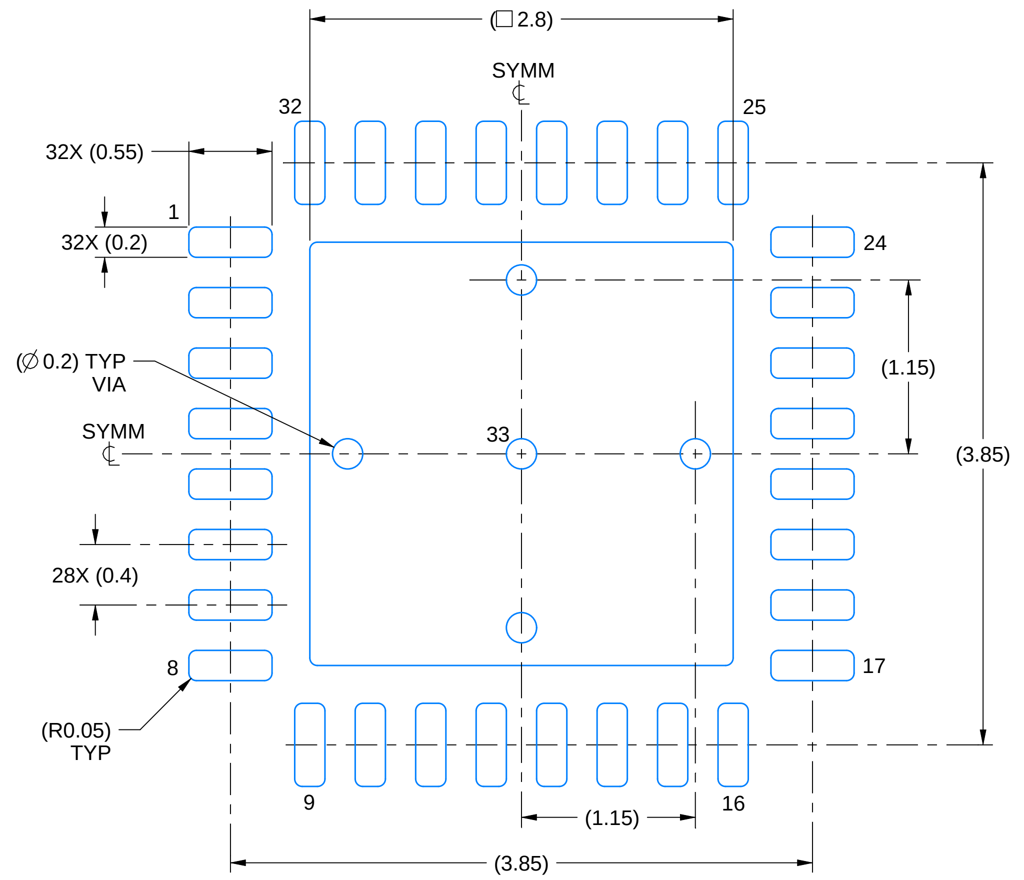
PLASTIC QUAD FLATPACK - NO LEAD



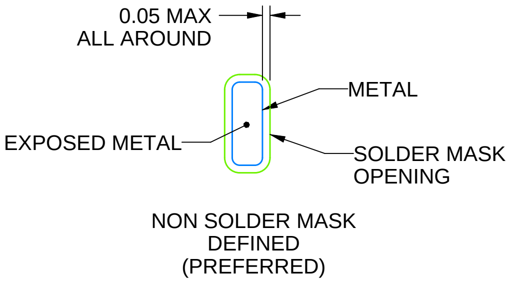
4219108/B 08/2019

NOTES:

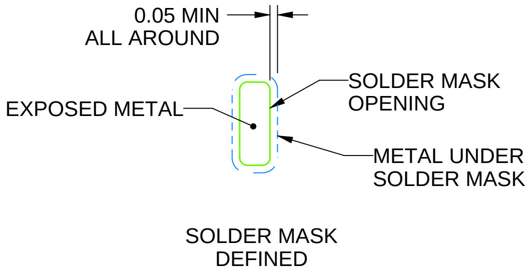
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:20X



NON SOLDER MASK
DEFINED
(PREFERRED)



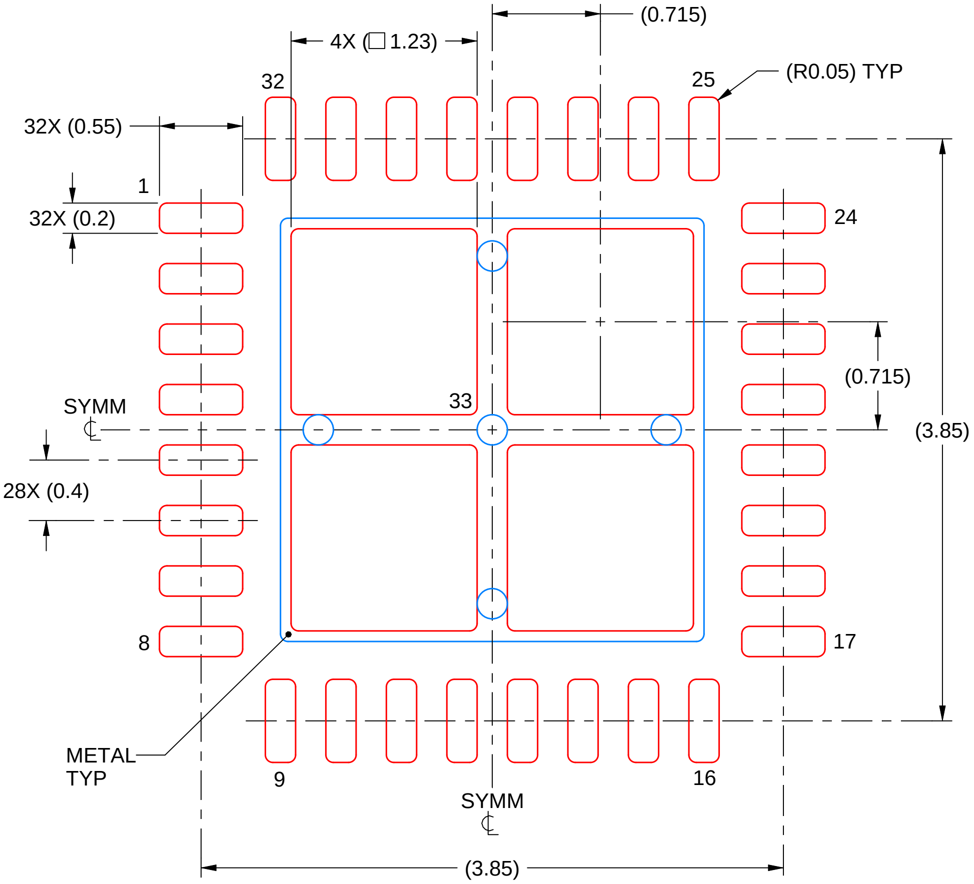
SOLDER MASK
DEFINED

SOLDER MASK DETAILS

4219108/B 08/2019

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.1 mm THICK STENCIL

EXPOSED PAD 33:
77% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:20X

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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