

# TPS65219 Power Management IC (PMIC) with 3 BUCKs and 4 LDOs for Industrial Applications

## 1 Features

- 3 buck converters at up to 2.3MHz switching frequency.
  - 1× VIN: 2.5V – 5.5V; I<sub>OUT</sub>: 3.5A; V<sub>OUT</sub> 0.6V – 3.4V
  - 2× VIN: 2.5V – 5.5V; I<sub>OUT</sub>: 2A; V<sub>OUT</sub> 0.6V – 3.4V
- 4 linear regulators:
  - 2x VIN: 1.5V – 5.5V; I<sub>OUT</sub>: 400mA; V<sub>OUT</sub>: 0.6V – 3.4V (configurable as load switch and bypass-mode, supporting SD-card)
  - 2x VIN: 2.2V – 5.5V; I<sub>OUT</sub>: 300mA; V<sub>OUT</sub>: 1.2V – 3.3V (configurable as load switch)
- Dynamic voltage scaling on all three buck converters
- Low IQ/PFM, PWM-mode (quasi-fixed frequency)
- Programmable power sequencing and default voltages
- I<sup>2</sup>C interface, supporting standard, fast-mode and fast-mode+
- Designed to support systems with 14+ rails (2× TPS65219 devices in multi-PMIC configuration)
- 2 GPOs, 1 GPIO, and 3 multi-function-pins
- EEPROM programmability

## 2 Applications

- Low power industrial MPUs and MCUs such as [AM62x](#), [AM64x](#) and [AM243x](#)
- HMI
- PLC
- Industrial PC
- Building security
- HVAC
- Video surveillance
- Data concentrators
- Smart meter
- Protection relays
- Patient monitoring and diagnostics
- Imaging

## 3 Description

The TPS65219 is a Power Management IC (PMIC) designed to supply a wide range of SoCs in both portable and stationary applications. The device is characterized across an ambient temperature range of -40°C to +105°C, making the PMIC an excellent choice for various industrial applications. The device includes three synchronous stepdown DC-DC converters and four linear regulators.

The DC-DC converters are capable of 1x 3.5A and 2x 2A. The converters require a small 470nH inductor, 4.7µF input capacitance, and a minimum 10µF output capacitance per rail depending on the switching mode configuration.

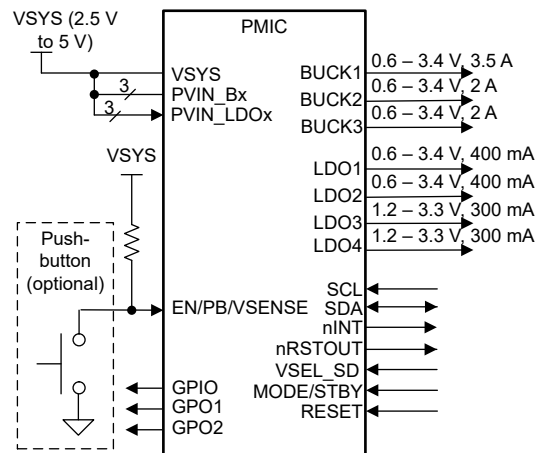
Two of the LDOs support output currents of 400mA at an output voltage range of 0.6V to 3.4V. These LDOs support bypass mode, acting as a load-switch, and allow voltage-changes during operation. The other two LDOs support output currents of 300mA at an output voltage range of 1.2V to 3.3V. These LDOs also support load-switch mode.

The I<sup>2</sup>C-interface, IOs, GPIOs and multi-function-pins (MFP) allow a seamless interface to a wide range of SoCs.

### Package Information

| PART NUMBER | PACKAGE <sup>(1)</sup> | PACKAGE SIZE (NOM) |
|-------------|------------------------|--------------------|
| TPS65219    | RSM(32-pin QFN)        | 4.00mm × 4.00mm    |
| TPS65219    | RHB(32-pin QFN)        | 5.00mm × 5.00mm    |

- (1) For all available packages, see the orderable addendum at the end of the data sheet.



**Simplified Application**

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## 4 Device Comparison

Table 4-1 lists a brief summary of the pre-configured orderable part numbers (OPNs) and the recommended application use case. This table also includes the collateral resources that are available to support new designs. The Applications note describes how the power and digital resources of the TPS65219 PMIC are used to meet the requirements of specific processors and MCUs. A full summary of the default non-volatile memory (NVM) register settings for each orderable can be found in the Technical Reference Manual (TRM).

The TPS6521905 is the user-programmable version that comes with all the power rails OFF by default and can be programmed to meet the power requirements of any processors or SoCs.

**Table 4-1. Device Comparison Table for TI Processors and MCUs**

| Device Name                | Processor / MCU               | Application Use Case |        |                  | Collateral   |   |
|----------------------------|-------------------------------|----------------------|--------|------------------|--|---|
|                            |                               | V <sub>in</sub>      | Memory | VDD_CORE         | TRM  | Apps Note   |
| TPS6521901                 | AM62x, AM62x SIP, AM64        | 5V                   | DDR4   | 0.75V            | <a href="#">SLVUCH3</a>  | <ul style="list-style-type: none"> <li>AM62 <a href="#">SLVAFD0</a></li> <li>AM64 <a href="#">SLVAFE9</a></li> <li>AM243 <a href="#">SLVAFK3</a></li> </ul> |
| TPS6521902                 | AM62x, AM62x SIP, AM64        | 3.3V or 5V           | LPDDR4 | 0.75V            | <a href="#">SLVUCL0</a>  |   |
| TPS6521903 (1)             | AM62x, AM62x SIP, AM64        | 3.3V or 5V           | DDR4   | 0.75V            | <a href="#">SLVUCJ2</a>  |   |
| TPS6521904 (1)             | AM62x, AM62x SIP, AM64, AM243 | 3.3V or 5V           | DDR4   | 0.85V            | <a href="#">SLVUCL1</a>  |   |
| TPS6521907                 | AM62x, AM62x SIP, AM64, AM243 | 5V                   | DDR4   | 0.85V            | <a href="#">SLVUCL9</a>  |   |
| TPS6521908                 | AM62x, AM62x SIP, AM64, AM243 | 3.3V or 5V           | LPDDR4 | 0.85V            | <a href="#">SLVUCM0</a>  |   |
| TPS6521909                 | AM62A, AM67                   | 5V                   | LPDDR4 | 0.85V or 0.75V   | <a href="#">SLVUCZ4</a>  |   |
| TPS6521910                 | AM62A, AM67                   | 5V                   | LPDDR4 | 0.85V or 0.75V   | <a href="#">SLVUD09</a>  |   |
| TPS6521914                 | STM32MP135A                   | 5V                   | LPDDR3 | 1.25V (external) | <a href="#">SPMU420</a>  |   |
| TPS652190C                 | NXP I.MX 8M Plus              | 3.3V                 | DDR4   | 0.85             | <a href="#">SLVUCV3</a>  | <a href="#">SLVAFQ2</a>   |
| TPS6521940                 | NXP I.MX93                    | 5V                   | LPDDR4 | 0.85V            | <a href="#">SLVUD41</a>  | <a href="#">TIDA-050087</a>   |
| <a href="#">TPS6521905</a> | User-Programmable Version     | ANY                  | ANY    | ANY              | <a href="#">TPS65219 Non-Volatile Memory (NVM) Programming Guide</a> |   |

(1) The [AM62B starter kit with PMIC](#) comes with the TPS6521904 by default, supporting VDD\_CORE=0.85V. This hardware can also be modified to support VDD\_CORE=0.75V using the TPS6521903 PMIC.

## 5 Pin Configuration and Functions

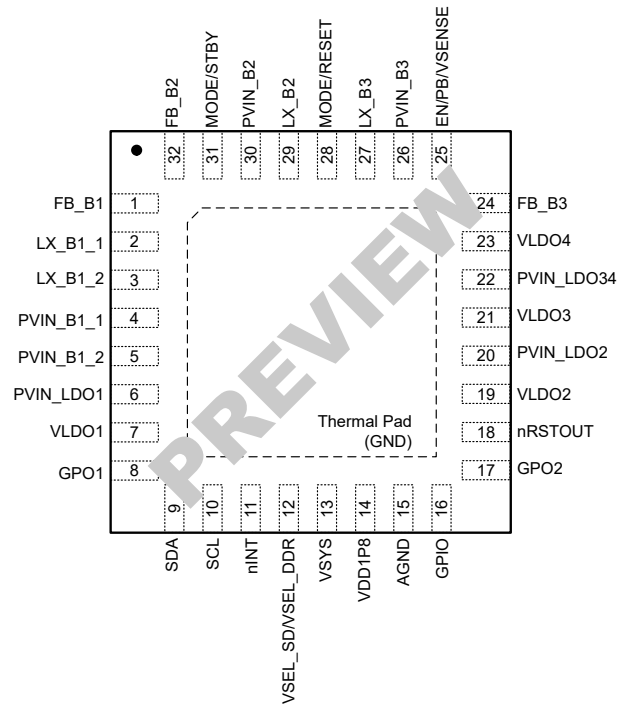
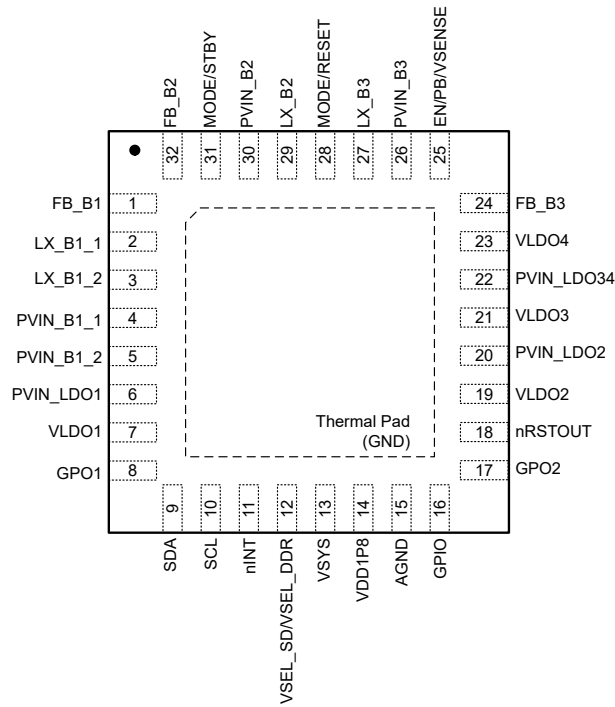


Figure 5-1. RHB Package, 32-pin QFN (Top View)

Figure 5-2. RSM Package, 32-pin QFN (Top View)

Table 5-1. Pin Functions

| PIN NAME  | PIN NO. | TYPE | DESCRIPTION   | CONNECTION if not used (output rails must be permanently disabled) |
|-----------|---------|------|---|--|
| FB_B1     | 1       | I    | Feedback Input for Buck1. Connect to Buck1 output filter. Nominal output voltage is configured in EEPROM.   | Connect to GND   |
| LX_B1_1   | 2       | PWR  | Switch Pin for Buck1. Connect one side of the Buck1-inductor to this pin.   | Leave floating   |
| LX_B1_2   | 3       | PWR  | 2nd Switch Pin for Buck1. Connect one side of the Buck1-inductor to this pin. Connect to LX_B1_1.   | Leave floating   |
| PVIN_B1_1 | 4       | PWR  | Power Input for BUCK1. Bypass this pin to ground with a 4.7µF or greater ceramic capacitor. Voltage on PVIN_B1_1 pin must not exceed voltage on VSYS pin. | Connect to VSYS  |
| PVIN_B1_2 | 5       | PWR  | 2nd Power Input for BUCK1. This pin shares the bypass capacitor from pin 4. Voltage on PVIN_B1_2 pin must not exceed voltage on VSYS pin.                 | Connect to VSYS  |
| PVIN_LDO1 | 6       | PWR  | Power Input for LDO1. Voltage on PVIN_LDO1 pin must not exceed voltage on VSYS pin.   | Connect to VSYS  |
| VLDO1     | 7       | PWR  | Output Voltage of LDO1. Nominal output voltage is configured in EEPROM. Bypass this pin to ground with a 2.2µF or greater ceramic capacitor.              | Leave floating   |
| GPO1      | 8       | O    | General Purpose Open-Drain Output. Configurable in the power-up and power-down-sequence to enable an external rail.                                       | Leave floating   |
| SDA       | 9       | I/O  | Data Pin for the I2C Serial Port. The I2C logic levels depend on the external pull-up voltage.  | Connect to VIO   |

**Table 5-1. Pin Functions (continued)**

| PIN NAME                     | PIN NO. | TYPE | DESCRIPTION  | CONNECTION if not used<br>(output rails must be permanently disabled) |
|------------------------------|---------|------|--|---|
| <b>SCL</b>                   | 10      | I    | Clock Pin for the I2C Serial Port. The I2C logic levels depend on the external pull-up voltage.  | Connect to VIO  |
| <b>nINT</b>                  | 11      | O    | Interrupt Request Output. Open-drain driver is pulled low for fault conditions. Released if bit is cleared   | Leave floating  |
| <b>VSEL_SD/<br/>VSEL_DDR</b> | 12      | I    | Multi-Function-Pin:<br>Configured as VSEL_SD: SD-card-IO-voltage select. Connected to SoC. Trigger a voltage change between 1.8V and register-based VOUT on LDO1 or LDO2. Polarity is configurable.<br>Configured as VSEL_DDR: DDR-voltage selection. Hard-wired pull-up (1.35V), pull-down (register based VOUT) or floating (1.2V) | n/a (connect to GND)  |
| <b>VSYS</b>                  | 13      | PWR  | Input supply pin for reference system. Bypass this pin to ground with a 2.2µF or greater ceramic capacitor (can be shared with PVIN-capacitors).   | n/a   |
| <b>VDD1P8</b>                | 14      | PWR  | Internal Reference Voltage: For Internal Use Only. Bypass this pin to ground with a 2.2µF or greater ceramic capacitor.  | n/a   |
| <b>AGND</b>                  | 15      | GND  | Ground pin for Analog GND  | n/a   |
| <b>GPIO</b>                  | 16      | I/O  | GPO-configuration: General Purpose Open-Drain Output. Configurable in the power-up and power-down-sequence to enable an external rail.<br>GPIO-configuration:<br>Synchronizing I/O. Used to synchronize two or more TPS65219. The pin is level-sensitive.  | Leave floating  |
| <b>GPO2</b>                  | 17      | O    | General Purpose Open-Drain Output. Configurable in the power-up and power-down-sequence to enable an external rail.  | Leave floating  |
| <b>nRSTOUT</b>               | 18      | O    | Reset-output to SoC. Controlled by sequencer. High in ACTIVE and STBY state.   | Leave floating  |
| <b>VLDO2</b>                 | 19      | PWR  | Output Voltage of LDO2. Nominal output voltage is configured in EEPROM. Bypass this pin to ground with a 2.2µF or greater ceramic capacitor.   | Leave floating  |
| <b>PVIN_LDO2</b>             | 20      | PWR  | Power Input for LDO2. Bypass this pin to ground with a 2.2µF or greater ceramic capacitor. Voltage on PVIN_LDO2 pin must not exceed voltage on VSYS pin.   | Connect to VSYS   |
| <b>VLDO3</b>                 | 21      | PWR  | Output Voltage of LDO3. Nominal output voltage is configured in EEPROM. Bypass this pin to ground with a 2.2µF or greater ceramic capacitor.   | Leave floating  |
| <b>PVIN_LDO34</b>            | 22      | PWR  | Power Input for LDO3 and LDO4. Bypass this pin to ground with a 4.7µF or greater ceramic capacitor. Voltage on PVIN_LDO34 pin must not exceed voltage on VSYS pin.   | Connect to VSYS   |
| <b>VLDO4</b>                 | 23      | PWR  | Output Voltage of LDO4. Nominal output voltage is configured in EEPROM. Bypass this pin to ground with a 2.2µF or greater ceramic capacitor.   | Leave floating  |
| <b>FB_B3</b>                 | 24      | I    | Feedback Input for Buck3. Connect to Buck3 output filter. Nominal output voltage is configured in EEPROM.  | Connect to GND  |

**Table 5-1. Pin Functions (continued)**

| PIN NAME                 | PIN NO. | TYPE | DESCRIPTION  | CONNECTION if not used<br>(output rails must be permanently disabled)                            |
|--------------------------|---------|------|--|--|
| <b>EN/PB/<br/>VSENSE</b> | 25      | I    | ON-request input.<br>Configured as EN: Device enable pin, high level is ON-request, low-level is OFF-request.<br>Configured as PB: Push-button monitor input.<br>600ms low-level is an ON-request, 8s low-level is an OFF-request.<br>Configured as VSENSE: Power-fail comparator input. Set sense voltage using a resistor divider connected from the input to the pre-regulator to this pin to ground. Detects rising/falling voltage on pre-regulator and triggers ON- / OFF-request.<br>The pin is edge-sensitive with a wait-time in PB-configuration and deglitch time for EN- and VSENSE-configuration. | n/a (configure as EN and connect to VSYS)  |
| <b>PVIN_B3</b>           | 26      | PWR  | Power Input for BUCK3. Bypass this pin to ground with a 4.7 $\mu$ F or greater ceramic capacitor. Voltage on PVIN_B3 pin must not exceed voltage on VSYS pin.  | Connect to VSYS  |
| <b>LX_B3</b>             | 27      | PWR  | Switch Pin for Buck3. Connect one side of the Buck3-inductor to this pin.  | Leave floating   |
| <b>MODE/RESET</b>        | 28      | I    | Multi-Function-Pin:<br>Configured as MODE: Connected to SoC or hard-wired pull-up/-down. Forces the Buck-converters into PWM or permits auto-entry in PFM-mode.<br>Configured as RESET: Connected to SoC. Forces a WARM or COLD reset (configurable), WARM reset resetting output voltages to defaults, COLD reset sequencing down all enabled rails and power up again.<br>Polarity is configurable.<br>The pin is level-sensitive for MODE-configuration, edge-sensitive for RESET-configuration.  | n/a (tie high or low, dependent on configuration, see 'PWM/PFM and Reset (MODE/RESET)')          |
| <b>LX_B2</b>             | 29      | PWR  | Switch Pin for Buck2. Connect one side of the Buck2-inductor to this pin.  | Leave floating   |
| <b>PVIN_B2</b>           | 30      | PWR  | Power Input for BUCK2. Bypass this pin to ground with a 4.7 $\mu$ F or greater ceramic capacitor. Voltage on PVIN_B2 pin must not exceed voltage on VSYS pin.  | Connect to VSYS  |
| <b>MODE/STBY</b>         | 31      | I    | Multi-Function-Pin:<br>Configured as MODE:<br>Connected to SoC or hard-wired pull-up/-down. Forces the Buck-converters into PWM or permits auto-entry in PFM-mode.<br>Configured as STBY: Low-power-mode command, disables selected rails.<br>Both functions, MODE and STBY, can be combined.<br>The pin is level-sensitive.   | n/a (tie high or low, dependent on configuration, see 'PWM/PFM and Low Power Modes (MODE/STBY)') |
| <b>FB_B2</b>             | 32      | I    | Feedback Input for Buck2. Connect to Buck2 output filter. Nominal output voltage is configured in EEPROM.  | Connect to GND   |

**Table 5-1. Pin Functions (continued)**

| PIN NAME    | PIN NO.  | TYPE | DESCRIPTION  | CONNECTION if not used<br>(output rails must be permanently disabled) |
|-------------|----------|------|--|---|
| <b>PGND</b> | PowerPad | GND  | Power-Ground. The exposed pad must be connected to a continuous ground plane of the printed circuit board by multiple interconnect vias directly under the TPS65219 to maximize electrical and thermal conduction. | n/a   |

## 6 Specifications

### 6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)<sup>(1)</sup>

| POS   |  |   | MIN  | MAX                          | UNIT |
|-------|--|---|------|------------------------------|------|
| 1.1.1 | Input voltage                                  | VSYS  | -0.3 | 6                            | V    |
| 1.1.2 | Input voltage                                  | PVIN_B1, PVIN_B2, PVIN_B3, PVIN_LDO1, PVIN_LDO2, PVIN_LDO34     | -0.3 | 6                            | V    |
| 1.1.3 | Input voltage vs. VSYS for Bucks               | PVIN_B1, PVIN_B2, PVIN_B3 maximum voltage exceeding VSYS        |      | 200                          | mV   |
| 1.1.4 | Input voltage vs. VSYS for LDOs                | PVIN_LDO1, PVIN_LDO2, PVIN_LDO34 maximum voltage exceeding VSYS |      | 20                           | mV   |
| 1.1.5 | Input voltage                                  | FB_B1, FB_B2, FB_B3   | -0.3 | 6                            | V    |
| 1.1.6 | Input voltage                                  | EN/PB/VSENSE, MODE/STBY, MODE/RESET, VSEL_SD/VSEL_DDR           | -0.3 | 6                            | V    |
| 1.2.1 | Output voltage                                 | LX_B1, LX_B2, LX_B3   | -0.3 | PVIN_Bx + 0.3 V, up to 6 V   | V    |
| 1.2.2 | Output voltage                                 | LX_B1, LX_B2, LX_B3 spikes for maximum 10ns                     | -2   | 10                           | V    |
| 1.2.3 | Output voltage                                 | GPO1, GPO2, GPIO  | -0.3 | 6                            | V    |
| 1.2.4 | Output voltage                                 | VLDO1, VLDO2, VLDO3, VLDO4                                      | -0.3 | PVIN_LDOx + 0.3 V, up to 6 V | V    |
| 1.2.5 | Output voltage                                 | VDD1P8  | -0.3 | 2                            | V    |
| 1.2.6 | Output voltage                                 | SDA, SCL  | -0.3 | 6                            | V    |
| 1.2.7 | Output voltage                                 | nINT, nRSTOUT   | -0.3 | 6                            | V    |
| 1.4.1 | Operating junction temperature, T <sub>J</sub> |   | -40  | 125                          | °C   |
| 1.4.2 | Storage temperature, T <sub>stg</sub>          |   | -40  | 150                          | °C   |

- (1) Operation outside the *Absolute Maximum Ratings* may cause permanent device damage. *Absolute Maximum Ratings* do not imply functional operation of the device at these or any other conditions beyond those listed under *Recommended Operating Conditions*. If used outside the *Recommended Operating Conditions* but within the *Absolute Maximum Ratings*, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.

### 6.2 ESD Ratings

| POS |                    |   | VALUE   | UNIT    |
|-----|--------------------|---|---|---------|
| 2.1 | V <sub>(ESD)</sub> | Electrostatic discharge, Human Body Model     | Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins <sup>(1)</sup>     | ±2000 V |
| 2.2 | V <sub>(ESD)</sub> | Electrostatic discharge, Charged Device Model | Charged device model (CDM), per ANSI/ESDA/JEDEC JS-002, all pins <sup>(2)</sup> | ±500 V  |

- (1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.

- (2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

### 6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

| POS   |   |   | MIN                | NOM | MAX                | UNIT |
|-------|---|---|--------------------|-----|--------------------|------|
| 3.1.1 | V <sub>VSYS</sub>   | Input voltage   | 2.5 <sup>(1)</sup> |     | 5.5                | V    |
| 3.1.2 | V <sub>PVIN_B1</sub> , V <sub>PVIN_B2</sub> , V <sub>PVIN_B3</sub> , V <sub>LX_B1</sub> , V <sub>LX_B2</sub> , V <sub>LX_B3</sub> | BUCKx Pins  | 2.5                |     | 5.5 <sup>(2)</sup> | V    |
| 3.1.3 | ΔV <sub>VSYS_PVIN_Bx</sub>  | Voltage differential from V <sub>PVIN_Bx</sub> to V <sub>VSYS</sub> |                    |     | 0                  | mV   |

### 6.3 Recommended Operating Conditions (continued)

over operating free-air temperature range (unless otherwise noted)

| POS     |  |  | MIN  | NOM | MAX     | UNIT        |
|---------|--|--|------|-----|---------|-------------|
| 3.1.4   | $\Delta V_{VSYS\_PVIN\_LDO1,LDO2}$                                       | Voltage differential from $V_{PVIN\_LDO1}$ or $V_{PVIN\_LDO2}$ to $V_{VSYS}$   |      |     | 0       | mV          |
| 3.1.5   | $\Delta V_{VSYS\_VLDO34}$  | Voltage by which $V_{VSYS}$ must exceed LDO output voltage (VLDO3, VLDO4); $V_{VSYS} = 2.5V$ to 3.45V; LDO mode  | 150  |     |         | mV          |
| 3.1.6   | $\Delta V_{VSYS\_VLDO34}$  | Voltage by which $V_{VSYS}$ must exceed LDO output voltage (VLDO3, VLDO4); $V_{VSYS} = 3.45V$ to 5.5V in LDO-mode or $V_{VSYS} = 2.5V$ to 5.5V in LSW-mode | n/a  |     |         | mV          |
| 3.1.7   | $C_{PVIN\_B1}, C_{PVIN\_B2}, C_{PVIN\_B3}$                               | BUCKx Input Capacitance  | 3.9  | 4.7 |         | $\mu F$     |
| 3.1.8   | $L_{B1}, L_{B2}, L_{B3}$   | BUCKx Output Inductance  | 330  | 470 | 611     | nH          |
| 3.1.9a  | $C_{OUT\_B1}, C_{OUT\_B2}, C_{OUT\_B3}$                                  | BUCKx Output Capacitance, forced PWM or auto-PFM, low bandwidth case   | 10   |     | 75      | $\mu F$     |
| 3.1.10a | $C_{OUT\_B1}, C_{OUT\_B2}, C_{OUT\_B3}$                                  | BUCKx Output Capacitance, forced PWM or auto-PFM, high bandwidth case  | 30   |     | 220     | $\mu F$     |
| 3.1.11  | $V_{FB\_B1}, V_{FB\_B2}, V_{FB\_B3}$                                     | BUCKx FB Pins  | 0    |     | 5.5 (2) | V           |
| 3.1.12  | $V_{PVIN\_LDO1}, V_{PVIN\_LDO2}$   | LDO Input Voltage  | 1.5  |     | 5.5 (2) | V           |
| 3.1.13  | $V_{PVIN\_LDO1}, V_{PVIN\_LDO2}$   | LDO Input Voltage in bypass mode   | 1.5  |     | 3.6     | V           |
| 3.1.14  | $V_{PVIN\_LDO1}, V_{PVIN\_LDO2}$   | Allowable delta between $V_{PVIN\_LDOx}$ and configured $V_{VLDOx}$ in bypass mode   | -200 |     | 200     | mV          |
| 3.1.15  | $V_{VLDO1}, V_{VLDO2}$   | LDO Output Voltage Range   | 0.6  |     | 3.4     | V           |
| 3.1.16  | $C_{PVIN\_LDO1}, C_{PVIN\_LDO2}$   | LDO Input Capacitance  | 1.6  | 2.2 |         | $\mu F$     |
| 3.1.17  | $C_{VLDO1}, C_{VLDO2}$   | LDO Output Capacitance   | 1.6  | 2.2 | 20      | $\mu F$     |
| 3.1.18  | $V_{PVIN\_LDO3}, V_{PVIN\_LDO4}$   | LDO Input Voltage  | 2.2  |     | 5.5 (2) | V           |
| 3.1.19  | $V_{VLDO3}, V_{VLDO4}$   | LDO Output Voltage Range   | 1.2  |     | 3.3     | V           |
| 3.1.20  | $C_{PVIN\_LDO34}$  | LDO Input Capacitance  | 2.2  | 4.7 |         | $\mu F$     |
| 3.1.21  | $C_{VLDO3}, C_{VLDO4}$   | LDO Output Capacitance   | 1.6  | 2.2 | 30 (3)  | $\mu F$     |
| 3.1.22  | $V_{VDD1P8}$   | VDD1P8 pin   | 0    |     | 1.8     | V           |
| 3.1.23  | $C_{VDD1P8}$   | Internal Regulator Decoupling Capacitance  | 1    | 2.2 | 4       | $\mu F$     |
| 3.1.24  | $C_{VSYS}$   | VSYS Input Decoupling Capacitance  | 1    | 2.2 |         | $\mu F$     |
| 3.1.25  | $V_{nINT}, V_{nRSTOUT}$  | Digital Outputs  | 0    |     | 3.4     | V           |
| 3.1.26  | $V_{GPO1}, V_{GPO2}, V_{GPIO}$   | Digital Outputs  | 0    |     | 5.5 (2) | V           |
| 3.1.27  | $V_{SCL}, V_{SDA}$   | I2C Interface  | 0    |     | 3.4     | V           |
| 3.1.28  | $V_{EN/PB/VSENSE}, V_{MODE/STBY}, V_{MODE/RESET}, V_{VSEL\_SD/VSEL/DDR}$ | Digital Inputs   | 0    |     | 5.5 (2) | V           |
| 3.2.1   | $t_{VSYS\_RAMP\_RISE}$   | Input voltage rising ramp Time, Input voltage controlled by a pre-regulator. $V_{VSYS} = V_{PVIN\_Bx} = V_{PVIN\_LDOx} = 0V$ to 5V                         | 0.1  |     | 600000  | ms          |
| 3.2.2   | $t_{VSYS\_RAMP\_FALL}$   | Input voltage falling Ramp Time, $V_{VSYS} = V_{PVIN\_Bx} = V_{PVIN\_LDOx} = 5V$ to 2.5V   | 0.4  |     | 600000  | ms          |
| 3.3.1   | $T_A$  | Operating free-air temperature   | -40  |     | 105     | $^{\circ}C$ |
| 3.3.2   | $T_J$  | Operating junction temperature   | -40  |     | 125     | $^{\circ}C$ |

(1) For EEPROM programming,  $VSYS(\min)=3.3V$

(2) Must not exceed  $VSYS$

(3) In slow-ramp-mode. Fast-ramp supports 15 $\mu F$  maximum

## 6.4 Thermal Information

| THERMAL METRIC <sup>(1)</sup> |  | TPS65219                    | TPS65219                    | UNIT |
|-------------------------------|--|-----------------------------|-----------------------------|------|
|                               |  | RHB (QFN)                   | RSM (QFN)                   |      |
|                               |  | 32 PINS, 5x5mm <sup>2</sup> | 32 PINS, 4x4mm <sup>2</sup> |      |
| R <sub>ΘJA</sub>              | Junction-to-ambient thermal resistance       | 31.3                        | 31.9                        | °C/W |
| R <sub>ΘJC(top)</sub>         | Junction-to-case (top) thermal resistance    | 20.4                        | 25.6                        | °C/W |
| R <sub>ΘJB</sub>              | Junction-to-board thermal resistance         | 10.9                        | 10.5                        | °C/W |
| Ψ <sub>JT</sub>               | Junction-to-top characterization parameter   | 0.3                         | 0.3                         | °C/W |
| Ψ <sub>JB</sub>               | Junction-to-board characterization parameter | 10.8                        | 10.5                        | °C/W |
| R <sub>ΘJC(bot)</sub>         | Junction-to-case (bottom) thermal resistance | 2.8                         | 2.9                         | °C/W |

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report, SPRA953.

## 6.5 System Control Thresholds

Over operating free-air temperature range (unless otherwise noted). Voltage level refers to the AGND ground of the device.

| POS                               | PARAMETER                    | TEST CONDITIONS  | MIN   | TYP | MAX  | UNIT |
|-----------------------------------|------------------------------|--|---|-----|------|------|
| <b>Electrical Characteristics</b> |                              |  |   |     |      |      |
| 4.1.1                             | VSYS                         | Operating Input Voltage  | 2.5   |     | 5.5  | V    |
| 4.1.2                             | VSYS <sub>POR_Rising</sub>   | VSYS POR rising threshold                                      | Measured on VSYS pin, untrimmed   |     | 2.5  | V    |
| 4.1.3                             | VSYS <sub>UVLO_Falling</sub> | VSYS UVLO falling threshold                                    | Measured on VSYS pin, trimmed   |     | 2.25 | V    |
| 4.1.4                             | VSYS <sub>POR_Hyst</sub>     | VSYS UVLO/POR hysteresis                                       | VSYS <sub>POR_Rising_untrimmed</sub><br>VSYS <sub>UVLO_Falling_trimmed</sub>  |     | 130  | mV   |
| 4.1.5                             | V <sub>VSYS_OVP_Rise</sub>   | VSYS OVP rising threshold, trimmed                             | Measured on VSYS pin, trimmed   |     | 6.1  | V    |
| 4.1.6                             | V <sub>VSYS_OVP_Fall</sub>   | VSYS OVP falling threshold, trimmed                            | Measured on VSYS pin, trimmed   |     | 5.95 | V    |
| 4.1.7                             | V <sub>VSYS_OVP_Hyst</sub>   | VSYS OVP hysteresis  | VSYS <sub>OVP_Rising_trimmed</sub><br>VSYS <sub>OVP_falling_trimmed</sub>   |     | 180  | mV   |
| 4.1.8                             | V <sub>VDD1P8</sub>          | VDD1P8 voltage   | 1.7   | 1.8 | 1.9  | V    |
| 4.2.1a                            | I <sub>INITIALIZE</sub>      | Current Consumption in INITIALIZE state, at 25°C               | Combined Current from VSYS and PVIN <sub>x</sub> pins. VSYS = PVIN <sub>Bx</sub> = PVIN <sub>LDOx</sub> = 5V. All Monitors are off. T <sub>J</sub> = 25°C   |     | 22   | μA   |
| 4.2.1b                            | I <sub>INITIALIZE</sub>      | Current Consumption in INITIALIZE state, 40°C to 125°C         | Combined Current from VSYS and PVIN <sub>x</sub> pins. VSYS = PVIN <sub>Bx</sub> = PVIN <sub>LDOx</sub> = 5V. All Monitors are off. T <sub>J</sub> = -40°C to 125°C   |     | 35   | μA   |
| 4.2.2a                            | I <sub>ACTIVE</sub>          | ACTIVE State Current Consumption, all rails on, at 25°C        | Combined Current from VSYS and PVIN <sub>x</sub> pins. VSYS = PVIN <sub>Bx</sub> = PVIN <sub>LDOx</sub> = 5V. All Outputs are on, all LDOs in LDO-mode, Bucks in PFM mode. No Load. T <sub>J</sub> = 25°C           |     | 290  | μA   |
| 4.2.2b                            | I <sub>ACTIVE</sub>          | ACTIVE State Current Consumption, all rails on, -40°C to 125°C | Combined Current from VSYS and PVIN <sub>x</sub> pins. VSYS = PVIN <sub>Bx</sub> = PVIN <sub>LDOx</sub> = 5V. All Outputs are on, all LDOs in LDO-mode, Bucks in PFM mode. No Load. T <sub>J</sub> = -40°C to 125°C |     | 430  | μA   |

## 6.5 System Control Thresholds (continued)

Over operating free-air temperature range (unless otherwise noted). Voltage level refers to the AGND ground of the device.

| POS    | PARAMETER  |   | TEST CONDITIONS  | MIN | TYP | MAX | UNIT          |
|--------|------------|---|--|-----|-----|-----|---------------|
| 4.2.3a | $I_{STBY}$ | STBY State Current Consumption, only LDO1 on, at 25°C                 | Combined Current from VSYS and PVIN_x pins. VSYS = PVIN_Bx = PVIN_LDOx = 5V. Only LDO1 on in LDO-mode. No Load.<br>$T_J = 25^\circ\text{C}$  |     | 105 | 125 | $\mu\text{A}$ |
| 4.2.3b | $I_{STBY}$ | STBY State Current Consumption, only LDO1 on, -40°C to 125°C          | Combined Current from VSYS and PVIN_x pins. VSYS = PVIN_Bx = PVIN_LDOx = 5V. Only LDO1 on in LDO-mode. No Load.<br>$T_J = -40^\circ\text{C}$ to $125^\circ\text{C}$  |     | 105 | 150 | $\mu\text{A}$ |
| 4.2.4a | $I_{STBY}$ | STBY State Current Consumption, all rails on, VMON on at 25°C         | Combined Current from VSYS and PVIN_x pins. VSYS = PVIN_Bx = PVIN_LDOx = 5V. All Outputs are on, all LDOs in LDO-mode, Bucks in PFM mode. No Load. Output-voltage Monitors are on, VSYS-monitor (UV/OVP) are on.<br>$T_J = 25^\circ\text{C}$                         |     | 250 | 290 | $\mu\text{A}$ |
| 4.2.4b | $I_{STBY}$ | STBY State Current Consumption, all rails on, VMON on, -40°C to 125°C | Combined Current from VSYS and PVIN_x pins. VSYS = PVIN_Bx = PVIN_LDOx = 5V. All Outputs are on, all LDOs in LDO-mode, Bucks in PFM mode. No Load. Output-voltage Monitors are on, VSYS-monitor (UV/OVP) are on.<br>$T_J = -40^\circ\text{C}$ to $125^\circ\text{C}$ |     | 250 | 430 | $\mu\text{A}$ |

### Timing Requirements

|        |                          |  |   |    |    |  |    |
|--------|--------------------------|--|---|----|----|--|----|
| 4.3.1  | $t_{OFF\_TO\_INIT}$      | Time from VSYS passing VSYS_POR until entering INITIALIZE state, including EEPROM-read, ready for ON-request   | Time from VSYS passing VSYS_POR until entering INITIALIZE state. On request execution gated by HOT and RV |    |    | 3.2  | ms |
| 4.3.2a | $t_{TIMEOUT\_UV}$        | UV-detection in case a rail does not reach UV-threshold during ramp-up   |   |    |    | end of $t_{RAMP}$ + sample- and deglitch time  |    |
| 4.3.2b | $t_{TIMEOUT\_UV\_SLOT}$  | Timeout in case a rail does not reach UV-threshold during ramp-up, applicable in Multi-PMIC-configuration only |   |    |    | end of slot- extension time (3ms, 4ms or 13ms) |    |
| 4.3.3  | $t_{TIMEOUT\_Discharge}$ | Timeout in case a rail cannot be discharged when transitioning from STBY to ACTIVE state                       |   | 72 | 80 | 88   | ms |

## 6.6 BUCK1 Converter

over operating free-air temperature range (unless otherwise noted)

| POS                               | PARAMETER       |                              | TEST CONDITIONS                   | MIN | TYP | MAX | UNIT |
|-----------------------------------|-----------------|------------------------------|-----------------------------------|-----|-----|-----|------|
| <b>Electrical Characteristics</b> |                 |                              |                                   |     |     |     |      |
| 5.1.1a                            | $V_{IN\_BUCK1}$ | Input voltage <sup>(1)</sup> | Buck supply voltage, maximum VSYS | 2.5 |     | 5.5 | V    |

## 6.6 BUCK1 Converter (continued)

over operating free-air temperature range (unless otherwise noted)

| POS    | PARAMETER               | TEST CONDITIONS   | MIN  | TYP | MAX   | UNIT |         |            |
|--------|-------------------------|---|--|-----|-------|------|---------|------------|
| 5.1.1b | $V_{OUT\_BUCK1}$        | Buck Output Voltage configurable Range                                      | Output voltage configurable in 25mV-steps for $0.6V \leq V_{OUT} \leq 1.4V$ , in 100mV steps for $1.4V < V_{OUT} \leq 3.4V$                          |     | 0.6   | 3.4  | V       |            |
| 5.1.2a | $I_{Q\_BUCK1}$          | Quiescent Current at 25°C, PFM, low BW case                                 | PFM, BUCK1 enabled, no load, $V_{IN} = 5.0V$ , $V_{OUT} = 1.2V$ , $T_J = 25^\circ C$   |     | 10    | 13   | $\mu A$ |            |
| 5.1.2b | $I_{Q\_BUCK1}$          | Quiescent Current -40°C to 125°C, PFM, low BW case                          | PFM, BUCK1 enabled, no load, $V_{IN} = 5.0V$ , $V_{OUT} = 1.2V$ , $T_J = -40^\circ C$ to $125^\circ C$   |     | 15    | 44   | $\mu A$ |            |
| 5.1.2c | $I_{Q\_BUCK1}$          | Quiescent Current -40°C to 150°C, PFM, low BW case                          | PFM, BUCK1 enabled, no load, $V_{IN} = 5.0V$ , $V_{OUT} = 1.2V$ , $T_J = -40^\circ C$ to $150^\circ C$   |     | 20    | 63   | $\mu A$ |            |
| 5.1.3a | $V_{HEADROOM\_PWM}$     | Input to Output Voltage Headroom <sup>(2)</sup>                             | Corner cases at maximum load $I_{OUT} = 2.5A$  |     | 500   |      | mV      |            |
| 5.1.3b | $V_{HEADROOM\_PWM}$     | Input to Output Voltage Headroom at $I_{OUT} = I_{OUT\_MAX}$ <sup>(2)</sup> | Corner cases at $I_{OUT} = I_{OUT\_MAX}$   |     | 700   |      | mV      |            |
| 5.1.4  | $V_{OUT\_STEP\_LOW}$    | Output voltage Steps  | $0.6V \leq V_{OUT} \leq 1.4V$  |     | 25    |      | mV      |            |
| 5.1.5  | $V_{OUT\_STEP\_HIGH}$   | Output voltage Steps  | $1.5V \leq V_{OUT} \leq 3.4V$  |     | 100   |      | mV      |            |
| 5.1.6a | $V_{OUT\_ACC\_DC\_PWM}$ | DC Output Voltage Accuracy in forced PWM mode, low and high BW case         | $I_{OUT} = I_{OUT\_MAX}$ , $V_{OUT} \geq 0.7V$ to $3.4V$ , $V_{IN} - V_{OUT} > 700$ mV forced PWM, low BW case                                       |     | -1.5% | 1.5% |         |            |
| 5.1.6b | $V_{OUT\_ACC\_DC\_PWM}$ | DC Output Voltage Accuracy in forced PWM mode, low and high BW case         | $I_{OUT} = I_{OUT\_MAX}$ , $V_{OUT} = 0.6V$ to $0.7V$ , $V_{IN} - V_{OUT} > 700$ mV forced PWM, low BW case  |     | -10   | 10   | mV      |            |
| 5.1.6c | $V_{OUT\_ACC\_DC\_PFM}$ | DC Output Voltage Accuracy in auto-PFM mode, low and high BW case           | $I_{OUT} = 1mA$ , $V_{OUT} = 0.6V$ to $3.4V$ , $V_{IN} - V_{OUT} > 500$ mV auto-PFM, low BW case   |     | -3.0% | 3.5% |         |            |
| 5.1.7  | $R_{FB\_INPUT}$         | Feedback input impedance  | Converter enabled  |     | 2.3   | 3.75 | 5.0     | M $\Omega$ |
| 5.2.1a | $V_{LOAD\_REG\_PWM}$    | DC Load Regulation, forced PWM, low BW case                                 | $V_{IN} = 5.0V$ , $V_{OUT} = 1.2V$ , $I_{OUT} = 0$ to $I_{OUT\_MAX}$ , forced PWM, low BW case, $C_{OUT} = 40\mu F$                                  |     | 0.1   | 0.16 | %/A     |            |
| 5.2.2a | $V_{LINE\_REG}$         | DC Line Regulation, forced PWM, low BW case                                 | $V_{IN} = 3.3V$ to $5.5V$ , $V_{OUT} = 1.2V$ , $I_{OUT} = 1mA$ and $I_{OUT\_MAX}$ forced PWM, low BW case, $C_{OUT} = 40\mu F$                       |     | 0.1   | 0.16 | %/V     |            |
| 5.2.3a | $V_{LOAD\_TRANSIENT}$   | Load Transient, $V_{OUT} = 0.75V$ , auto-PFM, high BW case                  | $V_{IN} = 5.0V$ , $V_{OUT} = 0.75V$ , $I_{OUT} = 100mA$ to $1100mA$ to $100mA$ , $t_R = t_F = 500ns$ , auto-PFM, high BW case, $C_{OUT} = 80\mu F$   |     | -27.5 | 27.5 | mV      |            |
| 5.2.3b | $V_{LOAD\_TRANSIENT}$   | Load Transient, $V_{OUT} = 0.75V$ , forced PWM, high BW case                | $V_{IN} = 5.0V$ , $V_{OUT} = 0.75V$ , $I_{OUT} = 100mA$ to $1100mA$ to $100mA$ , $t_R = t_F = 500ns$ , forced PWM, high BW case, $C_{OUT} = 80\mu F$ |     | -27.5 | 27.5 | mV      |            |
| 5.2.4a | $V_{LOAD\_TRANSIENT}$   | Load Transient, $V_{OUT} = 1.8V$ , auto-PFM, low BW case                    | $V_{IN} = 5.0V$ , $V_{OUT} = 1.8V$ , $I_{OUT} = 1mA$ to $1A$ to $1mA$ , $t_R = t_F = 1\mu s$ , auto-PFM, $C_{OUT} = 40\mu F$                         |     | -90   | 90   | mV      |            |

## 6.6 BUCK1 Converter (continued)

over operating free-air temperature range (unless otherwise noted)

| POS                              | PARAMETER                   | TEST CONDITIONS   | MIN   | TYP | MAX  | UNIT |                  |       |
|----------------------------------|-----------------------------|---|---|-----|------|------|------------------|-------|
| 5.2.4b                           | V <sub>LOAD_TRANSIENT</sub> | Load Transient, V <sub>OUT</sub> =1.8V, forced PWM, low BW case | V <sub>IN</sub> = 5.0V, V <sub>OUT</sub> = 1.8V, I <sub>OUT</sub> = 1mA to 1A to 1mA, t <sub>R</sub> = t <sub>F</sub> = 1μs, forced PWM, C <sub>OUT</sub> = 40μF    |     | -60  | 60   | mV               |       |
| 5.2.5a                           | V <sub>LINE_TRANSIENT</sub> | Line Transient, V <sub>OUT</sub> =1.2V, forced PWM, low BW case | V <sub>IN</sub> = 3.3V to 5.5V in 50μs, V <sub>OUT</sub> = 1.2V, I <sub>OUT</sub> = 1mA and I <sub>OUT_MAX</sub> , forced PWM, low BW case, C <sub>OUT</sub> = 40μF |     | -50  | 50   | mV               |       |
| 5.2.6a                           | V <sub>RIPPLE_PP_PWM</sub>  | Forced PWM Mode, low BW case                                    | V <sub>IN</sub> = 5.0V, V <sub>OUT</sub> = 2.5V, forced PWM, low BW case, C <sub>OUT</sub> = 40μF, X5R, ESR = 10mOhm, L = 470nH, DCR = 50mΩ, I <sub>OUT</sub> = 1A  |     | 10   | 20   | mV <sub>PP</sub> |       |
| 5.2.6b                           | V <sub>RIPPLE_PP_PFM</sub>  | Auto PFM Mode, low BW case                                      | V <sub>IN</sub> = 5.0V, V <sub>OUT</sub> = 2.5V, auto PFM, low BW case, C <sub>OUT</sub> = 40μF, X5R, ESR = 10mOhm, L = 470nH, DCR = 50mΩ, I <sub>OUT</sub> = 20mA  |     | 20   | 40   | mV <sub>PP</sub> |       |
| 5.3.1                            | I <sub>OUT_MAX</sub>        | Maximum Operating Current                                       |   |     |      | 3.5  | A                |       |
| 5.3.2                            | I <sub>CURRENT_LIMIT</sub>  | Peak Current Limit  | V <sub>IN</sub> = 2.5V to 5.5V  |     | 4.6  | 5.7  | 6.9              | A     |
| 5.3.3                            | I <sub>REV_CUR_LIMIT</sub>  | Reverse Peak Current Limit                                      | V <sub>IN</sub> = 2.5V to 5.5V  |     | -2.0 | -1.5 | -1.0             | A     |
| 5.3.4a                           | R <sub>DSON_HS</sub>        | High Side MOSFET On Resistance, 5V-supply                       | Measured Pin to Pin, V <sub>IN</sub> = 5V   |     |      | 70   | mΩ               |       |
| 5.3.4b                           | R <sub>DSON_HS</sub>        | High Side MOSFET On Resistance, 3.3V-supply                     | Measured Pin to Pin, V <sub>IN</sub> = 3.3V   |     |      | 80   | mΩ               |       |
| 5.3.5a                           | R <sub>DSON_LS</sub>        | Low Side MOSFET On Resistance, 5V-supply                        | Measured Pin to Pin, V <sub>IN</sub> = 5V   |     |      | 40   | mΩ               |       |
| 5.3.5b                           | R <sub>DSON_LS</sub>        | Low Side MOSFET On Resistance, 3.3V-supply                      | Measured Pin to Pin, V <sub>IN</sub> = 3.3V   |     |      | 50   | mΩ               |       |
| 5.3.6                            | R <sub>DISCHARGE</sub>      | Output Discharge Resistance                                     | Active only when converter is disabled  |     | 60   | 125  | 200              | Ω     |
| 5.4.1                            | L <sub>SW</sub>             | Output Inductance   | DCR = 50mΩ max  |     | 330  | 470  | 611              | nH    |
| 5.4.2a                           | C <sub>OUT</sub>            | Output Capacitance in auto-PFM or forced PWM for low BW case    | ESR = 10mΩ max  |     | 10   | 75   | μF               |       |
| 5.4.3a                           | C <sub>OUT_HIGH_BW</sub>    | Output Capacitance in auto-PFM or forced PWM for high BW case   | ESR = 10mΩ max  |     | 30   | 220  | μF               |       |
| <b>Timing Requirements</b>       |                             |   |   |     |      |      |                  |       |
| 5.5.1                            | t <sub>RAMP</sub>           | Ramp Time in forced PWM, low BW case                            | Time from enable to 98% of target value, assuming no residual voltage   |     | 0.3  | 1.65 | ms               |       |
| 5.5.2a                           | DVFS_RISE_QFF               | DVFS timing requirements in forced PWM, rising slope            | Step-duration during DVFS voltage adjustments from 0.6V to 1.4V   |     | 2.9  | 3.2  | 3.5              | mV/μs |
| 5.5.2c                           | DVFS_FALL                   | DVFS timing requirements in forced PWM, falling slope           | Step-duration during DVFS voltage adjustments from 1.4V to 0.6V   |     | 0.45 | 0.53 | 0.61             | mV/μs |
| <b>Switching Characteristics</b> |                             |   |   |     |      |      |                  |       |
| 5.6.1a                           | f <sub>SW</sub>             | Switching Frequency, forced PWM, high or low BW case            | Forced PWM, V <sub>IN</sub> = 3.3V to 5V, V <sub>OUT</sub> = 0.8V to 1.8V, I <sub>OUT</sub> = 1A to 3A  |     |      | 2.3  | MHz              |       |

- (1) PVIN\_Bx must not exceed VSYS
- (2) Refers to DC-regulation only. Transient response typically improves with more headroom. With low headroom, the frequency variation increases for quasi-fixed frequency.

## 6.7 BUCK2, BUCK3 Converter

over operating free-air temperature range (unless otherwise noted)

| POS                               | PARAMETER                   |  | TEST CONDITIONS  | MIN   | TYP  | MAX  | UNIT |
|-----------------------------------|-----------------------------|--|--|-------|------|------|------|
| <b>Electrical Characteristics</b> |                             |  |  |       |      |      |      |
| 6.1.1a                            | V <sub>IN_BUCK23</sub>      | Input Voltage <sup>(1)</sup>   | Buck supply voltage, maximum V <sub>SYS</sub>  | 2.5   |      | 5.5  | V    |
| 6.1.1b                            | V <sub>OUT_BUCK23</sub>     | Buck Output Voltage configurable Range   | Output voltage configurable in 25mV-steps for 0.6V ≤ V <sub>OUT</sub> ≤ 1.4V, in 100mV steps for 1.4V < V <sub>OUT</sub> ≤ 3.4V  | 0.6   |      | 3.4  | V    |
| 6.1.2a                            | I <sub>Q_BUCK23</sub>       | Quiescent Current at 25°C, PFM   | PFM, BUCKx enabled, no load, V <sub>IN</sub> = 5.0V, V <sub>OUT</sub> = 1.2V, T <sub>J</sub> = 25°C  |       | 10   | 13   | μA   |
| 6.1.2b                            | I <sub>Q_BUCK23</sub>       | Quiescent Current -40°C to 125°C, PFM, low BW case   | PFM, BUCKx enabled, no load, V <sub>IN</sub> = 5.0V, V <sub>OUT</sub> = 1.2V, T <sub>J</sub> = -40°C to 125°C  |       | 15   | 43   | μA   |
| 6.1.2c                            | I <sub>Q_BUCK23</sub>       | Quiescent Current -40°C to 150°C, PFM, low BW case   | PFM, BUCKx enabled, no load, V <sub>IN</sub> = 5.0V, V <sub>OUT</sub> = 1.2V, T <sub>J</sub> = -40°C to 150°C  |       | 20   | 63   | μA   |
| 6.1.3a                            | V <sub>HEADROOM_PWM</sub>   | Input to Output Voltage Headroom <sup>(2)</sup>  | Corner cases at maximum load I <sub>OUT</sub> = 85% of I <sub>OUT_MAX</sub>  | 500   |      |      | mV   |
| 6.1.3b                            | V <sub>HEADROOM_PWM</sub>   | Input to Output Voltage Headroom at I <sub>OUT</sub> = I <sub>OUT_MAX</sub> <sup>(2)</sup> | Corner cases at I <sub>OUT</sub> = I <sub>OUT_MAX</sub>  | 700   |      |      | mV   |
| 6.1.4                             | V <sub>OUT_STEP_LOW</sub>   | Output voltage Steps Buck2 and Buck3   | 0.6V ≤ V <sub>OUT</sub> ≤ 1.4V   |       | 25   |      | mV   |
| 6.1.5                             | V <sub>OUT_STEP_HIGH</sub>  | Output voltage Steps Buck2, Buck3  | 1.5V ≤ V <sub>OUT</sub> ≤ 3.4V   |       | 100  |      | mV   |
| 6.1.6a                            | V <sub>OUT_ACC_DC_PWM</sub> | DC Output Voltage Accuracy in forced PWM mode, low and high BW case                        | I <sub>OUT</sub> = I <sub>OUT_MAX</sub> , V <sub>OUT</sub> ≥ 0.7V to 3.4V, V <sub>IN</sub> - V <sub>OUT</sub> > 700 mV forced PWM, low BW case   | -1.5% |      | 1.5% |      |
| 6.1.6b                            | V <sub>OUT_ACC_DC_PWM</sub> | DC Output Voltage Accuracy in forced PWM mode, low and high BW case                        | I <sub>OUT</sub> = I <sub>OUT_MAX</sub> , V <sub>OUT</sub> = 0.6V to 0.7V, V <sub>IN</sub> - V <sub>OUT</sub> > 700 mV forced PWM, low BW case   | -10   |      | 10   | mV   |
| 6.1.6c                            | V <sub>OUT_ACC_DC_PFM</sub> | DC Output Voltage Accuracy in auto-PFM mode, low and high BW case                          | I <sub>OUT</sub> = 1mA, V <sub>OUT</sub> = 0.6V to 3.4V, V <sub>IN</sub> - V <sub>OUT</sub> > 500 mV auto-PFM, low BW case   | -3.0% |      | 3.5% |      |
| 6.1.9                             | R <sub>FB_INPUT</sub>       | Feedback input impedance   | Converter enabled  | 2.3   | 3.75 | 5.0  | MΩ   |
| 6.2.1a                            | V <sub>LOAD_REG_PWM</sub>   | DC Load Regulation, forced PWM, low BW case  | V <sub>IN</sub> = 5.0V, V <sub>OUT</sub> = 1.2V, I <sub>OUT</sub> = 0 to I <sub>OUT_MAX</sub> , forced PWM, low BW case  |       | 0.1  | 0.16 | %/A  |
| 6.2.2a                            | V <sub>LINE_REG</sub>       | DC Line Regulation, forced PWM, low BW case  | V <sub>IN</sub> = 3.3V to 5.5V, V <sub>OUT</sub> = 1.2V, I <sub>OUT</sub> = 1mA and I <sub>OUT_MAX</sub> forced PWM, low BW case, C <sub>OUT</sub> = 40μF                                  |       | 0.1  | 0.16 | %/V  |
| 6.2.3a                            | V <sub>LOAD_TRANSIENT</sub> | Load Transient, V <sub>OUT</sub> =0.75V, auto-PFM, high BW case                            | V <sub>IN</sub> = 5.0V, V <sub>OUT</sub> = 0.75V, I <sub>OUT</sub> = 100mA to 1100mA to 100mA, t <sub>R</sub> = t <sub>F</sub> = 500ns, auto-PFM, high BW case, C <sub>OUT</sub> = 80μF    | -27.5 |      | 27.5 | mV   |
| 6.2.3b                            | V <sub>LOAD_TRANSIENT</sub> | Load Transient, V <sub>OUT</sub> =0.75V, forced PWM, high BW case                          | V <sub>IN</sub> = 5.0V, V <sub>OUT</sub> = 0.75V, I <sub>OUT</sub> = 100mA to 1100mA to 100mA, t <sub>R</sub> = t <sub>F</sub> = 500ns, forced PWM, high BW case, C <sub>OUT</sub> = 80 μF | -27.5 |      | 27.5 | mV   |

## 6.7 BUCK2, BUCK3 Converter (continued)

over operating free-air temperature range (unless otherwise noted)

| POS                              | PARAMETER                   | TEST CONDITIONS   | MIN   | TYP  | MAX  | UNIT |                  |
|----------------------------------|-----------------------------|---|---|------|------|------|------------------|
| 6.2.4a                           | V <sub>LOAD_TRANSIENT</sub> | Load Transient, V <sub>OUT</sub> =1.8V, auto-PFM, low BW case   | V <sub>IN</sub> = 5.0V, V <sub>OUT</sub> = 1.8V, I <sub>OUT</sub> = 1mA to 1A to 1mA, t <sub>R</sub> = t <sub>F</sub> = 1μs, auto-PFM, C <sub>OUT</sub> = 40μF      | -90  |      | 90   | mV               |
| 6.2.4b                           | V <sub>LOAD_TRANSIENT</sub> | Load Transient, V <sub>OUT</sub> =1.8V, forced PWM, low BW case | V <sub>IN</sub> = 5.0V, V <sub>OUT</sub> = 1.8V, I <sub>OUT</sub> = 1mA to 1A to 1mA, t <sub>R</sub> = t <sub>F</sub> = 1μs, forced PWM, C <sub>OUT</sub> = 40μF    | -60  |      | 60   | mV               |
| 6.2.5a                           | V <sub>LINE_TRANSIENT</sub> | Line Transient, V <sub>OUT</sub> =1.2V, forced PWM, low BW case | V <sub>IN</sub> = 3.3V to 5.5V in 50μs, V <sub>OUT</sub> = 1.2V, I <sub>OUT</sub> = 1mA and I <sub>OUT_MAX</sub> , forced PWM, low BW case, C <sub>OUT</sub> = 40μF | -50  |      | 50   | mV               |
| 6.2.6a                           | V <sub>RIPPLE_PP_PWM</sub>  | Forced PWM Mode, low BW case                                    | V <sub>IN</sub> = 5.0V, V <sub>OUT</sub> = 2.5V, forced PWM, low BW case, C <sub>OUT</sub> = 40uF, X5R, ESR = 10mOhm, L = 470nH, DCR = 50mΩ, I <sub>OUT</sub> = 1A  |      | 10   | 20   | mV <sub>PP</sub> |
| 6.2.6b                           | V <sub>RIPPLE_PP_PFM</sub>  | Auto PFM Mode, low BW case                                      | V <sub>IN</sub> = 5.0V, V <sub>OUT</sub> = 2.5V, auto PFM, low BW case, C <sub>OUT</sub> = 40uF, X5R, ESR = 10mOhm, L = 470nH, DCR = 50mΩ, I <sub>OUT</sub> = 20mA  |      | 20   | 40   | mV <sub>PP</sub> |
| 6.3.1                            | I <sub>OUT_MAX</sub>        | Maximum Operating Current                                       |   |      |      | 2.0  | A                |
| 6.3.2                            | I <sub>CURRENT_LIMIT</sub>  | Peak Current Limit  | V <sub>IN</sub> = 2.5V to 5.5V  | 3.1  | 3.9  | 4.7  | A                |
| 6.3.3                            | I <sub>REV_CUR_LIMIT</sub>  | Reverse Peak Current Limit                                      | V <sub>IN</sub> = 2.5V to 5.5V  | -2.0 | -1.5 | -1.0 | A                |
| 6.3.4a                           | R <sub>DSON_HS</sub>        | High Side MOSFET On Resistance, 5V-supply                       | Measured Pin to Pin, V <sub>IN</sub> = 5V   |      |      | 110  | mΩ               |
| 6.3.4b                           | R <sub>DSON_HS</sub>        | High Side MOSFET On Resistance, 3.3V-supply                     | Measured Pin to Pin, V <sub>IN</sub> = 3.3V   |      |      | 135  | mΩ               |
| 6.3.5a                           | R <sub>DSON_LS</sub>        | Low Side MOSFET On Resistance, 5V-supply                        | Measured Pin to Pin, V <sub>IN</sub> = 5V   |      |      | 110  | mΩ               |
| 6.3.5b                           | R <sub>DSON_LS</sub>        | Low Side MOSFET On Resistance, 3.3V-supply                      | Measured Pin to Pin, V <sub>IN</sub> = 3.3V   |      |      | 130  | mΩ               |
| 6.3.6                            | R <sub>DISCHARGE</sub>      | Output Discharge Resistance                                     | Active only when converter is disabled  | 60   | 125  | 200  | Ω                |
| 6.4.1                            | L <sub>SW</sub>             | Output Inductance   | DCR = 50mΩ max  | 330  | 470  | 611  | nH               |
| 6.4.2a                           | C <sub>OUT</sub>            | Output Capacitance in auto-PFM or forced PWM for low BW case    | ESR = 10mΩ max  | 10   |      | 75   | μF               |
| 6.4.3a                           | C <sub>OUT_HIGH_BW</sub>    | Output Capacitance in auto-PFM or forced PWM for high BW case   | ESR = 10mΩ max  | 30   |      | 220  | μF               |
| <b>Timing Requirements</b>       |                             |   |   |      |      |      |                  |
| 6.5.1                            | t <sub>RAMP</sub>           | Ramp Time in quasi-fixed-frequency mode                         | Time from enable to 98% of target value, assuming no residual voltage   | 0.3  |      | 1.65 | ms               |
| 6.5.2a                           | DVFS_SLOPE_QFF              | DVFS timing requirements in forced PWM, low BW case             | Step-duration during DVFS voltage adjustments from 0.6V to 1.4V   | 2.9  | 3.2  | 3.5  | mV/μs            |
| <b>Switching Characteristics</b> |                             |   |   |      |      |      |                  |
| 6.5.2c                           | DVFS_FALL                   | DVFS timing requirements in forced PWM, falling slope           | Step-duration during DVFS voltage adjustments from 1.4V to 0.6V   | 0.45 | 0.53 | 0.61 | mV/μs            |
| 6.6.1a                           | f <sub>SW</sub>             | Switching Frequency, forced PWM, high or low BW case            | Forced PWM, V <sub>IN</sub> = 3.3V to 5V, V <sub>OUT</sub> = 0.8V to 1.8V, I <sub>OUT</sub> = 1A to 1.8A  |      | 2.3  |      | MHz              |

(1) PVIN\_Bx must not exceed VSYS

- (2) Refers to DC-regulation only. Transient response typically improves with more headroom. With low headroom, the frequency variation increases for quasi-fixed frequency.

## 6.8 General Purpose LDOs (LDO1, LDO2)

over operating free-air temperature range (unless otherwise noted)

| POS                               | PARAMETER                    |  | TEST CONDITIONS   | MIN | TYP | MAX  | UNIT              |
|-----------------------------------|------------------------------|--|---|-----|-----|------|-------------------|
| <b>Electrical Characteristics</b> |                              |  |   |     |     |      |                   |
| 7.1.1                             | V <sub>IN_LDO</sub>          | Input Voltage (LDO-mode) <sup>(1)</sup>  | LDO-mode, maximum V <sub>SYS</sub>  | 1.5 |     | 5.5  | V                 |
| 7.1.2                             | V <sub>IN_LDO_BYP</sub>      | Input Voltage (bypass-mode) <sup>(1) (5)</sup>   | Bypass-mode, maximum V <sub>SYS</sub>   | 1.5 |     | 3.4  | V                 |
| 7.1.3                             | V <sub>IN_LDO_LSW</sub>      | Input Voltage (LSW-mode) <sup>(1)</sup>  | LSW-mode, maximum V <sub>SYS</sub>  | 1.5 |     | 5.5  | V                 |
| 7.1.4                             | V <sub>OUT_LDO</sub>         | LDO Output Voltage configurable Range  | LDO mode, with 50-mV steps, V <sub>IN</sub> - V <sub>OUT</sub> > 300 mV   | 0.6 |     | 3.4  | V                 |
| 7.1.5                             | V <sub>OUT_LDO_BYP</sub>     | LDO Output Voltage configurable Range in bypass-mode   | Bypass mode, configurable V <sub>OUT</sub> range with 50-mV steps   | 1.5 |     | 3.4  | V                 |
| 7.1.6                             | V <sub>OUT_STEP</sub>        | Output Voltage Steps   | LDO mode, 0.6V ≤ V <sub>OUT</sub> ≤ 3.4V  |     | 50  |      | mV                |
| 7.1.7                             | V <sub>DROPOUT</sub>         | Dropout Voltage  | V <sub>INmin</sub> ≤ V <sub>IN</sub> ≤ V <sub>INmax</sub> , I <sub>OUT</sub> = 400 mA   |     | 150 | 300  | mV                |
| 7.1.8                             | V <sub>OUT_ACCURACY_H</sub>  | Total DC Output Voltage accuracy, including Voltage References, DC load and line regulations, process and temperature variations | LDO-mode, V <sub>IN</sub> - V <sub>OUT</sub> > 300 mV, V <sub>OUT</sub> ≥ 1V  | -1% |     | 1%   |                   |
| 7.1.9                             | V <sub>OUT_ACCURACY_L</sub>  | Total DC Output Voltage accuracy, including Voltage References, DC load and line regulations, process and temperature variations | LDO-mode, V <sub>IN</sub> - V <sub>OUT</sub> > 300 mV, V <sub>OUT</sub> < 1V  | -10 |     | 10   | mV                |
| 7.1.10                            | R <sub>BYPASS_H</sub>        | Bypass Resistance, high output voltage   | 2.5 V ≤ V <sub>IN</sub> ≤ 3.6 V, V <sub>IN</sub> ≤ V <sub>SYS</sub> , I <sub>OUT</sub> = 400 mA, bypass-mode                  |     |     | 200  | mΩ                |
| 7.1.11                            | R <sub>BYPASS_L</sub>        | Bypass Resistance, low output voltage  | 1.5 V ≤ V <sub>IN</sub> ≤ 2.5 V, V <sub>IN</sub> ≤ V <sub>SYS</sub> , I <sub>OUT</sub> = 400 mA, bypass-mode                  |     |     | 250  | mΩ                |
| 7.1.12                            | R <sub>LSW_H</sub>           | LSW Resistance, high output voltage  | 2.5 V ≤ V <sub>IN</sub> ≤ 5.5 V, V <sub>IN</sub> ≤ V <sub>SYS</sub> , I <sub>OUT</sub> = 400 mA, LSW-mode                     |     |     | 200  | mΩ                |
| 7.1.13                            | R <sub>LSW_L</sub>           | LSW Resistance, low output voltage   | 1.5 V ≤ V <sub>IN</sub> ≤ 2.5 V, V <sub>IN</sub> ≤ V <sub>SYS</sub> , I <sub>OUT</sub> = 400 mA, LSW-mode                     |     |     | 250  | mΩ                |
| 7.2.1                             | V <sub>LOAD_TRANSIENT</sub>  | Transient Load Regulation, ΔV <sub>OUT</sub>   | I <sub>OUT</sub> = 20% to 80% to 20% of I <sub>OUT_MAX</sub> , t <sub>r</sub> = t <sub>f</sub> = 1 μs                         | -35 |     | 35   | mV                |
| 7.2.2                             | V <sub>LINE_TRANSIENT</sub>  | Transient Line Regulation  | V <sub>IN</sub> step = 600 mV <sub>PP</sub> , t <sub>R</sub> = t <sub>F</sub> = 10 μs, LDO not in dropout condition, LDO-mode | -25 |     | 25   | mV                |
| 7.2.3                             | NOISE <sub>RMS</sub>         | RMS Noise  | 100 Hz < f ≤ 100 kHz, V <sub>IN</sub> = 3.3 V, V <sub>OUT</sub> = 1.8 V, I <sub>OUT</sub> = 300 mA                            |     | 600 |      | μV <sub>RMS</sub> |
| 7.2.4                             | V <sub>RIPPLE</sub>          | Voltage Ripple   |   |     |     | 5    | mV <sub>PP</sub>  |
| 7.3.1                             | I <sub>OUT_MAX</sub>         | Output Current   | V <sub>PVIN_LDOxmin</sub> ≤ V <sub>IN</sub> ≤ V <sub>PVIN_LDOxmax</sub> , Applies to LDO-, bypass- and LSW-mode               |     |     | 400  | mA                |
| 7.3.2                             | I <sub>CURRENT_LIMIT</sub>   | Short Circuit Current Limit  | V <sub>IN</sub> = 3.6V, V <sub>OUT</sub> = 0V   | 600 | 980 | 1600 | mA                |
| 7.3.3                             | I <sub>IN_RUSH_LDO</sub>     | LDO Inrush Current   | LDO-mode, with maximum 20-μF load connected to VLDOx, I <sub>OUT</sub> = 0 mA or 400mA  |     |     | 1500 | mA                |
| 7.3.4                             | I <sub>IN_RUSH_LDO_BYP</sub> | LDO Inrush Current in bypass-mode  | Bypass-mode, with maximum 50-μF load connected to VLDOx   |     |     | 1500 | mA                |
| 7.3.5                             | I <sub>IN_RUSH_LDO_LSW</sub> | LDO Inrush Current in LSW-mode   | LSW-mode, with maximum 50-μF load connected to VLDOx  |     |     | 1500 | mA                |
| 7.3.6                             | R <sub>DISCHARGE</sub>       | Pulldown Discharge Resistance at LDO Output  | Active only when converter is disabled. Applies to LDO-, bypass- and LSW-mode   | 100 | 200 | 300  | Ω                 |

## 6.8 General Purpose LDOs (LDO1, LDO2) (continued)

over operating free-air temperature range (unless otherwise noted)

| POS                        | PARAMETER                   | TEST CONDITIONS   | MIN | TYP | MAX  | UNIT              |
|----------------------------|-----------------------------|---|-----|-----|------|-------------------|
| 7.3.7a                     | $I_{Q\_ACTIVE\_LDO}$        | Quiescent Current in ACTIVE state at 25°C, LDO-mode                   |     | 50  | 62   | $\mu\text{A}$     |
| 7.3.7b                     | $I_{Q\_ACTIVE\_LDO}$        | Quiescent Current in ACTIVE state -40°C to 125°C, LDO-mode            |     | 50  | 65   | $\mu\text{A}$     |
| 7.3.7b                     | $I_{Q\_ACTIVE\_LDO}$        | Quiescent Current in ACTIVE state -40°C to 150°C, LDO-mode            |     | 50  | 66   | $\mu\text{A}$     |
| 7.3.8a                     | $I_{Q\_ACTIVE\_LDO\_BY\_P}$ | Quiescent Current in ACTIVE state at 25°C, bypass-mode                |     | 43  | 48   | $\mu\text{A}$     |
| 7.3.8b                     | $I_{Q\_ACTIVE\_LDO\_BY\_P}$ | Quiescent Current in ACTIVE state -40°C to 125°C, bypass-mode         |     | 43  | 50   | $\mu\text{A}$     |
| 7.3.8b                     | $I_{Q\_ACTIVE\_LDO\_BY\_P}$ | Quiescent Current in ACTIVE state -40°C to 150°C, bypass-mode         |     | 43  | 50   | $\mu\text{A}$     |
| 7.3.9a                     | $I_{Q\_ACTIVE\_LDO\_LS\_W}$ | Quiescent Current in ACTIVE state at 25°C, LSW-mode                   |     | 46  | 53   | $\mu\text{A}$     |
| 7.3.9b                     | $I_{Q\_ACTIVE\_LDO\_LS\_W}$ | Quiescent Current in ACTIVE state -40°C to 125°C, LSW-mode            |     | 46  | 53   | $\mu\text{A}$     |
| 7.3.9b                     | $I_{Q\_ACTIVE\_LDO\_LS\_W}$ | Quiescent Current in ACTIVE state -40°C to 150°C, LSW-mode            |     | 46  | 54   | $\mu\text{A}$     |
| 7.4.1                      | $C_{IN}$                    | Input Filtering Capacitance <sup>(2)</sup>                            | 1.6 | 2.2 |      | $\mu\text{F}$     |
| 7.4.2                      | $C_{OUT}$                   | Output Filtering Capacitance <sup>(3)</sup>                           | 1.6 | 2.2 | 4    | $\mu\text{F}$     |
| 7.4.3                      | $C_{OUT\_TOTAL}$            | Total Capacitance at Output (Local + POL), LDO-mode <sup>(4)</sup>    |     |     | 20   | $\mu\text{F}$     |
| 7.4.4                      | $C_{OUT\_TOTAL\_BYP}$       | Total Capacitance at Output (Local + POL), bypass-mode <sup>(4)</sup> |     |     | 50   | $\mu\text{F}$     |
| 7.4.5                      | $C_{OUT\_TOTAL\_LSW}$       | Total Capacitance at Output (Local + POL), LSW-mode <sup>(4)</sup>    |     |     | 50   | $\mu\text{F}$     |
| 7.4.6                      | $C_{ESR}$                   | Filtering capacitor ESR max   |     | 10  | 20   | m $\Omega$        |
| <b>Timing Requirements</b> |                             |   |     |     |      |                   |
| 7.5.1                      | $t_{RAMP}$                  | Ramp Time LDO in LDO- and bypass-mode                                 |     |     | 950  | $\mu\text{s}$     |
| 7.5.2                      | $t_{RAMP\_SLEW}$            | Ramp up Slew Rate in LDO- and bypass-mode                             |     |     | 12   | mV/ $\mu\text{s}$ |
| 7.5.3                      | $t_{RAMP\_LSW}$             | Ramp Time LSW-mode  |     |     | 1250 | $\mu\text{s}$     |
| 7.5.4                      | $t_{RAMP\_SLEW}$            | Ramp up Slew Rate in LSW-mode   |     |     | 12   | mV/ $\mu\text{s}$ |

## 6.8 General Purpose LDOs (LDO1, LDO2) (continued)

over operating free-air temperature range (unless otherwise noted)

| POS   | PARAMETER                  | TEST CONDITIONS             | MIN  | TYP | MAX | UNIT |
|-------|----------------------------|-----------------------------|--|-----|-----|------|
| 7.5.5 | t <sub>TRANS_1P8_3P3</sub> | Transition Time 1.8V - 3.3V | V <sub>IN</sub> = 4.0V, I <sub>OUT</sub> = 300mA |     |     | ms   |
| 7.5.6 | t <sub>TRANS_3P3_1P8</sub> | Transition Time 3.3V - 1.8V | V <sub>IN</sub> = 4.0V, I <sub>OUT</sub> = 300mA |     |     | ms   |

- (1) PVIN\_LDOx must not exceed V<sub>SYS</sub>
- (2) Input capacitors must be placed as close as possible to the device pins.
- (3) When DC voltage is applied to a ceramic capacitor, the effective capacitance is reduced due to DC bias effect. The table above therefore lists the minimum value as CAPACITANCE. In order to meet the minimum capacitance requirement, the nominal value of the capacitor must be scaled accordingly to take the drop of capacitance into account for a given dc voltage at the outputs of regulators.
- (4) Additional capacitance, including local and POL, beyond the specified value impacts the LDO's stability.
- (5) PVIN\_LDOx voltage must be within (configured V<sub>OUT</sub>) and (configured V<sub>OUT</sub> + 200mV), maximum 3.6V.

## 6.9 General Purpose LDOs (LDO3, LDO4)

over operating free-air temperature range (unless otherwise noted)

| POS                               | PARAMETER                    | TEST CONDITIONS   | MIN  | TYP | MAX | UNIT              |
|-----------------------------------|------------------------------|---|--|-----|-----|-------------------|
| <b>Electrical Characteristics</b> |                              |   |  |     |     |                   |
| 8.1.1                             | V <sub>IN</sub>              | Input Voltage (LDO-mode) <sup>(1)</sup>   | LDO-mode, maximum V <sub>VSYS</sub>  |     |     | V                 |
| 8.1.2                             | V <sub>IN</sub>              | Input Voltage (LSW-mode) <sup>(1)</sup>   | LSW-mode, maximum V <sub>VSYS</sub>  |     |     | V                 |
| 8.1.3                             | V <sub>OUT</sub>             | LDO Output Voltage configurable Range   | V <sub>IN</sub> = 2.2V to 5.5V, maximum V <sub>VSYS</sub>  |     |     | V                 |
| 8.1.4                             | V <sub>OUT_STEP</sub>        | Output voltage Steps  | 1.2V ≤ V <sub>OUT</sub> ≤ 3.3V   |     |     | mV                |
| 8.1.5                             | V <sub>DROPOUT</sub>         | Dropout Voltage   | V <sub>INmin</sub> ≤ V <sub>IN</sub> ≤ V <sub>INmax</sub> , I <sub>OUT</sub> = I <sub>OUT_MAX</sub>  |     |     | mV                |
| 8.1.6                             | V <sub>OUT_DC_ACCURACY</sub> | Total DC accuracy including DC load and line regulation for all valid output voltages | LDO-mode, V <sub>IN</sub> - V <sub>OUT</sub> > 300 mV  |     |     | %                 |
| 8.1.7                             | R <sub>BYPASS</sub>          | Bypass resistance in LSW-mode   | V <sub>IN</sub> = 3.3V, I <sub>OUT</sub> = 100mA, Loadswitch-mode enabled  |     |     | Ω                 |
| 8.2.1                             | V <sub>LOAD_TRANSIENT</sub>  | Transient load regulation, ΔV <sub>OUT</sub>  | V <sub>IN</sub> = 3.3V, V <sub>OUT</sub> = 1.80V, I <sub>OUT</sub> = 20% of I <sub>OUT_MAX</sub> to 80% of I <sub>OUT_MAX</sub> in 1μs, C <sub>OUT</sub> = 2.2μF |     |     | mV                |
| 8.2.2                             | V <sub>LINE_TRANSIENT</sub>  | Transient line regulation, ΔV <sub>OUT</sub> / V <sub>OUT</sub>                       | On mode, not under dropout condition, V <sub>IN</sub> step = 600 mV <sub>PP</sub> , t <sub>r</sub> = t <sub>f</sub> = 10μs                                       |     |     | mV                |
| 8.2.3                             | NOISE <sub>RMS</sub>         | RMS Noise   | LDO-mode, f=100Hz to 100KHz, V <sub>IN</sub> = 3.3V, V <sub>OUT</sub> = 1.8V, I <sub>OUT</sub> = 300mA   |     |     | μV <sub>RMS</sub> |
| 8.2.4                             | PSRR <sub>1KHZ</sub>         | Power Supply Ripple Rejection   | LDO-mode, V <sub>IN</sub> = 3.3V, V <sub>OUT</sub> = 1.8V, I <sub>OUT</sub> = 300mA  |     |     | db                |
| 8.2.5                             | PSRR <sub>10KHZ</sub>        | Power Supply Ripple Rejection   | LDO-mode, V <sub>IN</sub> = 3.3V, V <sub>OUT</sub> = 1.8V, I <sub>OUT</sub> = 300mA  |     |     | db                |
| 8.2.6                             | PSRR <sub>100KHZ</sub>       | Power Supply Ripple Rejection   | LDO-mode, V <sub>IN</sub> = 3.3V, V <sub>OUT</sub> = 1.8V, I <sub>OUT</sub> = 300mA  |     |     | db                |
| 8.2.7                             | PSRR <sub>1MHZ</sub>         | Power Supply Ripple Rejection   | LDO-mode, V <sub>IN</sub> = 3.3V, V <sub>OUT</sub> = 1.8V, I <sub>OUT</sub> = 300mA  |     |     | db                |
| 8.3.1                             | I <sub>OUT_MAX</sub>         | Output Current  |  |     |     | mA                |
| 8.3.2                             | I <sub>CURRENT_LIMIT</sub>   | Short Circuit Current Limit   | V <sub>IN</sub> = 3.6V, V <sub>OUT</sub> = 0V, Tested under a pulsed load condition  |     |     | mA                |
| 8.3.3                             | I <sub>IN_RUSH</sub>         | LDO inrush current  | LDO- or LSW-mode, V <sub>IN</sub> = 3.3V and then LDO is enabled, C <sub>OUT</sub> = 4μF, I <sub>OUT</sub> = 0 mA or 300mA                                       |     |     | mA                |
| 8.3.4                             | R <sub>DISCHARGE</sub>       |   | Active only when converter is disabled   |     |     | Ω                 |

## 6.9 General Purpose LDOs (LDO3, LDO4) (continued)

over operating free-air temperature range (unless otherwise noted)

| POS                        | PARAMETER              |   | TEST CONDITIONS  | MIN | TYP | MAX | UNIT              |
|----------------------------|------------------------|---|--|-----|-----|-----|-------------------|
| 8.3.5a                     | $I_{Q\_ACTIVE}$        | Quiescent Current in ACTIVE state at 25°C                     | $V_{VSYS} = V_{IN} = 3.3\text{ V}$ , $I_{OUT} = 0\text{ mA}$<br>Applies to LDO-mode,<br>$T_J = 25^\circ\text{C}$                           |     | 25  | 30  | $\mu\text{A}$     |
| 8.3.5b                     | $I_{Q\_ACTIVE}$        | Quiescent Current in ACTIVE state -40°C to 125°C              | $V_{VSYS} = V_{IN} = 3.3\text{ V}$ , $I_{OUT} = 0\text{ mA}$<br>Applies to LDO-mode,<br>$T_J = -40^\circ\text{C}$ to $125^\circ\text{C}$   |     | 25  | 40  | $\mu\text{A}$     |
| 8.3.5b                     | $I_{Q\_ACTIVE}$        | Quiescent Current in ACTIVE state -40°C to 150°C              | $V_{VSYS} = V_{IN} = 3.3\text{ V}$ , $I_{OUT} = 0\text{ mA}$ ,<br>Applies to LDO-mode,<br>$T_J = -40^\circ\text{C}$ to $150^\circ\text{C}$ |     | 25  | 40  | $\mu\text{A}$     |
| 8.3.5c                     | $I_{Q\_ACTIVE}$        | Quiescent Current in ACTIVE state at 25°C                     | $V_{VSYS} = V_{IN} = 3.3\text{ V}$ , $I_{OUT} = 0\text{ mA}$<br>Applies to LSW-mode,<br>$T_J = 25^\circ\text{C}$                           |     | 60  | 112 | $\mu\text{A}$     |
| 8.3.5d                     | $I_{Q\_ACTIVE}$        | Quiescent Current in ACTIVE state -40°C to 125°C              | $V_{VSYS} = V_{IN} = 3.3\text{ V}$ , $I_{OUT} = 0\text{ mA}$<br>Applies to LSW-mode,<br>$T_J = -40^\circ\text{C}$ to $125^\circ\text{C}$   |     | 70  | 145 | $\mu\text{A}$     |
| 8.3.5d                     | $I_{Q\_ACTIVE}$        | Quiescent Current in ACTIVE state -40°C to 150°C              | $V_{VSYS} = V_{IN} = 3.3\text{ V}$ , $I_{OUT} = 0\text{ mA}$ ,<br>Applies to LSW-mode,<br>$T_J = -40^\circ\text{C}$ to $150^\circ\text{C}$ |     | 70  | 145 | $\mu\text{A}$     |
| 8.4.1                      | $C_{IN}$               | Input Filtering Capacitance (2)                               |  | 2.2 | 4.7 |     | $\mu\text{F}$     |
| 8.4.2                      | $C_{OUT}$              | Output Filtering Capacitance (2)                              | Connected from VLDOx to GND,<br>LDO-mode   | 1.6 | 2.2 | 4   | $\mu\text{F}$     |
| 8.4.3a                     | $C_{OUT\_TOTAL\_FAST}$ | Total Capacitance at Output (Local + POL), fast ramp-time (3) | 1 MHz < f < 10 MHz, impedance between output and point-of-load maximum 6nH   |     |     | 15  | $\mu\text{F}$     |
| 8.4.3b                     | $C_{OUT\_TOTAL\_SLOW}$ | Total Capacitance at Output (Local + POL), slow ramp-time (3) | 1 MHz < f < 10 MHz, impedance between output and point-of-load maximum 6nH   |     |     | 30  | $\mu\text{F}$     |
| 8.4.4                      | $C_{ESR}$              | Filtering capacitor ESR max                                   | 1MHz to 10MHz  |     | 10  | 20  | m $\Omega$        |
| <b>Timing Requirements</b> |                        |   |  |     |     |     |                   |
| 8.5.1a                     | $t_{RAMP\_FAST}$       | Ramp Time fast  | Measured from enable to 98% of target value, LDO-mode, measured when enabled individually, assuming no residual voltage                    |     |     | 660 | $\mu\text{s}$     |
| 8.5.1b                     | $t_{RAMP\_SLOW}$       | Ramp Time slow  | Measured from enable to 98% of target value, LDO-mode, measured when enabled individually, assuming no residual voltage                    |     |     | 2.3 | ms                |
| 8.5.2a                     | $t_{RAMP\_SLEW\_FAST}$ | Ramp Up Slew Rate fast  | LDO- or LSW-mode, measured from 0.5V to target value   |     |     | 25  | mV/ $\mu\text{s}$ |
| 8.5.2b                     | $t_{RAMP\_SLEW\_SLOW}$ | Ramp Up Slew Rate slow  | LDO- or LSW-mode, measured from 0.5V to target value   |     |     | 9   | mV/ $\mu\text{s}$ |

(1)  $PVIN\_LDOx$  must not exceed  $VSYS$

(2) When DC voltage is applied to a ceramic capacitor, the effective capacitance is reduced due to DC bias effect. The table above therefore lists the minimum value as CAPACITANCE. In order to meet the minimum capacitance requirement, the nominal value of the capacitor must be scaled accordingly to take the drop of capacitance into account for a given dc voltage at the outputs of regulators.

(3) Additional capacitance, including local and POL, beyond the specified value impacts the LDO's stability.

## 6.10 GPIOs and multi-function pins (EN/PB/VSENSE, nRSTOUT, nINT, GPO1, GPO2, GPIO, MODE/RESET, MODE/STBY, VSEL\_SD/VSEL\_DDR)

over operating free-air temperature range (unless otherwise noted)

| POS                               | PARAMETER                    | TEST CONDITIONS   | MIN   | TYP  | MAX  | UNIT |    |
|-----------------------------------|------------------------------|---|---|------|------|------|----|
| <b>Electrical Characteristics</b> |                              |   |   |      |      |      |    |
| 9.1.1                             | $V_{OL}$                     | Low-level Output Voltage (open-drain)   | VIO = 3.6V, I <sub>OL</sub> = 2mA, GPO1, GPO2, GPIO, nRSTOUT, nINT          |      |      | 0.40 | V  |
| 9.1.2                             | $V_{IL}$                     | Low-level Input Voltage   | EN/PB, MODE/STBY, MODE/RESET and VSEL_SD/VSEL_DDR, GPIO                     |      |      | 0.4  | V  |
| 9.1.3                             | $V_{IH}$                     | High-level Input Voltage  | EN/PB, MODE/STBY, MODE/RESET and VSEL_SD/VSEL_DDR, GPIO                     |      |      | 1.26 | V  |
| 9.1.4                             | $V_{VSENSE}$                 | VSENSE Comparator Threshold (EN/PB/VSENSE)  | 1.08  | 1.20 | 1.32 | V    |    |
| 9.1.5                             | $V_{VSENSE\_HYS}$            | VSENSE Comparator Hysteresis (EN/PB/VSENSE)   | 8   | 30   | 55   | mV   |    |
| 9.1.6                             | $I_{LKG}$                    | Input leakage current (GPIO, EN/PB/VSENSE, MODE/STBY, MODE/RESET, VSEL_SD/VSEL_DDR)               | V <sub>IN</sub> = 3.3 V   |      |      | 1.0  | μA |
| 9.1.7                             | $C_{IN}$                     | Internal input pin capacitance (GPIO, EN/PB/VSENSE, MODE/STBY, MODE/RESET, VSEL_SD/VSEL_DDR)      |   |      |      | 10   | pF |
| 9.1.8                             | $I_{PD}$                     | pull-down current, available 100us after VSYS is applied  | 18  | 25   | 35   | nA   |    |
| 9.1.9                             | $I_{LKG\_VSY\_ONLY}$         | Pin leakage when VSYS is present, but digital supply VDD1P8 is not                                | SDA only  |      |      | 1    | μA |
| 9.1.10                            | $V_{PIN\_VSY\_ONLY}$         | Pin voltage when VSYS is present, but digital supply VDD1P8 is not                                | GPO1, GPO2, GPIO, nRSTOUT, nINT, I <sub>OL</sub> =2mA                       |      |      | 0.4  | V  |
| <b>Timing Requirements</b>        |                              |   |   |      |      |      |    |
| 9.2.1a                            | $t_{FALL}$                   | Output buffer fall time (90% to 10%)  | GPO1, GPO2, GPIO, nRSTOUT, nINT, C <sub>OUT</sub> = 10pF                    |      |      | 50   | ns |
| 9.2.1b                            | $t_{RISE}$                   | GPIO Output buffer rise time (10% to 90%)   | GPIO, applicable in Multi-PMIC-configuration                                |      |      | 5    | μs |
| 9.2.1.1                           | $t_{DLY\_FALL}$              | Output buffer falling time delay (input crossing 50% to output crossing 50%)                      | C <sub>OUT</sub> = 10pF   |      |      | 50   | ns |
| 9.2.2.1                           | $t_{DLY\_RISE}$              | Open Drain Output buffer rising time delay (digital input to output crossing 50%)                 | C <sub>OUT</sub> = 10pF, R <sub>PU</sub> =1k (external pull up), VIO = 1.8V |      |      | 300  | ns |
| 9.2.2.3                           | FLT_HIGH <sub>Duration</sub> | Time the digital has allotted for the test to see if the pin is able to be pulled high internally | C <sub>OUT</sub> = 10pF   |      |      | 15   | μs |
| 9.2.2.4                           | FLT_LOW <sub>Duration</sub>  | Time the digital has allotted for the test to see if the pin is able to be pulled low internally  | C <sub>OUT</sub> = 10pF   |      |      | 15   | μs |
| 9.2.2a                            | $t_{PB\_ON\_SLOW}$           | EN/PB/VSENSE, Wait Time PB, ON request, slow  | 540   | 600  | 660  | ms   |    |
| 9.2.2b                            | $t_{PB\_ON\_FAST}$           | EN/PB/VSENSE, Wait Time PB, ON request, fast  | 180   | 200  | 220  | ms   |    |
| 9.2.3                             | $t_{PB\_OFF}$                | EN/PB/VSENSE, Wait Time PB, OFF request   | 7.2   | 8.0  | 8.8  | s    |    |

## 6.10 GPIOs and multi-function pins (EN/PB/VSENSE, nRSTOUT, nINT, GPO1, GPO2, GPIO, MODE/RESET, MODE/STBY, VSEL\_SD/VSEL\_DDR) (continued)

over operating free-air temperature range (unless otherwise noted)

| POS    | PARAMETER                       | TEST CONDITIONS   | MIN  | TYP  | MAX  | UNIT |
|--------|---------------------------------|---|------|------|------|------|
| 9.2.4  | t <sub>PB_RISE_DEGL</sub>       | EN/PB/VSENSE, Deglitch time PB, rising edge                                 | 115  | 200  | 275  | ms   |
| 9.2.5  | t <sub>PB_INT_DEGL</sub>        | EN/PB/VSENSE, Deglitch time PB, rising or falling edge                      | 59   | 100  | 137  | ms   |
| 9.2.6  | t <sub>DEGL_EN_Rise_Slow</sub>  | EN/PB/VSENSE, DeglitchTime EN slow, rising                                  | 45   | 50   | 55   | ms   |
| 9.2.7  | t <sub>DEGL_EN_Rise_Fast</sub>  | EN/PB/VSENSE, DeglitchTime EN fast, rising                                  | 60   | 120  | 150  | µs   |
| 9.2.8  | t <sub>DEGL_EN_Fall</sub>       | EN/PB/VSENSE, DeglitchTime EN, falling                                      | 50   | 70   | 93   | µs   |
| 9.2.9  | t <sub>DEGL_VSENSE_Rise</sub>   | VSENSE rising: only gated by VSYS <sub>POR_Rising</sub> and VSENSE-voltage  |      | N/A  |      |      |
| 9.2.10 | t <sub>DEGL_VSENSE_Fall</sub>   | EN/PB/VSENSE, DeglitchTime VSENSE, falling, regardless of fast/slow setting | 50   | 70   | 93   | µs   |
| 9.2.11 | t <sub>DEGL_EN/VSENSE_I2C</sub> | EN/VSENSE falling edge deglitch time after I2C-triggered shutdown           | 12.5 | 25   | 37.5 | µs   |
| 9.2.12 | t <sub>DEGL_RESET</sub>         | MODE/RESET, Deglitch Time RESET   | 90   | 120  | 150  | µs   |
| 9.2.13 | t <sub>DEGL_MFP</sub>           | Deglitch Time MODE/STBY, MODE(not/RESET), VSEL_SD/VSEL_DDR                  | 90   | 120  | 150  | µs   |
| 9.2.14 | t <sub>DEGL_GPIO</sub>          | Deglitch Time GPIO  | 6.6  | 15.6 | 18   | µs   |
| 9.2.15 | t <sub>REACTION_ON</sub>        | ON-request propagation delay (after deglitch)                               |      | 75   | 103  | µs   |
| 9.2.16 | t <sub>REACTION_OFF</sub>       | OFF-request propagation delay (after deglitch)                              | 39   | 56   | 73.5 | µs   |

## 6.11 Voltage and Temperature Monitors

over operating free-air temperature range (unless otherwise noted)

| POS                               | PARAMETER  | TEST CONDITIONS  | MIN   | TYP   | MAX   | UNIT |
|-----------------------------------|--|--|-------|-------|-------|------|
| <b>Electrical Characteristics</b> |  |  |       |       |       |      |
| 10.1.1                            | V <sub>BUCKx_UV_TH_5</sub> , V <sub>LDOx_UV_TH_5</sub>   | Undervoltage monitoring for buck output, programable low-going threshold accuracy                |       | -5%   |       |      |
| 10.1.2                            | V <sub>BUCKx_UV_TH_10</sub> , V <sub>LDOx_UV_TH_10</sub> | Undervoltage monitoring for buck output and LDO output, programable low-going threshold accuracy |       | -10%  |       |      |
| 10.1.3                            | V <sub>BUCKx_UV_H_ACC</sub> , V <sub>LDOx_UV_H_ACC</sub> | Undervoltage Threshold Accuracy, V <sub>OUT</sub> ≥ 1V   |       | -1.5% | +1.5% |      |
| 10.1.4                            | V <sub>BUCKx_UV_L_ACC</sub> , V <sub>LDOx_UV_L_ACC</sub> | Undervoltage Threshold Accuracy, V <sub>OUT</sub> < 1V   |       | -10   | +10   | mV   |
| 10.1.5                            | V <sub>BUCKx_UV_HYS</sub> , V <sub>LDOx_UV_HYS</sub>     | Undervoltage Hysteresis  | 0.25% | 1%    | 1.75% |      |

## 6.11 Voltage and Temperature Monitors (continued)

over operating free-air temperature range (unless otherwise noted)

| POS                        | PARAMETER   | TEST CONDITIONS  | MIN  | TYP | MAX | UNIT |    |
|----------------------------|---|--|--|-----|-----|------|----|
| 10.1.6                     | $V_{\text{BUCKx\_SCG\_TH}}$ ,<br>$V_{\text{LDOx\_SCG\_TH}}$   | Short-circuit (SCG) and residual voltage (RV) detection low-going threshold                | 220  | 260 | 300 | mV   |    |
| 10.1.7                     | $V_{\text{BUCKx\_SCG\_HYS}}$ ,<br>$V_{\text{LDOx\_SCG\_HYS}}$ | Short-circuit (SCG) and residual voltage (RV) detection threshold hysteresis               |  | 75  |     | mV   |    |
| 10.2.1a                    | $T_{\text{WARM\_Rising}}$                                     | Temperature rising Warning Threshold (WARM)  | for each of the four sensors                     | 110 | 120 | 130  | °C |
| 10.2.1b                    | $T_{\text{WARM\_Falling}}$                                    | Temperature falling Warning Threshold (WARM)   | for each of the four sensors                     | 105 | 115 | 125  | °C |
| 10.2.2a                    | $T_{\text{HOT\_Rising}}$                                      | Temperature rising Shutdown Threshold (TSD, HOT)   | for each of the four sensors                     | 130 | 140 | 150  | °C |
| 10.2.2b                    | $T_{\text{HOT\_Falling}}$                                     | Temperature falling Shutdown Threshold (TSD, HOT)  | for each of the four sensors                     | 125 | 135 | 145  | °C |
| 10.2.3                     | $T_{\text{HYS}}$  | Temperature Hysteresis for WARM  | for each of the four sensors                     |     | -5  |      | °C |
| <b>Timing Requirements</b> |   |  |  |     |     |      |    |
| 10.3.1a                    | $t_{\text{DEGLITCH}}$   | Fault Detection Deglitch Time for Undervoltage (UV) and Short to GND (SCG)                 | Measured from UV/SCG event                       | 13  | 20  | 27   | µs |
| 10.3.1b                    | $t_{\text{DEGLITCH\_OC\_short}}$                              | Fault Detection Deglitch Time for Over Current (OC), rising edge, short                    | Measured from OC event, rising edge              | 26  | 35  | 45   | µs |
| 10.3.1c                    | $t_{\text{DEGLITCH\_OC\_long}}$                               | Fault Detection Deglitch Time for Over Current (OC), rising edge, long                     | Measured from OC event, rising edge              | 1.6 | 2   | 2.2  | ms |
| 10.3.2a                    | $t_{\text{REACTION}}$   | Fault Reaction Time for Undervoltage (UV) and Short to GND (SCG) (including deglitch time) | Measured from UV/SCG event to nINT pulled low    | 26  | 40  | 54   | µs |
| 10.3.2b                    | $t_{\text{REACTION\_OC\_short}}$                              | Fault Reaction Time for Over Current (OC) (including deglitch time)                        | Measured from UV/OC/SCG event to nINT pulled low | 45  | 65  | 81   | µs |
| 10.3.2c                    | $t_{\text{REACTION\_OC\_long}}$                               | Fault Detection Deglitch Time for Over Current (OC), rising edge, long                     | Measured from OC event, rising edge              | 1.6 | 2   | 2.2  | ms |
| 10.3.2d                    | $t_{\text{REACTION\_WARM}}$                                   | Fault Reaction Time for Temperature Warning (WARM), Thermal Shutdown (TSD / HOT)           | Measured from WARM/HOT event to nINT pulled low  |     |     | 525  | µs |

## 6.12 I<sup>2</sup>C Interface

Over operating free-air temperature range (unless otherwise noted). Device supports standard mode (100 kHz), fast mode (400 kHz), and fast mode+ (1 MHz) when VIO is 3.3V or 1.8V.

| POS                               | PARAMETER         | TEST CONDITIONS                 | MIN   | TYP  | MAX  | UNIT |    |
|-----------------------------------|-------------------|---------------------------------|---|------|------|------|----|
| <b>Electrical Characteristics</b> |                   |                                 |   |      |      |      |    |
| 11.1.1                            | $V_{\text{OL}}$   | Low-level Output Voltage        | VIO = 3.6V, $I_{\text{OL}} = 3\text{mA}$ for Standard mode and Fast mode, $I_{\text{OL}} = 20\text{mA}$ for Fast mode+, SDA |      | 0.40 | V    |    |
| 11.1.2                            | $V_{\text{IL}}$   | Low-level Input Voltage         | SDA, SCL  |      | 0.40 | V    |    |
| 11.1.3                            | $V_{\text{IH}}$   | High-level Input Voltage        | SDA, SCL  | 1.26 |      | V    |    |
| 11.1.4                            | $V_{\text{HYST}}$ | Input buffer Hysteresis         | EN_BP/VSENSE, MODE_RESET, MODE_STBY, SDA, SCL, GPIO   | 100  |      | 500  | mV |
| 11.1.5                            | $C_{\text{B}}$    | Capacitive Load for SDA and SCL |   |      | 400  | pF   |    |

## 6.12 I<sup>2</sup>C Interface (continued)

Over operating free-air temperature range (unless otherwise noted). Device supports standard mode (100 kHz), fast mode (400 kHz), and fast mode+ (1 MHz) when VIO is 3.3V or 1.8V.

| POS                        | PARAMETER    | TEST CONDITIONS                                      | MIN  | TYP | MAX  | UNIT    |
|----------------------------|--------------|--|--|-----|------|---------|
| <b>Timing Requirements</b> |              |  |  |     |      |         |
| 11.2.1                     | $f_{SCL}$    | Serial Clock Frequency                               | Standard mode  |     | 100  | kHz     |
| 11.2.2                     |              |  | Fast mode  |     | 400  |         |
| 11.2.3                     |              |  | Fast mode+   |     | 1    | MHz     |
| 11.3.1                     | $t_{LOW}$    | SCL low Time   | Standard mode  |     | 4.7  | $\mu$ s |
| 11.3.2                     |              |  | Fast mode  |     | 1.3  |         |
| 11.3.3                     |              |  | Fast mode+   |     | 0.50 |         |
| 11.4.1                     | $t_{HIGH}$   | SCL high Time  | Standard mode  |     | 4.0  | $\mu$ s |
| 11.4.2                     |              |  | Fast mode  |     | 0.60 |         |
| 11.4.3                     |              |  | Fast mode+   |     | 0.26 |         |
| 11.5.1                     | $t_{SU,DAT}$ | Data setup Time                                      | Standard mode  |     | 250  | ns      |
| 11.5.2                     |              |  | Fast mode  |     | 100  |         |
| 11.5.3                     |              |  | Fast mode+   |     | 50   |         |
| 11.6.1                     | $t_{HD,DAT}$ | Data hold Time                                       | Standard mode  |     | 10   | ns      |
| 11.6.2                     |              |  | Fast mode  |     | 10   |         |
| 11.6.6                     |              |  | Fast mode+   |     | 10   |         |
| 11.7.1                     | $t_{SU,STA}$ | Setup Time for a Start or a REPEATED Start Condition | Standard mode  |     | 4.7  | $\mu$ s |
| 11.7.2                     |              |  | Fast mode  |     | 0.60 |         |
| 11.7.3                     |              |  | Fast mode+   |     | 0.26 |         |
| 11.8.1                     | $t_{HD,STA}$ | Hold Time for a Start or a REPEATED Start Condition  | Standard mode  |     | 4.7  | $\mu$ s |
| 11.8.2                     |              |  | Fast mode  |     | 0.60 |         |
| 11.8.3                     |              |  | Fast mode+   |     | 0.26 |         |
| 11.9.1                     | $t_{BUF}$    | Bus free Time between a STOP and Start Condition     | Standard mode  |     | 4.7  | $\mu$ s |
| 11.9.2                     |              |  | Fast mode  |     | 1.3  |         |
| 11.9.3                     |              |  | Fast mode+   |     | 0.50 |         |
| 11.10.1                    | $t_{SU,STO}$ | Setup Time for a STOP Condition                      | Standard mode  |     | 0.60 | $\mu$ s |
| 11.10.2                    |              |  | Fast mode  |     | 0.60 |         |
| 11.10.3                    |              |  | Fast mode+   |     | 0.26 |         |
| 11.10.1                    | $t_{rDA}$    | Rise Time of SDA Signal                              | Standard mode, VIO = 1.8V, R <sub>PU</sub> = 10 k $\Omega$ and C <sub>B</sub> = 400 pF |     | 1000 | ns      |
| 11.10.2                    |              |  | Fast mode, VIO = 1.8V, R <sub>PU</sub> = 1 k $\Omega$ and C <sub>B</sub> = 400 pF      |     | 20   |         |
| 11.10.3                    |              |  | Fast mode+, VIO = 1.8V, R <sub>PU</sub> = 330 $\Omega$ and C <sub>B</sub> = 400 pF     |     | 120  |         |
| 11.12.1                    | $t_{fDA}$    | Fall Time of SDA Signal                              | Standard mode, VIO = 1.8V, R <sub>PU</sub> = 10 k $\Omega$ and C <sub>B</sub> = 400 pF |     | 300  | ns      |
| 11.12.2                    |              |  | Fast mode, VIO = 1.8V, R <sub>PU</sub> = 1 k $\Omega$ and C <sub>B</sub> = 400 pF      |     | 6.5  |         |
| 11.12.3                    |              |  | Fast mode+, VIO = 1.8V, R <sub>PU</sub> = 330 $\Omega$ and C <sub>B</sub> = 400 pF     |     | 6.5  |         |
| 11.13.1                    | $t_{rCL}$    | Rise Time of SCL Signal                              | Standard mode, VIO = 1.8V, R <sub>PU</sub> = 10 k $\Omega$ and C <sub>B</sub> = 400 pF |     | 1000 | ns      |
| 11.13.2                    |              |  | Fast mode, VIO = 1.8V, R <sub>PU</sub> = 1 k $\Omega$ and C <sub>B</sub> = 400 pF      |     | 20   |         |
| 11.13.3                    |              |  | Fast mode+, VIO = 1.8V, R <sub>PU</sub> = 330 $\Omega$ and C <sub>B</sub> = 400 pF     |     | 120  |         |

## 6.12 I<sup>2</sup>C Interface (continued)

Over operating free-air temperature range (unless otherwise noted). Device supports standard mode (100 kHz), fast mode (400 kHz), and fast mode+ (1 MHz) when VIO is 3.3V or 1.8V.

| POS     | PARAMETER        | TEST CONDITIONS  | MIN                       | TYP | MAX  | UNIT |
|---------|------------------|--|---------------------------|-----|--|------|
| 11.14.1 | t <sub>FCL</sub> | Fall Time of SCL Signal  |                           |     | 300  | ns   |
| 11.14.2 |                  |  |                           |     | Standard mode, VIO = 1.8V, R <sub>PU</sub> = 10 kΩ and C <sub>B</sub> = 400 pF |      |
| 11.14.3 |                  |  |                           |     | Fast mode, VIO = 1.8V, R <sub>PU</sub> = 1 kΩ and C <sub>B</sub> = 400 pF      |      |
| 11.15.1 | t <sub>SP</sub>  | Pulse Width of Spike suppressed (SCL and SDA Spikes that are less than the indicated Width are suppressed) | Fast mode, and fast mode+ |     | 50   | ns   |

### 6.13 Typical Characteristics

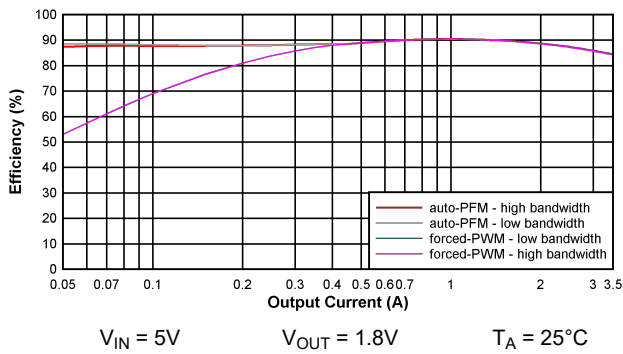


Figure 6-1. Efficiency BUCK1

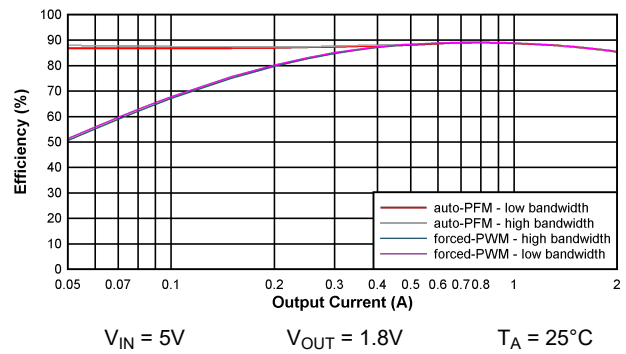


Figure 6-2. Efficiency BUCK23

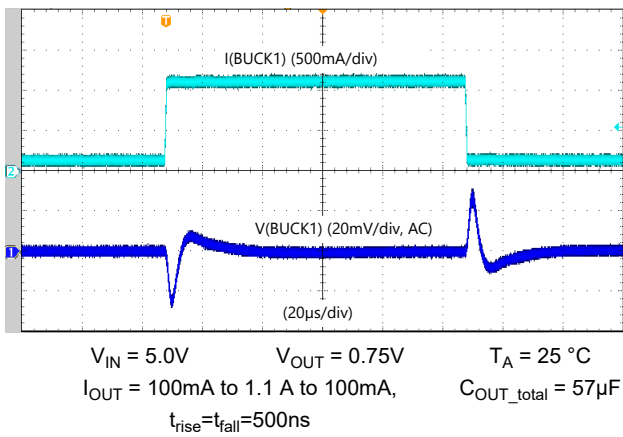


Figure 6-3. BUCK1 Load-step Response - High Bandwidth, Forced PWM

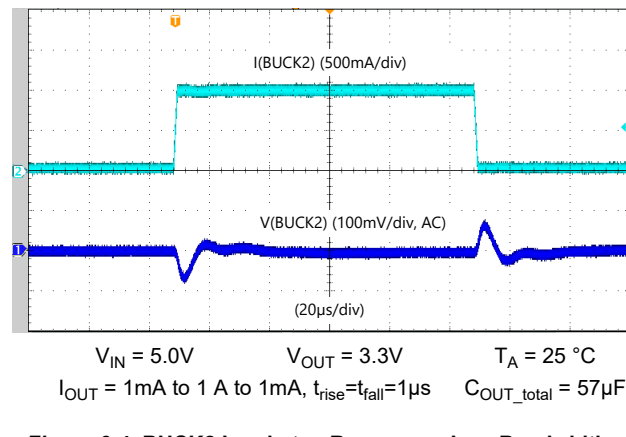


Figure 6-4. BUCK2 Load-step Response - Low Bandwidth, Forced PWM

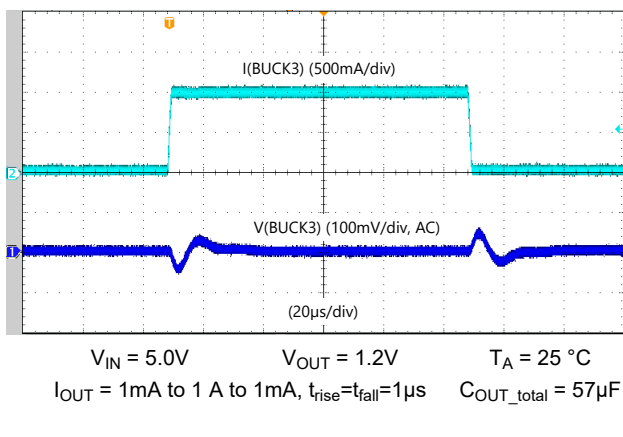


Figure 6-5. BUCK3 Load-step Response - Low Bandwidth, Forced PWM

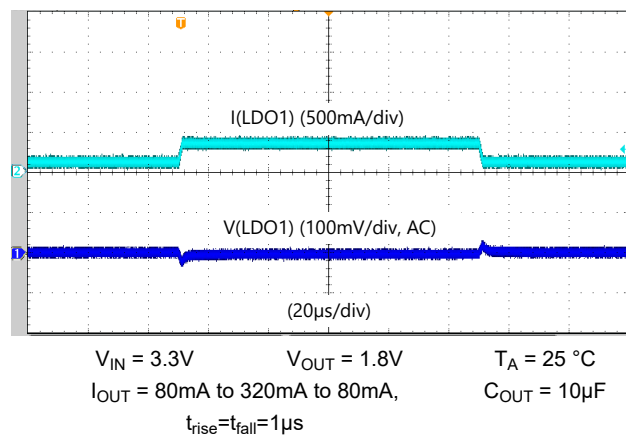
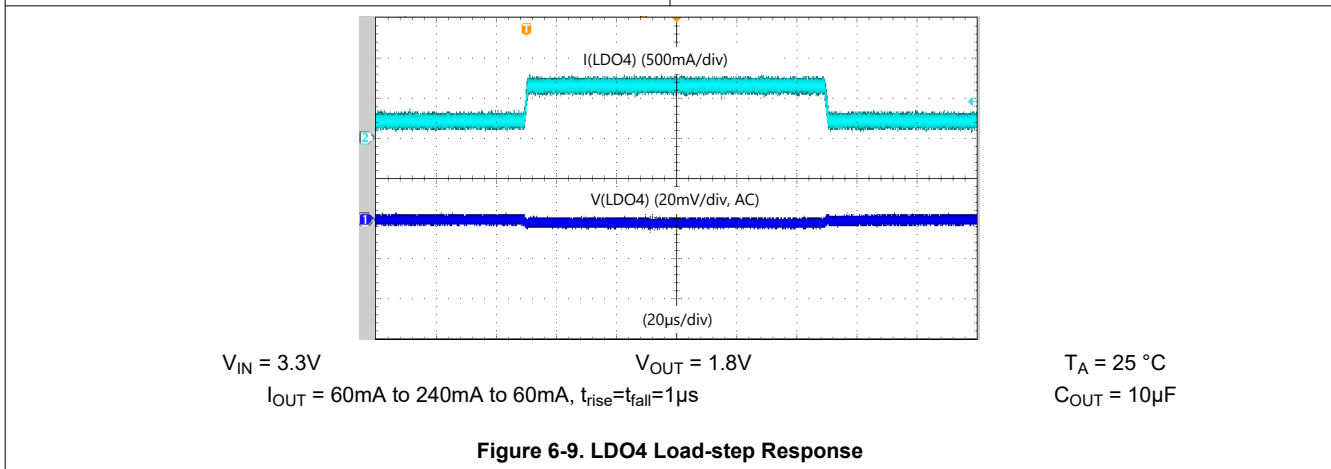
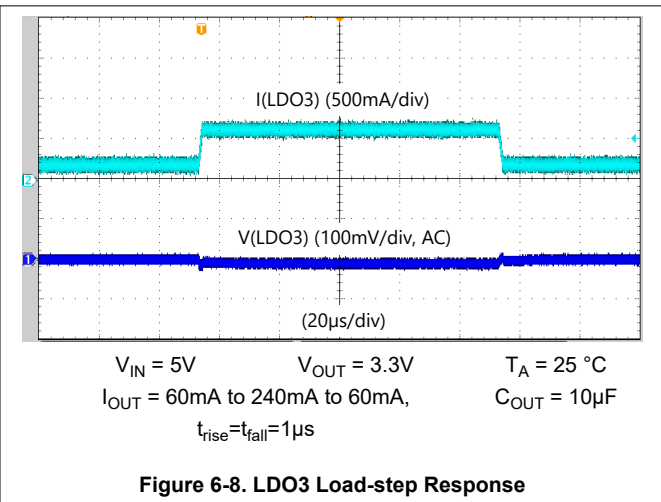
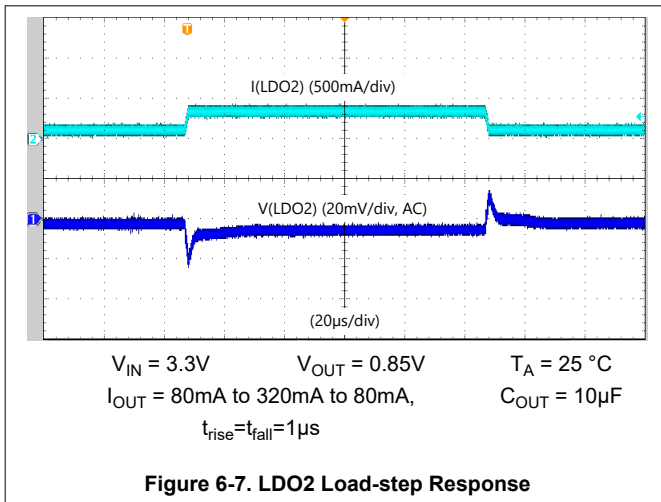


Figure 6-6. LDO1 Load-step Response

### 6.13 Typical Characteristics (continued)



## 7 Detailed Description

### 7.1 Overview

The TPS65219 provides three step-down converters, four LDOs, three general-purpose I/Os and three multi-Function pins. The system is able to be supplied with a single cell Li-Ion battery, two primary cells or a regulated supply. The device is characterized across a -40°C to +105°C temperature range, which makes the PMIC an excellent choice for various industrial applications.

The I2C interface provides comprehensive features for using TPS65219. All rails, the GPOs and the GPIO are configurable as enabled or disabled. Voltage thresholds for the undervoltage monitoring are customizable.

The integrated voltage supervisor monitors Buck 1–3 and LDO1–4 for undervoltage. The monitor has two sensitivity settings. A power good signal is provided to report the successful ramp of the power rails and GPIOs. The nRSTOUT pin is pulled low until the device enters ACTIVE state. When powering down from ACTIVE- or STBY-state, nRSTOUT is pulled low again. The nRSTOUT pin has an open-drain output. A fault-pin, nINT, notifies the SoC about faults.

Buck1 step-down converter supplies up to 3.5A of current, Buck2 and Buck3 supplies up to 2A each. The default output voltages for each converter are adjustable through the I2C interface. All three buck-converters feature dynamic voltage scaling. The step-down converters operate in a low power mode at light load or in a forced into PWM operation for noise sensitive applications.

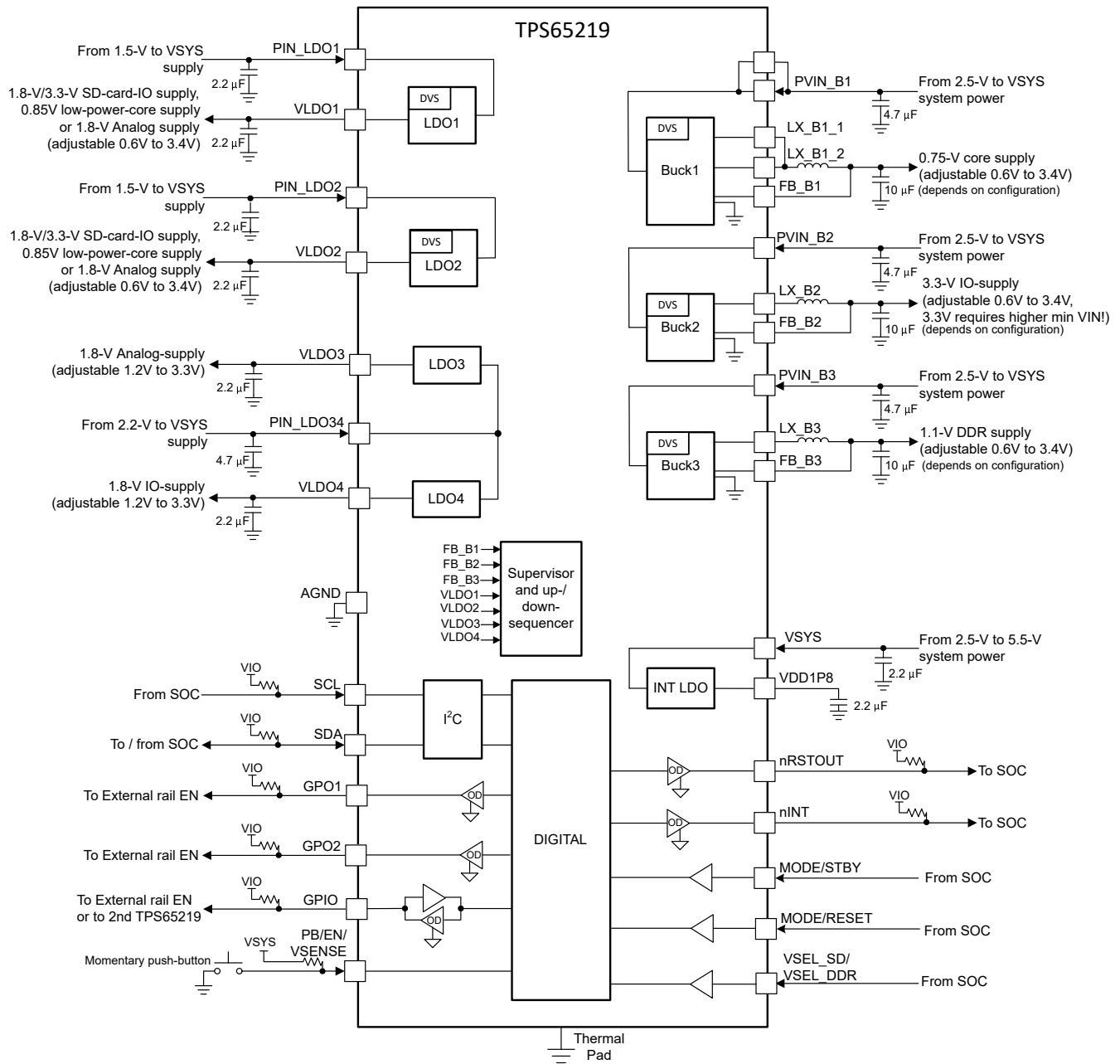
LDO1 and LDO2 support output currents of 400mA at an output voltage range of 0.6V to 3.4V. These LDOs support bypass mode, acting as a load-switch, and allowing voltage-changes during operation for applications like SD-card-supply, adjusting the IO-supply of the SD-card from 3.3V to 1.8V after initialization.

LDO3 and LDO4 support output currents of 300mA at an output voltage range of 1.2V to 3.3V. These LDOs support load-switch-mode, but not bypass mode.

The I2C-interface, IOs, GPIOs, and multi-function-pins (MFP) allow a seamless interface to a wide range of SoCs.

All configurations of the rails, for example output-voltages, sequencing, are backed up by EEPROM. Please refer to the Technical Reference Manual (TRM) of the chosen configuration.

## 7.2 Functional Block Diagram



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Figure 7-1. Functional Block Diagram

### Note

VIO is the external pull-up supply that must be selected within the recommended operating voltage range.

## 7.3 Feature Description

### 7.3.1 Power-Up Sequencing

The TPS65219 allows flexible sequencing of the rails. The order of the rails, including GPO1, GPO2, GPIO for the external rails, and the nRSTOUT pin is defined by the NVM. Prior to starting the power-up sequence, the device checks if the voltage on all rails fell below the SCG-threshold to avoid starting into a pre-biased rail. The sequence is timing based. In addition, the previous rail must have passed the UV-threshold to enable the subsequent rail. If UV is masked, the sequence proceeds even if the UV-threshold is not reached. GPO1, GPO2, GPIO, and LDOs configured in bypass- or LSW-mode are not monitored for undervoltage, thus these outputs do not gate subsequent rails.

In case the sequence is interrupted due to an unmasked fault on a rail, the device powers down. The TPS65219 attempts to power up two more times. If both of those re-tries fail to enter ACTIVE state, the device remains in INITIALIZE state until VSYS is power-cycled. While encouraged to keep this retry-counter active, the retry-counter is maskable by setting bit MASK\_RETRY\_COUNT in INT\_MASK\_UV register.

To disable the retry-counter, set bit MASK\_RETRY\_COUNT in INT\_MASK\_UV register. When set, the device attempts to retry infinitely.

The TPS65219 allows to configure the power-down sequence independent from the power-up sequence. The sequences are configured in the non-volatile memory.

At initial power-up, the device monitors the VSYS supply voltage and allows power-up and transition to INITIALIZE state only if VSYS passed the VSYS<sub>POR\_Rising</sub> threshold.

The power-up sequence is configured as follows:

- The slot (respectively the position in the sequence) for each rail and GPO1, GPO2, GPIO, and nRSTOUT is defined using the corresponding \*\_SEQUENCE\_SLOT registers, the four MSB for the power-up sequence, the four LSB for the power-down sequence.
- The duration of each slot is defined in the POWER\_UP\_SLOT\_DURATION\_x registers and are configurable as 0ms, 1.5ms, 3ms or 10ms. In total, 16 slots are available, allowing the sequence to span over multiple TPS65219-devices if more rails need to be supported.
- In addition to the timing as defined above, the power-up-sequence is also gated by the UV-monitor: a subsequent rail only gets enabled after the previous one passed the undervoltage threshold (unless UV is masked). If a rail has not reached the UV-threshold by the end of t<sub>RAMP</sub> (respectively t<sub>RAMP\_LSW</sub>, t<sub>RAMP\_SLOW</sub>, t<sub>RAMP\_FAST</sub>), the sequence is aborted and the device sequences down at the end of the slot-duration. For the respective rail, the device sets INT\_BUCK\_x\_y\_IS\_SET respectively INT\_LDO\_x\_y\_IS\_SET bit in INT\_SOURCE register and BUCKx\_UV respectively LDOx\_UV bit in INT\_BUCK\_x\_y respectively INT\_LDO\_x\_y register as well as bit TIMEOUT in the INT\_TIMEOUT\_RV\_SD register.
- The initiation of the sequence is gated by the successful discharge of all rails, irrespective if enabled during the sequence or not. If the device is unable to discharge all rails below the SCG-threshold, the device sets INT\_BUCK\_x\_y\_IS\_SET respectively INT\_LDO\_x\_y\_IS\_SET bit in INT\_SOURCE register and BUCKx\_RV respectively LDOx\_RV bit if the residual voltage is still present after 4ms to 5ms and the device remains in INITIALIZE state.
- The initiation of the sequence is gated by the die-temperature: if any one of the WARM detections is unmasked, the device does not power-up until the temperature on all sensors fell below T<sub>WARM\_falling</sub> threshold if INITIALIZE state was entered due to a thermal event, respectively until the temperature on all sensors is below T<sub>WARM\_rising</sub> threshold if INITIALIZE state was entered from OFF-state. If all thermal sensors are masked (WARM detection not causing a power-down), the device does not power-up until the temperature on all sensors is below T<sub>HOT\_falling</sub> threshold

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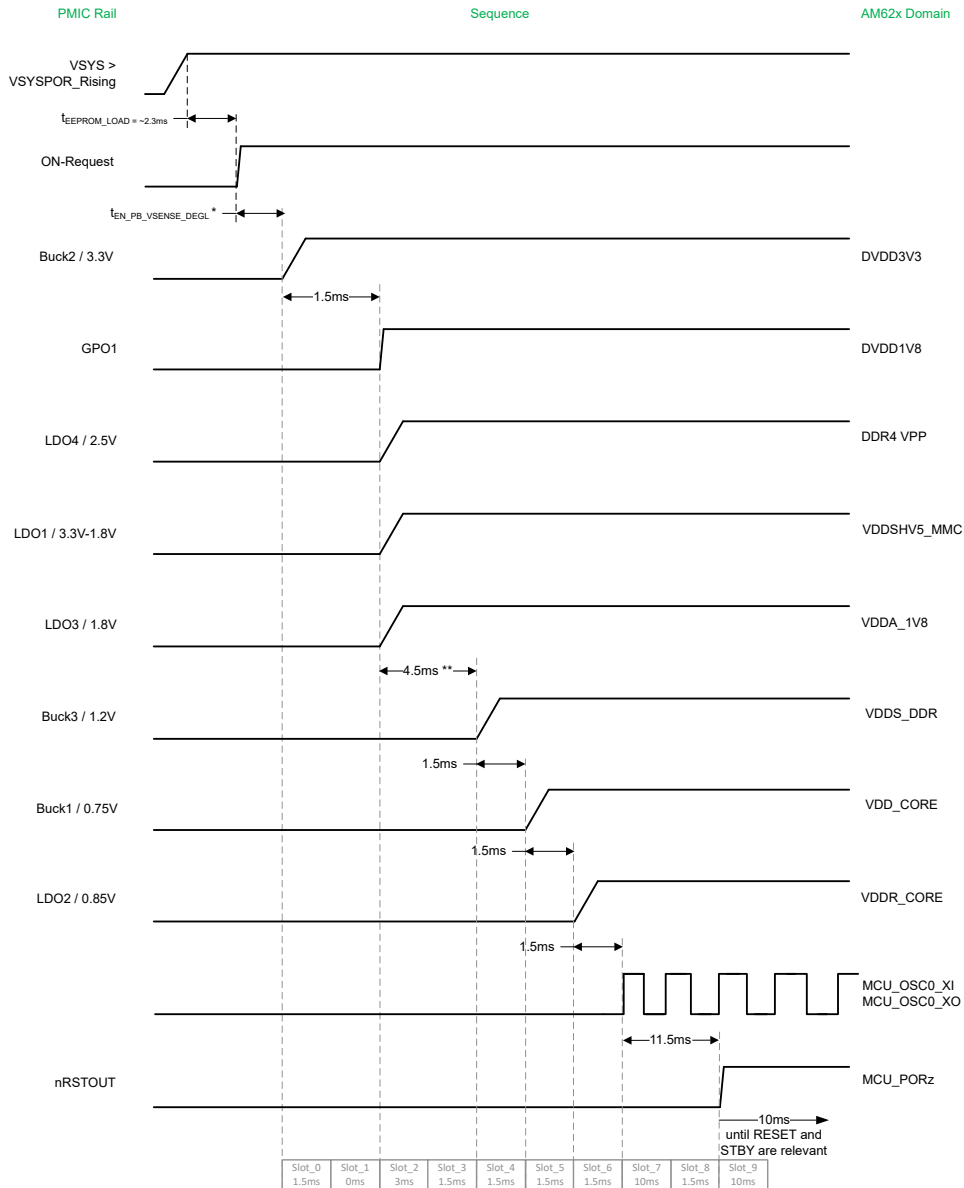
#### Note

All rails get discharged prior to enable (irrespective if discharge-function is disabled).

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An ON-request is deglitched to not trigger on noise. After the deglitch time, the device takes approximately 300µs until the first slot of the sequence starts. In case discharging of pre-biased rails is not completed by that time, the start of the sequence is further gated until all rails have discharged below SCG-voltage level.

Figure 7-2 shows an example of a power up sequence. The power up sequence is triggered through a valid on request.



\* depends on EN / PB / VSENSE and long/short configuration, ~0 if FSD is enabled  
 \*\* if applicable, slot-duration needs to adopt for enable- & ramp-time of external rail

Figure 7-2. Power-up Sequencing (example)

For details on ON-requests please see Push Button and Enable Input (PB/EN/VSENSE).

**CAUTION**  
 I2C commands must only be issued after EEPROM-load completed.

### 7.3.2 Power-Down Sequencing

An OFF-request or a shut-down-fault triggers the power-down sequence. The OFF-request is triggered by a falling edge on EN/PB/VSENSE if configured for EN or VSENSE respectively a long press of the push-button if configured as PB or by an I2C-command to I2C\_OFF\_REQ in MFP\_CTRL register. This bit self-clears.

An I2C-triggered shut-down requires a renewed ON-request on the EN/PB/VSENSE pin. In case of EN- or VSENSE-configuration, a low-going edge followed by a high-going-edge is required on the EN/PB/VSENSE-pin. The falling-edge deglitch time for EN or VSENSE configuration  $t_{DEGL\_EN/VSENSE\_I2C}$  is shorter than the deglitch-time for pin-induced OFF-requests ( $t_{DEGL\_EN\_Fall}$  and  $t_{DEGL\_VSENSE\_Fall}$ ). The deglitch-times for PB-configuration remain.

In many cases, the power-down sequence follows the reverse power-up sequence. In some applications, all rails are required to shut down at the same time with no delay between rails or require wait-times to allow discharging of rail.

The power-down sequence is configured as follows:

- The slot (respectively the position in the sequence) for each rail and GPO1, GPO2, GPIO, and nRSTOUT is defined using the corresponding \*\_SEQUENCE\_SLOT registers, the four MSB for the ON-sequence, the four LSB for the down-sequencing.
- The duration of each slot is defined in the POWER\_DOWN\_SLOT\_DURATION\_x registers and are configurable as 0 ms, 1.5ms, 3ms or 10ms. In total, 16 slots are available, allowing the sequence to span over multiple TPS65219-devices if more rails need to be supported.
- In addition to the slot-duration, the power-down sequence is also gated by the previous rail being discharged below the SCG-threshold, unless active discharge is disabled on the previous rail. If that does not occur, the power-down of subsequent rails is paused. To allow for power-down in case of biased or shorted rails, the sequence continues despite an incomplete discharge of the previous rail after eight times the slot-duration (or 12ms in case of slot-duration of 0ms).
- To bypass the discharge-check, set the bit BYPASS\_RAILS\_DISCHARGED\_CHECK in register GENERAL\_CONFIG to '1'.

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#### Note

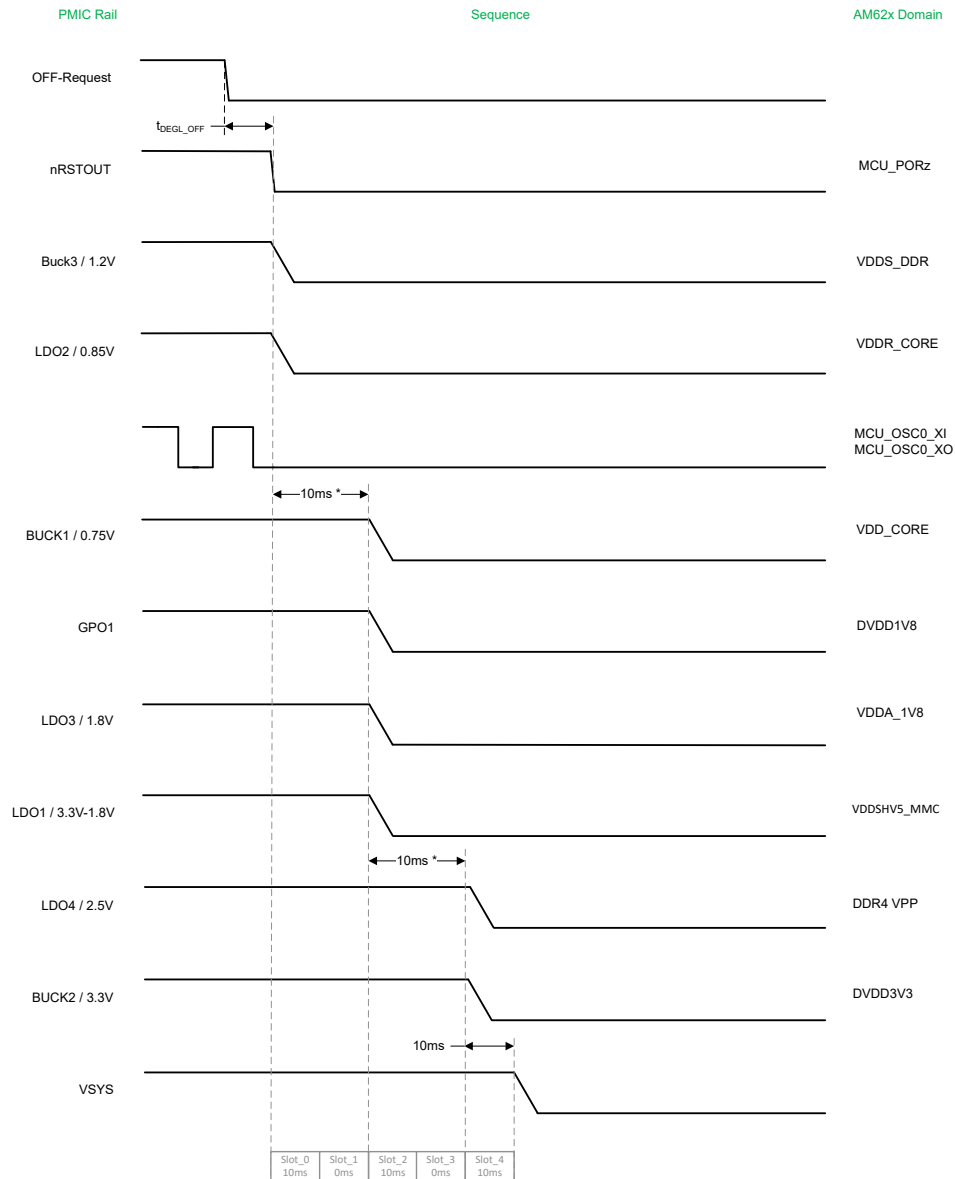
In case active discharge on a rail is disabled, unsuccessful discharge of the rail within the slot duration does not gate the disable of the subsequent rail, but the sequence is purely timing based. In case of residual voltage, the RV-bit is be set regardless.

---

Active discharge is enabled by default and not NVM based. Thus, if desired, discharge need to be disabled after each VSYS-power-cycle. During RESET or OFF-request, the discharge configuration is not reset, as long as VSYS is present. However, in INITIALIZE state and prior to the power-up-sequence, all rails get discharged, regardless of the setting.

During the power-down-sequence, non-EEPROM-backed bits get reset, with the exception of unmasked interrupt bits and \*\_DISCHARGE\_EN bits.

Below graphic shows the power-down-sequence for NVM-ID 0x01, revision 0x2 as an example:



\* discharge-duration depends on Vout, Cout and load. Slot-duration needs to adopt. Slot-duration extends up to 8x its configured value.

**Figure 7-3. Power-down Sequencing (example)**

**CAUTION**

Do not change the registers related to an ongoing sequence by I2C-command!

Non-NVM-bits are not accessible for approximately 80µs after starting a transition into INITIALIZE state.

**7.3.3 Push Button and Enable Input (EN/PB/VSENSE)**

The EN/PB/VSENSE pin is used to enable the PMIC. The pin is configurable to three different functions:

- Device enable (EN):
  - This pin needs to be pulled high to enable the device. Pulling this pin low disables the device.
  - The deglitch-time of the EN-pin is configured by EN\_PB\_VSENSE\_DEGL in MFP\_2\_CONFIG register.

- The power-up sequence starts if the EN input is above the  $V_{IL}$ -threshold low for the configured  $t_{DEGL\_EN\_Rise}$ .
- To signify the power-up based on an EN/PB/VSENSE pin-event, the device sets bit POWER\_UP\_FROM\_EN\_PB\_VSENSE in POWER\_UP\_STATUS\_REG register. This bit does not assert the nINT pin. Write W1C to clear the bit.
- The power-down sequence starts if the EN input is below the  $V_{IH}$ -threshold for  $t_{DEGL\_EN\_Fall}$ .
- In case of a shut-down fault, no renewed on-request is required. The device automatically executes the power-up sequence if EN input is still above the  $V_{IH}$ -threshold. (EN considered level-sensitive)
- In case of a cold reset (regardless if by RESET-pin or I2C-request), no renewed on-request is required. The device automatically executes the power-up sequence if EN input is still above the  $V_{IH}$ -threshold. (EN considered level-sensitive)
- Push-Button (PB):
  - The PB pin is a CMOS-type input used to power-up the PMIC. Typically, the PB pin is connected to a momentary switch to ground and an external pullup resistor.
  - The hold-time of the push-button is configured by EN\_PB\_VSENSE\_DEGL in MFP\_2\_CONFIG register.
  - The power-up sequence starts if the PB input is below the  $V_{IL}$ -threshold low for the configured  $t_{PB\_ON}$ .
  - To signify the power-up based on an EN/PB/VSENSE pin-event, the device sets bit POWER\_UP\_FROM\_EN\_PB\_VSENSE in POWER\_UP\_STATUS\_REG register. This bit does not assert the nINT pin. Write W1C to clear the bit.
  - The PB pin has a rising-edge deglitch  $t_{PB\_RISE\_DEGL}$  to filter bouncing of the switch
  - The power-down sequence starts if the PB input is held low for  $t_{PB\_OFF}$ -time (not configurable).
  - In case of a shut-down fault, no renewed on-request is required. The device automatically executes the power-up sequence without a PB-press.
  - In case of a cold reset (regardless if by RESET-pin or I2C-request), no renewed on-request is required. The device automatically executes the power-up sequence without a PB-press.
  - A push-button press is only recognized after VSYS is above VSYS\_POR-threshold or the PB must be held long enough after VSYS is above VSYS\_POR-threshold.
  - Following bits in the signify the PB-press events:
    - PB\_FALLING\_EDGE\_DETECTED: PB was pressed for a time-interval longer than  $t_{PB\_INT\_DEGL}$  since the previous time this bit was cleared. This bit when set, does assert nINT pin (if config bit MASK\_INT\_FOR\_PB='0'). Write W1C to clear.
    - PB\_RISING\_EDGE\_DETECTED: PB was released for a time-interval longer than  $t_{PB\_INT\_DEGL}$  since the previous time this bit was cleared. This bit when set, does assert nINT pin (if config bit MASK\_INT\_FOR\_PB='0'). Write W1C to clear.
    - PB\_REAL\_TIME\_STATUS: Deglitched ( $t_{PB\_INT\_DEGL}$ ) real-time status of PB pin. Valid only when EN/PB/VSENSE pin is configured as PB. This bit does not assert the nINT pin.
- Power-fail comparator input (VSENSE):
  - Connected to a resistor divider from the supply-line of the pre-regulator, use this pin as a precision enable that senses the supply-voltage to the pre-regulator.
  - The deglitch-time of the VSENSE-pin is configurable by EN\_PB\_VSENSE\_DEGL in MFP\_2\_CONFIG register.
  - Power-up is gated by VSYS being above the  $VSYS_{POR\_Rising}$ -threshold and the VSENSE input is above the  $V_{VSENSE}$ -threshold (not deglitched)
  - The power-up sequence starts if the VSENSE input rises above  $V_{VSENSE}$ .
  - To signify the power-up based on an EN/PB/VSENSE pin-event, the device sets bit POWER\_UP\_FROM\_EN\_PB\_VSENSE in POWER\_UP\_STATUS\_REG register. This bit does not assert the nINT pin. Write W1C to clear the bit.
  - The power-down sequence starts if the VSENSE input falls below the  $V_{VSENSE}$ -threshold for  $t_{DEGL\_VSENSE\_Fall}$ , to avoid an un-sequenced power-off due to the loss of VSYS-supply-voltage.
  - In case of a shut-down fault, no renewed on-request is required. The device automatically executes the power-up sequence if VSENSE input is still above the  $V_{VSENSE}$ -threshold.
  - In case of a cold reset (regardless if by RESET-pin or I2C-request), no renewed on-request is required. The device automatically executes the power-up sequence if VSENSE input is still above the  $V_{VSENSE}$ -threshold.

- OFF-request by I2C-command
  - An I2C-command to I2C\_OFF\_REQ in MFP\_CTRL register triggers an OFF-request.
  - After an OFF-request, a new ON-request is required:
    - In case of EN-configuration, the EN input requires a rising edge (EN considered edge-sensitive)
    - In case of PB-configuration, the PB needs to be pressed for a valid ON-request
    - In case of VSENSE-configuration, the VSENSE input requires a rising edge (VSENSE considered edge-sensitive). Trigger a valid ON-request by power cycling the pre-regulator.
    - The falling-edge deglitch time for EN or VSENSE configuration  $t_{DEGL\_EN/VSENSE\_I2C}$  is shorter than the deglitch-time for pin-induced OFF-requests ( $t_{DEGL\_EN\_Fall}$  and  $t_{DEGL\_VSENSE\_Fall}$ ). The deglitch-times for PB-configuration remain.
- First Supply detection (FSD)
  - First Supply detection (FSD) allows power-up as soon as supply voltage is applied, even if EN/PB/VSENSE pin is at OFF\_REQ status.
  - Use FSD in combination with any ON-request configuration, EN, PB or VSENSE.
  - Enable FSD by setting PU\_ON\_FSD bit in MFP\_2\_CONFIG.
  - At first power-up the EN/PB/VSENSE pin is treated as if the pin had a valid ON request.
  - Once VSYS is above the  $VSYS_{POR\_Rising}$ -threshold, the PMIC
    - loads the EEPROM
    - enters INITIALIZE state
    - perform the discharge-check
    - initiates the power-up-sequence, regardless of the EN/PB/VSENSE-pin-state.
  - To signify the power-up based on FSD, the device sets bit POWER\_UP\_FROM\_FSD in POWER\_UP\_STATUS\_REG register. The nINT-pin does not toggle based on this bit. Write W1C to clear the bit.
  - Thereafter, the EN/PB/VSENSE-pin is treated as if the pin had a valid ON-request, until we enter ACTIVE state (at the expiration of the last slot in the power-up-sequence).
  - After that the device adheres to post-deglitch EN/PB/VSENSE-pin-status: if pin status has changed prior to entering ACTIVE state or in ACTIVE state, the device does adhere to the pin state. For example, if the EN/PB/VSENSE-pin is configured for EN, the device does power down in case the EN-pin is low (for longer than the deglitch time) at the time the device enters ACTIVE state.
  - The duration for how long the ON-request is considered valid, regardless of the pin-state, is controlled by the length of the nRSTOUT slot (and any empty slots thereafter), as the PMIC enters ACTIVE state only after the last slot of the sequence expired.

### 7.3.4 Reset to SoC (nRSTOUT)

The reset output (nRSTOUT) is an open-drain output, intended to release the reset to the SoC or FPGA at the end of the power-up sequence. The timing for nRSTOUT is configured in the sequence. nRSTOUT is driven low until the device enters ACTIVE state or when powering-down from ACTIVE- or STBY-state. The pin is driven high during ACTIVE- and STBY-state.

### 7.3.5 Buck Converters (Buck1, Buck2, and Buck3)

The TPS65219 integrates three buck converters. Buck1 is capable of supporting up to 3.5 A and Buck2/Buck3 are capable of supporting up to 2A of load current. The buck converters have an input voltage range from 2.5V to 5.5V. Connect the input voltage of the buck converters either directly to the system power or to the output of another buck converter. The output voltage is programmable in the range of 0.6V to 3.4V: in 25mV-steps up to 1.4V, in 100mV-steps between 1.4V and 3.4V.

- The ON/OFF state of the buck converters in ACTIVE state is controlled by the corresponding BUCKx\_EN bit in the ENABLE\_CTRL register.
- The ON/OFF state of the buck converters in STBY state is controlled by the corresponding BUCKx\_STBY\_EN bit in the STBY\_1\_CONFIG register.
- In INITIALIZE state, the buck converters are off, regardless of bit-settings.

**CAUTION**

In case of buck-regulators that are not to be used at all, the FB\_Bx pin must be tied to GND and the LX\_Bx pin must be left floating.

- Control the converters' activity with the sequencer or through I2C communication.

**Buck-switch-modes:**

- **Quasi-fixed Frequency Mode**

- The converters are operable in forced-PWM mode, irrespective of load-current, or in pulse-frequency-modulation (PFM) mode for low load-currents. The mode is controlled by either the MODE/STBY pin or the MODE/RESET pin if either of those is configured as 'MODE', or by an I2C-command to MODE\_I2C\_CTRL bit in MFP\_1\_CONFIG register (see pin-configuration and I2C-command in 'PWM/PFM and Low Power Modes (MODE/STBY)' and PWM/PFM and Reset (MODE/RESET)' section.
- During a transition to ACTIVE state or to INITIALIZE state, the buck converters are forced to PWM, irrespective of the pin-state. PFM-entry is only allowed when the device enters ACTIVE state, upon completion of the sequence and expiration of the last power-up-slot.
- In case of a DVFS-induced output voltage change, the TPS65219 temporarily forces the buck-regulators into PWM until the voltage change completed. If PFM is allowed, the entry and exit into PFM is load-current dependent. PFM starts when the inductor current reaches 0A, which is the case at a load current approximately calculated by:
- $I_{LOAD} = \{[(V_{PVIN\_Bx} - V_{BUCKx}) / L] \times (V_{BUCKx} / V_{PVIN\_Bx}) \times (1 / f_{SW})\} / 2$

**CAUTION**

The user **MUST NOT CHANGE** the BUCK\_FF\_ENABLE! The bit is pre-configured by the manufacturer.

- The converters are individually configurable for a high-bandwidth-mode for optimum transient-response or lower bandwidth, allowing minimum output filter capacitance. The selection is done by the BUCKx\_BW\_SEL bits in GENERAL\_CONFIG register. This bit must only change if this regulator is disabled. Please note the higher output-capacitance requirements for high bandwidth use case!
- If VSEL\_SD/VSEL\_DRR is configured as 'VSEL\_DDR' by the VSEL\_DDR\_SD bit in MFP\_1\_CONFIG register, configure the output voltage of Buck3 by pulling the VSEL\_SD/VSEL\_DDR pin high, low or leaving the pin floating. These settings supports DDR3LV, DDR4, and DDR4LV supply voltages without an EEPROM change.

**CAUTION**

The VSEL\_DDR-pin needs to be hard-wired and must not change during operation.

- The buck converters have an active discharge function. The discharge function for each rail is configurable as enabled or disabled in the DISCHARGE\_CONFIG register. If discharge is enabled, the device discharges the output is discharged to ground whenever a rail is disabled.
- Prior to a sequence into ACTIVE state (from INITIALIZE or STBY state), the device discharges the disabled rails regardless of the discharge-configuration to avoid starting into a pre-biased output.
- If a rail is enabled by an I2C-command, active discharge is not enforced, but the rail is only enabled if the output voltage is below the SCG-threshold.
- This register is not EEPROM-backed and does reset if the device enters OFF-state.
- When in INITIALIZE state (during RESET or an I2C-OFF-request), the discharge configuration is not reset.  
Note: when disabling the discharge function, consider the possibility of the TIMEOUT fault during the power-down-sequence.

All Buck Converters support Dynamic Voltage Frequency Scaling (DVFS). This allows dynamically changing the output-voltage during the operation to optimize the operating voltage for the operation point of the SoC in the lower output voltage range between 0.6V and 1.4V. The voltage change is controlled by writing

to BUCK1\_VOUT respectively BUCK2\_VOUT or BUCK3\_VOUT registers. During a DVFS-induced voltage transition, the active discharge function is temporarily enabled, irrespective of the discharge-configuration.

### Output Capacitance Requirements

The buck converters require sufficient output-capacitance for stability. The required minimum and supported maximum capacitance depends on the configuration:

- for quasi-fixed-frequency, low-bandwidth configuration, a minimum capacitance of 10uF is required and a maximum total capacitance of 75uF is supported
- for quasi-fixed-frequency, high-bandwidth configuration, a minimum capacitance of 30uF is required and a maximum total capacitance of 220uF is supported

### Buck Fault Handling

- The TPS65219 detects undervoltages on the buck converter outputs. The reaction to the detection of an undervoltage is dependent on the configuration of the respective BUCKx\_UV bit and the MASK\_EFFECT bit in INT\_MASK\_BUCKS. If not masked, the device sets bit INT\_BUCK\_1\_2\_IS\_SET respectively INT\_BUCK\_3\_IS\_SET bit in INT\_SOURCE register and bit BUCKx\_UV in INT\_BUCK\_1\_2 respectively INT\_BUCK\_3 register.

During a voltage transition (for example, when triggered by a DVFS induced voltage change), the device blanks the undervoltage detection by default and activates the undervoltage detection when the voltage transition completed.

If the device detects an undervoltage during the sequence into ACTIVE state (from INITIALIZE or STBY) and UV is not masked, the power-down-sequence starts at the end of the current slot.

If the device detects an undervoltage in ACTIVE-state or STBY-state and UV is not masked, the power-down sequence starts immediately. OC-detection is not maskable.

- The TPS65219 provides cycle-by-cycle current-limit on the buck converter outputs. If the device detects over-current for  $t_{\text{DEGLITCH\_OC\_short}}$ , respectively for  $t_{\text{DEGLITCH\_OC\_long}}$  (configurable individually per rail with EN\_LONG\_DEGL\_FOR\_OC\_BUCKx in OC\_DEGL\_CONFIG register; applicable for rising-edge only), the device sets INT\_BUCK\_1\_2\_IS\_SET respectively INT\_BUCK\_3\_IS\_SET bit in INT\_SOURCE register and bit BUCKx\_OC (for positive over-current) respectively BUCKx\_NEG\_OC (for negative over-current) in INT\_BUCK\_1\_2 respectively INT\_BUCK\_3 register.

During a voltage transition (for example, when triggered by a DVFS induced voltage change), the over current detection is blanked and only gets activated when the voltage transition is completed.

If the over-current occurs during the sequence into ACTIVE state (from INITIALIZE or STBY), the device disables the affected rail immediately and starts the power-down-sequence at the end of the current slot.

If the over-current occurs in ACTIVE-state or STBY-state, the device disables the affected rail immediately and starts the power-down sequence.

OC-detection is not maskable, but the deglitch-time is configurable. TI strongly recommends to use  $t_{\text{DEGLITCH\_OC\_short}}$ . Extended over-current leads to increased aging or overshoot upon recovery.

- The TPS65219 detects short-to-ground (SCG) faults on the buck-outputs. The reaction to the detection of an SCG event is to set INT\_BUCK\_1\_2\_IS\_SET respectively INT\_BUCK\_3\_IS\_SET bit in INT\_SOURCE register and bit BUCKx\_SCG in INT\_BUCK\_1\_2 respectively INT\_BUCK\_3 register. The affected rail is disabled immediately. The device sequences down all outputs and transitions into the INITIALIZE state.

SCG-detection is not maskable.

If a rail gets enabled, the device blanks SCG detection initially to allow the rail to ramp above the SCG-threshold.

- The TPS65219 detects residual voltage (RV) faults on the buck-outputs. The reaction to the detection of an RV event is to set INT\_RV\_IS\_SET bit in INT\_SOURCE register and bit BUCKx\_RV in INT\_RV register. The RV-detection is not maskable, but the nINT-reaction is globally configurable for all rails by

MASK\_INT\_FOR\_RV in INT\_MASK\_WARM register. The BUCKx\_RV-flag is set regardless of masking, INT\_RV\_IS\_SET bit is only set if nINT is asserted. The fault-reaction time and potential state-transition depends on the situation when residual voltage is detected:

- If the device detects residual voltage during an ON-request in the INITIALIZE state, the device gates power-up and the device remains in INITIALIZE state. If the RV-condition exists for more than 4ms to 5ms, the device sets BUCKx\_RV-bit. If the RV-condition is not present any more, the device transitions to ACTIVE state.
- If the device detects residual voltage during power-up, ACTIVE\_TO\_STANDBY, or STANDBY\_TO\_ACTIVE sequences, the sequence is aborted and the device powers down.
- If the device detects residual voltage for more than 80ms on any rail that was disabled during STBY state during a request to leave STBY state, the device transitions into INITIALIZE state. The device sets the BUCKx\_RV-bit if the condition persists for 4ms to 5ms, but less than 80ms.
- If the device detects residual voltage during power-up, ACTIVE\_TO\_STANDBY, or STANDBY\_TO\_ACTIVE sequences, the sequence is aborted and the device powers down.
- If residual voltage is detected during an EN-command of the rail by I2C, the BUCKx\_RV-flag is set immediately, but no state transition occurs.
- The buck converters have a local over-temperature sensor. The reaction to a temperature warning is dependent on the configuration of the respective SENSOR\_x\_WARM\_MASK bit in MASK\_CONFIG register and the MASK\_EFFECT bits in INT\_MASK\_BUCKS register. If the temperature at the sensor exceeds  $T_{WARM\_Rising}$  and is not masked, the device sets INT\_SYSTEM\_IS\_SET bit in INT\_SOURCE register and SENSOR\_x\_WARM bit in INT\_SYSTEM register. In case the sensor detects a temperature exceeding  $T_{HOT\_Rising}$ , the converters power dissipation and junction temperature exceeds safe operating value. The device powers down all active outputs immediately and sets INT\_SYSTEM\_IS\_SET bit in INT\_SOURCE register and SENSOR\_x\_HOT bit in INT\_SYSTEM register. The TPS65219 automatically recovers once the temperature drops below the  $T_{WARM\_Falling}$  threshold value (or below the  $T_{HOT\_Falling}$  threshold value in case  $T_{WARM}$  is masked). The \_HOT bit remains set and needs to be cleared by writing '1'. The HOT-detection is not maskable.

**CAUTION**

The buck only supplies output currents up to the respective current limit, including during start-up. Depending on the charge-current into the filter- and load-capacitance, the device is potentially unable to drive the full output current to the load while ramping. For a total load-capacitance exceeding 50µF, the load current must not exceed approximately 25% of the rated output current. This limit applies also for dynamic output-voltage changes.

**CAUTION**

The TPS65219 does not offer differential feedback pins. The device does not support remote sensing. To minimize noise in the single-ended sense trace, minimize the trace length from the respective FB pin to the direct connection at the output filter.

**Table 7-1. BUCK Output Voltage Settings**

| BUCKx_VSET [decimal] | BUCKx_VSET [binary] | BUCKx_VSET [hexadecimal] | VOUT (Buck1 & Buck2 and Buck3) [V] |
|----------------------|---------------------|--------------------------|------------------------------------|
| 0                    | 000000              | 00                       | 0.600                              |
| 1                    | 000001              | 01                       | 0.625                              |
| 2                    | 000010              | 02                       | 0.650                              |
| 3                    | 000011              | 03                       | 0.675                              |
| 4                    | 000100              | 04                       | 0.700                              |
| 5                    | 000101              | 05                       | 0.725                              |
| 6                    | 000110              | 06                       | 0.750                              |
| 7                    | 000111              | 07                       | 0.775                              |
| 8                    | 001000              | 08                       | 0.800                              |

**Table 7-1. BUCK Output Voltage Settings (continued)**

| BUCKx_VSET [decimal] | BUCKx_VSET [binary] | BUCKx_VSET [hexadecimal] | VOUT (Buck1 & Buck2 and Buck3) [V] |
|----------------------|---------------------|--------------------------|------------------------------------|
| 9                    | 001001              | 09                       | 0.825                              |
| 10                   | 001010              | 0A                       | 0.850                              |
| 11                   | 001011              | 0B                       | 0.875                              |
| 12                   | 001100              | 0C                       | 0.900                              |
| 13                   | 001101              | 0D                       | 0.925                              |
| 14                   | 001110              | 0E                       | 0.950                              |
| 15                   | 001111              | 0F                       | 0.975                              |
| 16                   | 010000              | 10                       | 1.000                              |
| 17                   | 010001              | 11                       | 1.025                              |
| 18                   | 010010              | 12                       | 1.050                              |
| 19                   | 010011              | 13                       | 1.075                              |
| 20                   | 010100              | 14                       | 1.100                              |
| 21                   | 010101              | 15                       | 1.125                              |
| 22                   | 010110              | 16                       | 1.150                              |
| 23                   | 010111              | 17                       | 1.175                              |
| 24                   | 011000              | 18                       | 1.200                              |
| 25                   | 011001              | 19                       | 1.225                              |
| 26                   | 011010              | 1A                       | 1.250                              |
| 27                   | 011011              | 1B                       | 1.275                              |
| 28                   | 011100              | 1C                       | 1.300                              |
| 29                   | 011101              | 1D                       | 1.325                              |
| 30                   | 011110              | 1E                       | 1.350                              |
| 31                   | 011111              | 1F                       | 1.375                              |
| 32                   | 100000              | 20                       | 1.400                              |
| 33                   | 100001              | 21                       | 1.500                              |
| 34                   | 100010              | 22                       | 1.600                              |
| 35                   | 100011              | 23                       | 1.700                              |
| 36                   | 100100              | 24                       | 1.800                              |
| 37                   | 100101              | 25                       | 1.900                              |
| 38                   | 100110              | 26                       | 2.000                              |
| 39                   | 100111              | 27                       | 2.100                              |
| 40                   | 101000              | 28                       | 2.200                              |
| 41                   | 101001              | 29                       | 2.300                              |
| 42                   | 101010              | 2A                       | 2.400                              |
| 43                   | 101011              | 2B                       | 2.500                              |
| 44                   | 101100              | 2C                       | 2.600                              |
| 45                   | 101101              | 2D                       | 2.700                              |
| 46                   | 101110              | 2E                       | 2.800                              |
| 47                   | 101111              | 2F                       | 2.900                              |
| 48                   | 110000              | 30                       | 3.000                              |
| 49                   | 110001              | 31                       | 3.100                              |
| 50                   | 110010              | 32                       | 3.200                              |
| 51                   | 110011              | 33                       | 3.300                              |
| 52                   | 110100              | 34                       | 3.400                              |

**Table 7-1. BUCK Output Voltage Settings (continued)**

| BUCKx_VSET [decimal] | BUCKx_VSET [binary] | BUCKx_VSET [hexadecimal] | VOUT (Buck1 & Buck2 and Buck3) [V] |
|----------------------|---------------------|--------------------------|------------------------------------|
| 53                   | 110101              | 35                       | 3.400                              |
| 54                   | 110110              | 36                       | 3.400                              |
| 55                   | 110111              | 37                       | 3.400                              |
| 56                   | 111000              | 38                       | 3.400                              |
| 57                   | 111001              | 39                       | 3.400                              |
| 58                   | 111010              | 3A                       | 3.400                              |
| 59                   | 111011              | 3B                       | 3.400                              |
| 60                   | 111100              | 3C                       | 3.400                              |
| 61                   | 111101              | 3D                       | 3.400                              |
| 62                   | 111110              | 3E                       | 3.400                              |
| 63                   | 111111              | 3F                       | 3.400                              |

### 7.3.6 Linear Regulators (LDO1 through LDO4)

The TPS65219 offers a total of four linear regulators, where LDO1 and LDO2 share their properties and LDO3 and LDO4 share theirs.

#### LDO1 and LDO2: 400mA, 0.6V - 3.4V

Both, LDO1 and LDO2 are general-purpose LDOs intended to provide power to analog circuitry on the SOC or peripherals. The LDOs have an input voltage range from 1.5V to 5.5V, and can be connected either directly to the system power or the output of a Buck converter. The output voltage is programmable in the range of 0.6V to 3.4V in 50mV-steps. Both LDOs support up to 400mA. The LDOs can be configured in by-pass-mode, acting as load-switches. If configured in bypass-mode, the desired output voltage still needs to be specified in LDOx\_VOUT register. The LDOs also support output-voltage changes while enabled, supporting functions like SD-card-IO-supply, changing from 3.3V to 1.8V after initialization, either in LDO-mode at a supply-voltage above 3.3V or with a 3.3V supply changing between bypass-mode and LDO-mode. The LDOs also support Load-switch mode (LSW\_mode): in this case, output voltages of 1.5V up to 5.5V are supported. The desired voltage does not need to be configured in the LDOx\_VOUT register.

- In case of SD-card-supply, one of the LDOs can be controlled by the VSEL\_SD/VSEL\_DDR, configured as VSEL\_SD. Which LDO is controlled is selected by VSEL\_RAIL bit in MFP\_1\_CONFIG register. The polarity of the pin can be configured via VSEL\_SD\_POLARITY bit in MFP\_1\_CONFIG register.

Alternatively, an I2C communication to VSEL\_SD\_I2C\_CTRL in MFP\_1\_CONFIG register controls the change of the output voltage. Therefore, even if VSEL\_SD/VSEL\_DDR pin is configured as VSEL\_DDR, the VSEL\_RAIL bit still needs to be configured to define which LDO is affected by the I2C-command.

- The LDOs can be configured as linear regulators or operate in bypass-mode or be configured as a load-switch (LSW-mode). The mode is configured by LDOx\_LSW\_CONFIG and LSW\_BYP\_CONFIG bits in LDOx\_VOUT register.

#### **CAUTION**

If an LDO is configured in bypass-mode, the output voltage must be configured and the PVIN\_LDOx supply voltage must match the configured output voltage. PVIN\_LDOx voltage must be within (configured VOUT) and (configured VOUT + 200mV). Violation of this can result in instability.

In bypass- or LSW-mode, the LDO acts as a switch, where VOUT is VIN minus the drop over the FET-resistance ( $R_{BYPASS}$ ,  $R_{LSW}$ ).

### Output Capacitance Requirements

The LDO regulators require sufficient output-capacitance for stability. The required minimum and supported maximum capacitance depends on the configuration:

- in LDO-mode, a minimum capacitance of 1.6uF is required and a maximum total load capacitance (output filter and point-of-load combined) of 20uF is supported
- in LSW- or bypass-mode, a minimum capacitance of 1.6uF is required and a maximum total capacitance (output filter and point-of-load combined) of 50uF is supported

### LDO3 and LDO4: 300mA, 1.2V - 3.3V

Both, LDO3 and LDO4 are general-purpose LDOs intended to provide power to analog circuitry on the SoC or peripherals. The LDOs have an input voltage range from 2.2V to 5.5V, and can be connected either directly to the system power or the output of a Buck converter. Note, these LDOs need a headroom between VSYS and the LDO-output voltage of minimum 150mV. The output voltage is programmable in the range of 1.2V to 3.3V in 50mV steps. Both LDOs support up to 300mA. The LDOs can be configured to act as load-switches. In this case, output voltages of 2.2V up to 5.5V are supported. The desired voltage does not need to be configured in the LDOx\_VOUT register.

These LDOs support a fast-ramp-mode with limited output capacitance and a slow-ramp-mode, allowing for larger total load capacitance.

### Output Capacitance Requirements

The LDO regulators require sufficient output-capacitance for stability. The required minimum and supported maximum capacitance depends on the configuration:

- for slow-ramp LDO-mode or LSW-mode, a minimum capacitance of 1.6uF is required and a maximum total capacitance (output filter and point-of-load combined) of 30uF is supported
- for fast-ramp LDO-mode or LSW-mode, a minimum capacitance of 1.6uF is required and a maximum total capacitance (output filter and point-of-load combined) of 15uF is supported

### LDO1, LDO2, LDO3 and LDO4

- The ON/OFF state of the LDOs in ACTIVE state is controlled by the corresponding LDOx\_EN bit in the ENABLE\_CTRL register.
- The ON/OFF state of the LDOs in STBY state is controlled by the corresponding LDOx\_STBY\_EN bit in the STBY\_1\_CONFIG register.
- In INITIALIZE state, the LDOs are off, regardless of bit-settings.

#### CAUTION

In case of linear regulators that are not to be used at all, the VLDOx pin must be left floating.

- Each of the LDOs can be configured as linear regulators or be configured as a load-switch (LSW-mode). LDO1 and LDO2 can also operate in bypass-mode. The mode is configured by LDOx\_LSW\_CONFIG and LSW\_BYP\_CONFIG bits in LDOx\_VOUT register individually per regulator.

#### CAUTION

A mode change between LDO(/bypass) and LSW-mode must only be performed, when the regulator is disabled!

(A change between LDO and bypass-mode (supported by LDO1 and LDO2 only) is supported during operation.)

- The LDOs have an active discharge function. Whenever LDOx is disabled, the output is discharged to ground. The discharge function can be disabled individually per rail in the DISCHARGE\_CONFIG register.
- Prior to a sequence into ACTIVE state (from INITIALIZE or STBY state), the device discharges the disabled rails regardless of the discharge-configuration to avoid starting into a pre-biased output.
- If a rail is enabled by an I2C-command, active discharge is not enforced, but the rail is only enabled if the output voltage is below the SCG-threshold.
- This register is not EEPROM-backed and is reset if the device enters OFF-state.
- When in INITIALIZE state (during RESET or an I2C-OFF-request), the discharge configuration is not reset. Note: the power-down-sequence can be violated if the discharge function is disabled

## LDO Fault Handling

- The TPS65219 detects under-voltages on the LDO-outputs. The reaction to the detection of an under-voltage is dependent on the configuration of the LDOx\_UV\_MASK bit in INT\_MASK\_LDOS register and the MASK\_EFFECT in INT\_MASK\_BUCKS register. If not masked, the device sets bit INT\_LDO\_1\_2\_IS\_SET respectively INT\_LDO\_3\_4\_IS\_SET bit in INT\_SOURCE register and bit LDOx\_UV in INT\_LDO\_1\_2 register respectively INT\_LDO\_3\_4 register.

During a voltage transition (at power-up or triggered by toggling VSEL\_SD-pin or an I2C-command), the device blanks the undervoltage detection by default and activates the undervoltage detection when the voltage transition completed.

If the device detects an undervoltage during the sequence into ACTIVE state (from INITIALIZE or STBY) and UV is not masked, the power-down-sequence starts at the end of the current slot.

If the device detects an undervoltage in ACTIVE-state or STBY-state and UV is not masked, the power-down sequence starts immediately. OC-detection is not maskable.

### CAUTION

If a LDO is configured in bypass-mode or LSW-mode, UV-detection is not supported.

- The TPS65219 provides current-limit on the LDO-outputs. If the PMIC detects over-current for  $t_{\text{DEGLITCH\_OC\_short}}$ , respectively for  $t_{\text{DEGLITCH\_OC\_long}}$  (configurable individually per rail with EN\_LONG\_DEGL\_FOR\_OC\_LDOx in OC\_DEGL\_CONFIG register; applicable for rising-edge only), the device sets INT\_LDO\_1\_2\_IS\_SET respectively INT\_LDO\_3\_4\_IS\_SET bit in INT\_SOURCE register and bit LDOx\_OC in INT\_LDO\_1\_2 respectively INT\_LDO\_3\_4 register. The effected rail is disabled immediately.

During a voltage transition (at power-up or triggered by toggling VSEL\_SD-pin or an I2C-command), the overcurrent detection is blanked and gets activated when the voltage transition completed.

If the over-current occurs during the sequence into ACTIVE state (from INITIALIZE or STBY), the device disables the affected rail immediately and starts the power-down-sequence at the end of the current slot.

If the over-current occurs in ACTIVE-state or STBY-state, the device disables the affected rail immediately and starts the power-down sequence.

OC-detection is not maskable, but the deglitch-time is configurable. It is strongly recommended to use  $t_{\text{DEGLITCH\_OC\_short}}$ . Extended over-current can lead to increased aging or overshoot upon recovery.

- The TPS65219 detects short-to-ground (SCG) faults on the LDO-outputs. The reaction to the detection of an SCG event is to set INT\_LDO\_1\_2\_IS\_SET respectively INT\_LDO\_3\_4\_IS\_SET bit in INT\_SOURCE register and bit LDOx\_SCG in INT\_LDO\_1\_2 register respectively INT\_LDO\_3\_4 register. The affected rail is disabled immediately. The device sequences down all outputs and transitions into INITIALIZE state.

SCG-detection is not maskable.

If a rail gets enabled, the device blanks SCG detection initially to allow the rail to ramp above the SCG-threshold.

- The TPS65219 detects residual voltage (RV) faults on the LDO-outputs. The reaction to the detection of an RV event is to set INT\_RV\_IS\_SET bit in INT\_SOURCE register and bit LDOx\_RV in INT\_RV register. The RV-detection is not maskable, but the nINT-reaction can be configured globally for all rails by MASK\_INT\_FOR\_RV in INT\_MASK\_WARM register. The device sets the LDOx\_RV-flag regardless of masking, INT\_RV\_IS\_SET bit is only set if nINT is asserted. The fault-reaction time and potential state-transition depends on the situation when the faults are detected:
  - If the device detects residual voltage during an ON-request in the INITIALIZE state, the PMIC gates power-up and the device remains in INITIALIZE state. If the RV-condition is detected for more than 4ms to 5ms, the device sets the LDOx\_RV-bit but remains in INITIALIZE state as long as the RV-condition exists. If the RV-condition is not present any more, the device transitions to ACTIVE state, provided the ON-request is still valid.

- If the device detects residual voltage during power-up, ACTIVE\_TO\_STANDBY, or STANDBY\_TO\_ACTIVE sequences, the sequence is aborted and the device powers down.
- If the device detects residual voltage for more than 80ms on any rail that was disabled during STBY state during a request to leave STBY state, the device transitions into INITIALIZE state. The device sets the LDOx\_RV-bit if the condition persists for 4ms to 5ms, but less than 80ms.
- If the device detects residual voltage during power-up, ACTIVE\_TO\_STANDBY, or STANDBY\_TO\_ACTIVE sequences, the sequence is aborted and the device powers down.
- If the device detects residual voltage during an EN-command of the rail by I2C, the LDOx\_RV-bit is set immediately, but no state transition occurs.
- The LDOs have a local over-temperature sensor. The reaction to a temperature warning is dependent on the configuration of the respective SENSOR\_x\_WARM\_MASK bit in and the MASK\_EFFECT bit in INT\_MASK\_BUCKS register. If the temperature at the sensor exceeds  $T_{WARM\_Rising}$  and is not masked, the device sets INT\_SYSTEM\_IS\_SET bit in INT\_SOURCE register and SENSOR\_x\_WARM bit in INT\_SYSTEM register. In case the sensor detects a temperature exceeding  $T_{HOT\_Rising}$ , the converters power dissipation and junction temperature exceeds safe operating value. The device powers down all active outputs immediately and sets INT\_SYSTEM\_IS\_SET bit in INT\_SOURCE register and SENSOR\_x\_HOT bit in INT\_SYSTEM register. The TPS65219 automatically recovers once the temperature drops below the  $T_{WARM\_Falling}$  threshold value (or below the  $T_{HOT\_Falling}$  threshold value in case  $T_{WARM}$  is masked). The \_HOT bit remains set and needs to be cleared by writing '1'. The HOT-detection is not maskable.

**Table 7-2. LDO Output Voltage Settings**

| LDOx_VSET [decimal] | LDOx_VSET [binary] | LDOx_VSET [hexa-decimal] | VOUT (LDO1 and LDO2, LDO mode) [V] | VOUT (LDO1 and LDO2, bypass-mode) [V] | VOUT (LDO3 and LDO4, LDO mode) [V] |
|---------------------|--------------------|--------------------------|------------------------------------|---------------------------------------|------------------------------------|
| 0                   | 000000             | 00                       | 0.60                               | reserved                              | 1.20                               |
| 1                   | 000001             | 01                       | 0.65                               | reserved                              | 1.20                               |
| 2                   | 000010             | 02                       | 0.70                               | reserved                              | 1.20                               |
| 3                   | 000011             | 03                       | 0.75                               | reserved                              | 1.20                               |
| 4                   | 000100             | 04                       | 0.80                               | reserved                              | 1.20                               |
| 5                   | 000101             | 05                       | 0.85                               | reserved                              | 1.20                               |
| 6                   | 000110             | 06                       | 0.90                               | reserved                              | 1.20                               |
| 7                   | 000111             | 07                       | 0.95                               | reserved                              | 1.20                               |
| 8                   | 001000             | 08                       | 1.00                               | reserved                              | 1.20                               |
| 9                   | 001001             | 09                       | 1.05                               | reserved                              | 1.20                               |
| 10                  | 001010             | 0A                       | 1.10                               | reserved                              | 1.20                               |
| 11                  | 001011             | 0B                       | 1.15                               | reserved                              | 1.20                               |
| 12                  | 001100             | 0C                       | 1.20                               | reserved                              | 1.20                               |
| 13                  | 001101             | 0D                       | 1.25                               | reserved                              | 1.25                               |
| 14                  | 001110             | 0E                       | 1.30                               | reserved                              | 1.30                               |
| 15                  | 001111             | 0F                       | 1.35                               | reserved                              | 1.35                               |
| 16                  | 010000             | 10                       | 1.40                               | reserved                              | 1.40                               |
| 17                  | 010001             | 11                       | 1.45                               | reserved                              | 1.45                               |
| 18                  | 010010             | 12                       | 1.50                               | 1.50                                  | 1.50                               |
| 19                  | 010011             | 13                       | 1.55                               | 1.55                                  | 1.55                               |
| 20                  | 010100             | 14                       | 1.60                               | 1.60                                  | 1.60                               |
| 21                  | 010101             | 15                       | 1.65                               | 1.65                                  | 1.65                               |
| 22                  | 010110             | 16                       | 1.70                               | 1.70                                  | 1.70                               |

**Table 7-2. LDO Output Voltage Settings (continued)**

| LDOx_VSET [decimal] | LDOx_VSET [binary] | LDOx_VSET [hexa-decimal] | VOUT (LDO1 and LDO2, LDO mode) [V] | VOUT (LDO1 and LDO2, bypass-mode) [V] | VOUT (LDO3 and LDO4, LDO mode) [V] |
|---------------------|--------------------|--------------------------|------------------------------------|---------------------------------------|------------------------------------|
| 23                  | 010111             | 17                       | 1.75                               | 1.75                                  | 1.75                               |
| 24                  | 011000             | 18                       | 1.80                               | 1.80                                  | 1.80                               |
| 25                  | 011001             | 19                       | 1.85                               | 1.85                                  | 1.85                               |
| 26                  | 011010             | 1A                       | 1.90                               | 1.90                                  | 1.90                               |
| 27                  | 011011             | 1B                       | 1.95                               | 1.95                                  | 1.95                               |
| 28                  | 011100             | 1C                       | 2.00                               | 2.00                                  | 2.00                               |
| 29                  | 011101             | 1D                       | 2.05                               | 2.05                                  | 2.05                               |
| 30                  | 011110             | 1E                       | 2.10                               | 2.10                                  | 2.10                               |
| 31                  | 011111             | 1F                       | 2.15                               | 2.15                                  | 2.15                               |
| 32                  | 100000             | 20                       | 2.20                               | 2.20                                  | 2.20                               |
| 33                  | 100001             | 21                       | 2.25                               | 2.25                                  | 2.25                               |
| 34                  | 100010             | 22                       | 2.30                               | 2.30                                  | 2.30                               |
| 35                  | 100011             | 23                       | 2.35                               | 2.35                                  | 2.35                               |
| 36                  | 100100             | 24                       | 2.40                               | 2.40                                  | 2.40                               |
| 37                  | 100101             | 25                       | 2.45                               | 2.45                                  | 2.45                               |
| 38                  | 100110             | 26                       | 2.50                               | 2.50                                  | 2.50                               |
| 39                  | 100111             | 27                       | 2.55                               | 2.55                                  | 2.55                               |
| 40                  | 101000             | 28                       | 2.60                               | 2.60                                  | 2.60                               |
| 41                  | 101001             | 29                       | 2.65                               | 2.65                                  | 2.65                               |
| 42                  | 101010             | 2A                       | 2.70                               | 2.70                                  | 2.70                               |
| 43                  | 101011             | 2B                       | 2.75                               | 2.75                                  | 2.75                               |
| 44                  | 101100             | 2C                       | 2.80                               | 2.80                                  | 2.80                               |
| 45                  | 101101             | 2D                       | 2.85                               | 2.85                                  | 2.85                               |
| 46                  | 101110             | 2E                       | 2.90                               | 2.90                                  | 2.90                               |
| 47                  | 101111             | 2F                       | 2.95                               | 2.95                                  | 2.95                               |
| 48                  | 110000             | 30                       | 3.00                               | 3.00                                  | 3.00                               |
| 49                  | 110001             | 31                       | 3.05                               | 3.05                                  | 3.05                               |
| 50                  | 110010             | 32                       | 3.10                               | 3.10                                  | 3.10                               |
| 51                  | 110011             | 33                       | 3.15                               | 3.15                                  | 3.15                               |
| 52                  | 110100             | 34                       | 3.20                               | 3.20                                  | 3.20                               |
| 53                  | 110101             | 35                       | 3.25                               | 3.25                                  | 3.25                               |
| 54                  | 110110             | 36                       | 3.30                               | 3.30                                  | 3.30                               |
| 55                  | 110111             | 37                       | 3.35                               | 3.35                                  | 3.30                               |
| 56                  | 111000             | 38                       | 3.40                               | 3.40                                  | 3.30                               |
| 57                  | 111001             | 39                       | 3.40                               | 3.40                                  | 3.30                               |
| 58                  | 111010             | 3A                       | 3.40                               | 3.40                                  | 3.30                               |
| 59                  | 111011             | 3B                       | 3.40                               | 3.40                                  | 3.30                               |

**Table 7-2. LDO Output Voltage Settings (continued)**

| LDOx_VSET [decimal] | LDOx_VSET [binary] | LDOx_VSET [hexadecimal] | VOUT (LDO1 and LDO2, LDO mode) [V] | VOUT (LDO1 and LDO2, bypass-mode) [V] | VOUT (LDO3 and LDO4, LDO mode) [V] |
|---------------------|--------------------|-------------------------|------------------------------------|---------------------------------------|------------------------------------|
| 60                  | 111100             | 3C                      | 3.40                               | 3.40                                  | 3.30                               |
| 61                  | 111101             | 3D                      | 3.40                               | 3.40                                  | 3.30                               |
| 62                  | 111110             | 3E                      | 3.40                               | 3.40                                  | 3.30                               |
| 63                  | 111111             | 3F                      | 3.40                               | 3.40                                  | 3.30                               |

### 7.3.7 Interrupt Pin (nINT)

During power-up, the output of the nINT pin does depend on whether any INT\_SOURCE flags are set and the configuration of the MASK\_EFFECT bit in INT\_MASK\_BUCKS register-. If one or more flags are set, then nINT pin is pulled low and is only released high after those flags have been cleared by writing '1' to them. Note, the nINT-pin only transitions 'high' if a VIO-voltage for the pull-up is available.

In ACTIVE or STBY state, the nINT pin signals any event or fault condition to the host processor. Whenever a fault or event occurs in the IC, the corresponding interrupt bit is set in the INT register, and the open-drain output is driven low. In case the device transitions to INITIALIZE state, the nINT pin is pulled low as well, regardless if the transition is triggered by an OFF-request or a fault.

If the fault is no longer present, a W1C (write '1' to clear) needs to be performed on the failure bits. This command also allows the nINT-pin to release (return to Hi-Z state).

If a failure persists, the corresponding bit remains set and the INT pin remains low.

The UV-faults are individually maskable per rail in INT\_MASK\_UV registers. The thermal sensors are individually maskable by SENSOR\_x\_WARM\_MASK in the MASK\_CONFIG register. The effect of the masking for UV and WARM is defined globally by MASK\_EFFECT bits in MASK\_CONFIG register.

The nINT reaction for RV-faults is defined globally by MASK\_INT\_FOR\_RV bits in MASK\_CONFIG register.

- 00b = no state change, no nINT reaction, no bit set
- 01b = no state change, no nINT reaction, bit set
- 10b = no state change, nINT reaction, bit set (same as 11b)
- 11b = no state change, nINT reaction, bit set (same as 10b)

#### CAUTION

Masking poses a risk to the device or the system. In case the masking is performed by I2C-command, the masking bits do get reset to EEPROM-based default after transitioning to INITIALIZE state. Bits corresponding to faults newly configured via I2C as SD-faults do not get cleared.

It is strongly discouraged to mask OC- and UV-detection on the same rail.

### 7.3.8 PWM/PFM and Low Power Modes (MODE/STBY)

The TPS65219 supports low power modes through the I2C-control or through the MODE/STBY pin. The configuration of the pin is selected by MODE\_STBY\_CONFIG in MFP\_2\_CONFIG register. Configure the polarity of this pin by writing to MODE\_STBY\_POLARITY in MFP\_1\_CONFIG register. The polarity-configuration must not change after power-up. Only either MODE/RESET or MODE/STBY must be configured as MODE. If both are configured as MODE, MODE/RESET takes priority and MODE/STBY is ignored.

#### MODE/STBY configured as 'MODE':

- If configured as 'MODE', the pin-status determines the switching-mode of the buck-converters.
- Forcing this pin for longer than  $t_{DEGLITCH\_MFP}$  forces the buck-regulators into PWM-mode (irrespective of load current). De-asserting this pin low allows the buck regulators to enter PFM-mode. The entry into PFM and

exit from PFM is governed by the load current. Only one pin, either MODE/STBY or MODE/RESET must be configured as 'MODE'.

- Control the selection of auto-PFM/forced-PWM by writing to the bit MODE\_I2C\_CTRL in MFP\_1\_CONFIG register.
- A change of the MODE does not cause a state-transition.
- During power-up of any one of the three bucks, a MODE change is blanked on this rail and only takes effect after the ramp completed.

**MODE/STBY configured as 'STBY':**

- Forcing this pin for longer than  $t_{DEGLITCH\_MFP}$  sequences down the rails selected to turn off in the STBY\_1\_CONFIG respectively the STBY\_2\_CONFIG register. De-asserting this pin sequences the selected rails on again.
- Another method to transition into and out of STBY state is writing to the bit STBY\_I2C\_CTRL in MFP\_CTRL register, provided I2C communication is supported during STBY state.
- A change of the MODE/STBY pin configured as 'STBY' does cause a state-transition by definition.
- Regardless of the pin-setting, the device always powers up into ACTIVE state. The device reacts to the STBY-pin-state or I2C-commands only after entering ACTIVE state.

**MODE/STBY configured as 'MODE & STBY':**

- The pin is configurable to perform both functions, MODE and STBY simultaneously
- Forcing this pin for longer than  $t_{DEGLITCH\_MFP}$  sequences down the rails selected to turn off in the STBY\_1\_CONFIG respectively the STBY\_2\_CONFIG register and allows auto-PFM entry (only applicable in quasi-fixed-frequency mode). De-asserting this pin sequences the selected rails on again and forces the buck-regulators to forced-PWM. Polarity settings need to be harmonized for this configuration.
- If a transition into and out of STBY state is commanded by writing to the bit STBY\_I2C\_CTRL in MFP\_CTRL register (provided I2C communication is supported during STBY state), a separate command for the MODE-change is required by writing to the bit MODE\_I2C\_CTRL in MFP\_1\_CONFIG register.
- A change of the MODE/STBY pin configured as 'MODE&STBY' does cause a state-transition by definition.
- By default STBY is deasserted and the pin is ignored until the device completed the power-up-sequence. During power-up of any one of the three bucks, a MODE-change is blanked on this rail and only takes effect after the ramp completed. A state-change commanded by STBY-pin is reacted to even during the ramp of rails (except during INITIALIZE-to-ACTIVE transition).

Please see below truth-table for pin- and I2C-commands.

**Table 7-3. MODE/STBY Configuration**

| Pin Name  | Pin Configuration (MODE_STBY_CONFIG) | Pin Polarity (MODE_STBY_POLARITY) | Pin state (schematic) | I2C control (MODE_I2C_CTRL) | Resulting Function |
|-----------|--------------------------------------|-----------------------------------|-----------------------|-----------------------------|--------------------|
| MODE/STBY | MODE                                 | x                                 | x                     | 1h                          | forced PWM         |
| MODE/STBY | MODE                                 | 0h                                | L                     | 0h                          | auto-PFM           |
| MODE/STBY | MODE                                 | 0h                                | H                     | 0h                          | forced PWM         |
| MODE/STBY | MODE                                 | 1h                                | L                     | 0h                          | forced PWM         |
| MODE/STBY | MODE                                 | 1h                                | H                     | 0h                          | auto-PFM           |
| MODE/STBY | STBY                                 | 0                                 | L                     | x                           | STBY               |
| MODE/STBY | STBY                                 | 0                                 | H                     | x                           | ACTIVE             |
| MODE/STBY | STBY                                 | 1                                 | L                     | x                           | ACTIVE             |
| MODE/STBY | STBY                                 | 1                                 | H                     | x                           | STBY               |

### 7.3.9 PWM/PFM and Reset (MODE/RESET)

This pin is configurable as an alternative MODE pin (in case MODE/STBY is configured for STBY-function) or as a RESET pin. The configuration of the pin is selected by MODE\_RESET\_CONFIG in MFP\_2\_CONFIG register. Configure the polarity of this pin by writing to MODE\_RESET\_POLARITY in MFP\_1\_CONFIG register. The polarity-configuration must not change after power-up. Only MODE/RESET or MODE/STBY must be configured as MODE. If both are configured as MODE, MODE/RESET takes priority and MODE/STBY is ignored.

#### MODE/RESET configured as 'MODE':

- If configured as 'MODE', the pin-status determines the switching-mode of the buck-converters.
- Forcing this pin for longer than  $t_{\text{DEGLITCH\_MFP}}$  forces the buck-regulators into PWM-mode (irrespective of load current). De-asserting this pin low allows the buck regulators to enter PFM-mode. The entry into PFM and exit from PFM is governed by the load current. Only one pin, either MODE/STBY or MODE/RESET must be configured as 'MODE'.
- Another method to control the selection of auto-PFM/forced-PWM is writing to the bit MODE\_I2C\_CTRL in MFP\_1\_CONFIG register.
- A change of the MODE does not cause a state-transition.
- During power-up of any one of the three bucks, a MODE-change is blanked on this rail and only takes effect after the ramp completed.

#### MODE/RESET configured as 'RESET':

- In RESET configuration, this pin is edge sensitive, but still applies the deglitch time. Consequently, toggling this pin and holding the pin for longer than  $t_{\text{DEGLITCH\_RESET}}$  causes a reset.
- By default, RESET is deasserted and RESET requests, via pin or I2C, are only serviced if the device is in ACTIVE state, STBY state, or transitions between these 2 states.
- The TPS65219 supports WARM or COLD reset. The configuration is made by bit WARM\_COLD\_RESET\_CONFIG in MFP\_2\_CONFIG register.
  - If configured for COLD reset, the device executes the power down sequence and transitions to INITIALIZE state. Then, EEPROM is reloaded and rails power-up again in normal power-up-sequence, provided there are no faults and no OFF-request. The execution of a COLD-reset sets the bit COLD\_RESET\_ISSUED in POWER\_UP\_STATUS\_REG register. The read-out of this bit allows to track if a COLD-reset was performed. The bit gets set regardless if the reset was commanded by I2C or by the pin. The nINT-pin does not toggle based on this bit. Write W1C to clear the bit.
  - If configured for WARM reset, all enabled rails remain on, but the output voltage of rails that support dynamic voltage change is reset to the boot-voltage. Specifically, following configurations get reset to the respective boot-values: BUCK1\_VSET, BUCK2\_VSET, BUCK3\_VSET, LDO1\_VSET, LDO2\_VSET, LDO1\_BYP\_CONFIG, LDO2\_BYP\_CONFIG and VSEL\_SD\_I2C\_CTRL.

All other bits, even in the same register, remain at the respective state. For example, LDOx\_LSW\_CONFIG, BUCKx\_BW\_SEL, BUCKx\_UV\_THR\_SEL and the MFP\_1\_CONFIG register bits do NOT get reset during a WARM-reset.

WARM Reset doesnot override the VSEL\_SD-pin command. In other words: even if a WARM Reset occurs, if the VSEL\_SD pin is commanding 1.8V-LDO mode, that remain in effect.

- Writing to the bit WARM\_RESET\_I2C\_CTRL respectively the bit COLD\_RESET\_I2C\_CTRL in MFP\_CTRL register also triggers a reset.

---

#### Note

Shut-down-faults and OFF-requests take priority over a RESET-request. If a RESET-requests occurs simultaneously with one of those, the device enters INITIALIZE state and requires a new ON-request to start up.

Reset requests, via pin or I2c, are only serviced in ACTIVE state, STBY state, or a transition between these two states.

---

Please see below truth-table for pin- and I2C-commands.

**Table 7-4. MODE/RESET Configuration**

| Pin Name   | Pin Configuration (MODE_RESET_CONFIG) | Pin Polarity (MODE_RESET_POLARITY) | Pin state (schematic) | I2C control (MODE_I2C_CTRL) | Resulting Function |
|------------|---------------------------------------|------------------------------------|-----------------------|-----------------------------|--------------------|
| MODE/RESET | MODE*                                 | x                                  | x                     | 1h                          | forced PWM         |
| MODE/RESET | MODE*                                 | 0h                                 | L                     | 0h                          | auto-PFM           |
| MODE/RESET | MODE*                                 | 0h                                 | H                     | 0h                          | forced PWM         |
| MODE/RESET | MODE*                                 | 1h                                 | L                     | 0h                          | forced PWM         |
| MODE/RESET | MODE*                                 | 1h                                 | H                     | 0h                          | auto-PFM           |
| MODE/RESET | RESET                                 | 0                                  | L                     | x                           | RESET              |
| MODE/RESET | RESET                                 | 0                                  | H                     | x                           | normal operation   |
| MODE/RESET | RESET                                 | 1                                  | L                     | x                           | normal operation   |
| MODE/RESET | RESET                                 | 1                                  | H                     | x                           | RESET              |

The \* for MODE indicates that the MODE/RESET pin takes priority in case both, MODE/RESET and MODE/STBY are configured as 'MODE', and thus the respective pin to be observed is MODE/RESET.

#### 7.3.10 Voltage Select Pin (VSEL\_SD/VSEL\_DDR)

The function of this pin is configured by VSEL\_DDR\_SD in MFP\_1\_CONFIG.

When configured as VSEL\_SD, the bit VSEL\_RAIL in MFP\_1\_CONFIG register selects LDO1 or LDO2 to be controlled by the pin. The configuration must not change after power-up.

##### VSEL\_SD/VSEL\_DDR configured as 'VSEL\_SD': SD-card-IO-select:

Configure the polarity of this pin by writing to VSEL\_SD\_POLARITY in MFP\_1\_CONFIG register. Toggling the pin changes the output voltage of the selected LDO between hard-coded 1.8V and the voltage configured in LDOx\_VOUT. For the SD-card-IO-supply, LDOx\_VOUT must be configured for 3.3V. A change of the VSEL\_SD status does not cause a state-transition.

**CAUTION**

In SD-card-configuration, customer must configure the pin-polarity and drive the pin so that the LDO delivers 3.3V at start-up.

##### VSEL\_SD/VSEL\_DDR configured as 'VSEL\_DDR':

Pulling this pin high sets the output voltage of Buck3 to 1.35V (DDR3LV), leaving the pin floating sets the output voltage of Buck3 to 1.2V (DDR4, LP-DDR3, some LP-DDR2), pulling the pin low sets the output voltage of the Buck3 voltage configured in BUCK3\_VOUT. For LP-DDR4, BUCK3\_VOUT must be configured to 1.1V.

**CAUTION**

This function needs to be hard-wired and must not change during operation.

**CAUTION**

The VSEL\_RAIL still needs to be configured for the LDO that supplies the SD-card-IO-voltage, as an I2C-command toggles the selected LDO-rail for the SD-card. The VSEL\_SD\_POLARITY bit has no effect if the pin is configured as VSEL\_DDR.

The Table below shows the various combinations.

**Table 7-5. VSEL\_SD/VSEL\_DDR Configuration Options**

| Pin Configuration (VSEL_DDR_SD) | Pin Polarity (VSEL_SD_POLARITY) | Rail selection (VSEL_RAIL)                       | PIN state (schematic) | I2C control (VSEL_SD_I2C_CTRL)          | Resulting Function     |
|---------------------------------|---------------------------------|--|-----------------------|---|------------------------|
| DDR                             | n/a                             | 0 = LDO1<br>1 = LDO2<br>(needed for I2C control) | L                     | 0h: LDOx = 1.8V<br>1h: LDOx = LDOx_VSET | BUCK3 = Buck3_VSET     |
| DDR                             | n/a                             | 0 = LDO1<br>1 = LDO2<br>(needed for I2C control) | open                  | 0h: LDOx = 1.8V<br>1h: LDOx = LDOx_VSET | BUCK3 = 1.2V           |
| DDR                             | n/a                             | 0 = LDO1<br>1 = LDO2<br>(needed for I2C control) | H                     | 0h: LDOx = 1.8V<br>1h: LDOx = LDOx_VSET | BUCK3 = 1.35           |
| SD                              | 0                               | 0 = LDO1   | L                     | x                                       | LDO1 = 1.8V (LDO mode) |
| SD                              | 0                               | 0 = LDO1   | H                     | x                                       | LDO1 = LDO1_VSET       |
| SD                              | 1                               | 0 = LDO1   | L                     | x                                       | LDO1 = LDO1_VSET       |
| SD                              | 1                               | 0 = LDO1   | H                     | x                                       | LDO1 = 1.8V (LDO mode) |
| SD                              | 0                               | 1 = LDO2   | L                     | x                                       | LDO2 = 1.8V (LDO mode) |
| SD                              | 0                               | 1 = LDO2   | H                     | x                                       | LDO2 = LDO2_VSET       |
| SD                              | 1                               | 1 = LDO2   | L                     | x                                       | LDO2 = LDO2_VSET       |
| SD                              | 1                               | 1 = LDO2   | H                     | x                                       | LDO2 = 1.8V (LDO mode) |

### 7.3.11 General Purpose Inputs or Outputs (GPO1, GPO2, and GPIO)

GPO1 and GPO2 pins are always configured as an output.

The GPIO-pin is an input/output, however, the input-functionality is only used in multi-PMIC configuration. In single-PMIC configuration, the pin is typically used as an output. Read the state by polling the bit GPIO\_STATUS bit in MFP\_CTRL register.

The I/O-configuration of the GPIO-pin is done by the MULTI\_DEVICE\_ENABLE bit in MFP\_1\_CONFIG register.

If configured as outputs, these pins are able to sequence external rails. Include the GP(I)Os in the power sequence, or control them via I2C-interface, writing to GPOx\_EN respectively GPIO\_EN bit in GENERAL\_CONFIG register. The GPO is released high if activated.

The GPIO function is to be used if multiple TPS65219 need to be synchronized, in case more rails need to be supplied. See application section on usage. See section "Multi-PMIC operation" for details.

The polarity of these pins is not changeable.

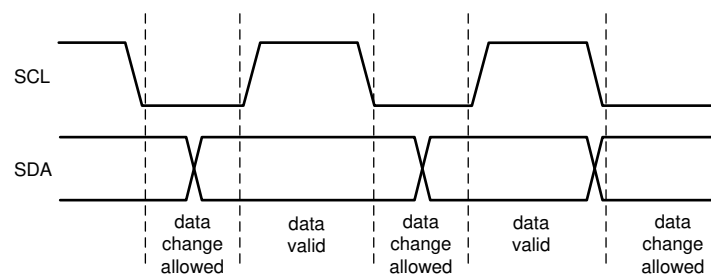
### 7.3.12 I<sup>2</sup>C-Compatible Interface

The default I<sup>2</sup>C 7-bit device address of the TPS65219 is set to 0x30 (0b0110000 in binary), but is changeable if needed, for example for multi-PMIC-operation.

The I<sup>2</sup>C-compatible synchronous serial interface provides access to the configurable functions and registers on the device. This protocol uses a two-wire interface for bidirectional communications between the devices connected to the bus. The two interface lines are the serial data line (SDA), and the serial clock line (SCL). Every device on the bus is assigned a unique address and acts as either a controller or a target depending on whether it generates or receives the serial clock SCL. The SCL and SDA lines must each have a pullup resistor placed somewhere on the line and remain HIGH even when the bus is idle. The TPS65219 supports standard mode (100kHz), fast mode (400kHz), and fast mode plus (1MHz) when VIO is 3.3V or 1.8V.

#### 7.3.12.1 Data Validity

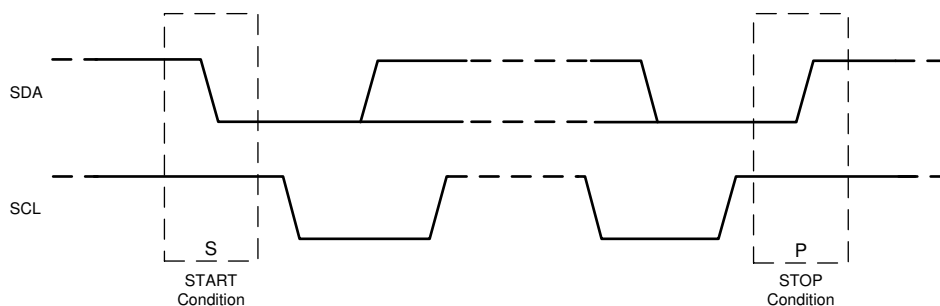
The data on the SDA line must be stable during the HIGH period of the clock signal (SCL). In other words, the state of the data line must only be changed when clock signal is LOW.



**Figure 7-4. Data Validity Diagram**

#### 7.3.12.2 Start and Stop Conditions

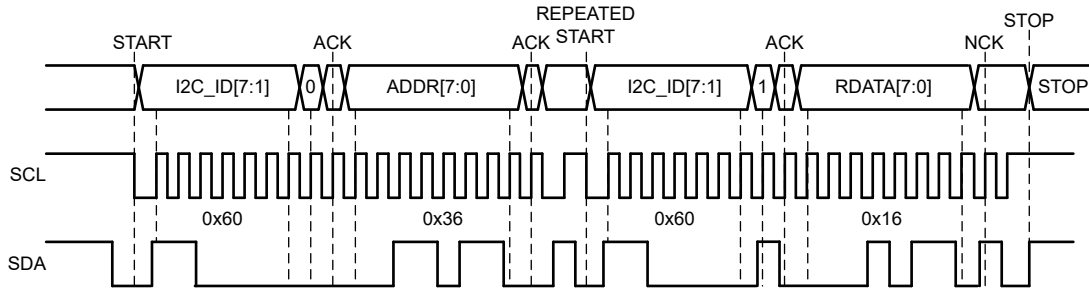
The device is controlled through an I<sup>2</sup>C-compatible interface. START and STOP conditions classify the beginning and end of the I<sup>2</sup>C session. A START condition is defined as the SDA signal going from HIGH to LOW while the SCL signal is HIGH. A STOP condition is defined as the SDA signal going from LOW to HIGH while the SCL signal is HIGH. The I<sup>2</sup>C controller device always generates the START and STOP conditions.



**Figure 7-5. Start and Stop Sequences**

The I<sup>2</sup>C bus is considered busy after a START condition and free after a STOP condition. The I<sup>2</sup>C controller device is permitted to generate repeated START conditions during data transmission. A START and a repeated START condition are equivalent function-wise. Figure 7-6 shows the SDA and SCL signal timing for the I<sup>2</sup>C-compatible bus. For timing values, see the *Specification* section.

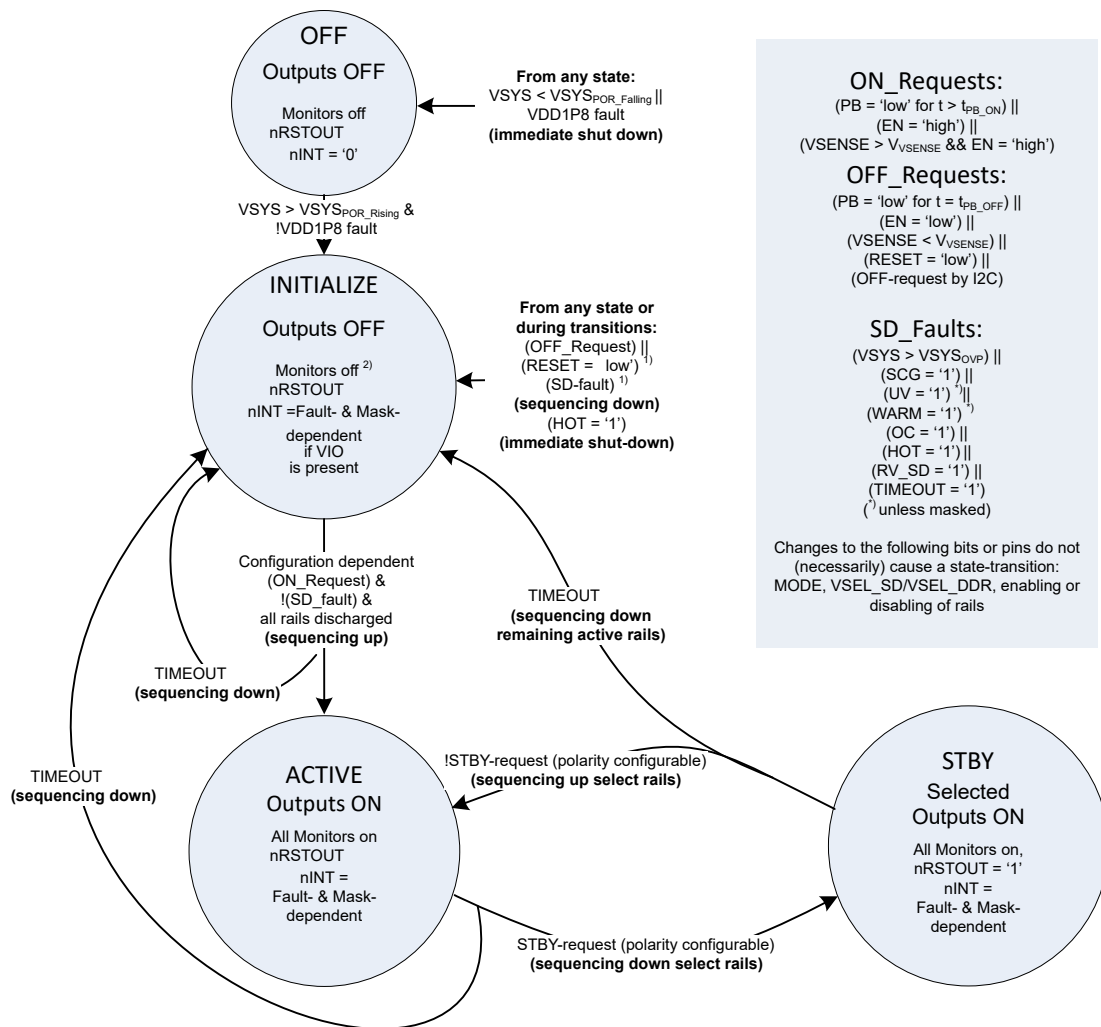




When READ function is to be accomplished, a WRITE function must precede the READ function as shown above.

Figure 7-9. I<sup>2</sup>C Read Cycle Without CRC

## 7.4 Device Functional Modes



1) in case of a RESET or a SD-fault, the device transitions from INITIALIZE state to the ACTIVE state without a new Push-button-ON\_Request. In EN or VSENSE configuration, the ON-request must still be valid to transition to ACTIVE state.

2) If INITIALIZE state was entered due to a Thermal-Shut-Down, the temperature monitors remain active until the temperature on all sensors fell below  $T_{WARM}$  threshold. Thermal-Shut-Down causes immediate shut-shutdown, no sequencing down

Figure 7-10. State Diagram

## 7.4.1 Modes of Operation

### 7.4.1.1 OFF State

In OFF state, the PMIC is insufficiently supplied. Neither internal logic nor external rails are available. If VSYS exceeds VSYS\_POR voltage and the internal 1.8V-rail (VDD1P8) is in regulation, the device enters the INITIALIZE state.

### 7.4.1.2 INITIALIZE State

In INITIALIZE state, the device is completely shut down with the exception of a few circuits to monitor the EN/PB/VSENSE input. Whenever entering the INITIALIZE state, the PMIC reads the memory and loads the registers to their EEPROM-default values. The I<sup>2</sup>C communication interface is turned off .

Entry to INITIALIZE state is gated if any one of the thermal sensors is above the  $T_{WARM\_Rising}$  threshold and WARM-detection is not masked.

The EEPROM loading takes approximately 2.3ms. The power-up sequence begins after the EEPROM-load and if all rails are discharged below the  $V_{BUCKx\_SCG\_TH}$  respectively  $V_{LDOx\_SCG\_TH}$  threshold.

If INITIALIZE state was entered from OFF state, bit POWER\_UP\_FROM\_OFF in POWER\_UP\_STATUS\_REG register is set and remains set until a write-1-clear is issued. Read-out of this bit allows to determine if INITIALIZE state was entered from OFF state or due to a Shut-down-fault or OFF-request.

In INITIALIZE state, the nINT pin status is dependent if faults are and masking thereof. If no faults are present or nINT-reaction for those are masked, nINT-pin is pulled high, provided a VIO-voltage for the pull-up is available.

To transition from the INITIALIZE state to the ACTIVE state, one of the ON-requests must occur:

- The EN input is 'high' (if EN/PB/VSENSE is configured as 'EN' or 'VSENSE')
- The PB input is pulled low for at least  $t_{PB\_ON\_SLOW}$  respectively  $t_{PB\_ON\_FAST}$  (if EN/PB/VSENSE is configured as 'PB')

#### Note

The DISCHARGE\_CONFIG register is purposefully omitted from RESET when entering INITIALIZE state from ACTIVE or STBY state. When entering INITIALIZE state from OFF state, the EEPROM content is loaded. If the discharge configuration changed after power-up, a different start-up behavior occurs, depending if the INITIALIZE state was entered from OFF state or from ACTIVE/STBY.

### 7.4.1.3 ACTIVE State

The ACTIVE state is the normal mode of operation when the system is up and running. All enabled buck converters and LDOs are operational and controllable through the I<sup>2</sup>C interface. After a wake-up event, the PMIC discharges potential residual voltages on the outputs, regardless of the discharge-configuration. ACTIVE state is directly enterable from STBY state by de-asserting the STBY pin high or by an I<sup>2</sup>C command. See STBY state description for details. To transition to STBY, the STBY pin must be forced or an I<sup>2</sup>C command to STBY\_I2C\_CTRL in MFP\_CTRL register must be issued.

To transition to INITIALIZE state, one of the following OFF\_Requests must occur:

- The EN input is 'low' (if EN/PB/VSENSE is configured as 'EN' or 'VSENSE')
- The PB input is pulled low for at least  $t_{PB\_OFF}$  (if EN/PB/VSENSE is configured as 'PB')
- An I<sup>2</sup>C OFF-request is issued

If a shut-down-fault (SD\_Fault) occurs while in the ACTIVE state, TPS65219 sequences down the active outputs and transition to the INITIALIZE state. The device does transition to ACTIVE state without a new Push-button-ON\_Request. In EN or VSENSE configuration, the ON-request must still be valid to transition to ACTIVE state.

### 7.4.1.4 STBY State

STBY state is a low-power mode of operation intended to support system standby. Enter this mode by the MODE/STBY pin, if configured as 'STBY' or by an I<sup>2</sup>C-command to STBY\_I2C\_CTRL in MFP\_CTRL

register. Typically, the majority of power rails are turned off with the exception of rails required by the SoC during this state. The power rails that remain on in STBY state are configurable in STBY\_1\_CONFIG and STBY\_2\_CONFIG register.

The monitoring functions are all available: Undervoltage- (UV), Short-to-GND- (SCG) and Over-current- (OC) detection, thermal warning (WARM) and thermal-shutdown (TSD/HOT) remain active.

The device enters ACTIVE state if STBY is de-asserted or an I2C command is received (provided VIO-supply remained active). Before starting the STBY to ACTIVE sequence, disabled rails are discharged. In case this fails to complete within 80ms, the device also runs into a timeout-condition and transitions to INITIALIZE state. The device sets bit TIMEOUT in the INT\_TIMEOUT\_RV\_SD register and the fault flags for the rail that caused the shut-down.

The sequence into and out of STBY state is the same as for power-down respectively for power-up. Rails that remain on in STBY are skipped, but the respective slots for those rails are still executed.

**CAUTION**

The device must first enter ACTIVE state before STBY, and is not capable of transitioning from INITIALIZE state to STBY state directly.

**CAUTION**

The device does not turn on previously disabled rails in STBY-state. Activity in STBY-state requires a AND-combination of LDOx\_EN / BUCKx\_EN and LDOx\_STBY\_EN/BUCKx\_STBY\_EN.

**CAUTION**

Do not change the registers related to an ongoing sequence by I2C-command!

Non-NVM-bits are not accessible for approximately 80us after starting a transition into INITIALIZE state.

#### 7.4.1.5 Fault Handling

##### Detectable Faults

The TPS65219 offers various fault-detections. Per default, all of them lead to a sequenced shut-down. Some of them are maskable and the reaction to masked faults is configurable.

The device provides the following fault-detections on the supply voltage (VSYS) and internal voltage supply (VDD1P8):

- Undervoltage on VSYS, resulting in transition to OFF state or gating start-up
- Overvoltage-protection on VSYS, resulting in transition to OFF state
- Under- or Overvoltage on internal 1.8V-supply (VDD1P8), resulting in transition to OFF state or gating start-up.

None of these faults are maskable.

The TPS65219 provides the following fault-detections on the buck- and LDO-outputs:

- Undervoltage detection (UV)
- Over Current detection (OC), triggering on positive as well as (for buck-converters) negative current-limit
- Short-to-GND detection (SCG)
- Temperature warning (WARM) and Thermal Shut Down (TSD / HOT)
- Residual Voltage (RV) and Residual Voltage - Shutdown (RV\_SD)
- Timeout (TO)

SCG, OC, HOT, RV\_SD and TO are not maskable. If any one of those occurs, the device powers down. Positive and negative current limit share the same mask-bit per regulator.

The reaction to UV, RV and WARM faults is configurable. If not masked, a fault triggers a sequenced shut-down. UV, RV and WARM are maskable individually per regulator in INT\_MASK\_BUCKS, INT\_MASK\_LDOS and INT\_MASK\_WARM registers. No state-transition occurs in case of a masked fault. Whether bits are set and if nINT is pulled low are globally configurable by MASK\_EFFECT bits in MASK\_CONFIG register. Positive and negative current limit share the same mask-bit per regulator.

- 00b = no state change, no nINT reaction, no bit set
- 01b = no state change, no nINT reaction, bit set
- 10b = no state change, nINT reaction, bit set (same as 11b)
- 11b = no state change, nINT reaction, bit set (same as 10b)

For any fault that corresponds to a shut-down condition, the fault-bit remains asserted until a W1C (write-one-clear) operation is performed via I2C (assuming the fault is not present any more). In case of a shut-down fault, no renewed on-request is required. The device automatically executes the power up sequence if the fault is no longer present as long as EN/VSENSE is still high and no PB-press is required for a restart.

For any fault that is not a shut-down condition (for example because the fault is masked), the bit is cleared when going to the INITIALIZE state.

### Thermal Warning and Shutdown

There are two thermal thresholds: Thermal-warning (WARM) and Thermal Shutdown (TSD / HOT).

- *Thermal Warning, WARM-threshold:*
- if the temperature exceeds  $T_{WARM\_Rising}$  threshold, the SENSOR\_x\_WARM-bit is set and the PMIC sequences down (unless masked).
- if the temperature fell below  $T_{WARM\_Falling}$  threshold, the device powers up again, without a new Push-button-ON\_Request. In EN or VSENSE configuration, the ON-request must still be valid to transition to ACTIVE state.
- if the temperature exceeds  $T_{WARM\_Rising}$  threshold, but SENSOR\_x\_WARM\_MASK bit is /bits are set, the PMIC remains in ACTIVE state. Fault-reporting occurs as configured by MASK\_EFFECT bits. The processor makes the decision to either sequence the power down or throttles back on the running applications to reduce the power consumption and hopefully avoiding a Thermal Shutdown situation.
- *Thermal Shutdown, HOT-threshold, applicable if WARM-threshold is masked:*
- if the temperature exceeds  $T_{HOT\_Rising}$  threshold, the SENSOR\_x\_HOT-bit is set and the PMIC powers off all rails immediately. This power down is simultaneously and not sequenced.
- in case ALL sensors are masked for WARM-detection (all SENSOR\_x\_WARM\_MASK bits are set), the PMIC does power back up once the temperature drops below the  $T_{HOT\_Falling}$  threshold, provided a valid ON-request is present.
- in case any one of the sensors is unmasked for WARM-detection, the PMIC does power back up once the temperature drops below the  $T_{WARM\_Falling}$  threshold, without a new Push-button-ON\_Request. In EN or VSENSE configuration, the ON-request must still be valid to transition to ACTIVE state.

### Residual Voltage

Residual voltage checks are performed at various occasions: before starting the INITIALIZE- to ACTIVE-transition and any time before a rail is enabled, regardless if during the sequence, by I2C-command or during the STBY- to ACTIVE-transition. RV-checks are also performed during the sequences, to detect if a rail that is supposed to be disabled is pulled up by another rail. The treatment of RV-faults depends on the situation when the fault occurs:

- INITIALIZE to ACTIVE:
  - if residual voltage is detected for more than 4ms to 5ms prior to the execution of the sequence, the respective INT\_RV\_IS\_SET bit in INT\_SOURCE register and LDOx\_RV respectively BUCKx\_RV bit in

- INT\_RV register is set and remains set, even if the discharge is successful at a later time and the ON-request is executed.
- if the residual voltage is detected during the sequence, this constitutes a shutdown-fault: the device initiates the power-down-sequence at the end of the slot-duration. The device sets the respective INT\_TIMEOUT\_RV\_SD\_IS\_SET bit in INT\_SOURCE register, LDOx\_RV\_SD respectively BUCKx\_RV\_SD bit and bit TIMEOUT in INT\_TIMEOUT\_RV\_SD register.
  - ACTIVE to STBY:
    - if active discharge is enabled and residual voltage is detected after eight times the power-down slot-duration, this constitutes a shutdown-fault: the device sequences down at the end of the slot. The device sets INT\_TIMEOUT\_RV\_SD\_IS\_SET bit in INT\_SOURCE register, the LDOx\_RV\_SD respectively BUCKx\_RV\_SD bit and the bit TIMEOUT in INT\_TIMEOUT\_RV\_SD register.
    - if the residual voltage is detected during the sequence, this constitutes a shutdown-fault: the device sequences down at the end of the slot-duration and sets bit INT\_TIMEOUT\_RV\_SD\_IS\_SET in INT\_SOURCE register and LDOx\_RV\_SD respectively BUCKx\_RV\_SD bit in INT\_TIMEOUT\_RV\_SD register.
  - STBY to ACTIVE:
    - if residual voltage is detected prior to the execution of the sequence for more than 4ms to 5ms, the device sets INT\_RV\_IS\_SET bit in INT\_SOURCE register and LDOx\_RV respectively BUCKx\_RV bit in INT\_RV register. The bit remains set, even if the discharge is successful before timeout expires and the STBY-to-ACTIVE-sequence is executed.
    - if residual voltage is detected for more than 80ms prior to the execution of the sequence, this constitutes a shutdown-fault: the device sequences down and sets the bit INT\_TIMEOUT\_RV\_SD\_IS\_SET in INT\_SOURCE register and LDOx\_RV\_SD respectively BUCKx\_RV\_SD bit in INT\_TIMEOUT\_RV\_SD register. In addition, the device sets the bit TIMEOUT in INT\_TIMEOUT\_RV\_SD register.
    - if the residual voltage is detected during the sequence, this constitutes a shutdown-fault: the device sequences down at the end of the slot-duration and sets the INT\_TIMEOUT\_RV\_SD\_IS\_SET bit in INT\_SOURCE register and LDOx\_RV\_SD respectively BUCKx\_RV\_SD bit in INT\_TIMEOUT\_RV\_SD register. The TIMEOUT bit is not set in this case.
  - ACTIVE to INITIALIZE or STBY to INITIALIZE
    - if the residual voltage is detected at the end of the power-down slot-duration of the respective rail, this gates the disabling of the subsequent rail for up to eight times the slot-duration, but then the power-sequence continues regardless of the residual voltage. No bit is set in this case.
  - MASKING of RV-bits
    - the reaction of the nINT-pin reaction in case of residual voltage detection is maskable for LDOx\_RV respectively BUCKx\_RV bits by MASK\_INT\_FOR\_RV bit in MASK\_CONFIG register.
    - neither the bit nor the shutdown-fault-reaction in case of residual voltage detection is maskable for LDOx\_RV\_SD respectively BUCKx\_RV\_SD bits.
  - Timeout
    - Timeout occurs if residual voltage is not discharged in time. The bit TIMEOUT in INT\_TIMEOUT\_RV\_SD register is set. See details above.

---

#### Note

In case active discharge on a rail is disabled, the unsuccessful discharge of that rail within the slot duration does not gate the disable of the subsequent rail.

During power-down, the device sets neither RV-bits nor RV\_SD-bits for rails with disabled discharge.

---

**CAUTION**

For every detected Shut-Down fault, irrespective if prior to the sequence due to unsuccessful discharge, during the power-up-sequence or in ACTIVE or STBY state, the retry counter (RETRY\_COUNT in POWER\_UP\_STATUS\_REG register) is incremented. The device attempts two retries to power-up. If both fail, a power-cycle on VSYS is required to reset the retry counter. Any successful power-up also resets the retry counter.

If faults are masked and do not cause a shut-down, the retry counter does not increment.

To disable the retry-counter, set bit MASK\_RETRY\_COUNT in INT\_MASK\_UV register. When set, the device attempts to retry infinitely.

Below table gives an overview of the fault-behavior in ACTIVE and STBY states if unmasked and whether a fault is maskable.

**CAUTION**

Masking of faults poses a risk to the device or the system, including but not limited to starting into a pre-biased output.

TI strongly recommends not to mask OC- and UV-detection on the same rail.

**Table 7-6. Fault Handling**

| Block      | Fault  | ACTIVE or STBY state (if fault NOT masked)                                | ACTIVE or STBY state (if fault IS masked) |
|------------|--|---|---|
| BUCK & LDO | Residual voltage - shutdown-Fault - RV_SD *) | Fault triggers a sequenced shut-down to INITIALIZE state                  | Not maskable                              |
| BUCK & LDO | Residual voltage - RV                        | Fault does not trigger state-change                                       | Fault does not trigger state-change       |
| BUCK & LDO | Timeout - TO *)                              | Fault triggers a sequenced shut-down to INITIALIZE state                  | Fault does not trigger state-change       |
| BUCK & LDO | Undervoltage - UV                            | Fault triggers a sequenced shut-down to INITIALIZE state                  | Fault does not trigger state-change       |
| BUCK & LDO | Overcurrent - OC                             | Fault triggers a sequenced shut-down to INITIALIZE state                  | Not maskable                              |
| BUCK & LDO | Short-to-GND - SCG                           | Fault triggers a sequenced shut-down to INITIALIZE state                  | Not maskable                              |
| BUCK & LDO | Temperature warning - WARM                   | Fault triggers a sequenced shut-down to INITIALIZE state                  | Yes                                       |
| BUCK & LDO | Temperature shut-down - HOT                  | Fault triggers an immediate shut-down to INITIALIZE state (not sequenced) | Not maskable                              |
| VSYS       | Undervoltage - UV                            | Fault triggers an immediate shut-down to OFF state (not sequenced)        | Not maskable                              |
| VSYS       | Overvoltage - OV                             | Fault triggers an immediate shut-down to OFF state (not sequenced)        | Not maskable                              |

**Table 7-6. Fault Handling (continued)**

| Block  | Fault                                  | ACTIVE or STBY state (if fault NOT masked)                         | ACTIVE or STBY state (if fault IS masked) |
|--------|--|--|---|
| VDD1P8 | Undervoltage or Overvoltage - UV or OV | Fault triggers an immediate shut-down to OFF state (not sequenced) | Not maskable                              |

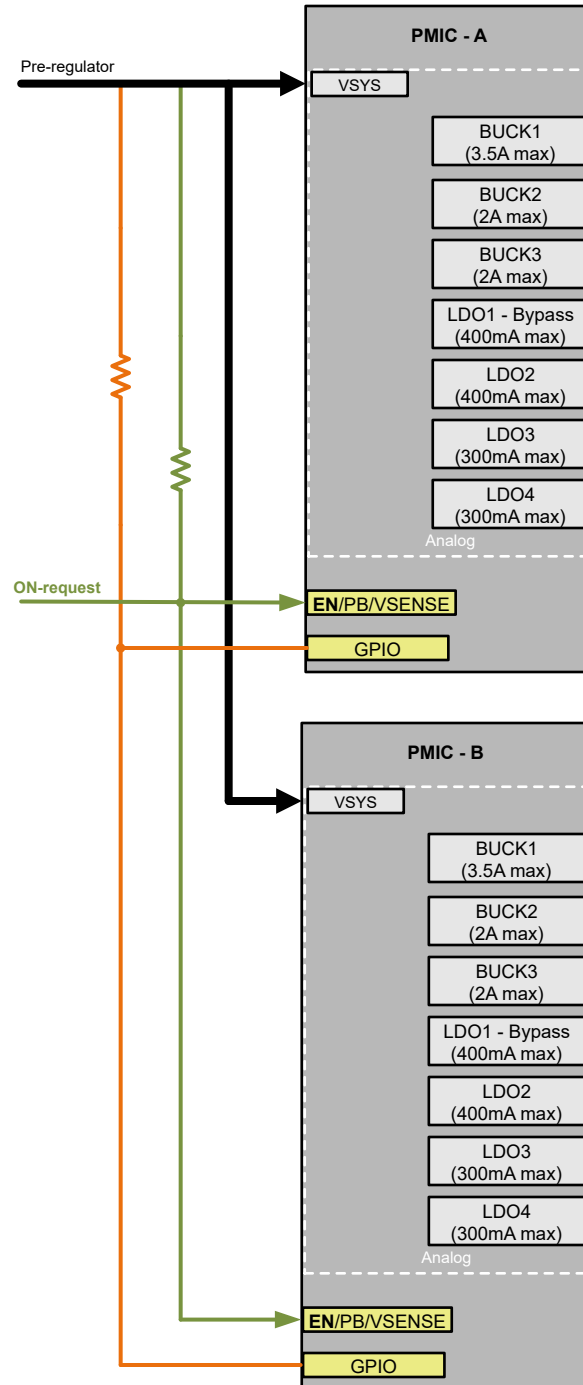
\*) RV\_SD and TIMEOUT faults only occur during a sequence

## 7.5 Multi-PMIC Operation

The GPIO (pin#16) is an input/output digital pin, however, the input-functionality is only used in multi-PMIC configuration. This pin behaves as GPO (general purpose output) when configured for single PMIC and behaves as GPIO (general purpose input-output) when configured for multi-device. Set this configuration on register field *MULTI\_DEVICE\_ENABLE* (address 0x1F). When configured for "multi-device", GPIO allows to synchronize the power-up and power-down sequence of multiple TPS65219 devices for applications requiring additional rails. The GPIO pin is used to indicate the status of each PMIC to maintain each in the same state and sequence slot. At the beginning of each sequence slot, all the TPS65219 PMICs drive GPIO pin low. After the sequence slot duration finishes, and all rails for that slot have reached the UV threshold, device releases the GPIO pin. Once both devices release the GPIO high, the internal sequencers advance to the next sequence slot together. Since both PMICs are always in the same power-up or power-down slot, multiple rails from each PMIC are synchronized to the same sequence slot. [Figure 7-11](#) shows an example PDN of two TPS65219 devices sharing the same input supply (VSYS), EN pin and GPIO for multi-PMIC operation.

### Requirements When Synchronizing Multiple TPS65219 PMICs

- The GPIO from each PMIC must be tied together, sharing the same pull-up resistor. The pull-up resistance needs to be chosen to meet the maximum allowable rise-time  $t_{RISE\_GPIO}$  in combination with the capacitance on the GPIO-line to allow for synchronization.
- The EN/PB/VSENSE pin must be tied together sharing the same external ON request. This pin must have the same configuration (same pin config, deglitch, FSD).
- All the TPS65219 PMICs must share the same VSYS supply.
- Each of the TPS65219 PMICs must have a different I2C address if connected to the same I2C bus. The I2C address for the second PMIC is changeable on register field *I2C\_ADDRESS*. Once the address is changed, the new value must be stored permanently into the NVM. Refer to NVM Programming for programming instructions.

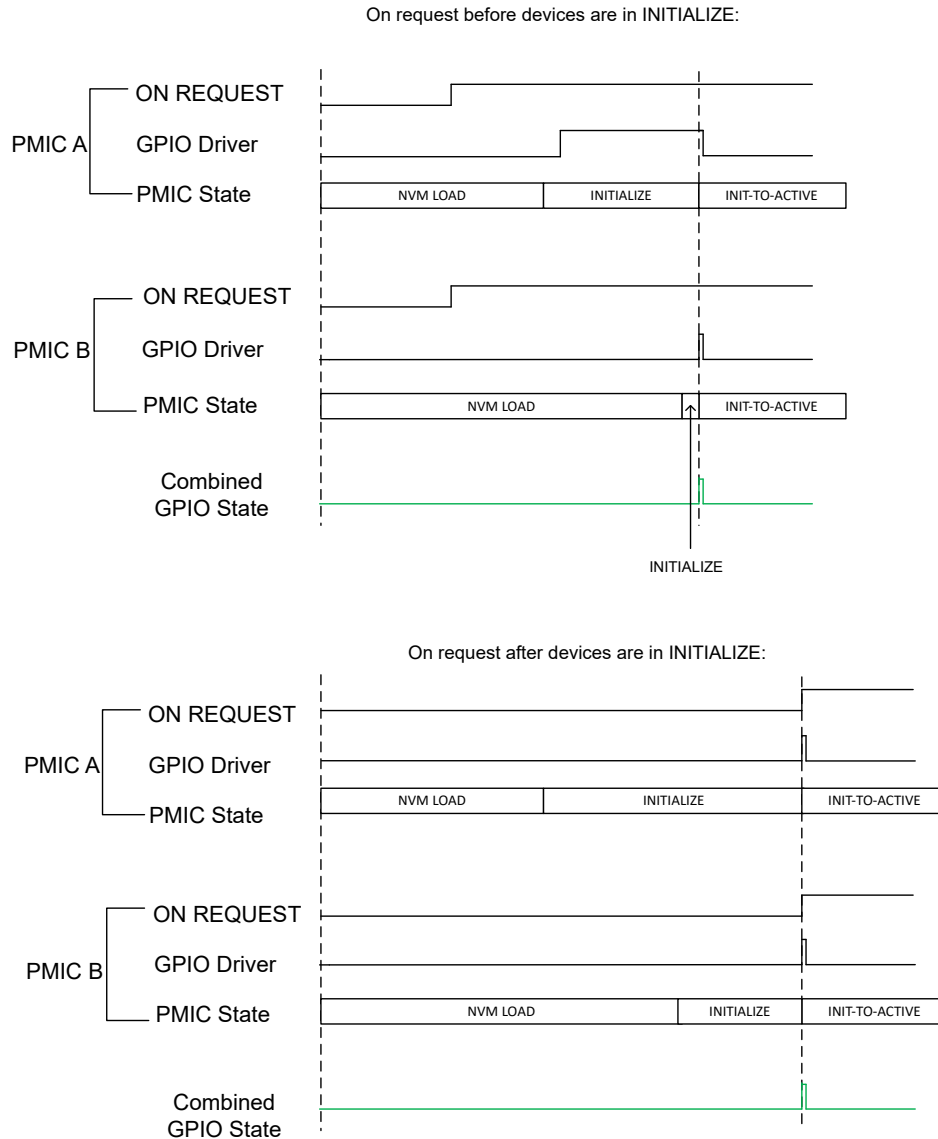


**Figure 7-11. Multi-PMIC Configuration Example**

**Note**

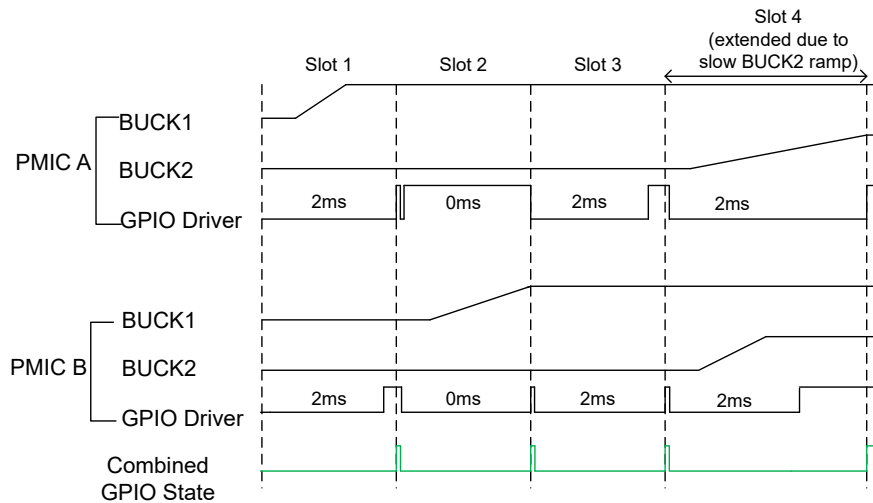
- The synchronization-times between the PMICs add to the slot-duration-timeout described in the Power-up and Power-Down sections: If power-up fails, the timeout tTIMEOUT\_UV\_SLOT occurs 3ms to 4ms later in multi-PMIC-configurations. If power-down fails due to discharge failing, the timeout occurs 20ms to 26ms later in multi-PMIC configurations.
- GPIO\_EN and GPIO\_STBY\_EN bits are ignored in multi-PMIC configuration.

Figure 7-12 shows the synchronization between two PMICs in Initialize state, before the power-up sequence is executed. While in INITIALIZE state, before the ON request is received, devices hold GPIO low. GPIO is only released when the ON request is received. The external signal driving the ON request must be connected to EN/PB/VSENSE pin of both devices. The PMICs proceed to execute the power-up sequence once both devices are in INITIALIZE state and both devices have received the ON request. This technique enables both devices start the power-up sequence at the same time, even if the respective internal boot-up times are different.



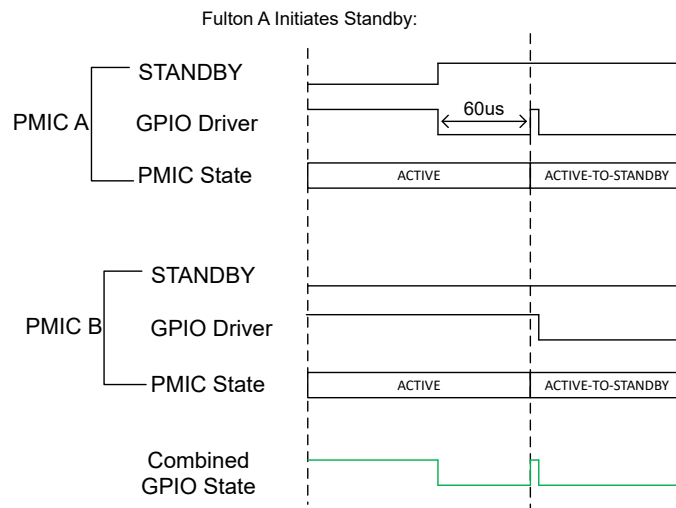
**Figure 7-12. Synchronization Before Power-up**

Figure 7-13 shows the synchronization between two PMICs during the power-up sequence. An open-drain GPIO is connected between both PMICs, and used as an indicator that the sequence slot has finished for the device. At the beginning of each sequence slot, both PMICs pull down this GPIO. After the device slot timer has expired, and all rails for that slot have reach UV threshold, the GPIO is released high. The combined GPIO goes high when both PMICs have released the GPIO. Once both devices release the GPIO high, both PMICs advance to the next sequence slot. Both PMICs are always in the same sequence slot at the same time.



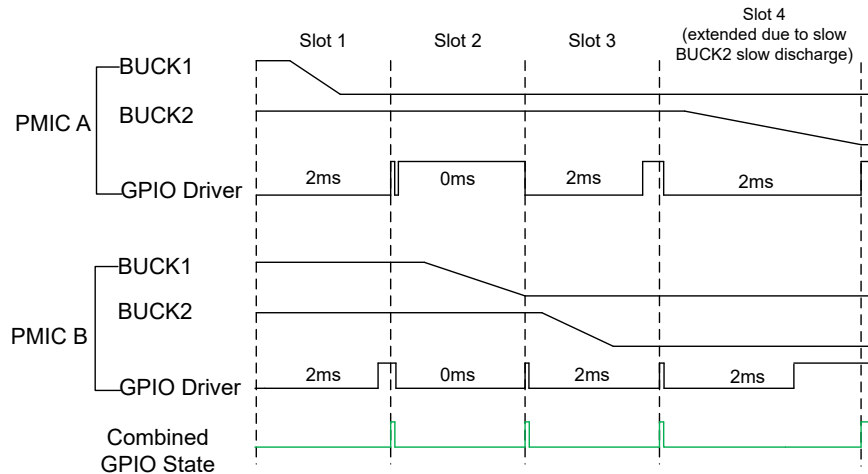
**Figure 7-13. Synchronization During Power-up Sequence**

Figure 7-14 shows the synchronization between two PMICs when transitioning from Active to Standby. In active or standby, GPIO default state is high. When a device wants to change states, GPIO is driven low for a specific low duration. The low duration determines the type of request. For STANDBY/ACTIVE request, GPIO is set low approximately 38-52us and for OFF request approximately 180-243us. Times are chosen such that devices always see the same state transition, accounting for clock variation and requests happening right after each other. While GPIO is low, devices are counting the time the GPIO remains low. On GPIO rising edge, devices start the state transition based on low duration. If GPIO stays low longer than the timeout duration, the devices indicate a GPIO fault and transition to INITIALIZE state.



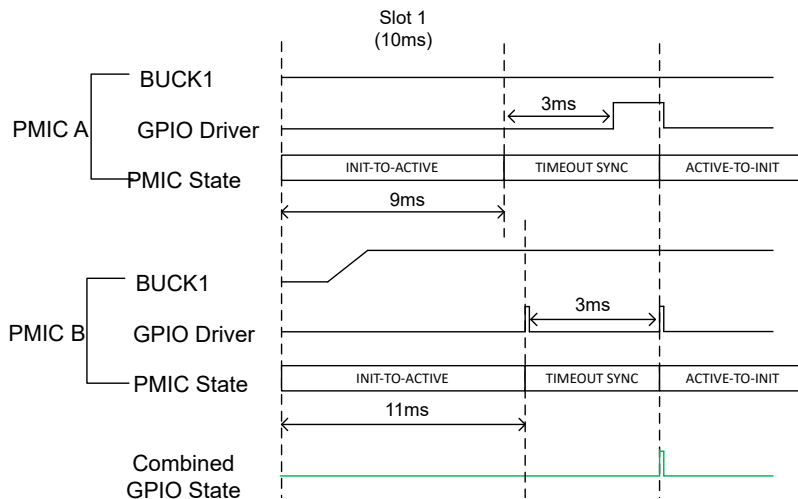
**Figure 7-14. Synchronization Before Transitioning to Standby/OFF Request/COLD RESET**

Figure 7-15 shows the synchronization between two PMICs during power-down sequence. Power-down sequence works similarly. If active discharge is enabled for a rail, the sequence slot is extended until rail is discharged below SCG threshold, unless the slot timeout occurs or register field *BYPASS\_RAILS\_DISCHARGED\_CHECK* is set. If discharge is disabled for all rails in current slot, the actual slot time is only based on selected slot duration. Once the slot duration expires and rails with active discharge are discharged, devices release the GPIO high. Once all devices release GPIO high, they advance to the next power-down step.



**Figure 7-15. Synchronization During Power-down Sequence**

Figure 7-16 shows the timeout synchronization between two PMICs. In case of a fault on an output rail, GPIO is not released. After a timeout, device goes to “timeout synchronization” state, and wait for 3ms before setting GPIO high. Once the combined GPIO goes high, both devices start the power-down sequence. For example: If BUCK1 from PMIC A is shorted to GND, after the slot duration expires, the regulator does not have hit UV and GPIO is not released. If Slot#1 duration is 10ms and PMIC A is 10% fast, it only takes 9ms to timeout. After timeout, device goes to timeout-sync state, at which point GPIO is set high after 3ms. PMIC B rails ramp up properly, but a high state on GPIO from PMIC A is initially not detected due to the fault on BUCK1. PMIC B also goes to timeout-sync state and sets GPIO high after 3ms. After the timeout sync of PMIC B, the combined GPIO is high and both PMICs start power-down together.



**Figure 7-16. Timeout Synchronization**

## 7.6 User Registers

The registers up to register 27h, USER\_GENERAL\_NVM\_STORAGE\_REG are backed up by EEPROM. The reset value corresponds to the configuration of the orderable part number and is signified by an 'X' herein. Please refer to the Technical Reference Manual (TRM) of the respective orderable part-number.

The registers 28h through 37h are not EEPROM-backed and reset to the value shown in the register map.

Registers 00h, TI\_DEV\_ID, 01h, NVM\_ID, 28h, MANUFACTURING\_VER and 41h, FACTORY\_CONFIG\_2 are hard-wired and are not changeable by the user.

## 7.7 Device Registers

Table 7-7 lists the memory-mapped registers for the Device registers. All register offset addresses not listed in Table 7-7 should be considered as reserved locations and the register contents should not be modified.

**Table 7-7. DEVICE Registers**

| Offset | Acronym                    | Register Name                             | Section            |
|--------|----------------------------|---|--------------------|
| 0h     | TI_DEV_ID                  | Device ID                                 | <a href="#">Go</a> |
| 1h     | NVM_ID                     | NVM configuration ID                      | <a href="#">Go</a> |
| 2h     | ENABLE_CTRL                | Enable/Push-Button/Vsense Control         | <a href="#">Go</a> |
| 3h     | BUCKS_CONFIG               | Generic Buck Configuration                | <a href="#">Go</a> |
| 4h     | LDO4_VOUT                  | LDO4 Configuration                        | <a href="#">Go</a> |
| 5h     | LDO3_VOUT                  | LDO3 Configuration                        | <a href="#">Go</a> |
| 6h     | LDO2_VOUT                  | LDO2 Configuration                        | <a href="#">Go</a> |
| 7h     | LDO1_VOUT                  | LDO1 Configuration                        | <a href="#">Go</a> |
| 8h     | BUCK3_VOUT                 | Buck3 Configuration                       | <a href="#">Go</a> |
| 9h     | BUCK2_VOUT                 | Buck2 Configuration                       | <a href="#">Go</a> |
| Ah     | BUCK1_VOUT                 | Buck1 Configuration                       | <a href="#">Go</a> |
| Bh     | LDO4_SEQUENCE_SLOT         | Power-up and -down slot for LDO4          | <a href="#">Go</a> |
| Ch     | LDO3_SEQUENCE_SLOT         | Power-up and -down slot for LDO3          | <a href="#">Go</a> |
| Dh     | LDO2_SEQUENCE_SLOT         | Power-up and -down slot for LDO2          | <a href="#">Go</a> |
| Eh     | LDO1_SEQUENCE_SLOT         | Power-up and -down slot for LDO10         | <a href="#">Go</a> |
| Fh     | BUCK3_SEQUENCE_SLOT        | Power-up and -down slot for Buck3         | <a href="#">Go</a> |
| 10h    | BUCK2_SEQUENCE_SLOT        | Power-up and -down slot for Buck2         | <a href="#">Go</a> |
| 11h    | BUCK1_SEQUENCE_SLOT        | Power-up and -down slot for Buck1         | <a href="#">Go</a> |
| 12h    | nRST_SEQUENCE_SLOT         | Power-up and -down slot for nRSTOUT       | <a href="#">Go</a> |
| 13h    | GPIO_SEQUENCE_SLOT         | Power-up and -down slot for GPIO          | <a href="#">Go</a> |
| 14h    | GPO2_SEQUENCE_SLOT         | Power-up and -down slot for GPO2          | <a href="#">Go</a> |
| 15h    | GPO1_SEQUENCE_SLOT         | Power-up and -down slot for GPO1          | <a href="#">Go</a> |
| 16h    | POWER_UP_SLOT_DURATION_1   | Slot-duration at power-up for slot0-3     | <a href="#">Go</a> |
| 17h    | POWER_UP_SLOT_DURATION_2   | Slot-duration at power-up for slot4-7     | <a href="#">Go</a> |
| 18h    | POWER_UP_SLOT_DURATION_3   | Slot-duration at power-up for slot8-11    | <a href="#">Go</a> |
| 19h    | POWER_UP_SLOT_DURATION_4   | Slot-duration at power-up for slot12-15   | <a href="#">Go</a> |
| 1Ah    | POWER_DOWN_SLOT_DURATION_1 | Slot-duration at power-down for slot0-3   | <a href="#">Go</a> |
| 1Bh    | POWER_DOWN_SLOT_DURATION_2 | Slot-duration at power-down for slot4-7   | <a href="#">Go</a> |
| 1Ch    | POWER_DOWN_SLOT_DURATION_3 | Slot-duration at power-down for slot8-11  | <a href="#">Go</a> |
| 1Dh    | POWER_DOWN_SLOT_DURATION_4 | Slot-duration at power-down for slot12-15 | <a href="#">Go</a> |
| 1Eh    | GENERAL_CONFIG             | LDO-undervoltage and GPO-enable           | <a href="#">Go</a> |
| 1Fh    | MFP_1_CONFIG               | Multi-Function pin configuration1         | <a href="#">Go</a> |
| 20h    | MFP_2_CONFIG               | Multi-Function pin configuration2         | <a href="#">Go</a> |
| 21h    | STBY_1_CONFIG              | STBY configuration LDOs and Bucks         | <a href="#">Go</a> |
| 22h    | STBY_2_CONFIG              | STBY configuration GPIO and GPO           | <a href="#">Go</a> |
| 23h    | OC_DEGL_CONFIG             | Overcurrent deglitch time per rail        | <a href="#">Go</a> |

**Table 7-7. DEVICE Registers (continued)**

| Offset | Acronym                      | Register Name                                    | Section            |
|--------|------------------------------|--|--------------------|
| 24h    | INT_MASK_UV                  | Undervoltage fault-masking                       | <a href="#">Go</a> |
| 25h    | MASK_CONFIG                  | WARM-masking and mask-effect                     | <a href="#">Go</a> |
| 26h    | I2C_ADDRESS_REG              | I2C-address                                      | <a href="#">Go</a> |
| 27h    | USER_GENERAL_NVM_STORAGE_REG | User-configurable register (NVM-backed)          | <a href="#">Go</a> |
| 28h    | MANUFACTURING_VER            | Silicon-revision (read-only)                     | <a href="#">Go</a> |
| 29h    | MFP_CTRL                     | I2C-control for RESET, STBY, OFF                 | <a href="#">Go</a> |
| 2Ah    | DISCHARGE_CONFIG             | Discharge configuration per rail                 | <a href="#">Go</a> |
| 2Bh    | INT_SOURCE                   | Interrupt source                                 | <a href="#">Go</a> |
| 2Ch    | INT_LDO_3_4                  | OC, UV, SCG for LDO3 and LDO4                    | <a href="#">Go</a> |
| 2Dh    | INT_LDO_1_2                  | OC, UV, SCG for LDO1 and LDO2                    | <a href="#">Go</a> |
| 2Eh    | INT_BUCK_3                   | OC, UV, SCG for Buck3                            | <a href="#">Go</a> |
| 2Fh    | INT_BUCK_1_2                 | OC, UV, SCG for Buck1 and Buck2                  | <a href="#">Go</a> |
| 30h    | INT_SYSTEM                   | WARM and HOT fault flags                         | <a href="#">Go</a> |
| 31h    | INT_RV                       | RV (residual voltage) per rail                   | <a href="#">Go</a> |
| 32h    | INT_TIMEOUT_RV_SD            | RV (residual voltage) per rail causing shut-down | <a href="#">Go</a> |
| 33h    | INT_PB                       | PushButton status and edge-detection             | <a href="#">Go</a> |
| 34h    | USER_NVM_CMD_REG             | DIY - user programming commands                  | <a href="#">Go</a> |
| 35h    | POWER_UP_STATUS_REG          | Power-up status and STATE                        | <a href="#">Go</a> |
| 36h    | SPARE_2                      | Spare register (not NVM-backed)                  | <a href="#">Go</a> |
| 37h    | SPARE_3                      | Spare register (not NVM-backed)                  | <a href="#">Go</a> |
| 41h    | FACTORY_CONFIG_2             | Revision of NVM-configuration (read only)        | <a href="#">Go</a> |

Complex bit access types are encoded to fit into small table cells. [Table 7-8](#) shows the codes that are used for access types in this section.

**Table 7-8. Device Access Type Codes**

| Access Type                   | Code    | Description                            |
|-------------------------------|---------|--|
| <b>Read Type</b>              |         |  |
| R                             | R       | Read                                   |
| <b>Write Type</b>             |         |  |
| W                             | W       | Write                                  |
| W1C                           | W<br>1C | Write<br>1 to clear                    |
| WSelfClrF                     | W       | Write                                  |
| <b>Reset or Default Value</b> |         |  |
| -n                            |         | Value after reset or the default value |

**7.7.1 TI\_DEV\_ID Register (Offset = 0h) [Reset = X]**

TI\_DEV\_ID is shown in [Figure 7-17](#) and described in [Table 7-9](#).

Return to the [Summary Table](#).

**Figure 7-17. TI\_DEV\_ID Register**

|              |   |   |   |   |   |   |   |
|--------------|---|---|---|---|---|---|---|
| 7            | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| TI_DEVICE_ID |   |   |   |   |   |   |   |
| R-X          |   |   |   |   |   |   |   |

**Table 7-9. TI\_DEV\_ID Register Field Descriptions**

| Bit | Field        | Type | Reset | Description   |
|-----|--------------|------|-------|---|
| 7-0 | TI_DEVICE_ID | R    | X     | TI_DEVICE_ID[7:6]:<br>0h = TA: -40°C to 105°C, TJ: -40°C to 125°C<br>2h = TA: -40°C to 125°C, TJ: -40°C to 150°C<br>3h = TA: -55°C to 125°C, TJ: -55°C to 150°C<br>TI_DEVICE_ID[5:0]:<br>Device GPN<br>Note: This register can be programmed only by the manufacturer!<br>Refer to Technical Reference Manual / User's Guide for specific numbering and associated configuration. (Default from NVM memory) |

### 7.7.2 NVM\_ID Register (Offset = 1h) [Reset = X]

NVM\_ID is shown in [Figure 7-18](#) and described in [Table 7-10](#).

Return to the [Summary Table](#).

**Figure 7-18. NVM\_ID Register**

|           |   |   |   |   |   |   |   |
|-----------|---|---|---|---|---|---|---|
| 7         | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| TI_NVM_ID |   |   |   |   |   |   |   |
| R-X       |   |   |   |   |   |   |   |

**Table 7-10. NVM\_ID Register Field Descriptions**

| Bit | Field     | Type | Reset | Description  |
|-----|-----------|------|-------|--|
| 7-0 | TI_NVM_ID | R    | X     | NVM ID of the IC Note: This register can be programmed only by the manufacturer! Refer to Technical Reference Manual / User's Guide for specific numbering and associated configuration. (Default from NVM memory) |

### 7.7.3 ENABLE\_CTRL Register (Offset = 2h) [Reset = X]

ENABLE\_CTRL is shown in [Figure 7-19](#) and described in [Table 7-11](#).

Return to the [Summary Table](#).

**Figure 7-19. ENABLE\_CTRL Register**

| 7        | 6       | 5       | 4       | 3       | 2        | 1        | 0        |
|----------|---------|---------|---------|---------|----------|----------|----------|
| RESERVED | LDO4_EN | LDO3_EN | LDO2_EN | LDO1_EN | BUCK3_EN | BUCK2_EN | BUCK1_EN |
| R-X      | R/W-X   | R/W-X   | R/W-X   | R/W-X   | R/W-X    | R/W-X    | R/W-X    |

**Table 7-11. ENABLE\_CTRL Register Field Descriptions**

| Bit | Field    | Type | Reset | Description   |
|-----|----------|------|-------|---|
| 7   | RESERVED | R    | X     | Reserved  |
| 6   | LDO4_EN  | R/W  | X     | Enable LDO4 regulator (Default from NVM memory)<br>0h = Disabled<br>1h = Enabled  |
| 5   | LDO3_EN  | R/W  | X     | Enable LDO3 regulator (Default from NVM memory)<br>0h = Disabled<br>1h = Enabled  |
| 4   | LDO2_EN  | R/W  | X     | Enable LDO2 regulator (Default from NVM memory)<br>0h = Disabled<br>1h = Enabled  |
| 3   | LDO1_EN  | R/W  | X     | Enable LDO1 regulator (Default from NVM memory)<br>0h = Disabled<br>1h = Enabled  |
| 2   | BUCK3_EN | R/W  | X     | Enable BUCK3 regulator (Default from NVM memory)<br>0h = Disabled<br>1h = Enabled |
| 1   | BUCK2_EN | R/W  | X     | Enable BUCK2 regulator (Default from NVM memory)<br>0h = Disabled<br>1h = Enabled |
| 0   | BUCK1_EN | R/W  | X     | Enable BUCK1 regulator (Default from NVM memory)<br>0h = Disabled<br>1h = Enabled |

### 7.7.4 BUCKS\_CONFIG Register (Offset = 3h) [Reset = X]

BUCKS\_CONFIG is shown in [Figure 7-20](#) and described in [Table 7-12](#).

Return to the [Summary Table](#).

**Figure 7-20. BUCKS\_CONFIG Register**

| 7                | 6                | 5              | 4              | 3                  | 2 | 1                  | 0 |
|------------------|------------------|----------------|----------------|--------------------|---|--------------------|---|
| USER_NVM_SPARE_2 | USER_NVM_SPARE_1 | BUCK_SS_ENABLE | BUCK_FF_ENABLE | BUCK3_PHASE_CONFIG |   | BUCK2_PHASE_CONFIG |   |
| R/W-X            | R/W-X            | R/W-X          | R/W-X          | R/W-X              |   | R/W-X              |   |

**Table 7-12. BUCKS\_CONFIG Register Field Descriptions**

| Bit | Field              | Type | Reset | Description  |
|-----|--------------------|------|-------|--|
| 7   | USER_NVM_SPARE_2   | R/W  | X     | Spare bit in user NVM space (Default from NVM memory)  |
| 6   | USER_NVM_SPARE_1   | R/W  | X     | Spare bit in user NVM space (Default from NVM memory)  |
| 5   | BUCK_SS_ENABLE     | R/W  | X     | Spread spectrum enabled on Bucks (only applicable in FF-mode) (Default from NVM memory)<br>0h = Spread spectrum disabled<br>1h = Spread spectrum enabled   |
| 4   | BUCK_FF_ENABLE     | R    | X     | All Bucks set into fixed frequency mode NOTE: MUST NOT CHANGE AT ANY TIME! (Default from NVM memory)<br>0h = Quasi-fixed frequency mode<br>1h = Fixed frequency mode   |
| 3-2 | BUCK3_PHASE_CONFIG | R/W  | X     | Phase of BUCK3 clock. Applicable if Bucks are configured for fixed frequency. NOTE: ONLY CHANGE WHILE RAIL IS DISABLED! (Default from NVM memory)<br>0h = 0 degrees<br>1h = 90 degrees<br>2h = 180 degrees<br>3h = 270 degrees |
| 1-0 | BUCK2_PHASE_CONFIG | R/W  | X     | Phase of BUCK2 clock. Applicable if Bucks are configured for fixed frequency. NOTE: ONLY CHANGE WHILE RAIL IS DISABLED! (Default from NVM memory)<br>0h = 0 degrees<br>1h = 90 degrees<br>2h = 180 degrees<br>3h = 270 degrees |

### 7.7.5 LDO4\_VOUT Register (Offset = 4h) [Reset = X]

LDO4\_VOUT is shown in [Figure 7-21](#) and described in [Table 7-13](#).

Return to the [Summary Table](#).

**Figure 7-21. LDO4\_VOUT Register**

|                   |                 |           |   |   |   |   |   |
|-------------------|-----------------|-----------|---|---|---|---|---|
| 7                 | 6               | 5         | 4 | 3 | 2 | 1 | 0 |
| LDO4_SLOW_PU_RAMP | LDO4_LSW_CONFIG | LDO4_VSET |   |   |   |   |   |
| R/W-X             | R/W-X           | R/W-X     |   |   |   |   |   |

**Table 7-13. LDO4\_VOUT Register Field Descriptions**

| Bit | Field             | Type | Reset | Description  |
|-----|-------------------|------|-------|--|
| 7   | LDO4_SLOW_PU_RAMP | R/W  | X     | LDO4 Power-up ramp When set high, slows down the power-up ramp to ~3ms. Cout max 30uF When set low, ramp time is ~660us. Cout max 15uF (Default from NVM memory)<br>0h = Fast ramp for power-up (~660us)<br>1h = Slow ramp for power-up (~3ms) |
| 6   | LDO4_LSW_CONFIG   | R/W  | X     | LDO4 LDO or LSW Mode. NOTE: ONLY CHANGE WHILE RAIL IS DISABLED! (Default from NVM memory)<br>0h = LDO Mode<br>1h = LSW Mode  |

**Table 7-13. LDO4\_VOUT Register Field Descriptions (continued)**

| Bit | Field     | Type | Reset | Description  |
|-----|-----------|------|-------|--|
| 5-0 | LDO4_VSET | R/W  | X     | Voltage selection for LDO4. The output voltage range is from 1.2V to 3.3V. (Default from NVM memory)<br>0h = 1.200V<br>1h = 1.200V<br>2h = 1.200V<br>3h = 1.200V<br>4h = 1.200V<br>5h = 1.200V<br>6h = 1.200V<br>7h = 1.200V<br>8h = 1.200V<br>9h = 1.200V<br>Ah = 1.200V<br>Bh = 1.200V<br>Ch = 1.200V<br>Dh = 1.250V<br>Eh = 1.300V<br>Fh = 1.350V<br>10h = 1.400V<br>11h = 1.450V<br>12h = 1.500V<br>13h = 1.550V<br>14h = 1.600V<br>15h = 1.650V<br>16h = 1.700V<br>17h = 1.750V<br>18h = 1.800V<br>19h = 1.850V<br>1Ah = 1.900V<br>1Bh = 1.950V<br>1Ch = 2.000V<br>1Dh = 2.050V<br>1Eh = 2.100V<br>1Fh = 2.150V<br>20h = 2.200V<br>21h = 2.250V<br>22h = 2.300V<br>23h = 2.350V<br>24h = 2.400V<br>25h = 2.450V<br>26h = 2.500V<br>27h = 2.550V<br>28h = 2.600V<br>29h = 2.650V<br>2Ah = 2.700V<br>2Bh = 2.750V<br>2Ch = 2.800V<br>2Dh = 2.850V<br>2Eh = 2.900V<br>2Fh = 2.950V<br>30h = 3.000V<br>31h = 3.050V<br>32h = 3.100V<br>33h = 3.150V<br>34h = 3.200V<br>35h = 3.250V<br>36h = 3.300V<br>37h = 3.300V<br>38h = 3.300V<br>39h = 3.300V<br>3Ah = 3.300V<br>3Bh = 3.300V<br>3Ch = 3.300V<br>3Dh = 3.300V<br>3Eh = 3.300V |

**Table 7-13. LDO4\_VOUT Register Field Descriptions (continued)**

| Bit | Field | Type | Reset | Description  |
|-----|-------|------|-------|--------------|
|     |       |      |       | 3Fh = 3.300V |

### 7.7.6 LDO3\_VOUT Register (Offset = 5h) [Reset = X]

LDO3\_VOUT is shown in [Figure 7-22](#) and described in [Table 7-14](#).

Return to the [Summary Table](#).

**Figure 7-22. LDO3\_VOUT Register**

|                   |                 |           |   |   |   |   |   |
|-------------------|-----------------|-----------|---|---|---|---|---|
| 7                 | 6               | 5         | 4 | 3 | 2 | 1 | 0 |
| LDO3_SLOW_PU_RAMP | LDO3_LSW_CONFIG | LDO3_VSET |   |   |   |   |   |
| R/W-X             | R/W-X           | R/W-X     |   |   |   |   |   |

**Table 7-14. LDO3\_VOUT Register Field Descriptions**

| Bit | Field             | Type | Reset | Description  |
|-----|-------------------|------|-------|--|
| 7   | LDO3_SLOW_PU_RAMP | R/W  | X     | LDO3 Power-up ramp When set high, slows down the power-up ramp to ~3ms. Cout max 30uF When set low, ramp time is ~660us. Cout max 15uF (Default from NVM memory)<br>0h = Fast ramp for power-up (~660us)<br>1h = Slow ramp for power-up (~3ms) |
| 6   | LDO3_LSW_CONFIG   | R/W  | X     | LDO3 LDO or LSW Mode. NOTE: ONLY CHANGE WHILE RAIL IS DISABLED! (Default from NVM memory)<br>0h = LDO Mode<br>1h = LSW Mode  |

**Table 7-14. LDO3\_VOUT Register Field Descriptions (continued)**

| Bit | Field     | Type | Reset | Description  |
|-----|-----------|------|-------|--|
| 5-0 | LDO3_VSET | R/W  | X     | Voltage selection for LDO3. The output voltage range is from 1.2V to 3.3V. (Default from NVM memory)<br>0h = 1.200V<br>1h = 1.200V<br>2h = 1.200V<br>3h = 1.200V<br>4h = 1.200V<br>5h = 1.200V<br>6h = 1.200V<br>7h = 1.200V<br>8h = 1.200V<br>9h = 1.200V<br>Ah = 1.200V<br>Bh = 1.200V<br>Ch = 1.200V<br>Dh = 1.250V<br>Eh = 1.300V<br>Fh = 1.350V<br>10h = 1.400V<br>11h = 1.450V<br>12h = 1.500V<br>13h = 1.550V<br>14h = 1.600V<br>15h = 1.650V<br>16h = 1.700V<br>17h = 1.750V<br>18h = 1.800V<br>19h = 1.850V<br>1Ah = 1.900V<br>1Bh = 1.950V<br>1Ch = 2.000V<br>1Dh = 2.050V<br>1Eh = 2.100V<br>1Fh = 2.150V<br>20h = 2.200V<br>21h = 2.250V<br>22h = 2.300V<br>23h = 2.350V<br>24h = 2.400V<br>25h = 2.450V<br>26h = 2.500V<br>27h = 2.550V<br>28h = 2.600V<br>29h = 2.650V<br>2Ah = 2.700V<br>2Bh = 2.750V<br>2Ch = 2.800V<br>2Dh = 2.850V<br>2Eh = 2.900V<br>2Fh = 2.950V<br>30h = 3.000V<br>31h = 3.050V<br>32h = 3.100V<br>33h = 3.150V<br>34h = 3.200V<br>35h = 3.250V<br>36h = 3.300V<br>37h = 3.300V<br>38h = 3.300V<br>39h = 3.300V<br>3Ah = 3.300V<br>3Bh = 3.300V<br>3Ch = 3.300V<br>3Dh = 3.300V<br>3Eh = 3.300V |

**Table 7-14. LDO3\_VOUT Register Field Descriptions (continued)**

| Bit | Field | Type | Reset | Description  |
|-----|-------|------|-------|--------------|
|     |       |      |       | 3Fh = 3.300V |

### 7.7.7 LDO2\_VOUT Register (Offset = 6h) [Reset = X]

LDO2\_VOUT is shown in [Figure 7-23](#) and described in [Table 7-15](#).

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**Figure 7-23. LDO2\_VOUT Register**

|                     |                     |           |   |   |   |   |   |
|---------------------|---------------------|-----------|---|---|---|---|---|
| 7                   | 6                   | 5         | 4 | 3 | 2 | 1 | 0 |
| LDO2_LSW_C<br>ONFIG | LDO2_BYP_CO<br>NFIG | LDO2_VSET |   |   |   |   |   |
| R/W-X               | R/W-X               | R/W-X     |   |   |   |   |   |

**Table 7-15. LDO2\_VOUT Register Field Descriptions**

| Bit | Field           | Type | Reset | Description   |
|-----|-----------------|------|-------|---|
| 7   | LDO2_LSW_CONFIG | R/W  | X     | LDO2 LDO/Bypass or LSW Mode. NOTE: ONLY CHANGE WHILE RAIL IS DISABLED! (Default from NVM memory)<br>0h = Not Applicable (LDO2 not configured as load-switch)<br>1h = LDO1 configured as Load-switch   |
| 6   | LDO2_BYP_CONFIG | R/W  | X     | LDO2 LDO or Bypass Mode. (Default from NVM memory)<br>0h = LDO2 configured as LDO (only applicable if LDO2_LSW_CONFIG 0x0)<br>1h = LDO2 configured as Bypass (only applicable if LDO2_LSW_CONFIG 0x0) |

**Table 7-15. LDO2\_VOUT Register Field Descriptions (continued)**

| Bit | Field     | Type | Reset | Description   |
|-----|-----------|------|-------|---|
| 5-0 | LDO2_VSET | R/W  | X     | <p>Voltage selection for LDO2. The output voltage range is from 0.6V to 3.4V in LDO mode and 1.5V to 3.4V in bypass-mode. (Default from NVM memory)</p> <p>0h = 0.600V<br/>           1h = 0.650V<br/>           2h = 0.700V<br/>           3h = 0.750V<br/>           4h = 0.800V<br/>           5h = 0.850V<br/>           6h = 0.900V<br/>           7h = 0.950V<br/>           8h = 1.000V<br/>           9h = 1.050V<br/>           Ah = 1.100V<br/>           Bh = 1.150V<br/>           Ch = 1.200V<br/>           Dh = 1.250V<br/>           Eh = 1.300V<br/>           Fh = 1.350V<br/>           10h = 1.400V<br/>           11h = 1.450V<br/>           12h = 1.500V<br/>           13h = 1.550V<br/>           14h = 1.600V<br/>           15h = 1.650V<br/>           16h = 1.700V<br/>           17h = 1.750V<br/>           18h = 1.800V<br/>           19h = 1.850V<br/>           1Ah = 1.900V<br/>           1Bh = 1.950V<br/>           1Ch = 2.000V<br/>           1Dh = 2.050V<br/>           1Eh = 2.100V<br/>           1Fh = 2.150V<br/>           20h = 2.200V<br/>           21h = 2.250V<br/>           22h = 2.300V<br/>           23h = 2.350V<br/>           24h = 2.400V<br/>           25h = 2.450V<br/>           26h = 2.500V<br/>           27h = 2.550V<br/>           28h = 2.600V<br/>           29h = 2.650V<br/>           2Ah = 2.700V<br/>           2Bh = 2.750V<br/>           2Ch = 2.800V<br/>           2Dh = 2.850V<br/>           2Eh = 2.900V<br/>           2Fh = 2.950V<br/>           30h = 3.000V<br/>           31h = 3.050V<br/>           32h = 3.100V<br/>           33h = 3.150V<br/>           34h = 3.200V<br/>           35h = 3.250V<br/>           36h = 3.300V<br/>           37h = 3.350V<br/>           38h = 3.400V<br/>           39h = 3.400V<br/>           3Ah = 3.400V<br/>           3Bh = 3.400V<br/>           3Ch = 3.400V<br/>           3Dh = 3.400V</p> |

**Table 7-15. LDO2\_VOUT Register Field Descriptions (continued)**

| Bit | Field | Type | Reset | Description                  |
|-----|-------|------|-------|------------------------------|
|     |       |      |       | 3Eh = 3.400V<br>3Fh = 3.400V |

### 7.7.8 LDO1\_VOUT Register (Offset = 7h) [Reset = X]

LDO1\_VOUT is shown in [Figure 7-24](#) and described in [Table 7-16](#).

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**Figure 7-24. LDO1\_VOUT Register**

|                 |                 |           |          |          |          |          |          |
|-----------------|-----------------|-----------|----------|----------|----------|----------|----------|
| <b>7</b>        | <b>6</b>        | <b>5</b>  | <b>4</b> | <b>3</b> | <b>2</b> | <b>1</b> | <b>0</b> |
| LDO1_LSW_CONFIG | LDO1_BYP_CONFIG | LDO1_VSET |          |          |          |          |          |
| R/W-X           | R/W-X           | R/W-X     |          |          |          |          |          |

**Table 7-16. LDO1\_VOUT Register Field Descriptions**

| Bit | Field           | Type | Reset | Description   |
|-----|-----------------|------|-------|---|
| 7   | LDO1_LSW_CONFIG | R/W  | X     | LDO1 LDO/Bypass or LSW Mode. NOTE: ONLY CHANGE WHILE RAIL IS DISABLED! (Default from NVM memory)<br>0h = Not Applicable (LDO1 not configured as load-switch)<br>1h = LDO1 configured as Load-switch   |
| 6   | LDO1_BYP_CONFIG | R/W  | X     | LDO1 LDO or Bypass Mode. (Default from NVM memory)<br>0h = LDO1 configured as LDO (only applicable if LDO1_LSW_CONFIG 0x0)<br>1h = LDO1 configured as Bypass (only applicable if LDO1_LSW_CONFIG 0x0) |

**Table 7-16. LDO1\_VOUT Register Field Descriptions (continued)**

| Bit | Field     | Type | Reset | Description  |
|-----|-----------|------|-------|--|
| 5-0 | LDO1_VSET | R/W  | X     | Voltage selection for LDO1. The output voltage range is from 0.6V to 3.4V in LDO-mode and 1.5V to 3.4V in bypass-mode. (Default from NVM memory)<br>0h = 0.600V<br>1h = 0.650V<br>2h = 0.700V<br>3h = 0.750V<br>4h = 0.800V<br>5h = 0.850V<br>6h = 0.900V<br>7h = 0.950V<br>8h = 1.000V<br>9h = 1.050V<br>Ah = 1.100V<br>Bh = 1.150V<br>Ch = 1.200V<br>Dh = 1.250V<br>Eh = 1.300V<br>Fh = 1.350V<br>10h = 1.400V<br>11h = 1.450V<br>12h = 1.500V<br>13h = 1.550V<br>14h = 1.600V<br>15h = 1.650V<br>16h = 1.700V<br>17h = 1.750V<br>18h = 1.800V<br>19h = 1.850V<br>1Ah = 1.900V<br>1Bh = 1.950V<br>1Ch = 2.000V<br>1Dh = 2.050V<br>1Eh = 2.100V<br>1Fh = 2.150V<br>20h = 2.200V<br>21h = 2.250V<br>22h = 2.300V<br>23h = 2.350V<br>24h = 2.400V<br>25h = 2.450V<br>26h = 2.500V<br>27h = 2.550V<br>28h = 2.600V<br>29h = 2.650V<br>2Ah = 2.700V<br>2Bh = 2.750V<br>2Ch = 2.800V<br>2Dh = 2.850V<br>2Eh = 2.900V<br>2Fh = 2.950V<br>30h = 3.000V<br>31h = 3.050V<br>32h = 3.100V<br>33h = 3.150V<br>34h = 3.200V<br>35h = 3.250V<br>36h = 3.300V<br>37h = 3.350V<br>38h = 3.400V<br>39h = 3.400V<br>3Ah = 3.400V<br>3Bh = 3.400V<br>3Ch = 3.400V<br>3Dh = 3.400V |

**Table 7-16. LDO1\_VOUT Register Field Descriptions (continued)**

| Bit | Field | Type | Reset | Description                  |
|-----|-------|------|-------|------------------------------|
|     |       |      |       | 3Eh = 3.400V<br>3Fh = 3.400V |

### 7.7.9 BUCK3\_VOUT Register (Offset = 8h) [Reset = X]

BUCK3\_VOUT is shown in [Figure 7-25](#) and described in [Table 7-17](#).

Return to the [Summary Table](#).

**Figure 7-25. BUCK3\_VOUT Register**

|                  |                      |            |   |   |   |   |   |
|------------------|----------------------|------------|---|---|---|---|---|
| 7                | 6                    | 5          | 4 | 3 | 2 | 1 | 0 |
| BUCK3_BW_S<br>EL | BUCK3_UV_TH<br>R_SEL | BUCK3_VSET |   |   |   |   |   |
| R/W-X            | R/W-X                | R/W-X      |   |   |   |   |   |

**Table 7-17. BUCK3\_VOUT Register Field Descriptions**

| Bit | Field            | Type | Reset | Description   |
|-----|------------------|------|-------|---|
| 7   | BUCK3_BW_SEL     | R/W  | X     | BUCK3 Bandwidth selection. NOTE: ONLY CHANGE WHILE RAIL IS DISABLED! (Default from NVM memory)<br>0h = low bandwidth<br>1h = high bandwidth |
| 6   | BUCK3_UV_THR_SEL | R/W  | X     | UV threshold selection for BUCK3. (Default from NVM memory)<br>0h = -5% UV detection<br>1h = -10% UV detection                              |

**Table 7-17. BUCK3\_VOUT Register Field Descriptions (continued)**

| Bit | Field      | Type | Reset | Description   |
|-----|------------|------|-------|---|
| 5-0 | BUCK3_VSET | R/W  | X     | Voltage selection for BUCK3. The output voltage range is from 0.6V to 3.4V. (Default from NVM memory)<br>0h = 0.600V<br>1h = 0.625V<br>2h = 0.650V<br>3h = 0.675V<br>4h = 0.700V<br>5h = 0.725V<br>6h = 0.750V<br>7h = 0.775V<br>8h = 0.800V<br>9h = 0.825V<br>Ah = 0.850V<br>Bh = 0.875V<br>Ch = 0.900V<br>Dh = 0.925V<br>Eh = 0.950V<br>Fh = 0.975V<br>10h = 1.000V<br>11h = 1.025V<br>12h = 1.050V<br>13h = 1.075V<br>14h = 1.100V<br>15h = 1.125V<br>16h = 1.150V<br>17h = 1.175V<br>18h = 1.200V<br>19h = 1.225V<br>1Ah = 1.250V<br>1Bh = 1.275V<br>1Ch = 1.300V<br>1Dh = 1.325V<br>1Eh = 1.350V<br>1Fh = 1.375V<br>20h = 1.400V<br>21h = 1.500V<br>22h = 1.600V<br>23h = 1.700V<br>24h = 1.800V<br>25h = 1.900V<br>26h = 2.000V<br>27h = 2.100V<br>28h = 2.200V<br>29h = 2.300V<br>2Ah = 2.400V<br>2Bh = 2.500V<br>2Ch = 2.600V<br>2Dh = 2.700V<br>2Eh = 2.800V<br>2Fh = 2.900V<br>30h = 3.000V<br>31h = 3.100V<br>32h = 3.200V<br>33h = 3.300V<br>34h = 3.400V<br>35h = 3.400V<br>36h = 3.400V<br>37h = 3.400V<br>38h = 3.400V<br>39h = 3.400V<br>3Ah = 3.400V<br>3Bh = 3.400V<br>3Ch = 3.400V<br>3Dh = 3.400V<br>3Eh = 3.400V |

**Table 7-17. BUCK3\_VOUT Register Field Descriptions (continued)**

| Bit | Field | Type | Reset | Description  |
|-----|-------|------|-------|--------------|
|     |       |      |       | 3Fh = 3.400V |

### 7.7.10 BUCK2\_VOUT Register (Offset = 9h) [Reset = X]

BUCK2\_VOUT is shown in [Figure 7-26](#) and described in [Table 7-18](#).

Return to the [Summary Table](#).

**Figure 7-26. BUCK2\_VOUT Register**

|                  |                      |            |   |   |   |   |   |
|------------------|----------------------|------------|---|---|---|---|---|
| 7                | 6                    | 5          | 4 | 3 | 2 | 1 | 0 |
| BUCK2_BW_S<br>EL | BUCK2_UV_TH<br>R_SEL | BUCK2_VSET |   |   |   |   |   |
| R/W-X            | R/W-X                | R/W-X      |   |   |   |   |   |

**Table 7-18. BUCK2\_VOUT Register Field Descriptions**

| Bit | Field            | Type | Reset | Description   |
|-----|------------------|------|-------|---|
| 7   | BUCK2_BW_SEL     | R/W  | X     | BUCK2 Bandwidth selection. NOTE: ONLY CHANGE WHILE RAIL IS DISABLED! (Default from NVM memory)<br>0h = low bandwidth<br>1h = high bandwidth |
| 6   | BUCK2_UV_THR_SEL | R/W  | X     | UV threshold selection for BUCK2. (Default from NVM memory)<br>0h = -5% UV detection<br>1h = -10% UV detection                              |

**Table 7-18. BUCK2\_VOUT Register Field Descriptions (continued)**

| Bit | Field      | Type | Reset | Description   |
|-----|------------|------|-------|---|
| 5-0 | BUCK2_VSET | R/W  | X     | Voltage selection for BUCK2. The output voltage range is from 0.6V to 3.4V. (Default from NVM memory)<br>0h = 0.600V<br>1h = 0.625V<br>2h = 0.650V<br>3h = 0.675V<br>4h = 0.700V<br>5h = 0.725V<br>6h = 0.750V<br>7h = 0.775V<br>8h = 0.800V<br>9h = 0.825V<br>Ah = 0.850V<br>Bh = 0.875V<br>Ch = 0.900V<br>Dh = 0.925V<br>Eh = 0.950V<br>Fh = 0.975V<br>10h = 1.000V<br>11h = 1.025V<br>12h = 1.050V<br>13h = 1.075V<br>14h = 1.100V<br>15h = 1.125V<br>16h = 1.150V<br>17h = 1.175V<br>18h = 1.200V<br>19h = 1.225V<br>1Ah = 1.250V<br>1Bh = 1.275V<br>1Ch = 1.300V<br>1Dh = 1.325V<br>1Eh = 1.350V<br>1Fh = 1.375V<br>20h = 1.400V<br>21h = 1.500V<br>22h = 1.600V<br>23h = 1.700V<br>24h = 1.800V<br>25h = 1.900V<br>26h = 2.000V<br>27h = 2.100V<br>28h = 2.200V<br>29h = 2.300V<br>2Ah = 2.400V<br>2Bh = 2.500V<br>2Ch = 2.600V<br>2Dh = 2.700V<br>2Eh = 2.800V<br>2Fh = 2.900V<br>30h = 3.000V<br>31h = 3.100V<br>32h = 3.200V<br>33h = 3.300V<br>34h = 3.400V<br>35h = 3.400V<br>36h = 3.400V<br>37h = 3.400V<br>38h = 3.400V<br>39h = 3.400V<br>3Ah = 3.400V<br>3Bh = 3.400V<br>3Ch = 3.400V<br>3Dh = 3.400V<br>3Eh = 3.400V |

**Table 7-18. BUCK2\_VOUT Register Field Descriptions (continued)**

| Bit | Field | Type | Reset | Description  |
|-----|-------|------|-------|--------------|
|     |       |      |       | 3Fh = 3.400V |

### 7.7.11 BUCK1\_VOUT Register (Offset = Ah) [Reset = X]

BUCK1\_VOUT is shown in [Figure 7-27](#) and described in [Table 7-19](#).

Return to the [Summary Table](#).

**Figure 7-27. BUCK1\_VOUT Register**

|                  |                      |            |   |   |   |   |   |
|------------------|----------------------|------------|---|---|---|---|---|
| 7                | 6                    | 5          | 4 | 3 | 2 | 1 | 0 |
| BUCK1_BW_S<br>EL | BUCK1_UV_TH<br>R_SEL | BUCK1_VSET |   |   |   |   |   |
| R/W-X            | R/W-X                | R/W-X      |   |   |   |   |   |

**Table 7-19. BUCK1\_VOUT Register Field Descriptions**

| Bit | Field            | Type | Reset | Description   |
|-----|------------------|------|-------|---|
| 7   | BUCK1_BW_SEL     | R/W  | X     | BUCK1 Bandwidth selection. NOTE: ONLY CHANGE WHILE RAIL IS DISABLED! (Default from NVM memory)<br>0h = low bandwidth<br>1h = high bandwidth |
| 6   | BUCK1_UV_THR_SEL | R/W  | X     | UV threshold selection for BUCK1. (Default from NVM memory)<br>0h = -5% UV detection<br>1h = -10% UV detection                              |

**Table 7-19. BUCK1\_VOUT Register Field Descriptions (continued)**

| Bit | Field      | Type | Reset | Description  |
|-----|------------|------|-------|--|
| 5-0 | BUCK1_VSET | R/W  | X     | <p>Voltage selection for BUCK1. The output voltage range is from 0.6V to 3.4V. (Default from NVM memory)</p> <p>0h = 0.600V<br/>           1h = 0.625V<br/>           2h = 0.650V<br/>           3h = 0.675V<br/>           4h = 0.700V<br/>           5h = 0.725V<br/>           6h = 0.750V<br/>           7h = 0.775V<br/>           8h = 0.800V<br/>           9h = 0.825V<br/>           Ah = 0.850V<br/>           Bh = 0.875V<br/>           Ch = 0.900V<br/>           Dh = 0.925V<br/>           Eh = 0.950V<br/>           Fh = 0.975V<br/>           10h = 1.000V<br/>           11h = 1.025V<br/>           12h = 1.050V<br/>           13h = 1.075V<br/>           14h = 1.100V<br/>           15h = 1.125V<br/>           16h = 1.150V<br/>           17h = 1.175V<br/>           18h = 1.200V<br/>           19h = 1.225V<br/>           1Ah = 1.250V<br/>           1Bh = 1.275V<br/>           1Ch = 1.300V<br/>           1Dh = 1.325V<br/>           1Eh = 1.350V<br/>           1Fh = 1.375V<br/>           20h = 1.400V<br/>           21h = 1.500V<br/>           22h = 1.600V<br/>           23h = 1.700V<br/>           24h = 1.800V<br/>           25h = 1.900V<br/>           26h = 2.000V<br/>           27h = 2.100V<br/>           28h = 2.200V<br/>           29h = 2.300V<br/>           2Ah = 2.400V<br/>           2Bh = 2.500V<br/>           2Ch = 2.600V<br/>           2Dh = 2.700V<br/>           2Eh = 2.800V<br/>           2Fh = 2.900V<br/>           30h = 3.000V<br/>           31h = 3.100V<br/>           32h = 3.200V<br/>           33h = 3.300V<br/>           34h = 3.400V<br/>           35h = 3.400V<br/>           36h = 3.400V<br/>           37h = 3.400V<br/>           38h = 3.400V<br/>           39h = 3.400V<br/>           3Ah = 3.400V<br/>           3Bh = 3.400V<br/>           3Ch = 3.400V<br/>           3Dh = 3.400V<br/>           3Eh = 3.400V</p> |

**Table 7-19. BUCK1\_VOUT Register Field Descriptions (continued)**

| Bit | Field | Type | Reset | Description  |
|-----|-------|------|-------|--------------|
|     |       |      |       | 3Fh = 3.400V |

### 7.7.12 LDO4\_SEQUENCE\_SLOT Register (Offset = Bh) [Reset = X]

LDO4\_SEQUENCE\_SLOT is shown in [Figure 7-28](#) and described in [Table 7-20](#).

Return to the [Summary Table](#).

**Figure 7-28. LDO4\_SEQUENCE\_SLOT Register**

|                       |   |   |   |                        |   |   |   |
|-----------------------|---|---|---|------------------------|---|---|---|
| 7                     | 6 | 5 | 4 | 3                      | 2 | 1 | 0 |
| LDO4_SEQUENCE_ON_SLOT |   |   |   | LDO4_SEQUENCE_OFF_SLOT |   |   |   |
| R/W-X                 |   |   |   | R/W-X                  |   |   |   |

**Table 7-20. LDO4\_SEQUENCE\_SLOT Register Field Descriptions**

| Bit | Field                  | Type | Reset | Description   |
|-----|------------------------|------|-------|---|
| 7-4 | LDO4_SEQUENCE_ON_SLOT  | R/W  | X     | LDO4 slot number for power-up (Default from NVM memory)<br>0h = slot 0<br>1h = slot 1<br>2h = slot 2<br>3h = slot 3<br>4h = slot 4<br>5h = slot 5<br>6h = slot 6<br>7h = slot 7<br>8h = slot 8<br>9h = slot 9<br>Ah = slot 10<br>Bh = slot 11<br>Ch = slot 12<br>Dh = slot 13<br>Eh = slot 14<br>Fh = slot 15   |
| 3-0 | LDO4_SEQUENCE_OFF_SLOT | R/W  | X     | LDO4 slot number for power-down (Default from NVM memory)<br>0h = slot 0<br>1h = slot 1<br>2h = slot 2<br>3h = slot 3<br>4h = slot 4<br>5h = slot 5<br>6h = slot 6<br>7h = slot 7<br>8h = slot 8<br>9h = slot 9<br>Ah = slot 10<br>Bh = slot 11<br>Ch = slot 12<br>Dh = slot 13<br>Eh = slot 14<br>Fh = slot 15 |

### 7.7.13 LDO3\_SEQUENCE\_SLOT Register (Offset = Ch) [Reset = X]

LDO3\_SEQUENCE\_SLOT is shown in [Figure 7-29](#) and described in [Table 7-21](#).

Return to the [Summary Table](#).

**Figure 7-29. LDO3\_SEQUENCE\_SLOT Register**

|                       |   |   |   |                        |   |   |   |
|-----------------------|---|---|---|------------------------|---|---|---|
| 7                     | 6 | 5 | 4 | 3                      | 2 | 1 | 0 |
| LDO3_SEQUENCE_ON_SLOT |   |   |   | LDO3_SEQUENCE_OFF_SLOT |   |   |   |
| R/W-X                 |   |   |   | R/W-X                  |   |   |   |

**Table 7-21. LDO3\_SEQUENCE\_SLOT Register Field Descriptions**

| Bit | Field                  | Type | Reset | Description   |
|-----|------------------------|------|-------|---|
| 7-4 | LDO3_SEQUENCE_ON_SLOT  | R/W  | X     | LDO3 slot number for power-up (Default from NVM memory)<br>0h = slot 0<br>1h = slot 1<br>2h = slot 2<br>3h = slot 3<br>4h = slot 4<br>5h = slot 5<br>6h = slot 6<br>7h = slot 7<br>8h = slot 8<br>9h = slot 9<br>Ah = slot 10<br>Bh = slot 11<br>Ch = slot 12<br>Dh = slot 13<br>Eh = slot 14<br>Fh = slot 15   |
| 3-0 | LDO3_SEQUENCE_OFF_SLOT | R/W  | X     | LDO3 slot number for power-down (Default from NVM memory)<br>0h = slot 0<br>1h = slot 1<br>2h = slot 2<br>3h = slot 3<br>4h = slot 4<br>5h = slot 5<br>6h = slot 6<br>7h = slot 7<br>8h = slot 8<br>9h = slot 9<br>Ah = slot 10<br>Bh = slot 11<br>Ch = slot 12<br>Dh = slot 13<br>Eh = slot 14<br>Fh = slot 15 |

### 7.7.14 LDO2\_SEQUENCE\_SLOT Register (Offset = Dh) [Reset = X]

LDO2\_SEQUENCE\_SLOT is shown in [Figure 7-30](#) and described in [Table 7-22](#).

Return to the [Summary Table](#).

**Figure 7-30. LDO2\_SEQUENCE\_SLOT Register**

|                       |   |   |   |                        |   |   |   |
|-----------------------|---|---|---|------------------------|---|---|---|
| 7                     | 6 | 5 | 4 | 3                      | 2 | 1 | 0 |
| LDO2_SEQUENCE_ON_SLOT |   |   |   | LDO2_SEQUENCE_OFF_SLOT |   |   |   |
| R/W-X                 |   |   |   | R/W-X                  |   |   |   |

**Table 7-22. LDO2\_SEQUENCE\_SLOT Register Field Descriptions**

| Bit | Field                  | Type | Reset | Description   |
|-----|------------------------|------|-------|---|
| 7-4 | LDO2_SEQUENCE_ON_SLOT  | R/W  | X     | LDO2 slot number for power-up (Default from NVM memory)<br>0h = slot 0<br>1h = slot 1<br>2h = slot 2<br>3h = slot 3<br>4h = slot 4<br>5h = slot 5<br>6h = slot 6<br>7h = slot 7<br>8h = slot 8<br>9h = slot 9<br>Ah = slot 10<br>Bh = slot 11<br>Ch = slot 12<br>Dh = slot 13<br>Eh = slot 14<br>Fh = slot 15   |
| 3-0 | LDO2_SEQUENCE_OFF_SLOT | R/W  | X     | LDO2 slot number for power-down (Default from NVM memory)<br>0h = slot 0<br>1h = slot 1<br>2h = slot 2<br>3h = slot 3<br>4h = slot 4<br>5h = slot 5<br>6h = slot 6<br>7h = slot 7<br>8h = slot 8<br>9h = slot 9<br>Ah = slot 10<br>Bh = slot 11<br>Ch = slot 12<br>Dh = slot 13<br>Eh = slot 14<br>Fh = slot 15 |

**7.7.15 LDO1\_SEQUENCE\_SLOT Register (Offset = Eh) [Reset = X]**

LDO1\_SEQUENCE\_SLOT is shown in [Figure 7-31](#) and described in [Table 7-23](#).

Return to the [Summary Table](#).

**Figure 7-31. LDO1\_SEQUENCE\_SLOT Register**

|                       |   |   |   |                        |   |   |   |
|-----------------------|---|---|---|------------------------|---|---|---|
| 7                     | 6 | 5 | 4 | 3                      | 2 | 1 | 0 |
| LDO1_SEQUENCE_ON_SLOT |   |   |   | LDO1_SEQUENCE_OFF_SLOT |   |   |   |
| R/W-X                 |   |   |   | R/W-X                  |   |   |   |

**Table 7-23. LDO1\_SEQUENCE\_SLOT Register Field Descriptions**

| Bit | Field                  | Type | Reset | Description   |
|-----|------------------------|------|-------|---|
| 7-4 | LDO1_SEQUENCE_ON_SLOT  | R/W  | X     | LDO1 slot number for power-up (Default from NVM memory)<br>0h = slot 0<br>1h = slot 1<br>2h = slot 2<br>3h = slot 3<br>4h = slot 4<br>5h = slot 5<br>6h = slot 6<br>7h = slot 7<br>8h = slot 8<br>9h = slot 9<br>Ah = slot 10<br>Bh = slot 11<br>Ch = slot 12<br>Dh = slot 13<br>Eh = slot 14<br>Fh = slot 15   |
| 3-0 | LDO1_SEQUENCE_OFF_SLOT | R/W  | X     | LDO1 slot number for power-down (Default from NVM memory)<br>0h = slot 0<br>1h = slot 1<br>2h = slot 2<br>3h = slot 3<br>4h = slot 4<br>5h = slot 5<br>6h = slot 6<br>7h = slot 7<br>8h = slot 8<br>9h = slot 9<br>Ah = slot 10<br>Bh = slot 11<br>Ch = slot 12<br>Dh = slot 13<br>Eh = slot 14<br>Fh = slot 15 |

### 7.7.16 BUCK3\_SEQUENCE\_SLOT Register (Offset = Fh) [Reset = X]

BUCK3\_SEQUENCE\_SLOT is shown in [Figure 7-32](#) and described in [Table 7-24](#).

Return to the [Summary Table](#).

**Figure 7-32. BUCK3\_SEQUENCE\_SLOT Register**

|                        |   |   |   |                         |   |   |   |
|------------------------|---|---|---|-------------------------|---|---|---|
| 7                      | 6 | 5 | 4 | 3                       | 2 | 1 | 0 |
| BUCK3_SEQUENCE_ON_SLOT |   |   |   | BUCK3_SEQUENCE_OFF_SLOT |   |   |   |
| R/W-X                  |   |   |   | R/W-X                   |   |   |   |

**Table 7-24. BUCK3\_SEQUENCE\_SLOT Register Field Descriptions**

| Bit | Field                  | Type | Reset | Description  |
|-----|------------------------|------|-------|--|
| 7-4 | BUCK3_SEQUENCE_ON_SLOT | R/W  | X     | BUCK3 slot number for power-up (Default from NVM memory)<br>0h = slot 0<br>1h = slot 1<br>2h = slot 2<br>3h = slot 3<br>4h = slot 4<br>5h = slot 5<br>6h = slot 6<br>7h = slot 7<br>8h = slot 8<br>9h = slot 9<br>Ah = slot 10<br>Bh = slot 11<br>Ch = slot 12<br>Dh = slot 13<br>Eh = slot 14<br>Fh = slot 15   |
| 3-0 | BUCK3_SEQUENCE_OF_SLOT | R/W  | X     | BUCK3 slot number for power-down (Default from NVM memory)<br>0h = slot 0<br>1h = slot 1<br>2h = slot 2<br>3h = slot 3<br>4h = slot 4<br>5h = slot 5<br>6h = slot 6<br>7h = slot 7<br>8h = slot 8<br>9h = slot 9<br>Ah = slot 10<br>Bh = slot 11<br>Ch = slot 12<br>Dh = slot 13<br>Eh = slot 14<br>Fh = slot 15 |

**7.7.17 BUCK2\_SEQUENCE\_SLOT Register (Offset = 10h) [Reset = X]**

BUCK2\_SEQUENCE\_SLOT is shown in [Figure 7-33](#) and described in [Table 7-25](#).

Return to the [Summary Table](#).

**Figure 7-33. BUCK2\_SEQUENCE\_SLOT Register**

|                        |   |   |   |                         |   |   |   |
|------------------------|---|---|---|-------------------------|---|---|---|
| 7                      | 6 | 5 | 4 | 3                       | 2 | 1 | 0 |
| BUCK2_SEQUENCE_ON_SLOT |   |   |   | BUCK2_SEQUENCE_OFF_SLOT |   |   |   |
| R/W-X                  |   |   |   | R/W-X                   |   |   |   |

**Table 7-25. BUCK2\_SEQUENCE\_SLOT Register Field Descriptions**

| Bit | Field                  | Type | Reset | Description  |
|-----|------------------------|------|-------|--|
| 7-4 | BUCK2_SEQUENCE_ON_SLOT | R/W  | X     | BUCK2 Slot number for power-up (Default from NVM memory)<br>0h = slot 0<br>1h = slot 1<br>2h = slot 2<br>3h = slot 3<br>4h = slot 4<br>5h = slot 5<br>6h = slot 6<br>7h = slot 7<br>8h = slot 8<br>9h = slot 9<br>Ah = slot 10<br>Bh = slot 11<br>Ch = slot 12<br>Dh = slot 13<br>Eh = slot 14<br>Fh = slot 15   |
| 3-0 | BUCK2_SEQUENCE_OF_SLOT | R/W  | X     | BUCK2 slot number for power-down (Default from NVM memory)<br>0h = slot 0<br>1h = slot 1<br>2h = slot 2<br>3h = slot 3<br>4h = slot 4<br>5h = slot 5<br>6h = slot 6<br>7h = slot 7<br>8h = slot 8<br>9h = slot 9<br>Ah = slot 10<br>Bh = slot 11<br>Ch = slot 12<br>Dh = slot 13<br>Eh = slot 14<br>Fh = slot 15 |

### 7.7.18 BUCK1\_SEQUENCE\_SLOT Register (Offset = 11h) [Reset = X]

BUCK1\_SEQUENCE\_SLOT is shown in [Figure 7-34](#) and described in [Table 7-26](#).

Return to the [Summary Table](#).

**Figure 7-34. BUCK1\_SEQUENCE\_SLOT Register**

|                        |   |   |   |                         |   |   |   |
|------------------------|---|---|---|-------------------------|---|---|---|
| 7                      | 6 | 5 | 4 | 3                       | 2 | 1 | 0 |
| BUCK1_SEQUENCE_ON_SLOT |   |   |   | BUCK1_SEQUENCE_OFF_SLOT |   |   |   |
| R/W-X                  |   |   |   | R/W-X                   |   |   |   |

**Table 7-26. BUCK1\_SEQUENCE\_SLOT Register Field Descriptions**

| Bit | Field                  | Type | Reset | Description  |
|-----|------------------------|------|-------|--|
| 7-4 | BUCK1_SEQUENCE_ON_SLOT | R/W  | X     | BUCK1 Slot number for power-up (Default from NVM memory)<br>0h = slot 0<br>1h = slot 1<br>2h = slot 2<br>3h = slot 3<br>4h = slot 4<br>5h = slot 5<br>6h = slot 6<br>7h = slot 7<br>8h = slot 8<br>9h = slot 9<br>Ah = slot 10<br>Bh = slot 11<br>Ch = slot 12<br>Dh = slot 13<br>Eh = slot 14<br>Fh = slot 15   |
| 3-0 | BUCK1_SEQUENCE_OF_SLOT | R/W  | X     | BUCK1 slot number for power-down (Default from NVM memory)<br>0h = slot 0<br>1h = slot 1<br>2h = slot 2<br>3h = slot 3<br>4h = slot 4<br>5h = slot 5<br>6h = slot 6<br>7h = slot 7<br>8h = slot 8<br>9h = slot 9<br>Ah = slot 10<br>Bh = slot 11<br>Ch = slot 12<br>Dh = slot 13<br>Eh = slot 14<br>Fh = slot 15 |

### 7.7.19 nRST\_SEQUENCE\_SLOT Register (Offset = 12h) [Reset = X]

nRST\_SEQUENCE\_SLOT is shown in [Figure 7-35](#) and described in [Table 7-27](#).

Return to the [Summary Table](#).

**Figure 7-35. nRST\_SEQUENCE\_SLOT Register**

| 7                     | 6 | 5 | 4 | 3                      | 2 | 1 | 0 |
|-----------------------|---|---|---|------------------------|---|---|---|
| nRST_SEQUENCE_ON_SLOT |   |   |   | nRST_SEQUENCE_OFF_SLOT |   |   |   |
| R/W-X                 |   |   |   | R/W-X                  |   |   |   |

**Table 7-27. nRST\_SEQUENCE\_SLOT Register Field Descriptions**

| Bit | Field                  | Type | Reset | Description   |
|-----|------------------------|------|-------|---|
| 7-4 | nRST_SEQUENCE_ON_SLOT  | R/W  | X     | nRST slot number for power-up (Default from NVM memory)<br>0h = slot 0<br>1h = slot 1<br>2h = slot 2<br>3h = slot 3<br>4h = slot 4<br>5h = slot 5<br>6h = slot 6<br>7h = slot 7<br>8h = slot 8<br>9h = slot 9<br>Ah = slot 10<br>Bh = slot 11<br>Ch = slot 12<br>Dh = slot 13<br>Eh = slot 14<br>Fh = slot 15   |
| 3-0 | nRST_SEQUENCE_OFF_SLOT | R/W  | X     | nRST slot number for power-down (Default from NVM memory)<br>0h = slot 0<br>1h = slot 1<br>2h = slot 2<br>3h = slot 3<br>4h = slot 4<br>5h = slot 5<br>6h = slot 6<br>7h = slot 7<br>8h = slot 8<br>9h = slot 9<br>Ah = slot 10<br>Bh = slot 11<br>Ch = slot 12<br>Dh = slot 13<br>Eh = slot 14<br>Fh = slot 15 |

### 7.7.20 GPIO\_SEQUENCE\_SLOT Register (Offset = 13h) [Reset = X]

GPIO\_SEQUENCE\_SLOT is shown in [Figure 7-36](#) and described in [Table 7-28](#).

Return to the [Summary Table](#).

**Figure 7-36. GPIO\_SEQUENCE\_SLOT Register**

|                       |   |   |   |                        |   |   |   |
|-----------------------|---|---|---|------------------------|---|---|---|
| 7                     | 6 | 5 | 4 | 3                      | 2 | 1 | 0 |
| GPIO_SEQUENCE_ON_SLOT |   |   |   | GPIO_SEQUENCE_OFF_SLOT |   |   |   |
| R/W-X                 |   |   |   | R/W-X                  |   |   |   |

**Table 7-28. GPIO\_SEQUENCE\_SLOT Register Field Descriptions**

| Bit | Field                  | Type | Reset | Description   |
|-----|------------------------|------|-------|---|
| 7-4 | GPIO_SEQUENCE_ON_SLOT  | R/W  | X     | GPIO slot number for power-up (Default from NVM memory)<br>0h = slot 0<br>1h = slot 1<br>2h = slot 2<br>3h = slot 3<br>4h = slot 4<br>5h = slot 5<br>6h = slot 6<br>7h = slot 7<br>8h = slot 8<br>9h = slot 9<br>Ah = slot 10<br>Bh = slot 11<br>Ch = slot 12<br>Dh = slot 13<br>Eh = slot 14<br>Fh = slot 15   |
| 3-0 | GPIO_SEQUENCE_OFF_SLOT | R/W  | X     | GPIO slot number for power-down (Default from NVM memory)<br>0h = slot 0<br>1h = slot 1<br>2h = slot 2<br>3h = slot 3<br>4h = slot 4<br>5h = slot 5<br>6h = slot 6<br>7h = slot 7<br>8h = slot 8<br>9h = slot 9<br>Ah = slot 10<br>Bh = slot 11<br>Ch = slot 12<br>Dh = slot 13<br>Eh = slot 14<br>Fh = slot 15 |

**7.7.21 GPO2\_SEQUENCE\_SLOT Register (Offset = 14h) [Reset = X]**

GPO2\_SEQUENCE\_SLOT is shown in [Figure 7-37](#) and described in [Table 7-29](#).

Return to the [Summary Table](#).

**Figure 7-37. GPO2\_SEQUENCE\_SLOT Register**

|                       |   |   |   |                        |   |   |   |
|-----------------------|---|---|---|------------------------|---|---|---|
| 7                     | 6 | 5 | 4 | 3                      | 2 | 1 | 0 |
| GPO2_SEQUENCE_ON_SLOT |   |   |   | GPO2_SEQUENCE_OFF_SLOT |   |   |   |
| R/W-X                 |   |   |   | R/W-X                  |   |   |   |

**Table 7-29. GPO2\_SEQUENCE\_SLOT Register Field Descriptions**

| Bit | Field                  | Type | Reset | Description   |
|-----|------------------------|------|-------|---|
| 7-4 | GPO2_SEQUENCE_ON_SLOT  | R/W  | X     | GPO2 slot number for power-up (Default from NVM memory)<br>0h = slot 0<br>1h = slot 1<br>2h = slot 2<br>3h = slot 3<br>4h = slot 4<br>5h = slot 5<br>6h = slot 6<br>7h = slot 7<br>8h = slot 8<br>9h = slot 9<br>Ah = slot 10<br>Bh = slot 11<br>Ch = slot 12<br>Dh = slot 13<br>Eh = slot 14<br>Fh = slot 15   |
| 3-0 | GPO2_SEQUENCE_OFF_SLOT | R/W  | X     | GPO2 slot number for power-down (Default from NVM memory)<br>0h = slot 0<br>1h = slot 1<br>2h = slot 2<br>3h = slot 3<br>4h = slot 4<br>5h = slot 5<br>6h = slot 6<br>7h = slot 7<br>8h = slot 8<br>9h = slot 9<br>Ah = slot 10<br>Bh = slot 11<br>Ch = slot 12<br>Dh = slot 13<br>Eh = slot 14<br>Fh = slot 15 |

### 7.7.22 GPO1\_SEQUENCE\_SLOT Register (Offset = 15h) [Reset = X]

GPO1\_SEQUENCE\_SLOT is shown in [Figure 7-38](#) and described in [Table 7-30](#).

Return to the [Summary Table](#).

**Figure 7-38. GPO1\_SEQUENCE\_SLOT Register**

|                       |   |   |   |                        |   |   |   |
|-----------------------|---|---|---|------------------------|---|---|---|
| 7                     | 6 | 5 | 4 | 3                      | 2 | 1 | 0 |
| GPO1_SEQUENCE_ON_SLOT |   |   |   | GPO1_SEQUENCE_OFF_SLOT |   |   |   |
| R/W-X                 |   |   |   | R/W-X                  |   |   |   |

**Table 7-30. GPO1\_SEQUENCE\_SLOT Register Field Descriptions**

| Bit | Field                  | Type | Reset | Description   |
|-----|------------------------|------|-------|---|
| 7-4 | GPO1_SEQUENCE_ON_SLOT  | R/W  | X     | GPO1 slot number for power-up (Default from NVM memory)<br>0h = slot 0<br>1h = slot 1<br>2h = slot 2<br>3h = slot 3<br>4h = slot 4<br>5h = slot 5<br>6h = slot 6<br>7h = slot 7<br>8h = slot 8<br>9h = slot 9<br>Ah = slot 10<br>Bh = slot 11<br>Ch = slot 12<br>Dh = slot 13<br>Eh = slot 14<br>Fh = slot 15   |
| 3-0 | GPO1_SEQUENCE_OFF_SLOT | R/W  | X     | GPO1 slot number for power-down (Default from NVM memory)<br>0h = slot 0<br>1h = slot 1<br>2h = slot 2<br>3h = slot 3<br>4h = slot 4<br>5h = slot 5<br>6h = slot 6<br>7h = slot 7<br>8h = slot 8<br>9h = slot 9<br>Ah = slot 10<br>Bh = slot 11<br>Ch = slot 12<br>Dh = slot 13<br>Eh = slot 14<br>Fh = slot 15 |

### 7.7.23 POWER\_UP\_SLOT\_DURATION\_1 Register (Offset = 16h) [Reset = X]

POWER\_UP\_SLOT\_DURATION\_1 is shown in [Figure 7-39](#) and described in [Table 7-31](#).

Return to the [Summary Table](#).

**Figure 7-39. POWER\_UP\_SLOT\_DURATION\_1 Register**

| 7                          | 6 | 5                          | 4 | 3                          | 2 | 1                          | 0 |
|----------------------------|---|----------------------------|---|----------------------------|---|----------------------------|---|
| POWER_UP_SLOT_0_DURATION_N |   | POWER_UP_SLOT_1_DURATION_N |   | POWER_UP_SLOT_2_DURATION_N |   | POWER_UP_SLOT_3_DURATION_N |   |
| R/W-X                      |   | R/W-X                      |   | R/W-X                      |   | R/W-X                      |   |

**Table 7-31. POWER\_UP\_SLOT\_DURATION\_1 Register Field Descriptions**

| Bit | Field                    | Type | Reset | Description  |
|-----|--------------------------|------|-------|--|
| 7-6 | POWER_UP_SLOT_0_DURATION | R/W  | X     | Duration of slot 0 during the power-up and standby-to-active sequences. (Default from NVM memory)<br>0h = 0ms<br>1h = 1.5ms<br>2h = 3ms<br>3h = 10ms |
| 5-4 | POWER_UP_SLOT_1_DURATION | R/W  | X     | Duration of slot 1 during the power-up and standby-to-active sequences. (Default from NVM memory)<br>0h = 0ms<br>1h = 1.5ms<br>2h = 3ms<br>3h = 10ms |
| 3-2 | POWER_UP_SLOT_2_DURATION | R/W  | X     | Duration of slot 2 during the power-up and standby-to-active sequences. (Default from NVM memory)<br>0h = 0ms<br>1h = 1.5ms<br>2h = 3ms<br>3h = 10ms |
| 1-0 | POWER_UP_SLOT_3_DURATION | R/W  | X     | Duration of slot 3 during the power-up and standby-to-active sequences. (Default from NVM memory)<br>0h = 0ms<br>1h = 1.5ms<br>2h = 3ms<br>3h = 10ms |

### 7.7.24 POWER\_UP\_SLOT\_DURATION\_2 Register (Offset = 17h) [Reset = X]

POWER\_UP\_SLOT\_DURATION\_2 is shown in [Figure 7-40](#) and described in [Table 7-32](#).

Return to the [Summary Table](#).

**Figure 7-40. POWER\_UP\_SLOT\_DURATION\_2 Register**

|                            |   |                            |   |                            |   |                            |   |
|----------------------------|---|----------------------------|---|----------------------------|---|----------------------------|---|
| 7                          | 6 | 5                          | 4 | 3                          | 2 | 1                          | 0 |
| POWER_UP_SLOT_4_DURATION_N |   | POWER_UP_SLOT_5_DURATION_N |   | POWER_UP_SLOT_6_DURATION_N |   | POWER_UP_SLOT_7_DURATION_N |   |
| R/W-X                      |   | R/W-X                      |   | R/W-X                      |   | R/W-X                      |   |

**Table 7-32. POWER\_UP\_SLOT\_DURATION\_2 Register Field Descriptions**

| Bit | Field                    | Type | Reset | Description  |
|-----|--------------------------|------|-------|--|
| 7-6 | POWER_UP_SLOT_4_DURATION | R/W  | X     | Duration of slot 4 during the power-up and standby-to-active sequences. (Default from NVM memory)<br>0h = 0ms<br>1h = 1.5ms<br>2h = 3ms<br>3h = 10ms |
| 5-4 | POWER_UP_SLOT_5_DURATION | R/W  | X     | Duration of slot 5 during the power-up and standby-to-active sequences. (Default from NVM memory)<br>0h = 0ms<br>1h = 1.5ms<br>2h = 3ms<br>3h = 10ms |
| 3-2 | POWER_UP_SLOT_6_DURATION | R/W  | X     | Duration of slot 6 during the power-up and standby-to-active sequences. (Default from NVM memory)<br>0h = 0ms<br>1h = 1.5ms<br>2h = 3ms<br>3h = 10ms |
| 1-0 | POWER_UP_SLOT_7_DURATION | R/W  | X     | Duration of slot 7 during the power-up and standby-to-active sequences. (Default from NVM memory)<br>0h = 0ms<br>1h = 1.5ms<br>2h = 3ms<br>3h = 10ms |

### 7.7.25 POWER\_UP\_SLOT\_DURATION\_3 Register (Offset = 18h) [Reset = X]

POWER\_UP\_SLOT\_DURATION\_3 is shown in [Figure 7-41](#) and described in [Table 7-33](#).

Return to the [Summary Table](#).

**Figure 7-41. POWER\_UP\_SLOT\_DURATION\_3 Register**

| 7                        | 6 | 5                        | 4 | 3                         | 2 | 1                         | 0 |
|--------------------------|---|--------------------------|---|---------------------------|---|---------------------------|---|
| POWER_UP_SLOT_8_DURATION |   | POWER_UP_SLOT_9_DURATION |   | POWER_UP_SLOT_10_DURATION |   | POWER_UP_SLOT_11_DURATION |   |
| R/W-X                    |   | R/W-X                    |   | R/W-X                     |   | R/W-X                     |   |

**Table 7-33. POWER\_UP\_SLOT\_DURATION\_3 Register Field Descriptions**

| Bit | Field                     | Type | Reset | Description   |
|-----|---------------------------|------|-------|---|
| 7-6 | POWER_UP_SLOT_8_DURATION  | R/W  | X     | Duration of slot 8 during the power-up and standby-to-active sequences. (Default from NVM memory)<br>0h = 0ms<br>1h = 1.5ms<br>2h = 3ms<br>3h = 10ms  |
| 5-4 | POWER_UP_SLOT_9_DURATION  | R/W  | X     | Duration of slot 9 during the power-up and standby-to-active sequences. (Default from NVM memory)<br>0h = 0ms<br>1h = 1.5ms<br>2h = 3ms<br>3h = 10ms  |
| 3-2 | POWER_UP_SLOT_10_DURATION | R/W  | X     | Duration of slot 10 during the power-up and standby-to-active sequences. (Default from NVM memory)<br>0h = 0ms<br>1h = 1.5ms<br>2h = 3ms<br>3h = 10ms |
| 1-0 | POWER_UP_SLOT_11_DURATION | R/W  | X     | Duration of slot 11 during the power-up and standby-to-active sequences. (Default from NVM memory)<br>0h = 0ms<br>1h = 1.5ms<br>2h = 3ms<br>3h = 10ms |

### 7.7.26 POWER\_UP\_SLOT\_DURATION\_4 Register (Offset = 19h) [Reset = X]

POWER\_UP\_SLOT\_DURATION\_4 is shown in [Figure 7-42](#) and described in [Table 7-34](#).

Return to the [Summary Table](#).

**Figure 7-42. POWER\_UP\_SLOT\_DURATION\_4 Register**

|                           |                           |                           |                           |          |          |          |          |
|---------------------------|---------------------------|---------------------------|---------------------------|----------|----------|----------|----------|
| <b>7</b>                  | <b>6</b>                  | <b>5</b>                  | <b>4</b>                  | <b>3</b> | <b>2</b> | <b>1</b> | <b>0</b> |
| POWER_UP_SLOT_12_DURATION | POWER_UP_SLOT_13_DURATION | POWER_UP_SLOT_14_DURATION | POWER_UP_SLOT_15_DURATION |          |          |          |          |
| R/W-X                     | R/W-X                     | R/W-X                     | R/W-X                     |          |          |          |          |

**Table 7-34. POWER\_UP\_SLOT\_DURATION\_4 Register Field Descriptions**

| Bit | Field                     | Type | Reset | Description   |
|-----|---------------------------|------|-------|---|
| 7-6 | POWER_UP_SLOT_12_DURATION | R/W  | X     | Duration of slot 12 during the power-up and standby-to-active sequences. (Default from NVM memory)<br>0h = 0ms<br>1h = 1.5ms<br>2h = 3ms<br>3h = 10ms |
| 5-4 | POWER_UP_SLOT_13_DURATION | R/W  | X     | Duration of slot 13 during the power-up and standby-to-active sequences. (Default from NVM memory)<br>0h = 0ms<br>1h = 1.5ms<br>2h = 3ms<br>3h = 10ms |
| 3-2 | POWER_UP_SLOT_14_DURATION | R/W  | X     | Duration of slot 14 during the power-up and standby-to-active sequences. (Default from NVM memory)<br>0h = 0ms<br>1h = 1.5ms<br>2h = 3ms<br>3h = 10ms |
| 1-0 | POWER_UP_SLOT_15_DURATION | R/W  | X     | Duration of slot 15 during the power-up and standby-to-active sequences. (Default from NVM memory)<br>0h = 0ms<br>1h = 1.5ms<br>2h = 3ms<br>3h = 10ms |

### 7.7.27 POWER\_DOWN\_SLOT\_DURATION\_1 Register (Offset = 1Ah) [Reset = X]

POWER\_DOWN\_SLOT\_DURATION\_1 is shown in [Figure 7-43](#) and described in [Table 7-35](#).

Return to the [Summary Table](#).

**Figure 7-43. POWER\_DOWN\_SLOT\_DURATION\_1 Register**

| 7                          | 6 | 5                          | 4 | 3                          | 2 | 1                          | 0 |
|----------------------------|---|----------------------------|---|----------------------------|---|----------------------------|---|
| POWER_DOWN_SLOT_0_DURATION |   | POWER_DOWN_SLOT_1_DURATION |   | POWER_DOWN_SLOT_2_DURATION |   | POWER_DOWN_SLOT_3_DURATION |   |
| R/W-X                      |   | R/W-X                      |   | R/W-X                      |   | R/W-X                      |   |

**Table 7-35. POWER\_DOWN\_SLOT\_DURATION\_1 Register Field Descriptions**

| Bit | Field                      | Type | Reset | Description  |
|-----|----------------------------|------|-------|--|
| 7-6 | POWER_DOWN_SLOT_0_DURATION | R/W  | X     | Duration of slot 0 during the power-down and active-to-standby sequences. (Default from NVM memory)<br>0h = 0ms<br>1h = 1.5ms<br>2h = 3ms<br>3h = 10ms |
| 5-4 | POWER_DOWN_SLOT_1_DURATION | R/W  | X     | Duration of slot 1 during the power-down and active-to-standby sequences. (Default from NVM memory)<br>0h = 0ms<br>1h = 1.5ms<br>2h = 3ms<br>3h = 10ms |
| 3-2 | POWER_DOWN_SLOT_2_DURATION | R/W  | X     | Duration of slot 2 during the power-down and active-to-standby sequences. (Default from NVM memory)<br>0h = 0ms<br>1h = 1.5ms<br>2h = 3ms<br>3h = 10ms |
| 1-0 | POWER_DOWN_SLOT_3_DURATION | R/W  | X     | Duration of slot 3 during the power-down and active-to-standby sequences. (Default from NVM memory)<br>0h = 0ms<br>1h = 1.5ms<br>2h = 3ms<br>3h = 10ms |

### 7.7.28 POWER\_DOWN\_SLOT\_DURATION\_2 Register (Offset = 1Bh) [Reset = X]

POWER\_DOWN\_SLOT\_DURATION\_2 is shown in [Figure 7-44](#) and described in [Table 7-36](#).

Return to the [Summary Table](#).

**Figure 7-44. POWER\_DOWN\_SLOT\_DURATION\_2 Register**

|                            |                            |                            |                            |   |   |   |   |
|----------------------------|----------------------------|----------------------------|----------------------------|---|---|---|---|
| 7                          | 6                          | 5                          | 4                          | 3 | 2 | 1 | 0 |
| POWER_DOWN_SLOT_4_DURATION | POWER_DOWN_SLOT_5_DURATION | POWER_DOWN_SLOT_6_DURATION | POWER_DOWN_SLOT_7_DURATION |   |   |   |   |
| R/W-X                      | R/W-X                      | R/W-X                      | R/W-X                      |   |   |   |   |

**Table 7-36. POWER\_DOWN\_SLOT\_DURATION\_2 Register Field Descriptions**

| Bit | Field                      | Type | Reset | Description  |
|-----|----------------------------|------|-------|--|
| 7-6 | POWER_DOWN_SLOT_4_DURATION | R/W  | X     | Duration of slot 4 during the power-down and active-to-standby sequences. (Default from NVM memory)<br>0h = 0ms<br>1h = 1.5ms<br>2h = 3ms<br>3h = 10ms |
| 5-4 | POWER_DOWN_SLOT_5_DURATION | R/W  | X     | Duration of slot 5 during the power-down and active-to-standby sequences. (Default from NVM memory)<br>0h = 0ms<br>1h = 1.5ms<br>2h = 3ms<br>3h = 10ms |
| 3-2 | POWER_DOWN_SLOT_6_DURATION | R/W  | X     | Duration of slot 6 during the power-down and active-to-standby sequences. (Default from NVM memory)<br>0h = 0ms<br>1h = 1.5ms<br>2h = 3ms<br>3h = 10ms |
| 1-0 | POWER_DOWN_SLOT_7_DURATION | R/W  | X     | Duration of slot 7 during the power-down and active-to-standby sequences. (Default from NVM memory)<br>0h = 0ms<br>1h = 1.5ms<br>2h = 3ms<br>3h = 10ms |

### 7.7.29 POWER\_DOWN\_SLOT\_DURATION\_3 Register (Offset = 1Ch) [Reset = X]

POWER\_DOWN\_SLOT\_DURATION\_3 is shown in [Figure 7-45](#) and described in [Table 7-37](#).

Return to the [Summary Table](#).

**Figure 7-45. POWER\_DOWN\_SLOT\_DURATION\_3 Register**

| 7                          | 6 | 5                          | 4 | 3                           | 2 | 1                           | 0 |
|----------------------------|---|----------------------------|---|-----------------------------|---|-----------------------------|---|
| POWER_DOWN_SLOT_8_DURATION |   | POWER_DOWN_SLOT_9_DURATION |   | POWER_DOWN_SLOT_10_DURATION |   | POWER_DOWN_SLOT_11_DURATION |   |
| R/W-X                      |   | R/W-X                      |   | R/W-X                       |   | R/W-X                       |   |

**Table 7-37. POWER\_DOWN\_SLOT\_DURATION\_3 Register Field Descriptions**

| Bit | Field                       | Type | Reset | Description   |
|-----|-----------------------------|------|-------|---|
| 7-6 | POWER_DOWN_SLOT_8_DURATION  | R/W  | X     | Duration of slot 8 during the power-down and active-to-standby sequences. (Default from NVM memory)<br>0h = 0ms<br>1h = 1.5ms<br>2h = 3ms<br>3h = 10ms  |
| 5-4 | POWER_DOWN_SLOT_9_DURATION  | R/W  | X     | Duration of slot 9 during the power-down and active-to-standby sequences. (Default from NVM memory)<br>0h = 0ms<br>1h = 1.5ms<br>2h = 3ms<br>3h = 10ms  |
| 3-2 | POWER_DOWN_SLOT_10_DURATION | R/W  | X     | Duration of slot 10 during the power-down and active-to-standby sequences. (Default from NVM memory)<br>0h = 0ms<br>1h = 1.5ms<br>2h = 3ms<br>3h = 10ms |
| 1-0 | POWER_DOWN_SLOT_11_DURATION | R/W  | X     | Duration of slot 11 during the power-down and active-to-standby sequences. (Default from NVM memory)<br>0h = 0ms<br>1h = 1.5ms<br>2h = 3ms<br>3h = 10ms |

### 7.7.30 POWER\_DOWN\_SLOT\_DURATION\_4 Register (Offset = 1Dh) [Reset = X]

POWER\_DOWN\_SLOT\_DURATION\_4 is shown in [Figure 7-46](#) and described in [Table 7-38](#).

Return to the [Summary Table](#).

**Figure 7-46. POWER\_DOWN\_SLOT\_DURATION\_4 Register**

|                             |                             |                             |                             |          |          |          |          |
|-----------------------------|-----------------------------|-----------------------------|-----------------------------|----------|----------|----------|----------|
| <b>7</b>                    | <b>6</b>                    | <b>5</b>                    | <b>4</b>                    | <b>3</b> | <b>2</b> | <b>1</b> | <b>0</b> |
| POWER_DOWN_SLOT_12_DURATION | POWER_DOWN_SLOT_13_DURATION | POWER_DOWN_SLOT_14_DURATION | POWER_DOWN_SLOT_15_DURATION |          |          |          |          |
| R/W-X                       | R/W-X                       | R/W-X                       | R/W-X                       |          |          |          |          |

**Table 7-38. POWER\_DOWN\_SLOT\_DURATION\_4 Register Field Descriptions**

| Bit | Field                       | Type | Reset | Description   |
|-----|-----------------------------|------|-------|---|
| 7-6 | POWER_DOWN_SLOT_12_DURATION | R/W  | X     | Duration of slot 12 during the power-down and active-to-standby sequences. (Default from NVM memory)<br>0h = 0ms<br>1h = 1.5ms<br>2h = 3ms<br>3h = 10ms |
| 5-4 | POWER_DOWN_SLOT_13_DURATION | R/W  | X     | Duration of slot 13 during the power-down and active-to-standby sequences. (Default from NVM memory)<br>0h = 0ms<br>1h = 1.5ms<br>2h = 3ms<br>3h = 10ms |
| 3-2 | POWER_DOWN_SLOT_14_DURATION | R/W  | X     | Duration of slot 14 during the power-down and active-to-standby sequences. (Default from NVM memory)<br>0h = 0ms<br>1h = 1.5ms<br>2h = 3ms<br>3h = 10ms |
| 1-0 | POWER_DOWN_SLOT_15_DURATION | R/W  | X     | Duration of slot 15 during the power-down and active-to-standby sequences. (Default from NVM memory)<br>0h = 0ms<br>1h = 1.5ms<br>2h = 3ms<br>3h = 10ms |

### 7.7.31 GENERAL\_CONFIG Register (Offset = 1Eh) [Reset = X]

GENERAL\_CONFIG is shown in [Figure 7-47](#) and described in [Table 7-39](#).

Return to the [Summary Table](#).

**Figure 7-47. GENERAL\_CONFIG Register**

| 7                             | 6           | 5           | 4           | 3           | 2       | 1       | 0       |
|-------------------------------|-------------|-------------|-------------|-------------|---------|---------|---------|
| BYPASS_RAILS_DISCHARGED_CHECK | LDO4_UV_THR | LDO3_UV_THR | LDO2_UV_THR | LDO1_UV_THR | GPIO_EN | GPO2_EN | GPO1_EN |
| R/W-X                         | R/W-X       | R/W-X       | R/W-X       | R/W-X       | R/W-X   | R/W-X   | R/W-X   |

**Table 7-39. GENERAL\_CONFIG Register Field Descriptions**

| Bit | Field                         | Type | Reset | Description   |
|-----|-------------------------------|------|-------|---|
| 7   | BYPASS_RAILS_DISCHARGED_CHECK | R/W  | X     | Bypass the all-rails discharged check to commence a transition to ACTIVE state, and the rails-in-slot discharged check executed in each slot during a power-down to INITIALIZE state. Does not bypass the check for RV(Pre-biased) condition prior to enabling a regulator. (Default from NVM memory)<br>0h = Discharged checks enforced<br>1h = Discharged checks bypassed |
| 6   | LDO4_UV_THR                   | R/W  | X     | UV threshold selection bit for LDO4. Only applicable if configured as LDO. (Default from NVM memory)<br>0h = -5% UV detection<br>1h = -10% UV detection   |
| 5   | LDO3_UV_THR                   | R/W  | X     | UV threshold selection bit for LDO3. Only applicable if configured as LDO. (Default from NVM memory)<br>0h = -5% UV detection<br>1h = -10% UV detection   |
| 4   | LDO2_UV_THR                   | R/W  | X     | UV threshold selection bit for LDO2. Only applicable if configured as LDO. (Default from NVM memory)<br>0h = -5% UV detection<br>1h = -10% UV detection   |
| 3   | LDO1_UV_THR                   | R/W  | X     | UV threshold selection bit for LDO1. Only applicable if configured as LDO. (Default from NVM memory)<br>0h = -5% UV detection<br>1h = -10% UV detection   |
| 2   | GPIO_EN                       | R/W  | X     | Both an enable and state control of GPIO. This bit enables the GPIO function and also controls the state of the GPIO pin. (Default from NVM memory)<br>0h = The GPIO function is disabled. The output state is 'low'.<br>1h = The GPIO function is enabled. The output state is 'high'.   |
| 1   | GPO2_EN                       | R/W  | X     | Both an enable and state control of GPO2. This bit enables the GPO2 function and also controls the state of the GPO2 pin. (Default from NVM memory)<br>0h = GPO2 disabled. The output state is low.<br>1h = GPO2 enabled. The output state is Hi-Z.   |
| 0   | GPO1_EN                       | R/W  | X     | Both an enable and state control of GPO1. This bit enables the GPO1 function and also controls the state of the GPO1 pin. (Default from NVM memory)<br>0h = GPO1 disabled. The output state is low.<br>1h = GPO1 enabled. The output state is Hi-Z.   |

### 7.7.32 MFP\_1\_CONFIG Register (Offset = 1Fh) [Reset = X]

MFP\_1\_CONFIG is shown in [Figure 7-48](#) and described in [Table 7-40](#).

Return to the [Summary Table](#).

**Figure 7-48. MFP\_1\_CONFIG Register**

| 7             | 6                | 5                   | 4                  | 3                   | 2         | 1                | 0           |
|---------------|------------------|---------------------|--------------------|---------------------|-----------|------------------|-------------|
| MODE_I2C_CTRL | VSEL_SD_I2C_CTRL | MODE_RESET_POLARITY | MODE_STBY_POLARITY | MULTI_DEVICE_ENABLE | VSEL_RAIL | VSEL_SD_POLARITY | VSEL_DDR_SD |
| R/W-X         | R/W-X            | R/W-X               | R/W-X              | R/W-X               | R/W-X     | R/W-X            | R/W-X       |

**Table 7-40. MFP\_1\_CONFIG Register Field Descriptions**

| Bit | Field               | Type | Reset | Description  |
|-----|---------------------|------|-------|--|
| 7   | MODE_I2C_CTRL       | R/W  | X     | MODE control using I2C. Consolidated with MODE control via MODE/RESET and/or MODE/STBY pins. Refer to table in the data sheet. (Default from NVM memory)<br>0h = Auto PFM<br>1h = Forced PWM   |
| 6   | VSEL_SD_I2C_CTRL    | R/W  | X     | VSEL_SD control using I2C. Applicable only if VSEL_SD/VSEL_DDR pin is configured as "VSEL_DDR". (Default from NVM memory)<br>0h = 1.8V<br>1h = LDOx_VOUT register setting  |
| 5   | MODE_RESET_POLARITY | R/W  | X     | MODE_RESET Pin Polarity configuration. Note: Ok to change during operation, but consider immediate reaction: MODE-change or RESET-entry! (Default from NVM memory)<br>0h = [if configured as MODE] LOW - auto-PFM / HIGH - forced PWM. [if configured as RESET] LOW - reset / HIGH - normal operation.<br>1h = [if configured as MODE] HIGH - auto-PFM / LOW - forced PWM. [if configured as RESET] HIGH - reset / LOW - normal operation.     |
| 4   | MODE_STBY_POLARITY  | R/W  | X     | MODE_STBY Pin Polarity configuration. Note: Ok to change during operation, but consider immediate reaction: MODE-change or STATE-change! (Default from NVM memory)<br>0h = [if configured as MODE] LOW - auto-PFM / HIGH - forced PWM. [if configured as a STBY] LOW - STBY state / HIGH - ACTIVE state.<br>1h = [if configured as MODE] HIGH - auto-PFM / LOW - forced PWM. [if configured as a STBY] HIGH - STBY state / LOW - ACTIVE state. |
| 3   | MULTI_DEVICE_ENABLE | R/W  | X     | Configures the device as a single device where GPO is used as GPO function, or as a multi-device configuration where GPO is used for synchronization with other devices. NOTE: ONLY CHANGE IN INITIALIZE STATE! (Default from NVM memory)<br>0h = Single-device configuration, GPIO pin configured as GPO<br>1h = Multi-device configuration, GPIO pin configured as GPIO  |
| 2   | VSEL_RAIL           | R/W  | X     | LDO controlled by VSEL_SD/VSEL_DDR. NOTE: ONLY CHANGE IN INITIALIZE STATE! (Default from NVM memory)<br>0h = LDO1<br>1h = LDO2   |
| 1   | VSEL_SD_POLARITY    | R/W  | X     | SD Card Voltage Select Note: Ok to change during operation, but consider immediate reaction: change of SD-card supply voltage! (Default from NVM memory)<br>0h = LOW - 1.8V / HIGH - LDOx_VOUT register setting<br>1h = HIGH - 1.8V / LOW - LDOx_VOUT register setting   |
| 0   | VSEL_DDR_SD         | R/W  | X     | VSEL_SD/VSEL_DDR Configuration NOTE: ONLY CHANGE IN INITIALIZE STATE! (Default from NVM memory)<br>0h = VSEL pin configured as DDR to set the voltage on Buck3<br>1h = VSEL pin configured as SD to set the voltage on the VSEL_RAIL   |

### 7.7.33 MFP\_2\_CONFIG Register (Offset = 20h) [Reset = X]

MFP\_2\_CONFIG is shown in [Figure 7-49](#) and described in [Table 7-41](#).

Return to the [Summary Table](#).

**Figure 7-49. MFP\_2\_CONFIG Register**

| 7         | 6                      | 5                   | 4 | 3                 | 2                 | 1                | 0 |
|-----------|------------------------|---------------------|---|-------------------|-------------------|------------------|---|
| PU_ON_FSD | WARM_COLD_RESET_CONFIG | EN_PB_VSENSE_CONFIG |   | EN_PB_VSENSE_DEGL | MODE_RESET_CONFIG | MODE_STBY_CONFIG |   |
| R/W-X     | R/W-X                  | R/W-X               |   | R/W-X             | R/W-X             | R/W-X            |   |

**Table 7-41. MFP\_2\_CONFIG Register Field Descriptions**

| Bit | Field                  | Type | Reset | Description   |
|-----|------------------------|------|-------|---|
| 7   | PU_ON_FSD              | R/W  | X     | Power up upon First Supply Detected (FSD). So when VSYS is applied, device does power up to ACTIVE state even if EN/PB/VSENSE pin is at OFF_REQ status. (Default from NVM memory)<br>0h = First Supply Detection (FSD) Disabled.<br>1h = First Supply Detection (FSD) Enabled.                                    |
| 6   | WARM_COLD_RESET_CONFIG | R/W  | X     | Selection between WARM or COLD Reset, when a RESET event is triggered via MODE/RESET pin (does not apply to RESET via I2C) (Default from NVM memory)<br>0h = COLD RESET<br>1h = WARM RESET  |
| 5-4 | EN_PB_VSENSE_CONFIG    | R/W  | X     | Enable / Push-Button / VSENSE Configuration. Do not change via I2C after NVM load (except as a precursor before programming NVM) (Default from NVM memory)<br>0h = Device Enable Configuration<br>1h = Push Button Configuration<br>2h = VSENSE Configuration<br>3h = Device Enable Configuration                 |
| 3   | EN_PB_VSENSE_DEGL      | R/W  | X     | Enable / Push-Button / VSENSE Deglitch NOTE: ONLY CHANGE IN INITIALIZE STATE! Consider immediate reaction when changing from EN/VSENSE to PB or vice versa: power-up! (Default from NVM memory)<br>0h = short (typ: 120us for EN/VSENSE and 200ms for PB)<br>1h = long (typ: 50ms for EN/VSENSE and 600ms for PB) |
| 2   | MODE_RESET_CONFIG      | R/W  | X     | MODE/RESET Configuration (Default from NVM memory)<br>0h = MODE<br>1h = RESET   |
| 1-0 | MODE_STBY_CONFIG       | R/W  | X     | MODE_STDBY Configuration (Default from NVM memory)<br>0h = MODE<br>1h = STBY<br>2h = MODE and STBY<br>3h = MODE   |

### 7.7.34 STBY\_1\_CONFIG Register (Offset = 21h) [Reset = X]

STBY\_1\_CONFIG is shown in [Figure 7-50](#) and described in [Table 7-42](#).

Return to the [Summary Table](#).

**Figure 7-50. STBY\_1\_CONFIG Register**

| 7        | 6            | 5            | 4            | 3            | 2             | 1             | 0             |
|----------|--------------|--------------|--------------|--------------|---------------|---------------|---------------|
| RESERVED | LDO4_STBY_EN | LDO3_STBY_EN | LDO2_STBY_EN | LDO1_STBY_EN | BUCK3_STBY_EN | BUCK2_STBY_EN | BUCK1_STBY_EN |
| R-X      | R/W-X        | R/W-X        | R/W-X        | R/W-X        | R/W-X         | R/W-X         | R/W-X         |

**Table 7-42. STBY\_1\_CONFIG Register Field Descriptions**

| Bit | Field         | Type | Reset | Description   |
|-----|---------------|------|-------|---|
| 7   | RESERVED      | R    | X     | Reserved  |
| 6   | LDO4_STBY_EN  | R/W  | X     | Enable LDO4 in STANDBY state. (Default from NVM memory)<br>0h = Disabled in STBY Mode<br>1h = Enabled in STBY Mode  |
| 5   | LDO3_STBY_EN  | R/W  | X     | Enable LDO3 in STANDBY state. (Default from NVM memory)<br>0h = Disabled in STBY Mode<br>1h = Enabled in STBY Mode  |
| 4   | LDO2_STBY_EN  | R/W  | X     | Enable LDO2 in STANDBY state. (Default from NVM memory)<br>0h = Disabled in STBY Mode<br>1h = Enabled in STBY Mode  |
| 3   | LDO1_STBY_EN  | R/W  | X     | Enable LDO1 in STANDBY state. (Default from NVM memory)<br>0h = Disabled in STBY Mode<br>1h = Enabled in STBY Mode  |
| 2   | BUCK3_STBY_EN | R/W  | X     | Enable BUCK3 in STANDBY state. (Default from NVM memory)<br>0h = Disabled in STBY Mode<br>1h = Enabled in STBY Mode |
| 1   | BUCK2_STBY_EN | R/W  | X     | Enable BUCK2 in STANDBY state. (Default from NVM memory)<br>0h = Disabled in STBY Mode<br>1h = Enabled in STBY Mode |
| 0   | BUCK1_STBY_EN | R/W  | X     | Enable BUCK1 in STANDBY state. (Default from NVM memory)<br>0h = Disabled in STBY Mode<br>1h = Enabled in STBY Mode |

### 7.7.35 STBY\_2\_CONFIG Register (Offset = 22h) [Reset = X]

STBY\_2\_CONFIG is shown in [Figure 7-51](#) and described in [Table 7-43](#).

Return to the [Summary Table](#).

**Figure 7-51. STBY\_2\_CONFIG Register**

| 7        | 6        | 5        | 4        | 3        | 2            | 1            | 0            |
|----------|----------|----------|----------|----------|--------------|--------------|--------------|
| RESERVED | RESERVED | RESERVED | RESERVED | RESERVED | GPIO_STBY_EN | GPO2_STBY_EN | GPO1_STBY_EN |
| R-X      | R-X      | R-X      | R-X      | R-X      | R/W-X        | R/W-X        | R/W-X        |

**Table 7-43. STBY\_2\_CONFIG Register Field Descriptions**

| Bit | Field        | Type | Reset | Description  |
|-----|--------------|------|-------|--|
| 7   | RESERVED     | R    | X     | Reserved   |
| 6   | RESERVED     | R    | X     | Reserved   |
| 5   | RESERVED     | R    | X     | Reserved   |
| 4   | RESERVED     | R    | X     | Reserved   |
| 3   | RESERVED     | R    | X     | Reserved   |
| 2   | GPIO_STBY_EN | R/W  | X     | Enable GPIO in STANDBY state. (Default from NVM memory)<br>0h = Disabled in STBY Mode<br>1h = Enabled in STBY Mode |
| 1   | GPO2_STBY_EN | R/W  | X     | Enable GPO2 in STANDBY state. (Default from NVM memory)<br>0h = Disabled in STBY Mode<br>1h = Enabled in STBY Mode |
| 0   | GPO1_STBY_EN | R/W  | X     | Enable GPO1 in STANDBY state. (Default from NVM memory)<br>0h = Disabled in STBY Mode<br>1h = Enabled in STBY Mode |

### 7.7.36 OC\_DEGL\_CONFIG Register (Offset = 23h) [Reset = X]

OC\_DEGL\_CONFIG is shown in [Figure 7-52](#) and described in [Table 7-44](#).

Return to the [Summary Table](#).

**Figure 7-52. OC\_DEGL\_CONFIG Register**

| 7        | 6                        | 5                        | 4                        | 3                        | 2                         | 1                         | 0                         |
|----------|--------------------------|--------------------------|--------------------------|--------------------------|---------------------------|---------------------------|---------------------------|
| RESERVED | EN_LONG_DEGL_FOR_OC_LDO4 | EN_LONG_DEGL_FOR_OC_LDO3 | EN_LONG_DEGL_FOR_OC_LDO2 | EN_LONG_DEGL_FOR_OC_LDO1 | EN_LONG_DEGL_FOR_OC_BUCK3 | EN_LONG_DEGL_FOR_OC_BUCK2 | EN_LONG_DEGL_FOR_OC_BUCK1 |
| R-X      | R/W-X                    | R/W-X                    | R/W-X                    | R/W-X                    | R/W-X                     | R/W-X                     | R/W-X                     |

**Table 7-44. OC\_DEGL\_CONFIG Register Field Descriptions**

| Bit | Field                     | Type | Reset | Description   |
|-----|---------------------------|------|-------|---|
| 7   | RESERVED                  | R    | X     | Reserved  |
| 6   | EN_LONG_DEGL_FOR_OC_LDO4  | R/W  | X     | When set, enables the long-deglitch option for OverCurrent signal of LDO4. When clear, enables the short-deglitch option for OverCurrent signal of LDO4. (Default from NVM memory)<br>0h = Deglitch duration for OverCurrent signals of LDO4 is ~20us<br>1h = Deglitch duration for OverCurrent signals of LDO4 is ~2ms   |
| 5   | EN_LONG_DEGL_FOR_OC_LDO3  | R/W  | X     | When set, enables the long-deglitch option for OverCurrent signal of LDO3. When clear, enables the short-deglitch option for OverCurrent signal of LDO3. (Default from NVM memory)<br>0h = Deglitch duration for OverCurrent signals of LDO3 is ~20us<br>1h = Deglitch duration for OverCurrent signals of LDO3 is ~2ms   |
| 4   | EN_LONG_DEGL_FOR_OC_LDO2  | R/W  | X     | When set, enables the long-deglitch option for OverCurrent signal of LDO2. When clear, enables the short-deglitch option for OverCurrent signal of LDO2. (Default from NVM memory)<br>0h = Deglitch duration for OverCurrent signals of LDO2 is ~20us<br>1h = Deglitch duration for OverCurrent signals of LDO2 is ~2ms   |
| 3   | EN_LONG_DEGL_FOR_OC_LDO1  | R/W  | X     | When set, enables the long-deglitch option for OverCurrent signal of LDO1. When clear, enables the short-deglitch option for OverCurrent signal of LDO1. (Default from NVM memory)<br>0h = Deglitch duration for OverCurrent signals of LDO1 is ~20us<br>1h = Deglitch duration for OverCurrent signals of LDO1 is ~2ms   |
| 2   | EN_LONG_DEGL_FOR_OC_BUCK3 | R/W  | X     | When set, enables the long-deglitch option for OverCurrent signals of BUCK3. When clear, enables the short-deglitch option for OverCurrent signals of BUCK3. (Default from NVM memory)<br>0h = Deglitch duration for OverCurrent signals for BUCK3 (High-Side Overcurrent, Low-Side Overcurrent and Low-Side Reverse/Negative OverCurrent) is ~20us<br>1h = Deglitch duration for OverCurrent signals for BUCK3 (High-Side Overcurrent, Low-Side Overcurrent and Low-Side Reverse/Negative OverCurrent) is ~2ms |
| 1   | EN_LONG_DEGL_FOR_OC_BUCK2 | R/W  | X     | When set, enables the long-deglitch option for OverCurrent signals of BUCK2. When clear, enables the short-deglitch option for OverCurrent signals of BUCK2. (Default from NVM memory)<br>0h = Deglitch duration for OverCurrent signals for BUCK2 (High-Side Overcurrent, Low-Side Overcurrent and Low-Side Reverse/Negative OverCurrent) is ~20us<br>1h = Deglitch duration for OverCurrent signals for BUCK2 (High-Side Overcurrent, Low-Side Overcurrent and Low-Side Reverse/Negative OverCurrent) is ~2ms |

**Table 7-44. OC\_DEGL\_CONFIG Register Field Descriptions (continued)**

| Bit | Field                     | Type | Reset | Description   |
|-----|---------------------------|------|-------|---|
| 0   | EN_LONG_DEGL_FOR_OC_BUCK1 | R/W  | X     | When set, enables the long-deglitch option for OverCurrent signals of BUCK1. When clear, enables the short-deglitch option for OverCurrent signals of BUCK1. (Default from NVM memory)<br>0h = Deglitch duration for OverCurrent signals for BUCK1 (High-Side Overcurrent, Low-Side Overcurrent and Low-Side Reverse/Negative OverCurrent) is ~20us<br>1h = Deglitch duration for OverCurrent signals for BUCK1 (High-Side Overcurrent, Low-Side Overcurrent and Low-Side Reverse/Negative OverCurrent) is ~2ms |

### 7.7.37 INT\_MASK\_UV Register (Offset = 24h) [Reset = X]

INT\_MASK\_UV is shown in [Figure 7-53](#) and described in [Table 7-45](#).

Return to the [Summary Table](#).

**Figure 7-53. INT\_MASK\_UV Register**

| 7                | 6             | 5             | 4             | 3            | 2            | 1            | 0            |
|------------------|---------------|---------------|---------------|--------------|--------------|--------------|--------------|
| MASK_RETRY_COUNT | BUCK3_UV_MASK | BUCK2_UV_MASK | BUCK1_UV_MASK | LDO4_UV_MASK | LDO3_UV_MASK | LDO2_UV_MASK | LDO1_UV_MASK |
| R/W-X            | R/W-X         | R/W-X         | R/W-X         | R/W-X        | R/W-X        | R/W-X        | R/W-X        |

**Table 7-45. INT\_MASK\_UV Register Field Descriptions**

| Bit | Field            | Type | Reset | Description   |
|-----|------------------|------|-------|---|
| 7   | MASK_RETRY_COUNT | R/W  | X     | When set, device can power up even after two retries. (Default from NVM memory)<br>0h = Device does retry up to 2 times, then stay off<br>1h = Device does retry infinitely |
| 6   | BUCK3_UV_MASK    | R/W  | X     | BUCK3 Undervoltage Mask. (Default from NVM memory)<br>0h = un-masked (Faults reported)<br>1h = masked (Faults not reported)   |
| 5   | BUCK2_UV_MASK    | R/W  | X     | BUCK2 Undervoltage Mask. (Default from NVM memory)<br>0h = un-masked (Faults reported)<br>1h = masked (Faults not reported)   |
| 4   | BUCK1_UV_MASK    | R/W  | X     | BUCK1 Undervoltage Mask. (Default from NVM memory)<br>0h = un-masked (Faults reported)<br>1h = masked (Faults not reported)   |
| 3   | LDO4_UV_MASK     | R/W  | X     | LDO4 Undervoltage Mask - Always masked in BYP or LSW modes. (Default from NVM memory)<br>0h = un-masked (Faults reported)<br>1h = masked (Faults not reported)              |
| 2   | LDO3_UV_MASK     | R/W  | X     | LDO3 Undervoltage Mask - Always masked in BYP or LSW modes. (Default from NVM memory)<br>0h = un-masked (Faults reported)<br>1h = masked (Faults not reported)              |
| 1   | LDO2_UV_MASK     | R/W  | X     | LDO2 Undervoltage Mask - Always masked in BYP or LSW modes. (Default from NVM memory)<br>0h = un-masked (Faults reported)<br>1h = masked (Faults not reported)              |
| 0   | LDO1_UV_MASK     | R/W  | X     | LDO1 Undervoltage Mask - Always masked in BYP or LSW modes. (Default from NVM memory)<br>0h = un-masked (Faults reported)<br>1h = masked (Faults not reported)              |

### 7.7.38 MASK\_CONFIG Register (Offset = 25h) [Reset = X]

MASK\_CONFIG is shown in [Figure 7-54](#) and described in [Table 7-46](#).

Return to the [Summary Table](#).

**Figure 7-54. MASK\_CONFIG Register**

| 7               | 6           | 5 | 4               | 3                  | 2                  | 1                  | 0                  |
|-----------------|-------------|---|-----------------|--------------------|--------------------|--------------------|--------------------|
| MASK_INT_FOR_PB | MASK_EFFECT |   | MASK_INT_FOR_RV | SENSOR_0_WARM_MASK | SENSOR_1_WARM_MASK | SENSOR_2_WARM_MASK | SENSOR_3_WARM_MASK |
| R/W-X           | R/W-X       |   | R/W-X           | R/W-X              | R/W-X              | R/W-X              | R/W-X              |

**Table 7-46. MASK\_CONFIG Register Field Descriptions**

| Bit | Field              | Type | Reset | Description   |
|-----|--------------------|------|-------|---|
| 7   | MASK_INT_FOR_PB    | R/W  | X     | Masking bit to control whether nINT pin is sensitive to PushButton (PB) press/release events or not. (Default from NVM memory)<br>0h = un-masked (nINT pulled low for any PB events)<br>1h = masked (nINT not sensitive to any PB events)   |
| 6-5 | MASK_EFFECT        | R/W  | X     | Effect of masking (global) (Default from NVM memory)<br>0h = no state change, no nINT reaction, no bit set for Faults<br>1h = no state change, no nINT reaction, bit set for Faults<br>2h = no state change, nINT reaction, bit set for Faults (same as 11b)<br>3h = no state change, nINT reaction, bit set for Faults (same as 10b) |
| 4   | MASK_INT_FOR_RV    | R/W  | X     | Masking bit to control whether nINT pin is sensitive to RV (Residual Voltage) events or not. (Default from NVM memory)<br>0h = un-masked (nINT pulled low for any RV events during transition to ACTIVE state or during enabling of rails)<br>1h = masked (nINT not sensitive to any RV events)                                       |
| 3   | SENSOR_0_WARM_MASK | R/W  | X     | Die Temperature Warm Fault Mask, Sensor 0. (Default from NVM memory)<br>0h = un-masked (Faults reported)<br>1h = masked (Faults not reported)   |
| 2   | SENSOR_1_WARM_MASK | R/W  | X     | Die Temperature Warm Fault Mask, Sensor 1. (Default from NVM memory)<br>0h = un-masked (Faults reported)<br>1h = masked (Faults not reported)   |
| 1   | SENSOR_2_WARM_MASK | R/W  | X     | Die Temperature Warm Fault Mask, Sensor 2. (Default from NVM memory)<br>0h = un-masked (Faults reported)<br>1h = masked (Faults not reported)   |
| 0   | SENSOR_3_WARM_MASK | R/W  | X     | Die Temperature Warm Fault Mask, Sensor 3. (Default from NVM memory)<br>0h = un-masked (Faults reported)<br>1h = masked (Faults not reported)   |

### 7.7.39 I2C\_ADDRESS\_REG Register (Offset = 26h) [Reset = X]

I2C\_ADDRESS\_REG is shown in [Figure 7-55](#) and described in [Table 7-47](#).

Return to the [Summary Table](#).

**Figure 7-55. I2C\_ADDRESS\_REG Register**

|                                    |             |   |   |   |   |   |   |
|------------------------------------|-------------|---|---|---|---|---|---|
| 7                                  | 6           | 5 | 4 | 3 | 2 | 1 | 0 |
| DIY_NVM_PRO<br>GRAM_CMD_I<br>SSUED | I2C_ADDRESS |   |   |   |   |   |   |
| R/W-X                              | R/W-X       |   |   |   |   |   |   |

**Table 7-47. I2C\_ADDRESS\_REG Register Field Descriptions**

| Bit | Field                          | Type | Reset | Description   |
|-----|--------------------------------|------|-------|---|
| 7   | DIY_NVM_PROGRAM_C<br>MD_ISSUED | R/W  | X     | Bit that indicates whether a DIY program command was attempted. Once set, remains always set. (Default from NVM memory)<br>0h = NVM data not changed<br>1h = NVM data attempted to be changed via DIY program command |
| 6-0 | I2C_ADDRESS                    | R/W  | X     | I2C secondary address. Note: Ok to change during operation, but consider immediate reaction: new address for read/write! (Default from NVM memory)  |

#### 7.7.40 USER\_GENERAL\_NVM\_STORAGE\_REG Register (Offset = 27h) [Reset = X]

USER\_GENERAL\_NVM\_STORAGE\_REG is shown in [Figure 7-56](#) and described in [Table 7-48](#).

Return to the [Summary Table](#).

**Figure 7-56. USER\_GENERAL\_NVM\_STORAGE\_REG Register**

|                          |   |   |   |   |   |   |   |
|--------------------------|---|---|---|---|---|---|---|
| 7                        | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| USER_GENERAL_NVM_STORAGE |   |   |   |   |   |   |   |
| R/W-X                    |   |   |   |   |   |   |   |

**Table 7-48. USER\_GENERAL\_NVM\_STORAGE\_REG Register Field Descriptions**

| Bit | Field                    | Type | Reset | Description  |
|-----|--------------------------|------|-------|--|
| 7-0 | USER_GENERAL_NVM_STORAGE | R/W  | X     | 8-bit NVM-based register available to the user to use to store user-data, for example NVM-ID of customer-modified NVM-version or other purposes. (Default from NVM memory) |

**7.7.41 MANUFACTURING\_VER Register (Offset = 28h) [Reset = 00h]**

MANUFACTURING\_VER is shown in [Figure 7-57](#) and described in [Table 7-49](#).

Return to the [Summary Table](#).

**Figure 7-57. MANUFACTURING\_VER Register**

|             |   |   |   |   |   |   |   |
|-------------|---|---|---|---|---|---|---|
| 7           | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| SILICON_REV |   |   |   |   |   |   |   |
| R-0h        |   |   |   |   |   |   |   |

**Table 7-49. MANUFACTURING\_VER Register Field Descriptions**

| Bit | Field       | Type | Reset | Description   |
|-----|-------------|------|-------|---|
| 7-0 | SILICON_REV | R    | 0h    | SILICON_REV[7:6] - Reserved<br>SILICON_REV[5:3] - ALR<br>SILICON_REV[2:0] - Metal Silicon Revision - Hard wired (not under NVM control) |

### 7.7.42 MFP\_CTRL Register (Offset = 29h) [Reset = X]

MFP\_CTRL is shown in [Figure 7-58](#) and described in [Table 7-50](#).

Return to the [Summary Table](#).

**Figure 7-58. MFP\_CTRL Register**

| 7        | 6        | 5        | 4           | 3                   | 2                   | 1             | 0              |
|----------|----------|----------|-------------|---------------------|---------------------|---------------|----------------|
| RESERVED | RESERVED | RESERVED | GPIO_STATUS | WARM_RESET_I2C_CTRL | COLD_RESET_I2C_CTRL | STBY_I2C_CTRL | I2C_OFF_REQ    |
| R-X      | R-X      | R-X      | R-0h        | R/WSelfClrF-0h      | R/W-0h              | R/W-0h        | R/WSelfClrF-0h |

**Table 7-50. MFP\_CTRL Register Field Descriptions**

| Bit | Field               | Type        | Reset | Description  |
|-----|---------------------|-------------|-------|--|
| 7   | RESERVED            | R           | X     | Reserved   |
| 6   | RESERVED            | R           | X     | Reserved   |
| 5   | RESERVED            | R           | X     | Reserved   |
| 4   | GPIO_STATUS         | R           | 0h    | Indicates the real-time value of GPIO pin<br>0h = The GPIO pin is currently '0'<br>1h = The GPIO pin is currently '1'  |
| 3   | WARM_RESET_I2C_CTRL | R/WSelfClrF | 0h    | Triggers a WARM RESET when written as '1'. Note: This bit self-clears automatically, so cannot be read as '1' after the write.<br>0h = normal operation<br>1h = WARM_RESET |
| 2   | COLD_RESET_I2C_CTRL | R/W         | 0h    | Triggers a COLD RESET when set high. Cleared upon entry to INITIALIZE.<br>0h = normal operation<br>1h = COLD_RESET   |
| 1   | STBY_I2C_CTRL       | R/W         | 0h    | STBY control using I2C. Consolidated with STBY control via MODE/STBY pin. Refer to table in spec.<br>0h = normal operation<br>1h = STBY mode                               |
| 0   | I2C_OFF_REQ         | R/WSelfClrF | 0h    | When '1' is written to this bit: Trigger OFF request. When '0': No effect. Does self-clear.<br>0h = No effect<br>1h = Trigger OFF Request                                  |

### 7.7.43 DISCHARGE\_CONFIG Register (Offset = 2Ah) [Reset = X]

DISCHARGE\_CONFIG is shown in [Figure 7-59](#) and described in [Table 7-51](#).

Return to the [Summary Table](#).

**Figure 7-59. DISCHARGE\_CONFIG Register**

| 7        | 6                 | 5                 | 4                 | 3                 | 2                  | 1                  | 0                  |
|----------|-------------------|-------------------|-------------------|-------------------|--------------------|--------------------|--------------------|
| RESERVED | LDO4_DISCHARGE_EN | LDO3_DISCHARGE_EN | LDO2_DISCHARGE_EN | LDO1_DISCHARGE_EN | BUCK3_DISCHARGE_EN | BUCK2_DISCHARGE_EN | BUCK1_DISCHARGE_EN |
| R-X      | R/W-1h            | R/W-1h            | R/W-1h            | R/W-1h            | R/W-1h             | R/W-1h             | R/W-1h             |

**Table 7-51. DISCHARGE\_CONFIG Register Field Descriptions**

| Bit | Field              | Type | Reset | Description  |
|-----|--------------------|------|-------|--|
| 7   | RESERVED           | R    | X     | Reserved   |
| 6   | LDO4_DISCHARGE_EN  | R/W  | 1h    | Discharge setting for LDO4<br>0h = No Discharge<br>1h = 250 Ω  |
| 5   | LDO3_DISCHARGE_EN  | R/W  | 1h    | Discharge setting for LDO3<br>0h = No Discharge<br>1h = 250 Ω  |
| 4   | LDO2_DISCHARGE_EN  | R/W  | 1h    | Discharge setting for LDO2<br>0h = No Discharge<br>1h = 200 Ω  |
| 3   | LDO1_DISCHARGE_EN  | R/W  | 1h    | Discharge setting for LDO1<br>0h = No Discharge<br>1h = 200 Ω  |
| 2   | BUCK3_DISCHARGE_EN | R/W  | 1h    | Discharge setting for BUCK3<br>0h = No Discharge<br>1h = 125 Ω |
| 1   | BUCK2_DISCHARGE_EN | R/W  | 1h    | Discharge setting for BUCK2<br>0h = No Discharge<br>1h = 125 Ω |
| 0   | BUCK1_DISCHARGE_EN | R/W  | 1h    | Discharge setting for BUCK1<br>0h = No Discharge<br>1h = 125 Ω |

### 7.7.44 INT\_SOURCE Register (Offset = 2Bh) [Reset = 00h]

INT\_SOURCE is shown in [Figure 7-60](#) and described in [Table 7-52](#).

Return to the [Summary Table](#).

**Figure 7-60. INT\_SOURCE Register**

| 7             | 6                  | 5                  | 4                 | 3                   | 2                 | 1             | 0                        |
|---------------|--------------------|--------------------|-------------------|---------------------|-------------------|---------------|--------------------------|
| INT_PB_IS_SET | INT_LDO_3_4_IS_SET | INT_LDO_1_2_IS_SET | INT_BUCK_3_IS_SET | INT_BUCK_1_2_IS_SET | INT_SYSTEM_IS_SET | INT_RV_IS_SET | INT_TIMEOUT_RV_SD_IS_SET |
| R-0h          | R-0h               | R-0h               | R-0h              | R-0h                | R-0h              | R-0h          | R-0h                     |

**Table 7-52. INT\_SOURCE Register Field Descriptions**

| Bit | Field                    | Type | Reset | Description   |
|-----|--------------------------|------|-------|---|
| 7   | INT_PB_IS_SET            | R    | 0h    | One or more sources of the INT present in register INT_PB<br>0h = No bits set in INT_PB<br>1h = One or more bits set in INT_PB                                  |
| 6   | INT_LDO_3_4_IS_SET       | R    | 0h    | One or more sources of the INT present in register INT_LDO_3_4<br>0h = No bits set in INT_LDO_3_4<br>1h = One or more bits set in INT_LDO_3_4                   |
| 5   | INT_LDO_1_2_IS_SET       | R    | 0h    | One or more sources of the INT present in register INT_LDO_1_2<br>0h = No bits set in INT_LDO_1_2<br>1h = One or more bits set in INT_LDO_1_2                   |
| 4   | INT_BUCK_3_IS_SET        | R    | 0h    | One or more sources of the INT present in register INT_BUCK_3<br>0h = No bits set in INT_BUCK_3<br>1h = One or more bits set in INT_BUCK_3                      |
| 3   | INT_BUCK_1_2_IS_SET      | R    | 0h    | One or more sources of the INT present in register INT_BUCK_1_2<br>0h = No bits set in INT_BUCK_1_2<br>1h = One or more bits set in INT_BUCK_1_2                |
| 2   | INT_SYSTEM_IS_SET        | R    | 0h    | One or more sources of the INT present in register INT_SYSTEM<br>0h = No bits set in INT_SYSTEM<br>1h = One or more bits set in INT_SYSTEM                      |
| 1   | INT_RV_IS_SET            | R    | 0h    | One or more sources of the INT present in register INT_RV<br>0h = No bits set in INT_RV<br>1h = One or more bits set in INT_RV                                  |
| 0   | INT_TIMEOUT_RV_SD_IS_SET | R    | 0h    | One or more sources of the INT present in register INT_TIMEOUT_RV_SD<br>0h = No bits set in INT_TIMEOUT_RV_SD<br>1h = One or more bits set in INT_TIMEOUT_RV_SD |

### 7.7.45 INT\_LDO\_3\_4 Register (Offset = 2Ch) [Reset = X]

INT\_LDO\_3\_4 is shown in [Figure 7-61](#) and described in [Table 7-53](#).

Return to the [Summary Table](#).

**Figure 7-61. INT\_LDO\_3\_4 Register**

| 7        | 6        | 5        | 4        | 3        | 2        | 1        | 0        |
|----------|----------|----------|----------|----------|----------|----------|----------|
| RESERVED | RESERVED | LDO4_UV  | LDO4_OC  | LDO4_SCG | LDO3_UV  | LDO3_OC  | LDO3_SCG |
| R-X      | R-X      | R/W1C-0h | R/W1C-0h | R/W1C-0h | R/W1C-0h | R/W1C-0h | R/W1C-0h |

**Table 7-53. INT\_LDO\_3\_4 Register Field Descriptions**

| Bit | Field    | Type  | Reset | Description   |
|-----|----------|-------|-------|---|
| 7   | RESERVED | R     | X     | Reserved  |
| 6   | RESERVED | R     | X     | Reserved  |
| 5   | LDO4_UV  | R/W1C | 0h    | LDO4 Undervoltage Fault. Is automatically cleared upon a transition to INITIALIZE state, if corresponding *_UV_MASK bit in register INT_MASK_UV is '1'<br>0h = No Fault detected<br>1h = Fault detected |
| 4   | LDO4_OC  | R/W1C | 0h    | LDO4 Overcurrent Fault.<br>0h = No Fault detected<br>1h = Fault detected  |
| 3   | LDO4_SCG | R/W1C | 0h    | LDO4 Short Circuit to Ground Fault<br>0h = No Fault detected<br>1h = Fault detected   |
| 2   | LDO3_UV  | R/W1C | 0h    | LDO3 Undervoltage Fault. Is automatically cleared upon a transition to INITIALIZE state, if corresponding *_UV_MASK bit in register INT_MASK_UV is '1'<br>0h = No Fault detected<br>1h = Fault detected |
| 1   | LDO3_OC  | R/W1C | 0h    | LDO3 Overcurrent Fault<br>0h = No Fault detected<br>1h = Fault detected   |
| 0   | LDO3_SCG | R/W1C | 0h    | LDO3 Short Circuit to Ground Fault<br>0h = No Fault detected<br>1h = Fault detected   |

### 7.7.46 INT\_LDO\_1\_2 Register (Offset = 2Dh) [Reset = X]

INT\_LDO\_1\_2 is shown in [Figure 7-62](#) and described in [Table 7-54](#).

Return to the [Summary Table](#).

**Figure 7-62. INT\_LDO\_1\_2 Register**

| 7        | 6        | 5        | 4        | 3        | 2        | 1        | 0        |
|----------|----------|----------|----------|----------|----------|----------|----------|
| RESERVED | RESERVED | LDO2_UV  | LDO2_OC  | LDO2_SCG | LDO1_UV  | LDO1_OC  | LDO1_SCG |
| R-X      | R-X      | R/W1C-0h | R/W1C-0h | R/W1C-0h | R/W1C-0h | R/W1C-0h | R/W1C-0h |

**Table 7-54. INT\_LDO\_1\_2 Register Field Descriptions**

| Bit | Field    | Type  | Reset | Description   |
|-----|----------|-------|-------|---|
| 7   | RESERVED | R     | X     | Reserved  |
| 6   | RESERVED | R     | X     | Reserved  |
| 5   | LDO2_UV  | R/W1C | 0h    | LDO2 Undervoltage Fault. Is automatically cleared upon a transition to INITIALIZE state, if corresponding *_UV_MASK bit in register INT_MASK_UV is '1'<br>0h = No Fault detected<br>1h = Fault detected |
| 4   | LDO2_OC  | R/W1C | 0h    | LDO2 Overcurrent Fault<br>0h = No Fault detected<br>1h = Fault detected   |
| 3   | LDO2_SCG | R/W1C | 0h    | LDO2 Short Circuit to Ground Fault<br>0h = No Fault detected<br>1h = Fault detected   |
| 2   | LDO1_UV  | R/W1C | 0h    | LDO1 Undervoltage Fault. Is automatically cleared upon a transition to INITIALIZE state, if corresponding *_UV_MASK bit in register INT_MASK_UV is '1'<br>0h = No Fault detected<br>1h = Fault detected |
| 1   | LDO1_OC  | R/W1C | 0h    | LDO1 Overcurrent Fault<br>0h = No Fault detected<br>1h = Fault detected   |
| 0   | LDO1_SCG | R/W1C | 0h    | LDO1 Short Circuit to Ground Fault<br>0h = No Fault detected<br>1h = Fault detected   |

### 7.7.47 INT\_BUCK\_3 Register (Offset = 2Eh) [Reset = X]

INT\_BUCK\_3 is shown in [Figure 7-63](#) and described in [Table 7-55](#).

Return to the [Summary Table](#).

**Figure 7-63. INT\_BUCK\_3 Register**

| 7        | 6        | 5        | 4        | 3        | 2            | 1        | 0         |
|----------|----------|----------|----------|----------|--------------|----------|-----------|
| RESERVED | RESERVED | RESERVED | RESERVED | BUCK3_UV | BUCK3_NEG_OC | BUCK3_OC | BUCK3_SCG |
| R-X      | R-X      | R-X      | R-X      | R/W1C-0h | R/W1C-0h     | R/W1C-0h | R/W1C-0h  |

**Table 7-55. INT\_BUCK\_3 Register Field Descriptions**

| Bit | Field        | Type  | Reset | Description  |
|-----|--------------|-------|-------|--|
| 7   | RESERVED     | R     | X     | Reserved   |
| 6   | RESERVED     | R     | X     | Reserved   |
| 5   | RESERVED     | R     | X     | Reserved   |
| 4   | RESERVED     | R     | X     | Reserved   |
| 3   | BUCK3_UV     | R/W1C | 0h    | BUCK3 Undervoltage Fault. Is automatically cleared upon a transition to INITIALIZE state, if corresponding *_UV_MASK bit in register INT_MASK_UV is '1'<br>0h = No Fault detected<br>1h = Fault detected |
| 2   | BUCK3_NEG_OC | R/W1C | 0h    | BUCK3 Negative Overcurrent Fault<br>0h = No Fault detected<br>1h = Fault detected  |
| 1   | BUCK3_OC     | R/W1C | 0h    | BUCK3 Positive Overcurrent Fault<br>0h = No Fault detected<br>1h = Fault detected  |
| 0   | BUCK3_SCG    | R/W1C | 0h    | BUCK3 Short Circuit to Ground Fault<br>0h = No Fault detected<br>1h = Fault detected   |

### 7.7.48 INT\_BUCK\_1\_2 Register (Offset = 2Fh) [Reset = 00h]

INT\_BUCK\_1\_2 is shown in [Figure 7-64](#) and described in [Table 7-56](#).

Return to the [Summary Table](#).

**Figure 7-64. INT\_BUCK\_1\_2 Register**

| 7        | 6            | 5        | 4         | 3        | 2            | 1        | 0         |
|----------|--------------|----------|-----------|----------|--------------|----------|-----------|
| BUCK2_UV | BUCK2_NEG_OC | BUCK2_OC | BUCK2_SCG | BUCK1_UV | BUCK1_NEG_OC | BUCK1_OC | BUCK1_SCG |
| R/W1C-0h | R/W1C-0h     | R/W1C-0h | R/W1C-0h  | R/W1C-0h | R/W1C-0h     | R/W1C-0h | R/W1C-0h  |

**Table 7-56. INT\_BUCK\_1\_2 Register Field Descriptions**

| Bit | Field        | Type  | Reset | Description  |
|-----|--------------|-------|-------|--|
| 7   | BUCK2_UV     | R/W1C | 0h    | BUCK2 Undervoltage Fault. Is automatically cleared upon a transition to INITIALIZE state, if corresponding *_UV_MASK bit in register INT_MASK_UV is '1'<br>0h = No Fault detected<br>1h = Fault detected |
| 6   | BUCK2_NEG_OC | R/W1C | 0h    | BUCK2 Negative Overcurrent Fault<br>0h = No Fault detected<br>1h = Fault detected  |
| 5   | BUCK2_OC     | R/W1C | 0h    | BUCK2 Positive Overcurrent Fault<br>0h = No Fault detected<br>1h = Fault detected  |
| 4   | BUCK2_SCG    | R/W1C | 0h    | BUCK2 Short Circuit to Ground Fault<br>0h = No Fault detected<br>1h = Fault detected   |
| 3   | BUCK1_UV     | R/W1C | 0h    | BUCK1 Undervoltage Fault. Is automatically cleared upon a transition to INITIALIZE state, if corresponding *_UV_MASK bit in register INT_MASK_UV is '1'<br>0h = No Fault detected<br>1h = Fault detected |
| 2   | BUCK1_NEG_OC | R/W1C | 0h    | BUCK1 Negative Overcurrent Fault<br>0h = No Fault detected<br>1h = Fault detected  |
| 1   | BUCK1_OC     | R/W1C | 0h    | BUCK1 Positive Overcurrent Fault<br>0h = No Fault detected<br>1h = Fault detected  |
| 0   | BUCK1_SCG    | R/W1C | 0h    | BUCK1 Short Circuit to Ground Fault<br>0h = No Fault detected<br>1h = Fault detected   |

### 7.7.49 INT\_SYSTEM Register (Offset = 30h) [Reset = 00h]

INT\_SYSTEM is shown in [Figure 7-65](#) and described in [Table 7-57](#).

Return to the [Summary Table](#).

**Figure 7-65. INT\_SYSTEM Register**

| 7                | 6                | 5                | 4                | 3                 | 2                 | 1                 | 0                 |
|------------------|------------------|------------------|------------------|-------------------|-------------------|-------------------|-------------------|
| SENSOR_0_H<br>OT | SENSOR_1_H<br>OT | SENSOR_2_H<br>OT | SENSOR_3_H<br>OT | SENSOR_0_W<br>ARM | SENSOR_1_W<br>ARM | SENSOR_2_W<br>ARM | SENSOR_3_W<br>ARM |
| R/W1C-0h         | R/W1C-0h         | R/W1C-0h         | R/W1C-0h         | R/W1C-0h          | R/W1C-0h          | R/W1C-0h          | R/W1C-0h          |

**Table 7-57. INT\_SYSTEM Register Field Descriptions**

| Bit | Field         | Type  | Reset | Description   |
|-----|---------------|-------|-------|---|
| 7   | SENSOR_0_HOT  | R/W1C | 0h    | TSD Hot detection for sensor 0<br>0h = No Fault detected<br>1h = Fault detected   |
| 6   | SENSOR_1_HOT  | R/W1C | 0h    | TSD Hot detection for sensor 1<br>0h = No Fault detected<br>1h = Fault detected   |
| 5   | SENSOR_2_HOT  | R/W1C | 0h    | TSD Hot detection for sensor 2<br>0h = No Fault detected<br>1h = Fault detected   |
| 4   | SENSOR_3_HOT  | R/W1C | 0h    | TSD Hot detection for sensor 3<br>0h = No Fault detected<br>1h = Fault detected   |
| 3   | SENSOR_0_WARM | R/W1C | 0h    | TSD Warm detection for sensor 0. Is automatically cleared upon a transition to INITIALIZE state, if corresponding *_WARM_MASK bit in register MASK_CONFIG is '1'<br>0h = No Fault detected<br>1h = Fault detected |
| 2   | SENSOR_1_WARM | R/W1C | 0h    | TSD Warm detection for sensor 1. Is automatically cleared upon a transition to INITIALIZE state, if corresponding *_WARM_MASK bit in register MASK_CONFIG is '1'<br>0h = No Fault detected<br>1h = Fault detected |
| 1   | SENSOR_2_WARM | R/W1C | 0h    | TSD Warm detection for sensor 2. Is automatically cleared upon a transition to INITIALIZE state, if corresponding *_WARM_MASK bit in register MASK_CONFIG is '1'<br>0h = No Fault detected<br>1h = Fault detected |
| 0   | SENSOR_3_WARM | R/W1C | 0h    | TSD Warm detection for sensor 3. Is automatically cleared upon a transition to INITIALIZE state, if corresponding *_WARM_MASK bit in register MASK_CONFIG is '1'<br>0h = No Fault detected<br>1h = Fault detected |

### 7.7.50 INT\_RV Register (Offset = 31h) [Reset = X]

INT\_RV is shown in [Figure 7-66](#) and described in [Table 7-58](#).

Return to the [Summary Table](#).

**Figure 7-66. INT\_RV Register**

| 7        | 6        | 5        | 4        | 3        | 2        | 1        | 0        |
|----------|----------|----------|----------|----------|----------|----------|----------|
| RESERVED | LDO4_RV  | LDO3_RV  | LDO2_RV  | LDO1_RV  | BUCK3_RV | BUCK2_RV | BUCK1_RV |
| R-X      | R/W1C-0h | R/W1C-0h | R/W1C-0h | R/W1C-0h | R/W1C-0h | R/W1C-0h | R/W1C-0h |

**Table 7-58. INT\_RV Register Field Descriptions**

| Bit | Field    | Type  | Reset | Description  |
|-----|----------|-------|-------|--|
| 7   | RESERVED | R     | X     | Reserved   |
| 6   | LDO4_RV  | R/W1C | 0h    | RV event detected on LDO4 rail during rail-turn-on, or after 4-5 ms during discharge checks prior to entering power sequence to ACTIVE state<br>0h = No RV detected<br>1h = RV detected  |
| 5   | LDO3_RV  | R/W1C | 0h    | RV event detected on LDO3 rail during rail-turn-on, or after 4-5 ms during discharge checks prior to entering power sequence to ACTIVE state<br>0h = No RV detected<br>1h = RV detected  |
| 4   | LDO2_RV  | R/W1C | 0h    | RV event detected on LDO2 rail during rail-turn-on, or after 4-5 ms during discharge checks prior to entering power sequence to ACTIVE state<br>0h = No RV detected<br>1h = RV detected  |
| 3   | LDO1_RV  | R/W1C | 0h    | RV event detected on LDO1 rail during rail-turn-on, or after 4-5 ms during discharge checks prior to entering power sequence to ACTIVE state<br>0h = No RV detected<br>1h = RV detected  |
| 2   | BUCK3_RV | R/W1C | 0h    | RV event detected on BUCK3 rail during rail-turn-on, or after 4-5 ms during discharge checks prior to entering power sequence to ACTIVE state<br>0h = No RV detected<br>1h = RV detected |
| 1   | BUCK2_RV | R/W1C | 0h    | RV event detected on BUCK2 rail during rail-turn-on, or after 4-5 ms during discharge checks prior to entering power sequence to ACTIVE state<br>0h = No RV detected<br>1h = RV detected |
| 0   | BUCK1_RV | R/W1C | 0h    | RV event detected on BUCK1 rail during rail-turn-on, or after 4-5 ms during discharge checks prior to entering power sequence to ACTIVE state<br>0h = No RV detected<br>1h = RV detected |

### 7.7.51 INT\_TIMEOUT\_RV\_SD Register (Offset = 32h) [Reset = 00h]

INT\_TIMEOUT\_RV\_SD is shown in [Figure 7-67](#) and described in [Table 7-59](#).

Return to the [Summary Table](#).

**Figure 7-67. INT\_TIMEOUT\_RV\_SD Register**

| 7        | 6          | 5          | 4          | 3          | 2           | 1           | 0           |
|----------|------------|------------|------------|------------|-------------|-------------|-------------|
| TIMEOUT  | LDO4_RV_SD | LDO3_RV_SD | LDO2_RV_SD | LDO1_RV_SD | BUCK3_RV_SD | BUCK2_RV_SD | BUCK1_RV_SD |
| R/W1C-0h | R/W1C-0h   | R/W1C-0h   | R/W1C-0h   | R/W1C-0h   | R/W1C-0h    | R/W1C-0h    | R/W1C-0h    |

**Table 7-59. INT\_TIMEOUT\_RV\_SD Register Field Descriptions**

| Bit | Field      | Type  | Reset | Description   |
|-----|------------|-------|-------|---|
| 7   | TIMEOUT    | R/W1C | 0h    | Is set if ShutDown occurred due to a TimeOut while: 1. Transitioning to ACTIVE state, and one or more rails did not rise past the UV level at the end of the assigned slot (and UV on this rail is configured as a SD fault). Which rail(s) is/are indicated by the *_UV bits in the INT_* registers. 2. Transitioning to STANDBY state, and one or more rails did not fall below the SCG level at the end of the assigned slot and discharge is enabled for that rail (which rail(s) is/are indicated by the corresponding RV_SD bit(s) in this register).<br>0h = No SD due to TimeOut occurred<br>1h = SD due to TimeOut occurred  |
| 6   | LDO4_RV_SD | R/W1C | 0h    | RV on LDO4 rail caused a shutdown during: 1. A transition to STANDBY state, this rail did not discharge at the end of the assigned slot and discharge is enabled for this rail 2. A transition to STANDBY state, RV was observed on this rail during the transition after this rail was disabled and discharge was enabled 3. A transition to ACTIVE state, RV was observed on this rail during the transition when this rail was OFF (rails are expected to be discharged before commencing the sequence to ACTIVE) 4. This rail did not discharge and therefore caused a Timeout-SD while attempting to discharge all rails at the start of a transition from STANDBY to ACTIVE (TIMEOUT bit gets also set in this case)<br>0h = No SD due to RV/DISCHARGE_TIMEOUT on LDO4 occurred<br>1h = SD due to RV/DISCHARGE_TIMEOUT on LDO4 occurred |
| 5   | LDO3_RV_SD | R/W1C | 0h    | RV on LDO4 rail caused a shutdown during: 1. A transition to STANDBY state, this rail did not discharge at the end of the assigned slot and discharge is enabled for this rail 2. A transition to STANDBY state, RV was observed on this rail during the transition after this rail was disabled and discharge was enabled 3. A transition to ACTIVE state, RV was observed on this rail during the transition when this rail was OFF (rails are expected to be discharged before commencing the sequence to ACTIVE) 4. This rail did not discharge and therefore caused a Timeout-SD while attempting to discharge all rails at the start of a transition from STANDBY to ACTIVE (TIMEOUT bit gets also set in this case)<br>0h = No SD due to RV/DISCHARGE_TIMEOUT on LDO3 occurred<br>1h = SD due to RV/DISCHARGE_TIMEOUT on LDO3 occurred |
| 4   | LDO2_RV_SD | R/W1C | 0h    | RV on LDO4 rail caused a shutdown during: 1. A transition to STANDBY state, this rail did not discharge at the end of the assigned slot and discharge is enabled for this rail 2. A transition to STANDBY state, RV was observed on this rail during the transition after this rail was disabled and discharge was enabled 3. A transition to ACTIVE state, RV was observed on this rail during the transition when this rail was OFF (rails are expected to be discharged before commencing the sequence to ACTIVE) 4. This rail did not discharge and therefore caused a Timeout-SD while attempting to discharge all rails at the start of a transition from STANDBY to ACTIVE (TIMEOUT bit gets also set in this case)<br>0h = No SD due to RV/DISCHARGE_TIMEOUT on LDO2 occurred<br>1h = SD due to RV/DISCHARGE_TIMEOUT on LDO2 occurred |

**Table 7-59. INT\_TIMEOUT\_RV\_SD Register Field Descriptions (continued)**

| Bit | Field       | Type  | Reset | Description   |
|-----|-------------|-------|-------|---|
| 3   | LDO1_RV_SD  | R/W1C | 0h    | RV on LDO4 rail caused a shutdown during: 1. A transition to STANDBY state, this rail did not discharge at the end of the assigned slot and discharge is enabled for this rail 2. A transition to STANDBY state, RV was observed on this rail during the transition after this rail was disabled and discharge was enabled 3. A transition to ACTIVE state, RV was observed on this rail during the transition when this rail was OFF (rails are expected to be discharged before commencing the sequence to ACTIVE) 4. This rail did not discharge and therefore caused a Timeout-SD while attempting to discharge all rails at the start of a transition from STANDBY to ACTIVE (TIMEOUT bit gets also set in this case)<br>0h = No SD due to RV/DISCHARGE_TIMEOUT on LDO1 occurred<br>1h = SD due to RV/DISCHARGE_TIMEOUT on LDO1 occurred   |
| 2   | BUCK3_RV_SD | R/W1C | 0h    | RV on LDO4 rail caused a shutdown during: 1. A transition to STANDBY state, this rail did not discharge at the end of the assigned slot and discharge is enabled for this rail 2. A transition to STANDBY state, RV was observed on this rail during the transition after this rail was disabled and discharge was enabled 3. A transition to ACTIVE state, RV was observed on this rail during the transition when this rail was OFF (rails are expected to be discharged before commencing the sequence to ACTIVE) 4. This rail did not discharge and therefore caused a Timeout-SD while attempting to discharge all rails at the start of a transition from STANDBY to ACTIVE (TIMEOUT bit gets also set in this case)<br>0h = No SD due to RV/DISCHARGE_TIMEOUT on BUCK3 occurred<br>1h = SD due to RV/DISCHARGE_TIMEOUT on BUCK3 occurred |
| 1   | BUCK2_RV_SD | R/W1C | 0h    | RV on LDO4 rail caused a shutdown during: 1. A transition to STANDBY state, this rail did not discharge at the end of the assigned slot and discharge is enabled for this rail 2. A transition to STANDBY state, RV was observed on this rail during the transition after this rail was disabled and discharge was enabled 3. A transition to ACTIVE state, RV was observed on this rail during the transition when this rail was OFF (rails are expected to be discharged before commencing the sequence to ACTIVE) 4. This rail did not discharge and therefore caused a Timeout-SD while attempting to discharge all rails at the start of a transition from STANDBY to ACTIVE (TIMEOUT bit gets also set in this case)<br>0h = No SD due to RV/DISCHARGE_TIMEOUT on BUCK2 occurred<br>1h = SD due to RV/DISCHARGE_TIMEOUT on BUCK2 occurred |
| 0   | BUCK1_RV_SD | R/W1C | 0h    | RV on LDO4 rail caused a shutdown during: 1. A transition to STANDBY state, this rail did not discharge at the end of the assigned slot and discharge is enabled for this rail 2. A transition to STANDBY state, RV was observed on this rail during the transition after this rail was disabled and discharge was enabled 3. A transition to ACTIVE state, RV was observed on this rail during the transition when this rail was OFF (rails are expected to be discharged before commencing the sequence to ACTIVE) 4. This rail did not discharge and therefore caused a Timeout-SD while attempting to discharge all rails at the start of a transition from STANDBY to ACTIVE (TIMEOUT bit gets also set in this case)<br>0h = No SD due to RV/DISCHARGE_TIMEOUT on BUCK1 occurred<br>1h = SD due to RV/DISCHARGE_TIMEOUT on BUCK1 occurred |

### 7.7.52 INT\_PB Register (Offset = 33h) [Reset = X]

INT\_PB is shown in [Figure 7-68](#) and described in [Table 7-60](#).

Return to the [Summary Table](#).

**Figure 7-68. INT\_PB Register**

| 7        | 6        | 5        | 4        | 3        | 2                       | 1                               | 0                                |
|----------|----------|----------|----------|----------|-------------------------|---------------------------------|----------------------------------|
| RESERVED | RESERVED | RESERVED | RESERVED | RESERVED | PB_REAL_TIM<br>E_STATUS | PB_RISING_E<br>DGE_DETECT<br>ED | PB_FALLING_E<br>DGE_DETECT<br>ED |
| R-X      | R-X      | R-X      | R-X      | R-X      | R-1h                    | R/W1C-0h                        | R/W1C-0h                         |

**Table 7-60. INT\_PB Register Field Descriptions**

| Bit | Field                    | Type  | Reset | Description   |
|-----|--------------------------|-------|-------|---|
| 7   | RESERVED                 | R     | X     | Reserved  |
| 6   | RESERVED                 | R     | X     | Reserved  |
| 5   | RESERVED                 | R     | X     | Reserved  |
| 4   | RESERVED                 | R     | X     | Reserved  |
| 3   | RESERVED                 | R     | X     | Reserved  |
| 2   | PB_REAL_TIME_STATUS      | R     | 1h    | Deglitched (64-128ms) real-time status of PB pin. Valid only when EN/PB/VSENSE pin is configured as PB.<br>0h = Current deglitched status of PB: PRESSED<br>1h = Current deglitched status of PB: RELEASED                            |
| 1   | PB_RISING_EDGE_DETECTED  | R/W1C | 0h    | PB was released for > deglitch period (64-128ms) since the previous time this bit was cleared. This bit when set, does assert nINT pin (if config bit MASK_INT_FOR_PB=0').<br>0h = No PB-release detected<br>1h = PB-release detected |
| 0   | PB_FALLING_EDGE_DETECTED | R/W1C | 0h    | PB was pressed for > deglitch period (64-128ms) since the previous time this bit was cleared. This bit when set, does assert nINT pin (if config bit MASK_INT_FOR_PB=0').<br>0h = No PB-press detected<br>1h = PB-press detected      |

### 7.7.53 USER\_NVM\_CMD\_REG Register (Offset = 34h) [Reset = 00h]

USER\_NVM\_CMD\_REG is shown in [Figure 7-69](#) and described in [Table 7-61](#).

Return to the [Summary Table](#).

**Figure 7-69. USER\_NVM\_CMD\_REG Register**

| 7                 | 6                    | 5              | 4          | 3            | 2 | 1 | 0 |
|-------------------|----------------------|----------------|------------|--------------|---|---|---|
| NVM_VERIFY_RESULT | CUST_NVM_VERIFY_DONE | CUST_PROG_DONE | I2C_OSC_ON | USER_NVM_CMD |   |   |   |
| R-0h              | R/W1C-0h             | R/W1C-0h       | R-0h       | R-0h         |   |   |   |

**Table 7-61. USER\_NVM\_CMD\_REG Register Field Descriptions**

| Bit | Field                | Type  | Reset | Description  |
|-----|----------------------|-------|-------|--|
| 7   | NVM_VERIFY_RESULT    | R     | 0h    | After an CUST_NVM_VERIFY_CMD is executed, this bit gives the result of the operation. (1 = fail, 0= pass). If '1', can only be cleared if a subsequent CUST_NVM_VERIFY_CMD passes.<br>0h = PASS<br>1h = FAIL |
| 6   | CUST_NVM_VERIFY_DONE | R/W1C | 0h    | Is set to '1' after a CUST_NVM_VERIFY_CMD is executed. Remains '1' until W1C by user.<br>0h = Not yet done / not in progress<br>1h = Done  |
| 5   | CUST_PROG_DONE       | R/W1C | 0h    | Is set to '1' after a CUST_PROG_CMD is executed. Remains '1' until W1C by user.<br>0h = Not yet done / not in progress<br>1h = Done  |
| 4   | I2C_OSC_ON           | R     | 0h    | This register field is set to '1' if an EN_OSC_DIY is received.<br>0h = OSC not controlled via I2C<br>1h = OSC unconditionally ON due to I2C command EN_OSC_DIY  |
| 3-0 | USER_NVM_CMD         | R     | 0h    | Commands to enter DIY programming mode and program user NVM space. Always reads as 0.<br>6h = DIS_OSC_DIY<br>7h = CUST_NVM_VERIFY_CMD<br>9h = EN_OSC_DIY<br>Ah = CUST_PROG_CMD                               |

### 7.7.54 POWER\_UP\_STATUS\_REG Register (Offset = 35h) [Reset = 00h]

POWER\_UP\_STATUS\_REG is shown in [Figure 7-70](#) and described in [Table 7-62](#).

Return to the [Summary Table](#).

**Figure 7-70. POWER\_UP\_STATUS\_REG Register**

| 7                     | 6                                  | 5                     | 4     | 3 | 2           | 1 | 0                     |
|-----------------------|------------------------------------|-----------------------|-------|---|-------------|---|-----------------------|
| POWER_UP_F<br>ROM_FSD | POWER_UP_F<br>ROM_EN_PB_<br>VSENSE | COLD_RESET_<br>ISSUED | STATE |   | RETRY_COUNT |   | POWER_UP_F<br>ROM_OFF |
| R/W1C-0h              | R/W1C-0h                           | R/W1C-0h              | R-0h  |   | R-0h        |   | R/W1C-0h              |

**Table 7-62. POWER\_UP\_STATUS\_REG Register Field Descriptions**

| Bit | Field                      | Type  | Reset | Description  |
|-----|----------------------------|-------|-------|--|
| 7   | POWER_UP_FROM_FSD          | R/W1C | 0h    | Is set if ON_REQ was triggered due to FSD<br>0h = No power-up via FSD detected<br>1h = Power-up via FSD detected   |
| 6   | POWER_UP_FROM_EN_PB_VSENSE | R/W1C | 0h    | Is set if ON_REQ was triggered due to EN/PB/VSENSE pin<br>0h = No power-up via pin detected<br>1h = Power-up via pin detected  |
| 5   | COLD_RESET_ISSUED          | R/W1C | 0h    | Is set if we received a COLD_RESET over pin or over I2C<br>0h = No COLD RESET received<br>1h = COLD RESET received either through pin or I2C   |
| 4-3 | STATE                      | R     | 0h    | Indicates the current device state<br>0h = Transition state<br>1h = INITIALIZE<br>2h = STANDBY<br>3h = ACTIVE  |
| 2-1 | RETRY_COUNT                | R     | 0h    | Reads the current retry count in the state machine. If RETRY_COUNT = 3 and is not masked, device does not power up.  |
| 0   | POWER_UP_FROM_OFF          | R/W1C | 0h    | Indicates if we powered up from OFF state (POR was asserted)<br>0h = OFF state not entered since the previous clearing of this bit<br>1h = OFF state was entered since the previous clearing of this bit |

### 7.7.55 SPARE\_2 Register (Offset = 36h) [Reset = 00h]

SPARE\_2 is shown in [Figure 7-71](#) and described in [Table 7-63](#).

Return to the [Summary Table](#).

**Figure 7-71. SPARE\_2 Register**

| 7         | 6         | 5         | 4         | 3         | 2         | 1         | 0         |
|-----------|-----------|-----------|-----------|-----------|-----------|-----------|-----------|
| SPARE_2_1 | SPARE_2_2 | SPARE_2_3 | SPARE_2_4 | SPARE_2_5 | SPARE_2_6 | SPARE_2_7 | SPARE_2_8 |
| R/W-0h    | R/W-0h    | R/W-0h    | R/W-0h    | R/W-0h    | R/W-0h    | R/W-0h    | R/W-0h    |

**Table 7-63. SPARE\_2 Register Field Descriptions**

| Bit | Field     | Type | Reset | Description                     |
|-----|-----------|------|-------|---------------------------------|
| 7   | SPARE_2_1 | R/W  | 0h    | Spare bit in user non-NVM space |
| 6   | SPARE_2_2 | R/W  | 0h    | Spare bit in user non-NVM space |
| 5   | SPARE_2_3 | R/W  | 0h    | Spare bit in user non-NVM space |
| 4   | SPARE_2_4 | R/W  | 0h    | Spare bit in user non-NVM space |
| 3   | SPARE_2_5 | R/W  | 0h    | Spare bit in user non-NVM space |
| 2   | SPARE_2_6 | R/W  | 0h    | Spare bit in user non-NVM space |
| 1   | SPARE_2_7 | R/W  | 0h    | Spare bit in user non-NVM space |
| 0   | SPARE_2_8 | R/W  | 0h    | Spare bit in user non-NVM space |

### 7.7.56 SPARE\_3 Register (Offset = 37h) [Reset = 00h]

SPARE\_3 is shown in [Figure 7-72](#) and described in [Table 7-64](#).

Return to the [Summary Table](#).

**Figure 7-72. SPARE\_3 Register**

|           |   |   |   |   |   |   |   |
|-----------|---|---|---|---|---|---|---|
| 7         | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| SPARE_3_1 |   |   |   |   |   |   |   |
| R/W-0h    |   |   |   |   |   |   |   |

**Table 7-64. SPARE\_3 Register Field Descriptions**

| Bit | Field     | Type | Reset | Description                     |
|-----|-----------|------|-------|---------------------------------|
| 7-0 | SPARE_3_1 | R/W  | 0h    | Spare bit in user non-NVM space |

**7.7.57 FACTORY\_CONFIG\_2 Register (Offset = 41h) [Reset = X]**

FACTORY\_CONFIG\_2 is shown in [Figure 7-73](#) and described in [Table 7-65](#).

Return to the [Summary Table](#).

**Figure 7-73. FACTORY\_CONFIG\_2 Register**

|              |   |          |   |          |          |          |          |
|--------------|---|----------|---|----------|----------|----------|----------|
| 7            | 6 | 5        | 4 | 3        | 2        | 1        | 0        |
| NVM_REVISION |   | RESERVED |   | RESERVED | RESERVED | RESERVED | RESERVED |
| R-X          |   | R-X      |   | R-X      | R-X      | R-X      | R-X      |

**Table 7-65. FACTORY\_CONFIG\_2 Register Field Descriptions**

| Bit | Field        | Type | Reset | Description  |
|-----|--------------|------|-------|--|
| 7-5 | NVM_REVISION | R    | X     | Specifies the version of the NVM configuration Note: This register can be programmed only by the manufacturer.<br>0h = V0<br>1h = V1 ... |
| 4   | RESERVED     | R    | X     | Reserved   |
| 3   | RESERVED     | R    | X     | Reserved   |
| 2   | RESERVED     | R    | X     | Reserved   |
| 1   | RESERVED     | R    | X     | Reserved   |
| 0   | RESERVED     | R    | X     | Reserved   |

## 8 Application and Implementation

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### Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

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### 8.1 Application Information

The following sections provide more detail on the proper utilization of the PMIC. Each orderable part number has unique default non-volatile memory (NVM) settings and the relevant Technical Reference Manual (TRM) for that orderable is available in the product folder, under Technical Documentation. Refer to these TRMs for specific application information. More generic topics and some examples are outlined here.

To help with new designs, a variety of tools and documents are available in the product folder. Some examples are:

- Evaluation module and user guide.
- GUI to communicate with the PMIC
- Schematic and layout checklist
- User's guide describing how to power specific processors and SoCs with the PMIC.
- Technical Reference Manual (TRM) describing the default register settings on each orderable.

### 8.2 Typical Application

The TPS65219 PMIC contains seven regulators; 3 Buck converters and 4 Low Drop-out Regulators (LDOs). In addition to the power resources, it also integrates 3 configurable multi-function pins, 1 GPIO, 2 GPOs and I2C communication making this power management IC a cost and size optimized solution to power multiple processors and SoCs. There are several considerations to take into account when designing the TPS65219 to power a processor and peripherals. The number of regulators needed, the required sequencing, the load current requirements, and the voltage characteristics are all critical in determining the number of supply rails as well as the external components used with it. The following section provides a generic case. For specific cases, refer to the relevant user's guide and TRM based on the orderable part number.

#### 8.2.1 Typical Application Example

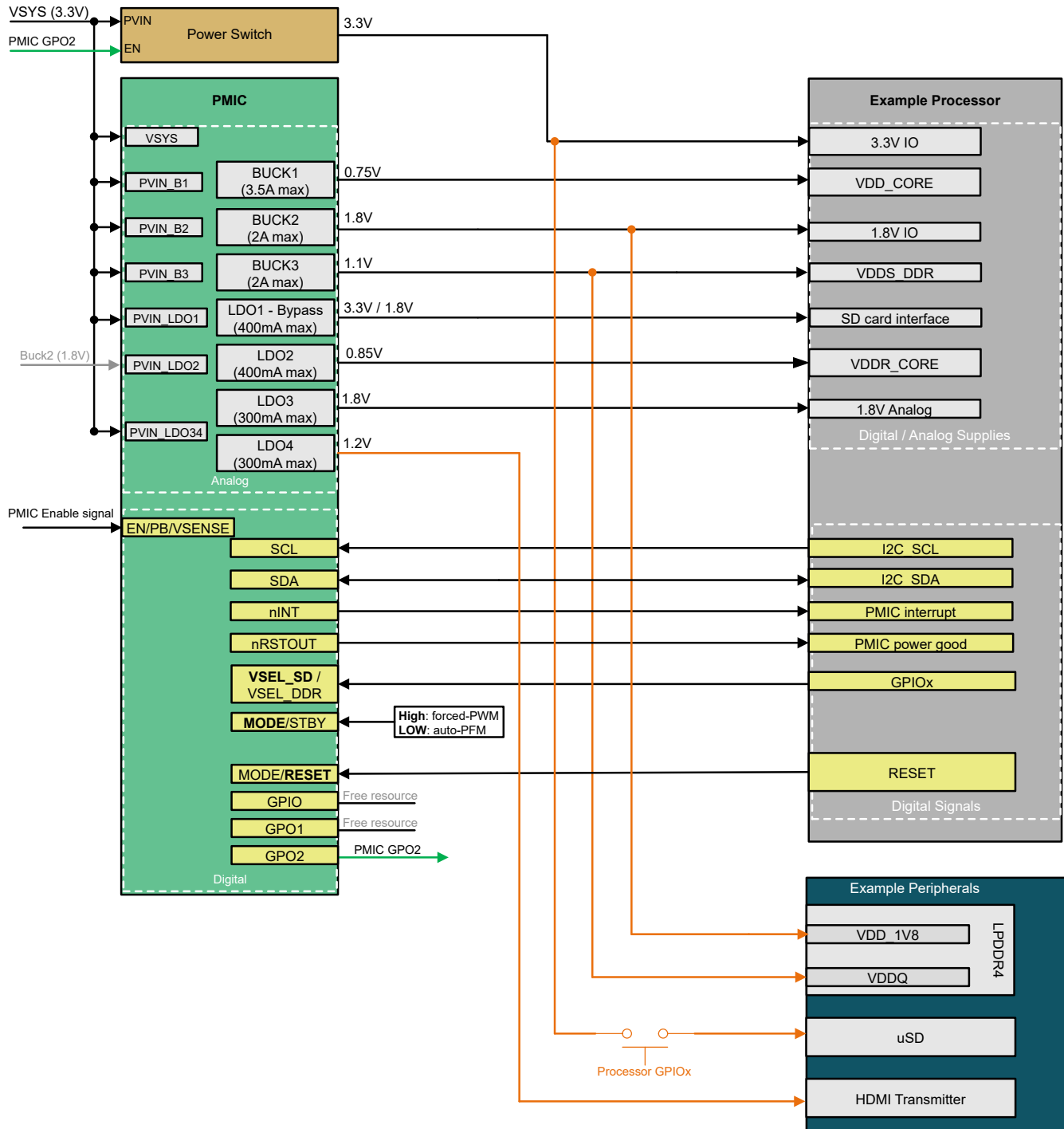
In this example, a single TPS65219 PMIC is used to power a generic processor. This power distribution network (PDN) shows a 3.3V input supply but 5V can be used as well to supply the Bucks and LDO (if not configured as bypass). To reduce power dissipation, the output from one of the PMIC Buck regulators can be used to supply the LDOs if it meets the required headroom and sequence needs. For example, Buck2 (1.8V) is used to supply LDO2 (0.85V). LDO1 is configured as bypass and assigned to supply the SD card interface. The bypass mode allows voltage change between VSET\_LDO1 and 1.8V to meet the SD spec for UHS speed which requires 3.3V to initialize the card before the voltage can be lowered to 1.8V for faster rise/fall time and lower electromagnetic interference. The VSEL\_SD multifunction pin is configurable to trigger the voltage change during operation. Since Buck1 is the regulator with the highest current capabilities, it was assigned to supply the CORE rail of the processor. Each of the Buck regulators have the option to be configured for high bandwidth to support higher load transients and higher total capacitance (local + point of load). Since the PMIC is being supplied by a 3.3V rail, an external load switch is used to supply the 3.3V IO domain on the processor. One of the PMIC GPOs (GPO2) is configured to be part of the power-up/power-down sequence and enables the external power-switch.

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### Note

If an external discrete is used to supply the 3.3V IO, it must be chosen with active discharge so the voltage discharges after the PMIC GPO2 disables it.

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**Figure 8-1. Example Power Map**

### 8.2.2 Design Requirements

The design requirements for the typical application described on this section are outlined below:

- VDD CORE rail requires 0.75V rail with high loadtransient response.
- VDDR CORE rail requires 0.85V.
- Low noise 1.8V required to supply the analog.
- 3.3V and 1.8V required to supply processor IO domains and peripherals.

- uSD card interface requires a rail with 3.3V at startup with dynamic voltage capability to switch from 3.3V to 1.8V and support ultra-high speed (UHS)
- LPDDR4 requires a 1.1V rail.
- HDMI transmitter requires 1.2V rail.

### 8.2.3 Detailed Design Procedure

This section describes the design procedure for each of the power modules integrated in the TPS65219 PMIC. Please note, most of the external component values that are mentioned in this section are based on the typical spec. For minimum and maximum values, refer to the corresponding parameter in the Specifications section.

#### 8.2.3.1 Buck1, Buck2, Buck3 Design Procedure

##### Input Capacitance - Buck1, Buck2, Buck3

Each of the Buck converters require an input capacitor on the corresponding PVIN\_Bx pin. The capacitor value must be selected taking into account the voltage and temperature de-rating. Due to the nature of the switching converter, a low ESR ceramic capacitor is required for best input voltage filtering. The typical recommended capacitance is 4.7uF, 10V capacitor. Higher input capacitance is acceptable if the PCB size allows larger footprint.

##### Output Capacitance - Buck1, Buck2, Buck3

Every Buck output requires a local output capacitor to form the capacitive part of the LC output filter. Ceramic capacitor with X7 temperature coefficient are recommended. Cost optimize for non-automotive applications by using X6 or lower based on the operating temperature. The Buck converters have multiple switching modes and bandwidth configuration that impact the output capacitor selection. The switching mode configuration (BUCK\_FF\_ENABLE) is a global register field that applies to the three Buck converters and must not be changed at any point. The bandwidth selection is an independent register field for each Buck converter. Refer to the Technical Reference Manual (TRM) for the specific orderable part number to identify the NVM configuration and the corresponding output capacitance requirements. [Table 8-1](#) shows the required minimum and maximum capacitance (after derating) for each switching mode and bandwidth configuration. DC bias voltage characteristics of ceramic capacitors, tolerance, aging and temperature effects must be considered. ESR must be 10mΩ or lower.

**Table 8-1. Buck Output Capacitance**

| Switching Mode Selection                          | Bandwidth Selection  | Spec parameter | Capacitance |   |
|---|--|----------------|-------------|---|
|   |  |                | Min         | Max<br>(Includes local + point of load) |
| Register Field:<br>BUCK_FF_ENABLE                 | Register fields:<br>BUCK1_BW_SEL,<br>BUCK2_BW_SEL,<br>BUCK3_BW_SEL |                |             |   |
| Quasi-fixed frequency<br>(auto-PFM or forced-PWM) | Low Bandwidth  | COUT           | 10uF        | 75uF                                    |
|   | High Bandwidth   | COUT_HIGH_BW   | 30uF        | 220uF                                   |

##### Inductor Selection - Buck1, Buck2, Buck3

Internal parameters for the buck converters are optimized for 0.47uH inductor. DCR must be 50mΩ or lower. TI recommends that the selected inductor is rated to support saturation current of at least 7.4A for Buck1 and 5.4A for Buck2/Buck3.

### 8.2.3.2 LDO1, LDO2 Design Procedure

#### Input Capacitance - LDO1, LDO2

LDO inputs require an input decoupling capacitor to minimize input ripple voltage. Using a typical of 2.2 $\mu$ F capacitance for each LDO is recommended. Depending on the input voltage of the LDO, use a 6.3V or higher rated capacitor. The same input capacitance requirements applies when the LDO is configured as LDO, bypass or "load-switch".

#### Output Capacitance - LDO1, LDO2

LDO outputs require an output capacitor to hold up the output voltage during a load step or changes to the input voltage. Using a 2.2 $\mu$ F local capacitance for each LDO output with ESR of 10m $\Omega$  or less is recommended. Local capacitance must not exceed 4 $\mu$ F (after derating). This requirement excludes any capacitance seen at the load and only refers to the capacitance seen close to the device. The total capacitance (local + point of load) that each LDO supports depends on the NVM configuration. [Table 8-2](#) shows the maximum total output capacitance allowed based on the rail configuration. Refer to the Technical Reference Manual (TRM) for the specific orderable part number to identify the LDO configuration based on the register settings and the applicable max total capacitance.

**Table 8-2. LDO1, LDO2 Output Capacitance**

| Register setting |                 | LDO config  | Max total capacitance (2.2 $\mu$ F local + point of load) |
|------------------|-----------------|-------------|---|
| LDOx_LSW_CONFIG  | LDOx_BYP_CONFIG |             |   |
| 0                | 0               | LDO         | 20 $\mu$ F  |
| 0                | 1               | Bypass      | 50 $\mu$ F  |
| 1                | X               | Load-switch | 50 $\mu$ F  |

### 8.2.3.3 LDO3, LDO4 Design Procedure

#### Input Capacitance - LDO3, LDO4

The input supply pin for LDO3 and LDO4 require an input decoupling capacitor to minimize input ripple voltage. These two LDOs share the same input supply pin. Using a minimum of 4.7 $\mu$ F input capacitance is recommended. Depending on the input voltage of the LDO, use a 6.3V or higher rated capacitor. The same input capacitance requirements applies when the LDO is configured as LDO or load-switch.

#### Output Capacitance - LDO3, LDO4

LDO outputs require an output capacitor to hold up the output voltage during a load step or changes to the input voltage. Using a 2.2 $\mu$ F local capacitance for each LDO output with ESR of 10m $\Omega$  or less is recommended. Local capacitance must not exceed 4 $\mu$ F (after derating). This requirement excludes any capacitance seen at the load and only refers to the capacitance seen close to the device. The total capacitance (local + point of load) that each LDO supports depends on the NVM configuration. [Table 8-3](#) shows the maximum total output capacitance allowed. Refer to the Technical Reference Manual (TRM) for the specific orderable part number to identify the LDO configuration based on the register settings and the applicable maximum total capacitance.

**Table 8-3. LDO3, LDO4 output capacitance**

| Register setting  | LDO ramp config | Max total capacitance (2.2 $\mu$ F local + point of load) |
|-------------------|-----------------|---|
| LDOx_SLOW_PU_RAMP |                 |   |
| 0                 | fast ramp       | 15 $\mu$ F  |
| 1                 | slow ramp       | 30 $\mu$ F  |

### 8.2.3.4 VSYS, VDD1P8

The VSYS pin provides power to the internal VDD1P8 LDO and other internal functions. This pin requires a typical of 2.2uF ceramic capacitor. Increase the input capacitance without any limit for better input-voltage filtering. On a typical application, this pin is connected to the same pre-regulator that supplies the PVIN\_Bx pins.

VDD1P8 in an internal reference LDO and must not have any load. This pin requires a 2.2uF ceramic capacitor.

### 8.2.3.5 Digital Signals Design Procedure

This section describes the external connections required for the digital pins. A VIO supply of 3.3V or 1.8V supply is commonly used as the voltage level for the digital signals that require an external pull-up. However, the device also supports any higher voltage up to the maximum spec. The VIO supply for the digital pins on the PMIC must be the same as the IO domain for the digital signal that is connected to on the processor. 100kΩ is the recommended pull-up resistor for EN/PB/VSENSE. Calculate the pull-up resistor for I2C pins based on system requirements. 10kΩ is recommended for all other digital pins.

If GPIO, GPO1 or GPO2 is assigned to the first slot of the power-up sequence to enable an external discrete, pull the pin up to VSYS.

Externally drive the EN/PB/VSENSE pin to enable or disable the PMIC. If the application does not have an external signal dedicated to drive this pin, pull the pin up to VSYS.

#### Note

Driving the EN/PB/VSENSE pin with an external signal is needed to wake-up the PMIC after an I2C OFF request is sent by I2C (I2C\_OFF\_REQ). If an OFF request is sent by I2C and the EN/PB/VSENSE is not driven by an external signal, a power cycle on VSYS must be performed to transfer the PMIC from Initialize state to Active.

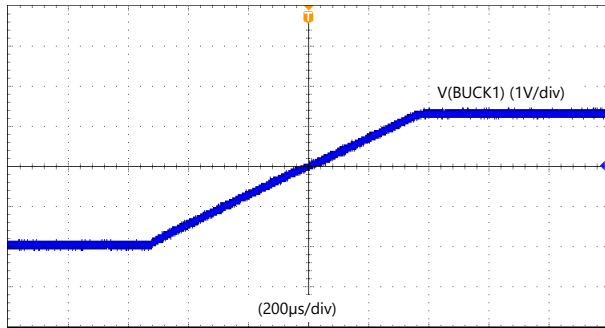
**Table 8-4. Digital Signals Requirements**

| Digital Pin        | External Connection  |
|--------------------|--|
| nINT               | Open-drain output. Requires external pull-up.  |
| nRSTOUT            | Open-drain output. Requires external pull-up.  |
| EN/PB/VSENSE       | When configured as EN, drive this signal with external logic to enable or disable the PMIC, or pull this pin up to VSYS.<br>When configured as PB, this signal requires a pull-up resistor connected to the VSYS pin. Push-button is optional.<br>When configured as VSENSE, this signal requires an external resistor divider to monitor the pre-regulator. |
| SDA                | I2C clock signal. Requires external pull-up.   |
| SCL                | I2C data signal. Requires external pull-up.  |
| GPIO               | When configured as GPIO (for multi-PMIC), this pin shares the external pull-up resistor with the second TPS65219 PMIC.<br>When configured as GPO (for single PMIC), requires external pull-up.   |
| GPO1               | Open-drain general purpose output. Requires external pull-up.  |
| GPO2               | Open-drain general purpose output. Requires external pull-up.  |
| VSEL_SD / VSEL_DDR | Input digital pin. The initial state (pull-up or pull-down) must be set before the assigned PMIC rail ramps up. For example, if this pin is used to set the voltage on LDO1, the state must be set before LDO1 powers up.  |
| MODE / STBY        | Input digital pin. The initial state (pull-up or pull-down) must be set before the power-up sequence is complete.  |

**Table 8-4. Digital Signals Requirements (continued)**

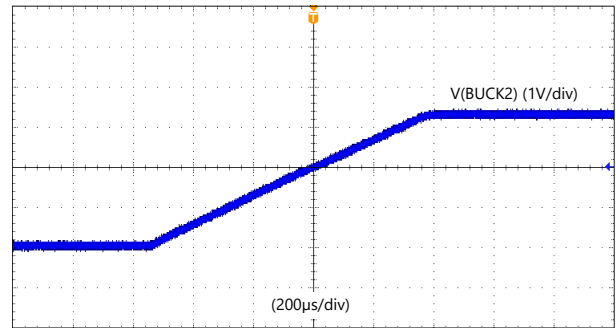
| Digital Pin  | External Connection   |
|--------------|---|
| MODE / RESET | Input digital pin. The initial state (pull-up or pull-down) must be set before the power-up sequence is complete. |

**8.2.4 Application Curves**



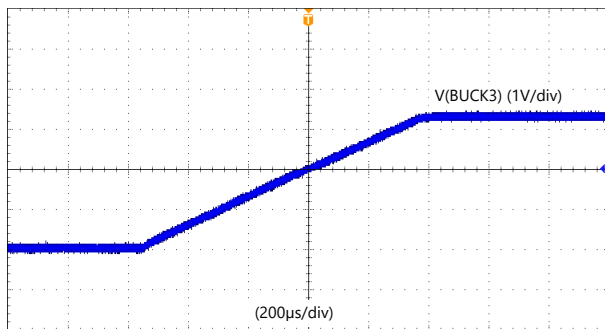
$V_{IN} = 5.0V$        $V_{OUT} = 3.3V$        $T_A = 25\text{ }^\circ\text{C}$   
 Forced-PWM / High       $I_{out} = 1A$        $C_{OUT\_total} = 57\mu F$   
 Bandwidth

**Figure 8-2. Buck1 Ramp**



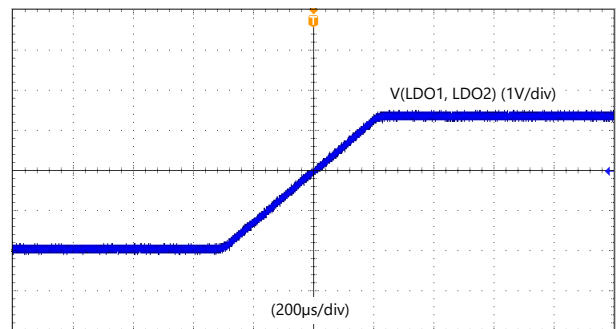
$V_{IN} = 5.0V$        $V_{OUT} = 3.3V$        $T_A = 25\text{ }^\circ\text{C}$   
 Forced-PWM / High       $I_{out} = 1A$        $C_{OUT\_total} = 57\mu F$   
 Bandwidth

**Figure 8-3. Buck2 Ramp**



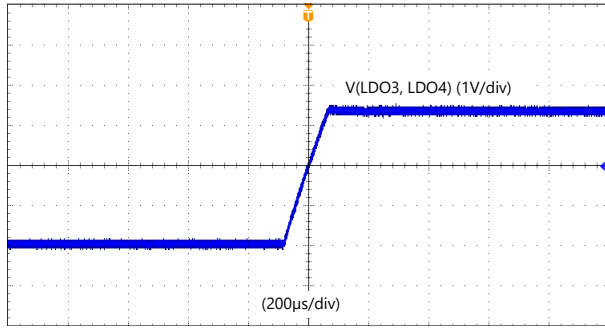
$V_{IN} = 5.0V$        $V_{OUT} = 3.3V$        $T_A = 25\text{ }^\circ\text{C}$   
 Forced-PWM / High       $I_{out} = 1A$        $C_{OUT\_total} = 57\mu F$   
 Bandwidth

**Figure 8-4. Buck3 Ramp**



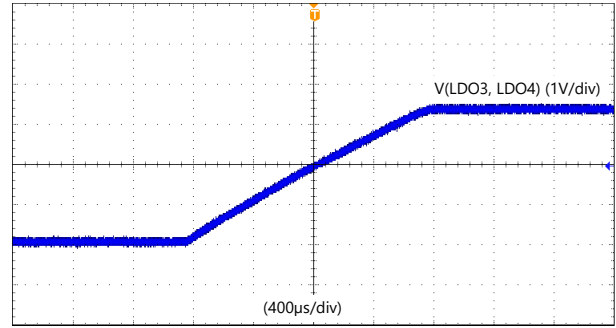
$V_{IN} = 5.0V$        $V_{OUT} = 3.3V$        $T_A = 25\text{ }^\circ\text{C}$   
 LDO mode       $I_{out} = 400mA$        $C_{OUT\_total} = 10\mu F$

**Figure 8-5. LDO1, LDO2 Ramp**



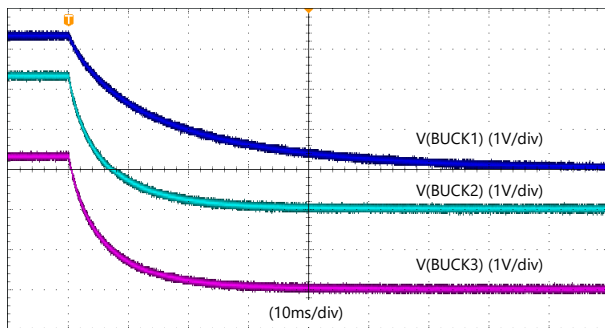
$V_{IN} = 5.0V$        $V_{OUT} = 3.3V$        $T_A = 25\text{ }^\circ\text{C}$   
 LDO mode / Fast ramp       $I_{out} = 300mA$        $C_{OUT\_total} = 10\mu F$

**Figure 8-6. LDO3, LDO4 Fast Ramp**



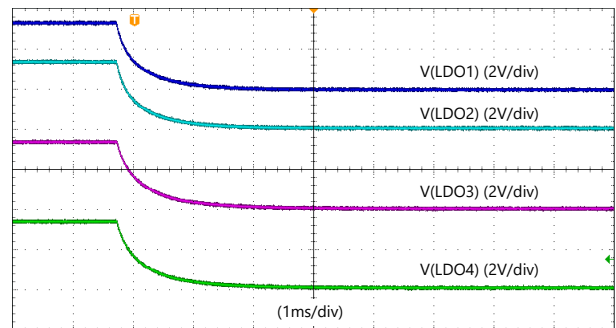
$V_{IN} = 5.0V$        $V_{OUT} = 3.3V$        $T_A = 25\text{ }^\circ\text{C}$   
 LDO mode / Slow ramp       $I_{out} = 300mA$        $C_{OUT\_total} = 10\mu F$

**Figure 8-7. LDO3, LDO4 Slow Ramp**



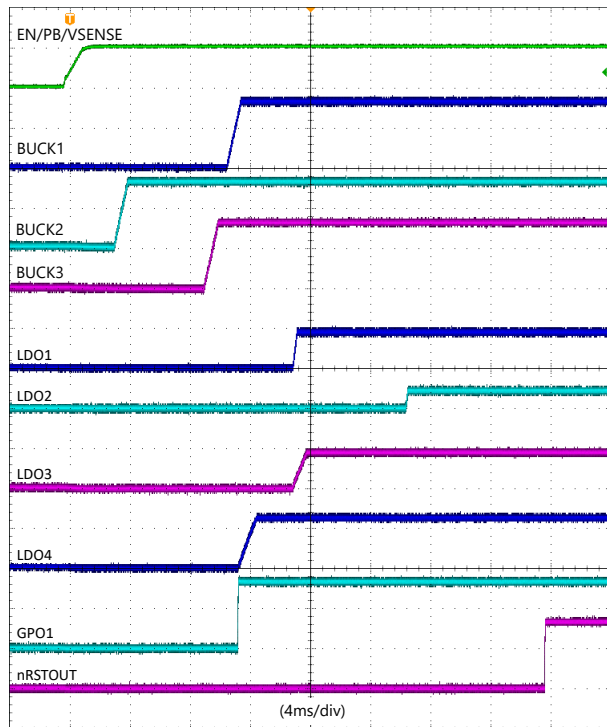
$V_{IN} = 5.0V$        $V_{OUT} = 3.3V$        $T_A = 25\text{ }^\circ\text{C}$   
 Forced-PWM / High Bandwidth      no load       $C_{OUT\_total} = 57\mu F$

**Figure 8-8. Bucks Discharge**



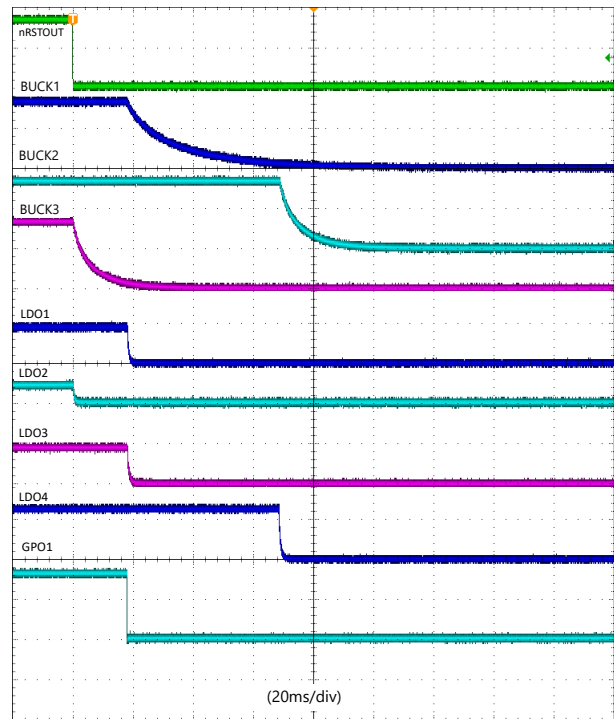
$V_{IN} = 5.0V$        $V_{OUT} = 3.3V$        $T_A = 25\text{ }^\circ\text{C}$   
 LDO mode      no load       $C_{OUT\_total} = 2.2\mu F$

**Figure 8-9. LDOs Discharge**



| Slot# | Duration | Assigned Rail             |
|-------|----------|---------------------------|
| 0     | 1.5ms    | BUCK2                     |
| 1     | 0ms      |                           |
| 2     | 3 ms     | LDO1 / LDO3 / LDO4 / GPO1 |
| 3     | 1.5ms    |                           |
| 4     | 1.5ms    | BUCK3                     |
| 5     | 1.5ms    | BUCK1                     |
| 6     | 1.5ms    | LDO2                      |
| 7     | 10ms     |                           |
| 8     | 1.5ms    |                           |
| 9     | 10ms     | nRSTOUT                   |
| 10-15 | 0ms      |                           |

**Figure 8-10. Configurable Power-up Sequence - Example**



| Slot# | Duration | Assigned Rail              |
|-------|----------|----------------------------|
| 0     | 10ms     | nRSTOUT / BUCK3 / LDO2     |
| 1     | 0ms      |                            |
| 2     | 10ms     | BUCK1 / LDO1 / LDO3 / GPO1 |
| 3     | 0ms      |                            |
| 4     | 10ms     | BUCK2 / LDO4               |
| 5-15  | 0ms      |                            |

**Figure 8-11. Configurable Power-Down sequence - Example**

### 8.3 Power Supply Recommendations

The device is designed to operate with an input voltage supply range between 2.5V and 5.5V. Examples of input supplies include a single cell Li-Ion battery, two primary cells or a regulated pre-regulator. The voltage headroom required for each of the PMIC regulators must be taken into account when defining selecting the supply voltage. For example, if the Bucks require 700mV head room and the output voltage is configured as 3.3V, then the input supply must be at least 4V to allow sufficient headroom. Design the resistance of the input supply rail low enough such that the input current transient does not cause too high of a drop in the device supply voltage. This drop has the ability to cause a false UVLO fault triggering. If the input supply is located more than a few inches from the device, consider additional bulk capacitance in addition to the ceramic bypass capacitors. An electrolytic capacitor with a value of 47µF is a typical choice. When using a pre-regulator to supply the PMIC, it is recommended to select the pre-regulator without active discharge to hold the voltage at the input of the PMIC for as long as possible during a uncontrolled power-down.

**CAUTION**

Sequencing and Voltage requirements: The voltage on PVIN\_Bx, and PVIN\_LDOx must not exceed VSYS. The Pull-up supply for the digital signals must not exceed VSYS at any point.

## 8.4 Layout

### 8.4.1 Layout Guidelines

For all switching power supplies, the layout is an important step in the design. If the layout is not carefully done, the regulators' stability and EMI is impacted. Therefore, use wide and short traces for the main current path and for the power ground tracks. The input capacitors, output capacitors, and inductors must be placed as close as possible to the device. The output capacitors must have a low impedance to ground. Use multiple VIAS (at least three) directly at the ground landing pad of the capacitor. Here are some layout guidelines:

- **PVIN\_Bx:** Place the input capacitor as close to the IC as allowed by the layout DRC rules. Any extra parasitic inductance between the input cap and the PVIN\_Bx pin increases the voltage spike. TI recommends to have wide a short trace or polygon to help minimize trace inductance. Do not route any sensitive signals close to the input cap and the device pin as this node has high frequency switching currents. Add 3-4 vias per amp of current on the GND pads for each DCDC. If the space is limited and does not allow to place the input capacitors on the same layer as the PMIC, then place the input capacitors on the opposite layer with VIAS, close to the IC, and add a small input capacitor (0.1uF) on the same layer as the PMIC. This small capacitor must be placed close to the PVIN\_Bx pin.
- **LX\_Bx:** Place the inductor close to the PMIC without compromising the PVIN input caps and use short a wide traces or polygons to connect the pin to the inductor. Do not route any sensitive signals close to this node. The inductor must be placed in the same layer as the IC to prevent having to use VIAS in the SW node. Since the SW-node voltage swings from the input voltage to ground with very fast rise and fall times, this node is the main generator of EMI. If needed, to reduce EMI, add a RC snubber to the SW node.
- **FB\_Bx:** Route each of the FB\_Bx pins as a trace to the output capacitor. Do not extend the output voltage polygon to the FB\_Bx pin as this pin requires to be routed as a trace. The trace resistance from the output capacitor to the FB\_Bx pin must be less than 1Ω. The TPS65219 does not support remote sensing so the FB\_Bx pins must be connected to the local capacitor of the PMIC. Avoid routing the FB\_Bx close to any noisy signals such as the switch node or under the inductor to avoid coupling. If space is a constraint, route the FB\_Bx pin through an inner layer. See example layout.
- **Bucks Cout:** The local output capacitors must be placed as close to the inductor as possible to minimize electromagnetic emissions.
- **PVIN\_LDOx:** Place the input capacitor as close as possible to the PVIN\_LDOx pin.
- **VLDOx:** Place the output capacitor close to the VLDOx pin. For the LDO regulators, the feedback connection is internal. Therefore, keep the PCB resistance between LDO output and target load in the range of the acceptable voltage, IR, drop for LDOs.
- **VSYS:** Connect VSYS directly to a quiet system voltage node. Place the decoupling capacitor as close as possible to the VSYS pin.
- **VDD1P8:** Place the 2.2uF cap as close as possible to the VDD1P8 pin. This capacitor needs to be placed in the same layer as the IC. Use two to three VIAS to connect the GND side of the capacitor to the GND plane of the PCB.
- **Power Pad:** The thermal pad must be connected to the PCB ground plane with a minimum of nine VIAS.
- **AGND:** Do not connect AGND to the power pad (or thermal pad). The AGDN pin must be connected to the PCB ground planes through a VIA . Keep the trace from the AGDN pin to the VIA short.



## 9 Device and Documentation Support

TI offers an extensive line of development tools. Tools and software to evaluate the performance of the device, generate code, and develop solutions are listed below.

### 9.1 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on [ti.com](http://ti.com). Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

### 9.2 Support Resources

[TI E2E™ support forums](#) are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's [Terms of Use](#).

### 9.3 Trademarks

TI E2E™ is a trademark of Texas Instruments.  
All trademarks are the property of their respective owners.

### 9.4 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

### 9.5 Glossary

[TI Glossary](#) This glossary lists and explains terms, acronyms, and definitions.

## 10 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

| <b>Changes from Revision C (April 2025) to Revision D (April 2026)</b>                        | <b>Page</b> |
|---|-------------|
| • Updated table to include newly released Orderable Part Number (OPN).....                    | 3           |
| • Updated wording from "Voltage by which may PVIN exceed VSYS" to "Voltage differential"..... | 8           |

| <b>Changes from Revision B (June 2024) to Revision C (April 2025)</b>                     | <b>Page</b> |
|---|-------------|
| • Updated Packaging Information table to include information on the RSM and RHB OPNs..... | 1           |
| • Updated table to include newly released OPNs.....                                       | 3           |

## 11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

**PACKAGING INFORMATION**

| Orderable part number          | Status<br>(1) | Material type<br>(2) | Package   Pins  | Package qty   Carrier | RoHS<br>(3) | Lead finish/<br>Ball material<br>(4) | MSL rating/<br>Peak reflow<br>(5) | Op temp (°C) | Part marking<br>(6) |
|--------------------------------|---------------|----------------------|-----------------|-----------------------|-------------|--------------------------------------|-----------------------------------|--------------|---------------------|
| <a href="#">TPS6521901RHBR</a> | Active        | Production           | VQFN (RHB)   32 | 3000   LARGE T&R      | Yes         | NIPDAU                               | Level-1-260C-UNLIM                | -40 to 105   | 65219<br>NVM 01     |
| TPS6521901RHBR.A               | Active        | Production           | VQFN (RHB)   32 | 3000   LARGE T&R      | Yes         | NIPDAU                               | Level-1-260C-UNLIM                | -40 to 105   | 65219<br>NVM 01     |
| <a href="#">TPS6521901RSMR</a> | Active        | Production           | VQFN (RSM)   32 | 3000   LARGE T&R      | Yes         | NIPDAU                               | Level-1-260C-UNLIM                | -40 to 105   | 65219<br>NVM 01     |
| TPS6521901RSMR.A               | Active        | Production           | VQFN (RSM)   32 | 3000   LARGE T&R      | Yes         | NIPDAU                               | Level-1-260C-UNLIM                | -40 to 105   | 65219<br>NVM 01     |
| <a href="#">TPS6521902RHBR</a> | Active        | Production           | VQFN (RHB)   32 | 3000   LARGE T&R      | Yes         | NIPDAU                               | Level-1-260C-UNLIM                | -40 to 105   | 65219<br>NVM 02     |
| TPS6521902RHBR.A               | Active        | Production           | VQFN (RHB)   32 | 3000   LARGE T&R      | Yes         | NIPDAU                               | Level-1-260C-UNLIM                | -40 to 105   | 65219<br>NVM 02     |
| <a href="#">TPS6521902RSMR</a> | Active        | Production           | VQFN (RSM)   32 | 3000   LARGE T&R      | Yes         | NIPDAU                               | Level-1-260C-UNLIM                | -40 to 105   | 65219<br>NVM 02     |
| TPS6521902RSMR.A               | Active        | Production           | VQFN (RSM)   32 | 3000   LARGE T&R      | Yes         | NIPDAU                               | Level-1-260C-UNLIM                | -40 to 105   | 65219<br>NVM 02     |
| <a href="#">TPS6521903RHBR</a> | Active        | Production           | VQFN (RHB)   32 | 3000   LARGE T&R      | Yes         | NIPDAU                               | Level-1-260C-UNLIM                | -40 to 105   | 65219<br>NVM 03     |
| TPS6521903RHBR.A               | Active        | Production           | VQFN (RHB)   32 | 3000   LARGE T&R      | Yes         | NIPDAU                               | Level-1-260C-UNLIM                | -40 to 105   | 65219<br>NVM 03     |
| <a href="#">TPS6521903RSMR</a> | Active        | Production           | VQFN (RSM)   32 | 3000   LARGE T&R      | Yes         | NIPDAU                               | Level-1-260C-UNLIM                | -40 to 105   | 65219<br>NVM 03     |
| TPS6521903RSMR.A               | Active        | Production           | VQFN (RSM)   32 | 3000   LARGE T&R      | Yes         | NIPDAU                               | Level-1-260C-UNLIM                | -40 to 105   | 65219<br>NVM 03     |
| <a href="#">TPS6521904RHBR</a> | Active        | Production           | VQFN (RHB)   32 | 3000   LARGE T&R      | Yes         | NIPDAU                               | Level-1-260C-UNLIM                | -40 to 105   | 65219<br>NVM 04     |
| TPS6521904RHBR.A               | Active        | Production           | VQFN (RHB)   32 | 3000   LARGE T&R      | Yes         | NIPDAU                               | Level-1-260C-UNLIM                | -40 to 105   | 65219<br>NVM 04     |
| <a href="#">TPS6521904RSMR</a> | Active        | Production           | VQFN (RSM)   32 | 3000   LARGE T&R      | Yes         | NIPDAU                               | Level-1-260C-UNLIM                | -40 to 105   | 65219<br>NVM 04     |
| TPS6521904RSMR.A               | Active        | Production           | VQFN (RSM)   32 | 3000   LARGE T&R      | Yes         | NIPDAU                               | Level-1-260C-UNLIM                | -40 to 105   | 65219<br>NVM 04     |

| Orderable part number          | Status<br>(1) | Material type<br>(2) | Package   Pins  | Package qty   Carrier | RoHS<br>(3) | Lead finish/<br>Ball material<br>(4) | MSL rating/<br>Peak reflow<br>(5) | Op temp (°C) | Part marking<br>(6) |
|--------------------------------|---------------|----------------------|-----------------|-----------------------|-------------|--------------------------------------|-----------------------------------|--------------|---------------------|
| <a href="#">TPS6521906RSMR</a> | Active        | Production           | VQFN (RSM)   32 | 3000   LARGE T&R      | Yes         | NIPDAU                               | Level-1-260C-UNLIM                | -40 to 105   | 65219<br>NVM 06     |
| TPS6521906RSMR.A               | Active        | Production           | VQFN (RSM)   32 | 3000   LARGE T&R      | Yes         | NIPDAU                               | Level-1-260C-UNLIM                | -40 to 105   | 65219<br>NVM 06     |
| <a href="#">TPS6521907RHBR</a> | Active        | Production           | VQFN (RHB)   32 | 3000   LARGE T&R      | Yes         | NIPDAU                               | Level-1-260C-UNLIM                | -40 to 105   | 65219<br>NVM 07     |
| TPS6521907RHBR.A               | Active        | Production           | VQFN (RHB)   32 | 3000   LARGE T&R      | Yes         | NIPDAU                               | Level-1-260C-UNLIM                | -40 to 105   | 65219<br>NVM 07     |
| <a href="#">TPS6521908RHBR</a> | Active        | Production           | VQFN (RHB)   32 | 3000   LARGE T&R      | Yes         | NIPDAU                               | Level-1-260C-UNLIM                | -40 to 105   | 65219<br>NVM 08     |
| TPS6521908RHBR.A               | Active        | Production           | VQFN (RHB)   32 | 3000   LARGE T&R      | Yes         | NIPDAU                               | Level-1-260C-UNLIM                | -40 to 105   | 65219<br>NVM 08     |
| <a href="#">TPS6521909RSMR</a> | Active        | Production           | VQFN (RSM)   32 | 3000   LARGE T&R      | Yes         | NIPDAU                               | Level-1-260C-UNLIM                | -40 to 105   | 65219<br>NVM 09     |
| TPS6521909RSMR.A               | Active        | Production           | VQFN (RSM)   32 | 3000   LARGE T&R      | Yes         | NIPDAU                               | Level-1-260C-UNLIM                | -40 to 105   | 65219<br>NVM 09     |
| <a href="#">TPS652190CRHBR</a> | Active        | Production           | VQFN (RHB)   32 | 3000   LARGE T&R      | Yes         | NIPDAU                               | Level-1-260C-UNLIM                | -40 to 105   | 65219<br>NVM 0C     |
| TPS652190CRHBR.A               | Active        | Production           | VQFN (RHB)   32 | 3000   LARGE T&R      | Yes         | NIPDAU                               | Level-1-260C-UNLIM                | -40 to 105   | 65219<br>NVM 0C     |
| <a href="#">TPS6521910RSMR</a> | Active        | Production           | VQFN (RSM)   32 | 3000   LARGE T&R      | Yes         | NIPDAU                               | Level-1-260C-UNLIM                | -40 to 105   | 65219<br>NVM 10     |
| TPS6521910RSMR.A               | Active        | Production           | VQFN (RSM)   32 | 3000   LARGE T&R      | Yes         | NIPDAU                               | Level-1-260C-UNLIM                | -40 to 105   | 65219<br>NVM 10     |
| <a href="#">TPS6521914RHBR</a> | Active        | Production           | VQFN (RHB)   32 | 3000   LARGE T&R      | Yes         | NIPDAU                               | Level-1-260C-UNLIM                | -40 to 105   | 65219<br>NVM 14     |
| <a href="#">TPS6521940RSMR</a> | Active        | Production           | VQFN (RSM)   32 | 3000   LARGE T&R      | Yes         | NIPDAU                               | Level-1-260C-UNLIM                | -40 to 105   | 65219<br>NVM 40     |
| TPS6521940RSMR.A               | Active        | Production           | VQFN (RSM)   32 | 3000   LARGE T&R      | Yes         | NIPDAU                               | Level-1-260C-UNLIM                | -40 to 105   | 65219<br>NVM 40     |

(1) **Status:** For more details on status, see our [product life cycle](#).

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

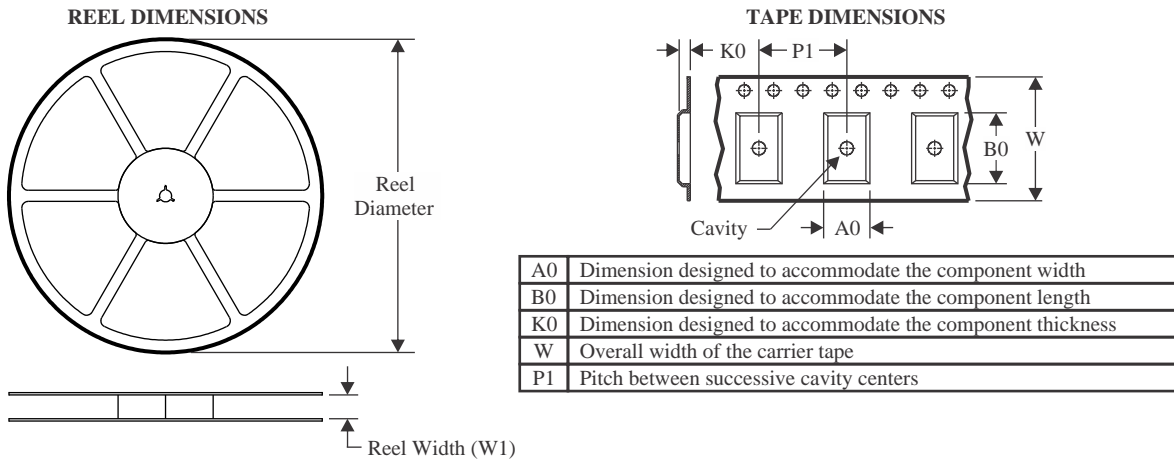
**OTHER QUALIFIED VERSIONS OF TPS65219 :**

- Automotive : [TPS65219-Q1](#)

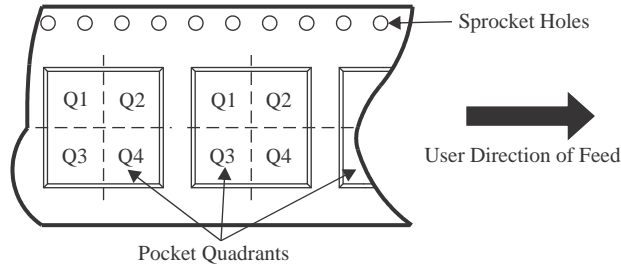
NOTE: Qualified Version Definitions:

- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects

## TAPE AND REEL INFORMATION

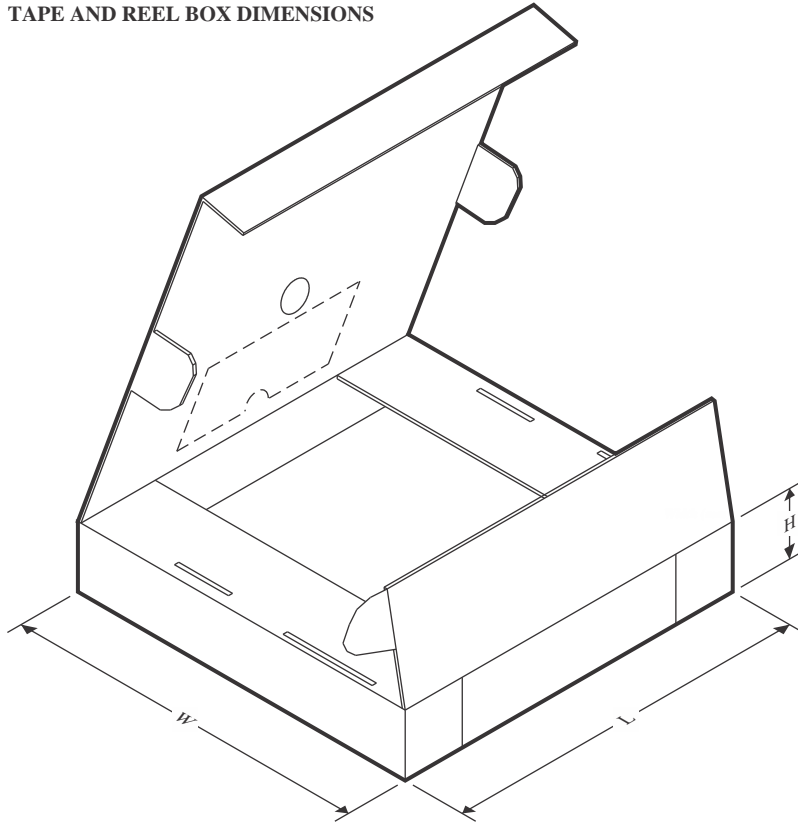


### QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



\*All dimensions are nominal

| Device         | Package Type | Package Drawing | Pins | SPQ  | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|----------------|--------------|-----------------|------|------|--------------------|--------------------|---------|---------|---------|---------|--------|---------------|
| TPS6521901RHBR | VQFN         | RHB             | 32   | 3000 | 330.0              | 12.4               | 5.3     | 5.3     | 1.1     | 8.0     | 12.0   | Q2            |
| TPS6521901RSMR | VQFN         | RSM             | 32   | 3000 | 330.0              | 12.4               | 4.25    | 4.25    | 1.15    | 8.0     | 12.0   | Q2            |
| TPS6521902RHBR | VQFN         | RHB             | 32   | 3000 | 330.0              | 12.4               | 5.3     | 5.3     | 1.1     | 8.0     | 12.0   | Q2            |
| TPS6521902RSMR | VQFN         | RSM             | 32   | 3000 | 330.0              | 12.4               | 4.25    | 4.25    | 1.15    | 8.0     | 12.0   | Q2            |
| TPS6521903RHBR | VQFN         | RHB             | 32   | 3000 | 330.0              | 12.4               | 5.3     | 5.3     | 1.1     | 8.0     | 12.0   | Q2            |
| TPS6521903RSMR | VQFN         | RSM             | 32   | 3000 | 330.0              | 12.4               | 4.25    | 4.25    | 1.15    | 8.0     | 12.0   | Q2            |
| TPS6521904RHBR | VQFN         | RHB             | 32   | 3000 | 330.0              | 12.4               | 5.3     | 5.3     | 1.1     | 8.0     | 12.0   | Q2            |
| TPS6521904RSMR | VQFN         | RSM             | 32   | 3000 | 330.0              | 12.4               | 4.25    | 4.25    | 1.15    | 8.0     | 12.0   | Q2            |
| TPS6521906RSMR | VQFN         | RSM             | 32   | 3000 | 330.0              | 12.4               | 4.25    | 4.25    | 1.15    | 8.0     | 12.0   | Q2            |
| TPS6521907RHBR | VQFN         | RHB             | 32   | 3000 | 330.0              | 12.4               | 5.3     | 5.3     | 1.1     | 8.0     | 12.0   | Q2            |
| TPS6521908RHBR | VQFN         | RHB             | 32   | 3000 | 330.0              | 12.4               | 5.3     | 5.3     | 1.1     | 8.0     | 12.0   | Q2            |
| TPS6521909RSMR | VQFN         | RSM             | 32   | 3000 | 330.0              | 12.4               | 4.25    | 4.25    | 1.15    | 8.0     | 12.0   | Q2            |
| TPS652190CRHBR | VQFN         | RHB             | 32   | 3000 | 330.0              | 12.4               | 5.3     | 5.3     | 1.1     | 8.0     | 12.0   | Q2            |
| TPS6521910RSMR | VQFN         | RSM             | 32   | 3000 | 330.0              | 12.4               | 4.25    | 4.25    | 1.15    | 8.0     | 12.0   | Q2            |
| TPS6521914RHBR | VQFN         | RHB             | 32   | 3000 | 330.0              | 12.4               | 5.3     | 5.3     | 1.1     | 8.0     | 12.0   | Q2            |
| TPS6521940RSMR | VQFN         | RSM             | 32   | 3000 | 330.0              | 12.4               | 4.25    | 4.25    | 1.15    | 8.0     | 12.0   | Q2            |

**TAPE AND REEL BOX DIMENSIONS**


\*All dimensions are nominal

| Device         | Package Type | Package Drawing | Pins | SPQ  | Length (mm) | Width (mm) | Height (mm) |
|----------------|--------------|-----------------|------|------|-------------|------------|-------------|
| TPS6521901RHBR | VQFN         | RHB             | 32   | 3000 | 367.0       | 367.0      | 35.0        |
| TPS6521901RSMR | VQFN         | RSM             | 32   | 3000 | 367.0       | 367.0      | 35.0        |
| TPS6521902RHBR | VQFN         | RHB             | 32   | 3000 | 367.0       | 367.0      | 35.0        |
| TPS6521902RSMR | VQFN         | RSM             | 32   | 3000 | 367.0       | 367.0      | 35.0        |
| TPS6521903RHBR | VQFN         | RHB             | 32   | 3000 | 367.0       | 367.0      | 35.0        |
| TPS6521903RSMR | VQFN         | RSM             | 32   | 3000 | 367.0       | 367.0      | 35.0        |
| TPS6521904RHBR | VQFN         | RHB             | 32   | 3000 | 367.0       | 367.0      | 35.0        |
| TPS6521904RSMR | VQFN         | RSM             | 32   | 3000 | 367.0       | 367.0      | 35.0        |
| TPS6521906RSMR | VQFN         | RSM             | 32   | 3000 | 367.0       | 367.0      | 35.0        |
| TPS6521907RHBR | VQFN         | RHB             | 32   | 3000 | 367.0       | 367.0      | 35.0        |
| TPS6521908RHBR | VQFN         | RHB             | 32   | 3000 | 367.0       | 367.0      | 35.0        |
| TPS6521909RSMR | VQFN         | RSM             | 32   | 3000 | 367.0       | 367.0      | 35.0        |
| TPS652190CRHBR | VQFN         | RHB             | 32   | 3000 | 367.0       | 367.0      | 35.0        |
| TPS6521910RSMR | VQFN         | RSM             | 32   | 3000 | 367.0       | 367.0      | 35.0        |
| TPS6521914RHBR | VQFN         | RHB             | 32   | 3000 | 360.0       | 360.0      | 36.0        |
| TPS6521940RSMR | VQFN         | RSM             | 32   | 3000 | 367.0       | 367.0      | 35.0        |

## GENERIC PACKAGE VIEW

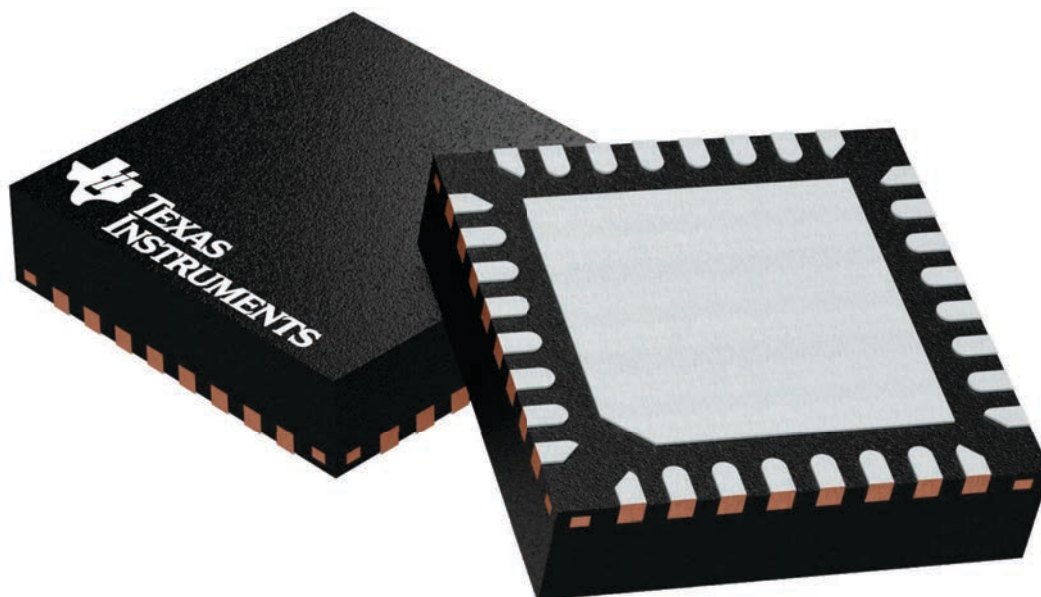
**RSM 32**

**VQFN - 1 mm max height**

4 x 4, 0.4 mm pitch

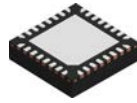
PLASTIC QUAD FLATPACK - NO LEAD

This image is a representation of the package family, actual package may vary.  
Refer to the product data sheet for package details.



4224982/A

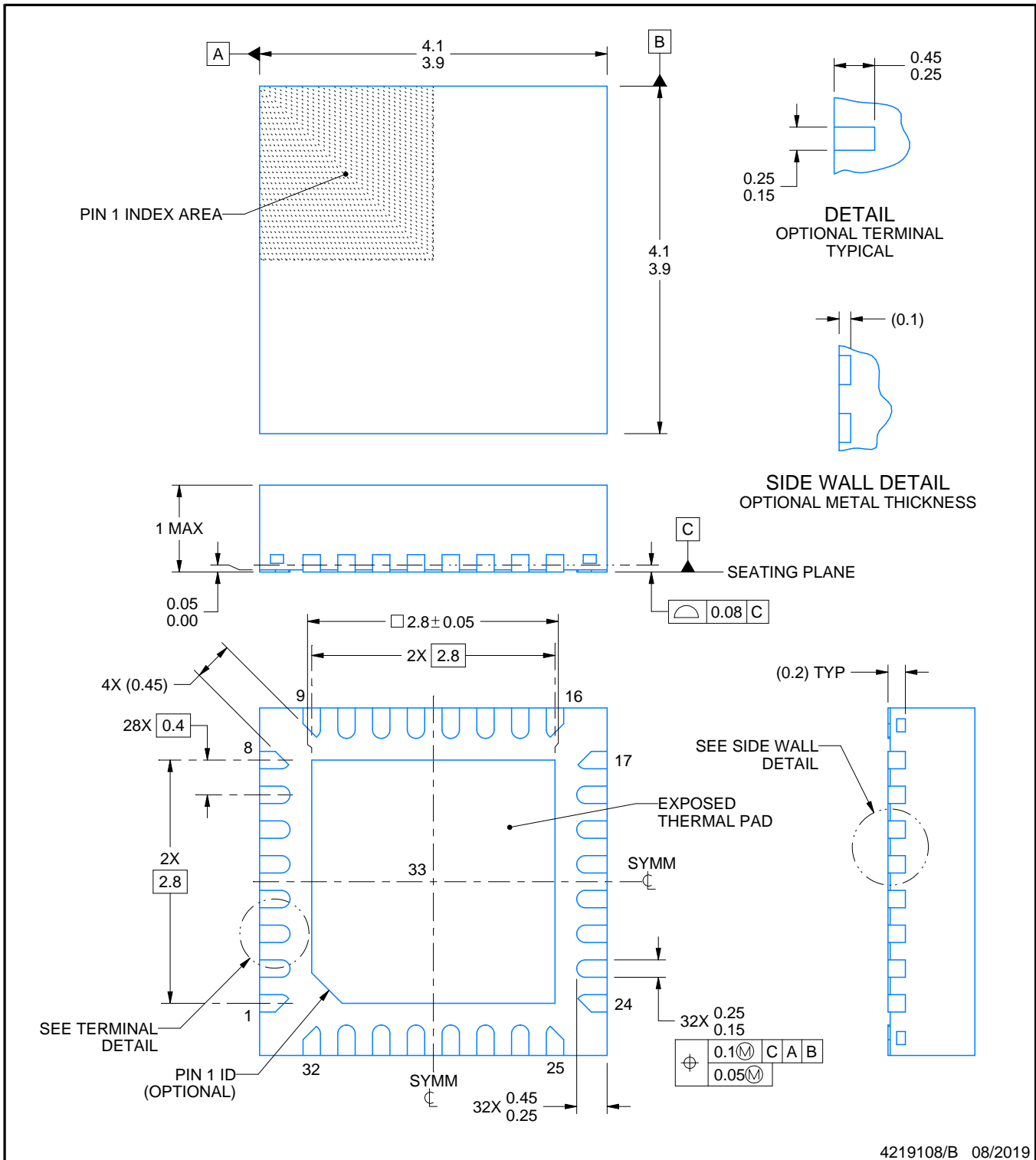
# RSM0032B



# PACKAGE OUTLINE

## VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



4219108/B 08/2019

**NOTES:**

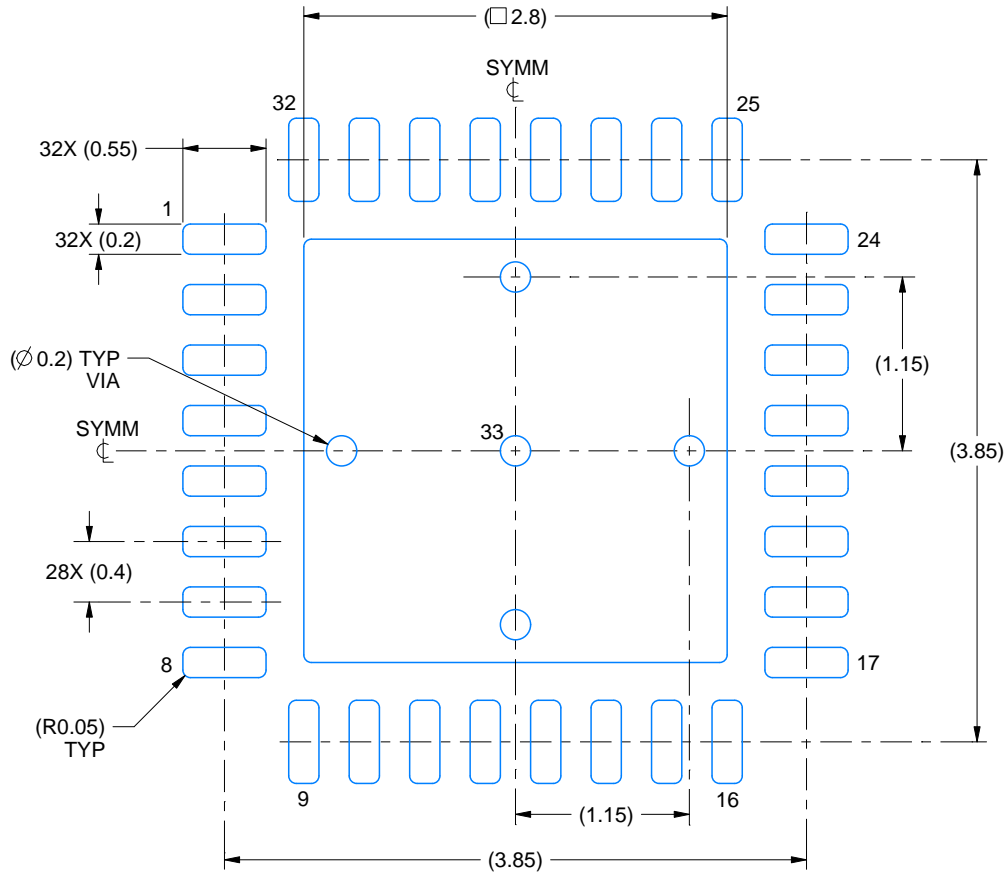
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.

# EXAMPLE BOARD LAYOUT

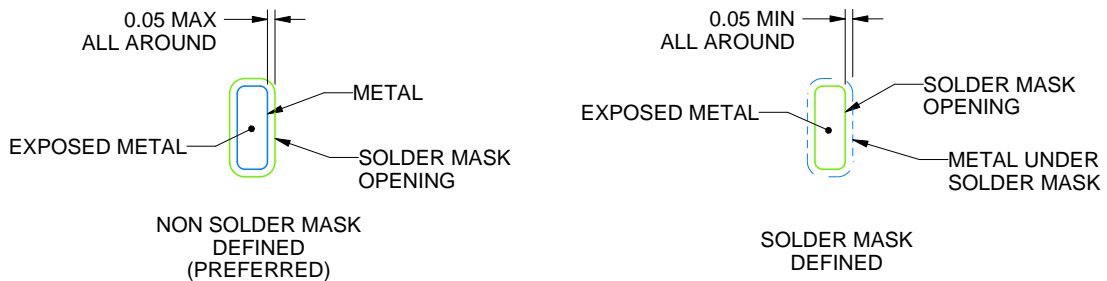
RSM0032B

VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



LAND PATTERN EXAMPLE  
EXPOSED METAL SHOWN  
SCALE:20X



SOLDER MASK DETAILS

4219108/B 08/2019

NOTES: (continued)

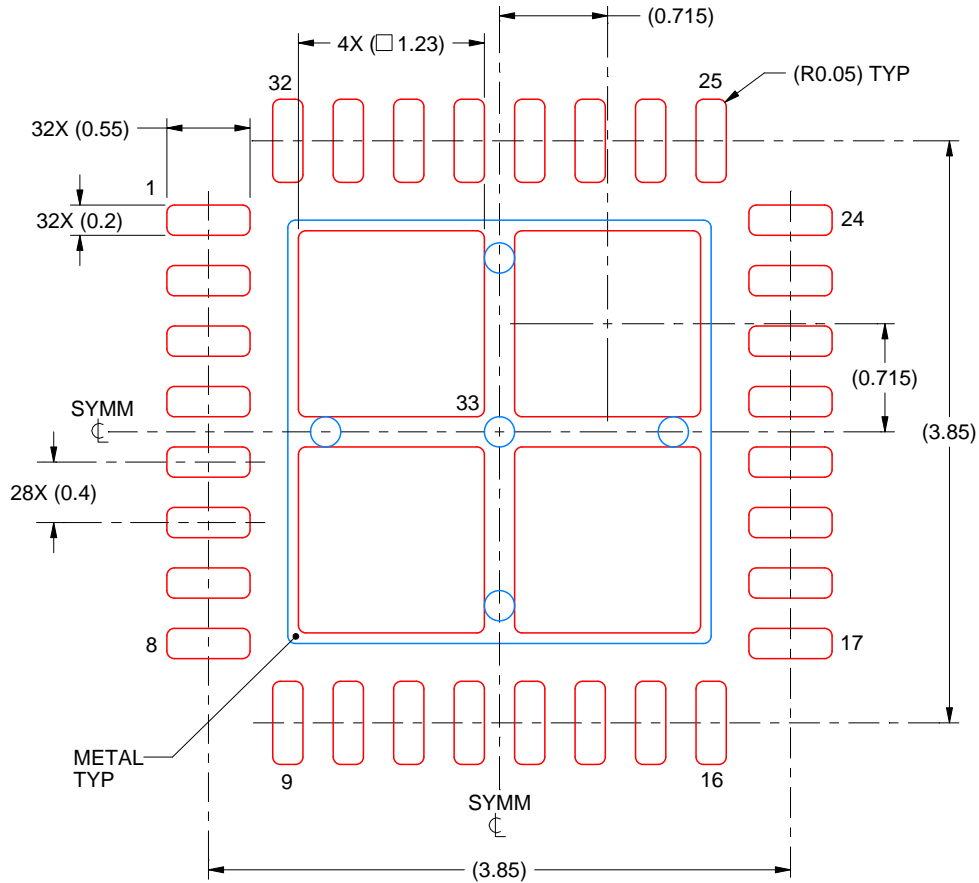
4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 ([www.ti.com/lit/slue271](http://www.ti.com/lit/slue271)).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.

# EXAMPLE STENCIL DESIGN

RSM0032B

VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



**SOLDER PASTE EXAMPLE**  
BASED ON 0.1 mm THICK STENCIL

EXPOSED PAD 33:  
77% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE  
SCALE:20X

4219108/B 08/2019

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

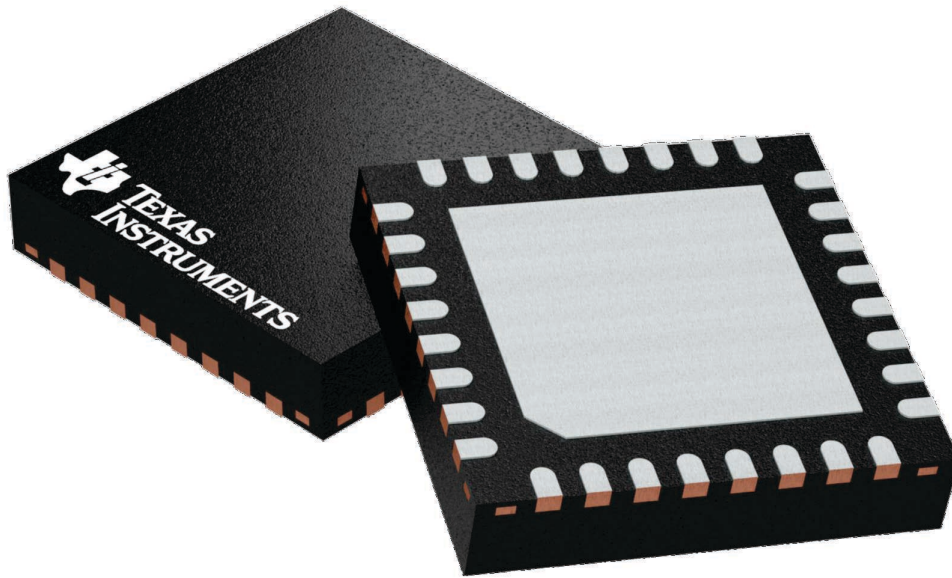
## GENERIC PACKAGE VIEW

**RHB 32**

**VQFN - 1 mm max height**

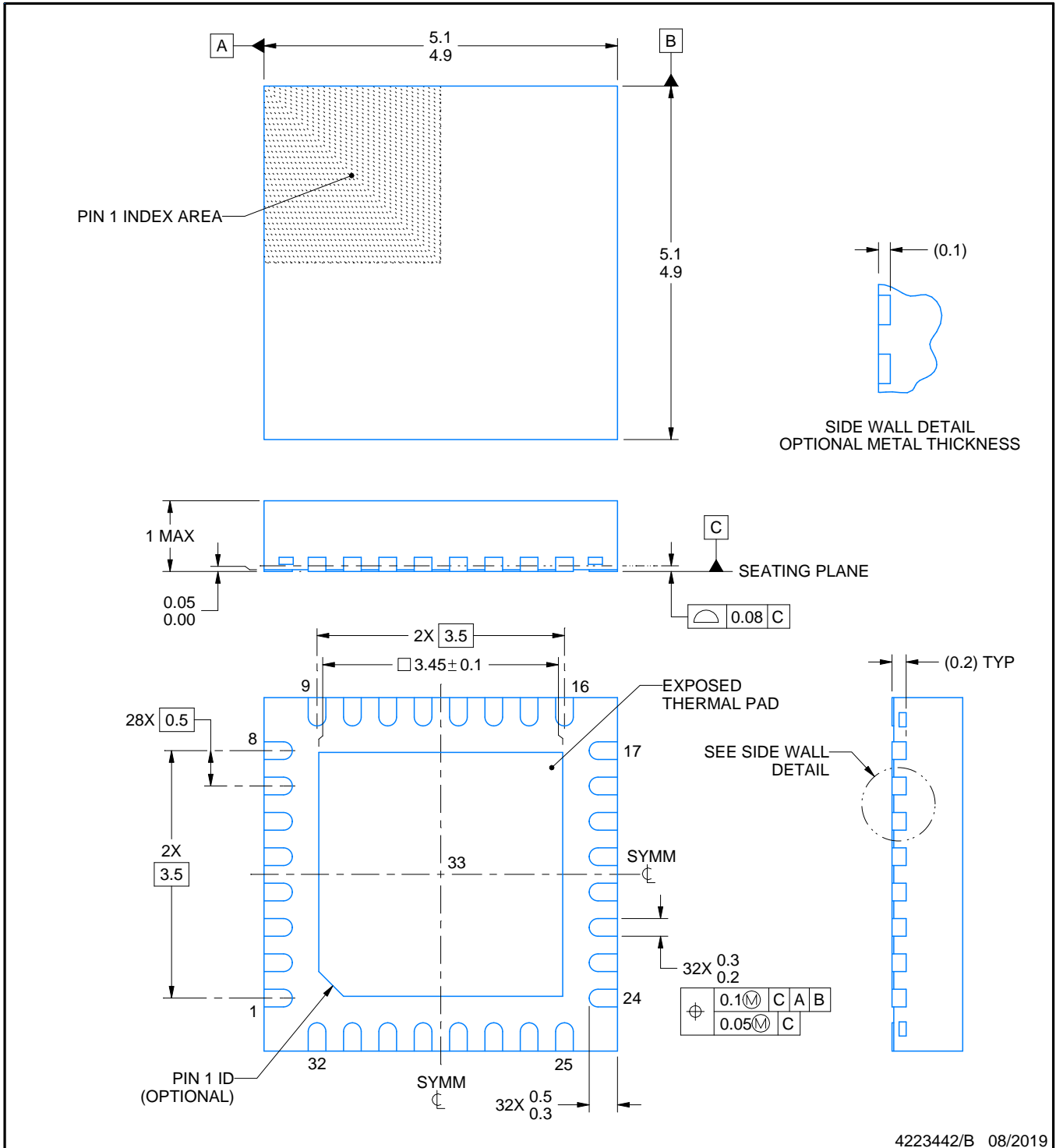
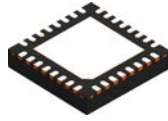
5 x 5, 0.5 mm pitch

PLASTIC QUAD FLATPACK - NO LEAD



Images above are just a representation of the package family, actual package may vary.  
Refer to the product data sheet for package details.

4224745/A



4223442/B 08/2019

NOTES:

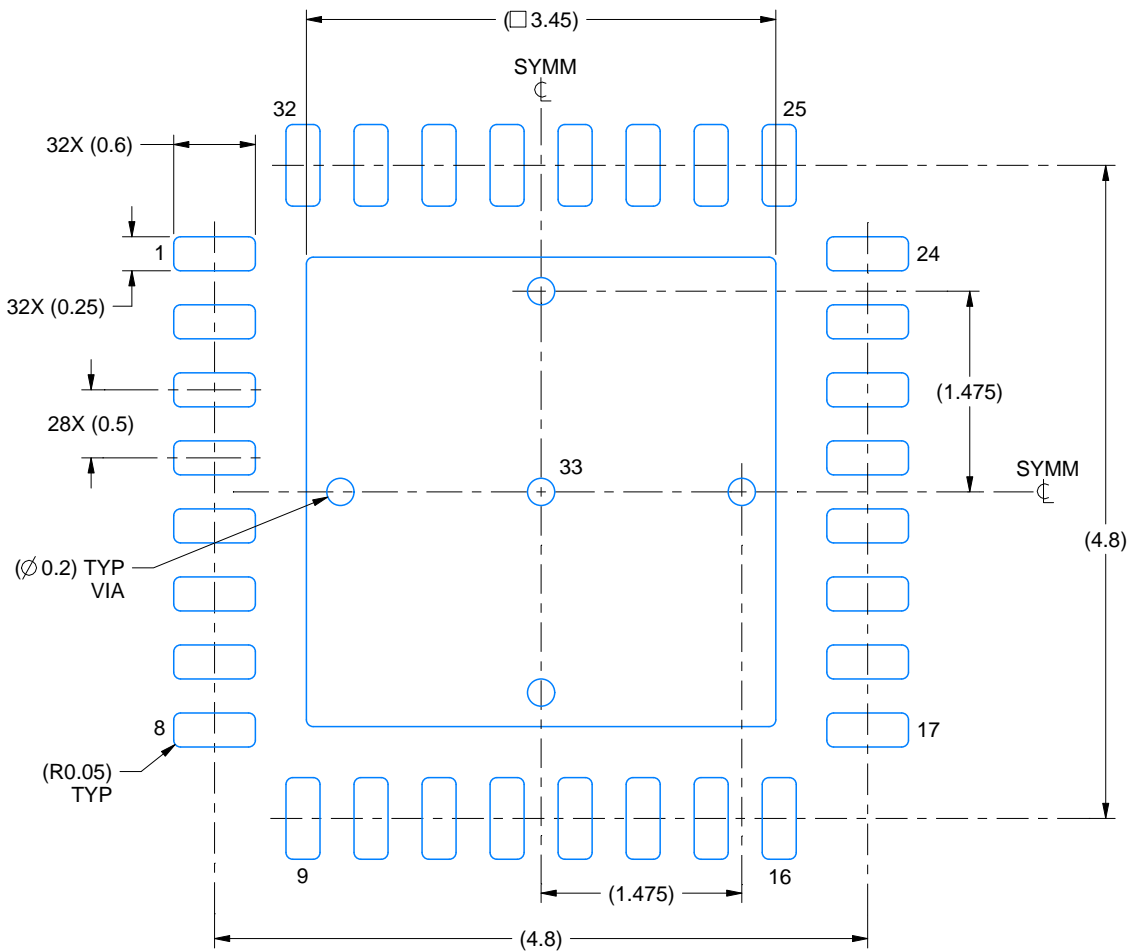
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.

# EXAMPLE BOARD LAYOUT

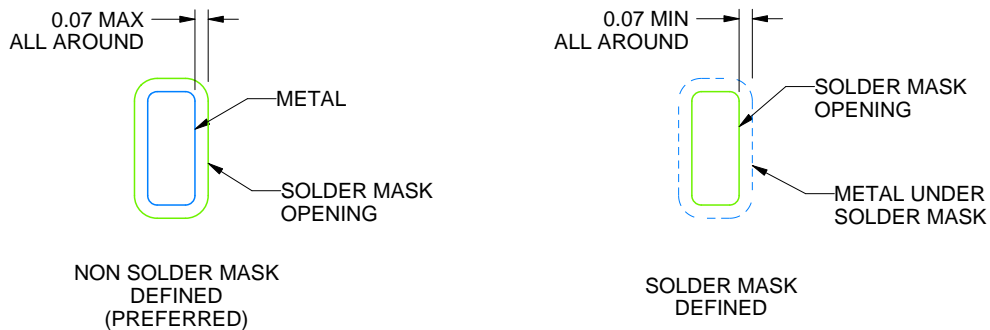
RHB0032E

VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



LAND PATTERN EXAMPLE  
SCALE:18X



SOLDER MASK DETAILS

4223442/B 08/2019

NOTES: (continued)

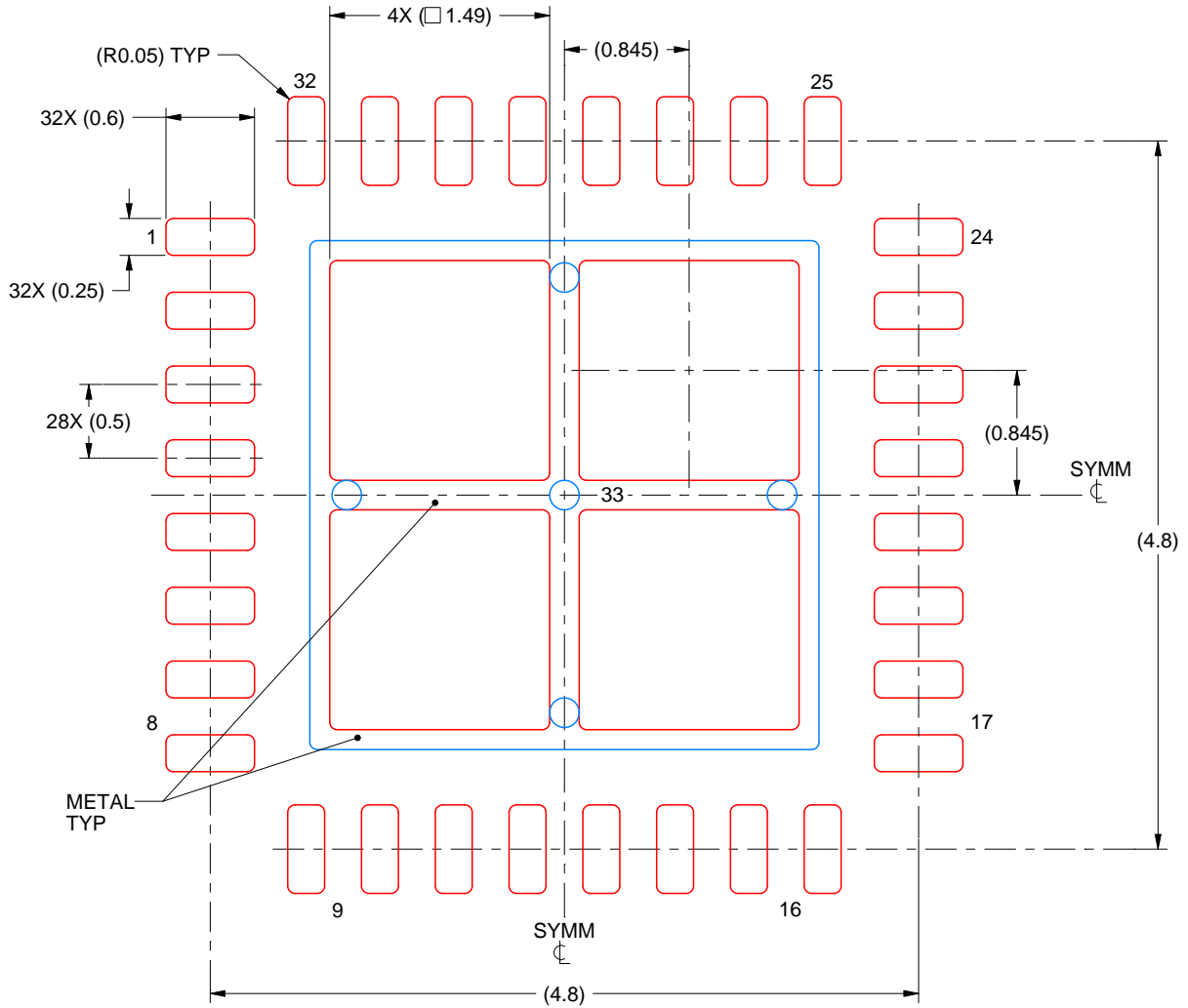
4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 ([www.ti.com/lit/slua271](http://www.ti.com/lit/slua271)).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.

# EXAMPLE STENCIL DESIGN

RHB0032E

VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



**SOLDER PASTE EXAMPLE**  
 BASED ON 0.125 mm THICK STENCIL

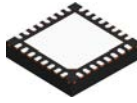
EXPOSED PAD 33:  
 75% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE  
 SCALE:20X

4223442/B 08/2019

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

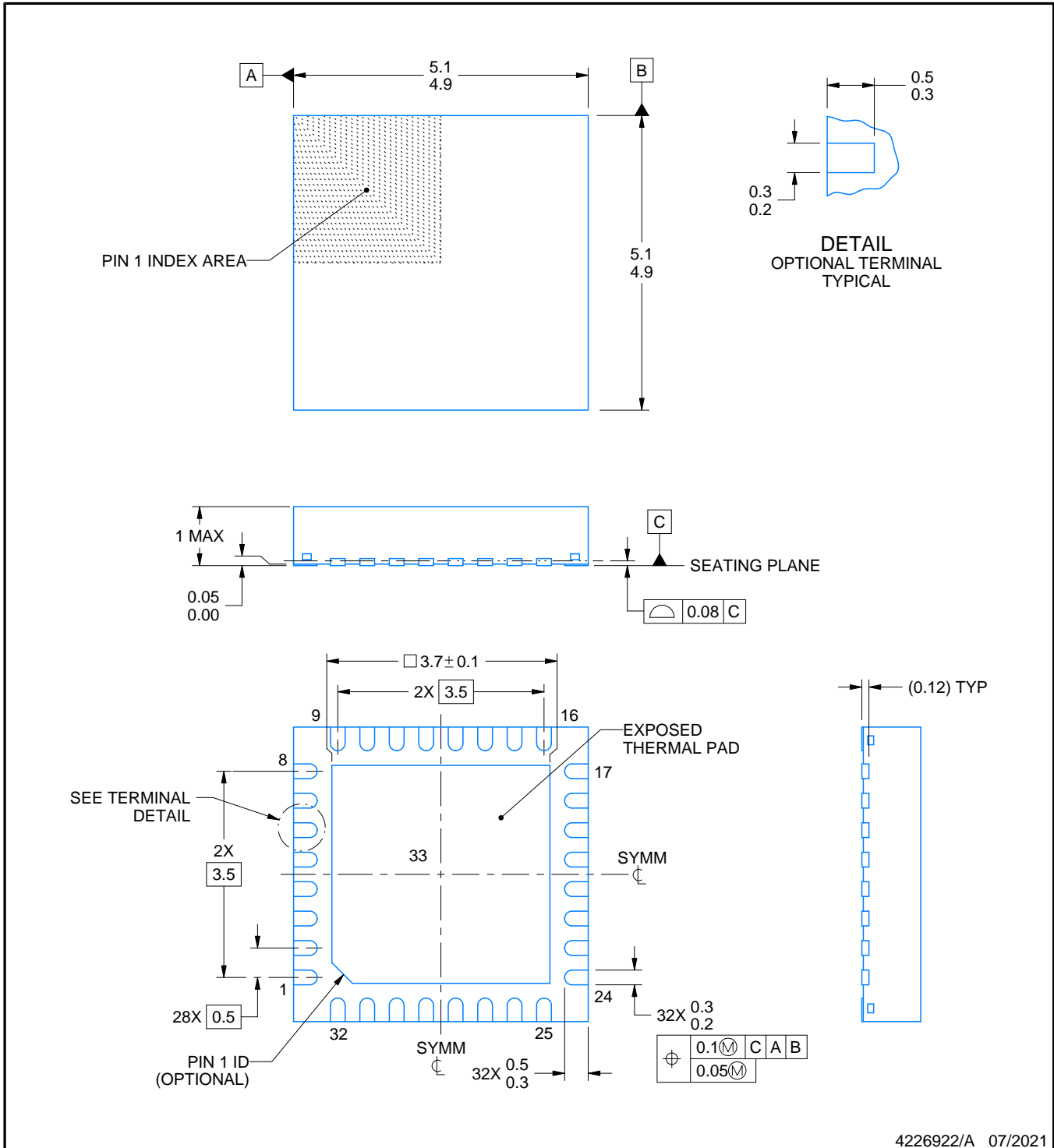
RHB0032W



PACKAGE OUTLINE

VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



4226922/A 07/2021

NOTES:

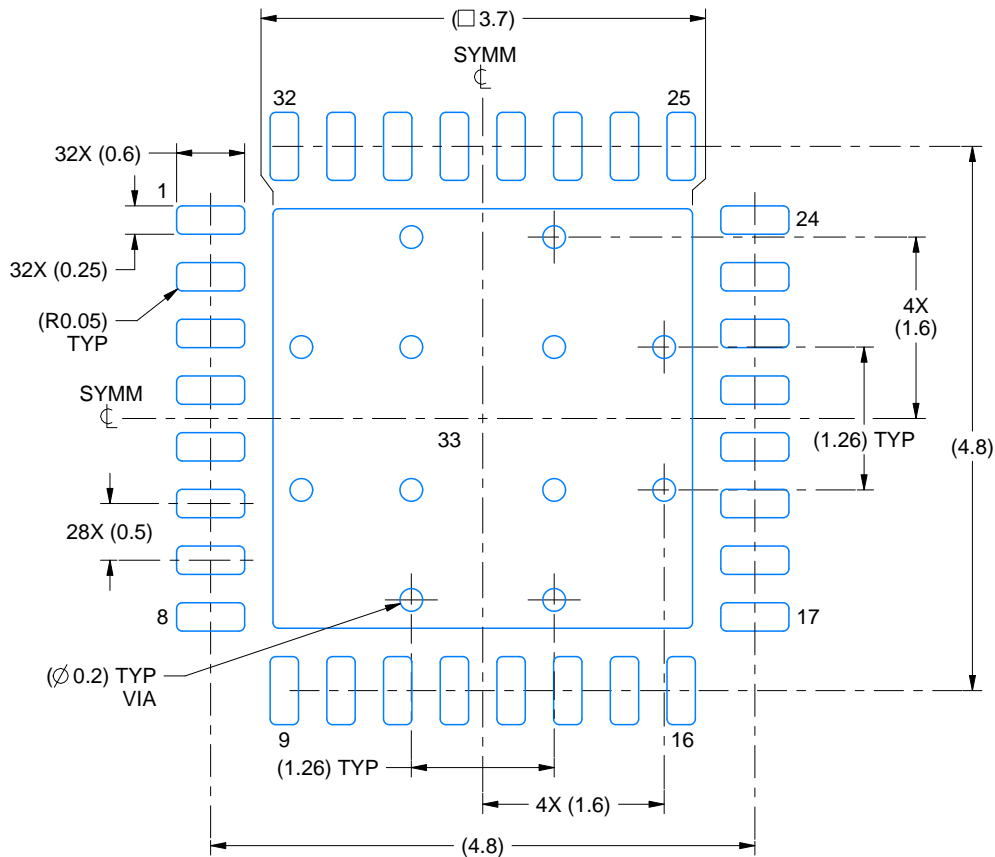
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.

# EXAMPLE BOARD LAYOUT

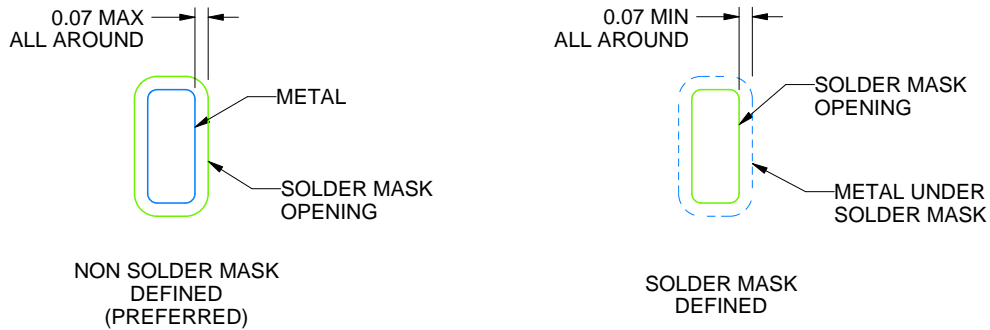
RHB0032W

VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



LAND PATTERN EXAMPLE  
SCALE:15X



SOLDER MASK DETAILS

4226922/A 07/2021

NOTES: (continued)

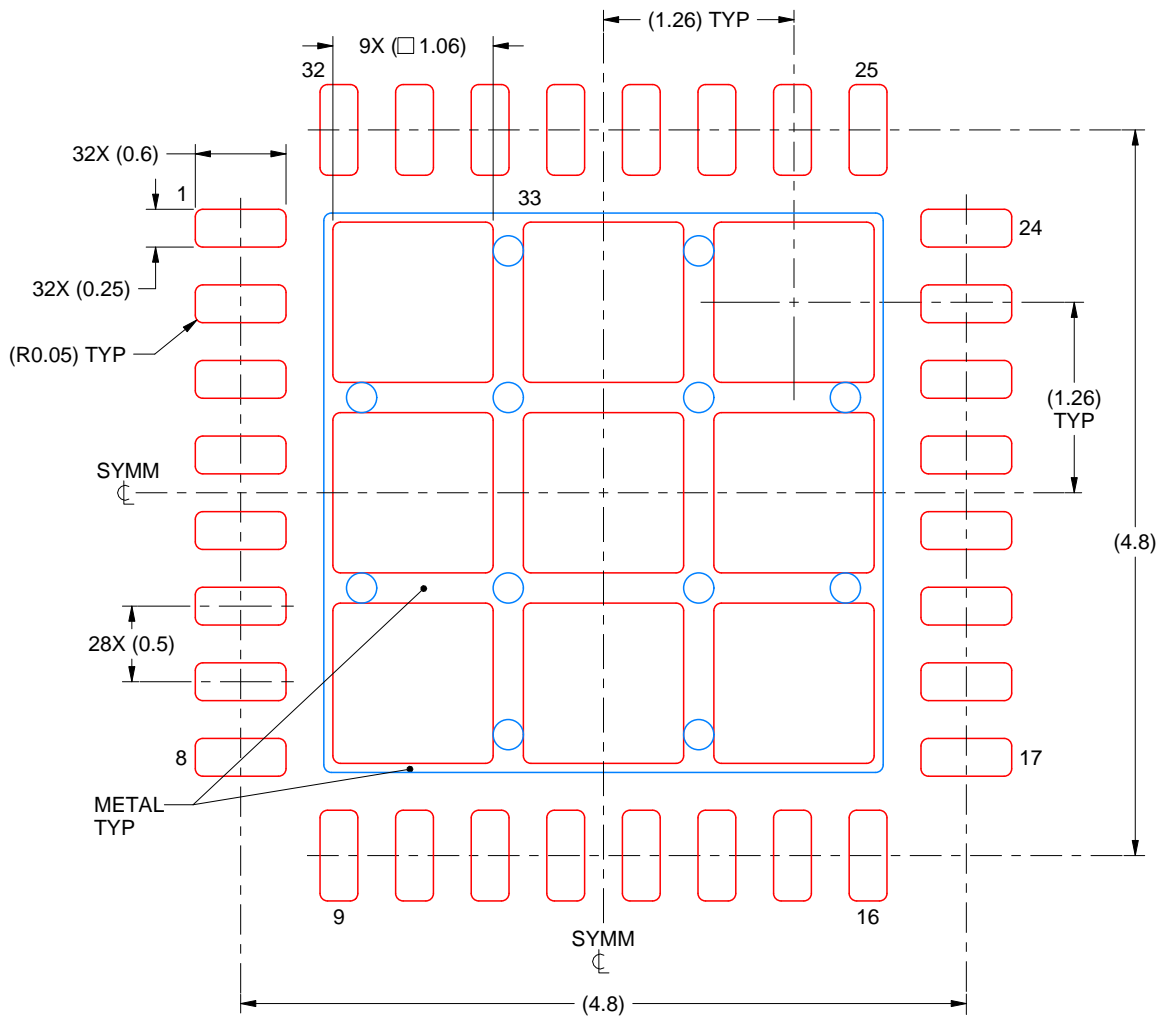
4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 ([www.ti.com/lit/sluea271](http://www.ti.com/lit/sluea271)).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.

# EXAMPLE STENCIL DESIGN

RHB0032W

VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



**SOLDER PASTE EXAMPLE**  
 BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD 33  
 74% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE  
 SCALE:20X

4226922/A 07/2021

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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