TPS65222-Q1 Power Management IC (PMIC) with 4 BUCKs and 3 LDOs for Safety-Relevant Applications

1 Features

- Qualified for automotive applications
- AEC-Q100 qualified with the following results:
  - Input supply: 3V to 5.5V
  - Temperature grade 1: –40°C to +125°C (ambient)
  - HBM classification level 2
  - CDM classification level C4A
- Functional safety-compliant
  - Developed for functional safety applications
  - Documentation available to aid ISO26262 system design
  - Documentation available to aid IEC61508 system design
  - Systematic integrity up to ASIL-D
  - Systematic integrity up to SIL-3
  - Hardware integrity up to ASIL-B
  - Hardware integrity up to SIL-2
  - Undervoltage and overvoltage monitors and current limit on all output supply rails
  - Undervoltage and overvoltage monitors for two external supply rails and for input supply
  - Watchdog (trigger or Q&A)
  - Error signal monitor (level or PWM)
  - Temperature warning and thermal shutdown
  - Built-in self-test on voltage monitors
- BUCK1 + BUCK2 high-efficiency step-down DC/DC converters
  - Output voltage: 0.5V to 3.3V (0.5V to 1.2V for dual-phase output)
  - Output current: 5.5A in single-phase, 10A in dual-phase
  - Switching frequency: 2.2MHz or 4.4MHz
- BUCK3 + BUCK4 high-efficiency step-down DC/DC converters
  - Output voltage: 0.5V to 3.3V
  - Output current: 2.4A
  - Switching frequency: 2.2MHz or 4.4MHz
- Two low-dropout (LDO) linear regulators with configurable load-switch mode
  - Output voltage: 0.6V to 3.3V in LDO-mode
  - Output current: 400mA
- One low-dropout (LDO) linear regulator with low-noise performance and with configurable load-switch mode
  - Output voltage: 1.2V to 3.3V in LDO-mode
  - Output current: 300mA
- Six configurable general-purpose input-output (GPIO) pins, reset and safe state outputs
- OTP configurable power sequence
- 36-pin, 5mm × 6mm, QFN package, 0.5mm pitch

2 Applications

- Processors such as AM62A3-Q1, AM62A3, AM62A7-Q1, AM62A7, AM67, AM62P(-Q1), AM62D(-Q1), AM275, TDA4VEN, TDA4AEN, or processors of other vendors
- Automotive infotainment and digital cluster, eMirror, Camera Mirror System (CMS)
- Driver Monitoring System (DMS), Occupancy Monitoring System (OMS), ADAS Front Camera
- Industrial control and automation, Machine Vision Camera, Autonomous Mobile Robots (AGV/AMR)

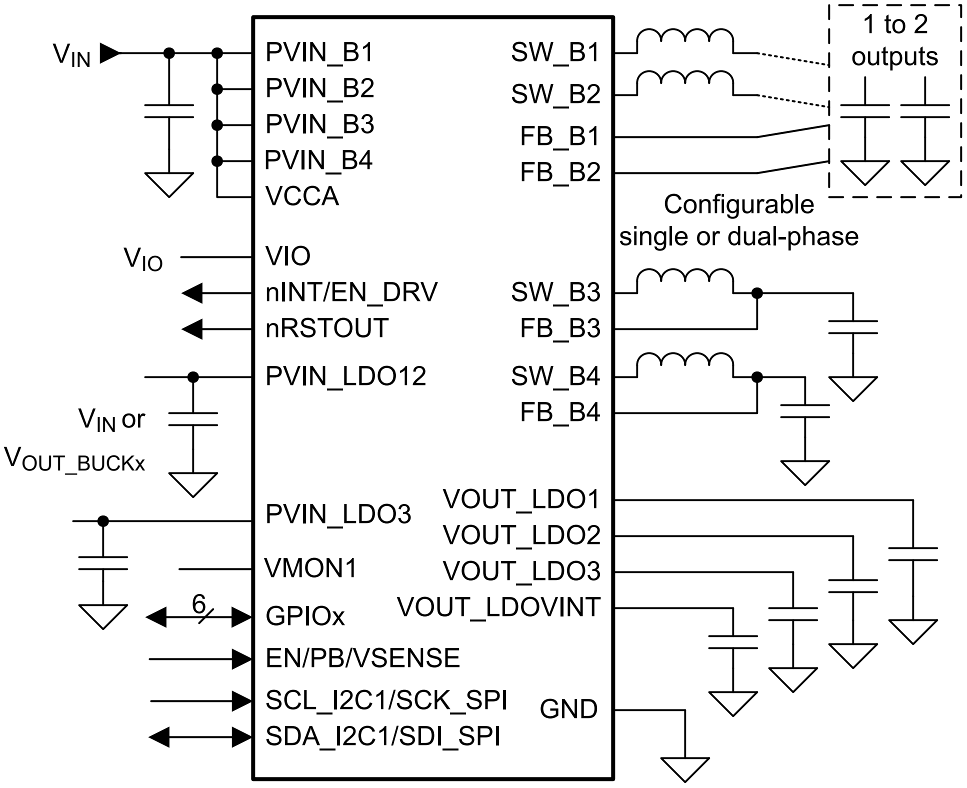
3 Description

The TPS65222-Q1 device meets the power management requirements of the latest processors and platforms in various safety-relevant applications. The device is characterized across an ambient temperature range of -40°C to +125°C, making the PMIC an excellent choice for various automotive applications. The device has four step-down DC/DC (BUCK) converters, of which two can be used in a dual-phase configuration. Furthermore, the device has three low drop-out (LDO) regulators, which can also be used as load-switches.

Packaging Information

PART NUMBER	PACKAGE[1]	PACKAGE SIZE[2]
TPS65222-Q1	VQFN-HR (36)	5.00mm × 6.00mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.
(2) The package size (length × width) is a nominal value and includes pins, where applicable



Simplified Application

4 Device and Documentation Support

TI offers an extensive line of development tools. Tools and software to evaluate the performance of the device, generate code, and develop solutions are listed in www.ti.com/product/TPS65222-Q1.

4.1 Device Support

4.1.1 Device Nomenclature

The following acronyms and terms are used in this data sheet. For a detailed list of terms, acronyms, and definitions, see the *TI glossary*.

ABIST	Analog Built-In Self-Test
AVS	Adaptive Voltage Scaling
BIST	Built-In Self-Test
CRC	Cyclic Redundancy Check
DAC	Digital-to-Analog Converter
DCR	DC Resistance of an inductor
DVS	Dynamic Voltage Scaling
EMC	Electromagnetic Compatibility
ESM	Error Signal Monitor
ESR	Equivalent Series Resistance
FSD	First Supply Detection
GPIO	General-Purpose Input and Output
I^2C	Inter-Integrated Circuit
LDO	Low-Dropout voltage linear regulator
NA	Not Applicable
MCU	Micro Controller Unit
NVM	Non-Volatile Memory
OPN	Orderable Part Number
OTP	One Time Programmable
OV	Overvoltage
OVP	Overvoltage Protection
PD	Pull-Down
PDN	Power Delivery Network
PFM	Pulse Frequency Modulation
PFSM	Pre-configured Finite State Machine
PGOOD	Power Good (signal which indicates that the monitored power supply rail is in range)
PLL	Phase Locked Loop
PMIC	Power-Management Integrated Circuit
POR	Power On Reset
PU	Pull-Up
PP	Push-Pull
PSRR	Power Supply Rejection Ratio

PWM	Pulse Width Modulation
SoC	System on Chip
SPI	Serial Peripheral Interface
TSD	Thermal Shut-Down
UV	Undervoltage
UVLO	Undervoltage Lockout
VMON	Voltage Monitor

4.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

4.3 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

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4.5 Trademarks

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4.6 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

4.7 Glossary

TI Glossary   This glossary lists and explains terms, acronyms, and definitions.

5 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

DATE	REVISION	NOTES
August 2025	*	Initial Release

6 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TPS6522230WRAHRQ1	Active	Production	VQFN-HR (RAH) | 36	3000 | LARGE T&R	Yes	Call TI	Level-2-260C-1 YEAR	-40 to 125	TPS6522 230WQ1
TPS65222C5RAHRQ1	Active	Production	VQFN-HR (RAH) | 36	3000 | LARGE T&R	Yes	SN	Level-2-260C-1 YEAR	-40 to 125	TPS6522 2C5Q1

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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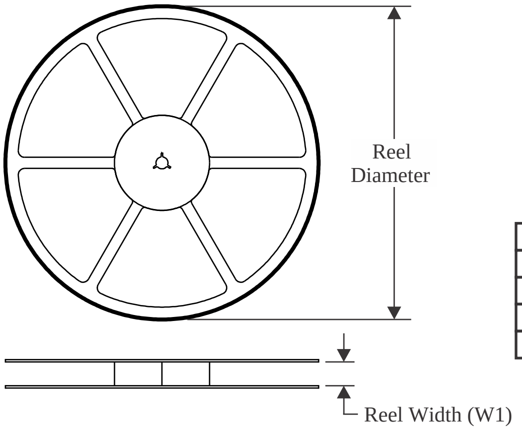
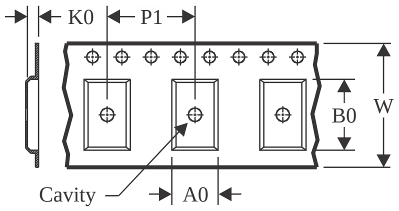
TAPE AND REEL INFORMATION

REEL DIMENSIONS

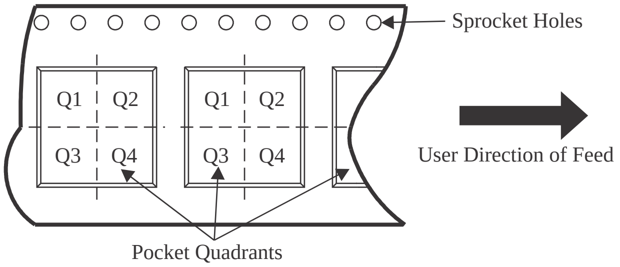


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

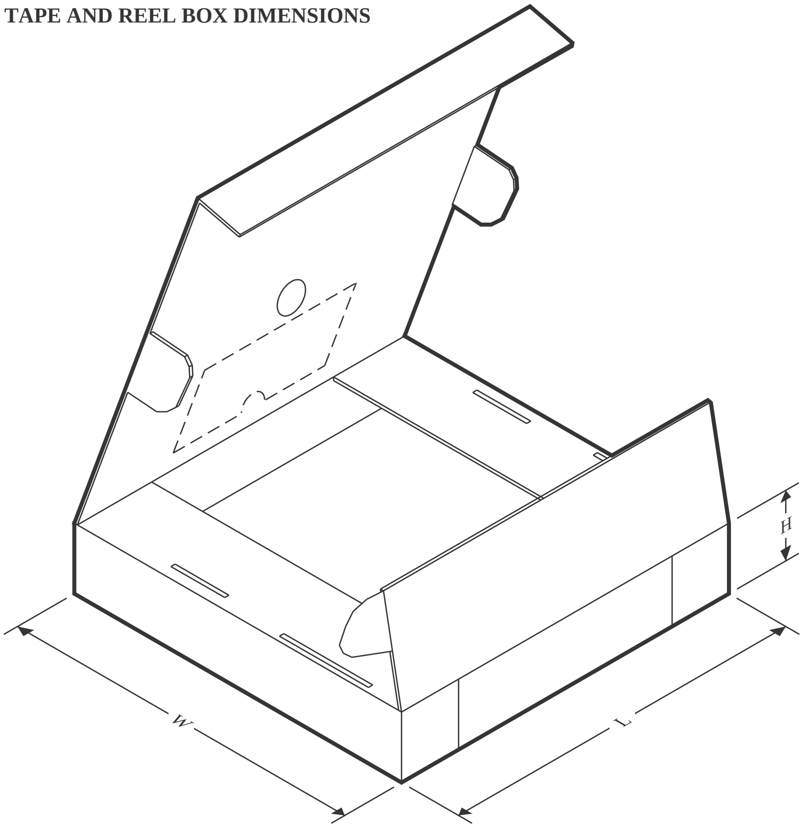
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS6522230WRAHRQ1	VQFN-HR	RAH	36	3000	330.0	12.4	5.3	6.3	1.15	8.0	12.0	Q2
TPS65222C5RAHRQ1	VQFN-HR	RAH	36	3000	330.0	12.4	5.3	6.3	1.15	8.0	12.0	Q2

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

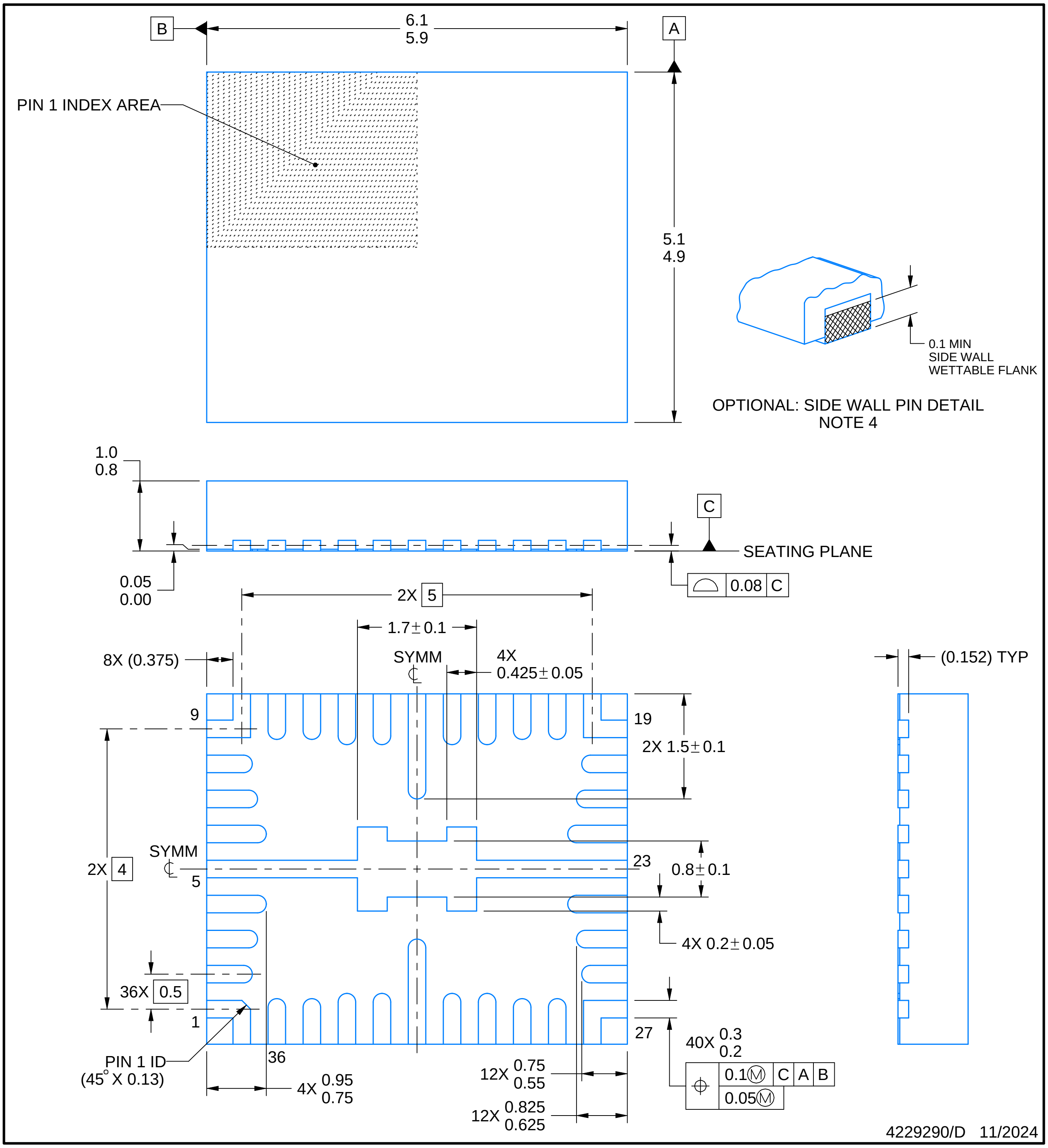
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS6522230WRAHRQ1	VQFN-HR	RAH	36	3000	367.0	367.0	35.0
TPS65222C5RAHRQ1	VQFN-HR	RAH	36	3000	367.0	367.0	35.0

RAH0036A

PACKAGE OUTLINE

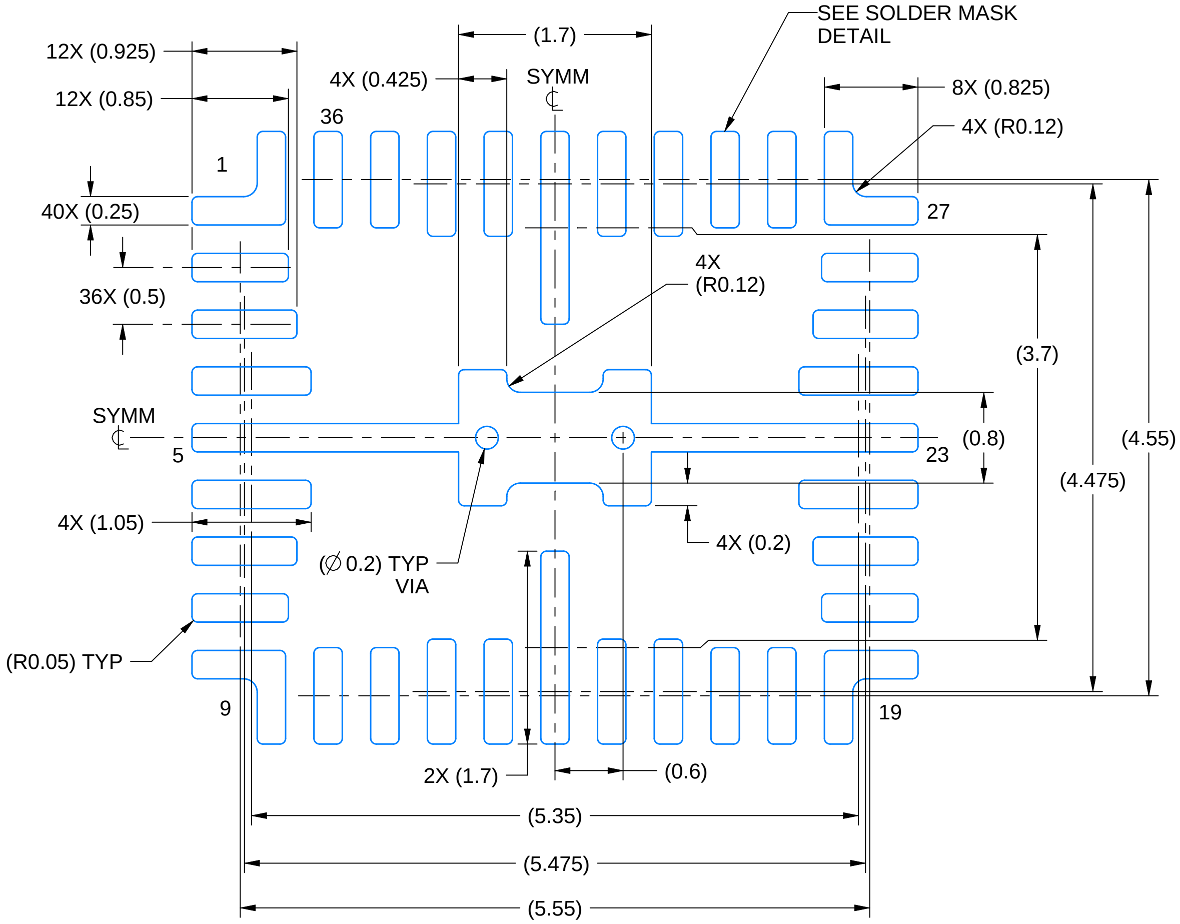
VQFN-HR - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD

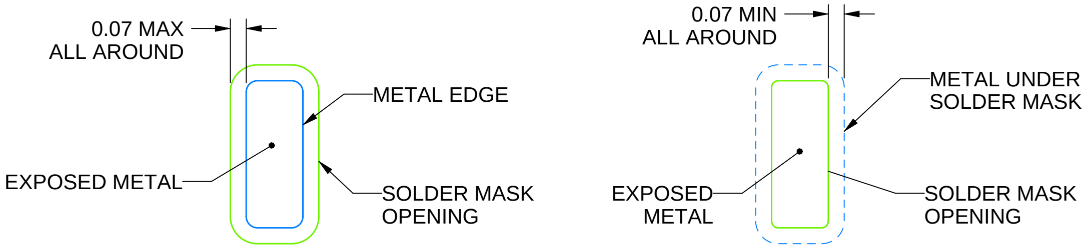


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.
4. Minimum 0.1 mm solder wetting on pin side wall. Available for wettable flank version only.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 15X



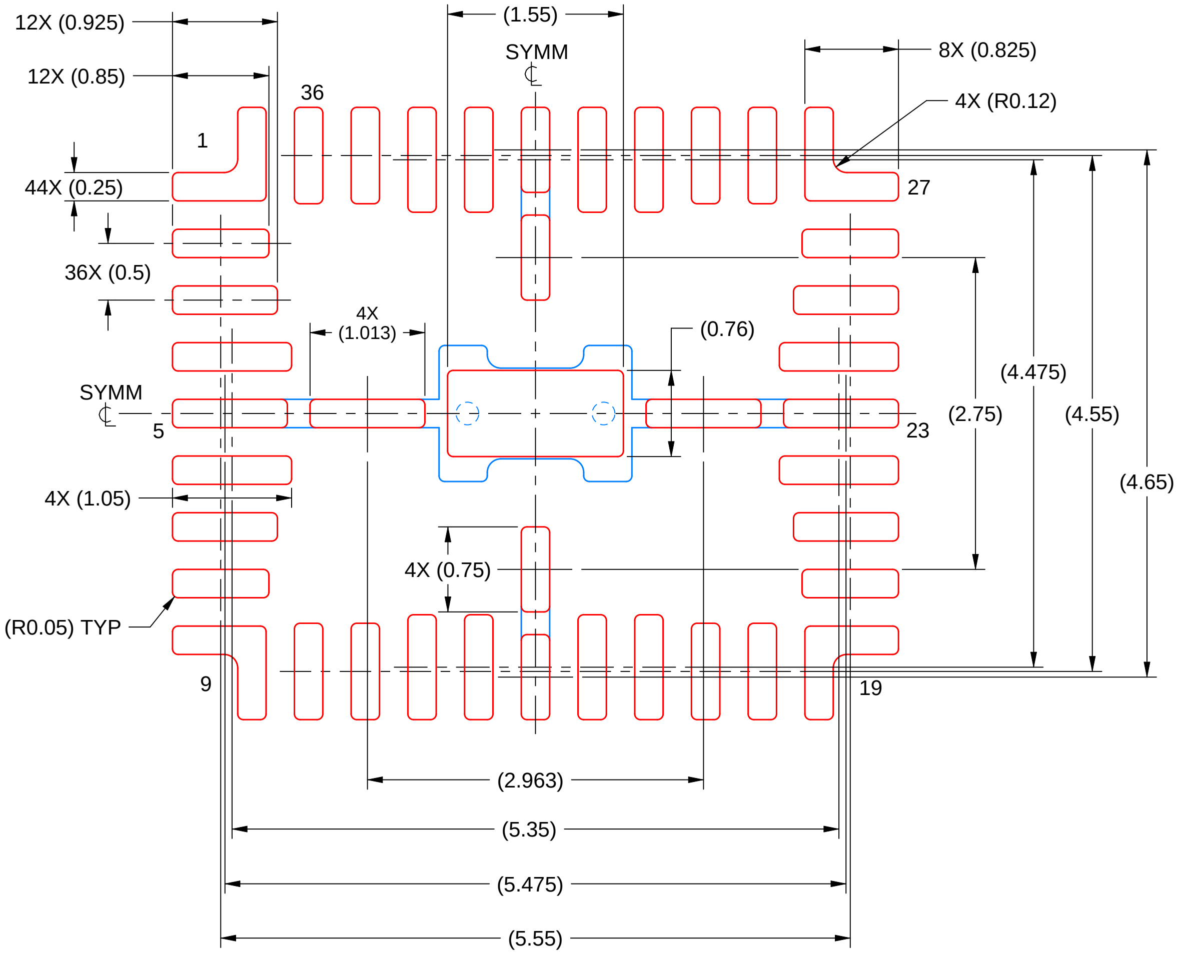
NON SOLDER MASK DEFINED (PREFERRED)

SOLDER MASK DEFINED

SOLDER MASK DETAILS

NOTES: (continued)

5. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
6. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 MM THICK STENCIL
SCALE: 15X

PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
PAD CONNECTED TO PINS 5 & 23: 76%
PADS 14 & 32: 88%

NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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