TPS723 200-mA, Low-Noise, High-PSRR, Negative Output Low-Dropout Linear Regulators

1 Features

- Ultralow noise: 60 μV_{RMS} typical
- High PSRR: 65 dB typical at 1 kHz
- Low dropout voltage: 280 mV typical at 200 mA, 2.5 V
- Available in –2.5-V and adjustable (–1.2 V to –10 V) versions
- Stable with a 2.2-µF ceramic output capacitor
- Less than 2-µA typical quiescent current in shutdown mode
- 2% overall accuracy (line, load, temperature)
- Thermal and over-current protection
- Packages:
  - SOT23-5 (DBV)
  - SOT23-5 (DDC)
  - WSON-6 (DRV)
- Operating junction temperature range: –40°C to 125°C

2 Applications

- Optical modules
- Semiconductor manufacturing
- Medical accessories
- Oscilloscopes
- Active antenna system mMIMO (AAS)

3 Description

The TPS723 low-dropout (LDO) negative voltage regulator offers an ideal combination of features to support low noise applications. This device is capable of operating with input voltages from –10 V to –2.7 V, and support outputs from –10 V to –1.2 V. This regulator is stable with small, low-cost ceramic capacitors, and include enable (EN) and noise reduction (NR) functions. Thermal short-circuit and over-current protections are provided by internal detection and shutdown logic. High PSRR (65 dB at 1 kHz) and low noise (60 μV_{RMS}) make the TPS723 ideal for low-noise applications.

The TPS723 uses a precision voltage reference to achieve 2% overall accuracy over load, line, and temperature variations. Available in a small SOT23-5 package, the TPS723 is fully specified over a temperature range of –40°C to 125°C.

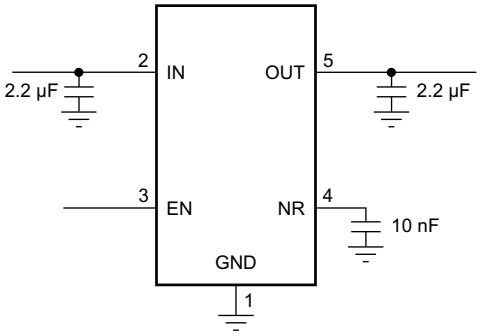
Device Information[1]

PART NUMBER	PACKAGE[2]	BODY SIZE (NOM)
TPS723	SOT-23 (5)	2.90 mm x 1.60 mm
	SOT (5)	2.90 mm x 1.60 mm
	WSON (6)	2.00 mm x 2.00 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

(2) The two SOT23 packages are identical in size, but the SOT package is thinner.

Typical Application Circuit



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4 Revision History

Changes from Revision C (September 2014) to Revision D **Page**

- Added DRV package to document ... 1
- Changed *Applications* section to link to end equipment ... 1

Changes from Revision B (July 2007) to Revision C **Page**

- Changed format to meet latest data sheet standards; added new sections, and moved existing sections ... 1
- Added bullet item for DDC package to Features list ... 1
- Revised *Device Information* table to include SOT-5 package ... 1
- Updated *Typical Application Circuit* to show SOT-5 (DDC) package pin configuration ... 1
- Added pin configuration drawings ... 3
- Deleted *Dissipation Ratings* table; see *Thermal Information* ... 4
- Changed y-axis title in Figure 11 to *Feedback Current* from *Supply Current* ... 6
- Reworded second paragraph in *Current Limit* subsection. ... 12

Changes from Revision A (June 2007) to Revision B **Page**

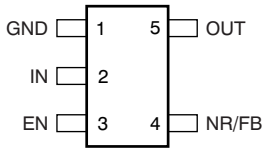
- Added second paragraph in *Current Limit* subsection ... 12
- Changed equation shown in Figure 27 ... 13

Changes from Original (September 2003) to Revision A **Page**

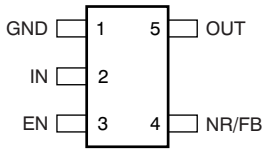
- Changed document format to correspond to current product line standards ... 1
- Removed *Output Voltage vs Output Current* graph (original Fig 2) ... 6

5 Pin Configuration and Functions

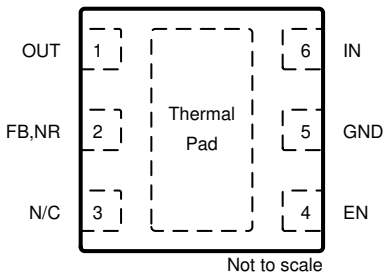
DBV Package
5-Pin SOT23
Top View



DDC Package
5-Pin SOT23
Top View



DRV Package
6-Pin WSON
Top View



Not to scale

Pin Functions

PIN			I/O	DESCRIPTION
NAME	NO.			
	DBV, DDC	DRV		
GND	1	5	—	Ground
IN	2	6	I	Input supply
EN	3	4	I	Bipolar enable pin. Driving this pin above the positive enable threshold or below the negative enable threshold turns on the regulator. Driving this pin below the positive disable threshold and above the negative disable threshold puts the regulator into shutdown mode.
NR	4	2	—	Fixed voltage versions only. Connecting an external capacitor between this pin and ground, bypasses noise generated by the internal band gap. This configuration allows output noise to be reduced to very low levels.
FB	4	2	I	Adjustable voltage version only. This pin is the input to the control loop error amplifier. This pin is used to set the output voltage of the device.
OUT	5	1	O	Regulated output voltage. A small, 2.2-μF ceramic capacitor is needed from this pin to GND to ensure stability.
N/C	—	3		No internal connection

6 Specifications

6.1 Absolute Maximum Ratings

over operating junction temperature range (unless otherwise noted)(1)(2)

		MIN	MAX	UNIT
Voltage	IN	–11	+0.3	V
	NR	–11	+5.5	
	EN	$-V_I$	+5.5	
	OUT	–11	+0.3	
Current	OUT	Internally limited		A
Output short-circuit duration		Indefinite		
Continuous total power dissipation		See Thermal Information table		
Operating junction temperature, T_J		–65	150	°C
Storage temperature, T_{stg}		–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values are with respect to network ground terminal.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±1000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101(2)	±500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating junction temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
V_I	Input supply voltage range	–10		–2.7	V
I_O	Output current	0		200	mA
T_J	Operating junction temperature	–40		125	°C

6.4 Thermal Information

THERMAL METRIC(1)		TPS723			UNIT
		DBV (SOT23)	DDC (SOT23)	DRV (WSON)	
		5 PINS	5 PINS	6 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	206.9	194.8	85.6	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	120.5	41.4	83.7	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	35.9	35.9	47.3	°C/W
ψ_{JT}	Junction-to-top characterization parameter	13.3	1.0	3.7	°C/W
ψ_{JB}	Junction-to-board characterization parameter	35.0	35.7	47.3	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	N/A	31.6	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC package thermal metrics* application report.

6.5 Electrical Characteristics

Over operating junction temperature range, $V_I = V_{O(NOM)} – 0.5$ V, $I_O = 1$ mA, $V_{EN} = 1.5$ V, $C_O = 2.2$ µF, and $C_{NR} = 0.01$ µF, unless otherwise noted. Typical values are at $T_J = 25°C$.

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_I	Input voltage range(1)			–10		–2.7	V
V_{FB}	Feedback reference voltage	TPS72301	$T_J = 25°C$	–1.210	–1.186	–1.162	V
V_O	Output voltage range	TPS72301		–10 + V_{DO}		V_{FB}	V
	Accuracy	Nominal	$T_J = 25°C$	–1%		1%	
		TPS72325 vs $V_I/I_O/T$	–10 V ≤ V_I ≤ V_O – 0.5 V, 10 µA ≤ I_O ≤ 200 mA	–2%	±1%	2%	
		TPS72301 vs $V_I/I_O/T$		–3%	±1	3%	
$\Delta V_{O(\Delta VI)}$	Line regulation		–10 V ≤ V_I ≤ $V_{O(NOM)}$ – 0.5 V		0.04		%/V
$\Delta V_{O(\Delta IO)}$	Load regulation		0 mA ≤ I_O ≤ 200 mA		0.002		%/mA
V_{DO}	Dropout voltage at $V_O = 0.96 \times V_{O(NOM)}$	TPS72325	I_O = 200 mA		280	500	mV
$I_{(LIM)}$	Current limit		$V_O = 0.85 \times V_{O(NOM)}$	300	550	800	mA
$I_{(GND)}$	Ground pin current		I_O = 0 mA (I_Q), –10 V ≤ V_I ≤ V_O – 0.5 V		130	200	µA
			I_O = 200 mA, –10 V ≤ V_I ≤ V_O – 0.5 V		350	500	
$I_{(SHDN)}$	Shutdown ground pin current		–0.4 V ≤ V_{EN} ≤ 0.4 V, –10 V ≤ V_I ≤ V_O – 0.5 V		0.1	2.0	µA
$I_{(FB)}$	Feedback pin current		–10 V ≤ V_I ≤ V_O – 0.5 V		0.05	1.0	µA
PSRR	Power-supply rejection ratio	TPS72325	I_O = 200 mA, 1 kHz, $C_I = C_O$ = 10 µF		65		dB
			I_O = 200 mA, 10 kHz, $C_I = C_O$ = 10 µF		48		
V_n	Output noise voltage	TPS72325	C_O = 10 µF, 10 Hz to 100 kHz, I_O = 200 mA		60		μV_{RMS}
t_{STR}	Startup time		V_O = –2.5 V, C_O = 1 µF, R_L = 25 Ω		1		ms
$V_{EN(HI)}$	Enable threshold positive			1.5			V
$V_{EN(LO)}$	Enable threshold negative					–1.5	V
$V_{DIS(HI)}$	Disable threshold positive					0.4	V
$V_{DIS(LO)}$	Disable threshold negative			–0.4			V
$I_{(EN)}$	Enable pin current		–10 V ≤ V_I ≤ V_O – 0.5 V, –10 V ≤ V_{EN} ≤ ±3.5 V		0.1	2.0	µA
T_{sd}	Thermal shutdown temperature		Shutdown, temperature increasing		165		°C
			Reset, temperature decreasing		145		
T_J	Operating junction temperature			–40		125	°C

(1) Maximum $V_I = (V_O – V_{DO})$ or – 2.7 V, whichever is more negative.

6.6 Typical Characteristics

TPS72325 at $V_I = V_{O(NOM)} – 0.5$ V, $I_O = 1$ mA, $V_{EN} = 1.5$ V, $C_O = 2.2$ µF, and $C_{NR} = 0.01$ µF, unless otherwise noted.

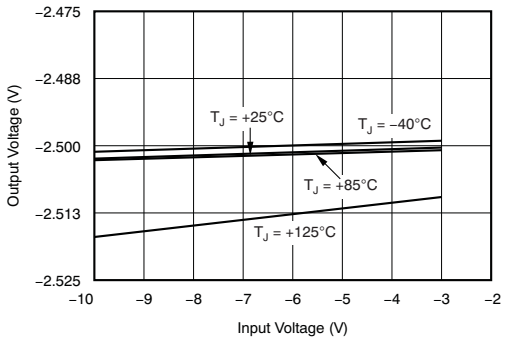


Figure 1. Output Voltage vs Input Voltage

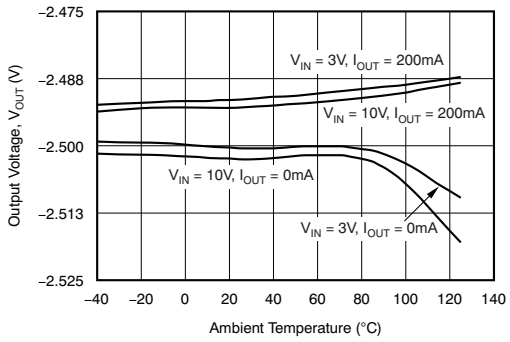


Figure 2. Output Voltage vs Ambient Temperature

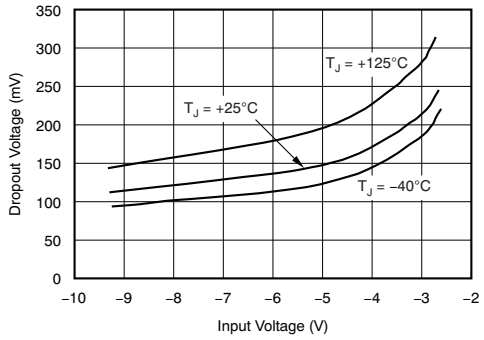


Figure 3. TPS72301 Dropout Voltage vs Input Voltage

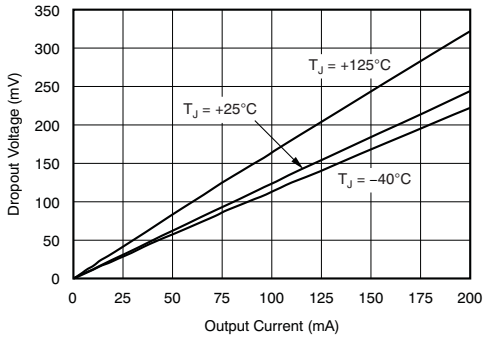


Figure 4. Dropout Voltage vs Output Current

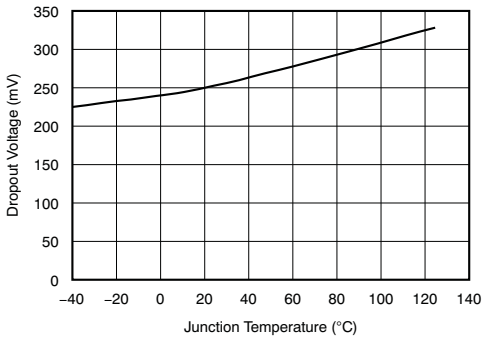


Figure 5. TPS72325 Dropout Voltage vs Junction Temperature

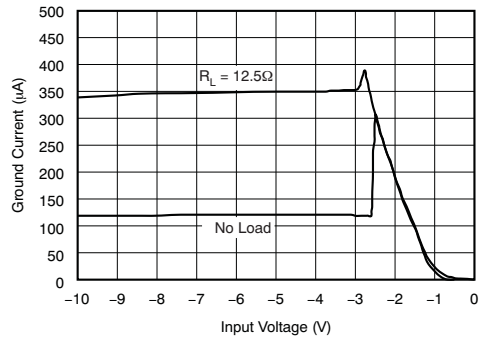


Figure 6. Ground Current vs Input Voltage

Typical Characteristics (continued)

TPS72325 at $V_I = V_{O(NOM)} - 0.5$ V, $I_O = 1$ mA, $V_{EN} = 1.5$ V, $C_O = 2.2$ µF, and $C_{NR} = 0.01$ µF, unless otherwise noted.

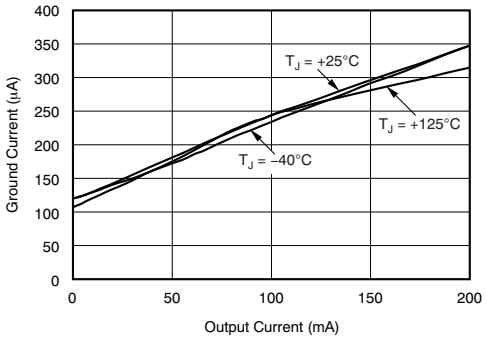


Figure 7. Ground Current vs Output Current

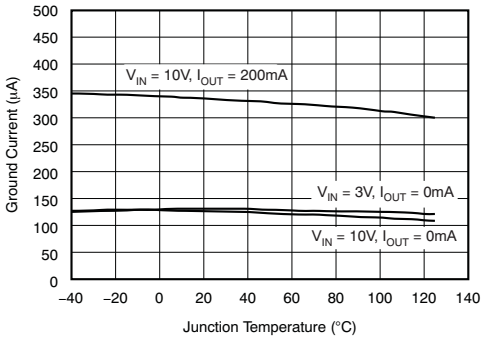


Figure 8. Ground Current vs Junction Temperature

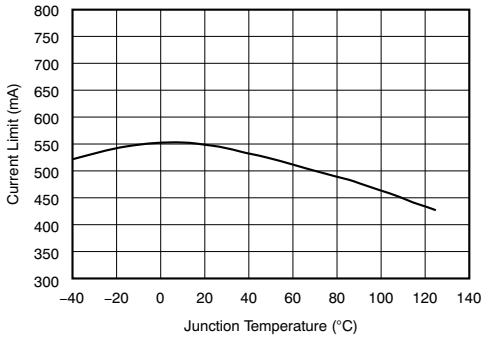


Figure 9. TPS72325 Current Limit vs Junction Temperature

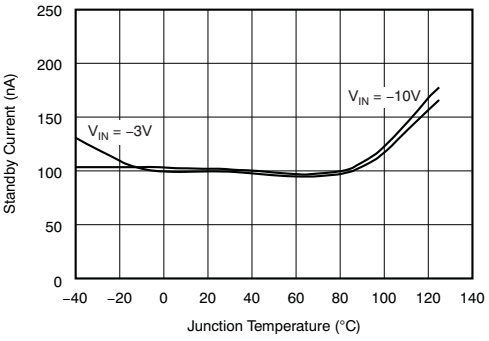


Figure 10. Standby Current vs Junction Temperature

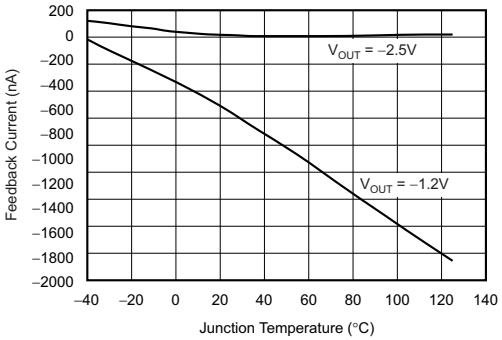


Figure 11. TPS72301 Feedback Pin Current vs Junction Temperature

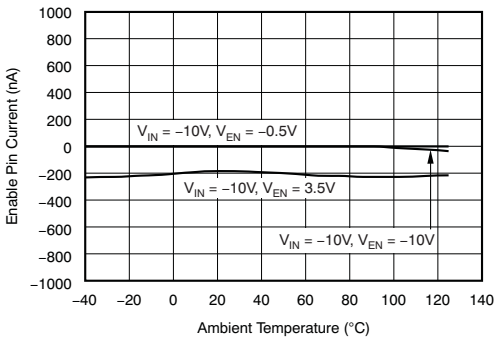


Figure 12. Enable Pin Current vs Junction Temperature

Typical Characteristics (continued)

TPS72325 at $V_I = V_{O(NOM)} – 0.5$ V, $I_O = 1$ mA, $V_{EN} = 1.5$ V, $C_O = 2.2$ µF, and $C_{NR} = 0.01$ µF, unless otherwise noted.

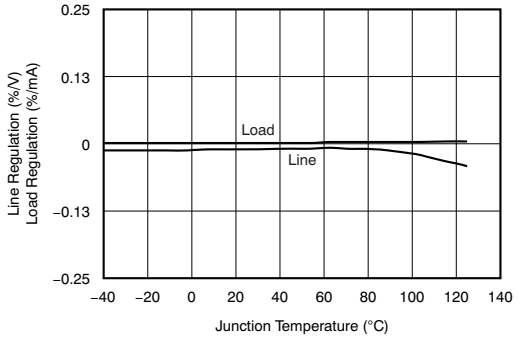


Figure 13. Line And Load Regulation vs Junction Temperature

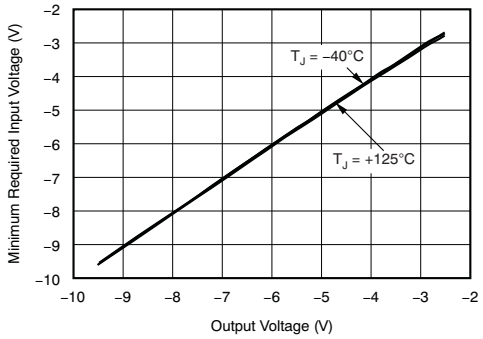


Figure 14. TPS72301 Minimum Required Input Voltage vs Output Voltage

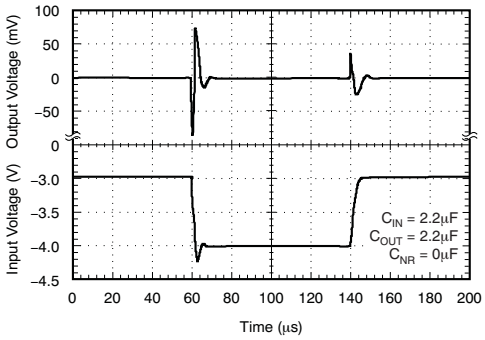


Figure 15. TPS72325 Line Transient Response

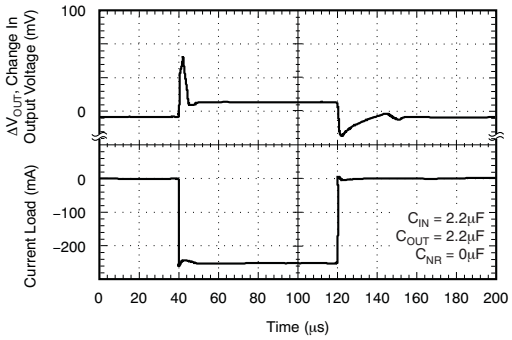


Figure 16. TPS72325 Load Transient Response

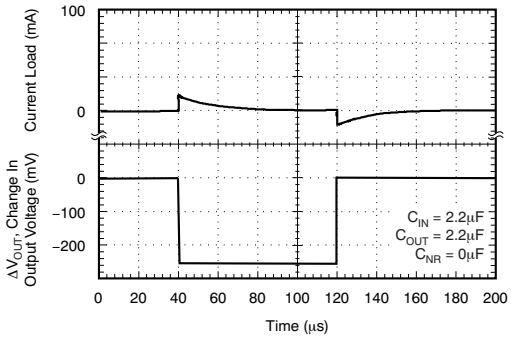


Figure 17. TPS72325 Load Transient Response

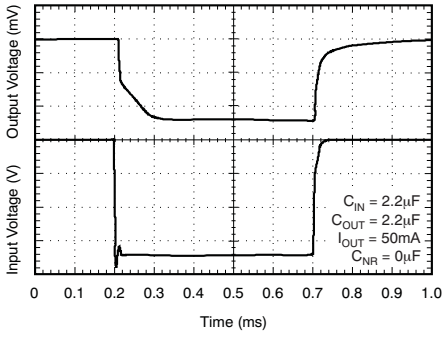


Figure 18. TPS72325 Start-Up Response

Typical Characteristics (continued)

TPS72325 at $V_I = V_{O(NOM)} - 0.5$ V, $I_O = 1$ mA, $V_{EN} = 1.5$ V, $C_O = 2.2$ µF, and $C_{NR} = 0.01$ µF, unless otherwise noted.

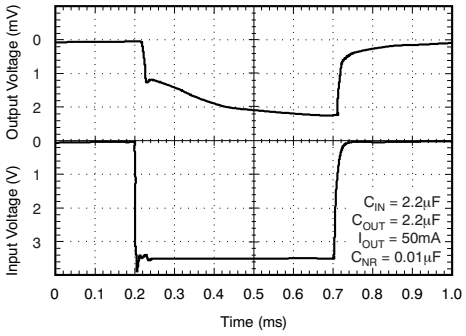


Figure 19. TPS72325 Start-Up Response

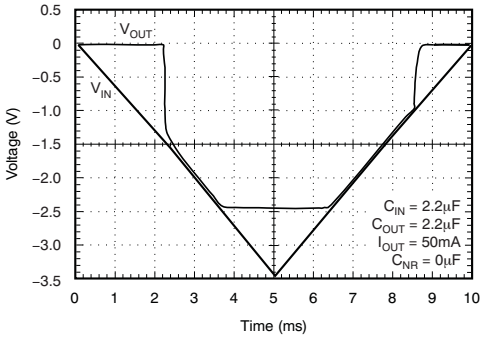


Figure 20. TPS72325 Power-Up/Power-Down

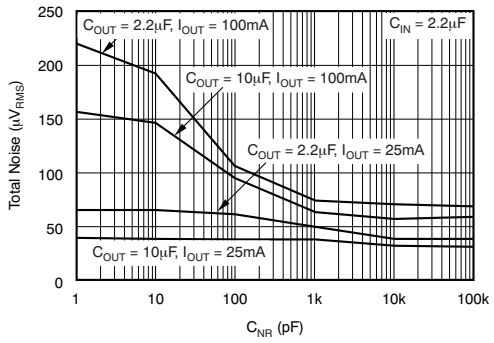


Figure 21. TPS72325 Total Noise vs C_{NR} (10 Hz to 100 kHz)

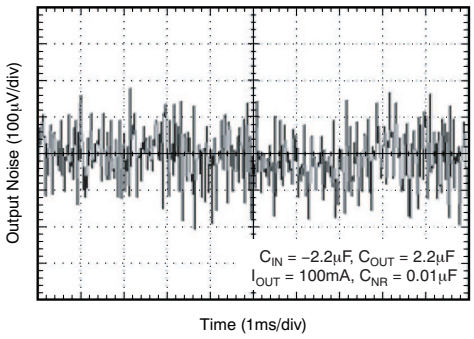


Figure 22. TPS72325 Output Noise vs Time

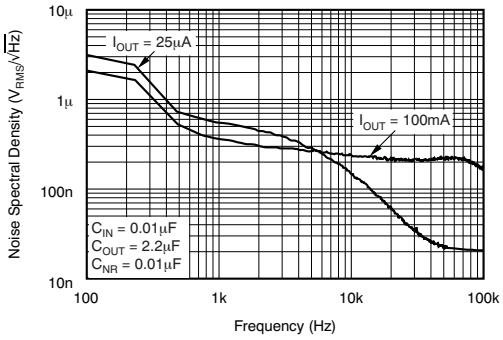


Figure 23. TPS72325 Noise Spectral Density vs Frequency

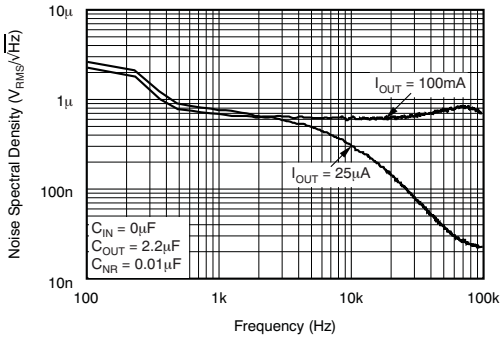


Figure 24. TPS72325 Noise Spectral Density vs Frequency

Typical Characteristics (continued)

TPS72325 at $V_I = V_{O(NOM)} – 0.5$ V, $I_O = 1$ mA, $V_{EN} = 1.5$ V, $C_O = 2.2$ µF, and $C_{NR} = 0.01$ µF, unless otherwise noted.

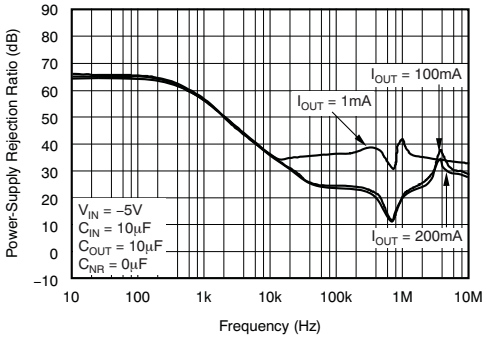


Figure 25. PSRR vs Frequency

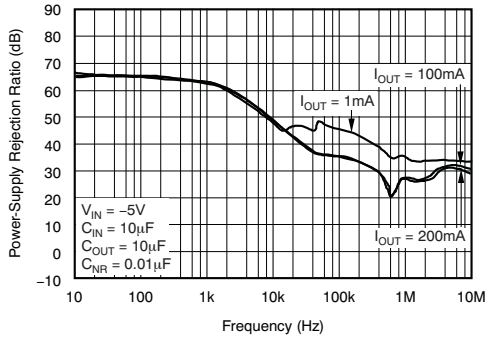


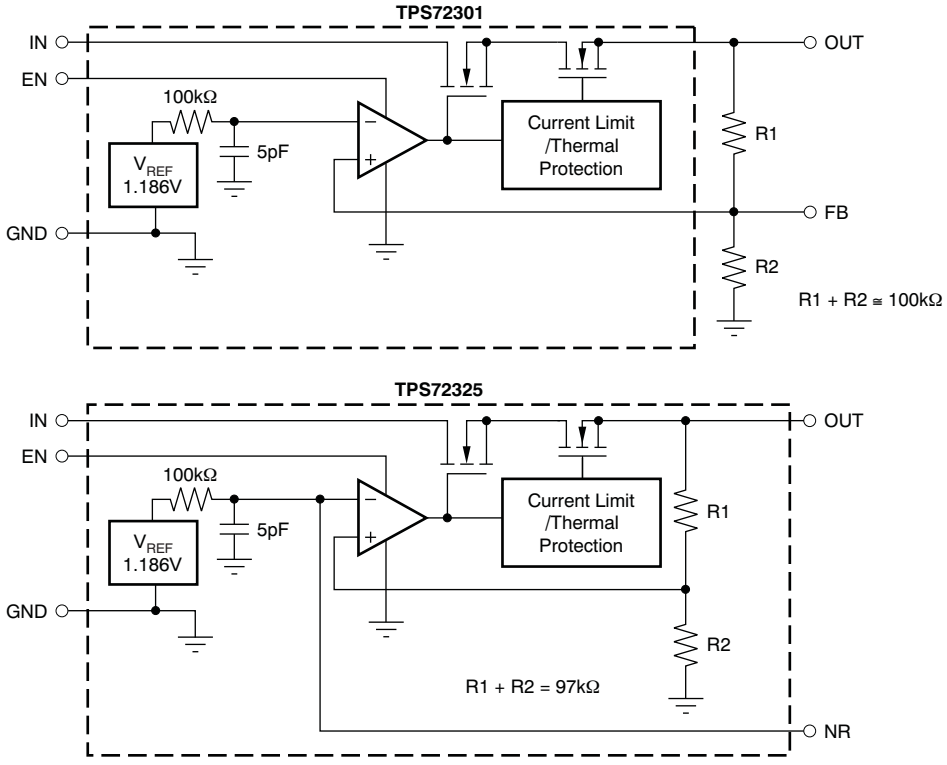
Figure 26. PSRR vs Frequency

7 Detailed Description

7.1 Overview

The TPS723 is a low-dropout, negative linear voltage regulator with a rated current of 200 mA. It is offered in trimmed output voltages between –1.5 V and –5.2 V and as an adjustable regulator from –1.2 V to –10 V. The device features very low noise and high power-supply rejection ratio (PSRR), making the TPS723 ideal for high-sensitivity analog and RF applications. A shutdown mode is available, reducing ground current to 2-μA maximum over temperature and process.

7.2 Functional Block Diagrams



7.3 Feature Description

7.3.1 Current Limit

The TPS723 has internal circuitry that monitors and limits output current to protect the regulator from damage under all load conditions. When output current reaches the output current limit (550 mA typical), protection circuitry turns on, reducing output voltage to ensure that current does not increase. See Figure 9 in the *Typical Characteristics* section.

Do not drive the output more than 0.3 V above the input. An output voltage more than 0.3 V above the input voltage biases the body diode in the pass FET, and allows current to flow from the output to the input. This current is not limited by the device. If this condition is expected, make sure to externally limit the reverse current.

7.3.2 Enable

The enable pin is active above +1.5 V and below –1.5 V, allowing it to be controlled by a standard TTL signal or by connection to V_I if not used. When driven to GND most internal circuitry is turned off, putting the TPS723 into shutdown mode, drawing 2-μA maximum ground current.

7.4 Device Functional Modes

Driving EN over 1.5 V or below –1.5 V turns on the regulator. Driving EN between –1.5 V and +1.5 V puts the regulator into shutdown mode, thus reducing the operating current to 100 nA, nominal.

8 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

The TPS723 LDO regulator provides high PSRR and low noise. These features make the device a good fit for high-sensitivity analog and RF applications.

8.2 Typical Application

The TPS72301 allows designers to specify any output voltage from –10 V to –1.2 V. As shown in the application circuit in Figure 27, an external resistor divider is used to scale the output voltage (V_O) to the reference voltage. For best accuracy, use precision resistors for R1 and R2. Use the equations in Figure 27 to determine the values for the resistor divider.

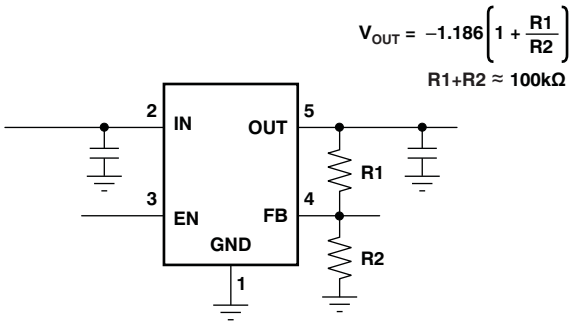


Figure 27. TPS72301 Adjustable LDO Regulator Programming

8.2.1 Design Requirements

8.2.1.1 Capacitor Selection for Stability

Appropriate input and output capacitors should be used for the intended application. The TPS723 only requires a 2.2-µF ceramic output capacitor to be used for stable operation. Both the capacitor value and equivalent series resistance (ESR) affect stability, output noise, PSRR, and transient response. For typical applications, a 2.2-µF ceramic output capacitor located close to the regulator is sufficient.

8.2.1.2 Output Noise

Without external bypassing, output noise of the TPS723 from 10 Hz to 100 kHz is 200 μV_{RMS} typical. The dominant contributor to output noise is the internal bandgap reference. Adding an external 0.01-µF capacitor to ground reduces noise to 60 μV_{RMS}. Best noise performance is achieved using appropriate low ESR capacitors for bypassing noise at the NR and OUT pins. See Figure 21 in the *Typical Characteristics* section.

8.2.1.3 Power-Supply Rejection

The TPS723 offers a very high PSRR for applications with noisy input sources or highly sensitive output supply lines. For best PSRR, use high-quality input and output capacitors.

8.2.2 Detailed Design Procedure

Select the desired device based on the output voltage.

Provide an input supply with adequate headroom to account for dropout and output current to account for the GND terminal current, and power the load.

Typical Application (continued)

8.2.3 Application Curves

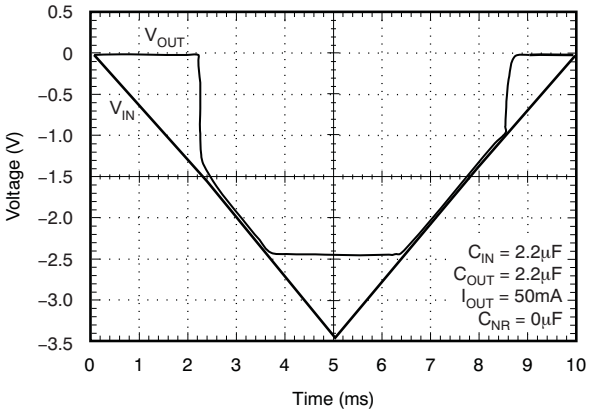


Figure 28. TPS72325 Power-Up/Power-Down

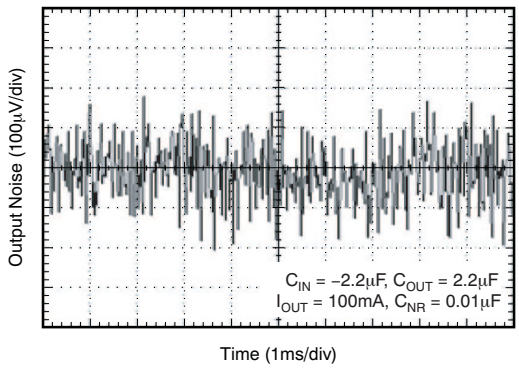


Figure 29. TPS72325 Output Noise vs Time

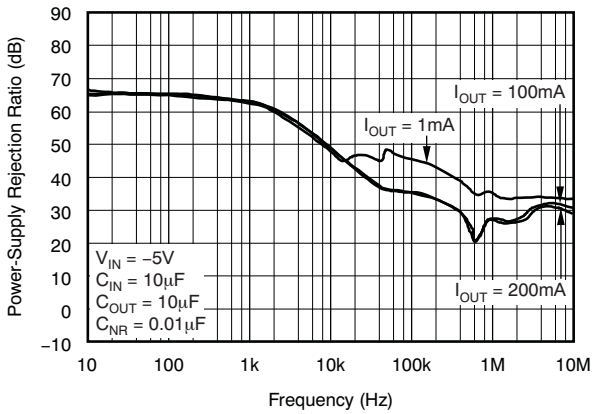


Figure 30. PSRR vs Frequency

8.3 What to Do and What Not to Do

Do place at least one 2.2-µF ceramic capacitor as close as possible to the OUT terminal of the regulator.

Do not place the output capacitor more than 10 mm away from the regulator.

Do connect a 0.1-µF to 2.2-µF low ESR capacitor across the IN terminal and GND input of the regulator.

Do not exceed the absolute maximum ratings.

9 Power Supply Recommendations

These devices are designed to operate from an input voltage supply range between –10 V and –2.7 V. The input voltage range must provide adequate headroom in order for the device to have a regulated output. This input supply must be well-regulated and stable. If the input supply is noisy, additional input capacitors with low ESR can help improve the output noise performance.

10 Layout

10.1 Layout Guidelines

To improve ac performance (such as PSRR, output noise, and transient response), design the board with separate ground planes for V_I and V_O, with each ground plane connected only at the GND pin of the device. In addition, connect the bypass capacitor directly to the GND pin of the device.

10.1.1 Power Dissipation

The ability to remove heat from the die is different for each package type, presenting different considerations in the printed circuit board (PCB) layout. The PCB area around the device that is free of other components moves the head from the device to the ambient air. Performance data for JEDEC low- and high-K boards are given in the *Thermal Information* table near the front of this data sheet. Using heavier copper increases the effectiveness in removing heat from the device. The addition of plated through-holes to heat-dissipating layers also improves heatsink effectiveness. Power dissipation depends on input voltage and load conditions. Power dissipation is equal to the product of the output current times the voltage drop across the output pass element, as shown in Equation 1:

$$P_D = \left(V_{IN} - V_{OUT}\right) \cdot I_{OUT} \quad (1)$$

10.1.2 Thermal Protection

As protection from damage due to excessive junction temperatures, the TPS723 has internal protection circuitry. When junction temperature reaches approximately 165°C, the output device is turned off. After the device has cooled to 145°C, the output device is enabled, allowing normal operation. For reliable operation, design is for worst-case junction temperature of ≤ 125°C taking into account worst-case ambient temperature and load conditions.

10.2 Layout Example

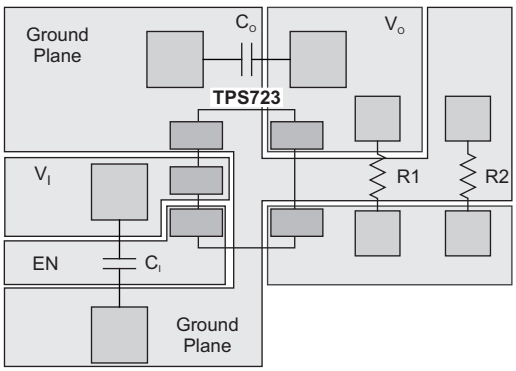


Figure 31. Example Layout

11 Device and Documentation Support

11.1 Device Support

11.1.1 Development Support

11.1.1.1 Spice Models

Computer simulation of circuit performance using SPICE is often useful when analyzing the performance of analog circuits and systems. A SPICE model for the TPS723xx is available through the product folders under *Simulation Models*.

11.1.2 Device Nomenclature

Table 1. Device Nomenclature(1)

PRODUCT	V_{OUT}
TPS723**xx** ***yyy z***	**XX** is nominal output voltage (for example, 25 = 2.5 V, 01 = Adjustable). **YYY** is package designator. **Z** is package quantity.

(1) For the most current package and ordering information see the Package Option Addendum at the end of this document, or visit the device product folder at www.ti.com.

11.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

11.3 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

11.4 Trademarks

E2E is a trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

11.5 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

11.6 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TPS72301DBVR	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	T08I
TPS72301DBVR.A	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	T08I
TPS72301DBVRG4	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	T08I
TPS72301DBVRG4.A	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	T08I
TPS72301DBVT	Obsolete	Production	SOT-23 (DBV) | 5	-	-	Call TI	Call TI	-40 to 125	T08I
TPS72301DDCR	Active	Production	SOT-23-THIN (DDC) | 5	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	T08I
TPS72301DDCR.A	Active	Production	SOT-23-THIN (DDC) | 5	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	T08I
TPS72301DDCT	Active	Production	SOT-23-THIN (DDC) | 5	250 | SMALL T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	T08I
TPS72301DDCT.A	Active	Production	SOT-23-THIN (DDC) | 5	250 | SMALL T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	T08I
TPS72301DRVR	Active	Production	WSON (DRV) | 6	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	1TLM
TPS72301DRVR.A	Active	Production	WSON (DRV) | 6	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	1TLM
TPS72301DRVT	Active	Production	WSON (DRV) | 6	250 | SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	1TLM
TPS72301DRVT.A	Active	Production	WSON (DRV) | 6	250 | SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	1TLM
TPS72325DBVR	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	T02I
TPS72325DBVR.A	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	T02I
TPS72325DBVRG4	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	T02I
TPS72325DBVRG4.A	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	T02I

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

OTHER QUALIFIED VERSIONS OF TPS723 :

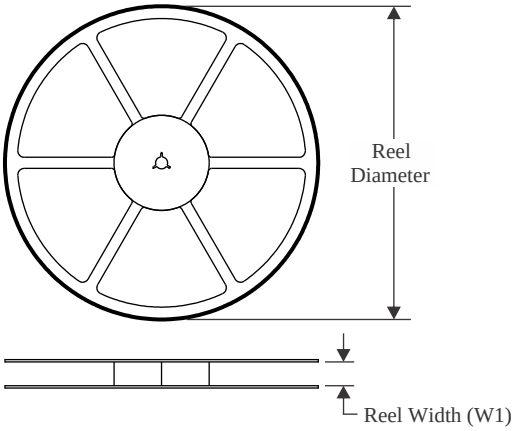
- Automotive : TPS723-Q1

NOTE: Qualified Version Definitions:

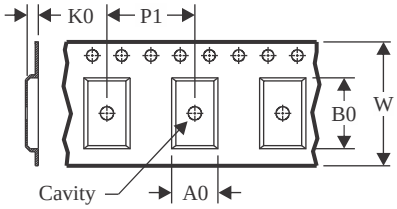
- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects

TAPE AND REEL INFORMATION

REEL DIMENSIONS

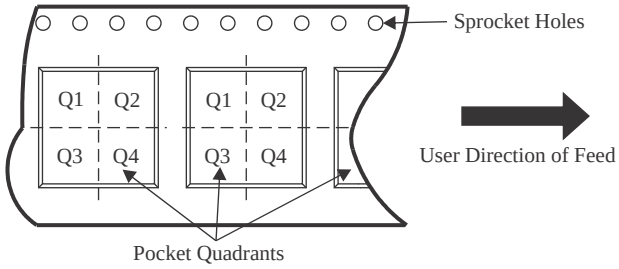


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

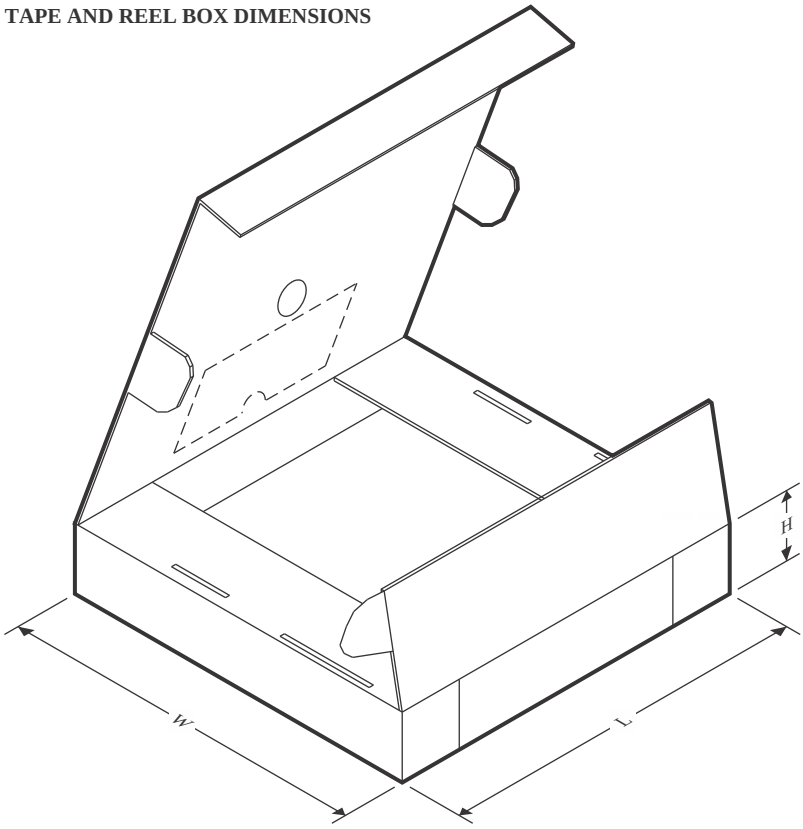
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS72301DBVR	SOT-23	DBV	5	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TPS72301DBVRG4	SOT-23	DBV	5	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TPS72301DDCR	SOT-23-THIN	DDC	5	3000	179.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TPS72301DDCT	SOT-23-THIN	DDC	5	250	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TPS72301DRVR	WSON	DRV	6	3000	178.0	8.4	2.25	2.25	1.0	4.0	8.0	Q2
TPS72301DRVT	WSON	DRV	6	250	178.0	8.4	2.25	2.25	1.0	4.0	8.0	Q2
TPS72325DBVR	SOT-23	DBV	5	3000	179.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TPS72325DBVRG4	SOT-23	DBV	5	3000	179.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

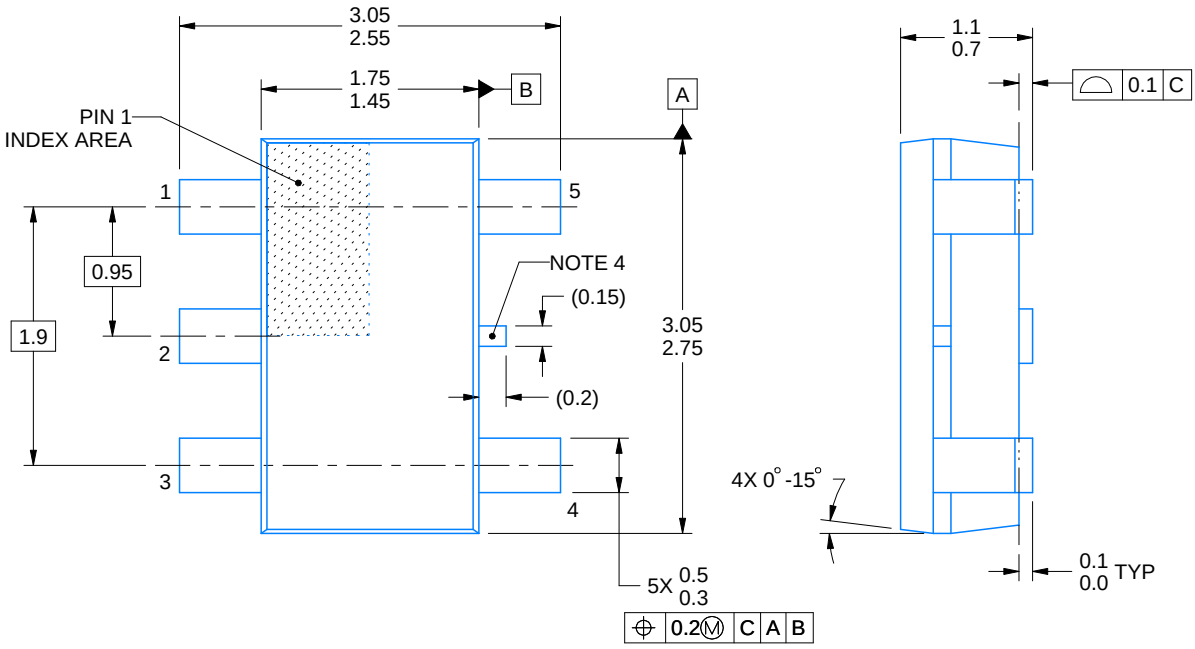
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS72301DBVR	SOT-23	DBV	5	3000	200.0	183.0	25.0
TPS72301DBVRG4	SOT-23	DBV	5	3000	200.0	183.0	25.0
TPS72301DDCR	SOT-23-THIN	DDC	5	3000	213.0	191.0	35.0
TPS72301DDCT	SOT-23-THIN	DDC	5	250	213.0	191.0	35.0
TPS72301DRVR	WSON	DRV	6	3000	205.0	200.0	33.0
TPS72301DRVT	WSON	DRV	6	250	205.0	200.0	33.0
TPS72325DBVR	SOT-23	DBV	5	3000	200.0	183.0	25.0
TPS72325DBVRG4	SOT-23	DBV	5	3000	200.0	183.0	25.0

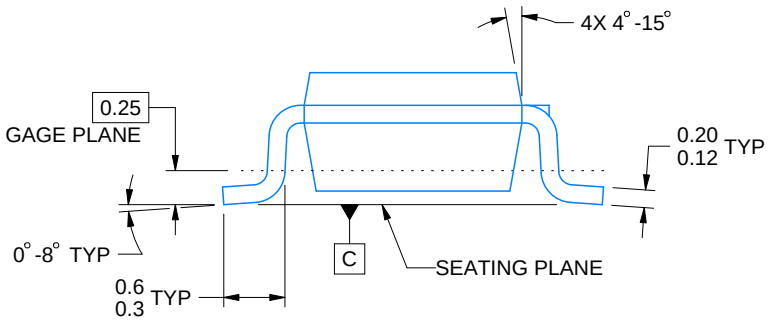
PACKAGE OUTLINE

DDC0005A

SOT-23 - 1.1 max height

SMALL OUTLINE TRANSISTOR

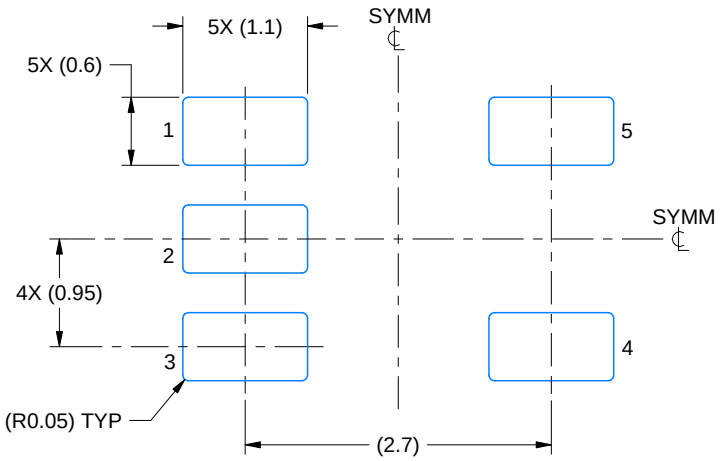




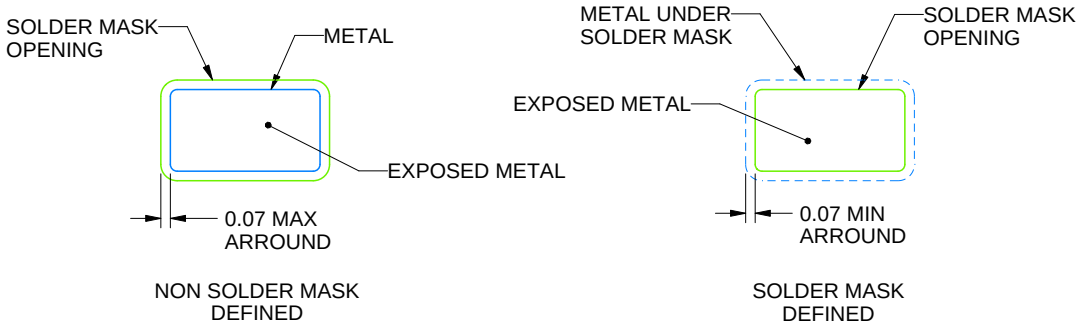
4220752/C 08/2024

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Reference JEDEC MO-193.
4. Support pin may differ or may not be present.



LAND PATTERN EXAMPLE
EXPLOSED METAL SHOWN
SCALE:15X

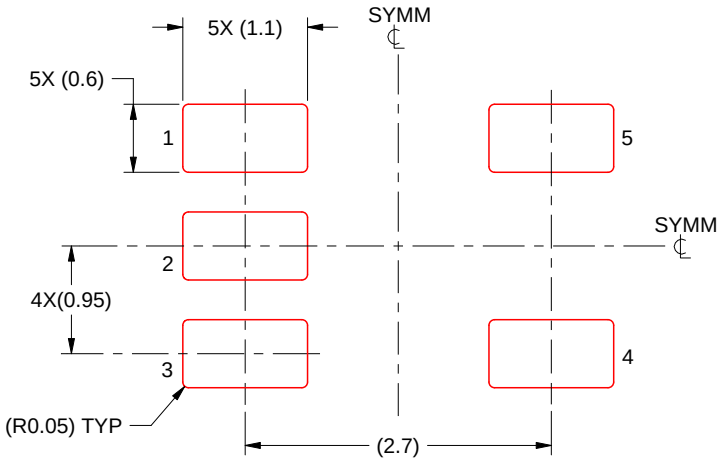


SOLDERMASK DETAILS

4220752/C 08/2024

NOTES: (continued)

4. Publication IPC-7351 may have alternate designs.
5. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 THICK STENCIL
SCALE:15X

4220752/C 08/2024

NOTES: (continued)

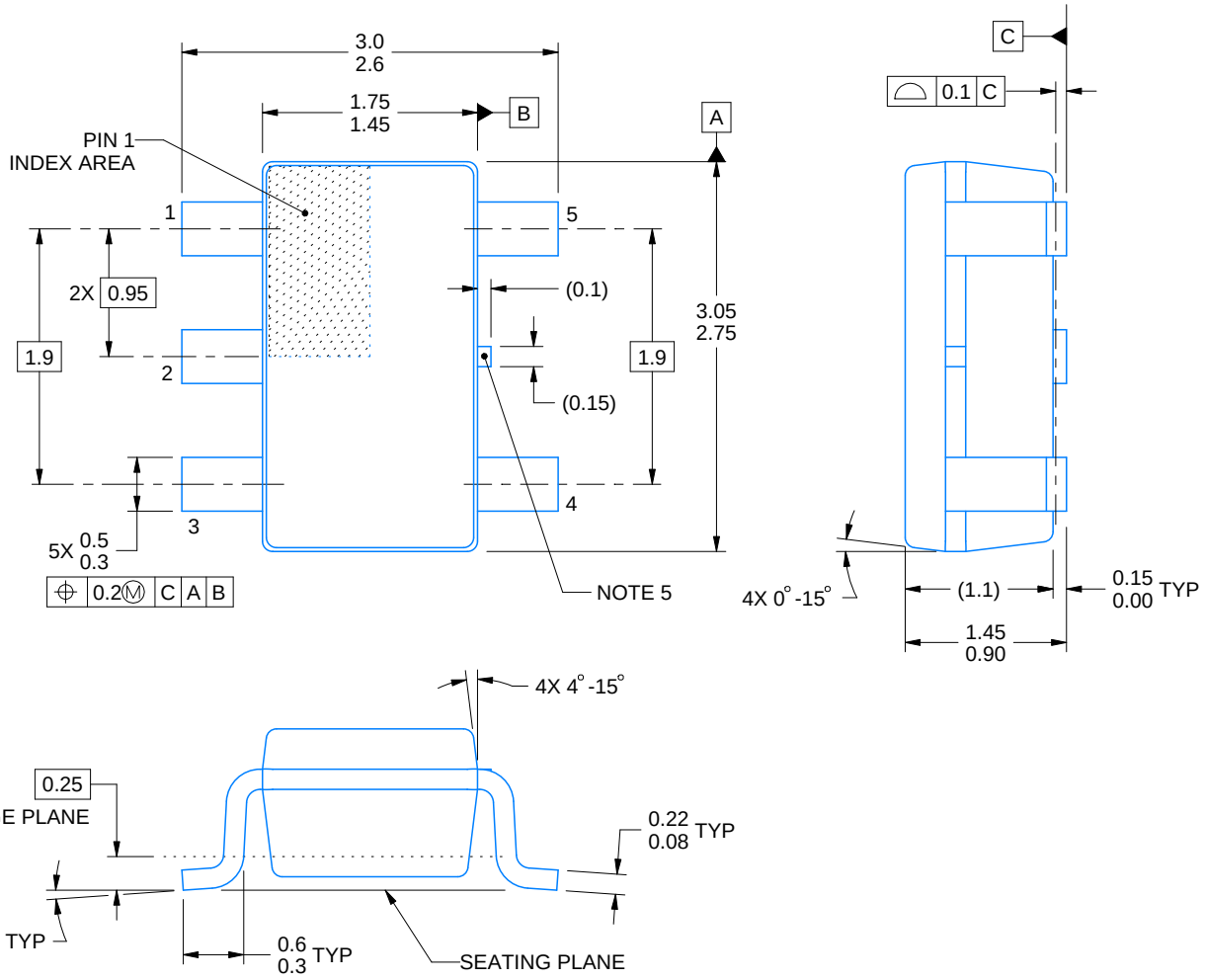
6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
7. Board assembly site may have different recommendations for stencil design.

PACKAGE OUTLINE

DBV0005A

SOT-23 - 1.45 mm max height

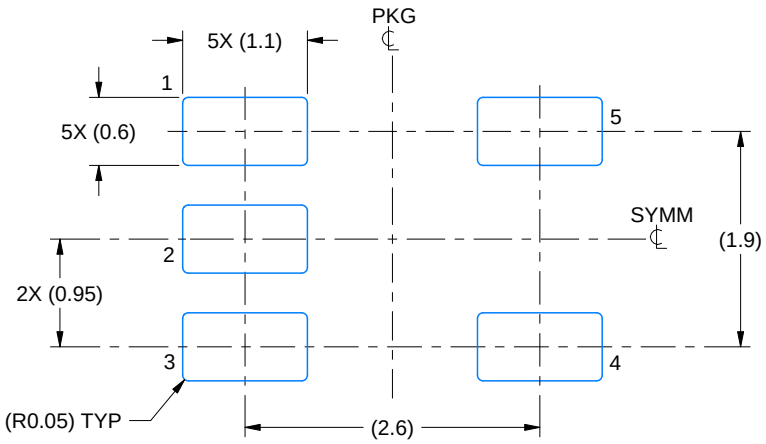
SMALL OUTLINE TRANSISTOR



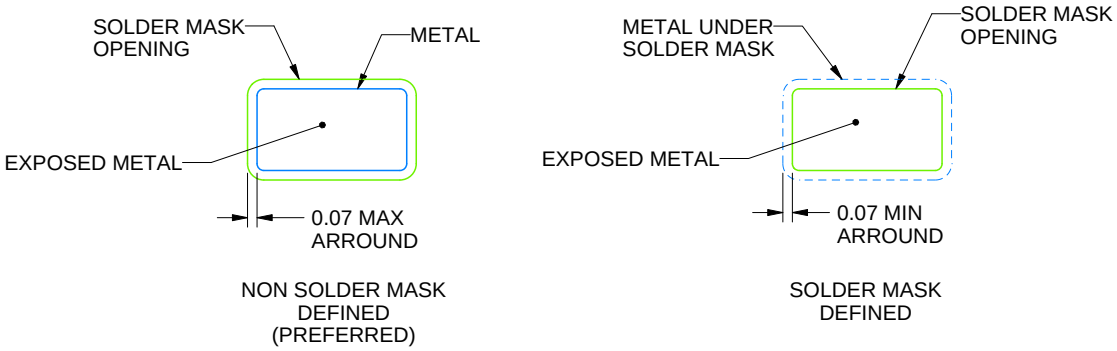
4214839/K 08/2024

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Refernce JEDEC MO-178.
4. Body dimensions do not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.25 mm per side.
5. Support pin may differ or may not be present.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X

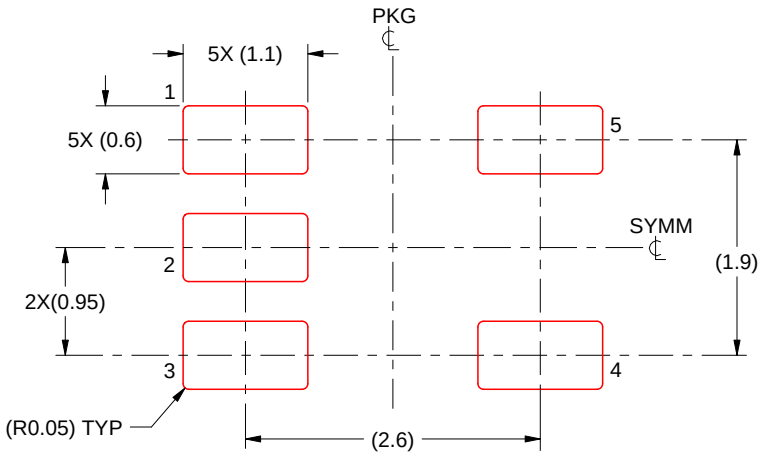


SOLDER MASK DETAILS

4214839/K 08/2024

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:15X

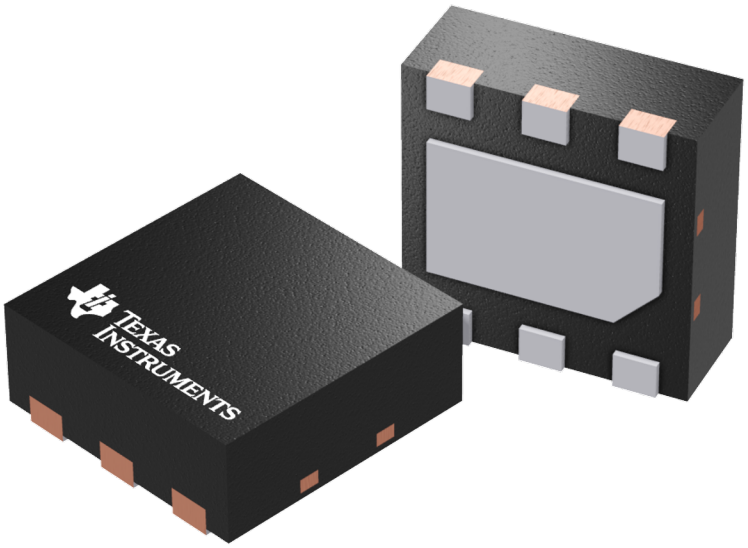
4214839/K 08/2024

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

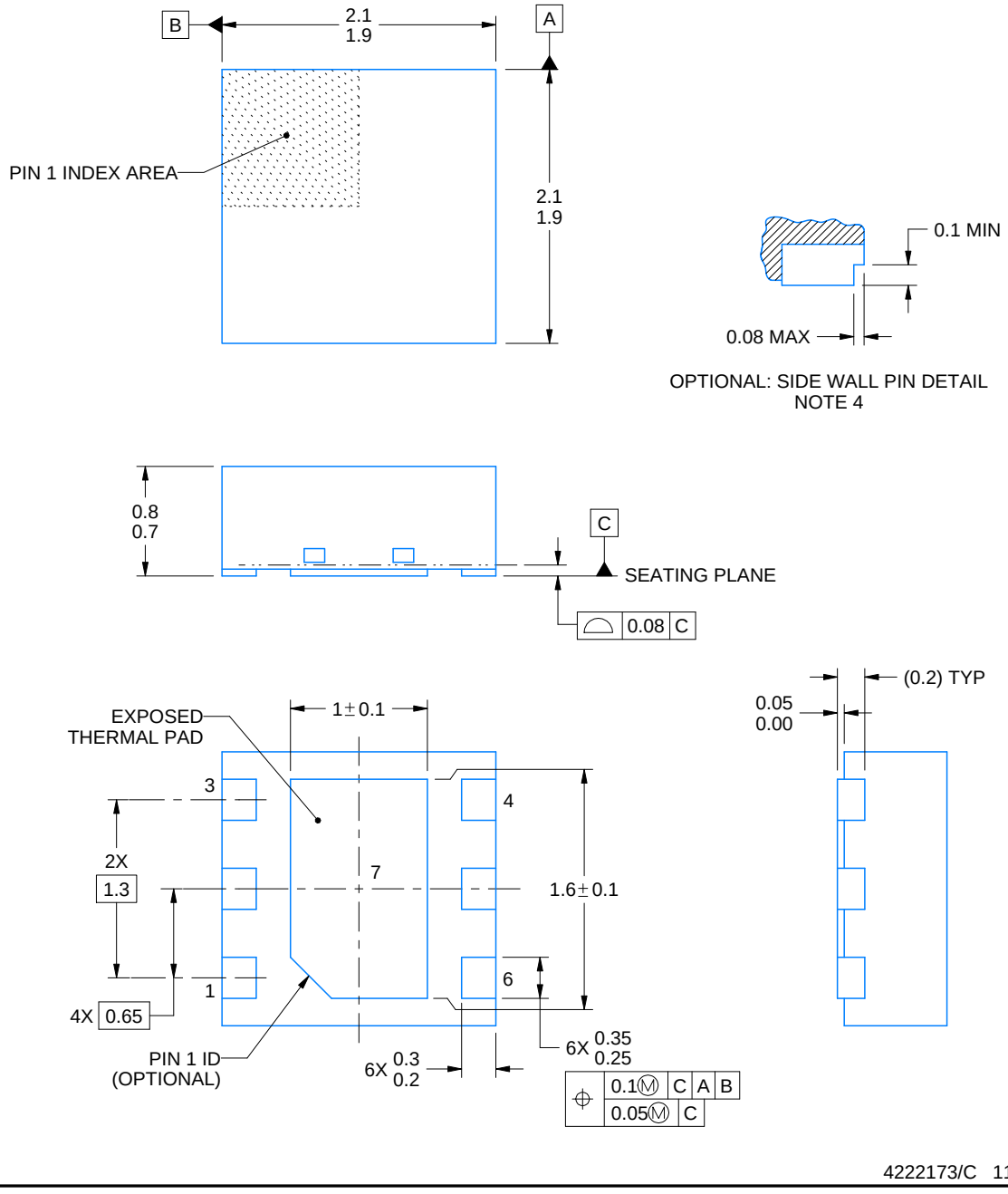
DRV 6 WSON - 0.8 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



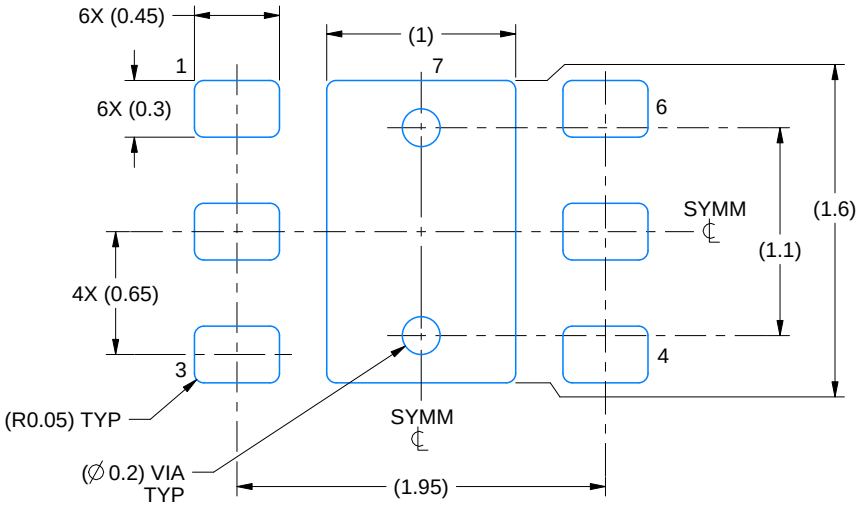
Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

PLASTIC SMALL OUTLINE - NO LEAD

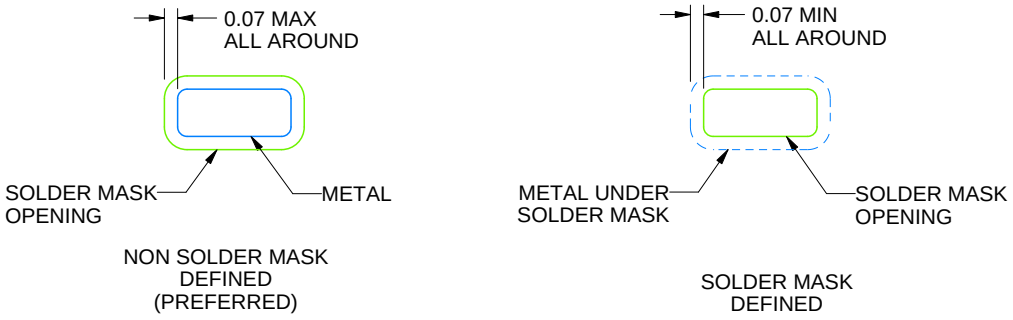


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.
4. Minimum 0.1 mm solder wetting on pin side wall. Available for wettable flank version only.



LAND PATTERN EXAMPLE
SCALE:25X



SOLDER MASK DETAILS

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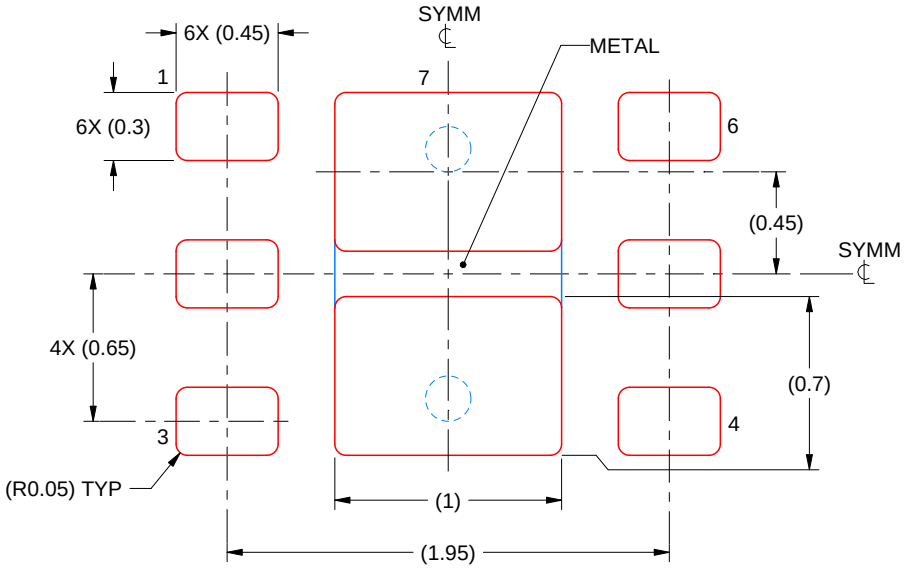
NOTES: (continued)

5. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
6. Vias are optional depending on application, refer to device data sheet. If some or all are implemented, recommended via locations are shown.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD #7
88% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:30X

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NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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Last updated 10/2025