200mA Low-Dropout Linear Regulator with Pin-Selectable Dual-Voltage Level Output

FEATURES

- **Very Low Dropout: 230mV Typical at 200mA**
- **3% Accuracy Over Load/Line/Temperature**
- **Low I_Q: 50µA in Active Mode**
- **Available in Fixed-Output Voltages From 0.9V to 3.6V Using Innovative Factory EEPROM Programming**
- **VSET Pin Toggles Output Voltage Between Two Preset Levels**
  - **Preset Output Voltage Levels Can Be EEPROM-Programmed To Any Combination**
- **High PSRR: 65dB at 1kHz**
- **Stable with a 1.0µF Ceramic Capacitor**
- **Thermal Shutdown and Over-Current Protection**
- **Available in Wafer-Level Chip Scale and 2mm x 2mm SON Packages**

APPLICATIONS

- **Power Rails with Programming Mode**
- **Dual Voltage Levels for Power-Saving Mode**
- **Leakage Reduction for 90nm and 65nm Processors**
- **Wireless Handsets, Smart Phones, PDAs**
- **MP3 Players and Other Handheld Products**

DESCRIPTION

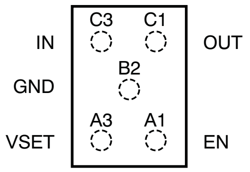
The TPS728xx series of low-dropout linear regulators (LDOs), with a selectable dual-voltage level output, is designed specially for applications that require two levels of output voltage regulation. Programming fuses and memory cards, reducing leakage effects, and conserving power in nanometric processes are some application examples.

The VSET pin is used to select one of two output voltage levels preset through innovative factory EEPROM programming. A precision bandgap and error amplifier provides an overall 3% accuracy over load, line, and temperature extremes.

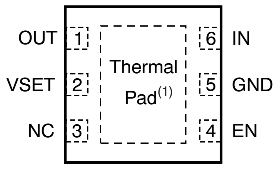
Ultra-small wafer chip scale (WCSP) and 2mm x 2mm SON packages make the TPS728xx series ideal for handheld applications.

This family of devices is fully specified over a temperature range of T_J = –40°C to +125°C.

TPS728xx Series
YZU PACKAGE
WCSP-5
(TOP VIEW)



TPS728xx Series
DRV PACKAGE
2mm x 2mm SON-6
(TOP VIEW)



(1) It is recommended that the SON package thermal pad be connected to ground.

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

ORDERING INFORMATION(1)

PRODUCT	V_{OUT} (2)
TPS728**vvvxxx*yyyz***	**VVV** is the nominal output voltage for V_{OUT1} and corresponds to V_{SET} = Low. **XXX** is the nominal output voltage for V_{OUT2} and corresponds to V_{SET} = High. **YYY** is package designator. **Z** is Tape and reel quantity (R = 3000, T = 250).

(1) For the most current package and ordering information see the Package Option Addendum at the end of this document, or see the TI website at www.ti.com.

(2) Output voltages from 0.9V to 3.6V in 50mV increments are available through the use of innovative factory EEPROM programming; minimum order quantities may apply. Contact factory for details and availability.

ABSOLUTE MAXIMUM RATINGS(1)

At T_J = –40°C to +125°C (unless otherwise noted). All voltages are with respect to GND.

PARAMETER		TPS728xx Series	UNIT
Input voltage range, V_{IN}		–0.3 to +7.0	V
Enable and VSET voltage range, V_{EN} and V_{SET}		–0.3 to V_{IN} + 0.3(2)	V
Output voltage range, V_{OUT}		–0.3 to +7.0	V
Maximum output current, I_{OUT}		Internally limited	
Output short-circuit duration		Indefinite	
Total continuous power dissipation, P_{DISS}		See Dissipation Ratings Table	
ESD rating	Human body model (HBM)	2	kV
	Charged device model (CDM)	500	V
Operating junction temperature range, T_J		–55 to +150	°C
Storage temperature range, T_{STG}		–55 to +150	°C

(1) Stresses above these ratings may cause permanent damage. Exposure to absolute maximum conditions for extended periods may degrade device reliability. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those specified is not implied.

(2) V_{EN} and V_{SET} absolute maximum rating is V_{IN} + 0.3V or +7.0V, whichever is less.

DISSIPATION RATINGS

BOARD	PACKAGE	$R_{\theta JC}$	$R_{\theta JA}$	DERATING FACTOR ABOVE T_A = +25°C	T_A < +25°C	T_A = +70°C	T_A = +85°C
High-K(1)	DRV	20°C/W	65°C/W	15.4mW/°C	1540mW	845mW	615mW
High-K(1)	YZU	85°C/W	268°C/W	3.7mW/°C	370mW	205mW	150mW

(1) The JEDEC high-K (2s2p) board used to derive this data was a 3- × 3-inch, multilayer board with 1-ounce internal power and ground planes and 2-ounce copper traces on top and bottom of the board.

ELECTRICAL CHARACTERISTICS

Over operating temperature range (T_J = –40°C to +125°C), V_{IN} = $V_{OUT(TYP)}$ + 0.5V or 2.7V, whichever is greater; I_{OUT} = 0.5mA, V_{SET} = V_{EN} = V_{IN}, C_{OUT} = 1.0µF, unless otherwise noted. Typical values are at T_J = +25°C.

PARAMETER			TEST CONDITIONS		MIN	TYP	MAX	UNIT
V_{IN}	Input voltage range				2.7		6.5	V
V_{OUT}(1)	DC output accuracy	Nominal	T_J = +25°C, V_{SET} = high/low		–2.5		+2.5	mV
		Over V_{IN}, I_{OUT}, temperature	V_{OUT} + 0.5V ≤ V_{IN} ≤ 6.5V, 0mA ≤ I_{OUT} ≤ 200mA, V_{SET} = high/low		–3.0		+3.0	%
ΔV_{OUT}	Load transient		100µA to 200mA in 1µs, 200mA to 100µA in 1µs, C_{OUT} = 1µF			±60.0		mV
V_O	Output voltage range				0.9		3.6	V
$\Delta V_O/\Delta V_{IN}$	Line regulation		$V_{OUT(NOM)}$ + 0.5V ≤ V_{IN} ≤ 6.5V, I_{OUT} = 5mA			130		µV/V
$\Delta V_O/\Delta I_{OUT}$	Load regulation		0mA ≤ I_{OUT} ≤ 200mA			75		µV/mA
V_{DO}	Dropout voltage(2)		V_{IN} = $V_{OUT(NOM)}$ – 0.1V, I_{OUT} = 200mA			230	400	mV
I_{CL}	Output current limit		V_{OUT} = 0.9 × $V_{OUT(NOM)}$		240	340	575	mA
I_{GND}	Ground pin current		I_{OUT} = 0mA			50	80	µA
			I_{OUT} = 200mA			120		µA
I_{SHDN}	Shutdown current (I_{GND})		V_{EN} ≤ 0.4V, 2.7V ≤ V_{IN} < 4.5V, T_J = –40°C to +85°C			0.10	1.0	µA
PSRR	Power-supply rejection ratio		V_{IN} = 3.8V, V_{OUT} = 2.8V, I_{OUT} = 200mA	f = 100Hz		65		dB
				f = 1kHz		65		dB
				f = 10kHz		55		dB
				f = 100kHz		40		dB
V_N	Output noise voltage		BW = 100Hz to 100kHz, V_{IN} = 3.3V, V_{OUT} = 2.8V, I_{OUT} = 10mA			75 × V_{OUT}		μV_{RMS}
t_{TR}	Transition time (low-to-high) V_{OUT} = V_{OUT_LOW} to V_{OUT_HIGH} V_{OUT} = 97% × V_{OUT_HIGH}		V_{OUT_LOW} = 1.8V, V_{OUT_HIGH} = 3.15V, I_{OUT} = 10mA			60		µs
t_{STR}	Startup time(3)		C_{OUT} = 1.0µF			160		µs
t_{SHUT}	Shutdown time(4)		R_L = ∞, C_{OUT} = 1.0µF, V_{OUT} = 2.8V			180(5)		µs
V_{HI}	VSET high (output V_{OUT2} selected), or enable pin high (enabled)				1.2		V_{IN}	V
V_{LO}	VSET low (output V_{OUT1} selected), or enable pin low (disabled)				0		0.4	V
I_{EN}, I_{VSET}	Enable and select pin currents		EN = VSET = 6.5V			0.04	1.0	µA
UVLO	Undervoltage lockout		V_{IN} rising, V_{SET} = high/low		2.38	2.51	2.65	V
	Hysteresis		V_{IN} falling, V_{SET} = high/low			230		mV
T_{SD}	Thermal shutdown temperature		Shutdown, temperature increasing			+160		°C
			Reset, temperature decreasing			+140		°C
T_J	Operating junction temperature				–40		+125	°C

(1) The output voltage for V_{SET} = low/high is programmed at the factory.
(2) V_{DO} is not measured for devices with $V_{OUT(NOM)}$ < 2.8V because minimum V_{IN} = 2.7V.
(3) Time from V_{EN} = 1.2V to V_{OUT} = 97% ($V_{OUT(NOM)}$).
(4) Time from V_{EN} = 0.4V to V_{OUT} = 5% ($V_{OUT(NOM)}$).
(5) See *Shutdown* in the *Application Information* section for more details.

DEVICE INFORMATION

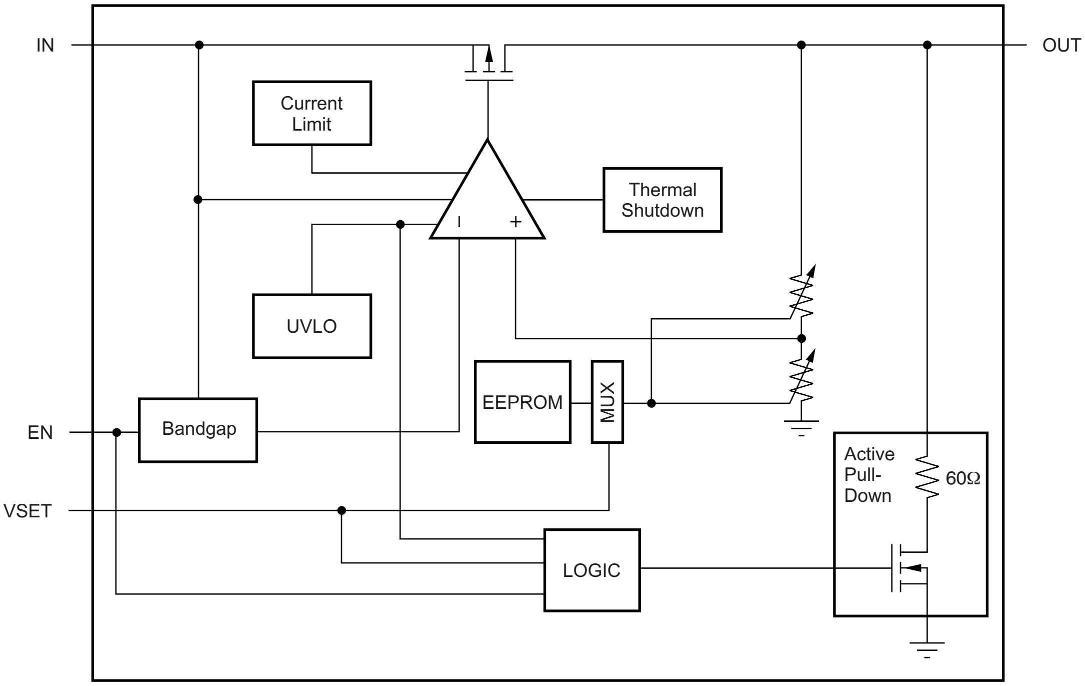
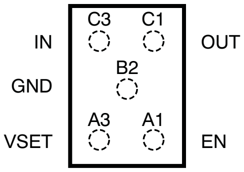
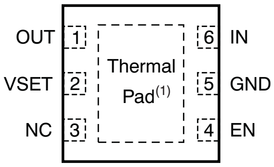


Figure 1. Functional Block Diagram

YZU PACKAGE
WCSP-5
(TOP VIEW)



DRV PACKAGE
SON-8
(TOP VIEW)



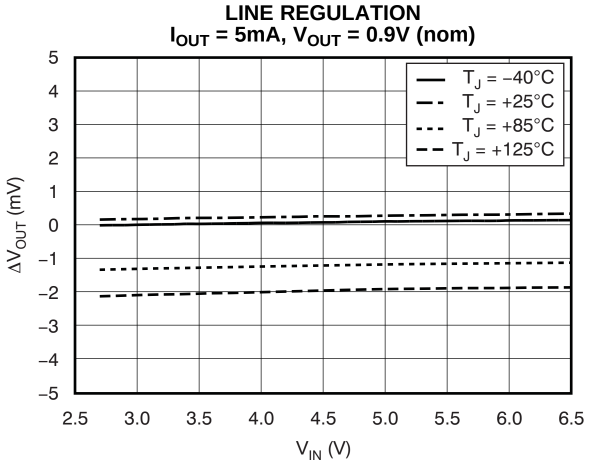
(1) It is recommended that the SON package thermal pad be connected to ground.

PIN DESCRIPTIONS

TPS728xx Series			
NAME	**DRV**	**YZU**	**DESCRIPTION**
OUT	1	C1	Regulated output voltage pin. A small 1μF ceramic capacitor is needed from this pin to ground to assure stability. See *Input and Output Capacitor Requirements* in the *Application Information* section for more details.
VSET	2	A3	Select pin. Driving VSET below 0.4V selects preset output voltage V_{OUT1}. Driving VSET over 1.2V selects preset output voltage V_{OUT2}.
NC	3	—	No connection.
EN	4	A1	Enable pin. Driving EN over 1.2V turns on the regulator. Driving EN below 0.4V puts the regulator into shutdown mode, thus reducing the operating current to 100nA, nominal.
GND	5	B2	Ground pin (connect DRV thermal pad to ground)
IN	6	C3	Input pin. A small capacitor is needed from this pin to ground to assure stability. See *Input and Output Capacitor Requirements* in the *Application Information* section for more details.

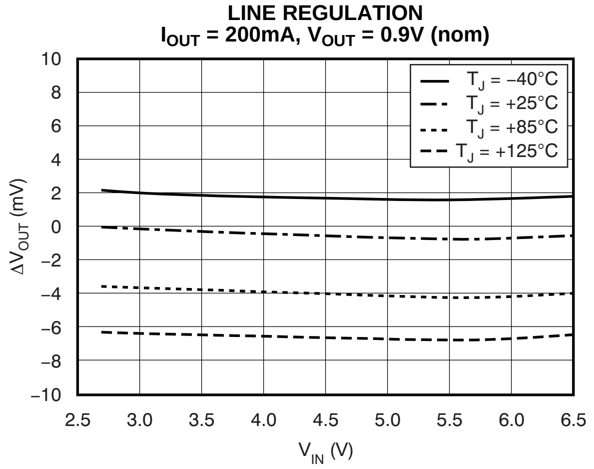
TYPICAL CHARACTERISTICS

Over operating temperature range (T_J = –40°C to +125°C), $V_{IN} = V_{OUT(TYP)}$ + 0.5V or 2.7V, whichever is greater; I_{OUT} = 0.5mA, $V_{EN} = V_{SET} = V_{IN}$, C_{OUT} = 1.0μF, unless otherwise noted. Typical values are at T_J = +25°C.



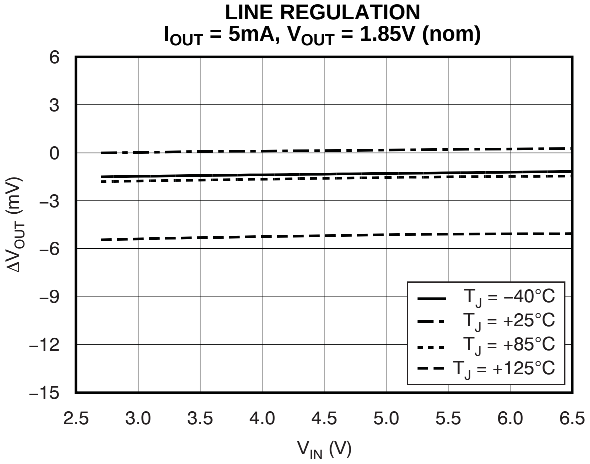
LINE REGULATION
I_{OUT} = 5mA, V_{OUT} = 0.9V (nom)

Figure 2.



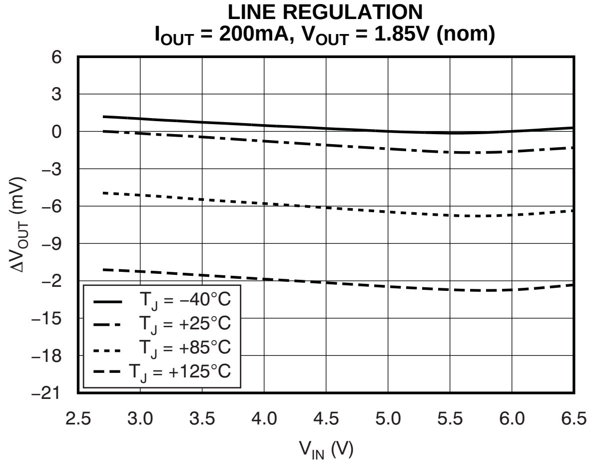
LINE REGULATION
I_{OUT} = 200mA, V_{OUT} = 0.9V (nom)

Figure 3.



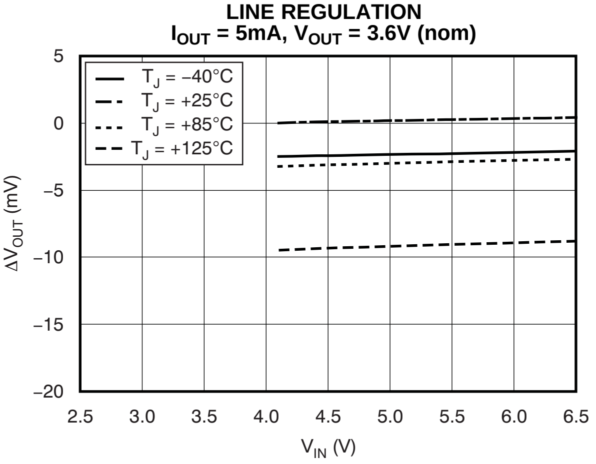
LINE REGULATION
I_{OUT} = 5mA, V_{OUT} = 1.85V (nom)

Figure 4.



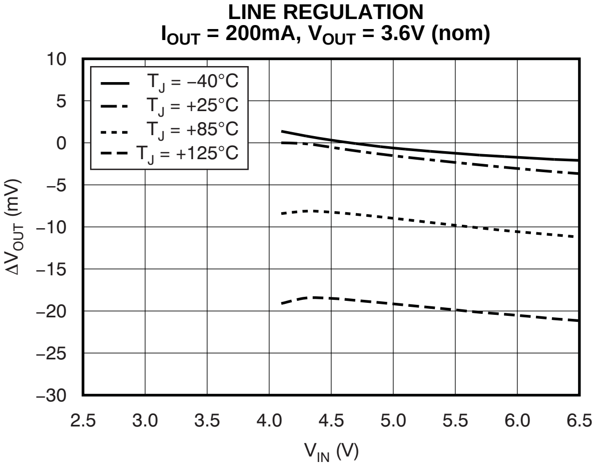
LINE REGULATION
I_{OUT} = 200mA, V_{OUT} = 1.85V (nom)

Figure 5.



LINE REGULATION
I_{OUT} = 5mA, V_{OUT} = 3.6V (nom)

Figure 6.



LINE REGULATION
I_{OUT} = 200mA, V_{OUT} = 3.6V (nom)

Figure 7.

TYPICAL CHARACTERISTICS (continued)

Over operating temperature range (T_J = –40°C to +125°C), $V_{IN} = V_{OUT(TYP)}$ + 0.5V or 2.7V, whichever is greater; I_{OUT} = 0.5mA, $V_{EN} = V_{SET} = V_{IN}$, C_{OUT} = 1.0μF, unless otherwise noted. Typical values are at T_J = +25°C.

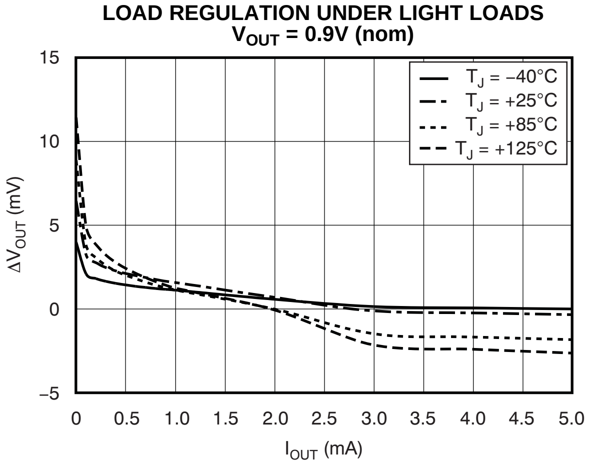

LOAD REGULATION UNDER LIGHT LOADS
V_{OUT} = 0.9V (nom)

Figure 8.

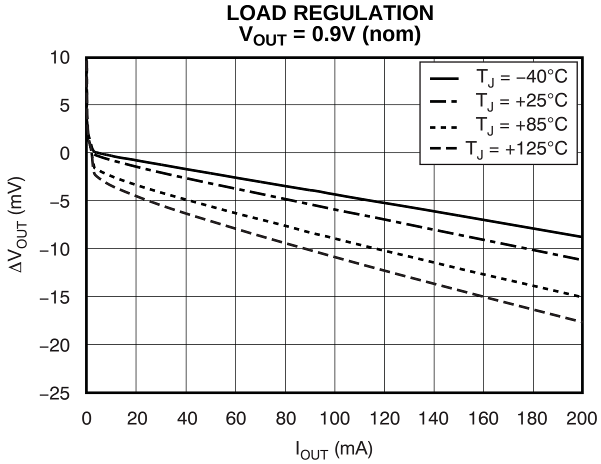

LOAD REGULATION
V_{OUT} = 0.9V (nom)

Figure 9.

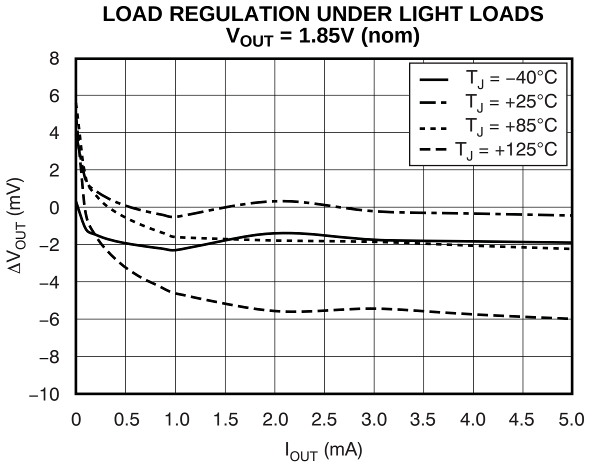

LOAD REGULATION UNDER LIGHT LOADS
V_{OUT} = 1.85V (nom)

Figure 10.

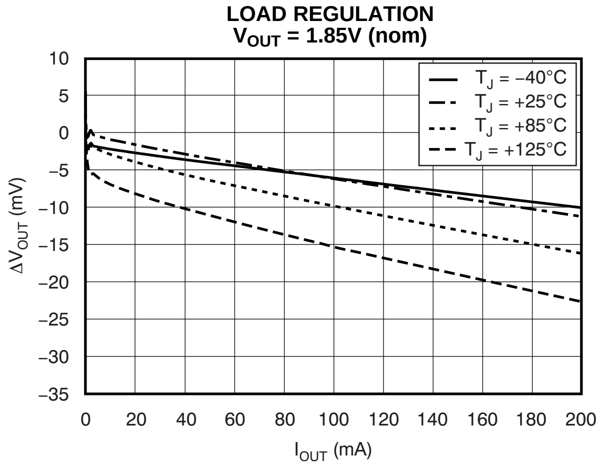

LOAD REGULATION
V_{OUT} = 1.85V (nom)

Figure 11.

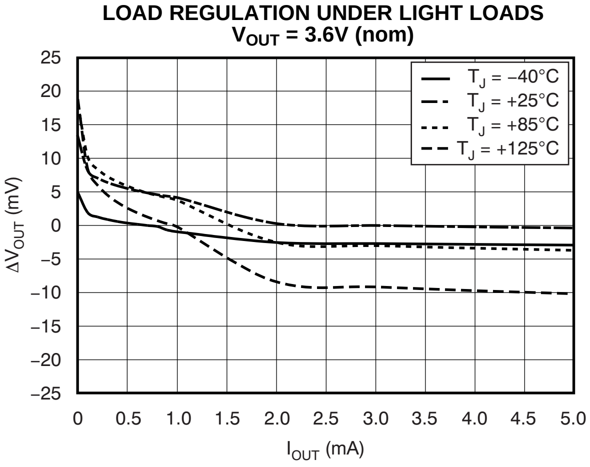

LOAD REGULATION UNDER LIGHT LOADS
V_{OUT} = 3.6V (nom)

Figure 12.

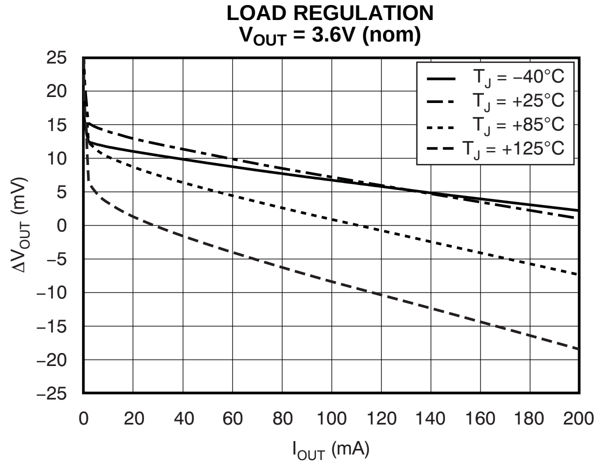

LOAD REGULATION
V_{OUT} = 3.6V (nom)

Figure 13.

TYPICAL CHARACTERISTICS (continued)

Over operating temperature range (T_J = –40°C to +125°C), $V_{IN} = V_{OUT(TYP)}$ + 0.5V or 2.7V, whichever is greater; I_{OUT} = 0.5mA, $V_{EN} = V_{SET} = V_{IN}$, C_{OUT} = 1.0μF, unless otherwise noted. Typical values are at T_J = +25°C.

DROPOUT VOLTAGE
vs OUTPUT CURRENT

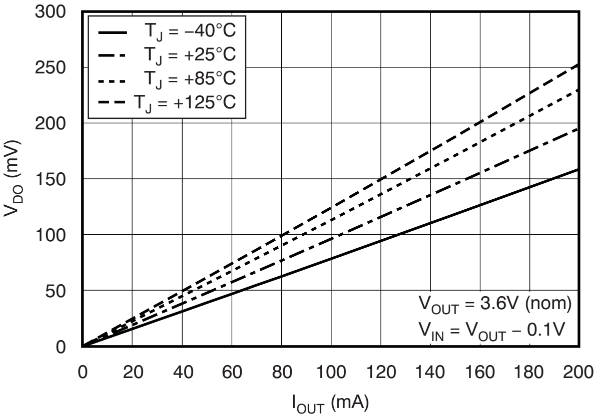


Figure 14.

OUTPUT VOLTAGE
vs TEMPERATURE

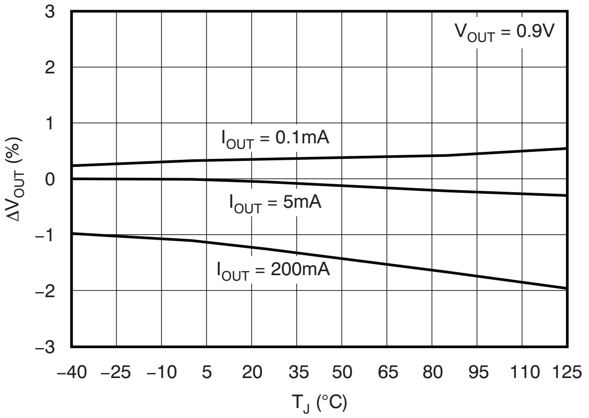


Figure 15.

OUTPUT VOLTAGE
vs TEMPERATURE

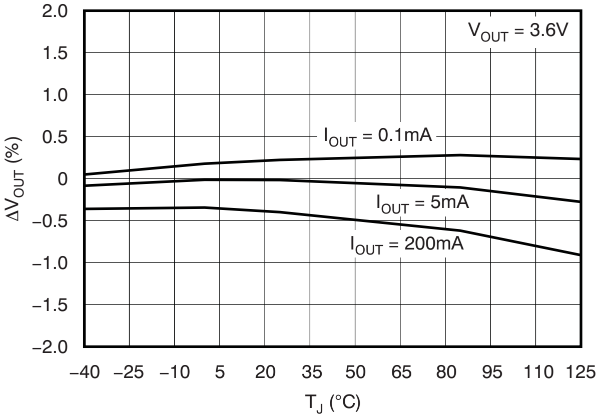


Figure 16.

GROUND PIN CURRENT
vs INPUT VOLTAGE

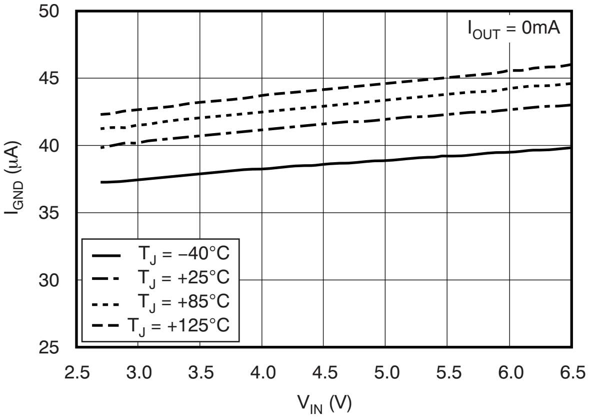


Figure 17.

GROUND PIN CURRENT
vs OUTPUT CURRENT

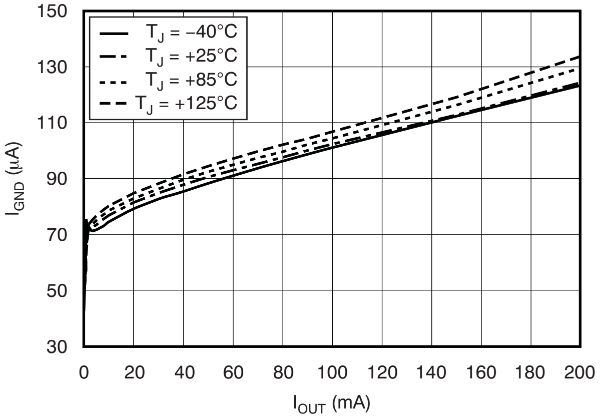


Figure 18.

GROUND PIN CURRENT
vs TEMPERATURE

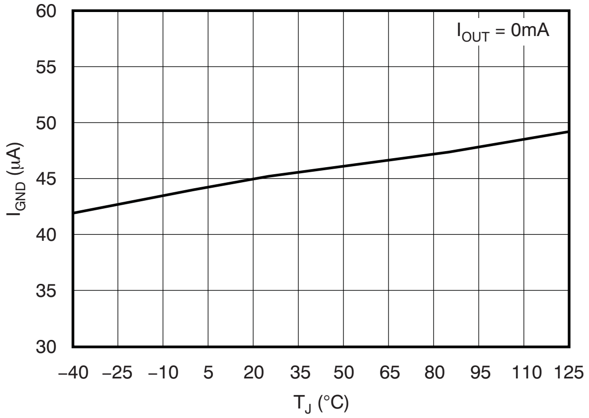


Figure 19.

TYPICAL CHARACTERISTICS (continued)

Over operating temperature range (T_J = –40°C to +125°C), V_{IN} = $V_{OUT(TYP)}$ + 0.5V or 2.7V, whichever is greater; I_{OUT} = 0.5mA, V_{EN} = V_{SET} = V_{IN}, C_{OUT} = 1.0μF, unless otherwise noted. Typical values are at T_J = +25°C.

SHUTDOWN CURRENT vs INPUT VOLTAGE

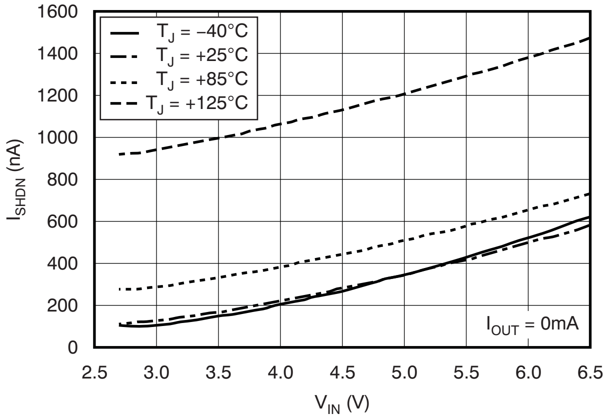


Figure 20.

CURRENT LIMIT vs INPUT VOLTAGE

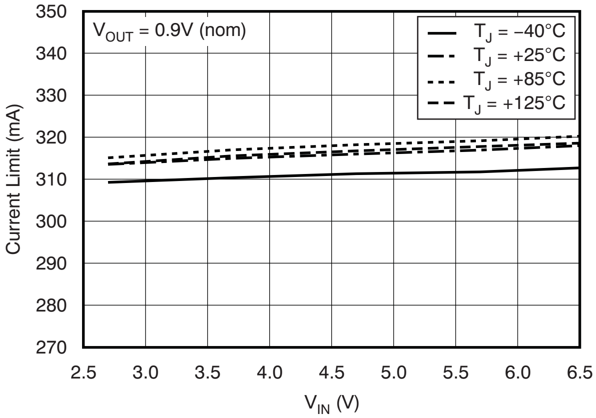


Figure 21.

CURRENT LIMIT vs INPUT VOLTAGE

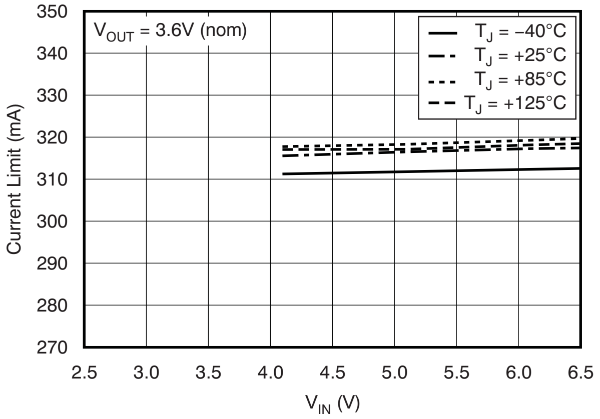


Figure 22.

TPS728185315 POWER-SUPPLY RIPPLE REJECTION vs FREQUENCY (V_{IN} – V_{OUT} = 0.85V)

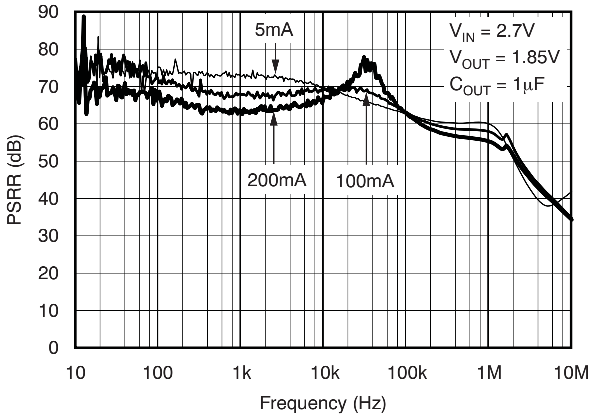


Figure 23.

TPS728185315 POWER-SUPPLY RIPPLE REJECTION vs FREQUENCY (V_{IN} – V_{OUT} = 1.0V)

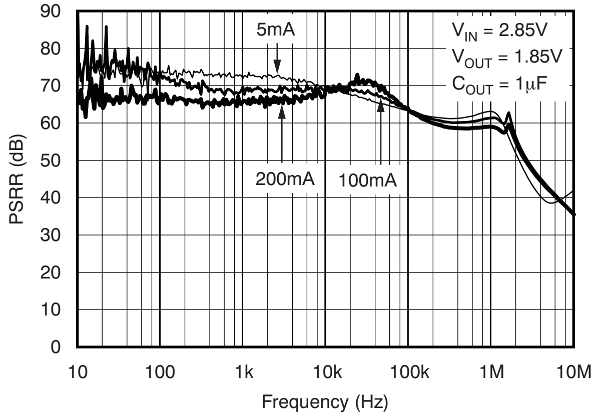


Figure 24.

TPS728185315 POWER-SUPPLY RIPPLE REJECTION vs FREQUENCY (V_{IN} – V_{OUT} = 0.5V)

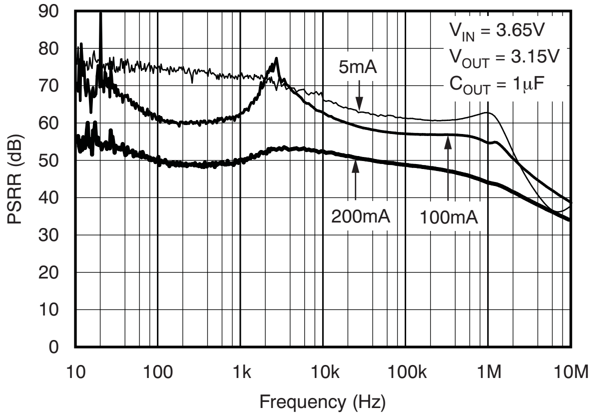


Figure 25.

TYPICAL CHARACTERISTICS (continued)

Over operating temperature range (T_J = –40°C to +125°C), $V_{IN} = V_{OUT(TYP)}$ + 0.5V or 2.7V, whichever is greater; I_{OUT} = 0.5mA, $V_{EN} = V_{SET} = V_{IN}$, C_{OUT} = 1.0μF, unless otherwise noted. Typical values are at T_J = +25°C.

TPS728185315 POWER-SUPPLY RIPPLE REJECTION vs FREQUENCY ($V_{IN} - V_{OUT}$ = 1.0V)

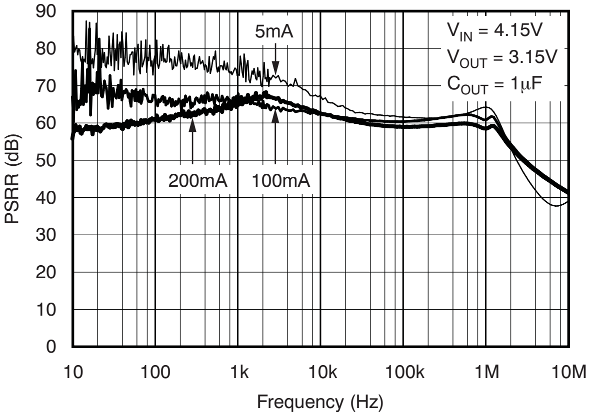


Figure 26.

OUTPUT SPECTRAL NOISE DENSITY vs FREQUENCY

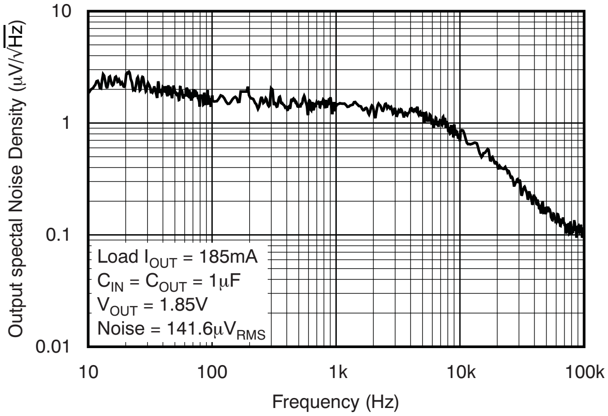


Figure 27.

OUTPUT SPECTRAL NOISE DENSITY vs FREQUENCY

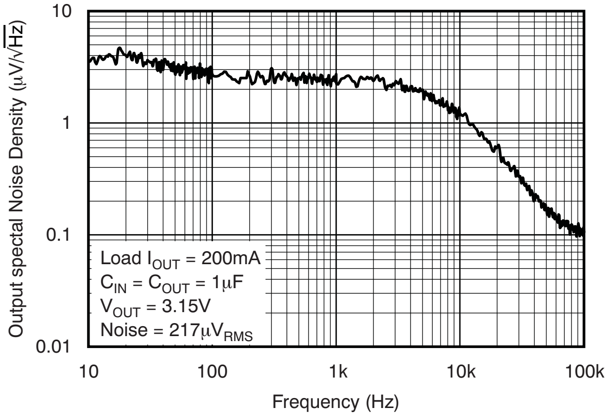


Figure 28.

LINE TRANSIENT RESPONSE

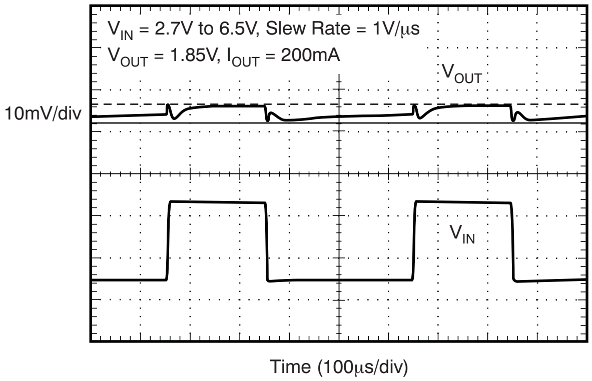


Figure 29.

LINE TRANSIENT RESPONSE

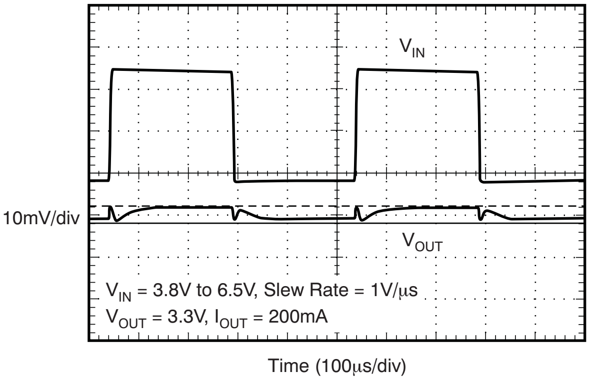


Figure 30.

LOAD TRANSIENT RESPONSE

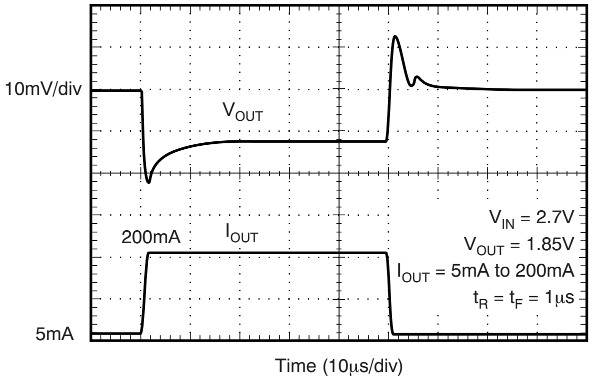


Figure 31.

TYPICAL CHARACTERISTICS (continued)

Over operating temperature range (T_J = –40°C to +125°C), V_{IN} = $V_{OUT(TYP)}$ + 0.5V or 2.7V, whichever is greater; I_{OUT} = 0.5mA, V_{EN} = V_{SET} = V_{IN}, C_{OUT} = 1.0μF, unless otherwise noted. Typical values are at T_J = +25°C.

LOAD TRANSIENT RESPONSE

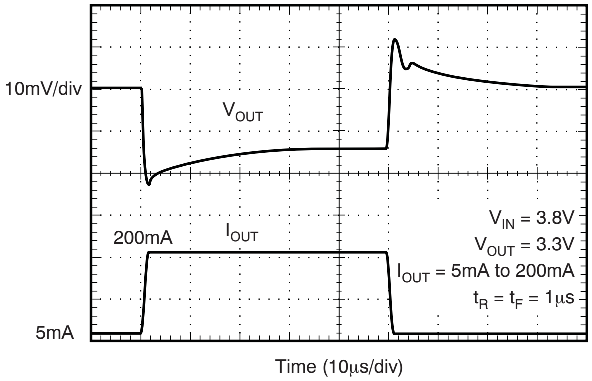


Figure 32.

ENABLE TRANSIENT RESPONSE

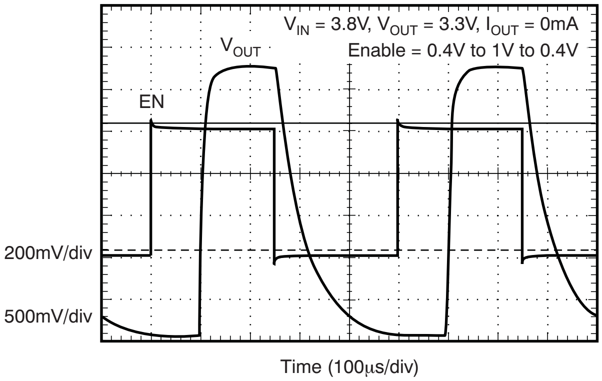


Figure 33.

V_{IN} RAMP UP AND RAMP DOWN RESPONSE

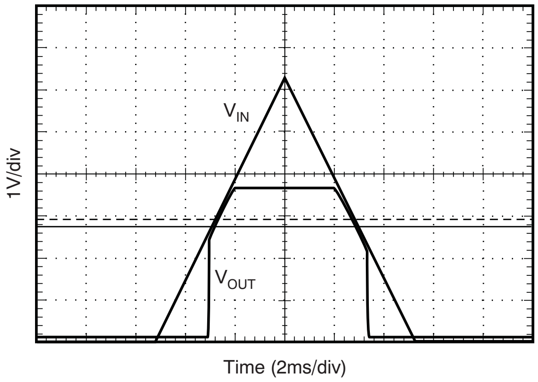


Figure 34.

VSET PIN TOGGLE

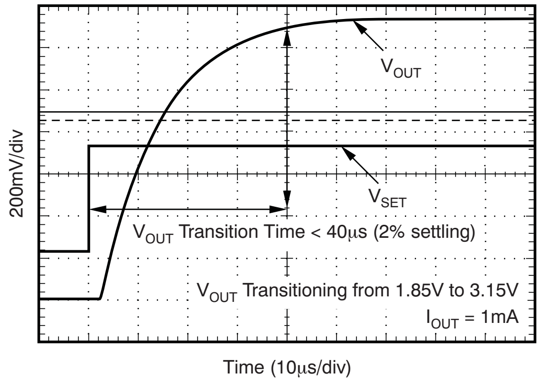


Figure 35.

VSET PIN TOGGLE

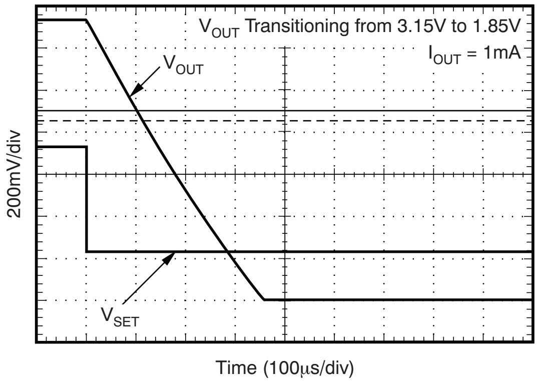


Figure 36.

VSET PIN TOGGLE

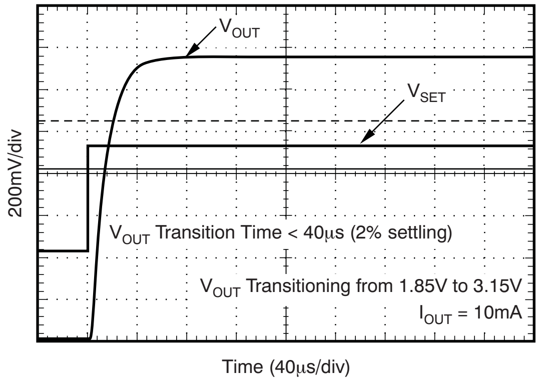


Figure 37.

TYPICAL CHARACTERISTICS (continued)

Over operating temperature range (T_J = –40°C to +125°C), V_{IN} = $V_{OUT(TYP)}$ + 0.5V or 2.7V, whichever is greater; I_{OUT} = 0.5mA, V_{EN} = V_{SET} = V_{IN}, C_{OUT} = 1.0μF, unless otherwise noted. Typical values are at T_J = +25°C.

VSET PIN TOGGLE

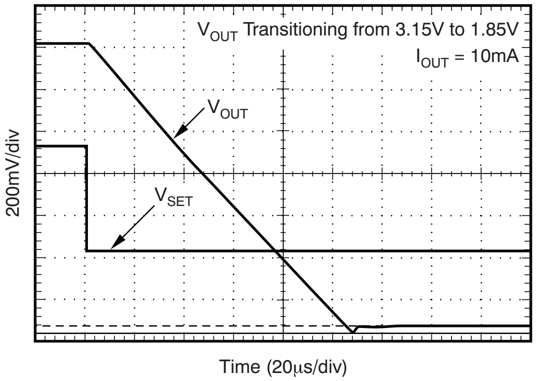


Figure 38.

APPLICATION INFORMATION

The TPS728xx series belongs to a family of new generation LDO regulators that use innovative circuitry to achieve ultra-wide bandwidth and high loop gain, resulting in extremely high PSRR (up to 1MHz) at very low headroom (V_{IN} – V_{OUT}). These features, combined with low noise, low ground pin current, and ultra-small packaging, make this device ideal for portable applications. This family of regulators offers sub-bandgap output voltages, current limit and thermal protection, and is fully specified from –40°C to +125°C.

Figure 39 shows the basic circuit connections.

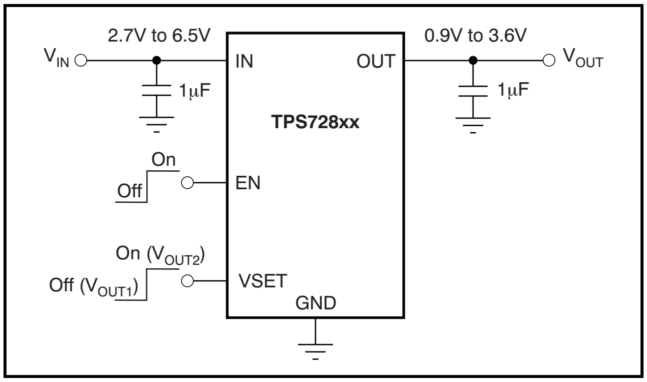


Figure 39. Typical Application Circuit

APPLICATION EXAMPLES

EEPROM-based applications require the programming voltage to be higher than the operating voltage. The TPS728xx suits such applications where the maximum programming voltage of the EEPROM is higher than the operating voltage. The VSET logic pin allows the application to transition between the higher EEPROM programming voltage and the lower operating voltage. For example, the TPS728xx typically takes less than 40µs to transition from a lower voltage of 1.85V to a higher voltage of 3.15V under an output load of 1mA to 10mA, as shown in Figure 35 and Figure 37, respectively. The special circuitry in the TPS728xx helps transition from the higher voltage to the lower voltage under no load. The load on the output at the end of the programming cycle is typically under 10mA. Output voltage overshoots and undershoots are minimal under this load condition. The TPS728xx typically takes less than 1ms of transition time going from 3.15V to 1.85V, as shown in Figure 36 and Figure 38, respectively. Both output states of the TPS728xx are programmable between 0.9V to 3.6V.

Another area where the TPS728xx can be used effectively is in dynamic voltage scaling (DVS) applications. In DVS applications, it is required to dynamically switch between a high operational voltage to a low standby voltage in order to balance performance of processors and achieve power savings. Modern multimillion gate microprocessors fabricated with the latest sub-micron processes save on power by transitioning to a lower voltage to reduce leakage currents without losing content. This architecture enables the microprocessor to transition quickly into an operational state (wake up) without requiring reloading of the states from external memory, or a reboot.

INPUT AND OUTPUT CAPACITOR REQUIREMENTS

Although an input capacitor is not required for stability, it is good analog design practice to connect a 0.1µF to 1.0µF low equivalent series resistance (ESR) capacitor across the input supply near the regulator. This capacitor counteracts reactive input sources and improves transient response, noise rejection, and ripple rejection. A higher-value capacitor may be necessary if large, fast rise-time load transients are anticipated, or if the device is not located near the power source. If source impedance is not sufficiently low, a 0.1µF input capacitor may be necessary to ensure stability.

The TPS728xx is designed to be stable with standard ceramic capacitors with values of 1.0µF or larger at the output. X5R- and X7R-type capacitors are best because they have minimal variation in value and ESR over temperature. Maximum ESR should be less than 1.0Ω.

BOARD LAYOUT RECOMMENDATIONS TO IMPROVE PSRR AND NOISE PERFORMANCE

To improve ac performance such as PSRR, output noise, and transient response, it is recommended that the board be designed with separate ground planes for V_{IN} and V_{OUT}, with each ground plane connected only at the GND pin of the device. In addition, the ground connection for the output capacitor should connect directly to the GND pin of the device. High ESR capacitors may degrade PSRR.

INTERNAL CURRENT LIMIT

The TPS728xx internal current limits help protect the regulator during fault conditions. During current limit, the output sources a fixed amount of current that is largely independent of output voltage. For reliable operation, the device should not be operated in a current limit state for extended periods of time.

The PMOS pass element in the TPS728xx has a built-in body diode that conducts current when the voltage at OUT exceeds the voltage at IN. This current is not limited, so if extended reverse voltage operation is anticipated, external limiting to 5% of rated output current may be appropriate.

SHUTDOWN

The enable pin (EN) is active high and is compatible with standard and low voltage, TTL-CMOS levels. When shutdown capability is not required, EN can be connected to the IN pin, as shown in Figure 40. Figure 41 shows when both EN and VSET are tied to IN. The TPS728xx, with internal active output pulldown circuitry, discharges the output to within 5% of V_{OUT} with a time (*t*) of:

$$t = 3\left(\frac{60 \times R_L}{60 + R_L}\right) \times C_{OUT}$$

Where:

R_L = output load resistance
C_{OUT} = output capacitance

DROPOUT VOLTAGE

The TPS728xx uses a PMOS pass transistor to achieve low dropout. When (V_{IN} – V_{OUT}) is less than the dropout voltage (V_{DO}), the PMOS pass device is in the linear region of operation and the input-to-output resistance is the $R_{DS(ON)}$ of the PMOS pass element. V_{DO} approximately scales with output current because the PMOS device behaves like a resistor in dropout.

As with any linear regulator, PSRR and transient response are degraded as (V_{IN} – V_{OUT}) approaches dropout. This effect is shown in Figure 25 and Figure 26 in the Typical Characteristics section.

TRANSIENT RESPONSE

As with any regulator, increasing the size of the output capacitor reduces over/undershoot magnitude but increases duration of the transient response.

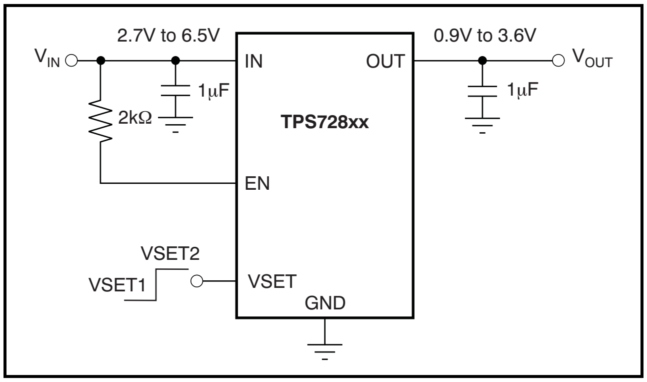


Figure 40. Circuit Showing EN Tied High when Shutdown Capability is Not Required

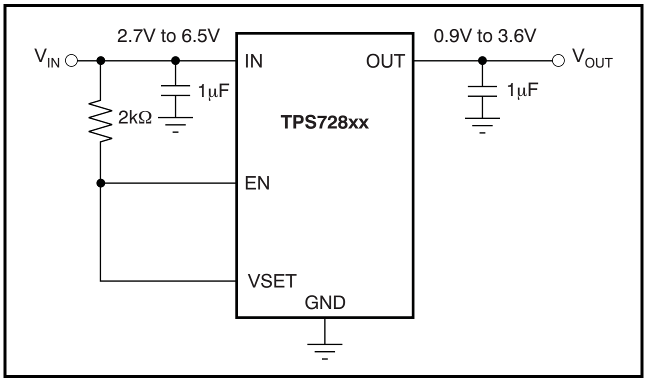


Figure 41. Circuit to Tie Both EN and VSET High

UNDERVOLTAGE LOCK-OUT (UVLO)

The TPS728xx uses an undervoltage lock-out circuit to keep the output shut off until the internal circuitry is operating properly. The UVLO circuit has a deglitch feature so that it typically ignores undershoot transients on the input if they are less than 5µs duration. The UVLO circuit triggers at approximately 2.3V on an undershooting or a falling input voltage. On the TPS728xx, the active pulldown discharges V_{OUT} when the device is in UVLO off condition. However, the input voltage must be greater than 0.8V for the active pulldown to work.

MINIMUM LOAD

The TPS728xx is stable with no output load. Traditional PMOS LDO regulators suffer from lower loop gain at very light output loads. The TPS728xx employs an innovative, low-current mode circuit under very light or no-load conditions, resulting in improved output voltage regulation performance down to zero output current.

THERMAL INFORMATION

Thermal Protection

Thermal protection disables the output when the junction temperature rises to approximately +160°C, allowing the device to cool. When the junction temperature cools to approximately +140°C the output circuitry is again enabled. Depending on power dissipation, thermal resistance, and ambient temperature, the thermal protection circuit may cycle on and off. This cycling limits the dissipation of the regulator, protecting it from damage as a result of overheating.

Any tendency to activate the thermal protection circuit indicates excessive power dissipation or an inadequate heatsink. For reliable operation, junction temperature should be limited to +125°C maximum. To estimate the margin of safety in a complete design (including heatsink), increase the ambient temperature until the thermal protection is triggered; use worst-case loads and signal conditions. For good reliability, thermal protection should trigger at least +35°C above the maximum expected ambient condition of your particular application. This configuration produces a worst-case junction temperature of +125°C at the highest expected ambient temperature and worst-case load.

The internal protection circuitry of the TPS728xx has been designed to protect against overload conditions. It was not intended to replace proper heatsinking. Continuously running the TPS728xx into thermal shutdown degrades device reliability.

Power Dissipation

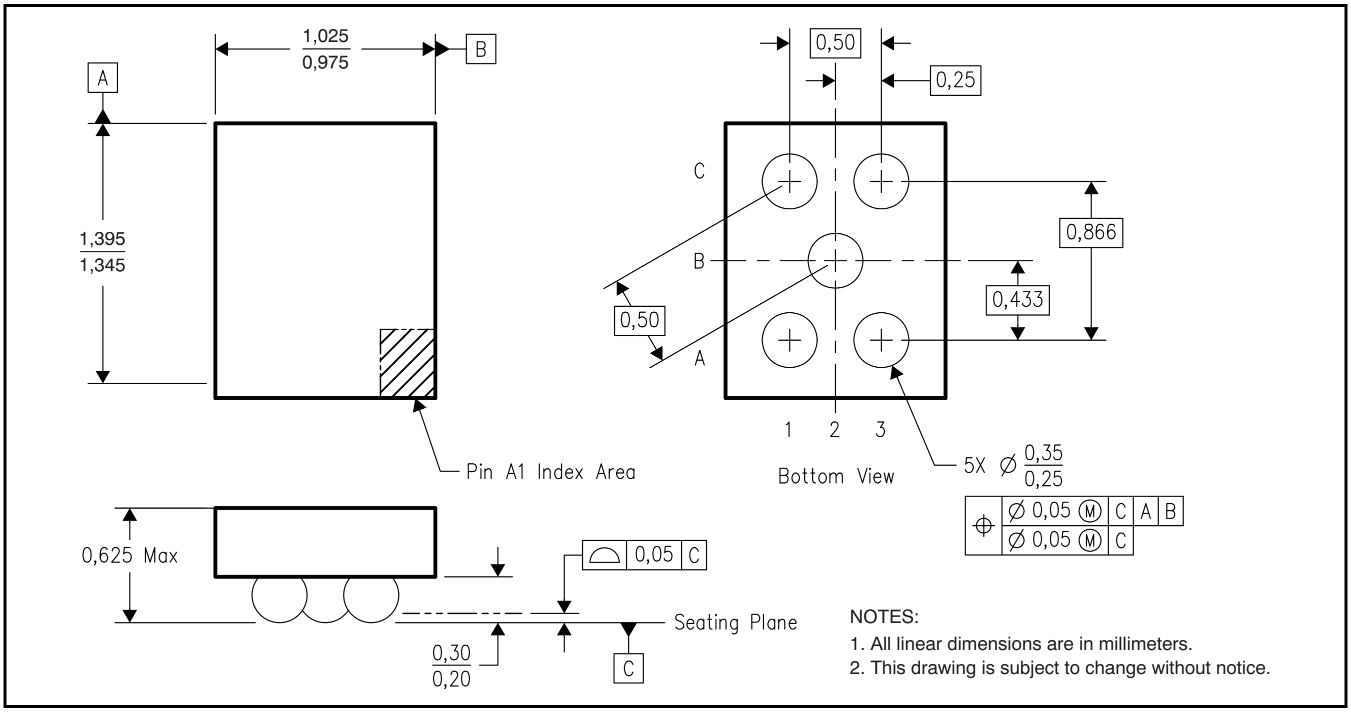
The ability to remove heat from the die is different for each package type, presenting different considerations in the printed circuit board (PCB) layout. The PCB area around the device that is free of other components moves the heat from the device to the ambient air. Performance data for JEDEC low- and high-K boards are given in the *Dissipation Ratings* table. Using heavier copper increases the effectiveness in removing heat from the device. The addition of plated through-holes to heat-dissipating layers also improves the heatsink effectiveness.

Power dissipation depends on input voltage and load conditions. Power dissipation (P_D) is equal to the product of the output current times the voltage drop across the output pass element (V_{IN} to V_{OUT}), as shown in Equation 1:

$$P_D = (V_{IN} - V_{OUT}) \times I_{OUT} \quad (1)$$

Package Mounting

Solder pad footprint recommendations for the TPS728xx are available from the Texas Instruments web site at www.ti.com.



NOTES:
1. All linear dimensions are in millimeters.
2. This drawing is subject to change without notice.

Figure 42. YZU Wafer Chip-Scale Package Dimensions (in mm)

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TPS728100180DRVR	Active	Production	WSON (DRV) | 6	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	1GZ
TPS728100180DRVR.B	Active	Production	WSON (DRV) | 6	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	1GZ
TPS728120150DRVR	Active	Production	WSON (DRV) | 6	3000 | LARGE T&R	Yes	NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	DAO
TPS728120150DRVR.B	Active	Production	WSON (DRV) | 6	3000 | LARGE T&R	Yes	NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	DAO
TPS728120150DRVT	Active	Production	WSON (DRV) | 6	250 | SMALL T&R	Yes	NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	DAO
TPS728120150DRVT.B	Active	Production	WSON (DRV) | 6	250 | SMALL T&R	Yes	NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	DAO
TPS728175295YZUR	Active	Production	DSBGA (YZU) | 5	3000 | LARGE T&R	Yes	SNAGCU	Level-1-260C-UNLIM	-40 to 125	AU
TPS728175295YZUR.B	Active	Production	DSBGA (YZU) | 5	3000 | LARGE T&R	Yes	SNAGCU	Level-1-260C-UNLIM	-40 to 125	AU
TPS728175295YZUT	Active	Production	DSBGA (YZU) | 5	250 | SMALL T&R	Yes	SNAGCU	Level-1-260C-UNLIM	-40 to 125	AU
TPS728175295YZUT.B	Active	Production	DSBGA (YZU) | 5	250 | SMALL T&R	Yes	SNAGCU	Level-1-260C-UNLIM	-40 to 125	AU
TPS728180285YZUR	Active	Production	DSBGA (YZU) | 5	3000 | LARGE T&R	Yes	SNAGCU	Level-1-260C-UNLIM	-40 to 125	DT
TPS728180285YZUR.B	Active	Production	DSBGA (YZU) | 5	3000 | LARGE T&R	Yes	SNAGCU	Level-1-260C-UNLIM	-40 to 125	DT
TPS728180285YZUT	Active	Production	DSBGA (YZU) | 5	250 | SMALL T&R	Yes	SNAGCU	Level-1-260C-UNLIM	-40 to 125	DT
TPS728180285YZUT.B	Active	Production	DSBGA (YZU) | 5	250 | SMALL T&R	Yes	SNAGCU	Level-1-260C-UNLIM	-40 to 125	DT
TPS728180300YZUR	Active	Production	DSBGA (YZU) | 5	3000 | LARGE T&R	Yes	SNAGCU	Level-1-260C-UNLIM	-40 to 125	VL
TPS728180300YZUR.B	Active	Production	DSBGA (YZU) | 5	3000 | LARGE T&R	Yes	SNAGCU	Level-1-260C-UNLIM	-40 to 125	VL
TPS728180300YZUT	Active	Production	DSBGA (YZU) | 5	250 | SMALL T&R	Yes	SNAGCU	Level-1-260C-UNLIM	-40 to 125	VL
TPS728180300YZUT.B	Active	Production	DSBGA (YZU) | 5	250 | SMALL T&R	Yes	SNAGCU	Level-1-260C-UNLIM	-40 to 125	VL
TPS728185295YZUR	Active	Production	DSBGA (YZU) | 5	3000 | LARGE T&R	Yes	SNAGCU	Level-1-260C-UNLIM	-40 to 125	VM
TPS728185295YZUR.B	Active	Production	DSBGA (YZU) | 5	3000 | LARGE T&R	Yes	SNAGCU	Level-1-260C-UNLIM	-40 to 125	VM
TPS728185295YZUT	Active	Production	DSBGA (YZU) | 5	250 | SMALL T&R	Yes	SNAGCU	Level-1-260C-UNLIM	-40 to 125	VM
TPS728185295YZUT.B	Active	Production	DSBGA (YZU) | 5	250 | SMALL T&R	Yes	SNAGCU	Level-1-260C-UNLIM	-40 to 125	VM
TPS728185315DRVT	Active	Production	WSON (DRV) | 6	250 | SMALL T&R	Yes	NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	BYW
TPS728185315DRVT.B	Active	Production	WSON (DRV) | 6	250 | SMALL T&R	Yes	NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	BYW
TPS728185315YZUR	Active	Production	DSBGA (YZU) | 5	3000 | LARGE T&R	Yes	SNAGCU	Level-1-260C-UNLIM	-40 to 125	FN
TPS728185315YZUR.B	Active	Production	DSBGA (YZU) | 5	3000 | LARGE T&R	Yes	SNAGCU	Level-1-260C-UNLIM	-40 to 125	FN
TPS728185315YZUT	Active	Production	DSBGA (YZU) | 5	250 | SMALL T&R	Yes	SNAGCU	Level-1-260C-UNLIM	-40 to 125	FN
TPS728185315YZUT.B	Active	Production	DSBGA (YZU) | 5	250 | SMALL T&R	Yes	SNAGCU	Level-1-260C-UNLIM	-40 to 125	FN
TPS728285180YZUR	Active	Production	DSBGA (YZU) | 5	3000 | LARGE T&R	Yes	SNAGCU	Level-1-260C-UNLIM	-40 to 125	TL

PACKAGE OPTION ADDENDUM

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TPS728285180YZUR.B	Active	Production	DSBGA (YZU) | 5	3000 | LARGE T&R	Yes	SNAGCU	Level-1-260C-UNLIM	-40 to 125	TL
TPS728285180YZUT	Active	Production	DSBGA (YZU) | 5	250 | SMALL T&R	Yes	SNAGCU	Level-1-260C-UNLIM	-40 to 125	TL
TPS728285180YZUT.B	Active	Production	DSBGA (YZU) | 5	250 | SMALL T&R	Yes	SNAGCU	Level-1-260C-UNLIM	-40 to 125	TL
TPS728330180YZUR	Active	Production	DSBGA (YZU) | 5	3000 | LARGE T&R	Yes	SNAGCU	Level-1-260C-UNLIM	-40 to 125	DJ
TPS728330180YZUR.B	Active	Production	DSBGA (YZU) | 5	3000 | LARGE T&R	Yes	SNAGCU	Level-1-260C-UNLIM	-40 to 125	DJ
TPS728330180YZUT	Active	Production	DSBGA (YZU) | 5	250 | SMALL T&R	Yes	SNAGCU	Level-1-260C-UNLIM	-40 to 125	DJ
TPS728330180YZUT.B	Active	Production	DSBGA (YZU) | 5	250 | SMALL T&R	Yes	SNAGCU	Level-1-260C-UNLIM	-40 to 125	DJ
TPS728330185DRVR	Active	Production	WSON (DRV) | 6	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	SBD
TPS728330185DRVR.B	Active	Production	WSON (DRV) | 6	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	SBD
TPS728330185DRVT	Active	Production	WSON (DRV) | 6	250 | SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	SBD
TPS728330185DRVT.B	Active	Production	WSON (DRV) | 6	250 | SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	SBD

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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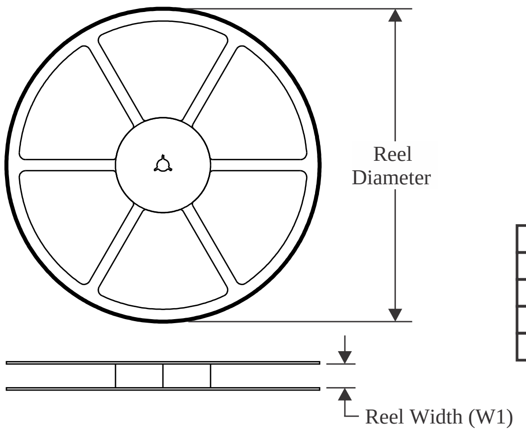
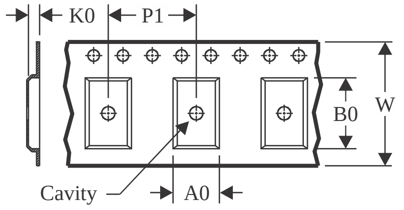
TAPE AND REEL INFORMATION

REEL DIMENSIONS

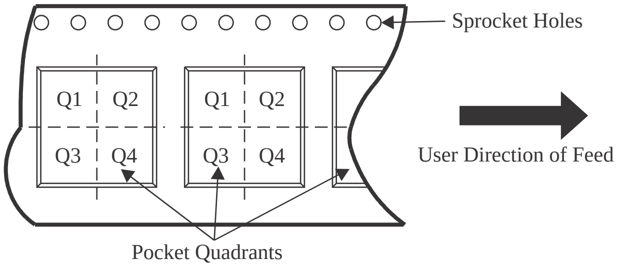


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE

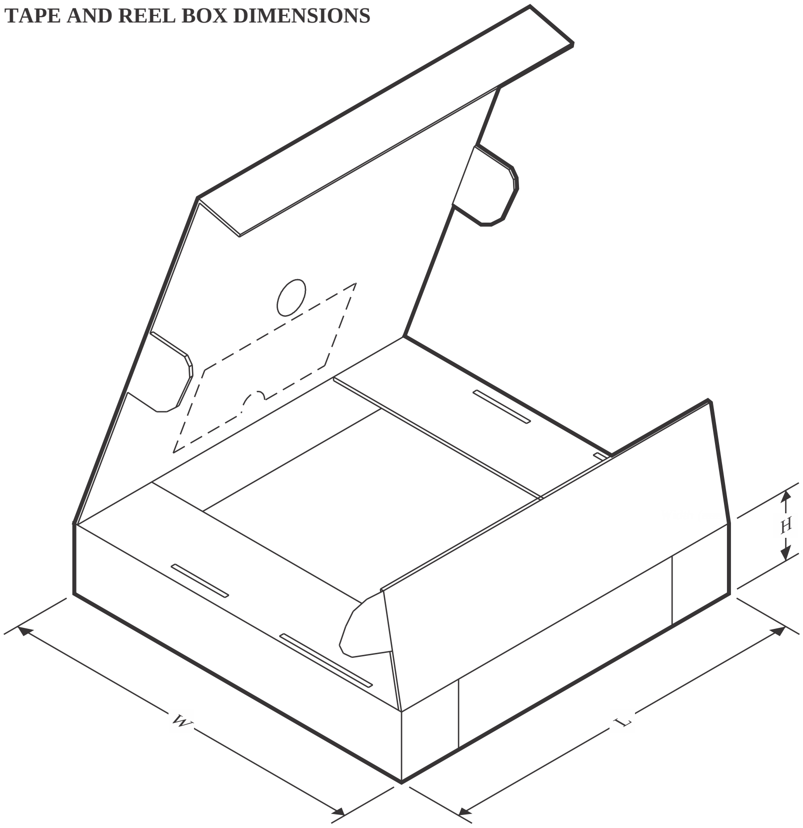


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS728120150DRVR	WSON	DRV	6	3000	179.0	8.4	2.2	2.2	1.2	4.0	8.0	Q2
TPS728120150DRVT	WSON	DRV	6	250	179.0	8.4	2.2	2.2	1.2	4.0	8.0	Q2
TPS728175295YZUR	DSBGA	YZU	5	3000	180.0	8.4	1.07	1.42	0.74	4.0	8.0	Q1
TPS728175295YZUT	DSBGA	YZU	5	250	180.0	8.4	1.07	1.42	0.74	4.0	8.0	Q1
TPS728180285YZUR	DSBGA	YZU	5	3000	180.0	8.4	1.07	1.42	0.74	4.0	8.0	Q1
TPS728180285YZUT	DSBGA	YZU	5	250	180.0	8.4	1.07	1.42	0.74	4.0	8.0	Q1
TPS728180300YZUR	DSBGA	YZU	5	3000	180.0	8.4	1.07	1.42	0.74	4.0	8.0	Q1
TPS728180300YZUT	DSBGA	YZU	5	250	180.0	8.4	1.07	1.42	0.74	4.0	8.0	Q1
TPS728185295YZUR	DSBGA	YZU	5	3000	180.0	8.4	1.07	1.42	0.74	4.0	8.0	Q1
TPS728185295YZUT	DSBGA	YZU	5	250	180.0	8.4	1.07	1.42	0.74	4.0	8.0	Q1
TPS728185315DRVT	WSON	DRV	6	250	179.0	8.4	2.2	2.2	1.2	4.0	8.0	Q2
TPS728185315YZUR	DSBGA	YZU	5	3000	180.0	8.4	1.07	1.42	0.74	4.0	8.0	Q1
TPS728185315YZUT	DSBGA	YZU	5	250	180.0	8.4	1.07	1.42	0.74	4.0	8.0	Q1
TPS728285180YZUR	DSBGA	YZU	5	3000	180.0	8.4	1.07	1.42	0.74	4.0	8.0	Q1
TPS728285180YZUT	DSBGA	YZU	5	250	180.0	8.4	1.07	1.42	0.74	4.0	8.0	Q1
TPS728330180YZUR	DSBGA	YZU	5	3000	180.0	8.4	1.07	1.42	0.74	4.0	8.0	Q1

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS728330180YZUT	DSBGA	YZU	5	250	180.0	8.4	1.07	1.42	0.74	4.0	8.0	Q1
TPS728330185DRVR	WSON	DRV	6	3000	179.0	8.4	2.2	2.2	1.2	4.0	8.0	Q2
TPS728330185DRVT	WSON	DRV	6	250	179.0	8.4	2.2	2.2	1.2	4.0	8.0	Q2

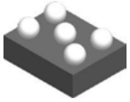
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS728120150DRVR	WSON	DRV	6	3000	200.0	183.0	25.0
TPS728120150DRVT	WSON	DRV	6	250	200.0	183.0	25.0
TPS728175295YZUR	DSBGA	YZU	5	3000	182.0	182.0	20.0
TPS728175295YZUT	DSBGA	YZU	5	250	182.0	182.0	20.0
TPS728180285YZUR	DSBGA	YZU	5	3000	182.0	182.0	20.0
TPS728180285YZUT	DSBGA	YZU	5	250	182.0	182.0	20.0
TPS728180300YZUR	DSBGA	YZU	5	3000	182.0	182.0	20.0
TPS728180300YZUT	DSBGA	YZU	5	250	182.0	182.0	20.0
TPS728185295YZUR	DSBGA	YZU	5	3000	182.0	182.0	20.0
TPS728185295YZUT	DSBGA	YZU	5	250	182.0	182.0	20.0
TPS728185315DRVT	WSON	DRV	6	250	200.0	183.0	25.0
TPS728185315YZUR	DSBGA	YZU	5	3000	182.0	182.0	20.0
TPS728185315YZUT	DSBGA	YZU	5	250	182.0	182.0	20.0
TPS728285180YZUR	DSBGA	YZU	5	3000	182.0	182.0	20.0
TPS728285180YZUT	DSBGA	YZU	5	250	182.0	182.0	20.0
TPS728330180YZUR	DSBGA	YZU	5	3000	182.0	182.0	20.0
TPS728330180YZUT	DSBGA	YZU	5	250	182.0	182.0	20.0
TPS728330185DRVR	WSON	DRV	6	3000	200.0	183.0	25.0

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS728330185DRVT	WSON	DRV	6	250	200.0	183.0	25.0

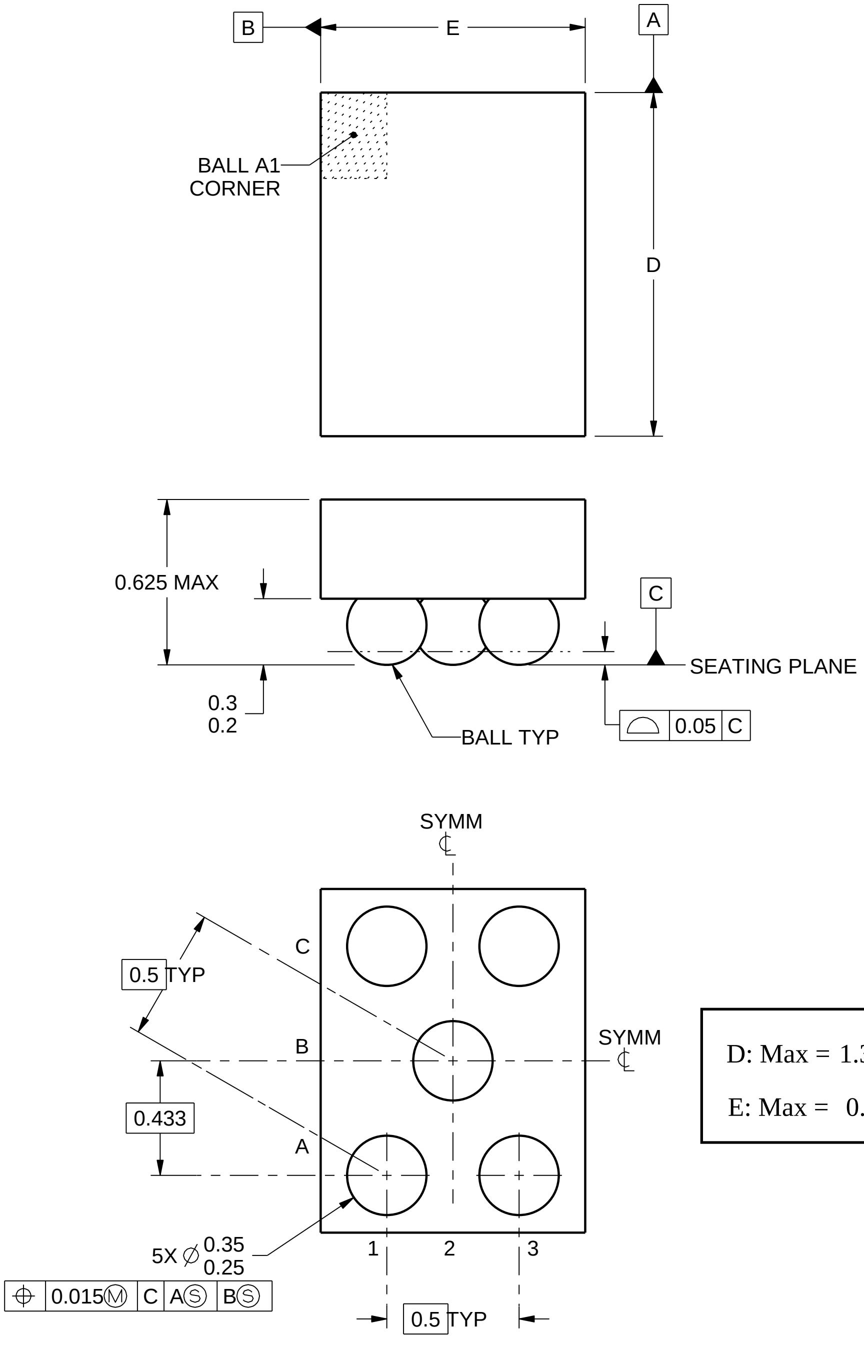


YZU0005

PACKAGE OUTLINE

DSBGA - 0.625 mm max height

DIE SIZE BALL GRID ARRAY



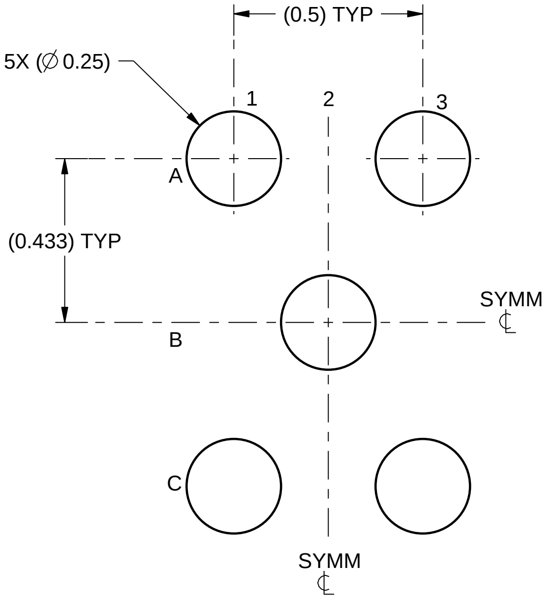
D: Max = 1.358 mm, Min =1.297 mm

E: Max = 0.99 mm, Min = 0.93 mm

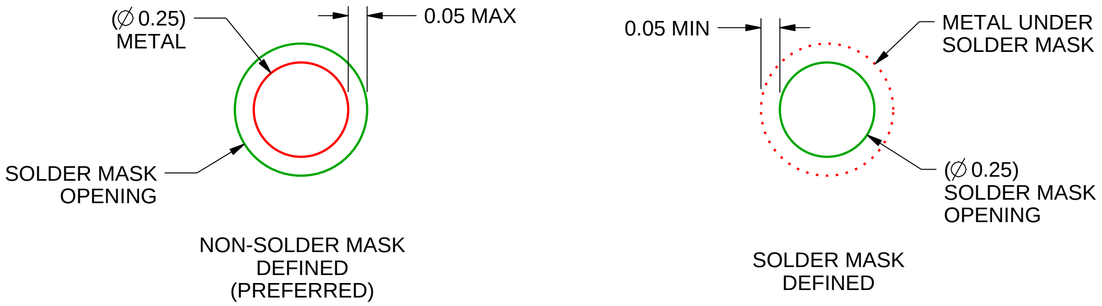
4222196/A 11/2015

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.



LAND PATTERN EXAMPLE
SCALE:50X

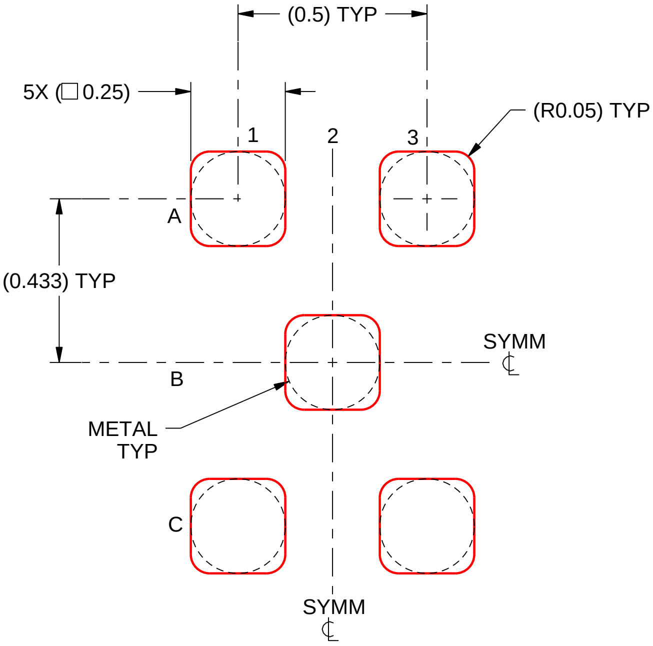


SOLDER MASK DETAILS
NOT TO SCALE

4222196/A 11/2015

NOTES: (continued)

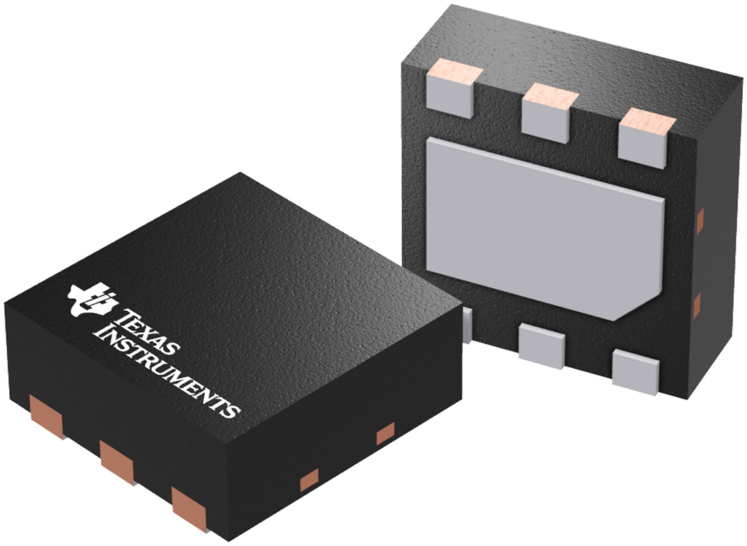
3. Final dimensions may vary due to manufacturing tolerance considerations and also routing constraints. Refer to Texas Instruments Literature No. SNVA009 (www.ti.com/lit/snva009).



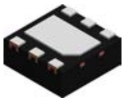
SOLDER PASTE EXAMPLE
BASED ON 0.1 mm THICK STENCIL
SCALE:50X

NOTES: (continued)

4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release.



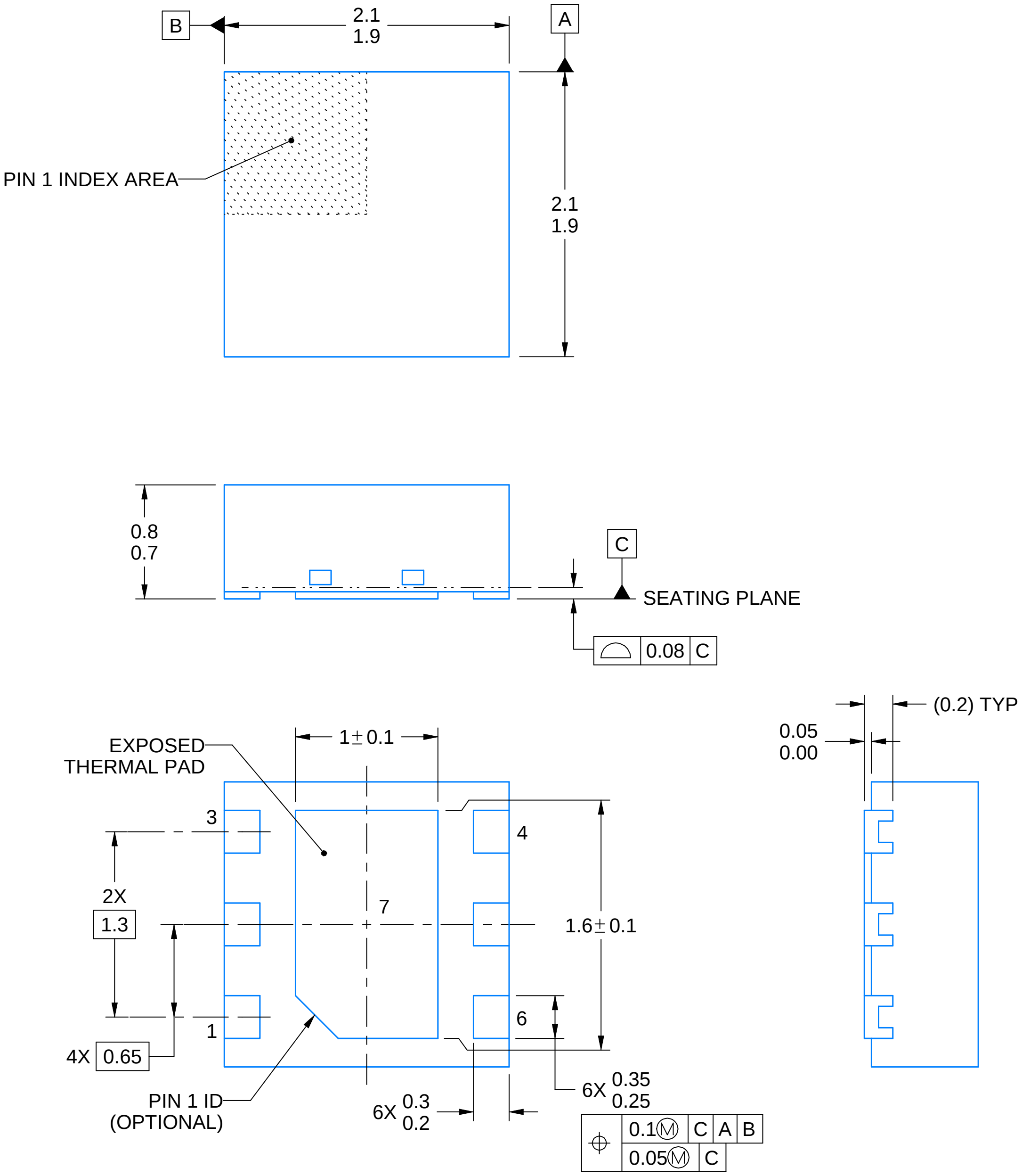
Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



PACKAGE OUTLINE

WSON - 0.8 mm max height

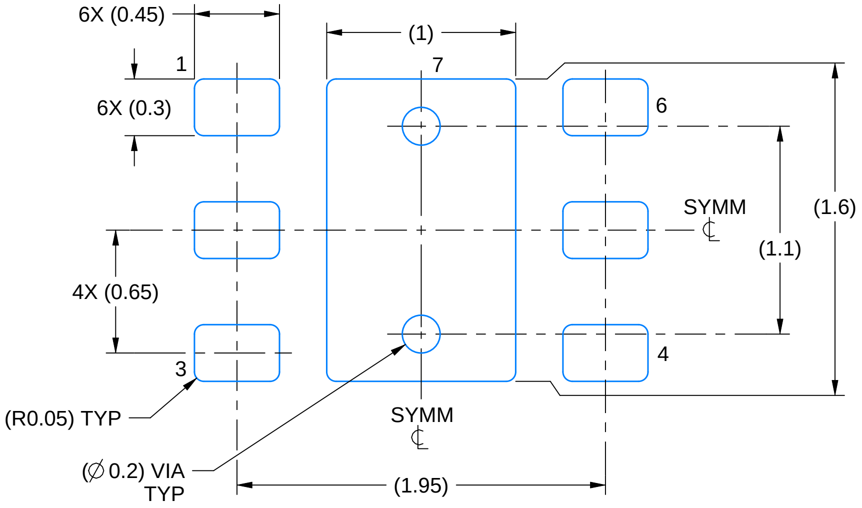
PLASTIC SMALL OUTLINE - NO LEAD



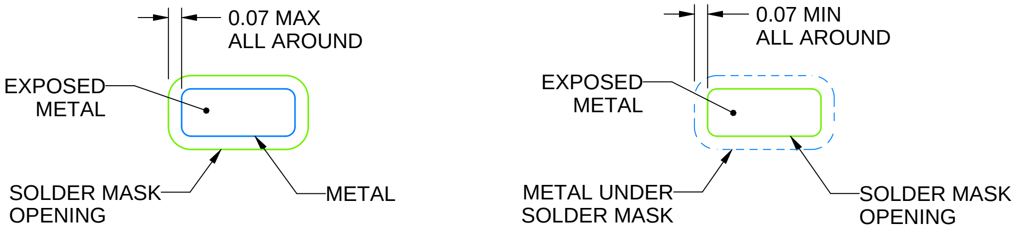
4225563/A 12/2019

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:25X



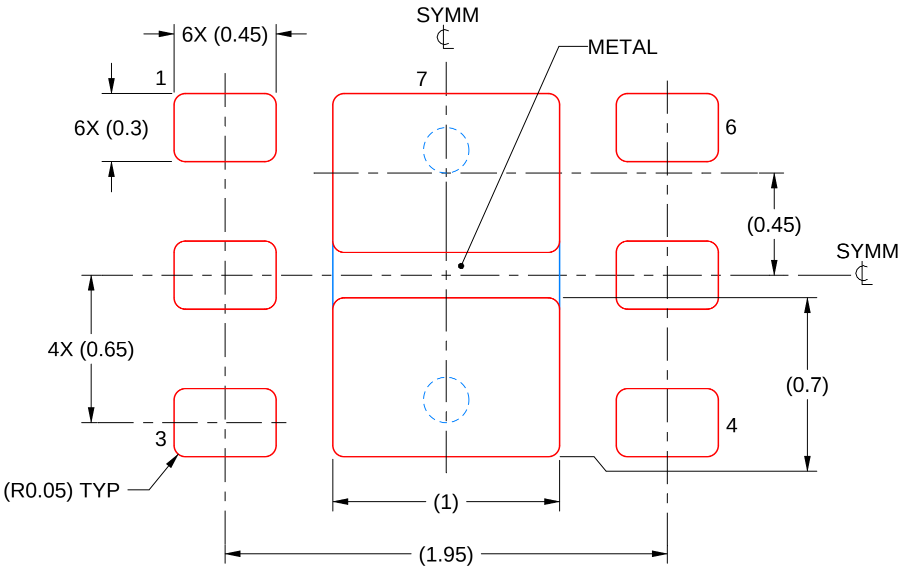
NON SOLDER MASK
DEFINED
(PREFERRED)

SOLDER MASK
DEFINED

SOLDER MASK DETAILS

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If some or all are implemented, recommended via locations are shown.



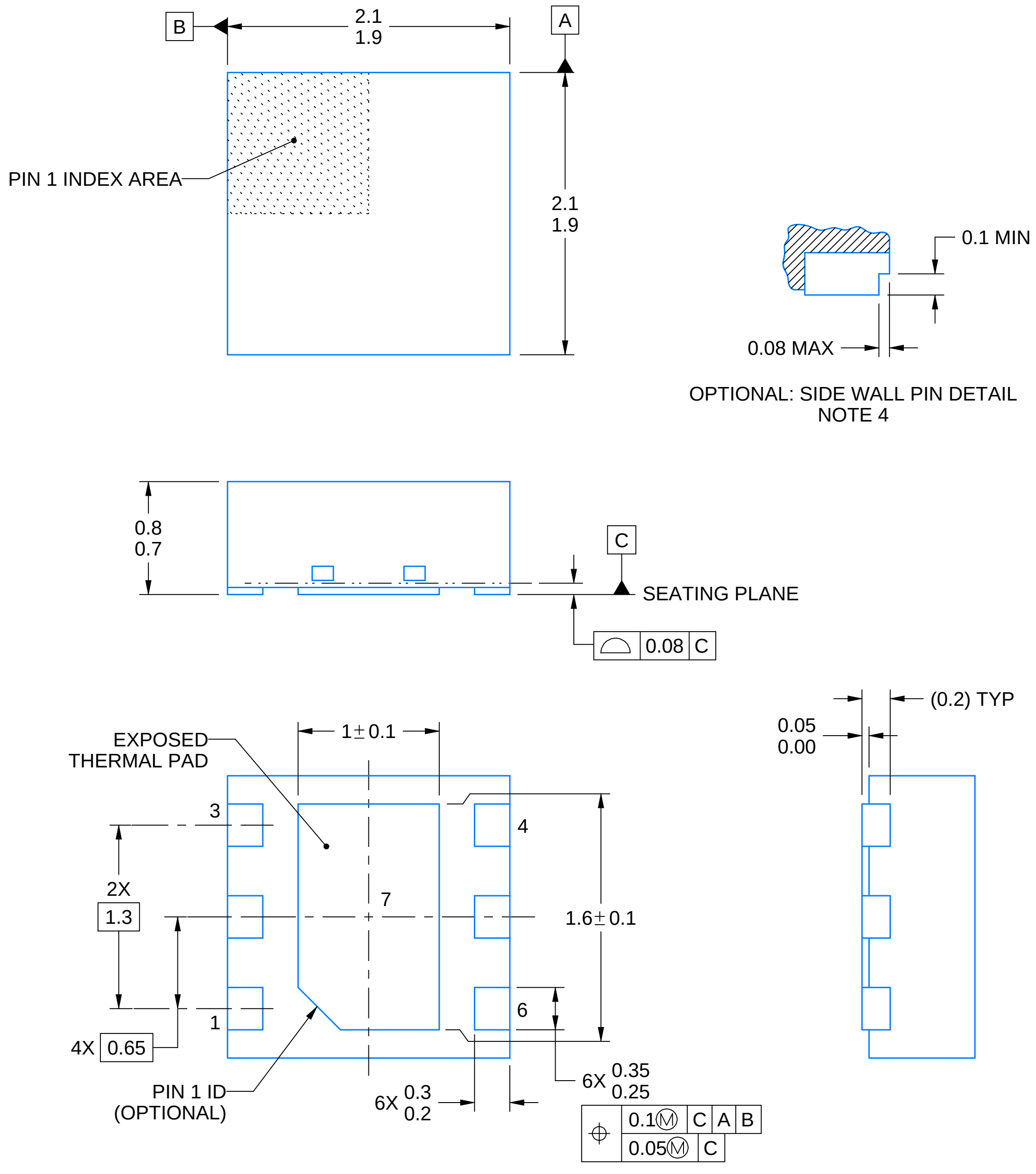
SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD #7
88% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:30X

4225563/A 12/2019

NOTES: (continued)

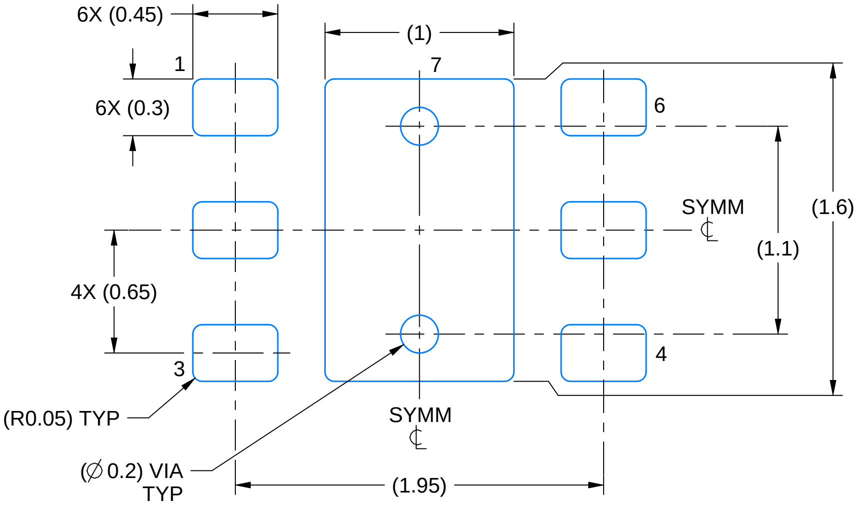
6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.



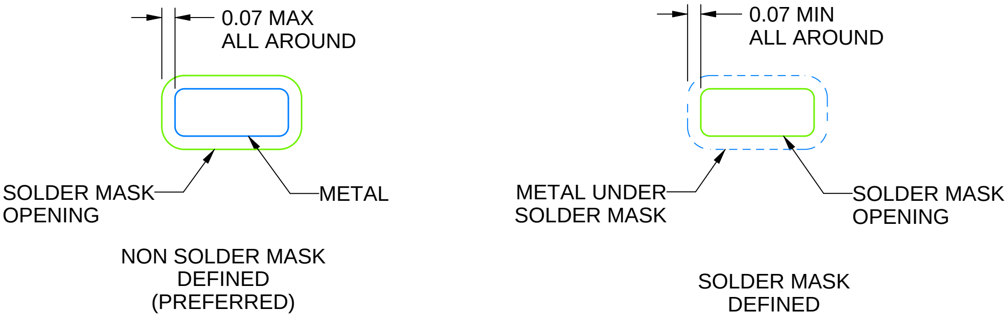
4222173/C 11/2025

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.
4. Minimum 0.1 mm solder wetting on pin side wall. Available for wettable flank version only.



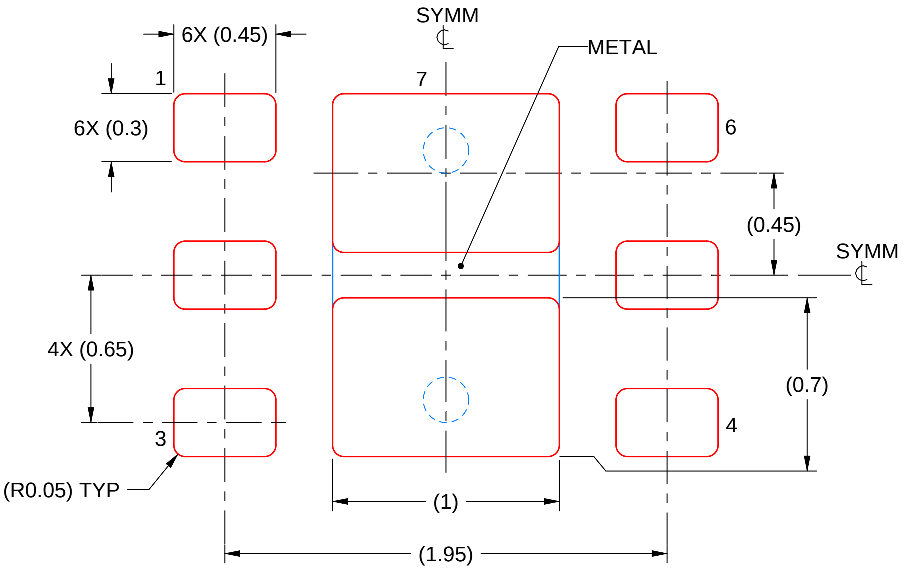
LAND PATTERN EXAMPLE
SCALE:25X



SOLDER MASK DETAILS

NOTES: (continued)

5. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
6. Vias are optional depending on application, refer to device data sheet. If some or all are implemented, recommended via locations are shown.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD #7
88% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:30X

NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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