TPS74301 1.5A Ultra-LDO With Programmable Sequencing

1 Features

- Track Pin Allows for Flexible Power-Up Sequencing
- 1% Accuracy Over Line, Load, and Temperature
- Supports Input Voltages as Low as 0.9V with External Bias Supply
- Adjustable Output (0.8V to 3.6V)
- Ultra-Low Dropout:
  - 55mV at 1.5A (typ)
- Stable with any output capacitor ≥ 2.2µF (new chip)
- Stable with any or no Output Capacitor (legacy chip)
- Excellent Transient Response
- Available in 5mm × 5mm × 1mm QFN and DDPAK-7 Packages
- Open-Drain Power-Good
- Active High Enable

2 Applications

- Network attached storage - enterprise
- Rack servers
- Network interface cards (NIC)
- Merchant network and server PSU

3 Description

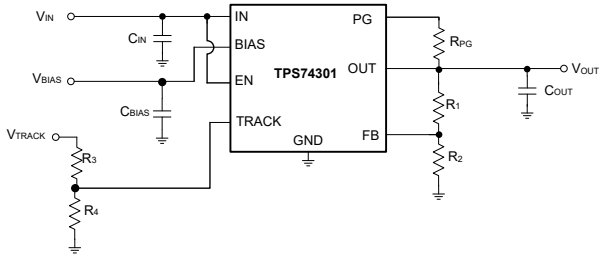
The TPS743 low-dropout (LDO) linear regulator provides an easy-to-use robust power management design for a wide variety of applications. The TRACK pin allows the output to track an external supply. This feature is useful in minimizing the stress on ESD structures that are present between the CORE and I/O power pins of many processors. The enable input and power-good output allow easy sequencing with external regulators. This complete flexibility allows the user to configure a solution that meets the sequencing requirements of FPGAs, DSPs, and other applications with special start-up requirements.

A precision reference and error amplifier deliver 1% accuracy over load, line, temperature, and process. The device is stable with any type of capacitor greater than or equal to 2.2µF. Each LDO is stable with low-cost ceramic output capacitors and the family is fully specified from –40°C to 125°C.

Package Information

PART NUMBER	PACKAGE(1)	PACKAGE SIZE(2)
TPS74301	RGW	5mm × 5mm
	KTW	10.1mm × 15.24mm

(1) For all available packages, see Section 10.
(2) The package size (length × width) is a nominal value and includes pins, where applicable.



Typical Application Circuit

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4 Pin Configurations and Functions

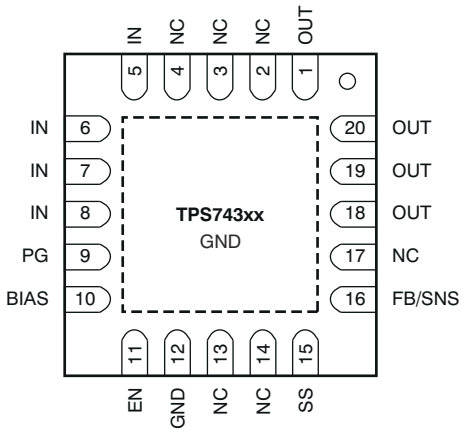


Figure 4-1. RGW PACKAGE 5 × 5 QFN-20 (TOP VIEW)

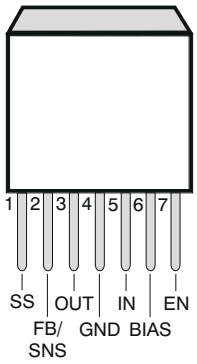


Figure 4-2. KTW PACKAGE DDPAK-7 SURFACE-MOUNT (Legacy only)

Pin Descriptions

Table 4-1. Pin Functions

PIN			TYPE[1]	DESCRIPTION
NAME	KTW (DDPAK)	RGW (QFN)		
Bias	6	10	I	Bias input voltage for error amplifier, reference, and internal control circuits.
EN	7	11	I	Enable pin. Driving this pin high enables the regulator. Driving this pin low puts the regulator into shutdown mode. This pin must not be left floating.
FB	2	16	I	This pin is the feedback connection to the center tap of an external resistor divider network that sets the output voltage. This pin must not be left floating.
GND	4	12	G	Ground.
IN	5	5–8	I	Unregulated input to the device.
NC	N/A	2–4, 13, 14, 17	—	No connection. This pin can be left floating or connected to GND to allow better thermal contact to the top-side plane.
OUT	3	1, 18–20	O	Regulated output voltage. No capacitor is required on this pin for stability.
PAD/TAB	—	—	—	Must be soldered to the ground plane for increased thermal performance.
PG	—	9	O	Power-Good (PG) is an open-drain, active-high output that indicates the status of V_{OUT}. When V_{OUT} exceeds the PG trip threshold, the PG pin goes into a high-impedance state. When V_{OUT} is below this threshold the pin is driven to a low-impedance state. A pullup resistor from 10kΩ to 1MΩ must be connected from this pin to a supply up to 5.5V. The supply can be higher than the input voltage. Alternatively, the PG pin can be left floating if output monitoring is not necessary.

Table 4-1. Pin Functions (continued)

PIN			TYPE[1]	DESCRIPTION
NAME	KTW (DDPAK)	RGW (QFN)		
TRACK	1	15	I	Tracking pin. Connect this pin to the center tap of a resistor divider off of an external supply to program the device to track an external supply.

(1) I = Input, O = Output, I/O = Input or Output, G = Ground, P = Power, N/A = Not applicable.

5 Specifications

5.1 Absolute Maximum Ratings

over operating temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
V_{IN}, V_{BIAS}	Input voltage	–0.3	6	V
V_{EN}	Enable voltage	–0.3	6	V
V_{PG}	Power good voltage	–0.3	6	V
I_{PG}	PG sink current	0	1.5	mA
V_{SS}	Soft-start voltage	–0.3	6	V
V_{FB}	Feedback voltage	–0.3	6	V
V_{OUT}	Output voltage	–0.3	V_{IN} + 0.3	V
I_{OUT}	Maximum output current	Internally limited		
	Output short-circuit duration	Indefinite		
P_{DISS}	Continuous total power dissipation	See Thermal Information		
T_J	Junction Temperature (Legacy Chip)	–40	125	°C
	Junction Temperature (New Chip)	–40	150	°C
T_{stg}	Storage Temperature	–55	150	

(1) Operation outside the Absolute Maximum Ratings may cause permanent device damage. Absolute Maximum Ratings do not imply functional operation of the device at these or any other conditions beyond those listed under Recommended Operating Conditions. If used outside the Recommended Operating Conditions but within the Absolute Maximum Ratings, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.

5.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins(1)	±2000	V
		Charged device model (CDM), per JEDEC specification JESD22-C101, all pins(2)	±500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

5.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
V_{IN}	Input supply voltage	V_{OUT} + V_{DO} (V_{IN})	V_{OUT} + 0.3	5.5	V
V_{EN}	Enable supply voltage		V_{IN}	5.5	V
V_{BIAS} (1)	BIAS supply voltage	V_{OUT} + V_{DO} (V_{BIAS})(2)	V_{OUT} + 1.6(2)	5.5	V
V_{OUT}	Output voltage	0.8		3.6	V
I_{OUT}	Output current	0		1.5	A
C_{OUT}	Output capacitor (legacy chip)	0			µF
	Output capacitor (new chip)	2.2			µF
C_{IN}	Input capacitor(3)	1			µF
C_{BIAS}	Bias capacitor	0.1	1		µF
T_J	Operating junction temperature	–40		125	°C

(1) BIAS supply is required when V_{IN} is below V_{OUT} + V_{DO} (V_{BIAS}).
(2) V_{BIAS} has a minimum voltage of 2.7 V or V_{OUT} + V_{DO} (V_{BIAS}), whichever is higher (new chip).
(3) If V_{IN} and V_{BIAS} are connected to the same supply, the recommended minimum capacitor for the supply is 4.7 µF.

5.4 Thermal Information

THERMAL METRIC (1)		TPS742				UNIT
		RGW (VQFN) (legacy chip)	RGW (VQFN) (new chip)	RGR (VQFN)	KTW (DDPAK/ TO-263)	
		20 PINS	20 PINS	20 PINS	7 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	35.4	34.7	44.2	47.2	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	32.4	31	50.3	63.7	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	14.7	13.5	19.6	19.5	°C/W
ψ_{JT}	Junction-to-top characterization parameter	0.4	1.4	0.7	4.2	°C/W
ψ_{JB}	Junction-to-board characterization parameter	14.8	13.5	17.8	19.4	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	3.9	3.6	4.3	3.3	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application note.

5.5 Electrical Characteristics

at V_{EN} = 1.1 V, V_{IN} = V_{OUT} + 0.3 V, C_{BIAS} = 0.1 µF, C_{IN} = C_{OUT} = 10 µF, I_{OUT} = 50 mA, V_{BIAS} = 5.0 V, and T_J = –40°C to 125°C, (unless otherwise noted); typical values are at T_J = 25°C

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{IN}	Input voltage range		V_{OUT} + V_{DO}		5.5	V
V_{BIAS}	BIAS pin voltage range		2.375		5.25	V
V_{REF}	Internal reference	T_J = 25°C	0.796	0.8	0.804	V
V_{OUT}	Output voltage	V_{IN} = 5V, I_{OUT} = 1.5A, V_{BIAS} = 5V	V_{REF}		3.6	V
V_{OUT}	Accuracy (1)	2.375V ≤ V_{BIAS} ≤ 5.25V, V_{OUT} + 1.62V ≤ V_{BIAS} 50mA ≤ I_{OUT} ≤ 1.5A	-1	±0.2	1	%
$\Delta V_{OUT(\Delta VIN)}$	Line regulation	$V_{OUT\ (NOM)}$ + 0.3V ≤ V_{IN} ≤ 5.5V, VQFN		0.0005	0.05	%/V
		$V_{OUT\ (NOM)}$ + 0.3V ≤ V_{IN} ≤ 5.5V, DDPAK/TO-263		0.0005	0.06	
$\Delta V_{OUT(\Delta IOUT)}$	Load regulation	0 mA ≤ I_{OUT} ≤ 50mA (Legacy Chip)		0.013		%/mA
		50 mA ≤ I_{OUT} ≤ 1.5 A (Legacy Chip)		0.04		%/A
		50 mA ≤ I_{OUT} ≤ 1.5 A (New Chip)		0.09		
V_{DO}	V_{IN} dropout voltage(2)	I_{OUT} = 1.5 A, V_{BIAS} – $V_{OUT\ (NOM)}$ ≥ 1.62 V, VQFN		55	100	mV
		I_{OUT} = 1.5 A, V_{BIAS} – $V_{OUT\ (NOM)}$ ≥ 1.62 V, DDPAK/ TO-263 (Legacy chip only)		60	120	
	V_{BIAS} dropout voltage(2)	I_{OUT} = 1.5A, V_{IN} = V_{BIAS} (Legacy Chip)			1.4	V
		I_{OUT} = 1.5A, V_{IN} = V_{BIAS} (New Chip)			1.43	
I_{CL}	Current limit	V_{OUT} = 80% × $V_{OUT(nom)}$, (Legacy Chip)	1.8		4	A
		V_{OUT} = 80% × $V_{OUT(nom)}$, (New Chip)	2		5.5	
I_{BIAS}	BIAS pin current	I_{OUT} = 0mA to 1.5A (Legacy Chip)		2	4	mA
		I_{OUT} = 0mA to 1.5A (New Chip)		1	2	

5.5 Electrical Characteristics (continued)

at V_{EN} = 1.1 V, V_{IN} = V_{OUT} + 0.3 V, C_{BIAS} = 0.1 µF, C_{IN} = C_{OUT} = 10 µF, I_{OUT} = 50 mA, V_{BIAS} = 5.0 V, and T_J = –40°C to 125°C, (unless otherwise noted); typical values are at T_J = 25°C

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_{SHDN}	Shutdown supply current (I_{GND})	V_{EN} ≤ 0.4V (Legacy Chip)		1	100	µA
		V_{EN} ≤ 0.4V, (New Chip)		0.85	2.75	
I_{FB}	Feedback pin current (3)	I_{OUT} = 50mA to 1.5A (Legacy Chip)	–250	68	250	nA
		I_{OUT} = 50mA to 1.5A (New Chip)	–30	0.15	30	nA
PSRR	Power-supply rejection (V_{IN} to V_{OUT})	1 kHz, I_{OUT} = 1.5 A, V_{IN} = 1.8 V, V_{OUT} = 1.5 V (Legacy Chip)		73		dB
		1 kHz, I_{OUT} = 1.5 A, V_{IN} = 1.8 V, V_{OUT} = 1.5 V (New Chip)		60		
		300 kHz, I_{OUT} = 1.5 A, V_{IN} = 1.8 V, V_{OUT} = 1.5 V (Legacy Chip)		42		
		300 kHz, I_{OUT} = 1.5 A, V_{IN} = 1.8 V, V_{OUT} = 1.5 V (New Chip)		30		
	Power-supply rejection (V_{BIAS} to V_{OUT})	1kHz, I_{OUT} = 1.5A, V_{IN} = 1.8V, V_{OUT} = 1.5V (Legacy Chip)		62		
		1kHz, I_{OUT} = 1.5A, V_{IN} = 1.8V, V_{OUT} = 1.5V (New Chip)		59		
		300kHz, I_{OUT} = 1.5A, V_{IN} = 1.8V, V_{OUT} = 1.5V		50		
V_n	Output noise voltage	BW = 100Hz to 100kHz, I_{OUT} = 1.5A, C_{SS} = 1nF (Legacy Chip)		16		µVrms x Vout
		BW = 100 Hz to 100 kHz, I_{OUT} = 3A, C_{SS} = 1nF (New Chip)		20		
V_{TRAN}	%V_{OUT} droop during load transient	I_{OUT} = 50mA to 1.5A at 1A/µs, C_{OUT}=none (Legacy Chip)		3.5		%V_{OUT}
V_{TRAN}	%V_{OUT} droop during load transient	I_{OUT} = 50mA to 1.5A at 1A/µs, C_{OUT}=2.2µF (New Chip)		1.7		%V_{OUT}
t_{STR}	Minimum start-up time	R_{LOAD} for I_{OUT} = 1.5A, C_{SS} = open (Legacy Chip)		100		µs
		R_{LOAD} for I_{OUT} = 1.0A, C_{SS} = open (New Chip)		250		
$V_{EN(hi)}$	Enable input high level		1.1		5.5	V
$V_{EN(lo)}$	Enable input low level		0		0.4	V
$V_{EN(hys)}$	Enable pin hysteresis	(Legacy Chip)		50		mV
		(New Chip)		55		
$V_{EN(dg)}$	Enable pin deglitch time			20		µs
I_{EN}	Enable pin current	V_{EN} = 5V (Legacy Chip)		0.1	1	µA
		V_{EN} = 5V (New Chip)		0.1	0.25	
V_{IT}	PG trip threshold	V_{OUT} decreasing (Legacy Chip)	86.5	90	93.5	%V_{OUT}
		V_{OUT} decreasing (New Chip)	85	90	94	
V_{HYS}	PG trip hysteresis	(Legacy Chip)		3		%V_{OUT}
		(New Chip)		2.5		

5.5 Electrical Characteristics (continued)

at V_{EN} = 1.1 V, V_{IN} = V_{OUT} + 0.3 V, C_{BIAS} = 0.1 µF, C_{IN} = C_{OUT} = 10 µF, I_{OUT} = 50 mA, V_{BIAS} = 5.0 V, and T_J = –40°C to 125°C, (unless otherwise noted); typical values are at T_J = 25°C

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$V_{PG(lo)}$	PG output low voltage	I_{PG} = 1 mA (sinking), V_{OUT} < V_{IT} (Legacy Chip)			0.3	V
		I_{PG} = 1 mA (sinking), V_{OUT} < V_{IT} (New Chip)			0.12	
$I_{PG(lkg)}$	PG leakage current	V_{PG} = 5.25 V, V_{OUT} > V_{IT} (Legacy Chip)		0.03	1	µA
		V_{PG} = 5.25 V, V_{OUT} > V_{IT} (New Chip)		0.001	0.05	
T_J	Operating junction temperature		–40		125	℃
T_{SD}	Thermal shutdown temperature	Shutdown, temperature increasing (Legacy Chip)		155		℃
		Shutdown, temperature increasing (New Chip)		165		
		Reset, temperature decreasing		140		

(1) For adjustable devices tested at 0.8V, resistor tolerance is not taken into account.
(2) Dropout is defined as the voltage from the input to V_{OUT} when V_{OUT} is 2% below nominal.
(3) I_{FB} current flow is out of the device.

5.6 Typical Characteristics

at T_J = 25°C, V_{OUT} = 1.5V, V_{IN} = $V_{OUT(NOM)}$ + 0.3V, V_{BIAS} = 3.3V (legacy chip), V_{BIAS} = 5.0V (new chip), I_{OUT} = 50 mA, V_{EN} =V_{IN}, C_{IN} = 1µF, C_{BIAS} = 4.7µF, C_{SS} = 0.01µF (legacy chip), and C_{OUT} = 10µF (unless otherwise noted)

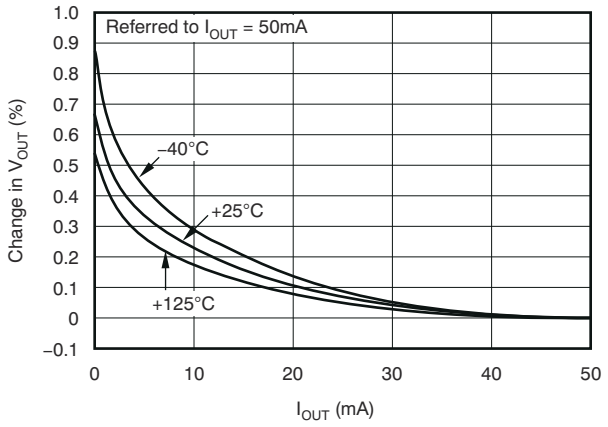


Figure 5-1. Load Regulation (legacy chip)

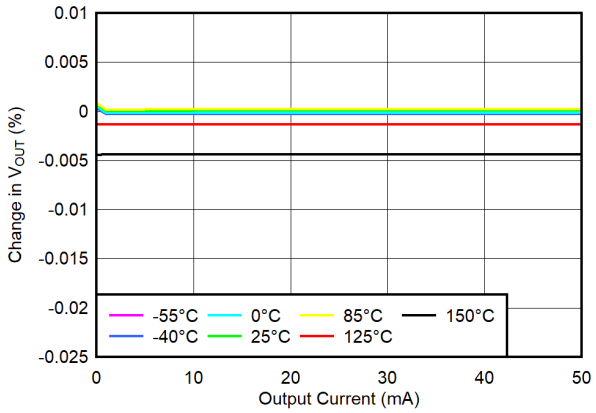


Figure 5-2. Load Regulation (new chip)

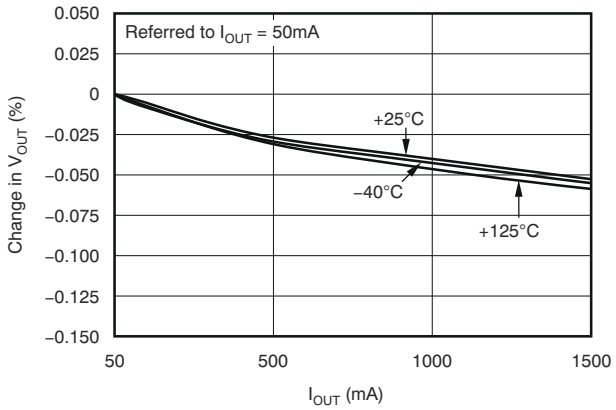


Figure 5-3. Load Regulation (legacy chip)

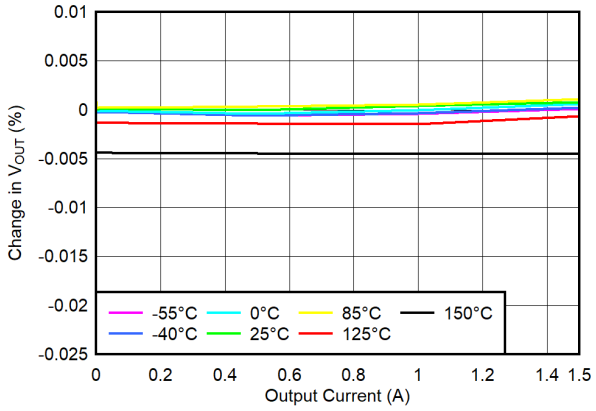


Figure 5-4. Load Regulation (new chip)

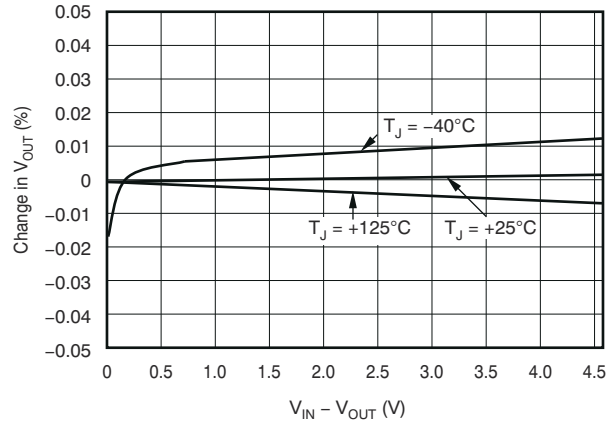


Figure 5-5. Line Regulation (legacy chip)

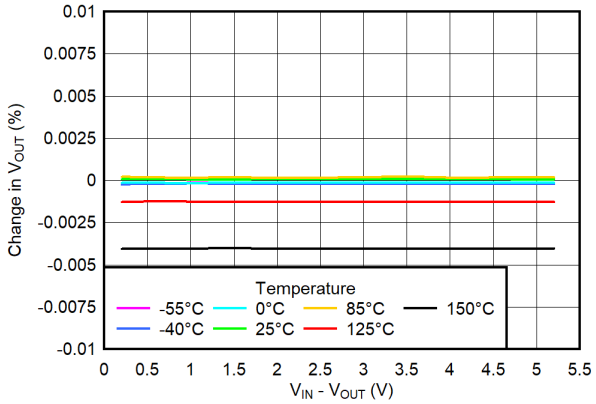


Figure 5-6. Line Regulation (new chip)

5.6 Typical Characteristics (continued)

at T_J = 25°C, V_{OUT} = 1.5V, V_{IN} = $V_{OUT(NOM)}$ + 0.3V, V_{BIAS} = 3.3V (legacy chip), V_{BIAS} = 5.0V (new chip), I_{OUT} = 50 mA, V_{EN} =V_{IN}, C_{IN} = 1µF, C_{BIAS} = 4.7µF, C_{SS} = 0.01µF (legacy chip), and C_{OUT} = 10µF (unless otherwise noted)

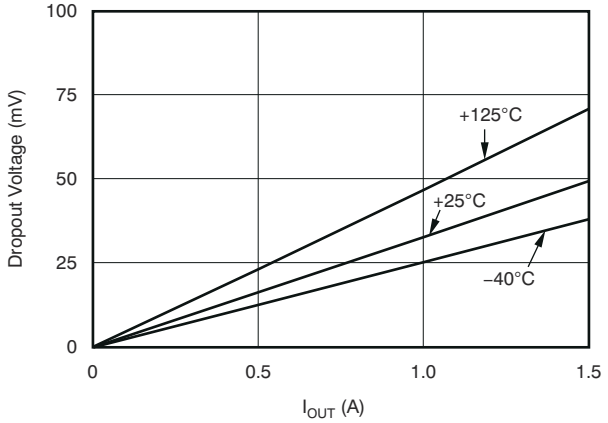


Figure 5-7. V_{IN} Dropout Voltage vs I_{OUT} and Temperature (T_J) (legacy chip)

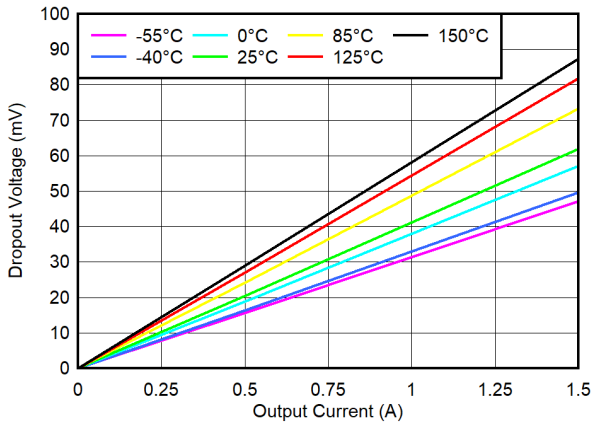


Figure 5-8. V_{IN} Dropout Voltage vs I_{OUT} and Temperature (T_J) (new chip)

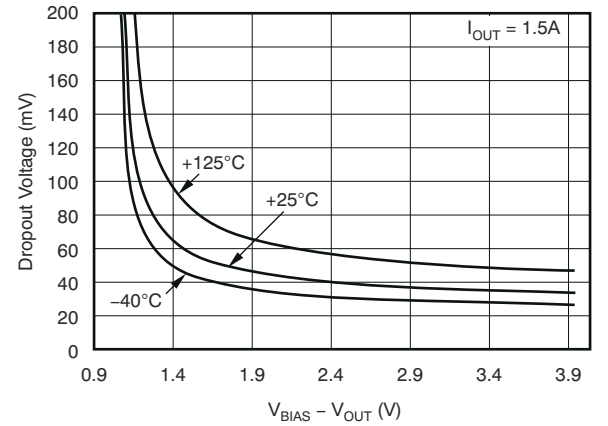


Figure 5-9. V_{IN} Dropout Voltage vs V_{BIAS} – V_{OUT} and Temperature (T_J)

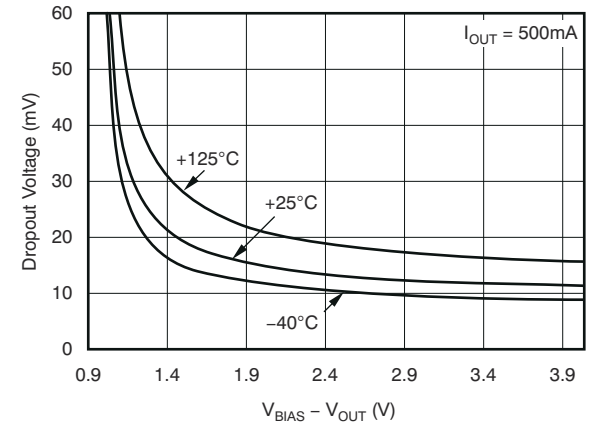


Figure 5-10. V_{IN} Dropout Voltage vs V_{BIAS} – V_{OUT} and Temperature (T_J)

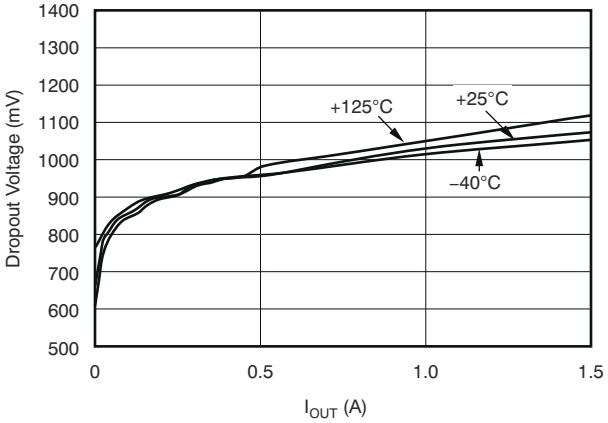


Figure 5-11. V_{BIAS} Dropout Voltage vs I_{OUT} and Temperature (legacy chip)

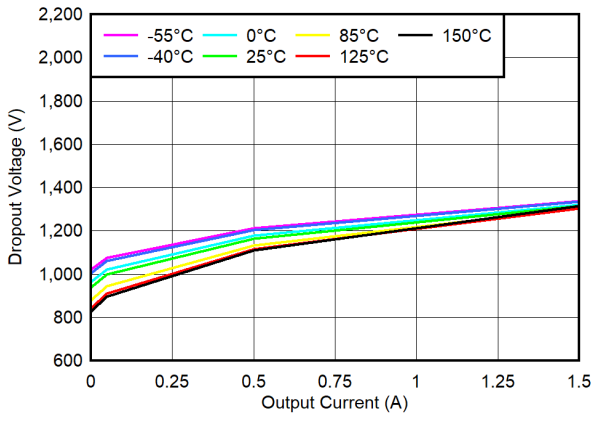


Figure 5-12. V_{BIAS} Dropout Voltage vs I_{OUT} and Temperature (new chip)

5.6 Typical Characteristics (continued)

at T_J = 25°C, V_{OUT} = 1.5V, V_{IN} = $V_{OUT(NOM)}$ + 0.3V, V_{BIAS} = 3.3V (legacy chip), V_{BIAS} = 5.0V (new chip), I_{OUT} = 50 mA, V_{EN} =V_{IN}, C_{IN} = 1µF, C_{BIAS} = 4.7µF, C_{SS} = 0.01µF (legacy chip), and C_{OUT} = 10µF (unless otherwise noted)

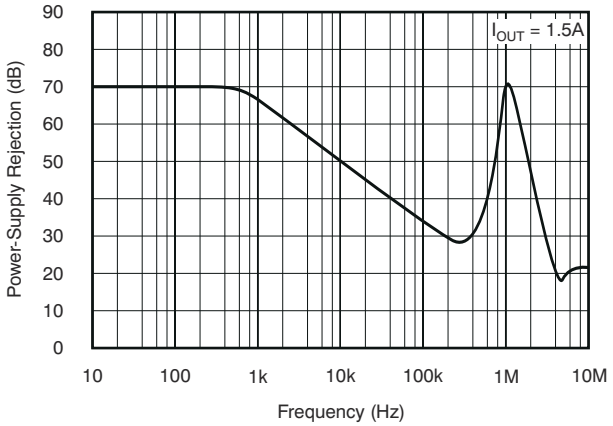


Figure 5-13. V_{BIAS} PSRR vs Frequency (legacy chip)

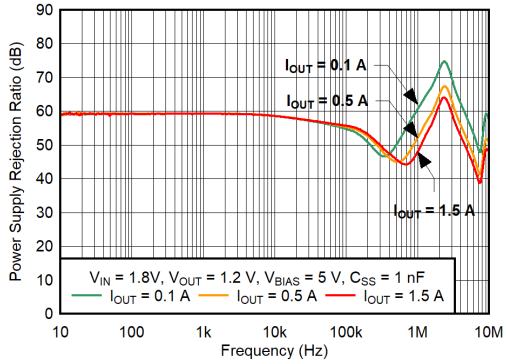


Figure 5-14. V_{BIAS} PSRR vs Frequency (new chip)

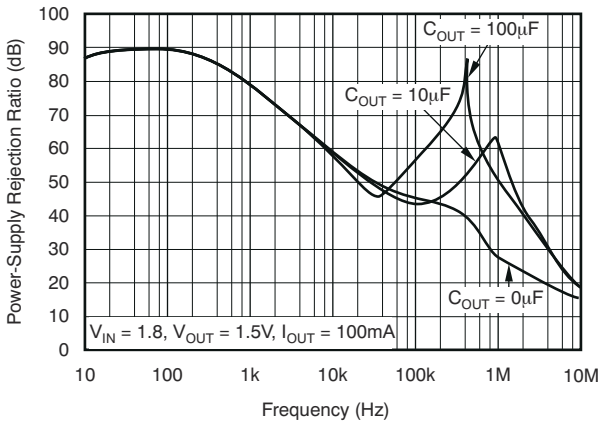


Figure 5-15. V_{IN} PSRR vs Frequency (legacy chip)

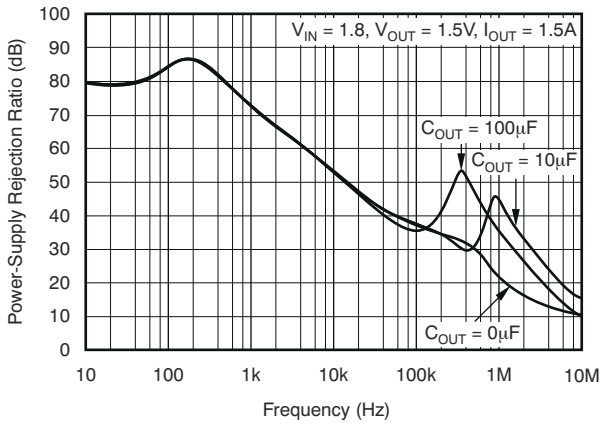
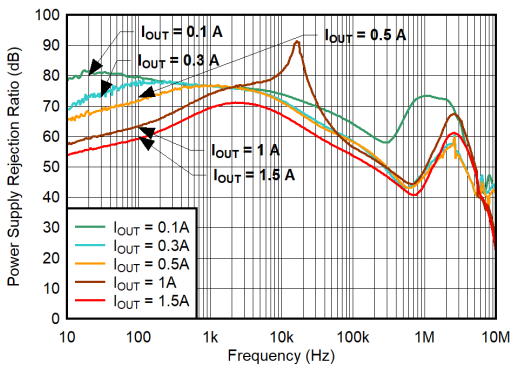


Figure 5-16. V_{IN} PSRR vs Frequency (legacy chip)



New chip

Figure 5-17. V_{IN} PSRR vs Frequency (new chip)

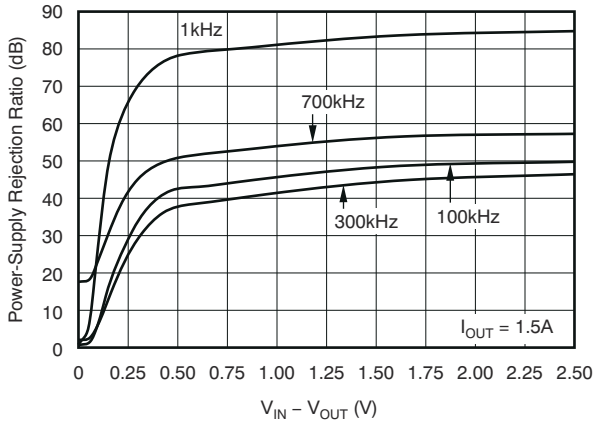


Figure 5-18. V_{IN} PSRR vs V_{IN} – V_{OUT} (legacy chip)

5.6 Typical Characteristics (continued)

at T_J = 25°C, V_{OUT} = 1.5V, V_{IN} = $V_{OUT(NOM)}$ + 0.3V, V_{BIAS} = 3.3V (legacy chip), V_{BIAS} = 5.0V (new chip), I_{OUT} = 50 mA, V_{EN} =V_{IN}, C_{IN} = 1µF, C_{BIAS} = 4.7µF, C_{SS} = 0.01µF (legacy chip), and C_{OUT} = 10µF (unless otherwise noted)

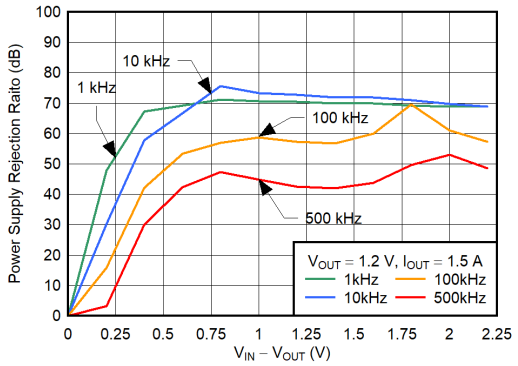


Figure 5-19. V_{IN} PSRR vs (V_{IN} – V_{OUT}) (new chip)

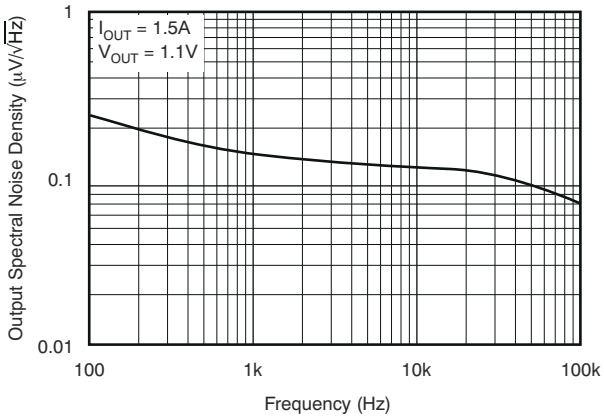


Figure 5-20. Noise Spectral Density (legacy chip)

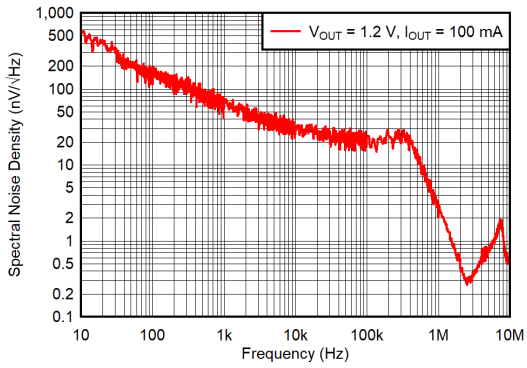


Figure 5-21. Noise Spectral Density (new chip)

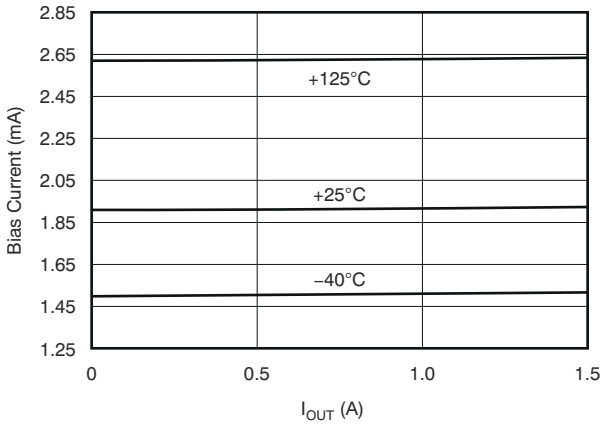


Figure 5-22. I_{BIAS} vs I_{OUT} and Temperature (legacy chip)

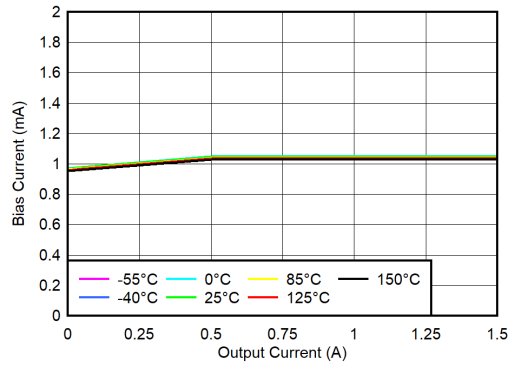


Figure 5-23. BIAS Pin Current vs Output Current and Temperature (T_J) (new chip)

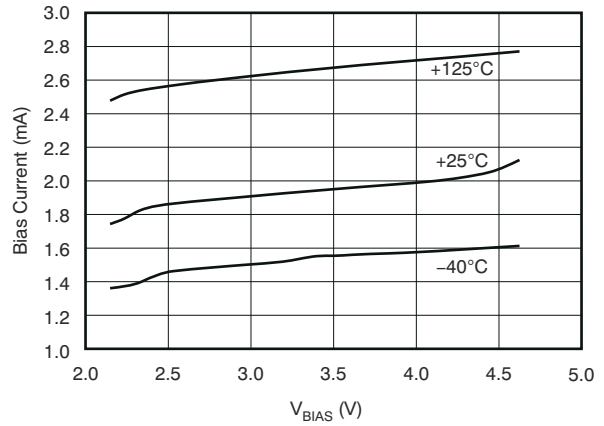


Figure 5-24. I_{BIAS} vs V_{BIAS} and V_{OUT} (legacy chip)

5.6 Typical Characteristics (continued)

at T_J = 25°C, V_{OUT} = 1.5V, V_{IN} = $V_{OUT(NOM)}$ + 0.3V, V_{BIAS} = 3.3V (legacy chip), V_{BIAS} = 5.0V (new chip), I_{OUT} = 50 mA, V_{EN} =V_{IN}, C_{IN} = 1µF, C_{BIAS} = 4.7µF, C_{SS} = 0.01µF (legacy chip), and C_{OUT} = 10µF (unless otherwise noted)

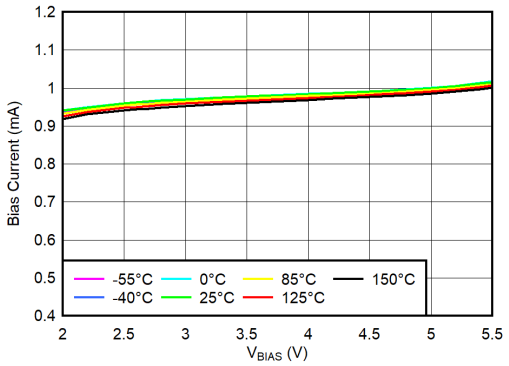


Figure 5-25. BIAS Pin Current vs V_{BIAS} and Temperature (T_J) (new chip)

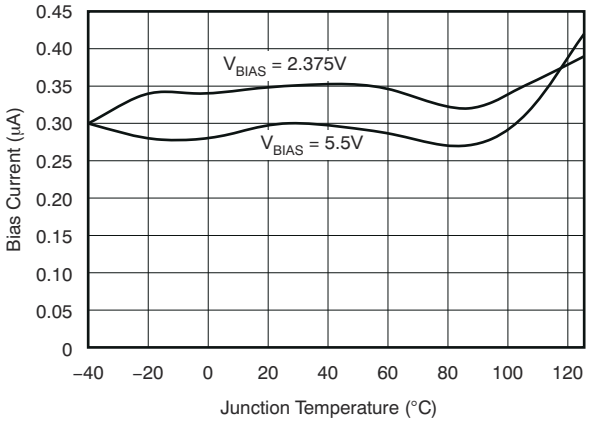


Figure 5-26. I_{BIAS} Shutdown vs Temperature (legacy chip)

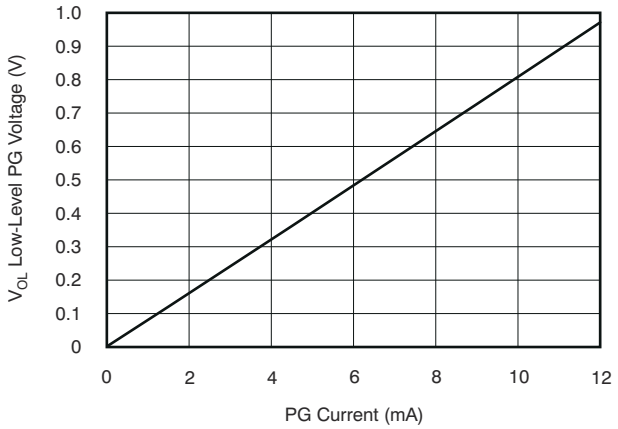


Figure 5-27. Low-Level PG Voltage vs PG Current (legacy chip)

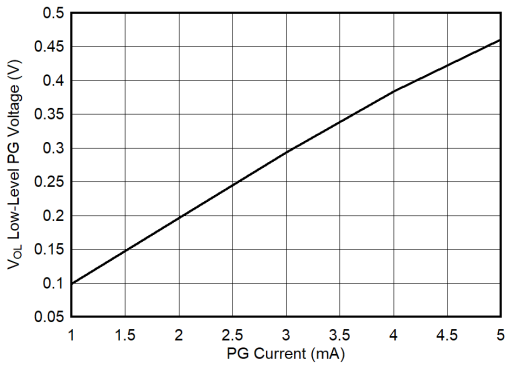


Figure 5-28. Low-Level PG Voltage vs Current (new chip)

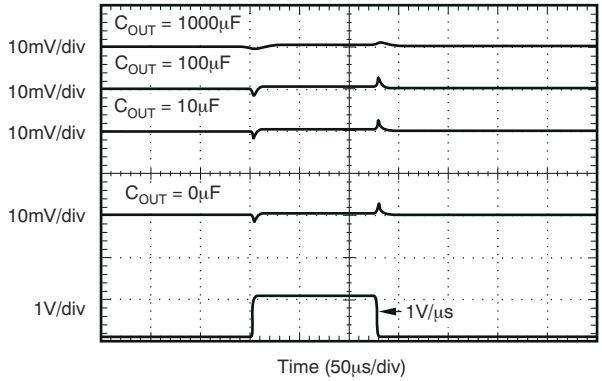


Figure 5-29. V_{BIAS} Line Transient (1.5A) (legacy chip)

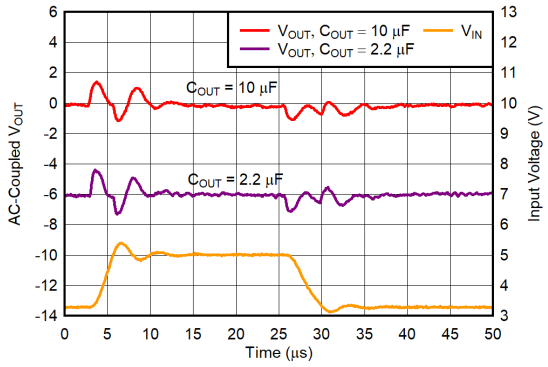


Figure 5-30. V_{BIAS} Line Transient (new chip)

5.6 Typical Characteristics (continued)

at T_J = 25°C, V_{OUT} = 1.5V, V_{IN} = $V_{OUT(NOM)}$ + 0.3V, V_{BIAS} = 3.3V (legacy chip), V_{BIAS} = 5.0V (new chip), I_{OUT} = 50 mA, V_{EN} =V_{IN}, C_{IN} = 1µF, C_{BIAS} = 4.7µF, C_{SS} = 0.01µF (legacy chip), and C_{OUT} = 10µF (unless otherwise noted)

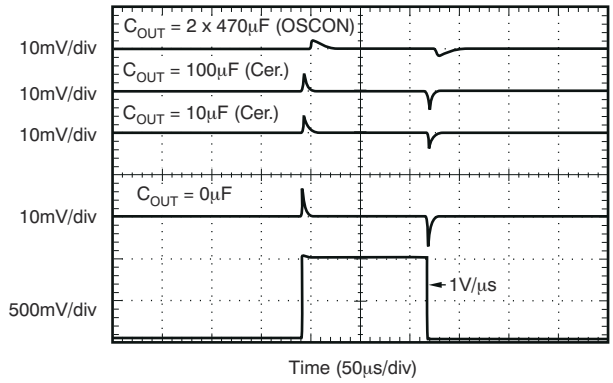
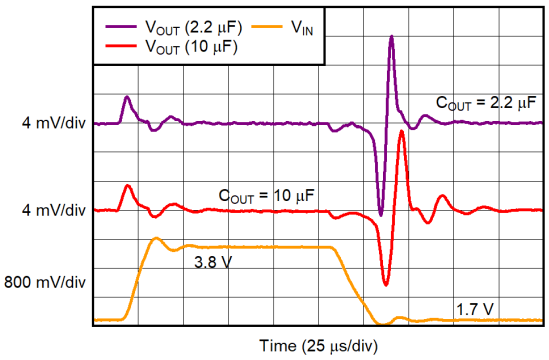


Figure 5-31. V_{IN} Line Transient (legacy chip)



New chip

Figure 5-32. V_{IN} Line Transient (new chip)

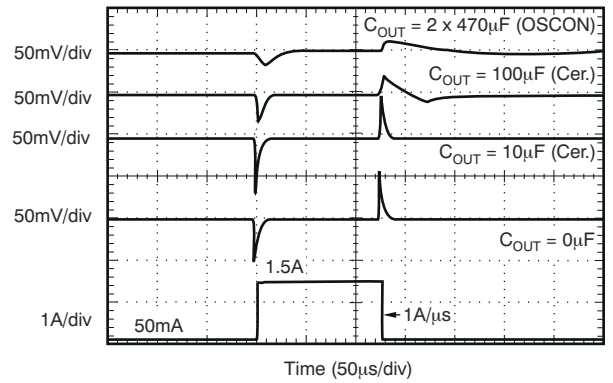


Figure 5-33. Output Load Transient Response (legacy chip)

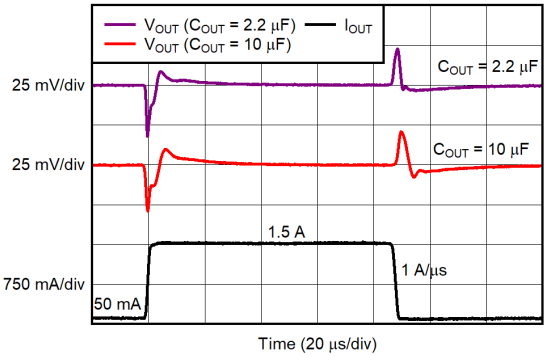


Figure 5-34. Output Load Transient Response (new chip)

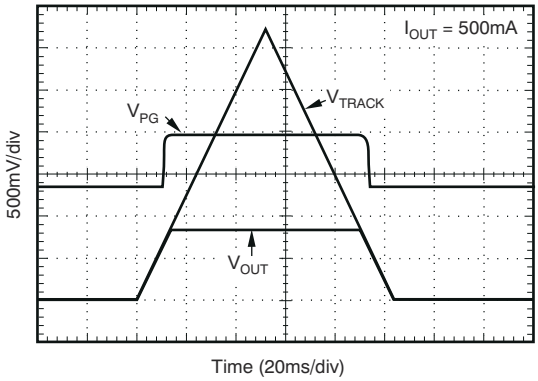


Figure 5-35. Tracking Response (legacy chip)

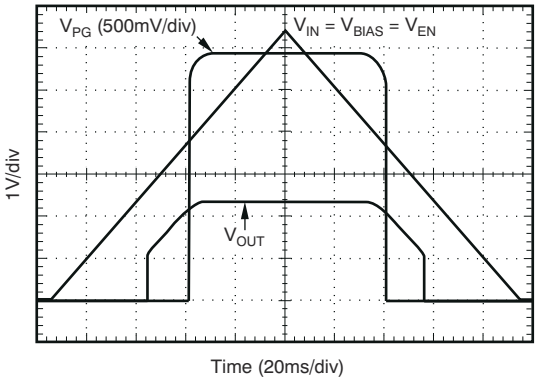


Figure 5-36. Power-Up/Power-Down (legacy chip)

5.6 Typical Characteristics (continued)

at T_J = 25°C, V_{OUT} = 1.5V, V_{IN} = $V_{OUT(NOM)}$ + 0.3V, V_{BIAS} = 3.3V (legacy chip), V_{BIAS} = 5.0V (new chip), I_{OUT} = 50 mA, V_{EN} =V_{IN}, C_{IN} = 1µF, C_{BIAS} = 4.7µF, C_{SS} = 0.01µF (legacy chip), and C_{OUT} = 10µF (unless otherwise noted)

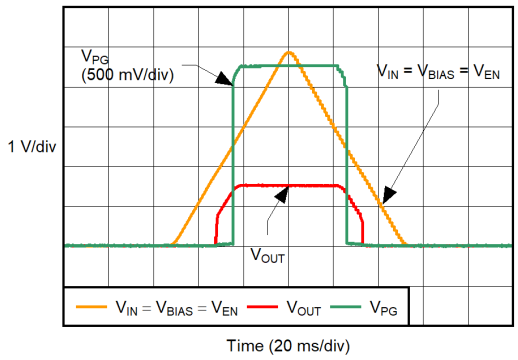


Figure 5-37. Power-Up, Power-Down (new chip)

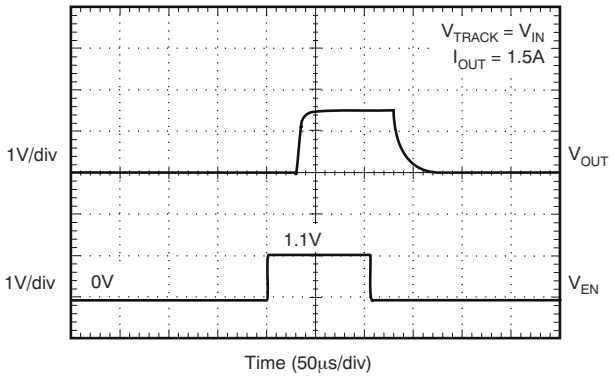


Figure 5-38. Turn-On Response (legacy chip)

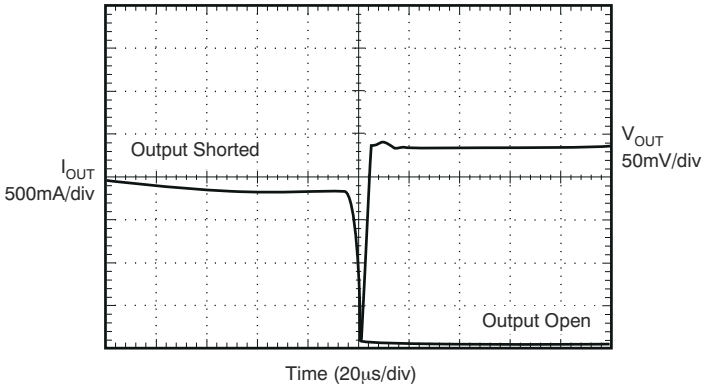


Figure 5-39. Output Short Circuit Recovery

6 Detailed Description

6.1 Overview

The TPS743 belongs to a family of ultra-low dropout regulators that feature soft-start and tracking capabilities. These regulators use a low current bias input to power all internal control circuitry, allowing the NMOS pass transistor to regulate very low input and output voltages.

The use of an NMOS-pass FET offers several critical advantages for many applications. Unlike a PMOS topology device, the output capacitor has little effect on loop stability. This architecture allows the TPS743 devices to be stable with any output capacitor ≥ 2.2µF. Transient response is also superior to PMOS topologies, particularly for low V_{IN} applications.

The TPS743 devices features a TRACK pin that allows the output to track an external supply. This feature is useful in minimizing the stress on ESD structures that are present between the CORE and I/O power pins of many processors. A power-good (PG) output is also available to allow supply monitoring and sequencing of follow-on supplies. To control the output turn-on, an enable (EN) pin with hysteresis and deglitch is provided to allow slow-ramping signals to be utilized for sequencing the device. The low V_{IN} and V_{OUT} capability allows for inexpensive, easy-to-design, and efficient linear regulation between the multiple supply voltages often present in processor intensive systems.

6.2 Functional Block Diagram

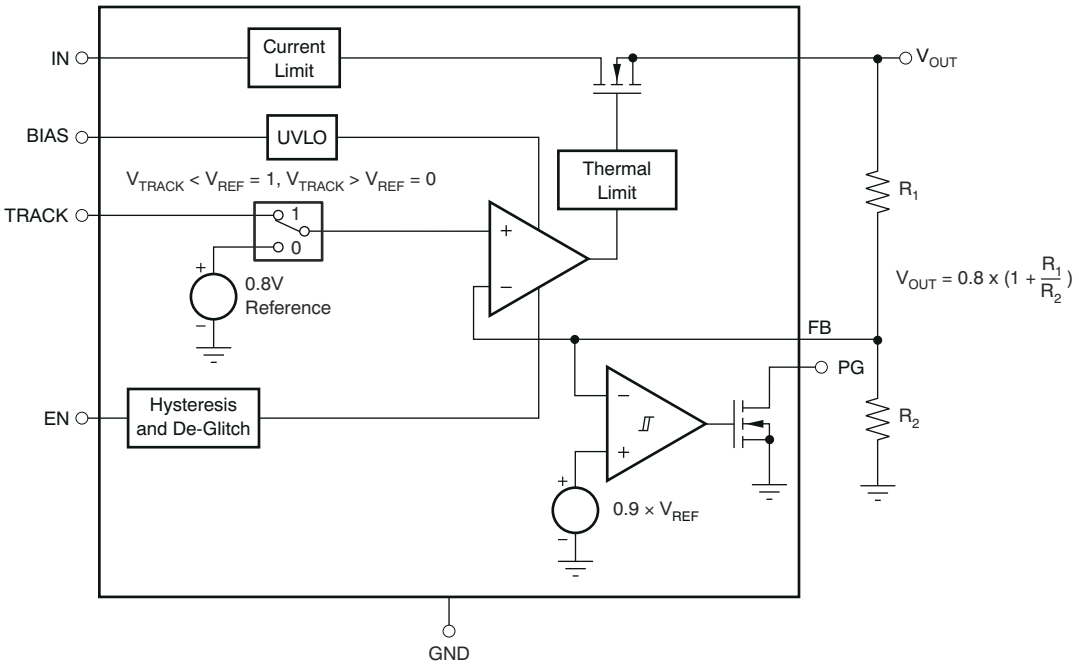


Figure 6-1. Legacy chip Functional Block Diagram

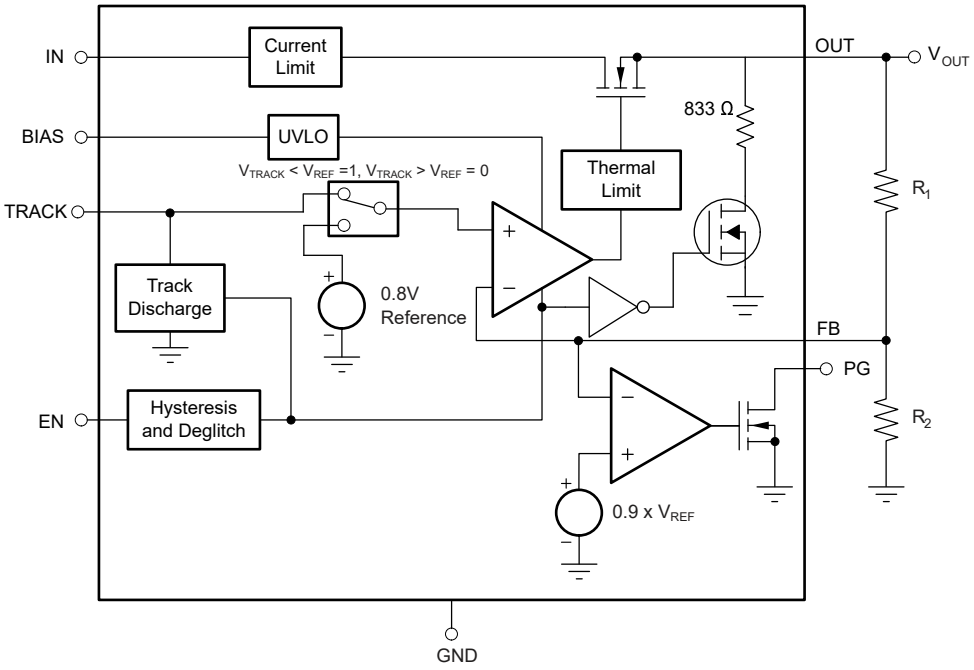


Figure 6-2. New chip Functional Block Diagram

6.3 Feature Description

6.3.1 Enable/Shutdown

The enable (EN) pin is active high and is compatible with standard digital signaling levels. V_{EN} below 0.4V turns the regulator off, while V_{EN} above 1.1V turns the regulator on. Unlike many regulators, the enable circuitry has hysteresis and deglitching for use with relatively slow-ramping analog signals. This configuration allows the TPS743 to be enabled by connecting the output of another supply to the EN pin. The enable circuitry typically has 50mV of hysteresis and a deglitch circuit to help avoid on-off cycling because of small glitches in the V_{EN} signal.

The enable threshold is typically 0.8V and varies with temperature and process variations. Temperature variation is approximately –1mV/°C; therefore, process variation accounts for most of the variation in the enable threshold. If precise turn-on timing is required, a fast rise-time signal must be used to enable the TPS743.

If not used, EN can be connected to either IN or BIAS. If EN is connected to IN, EN must be connected as close as possible to the largest capacitance on the input to prevent voltage droops on that line from triggering the enable circuit.

6.3.2 Power-Good (QFN Package Only)

The power-good (PG) pin is an open-drain output and can be connected to any 5.5V or lower rail through an external pullup resistor. This pin requires at least 1.1V on V_{BIAS} to have a valid output. The PG output is high-impedance when V_{OUT} is greater than $V_{IT} + V_{HYS}$. If V_{OUT} drops below V_{IT} or if V_{BIAS} drops below 1.9V, the open-drain output turns on and pulls the PG output low. The PG pin also asserts when the device is disabled. The recommended operating condition of PG pin sink current is up to 1mA, so the pullup resistor for PG must be in the range of 10kΩ to 1MΩ. PG is only provided on the QFN package. If output voltage monitoring is not needed, the PG pin can be left floating.

6.3.3 Internal Current Limit

The TPS743 features a factory-trimmed, accurate current limit that is flat over temperature and supply voltage. The current limit allows the device to supply surges of up to 1.8A and maintain regulation. The current limit responds in about 10µs to reduce the current during a short-circuit fault. Recovery from a short-circuit condition is well-controlled and results in very little output overshoot when the load is removed. See Output Short-Circuit Recovery in the *Typical Characteristics* section for output short-circuit recovery performance.

The internal current limit protection circuitry of the TPS743 is designed to protect against overload conditions. This circuitry is not intended to allow operation above the rated current of the device. Continuously running the TPS743 above the rated current degrades device reliability.

6.4 Device Functional Modes

6.4.1 Normal Operation

The device regulates to the nominal output voltage under the following conditions:

- The input voltage and bias voltage are both at least at the respective minimum specifications.
- The enable voltage has previously exceeded the enable rising threshold voltage and has not decreased below the enable falling threshold.
- The output current is less than the current limit.
- The device junction temperature is less than the maximum specified junction temperature.
- The device is not operating in dropout.

6.4.2 Dropout Operation

If the input voltage is lower than the nominal output voltage plus the specified dropout voltage, but all other conditions are met for normal operation, the device operates in dropout mode. In this condition, the output voltage is the same as the input voltage minus the dropout voltage. The transient performance of the device is significantly degraded because the pass device is in a triode state and no longer controls the current through the LDO. Line or load transients in dropout can result in large output voltage deviations.

6.4.3 Disabled

The device is disabled under the following conditions:

- The input or bias voltages are below the respective minimum specifications.
- The enable voltage is less than the enable falling threshold voltage or has not yet exceeded the enable rising threshold.
- The device junction temperature is greater than the thermal shutdown temperature.

Table 6-1 shows the conditions that lead to the different modes of operation.

Table 6-1. Device Functional Mode Comparison

OPERATING MODE	PARAMETER				
	V_{IN}	V_{EN}	V_{BIAS}	I_{OUT}	T_J
Normal mode	$V_{IN} > V_{OUT(nom)} + V_{DO} (V_{IN})$	$V_{EN} > V_{EN(high)}$	$V_{BIAS} \geq V_{OUT} + 1.4$ V	$I_{OUT} < I_{CL}$	$T_J < 125°C$
Dropout mode	$V_{IN} < V_{OUT(nom)} + V_{DO} (V_{IN})$	$V_{EN} > V_{EN(high)}$	$V_{BIAS} < V_{OUT} + 1.4$ V	—	$T_J < 125°C$
Disabled mode (any true condition disables the device)	$V_{IN} < V_{IN(min)}$	$V_{EN} < V_{EN(low)}$	$V_{BIAS} < V_{BIAS(min)}$	—	$T_J > 155°C$

7 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

7.1 Application Information

7.1.1 Input, Output, and Bias Capacitor Requirements

The legacy chip device does not require any output capacitor for stability, however, the new chip requires an output capacitor of 2.2µF or greater. If an output capacitor is needed, the device is designed to be stable for all available types and values of output capacitance. The device is also stable with multiple capacitors in parallel, of any type or value.

The capacitance required on the IN and BIAS pins is strongly dependent on the input supply source impedance. To counteract any inductance in the input, the minimum recommended capacitor for V_{IN} and V_{BIAS} is 1µF. If V_{IN} and V_{BIAS} are connected to the same supply, the recommended minimum capacitor for V_{BIAS} is 4.7µF. Good quality, low ESR capacitors must be used on the input; ceramic X5R and X7R capacitors are preferred. These capacitors must be placed as close the pins as possible for optimum performance.

7.1.2 Transient Response

The TPS743 is designed to have transient response within 5% for most applications without any output capacitor. In some cases, the transient response can be limited by the transient response of the input supply. This limitation is especially true in applications where the difference between the input and output is less than 300mV. In this case, adding additional input capacitance improves the transient response much more than just adding additional output capacitance. With a solid input supply, adding additional output capacitance reduces undershoot and overshoot during a transient at the expense of a slightly longer V_{OUT} recovery time. Refer to Output Load Transient Response in the *Typical Characteristics* section. Because the legacy chip is stable without an output capacitor and the new chip is stable with output capacitors ≥ 2.2µF, many applications can allow for little or no capacitance at the LDO output. For these applications, local bypass capacitance for the device under power can be sufficient to meet the transient requirements of the application. This design reduces the total solution cost by avoiding the need to use expensive high-value capacitors at the LDO output.

7.1.3 Dropout Voltage

The TPS743 offers industry-leading dropout performance, making the device well-suited for high-current low V_{IN}/low V_{OUT} applications. The extremely low dropout of the TPS743 allows the device to be used instead of a DC/DC converter and still achieve good efficiencies. This efficiency allows users to rethink the power architecture for user applications to find the smallest, simplest, and lowest cost solution.

There are two different specifications for dropout voltage with the TPS743. The first specification (as shown in Figure 7-1) is referred to as *V_{IN} Dropout* and is for users wishing to apply an external bias voltage to achieve low dropout. This specification assumes that V_{BIAS} is at least 1.62V above V_{OUT}, which is the case for V_{BIAS} when powered by a 3.3V rail with 5% tolerance and with V_{OUT} = 1.5V. If V_{BIAS} is higher than 3.3V × 0.95 or V_{OUT} is less than 1.5V, V_{IN} dropout is less than specified.

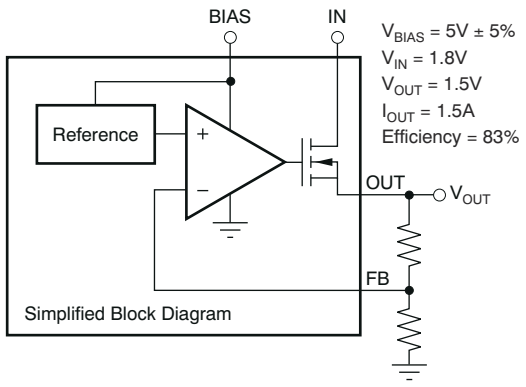


Figure 7-1. Typical Application of the TPS743 Using an Auxiliary Bias Rail

The second specification (shown in Figure 7-2), referred to as *V_{BIAS} Dropout*, is for users who wish to tie IN and BIAS together. This option allows the device to be used in applications where an auxiliary bias voltage is unavailable or low dropout is not required. Dropout is limited by BIAS in these applications because V_{BIAS} provides the gate drive to the pass FET, and therefore must be 1.4V above V_{OUT}. Because of this usage, IN and BIAS tied together easily consume huge power. Pay attention not to exceed the power rating of the IC package.

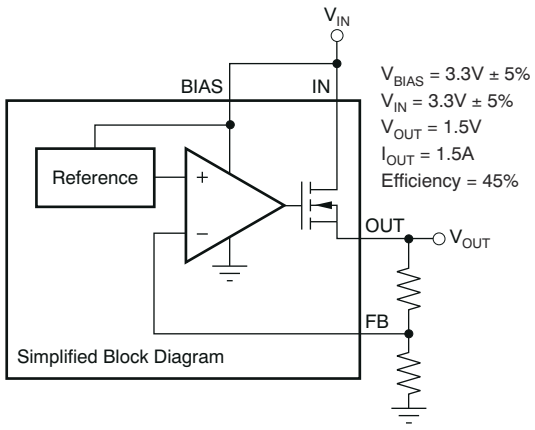
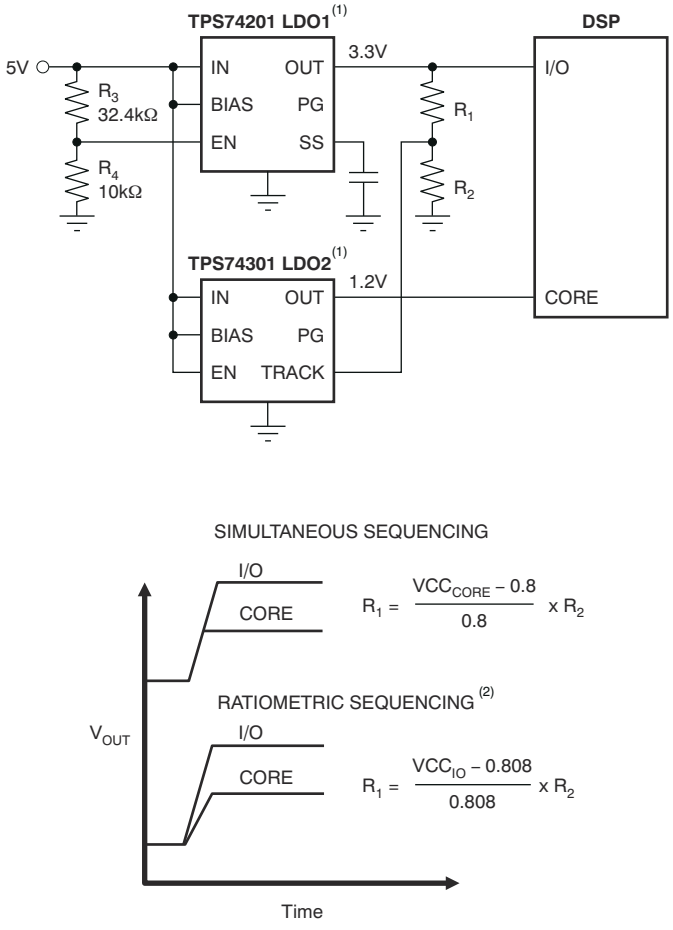


Figure 7-2. Typical Application of the TPS743xx Without an Auxiliary Bias

7.1.4 Programmable Sequencing With Track

The TPS743 features a track pin that allows the output to track an external supply at start-up. While the TRACK input is below 0.8V, the error amplifier regulates the FB pin to the TRACK input. Properly choosing the resistor divider network (R_1 and R_2) as shown in Figure 7-3 enables the regulator output to track the external supply to obtain a simultaneous or ratiometric start-up. Once the TRACK input reaches 0.8V, the error amplifier regulates the FB pin to the 0.8V internal reference. Further increases to the TRACK input have no effect.



NOTES: (1) Capacitors on IN, BIAS, and OUT along with the resistors necessary to set the output voltage have been omitted for simplification.
(2) Lowest value for V_{CORE} and highest value for R_2 should be used in this calculation. R_1 must be the closest standard value below the calculated value for proper ratiometric sequencing.

Figure 7-3. Various Sequencing Methods Using the TRACK Pin

The maximum recommended value for R_2 is 100kΩ. Once R_2 is selected, R_1 is calculated using one of the equations given in Figure 7-3.

7.1.5 Sequencing Requirements

The device can have V_{IN}, V_{BIAS}, V_{EN}, and V_{TRACK} sequenced in any order without causing damage to the device. However, for the track function to work as intended, certain sequencing rules must be applied. V_{BIAS} must be present and the device enabled before the track signal starts to ramp. V_{IN} must ramp up faster than the external supply being tracked so that the tracking signal does not drive the device into V_{IN} dropout as V_{OUT} ramps up. The preferred method to sequence the tracking device is to have V_{IN}, V_{BIAS}, and V_{EN} above the minimum

required voltages before enabling the master supply to initiate the startup sequence. This method is illustrated in Figure 7-3. Resistors R_3 and R_4 disable the master supply until the input voltage is above 3.52V (typical).

If the TRACK pin is not needed the pin must be connected to V_{IN} for the legacy chip, for the new chip this pin can be left floating. Configured in this way, the device starts up typically within 40µs (legacy chip) or 100µs (new chip), which can result in large inrush current that can cause the input supply to droop. If soft-start is needed, consider the TPS742 or TPS744 devices.

Note

NOTE: When V_{BIAS} and V_{EN} are present and V_{IN} is not supplied, this device outputs approximately 50µA of current from OUT. Although this condition does not cause any damage to the device, the output current can charge up the OUT node if total resistance between OUT and GND (including external feedback resistors) is greater than 10kΩ.

7.2 Typical Application

7.2.1 Adjustable Voltage Part and Setting

Figure 7-4 is a typical application circuit for the TPS74301 adjustable device.

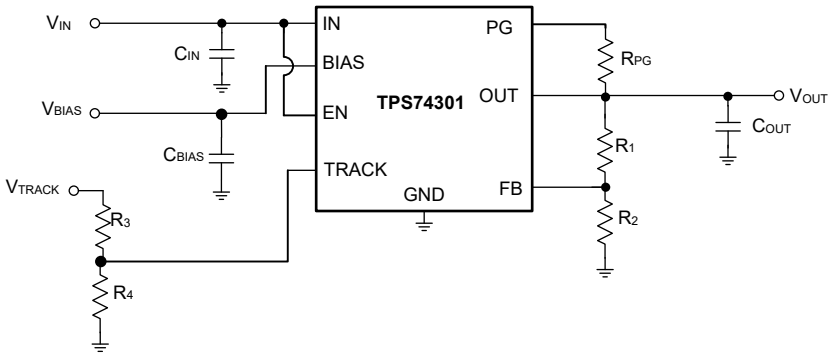


Figure 7-4. Typical Application Circuit for the TPS74301

R_1 and R_2 can be calculated for any output voltage using the formula shown in Table 7-1. Refer to Table 7-1 for sample resistor values of common output voltages. To achieve the maximum accuracy specifications, R_2 must be ≤ 4.99kΩ.

Table 7-1. Standard 1% Resistor Values for Programming the Output Voltage (1)

R_1 (kΩ)	R_2 (kΩ)	V_{OUT} (V)
Short	Open	0.8
0.619	4.99	0.9
1.13	4.53	1.0
1.37	4.42	1.05
1.87	4.99	1.1
2.49	4.99	1.2
4.12	4.75	1.5
3.57	2.87	1.8
3.57	1.69	2.5
3.57	1.15	3.3

(1) $V_{OUT} = 0.8 \times (1 + R1/R2)$

7.2.2 Design Requirements

The design goals are V_{IN} = 1.8 V, V_{OUT} = 1.5 V, and I_{OUT} = 1 A (maximum). The design optimizes transient response and meets a 1-ms start-up time with a start-up dominated by the soft-start feature. The input supply comes from a supply on the same circuit board. The available system rails for V_{BIAS} are 2.7 V, 3.3 V, and 5 V.

The design space consists of C_{IN}, C_{OUT}, C_{BIAS}, C_{SS}, V_{BIAS}, R_1, R_2, and R_3, and the circuit is from Section 7.2.1.

This example uses a V_{IN} of 1.8 V, with a V_{BIAS} of 2.5 V.

Table 7-2. Design Parameters

PARAMETER	VALUE
V_{IN}	1.8V
V_{OUT}	1.5V
I_{OUT}	1A
V_{BIAS}	2.5V

7.2.3 Detailed Design Procedure

This is assuming the table for the standard capacitor values is put back in as Table 6-1.

Using Section , R1 is selected to be 4.12 kΩ for V_{OUT} = 1.5 V and R2 is 4.75 kΩ. Using Section 6.4, C_{SS} is 1000 pF for a 1-ms typical start-up time. For optimal performance, 5-V rail for a Bias supply is used. And R3 of 100 kΩ is selected as the PG bus is used by other devices with additional 100-kΩ pullup resistors.

A C_{IN} of 10 µF is used for better transient performance on the input supply, a C_{BIAS} of 1 µF is used to verify that the Bias supply is solid, and a C_{OUT} of 1 µF is used to provide some local capacitance on the output.

7.2.4 Application Performance Plots

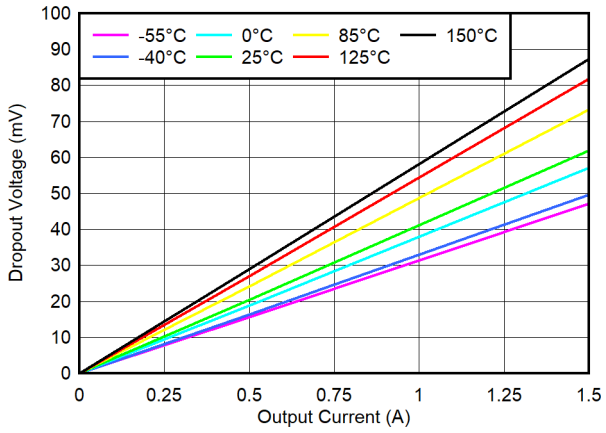


Figure 7-5. V_{IN} Dropout Voltage vs I_{OUT} and Temperature (T_J)

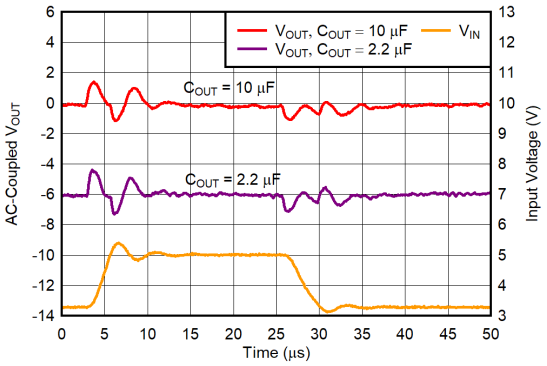


Figure 7-6. V_{BIAS} Line Transient

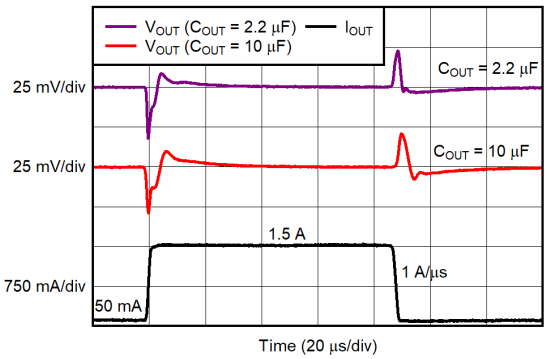


Figure 7-7. Output Load Transient Response (new chip)

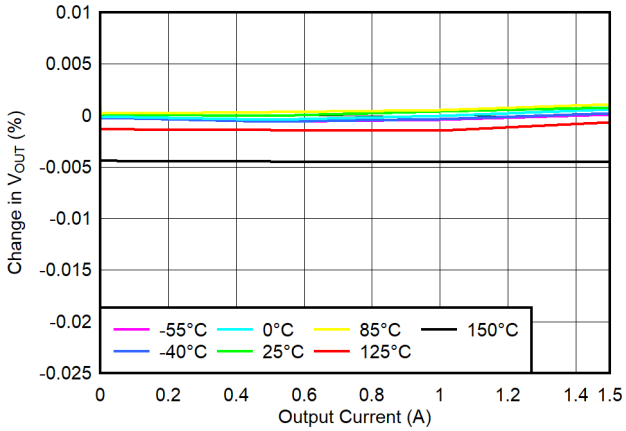


Figure 7-8. Load Regulation

7.3 Power Supply Recommendations

The TPS743 devices are designed to operate from an input voltage from 1.1 V to 5.5 V, provided the bias rail is at least 1.4-V higher than the input supply. The bias rail and the input supply must both provide adequate headroom and current for the device to operate normally.

Connect a low-output impedance power supply directly to the IN pin of the TPS743 devices. This supply must have at least 1 µF of capacitance near the IN pin for stability. A supply with similar requirements must also be connected directly to the bias rail with a separate 1 µF or larger capacitor.

If the IN pin is tied to the bias pin, a minimum 4.7 µF of capacitance is needed for stability.

To increase the overall PSRR of the solution at higher frequencies, use a pi-filter or ferrite bead before the input capacitor.

7.4 Layout

7.4.1 Layout Guidelines

7.4.1.1 Layout Recommendations and Power Dissipation

An optimal layout can greatly improve transient performance, PSRR, and noise. To minimize the voltage droop on the input of the device during load transients, the capacitance on IN and BIAS must be connected as close as possible to the device. This capacitance also minimizes the effects of parasitic inductance and resistance of the input source and can therefore improve stability. To achieve optimal transient performance and accuracy, the top side of R_1 in Figure 7-4 must be connected as close as possible to the load. If BIAS is connected to IN, connecting the BIAS as close as possible to the sense point of the input supply is recommended. This connection minimizes the voltage droop on BIAS during transient conditions and can improve the turn-on response.

Knowing the device power dissipation and proper sizing of the thermal plane that is connected to the tab or pad is critical to avoiding thermal shutdown and providing reliable operation. Power dissipation of the device depends on input voltage and load conditions, and can be calculated using Equation 1:

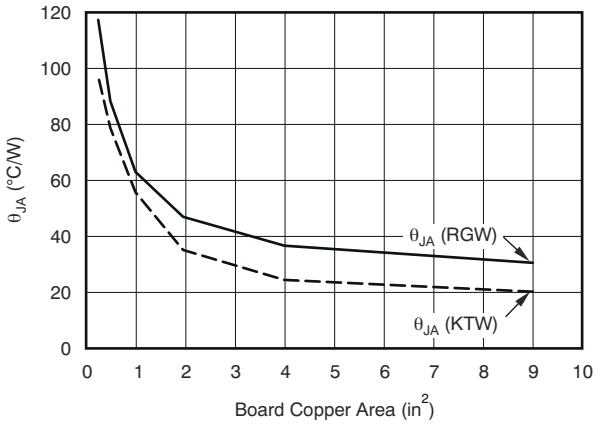
$$P_D = (V_{IN} - V_{OUT}) \times I_{OUT} \quad (1)$$

Power dissipation can be minimized and greater efficiency can be achieved by using the lowest possible input voltage necessary to achieve the required output voltage regulation.

On the QFN (RGW) package, the primary conduction path for heat is through the exposed pad to the printed circuit board (PCB). The pad can be connected to ground or be left floating; however, the pad must be attached to an appropriate amount of copper PCB area to verify the device does not overheat. On the DDPAK (KTW) package, the primary conduction path for heat is through the tab to the PCB. That tab must be connected to ground. The maximum junction-to-ambient thermal resistance depends on the maximum ambient temperature, maximum device junction temperature, and power dissipation of the device and can be calculated using Equation 2:

$$R_{\theta JA} = \frac{(+125^{o}C - T_A)}{P_D} \quad (2)$$

Knowing the maximum $R_{\theta JA}$, the minimum amount of PCB copper area needed for appropriate heatsinking can be estimated using Figure 7-9.



θ_{JA} value at board size of 9in^2 (that is, 3in × 3in) is a JEDEC standard.

Figure 7-9. θ_{JA} vs Board Size

Figure 7-9 shows the variation of θ_{JA} as a function of ground plane copper area in the board. This figure is intended only as a guideline to demonstrate the effects of heat spreading in the ground plane and must not be used to estimate actual thermal performance in real application environments.

Note

NOTE: When the device is mounted on an application PCB, using Ψ_{JT} and Ψ_{JB}, as explained in the Section 7.4.1.1 section is strongly recommended.

7.4.2 Layout Example

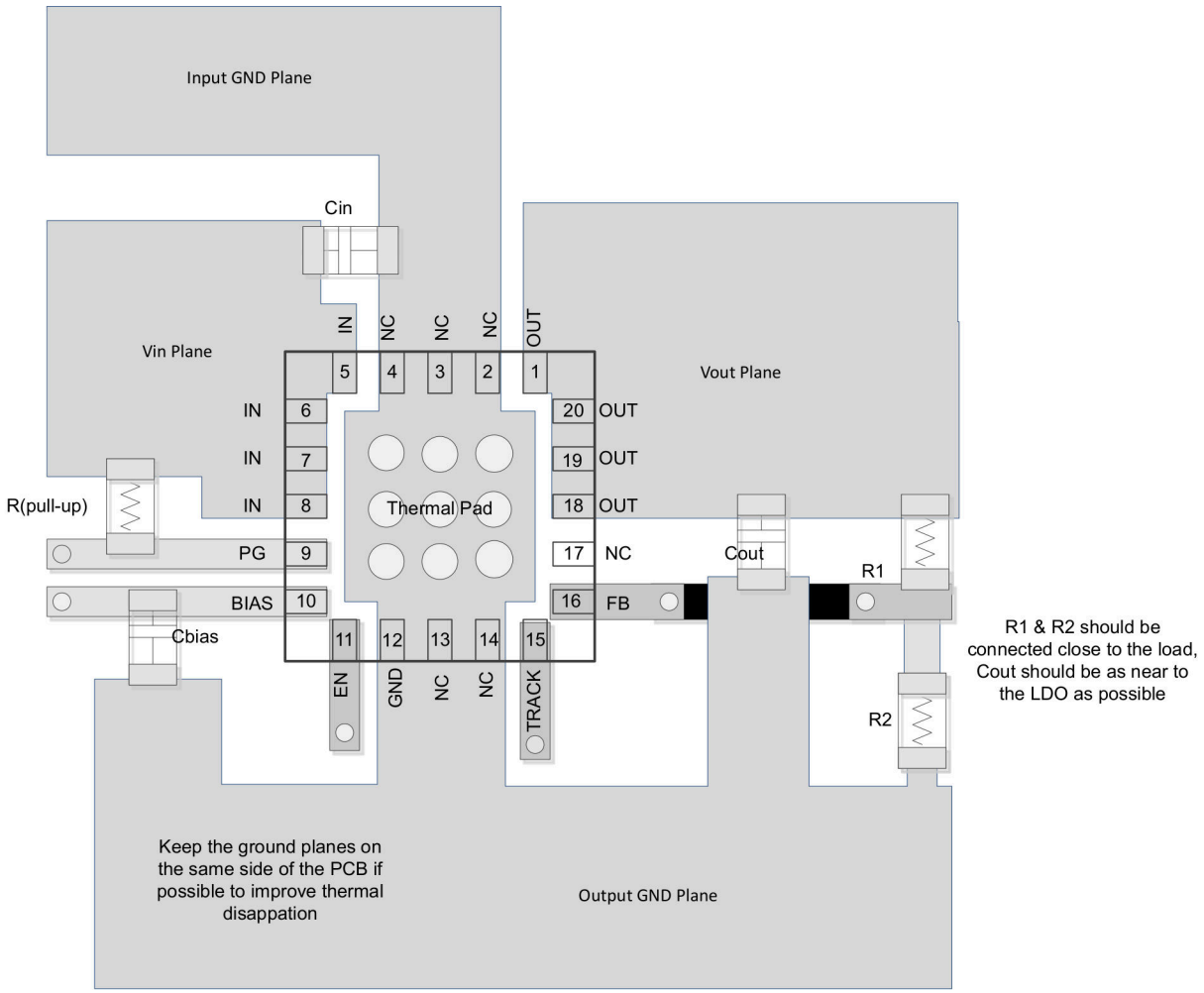


Figure 7-10. Layout Example

7.4.3 Thermal Protection

Thermal protection disables the output when the junction temperature rises to approximately 165°C, allowing the device to cool. When the junction temperature cools to approximately 140°C, the output circuitry is enabled. Depending on power dissipation, thermal resistance, and ambient temperature the thermal protection circuit can cycle on and off. This cycling limits the dissipation of the regulator, protecting the regulator from damage as a result of overheating.

Activation of the thermal protection circuit indicates excessive power dissipation or inadequate heatsinking. For reliable operation, junction temperature must be limited to 125°C maximum. To estimate the margin of safety in a complete design (including heatsink), increase the ambient temperature until thermal protection is triggered; use worst-case loads and signal conditions. For good reliability, thermal protection must trigger at least 40°C above the maximum expected ambient condition of the application. This condition produces a worst-case junction temperature of 125°C at the highest expected ambient temperature and worst-case load.

The internal protection circuitry of the TPS743 is designed to protect against overload conditions. The circuitry is not intended to replace proper heatsinking. Continuously running the TPS743 into thermal shutdown degrades device reliability.

7.4.4 Estimating Junction Temperature

Using the thermal metrics Ψ_{JT} and Ψ_{JB}, shown in the *Section 5.4* table, the junction temperature can be estimated with corresponding formulas (given in Equation 3). For backwards compatibility, an older $\theta_{JC,Top}$ parameter is listed as well.

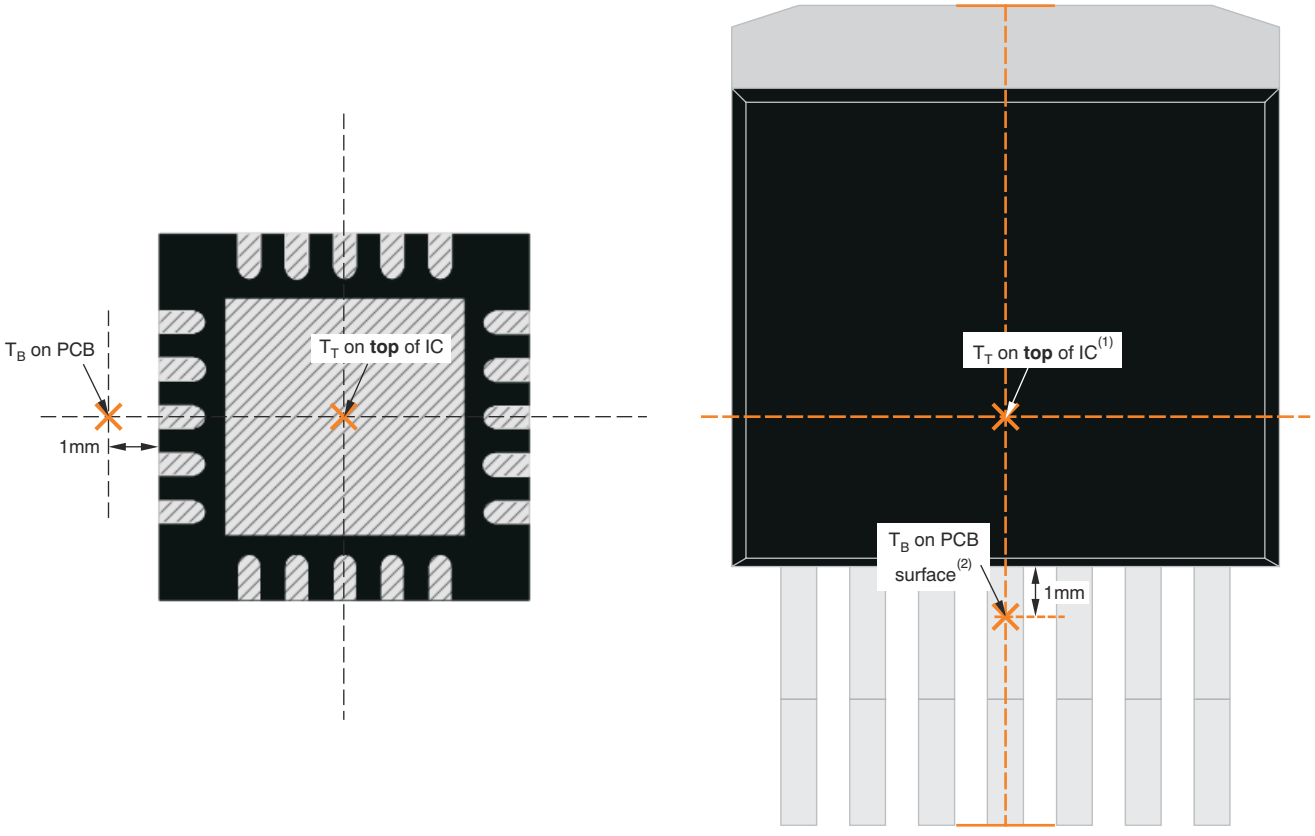
$$\Psi_{JT}: \quad T_J = T_T + \Psi_{JT} \bullet P_D$$
$$\Psi_{JB}: \quad T_J = T_B + \Psi_{JB} \bullet P_D \tag{3}$$

Where P_D is the power dissipation shown by Equation 1, T_T is the temperature at the center-top of the IC package, and T_B is the PCB temperature measured 1mm away from the IC package *on the PCB surface* (as Figure 7-11 shows).

Note

NOTE: Both T_T and T_B can be measured on actual application boards using a thermo-gun (an infrared thermometer).

For more information about measuring T_T and T_B, see the *Using New Thermal Metrics* application note, available for download at www.ti.com.



(a) Example RGW (QFN) Package Measurement

(b) Example KTW (DDPAK) Package Measurement

A. T_T is measured at the center of both the X- and Y-dimensional axes.
B. T_B is measured ***below*** the package lead **on the PCB surface**.

Figure 7-11. Measuring Points for T_T and T_B

Compared with θ_{JA}, the thermal metrics Ψ_{JT} and Ψ_{JB} are less independent of board size, but these metrics do have a small dependency. Figure 7-12 shows characteristic performance of Ψ_{JT} and Ψ_{JB} versus board size.

Looking at Figure 7-12, the RGW package thermal performance has negligible dependency on board size. The KTW package, however, does have a measurable dependency on board size. This dependency exists because the package shape is not point-symmetric to an IC center. In the KTW package, for example (see Figure 7-11), silicon is not beneath the measuring point of T_T which is the center of the X and Y dimension, so that Ψ_{JT} has a dependency. Also, because of that non-point-symmetry, device heat distribution on the PCB is not point-symmetric, either, so that Ψ_{JB} has a dependency.

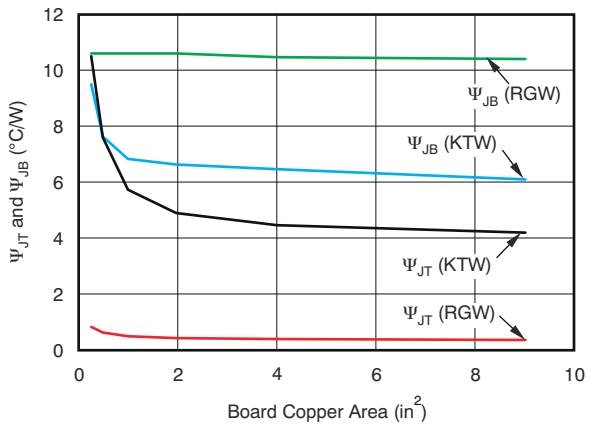


Figure 7-12. Ψ_{JT} and Ψ_{JB} vs Board Size

For a more detailed discussion of why TI does not recommend using θ_{JC},Top to determine thermal characteristics, refer to the *Using New Thermal Metrics* application note, available for download at www.ti.com. Also, refer to the IC Package Thermal Metrics application note (also available on the TI web site) for further information.

8 Device and Documentation Support

TI offers an extensive line of development tools. Tools and software to evaluate the performance of the device, generate code, and develop solutions are listed below.

8.1 Documentation Support

8.1.1 Related Documentation

For related documentation see the following:

- Texas Instruments, *6A Current-Sharing Dual LDO* design guide
- Texas Instruments, *Using New Thermal Metrics* application note

8.1.2 Device Nomenclature

Table 8-1. Device Nomenclature

PRODUCT[1]	V_{OUT}
TPS74301**yyyzM3**	**yyy** is the package designator. **z** is the package quantity. **M3** is a suffix designator for devices that only use the latest manufacturing flow (CSO: RFB). Devices without this suffix can ship with the legacy chip (CSO: DLN) or the new chip (CSO: RFB). The reel packaging label provides CSO information to distinguish which chip is being used. Device performance for new and legacy chips is denoted throughout the document.

(1) For the most current package and ordering information see the Package Option Addendum at the end of this document, or visit the device product folder on www.ti.com.

8.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

8.3 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

8.4 Trademarks

TI E2E™ is a trademark of Texas Instruments.
All trademarks are the property of their respective owners.

8.5 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

8.6 Glossary

TI Glossary	This glossary lists and explains terms, acronyms, and definitions.

9 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision K (December 2009) to Revision L (December 2024)	Page
• Updated the number formatting for tables, figures, and cross-references throughout the document	1
• Changed entire document to align with current family format	1
• Added M3 devices to document	1

Changes from Revision J (December, 2009) to Revision K (August, 2010)	Page
• Revised *Layout Recommendations and Power Dissipation* section	26
• Revised *Estimating Junction Temperature* section	29

10 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TPS74301KTWR	Active	Production	DDPAK/TO-263 (KTW) | 7	500 | LARGE T&R	Yes	SN	Level-3-245C-168 HR	-40 to 85	TPS74301
TPS74301KTWR.A	Active	Production	DDPAK/TO-263 (KTW) | 7	500 | LARGE T&R	Yes	SN	Level-3-245C-168 HR	-40 to 125	TPS74301
TPS74301RGWR	Active	Production	VQFN (RGW) | 20	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	TPS 74301
TPS74301RGWR.A	Active	Production	VQFN (RGW) | 20	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	TPS 74301
TPS74301RGWRG4	Active	Production	VQFN (RGW) | 20	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	TPS 74301
TPS74301RGWRM3	Active	Production	VQFN (RGW) | 20	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	TPS 74301
TPS74301RGWRM3.A	Active	Production	VQFN (RGW) | 20	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	TPS 74301
TPS74301RGWT	Active	Production	VQFN (RGW) | 20	250 | SMALL T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	TPS 74301
TPS74301RGWT.A	Active	Production	VQFN (RGW) | 20	250 | SMALL T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	TPS 74301
TPS74301RGWTG4	Active	Production	VQFN (RGW) | 20	250 | SMALL T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	TPS 74301

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

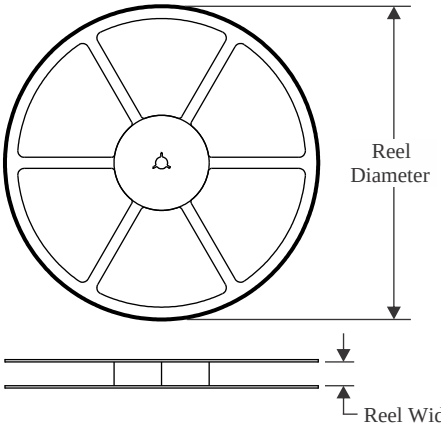
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

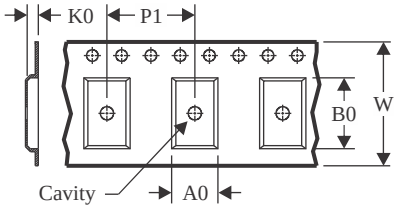
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

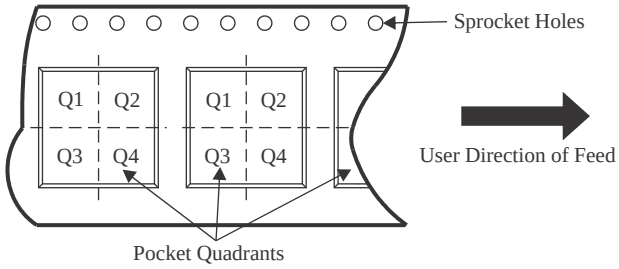


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

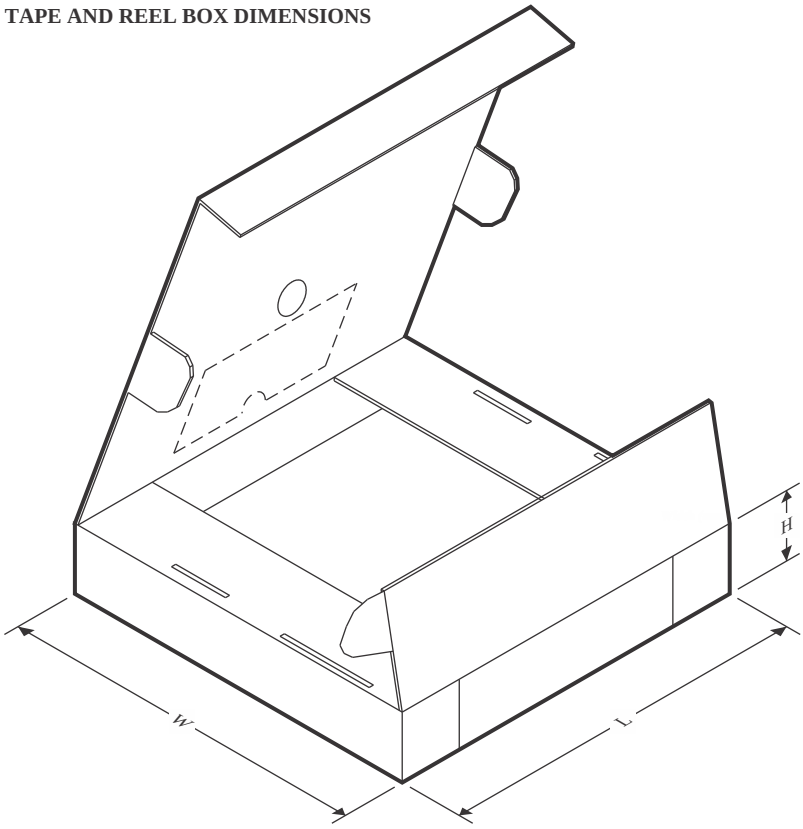
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS74301KTWR	DDPAK/ TO-263	KTW	7	500	330.0	24.4	10.6	15.8	4.9	16.0	24.0	Q2
TPS74301RGWR	VQFN	RGW	20	3000	330.0	12.4	5.3	5.3	1.1	8.0	12.0	Q2
TPS74301RGWRM3	VQFN	RGW	20	3000	330.0	12.4	5.3	5.3	1.1	8.0	12.0	Q2
TPS74301RGWT	VQFN	RGW	20	250	180.0	12.4	5.3	5.3	1.1	8.0	12.0	Q2

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS74301KTWR	DDPAK/TO-263	KTW	7	500	356.0	356.0	45.0
TPS74301RGWR	VQFN	RGW	20	3000	367.0	367.0	35.0
TPS74301RGWRM3	VQFN	RGW	20	3000	367.0	367.0	35.0
TPS74301RGWT	VQFN	RGW	20	250	210.0	185.0	35.0

GENERIC PACKAGE VIEW

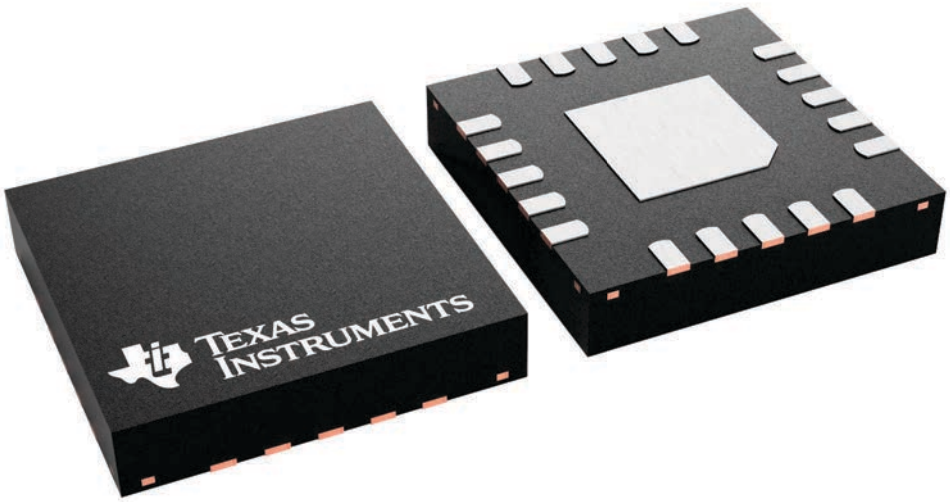
RGW 20

VQFN - 1 mm max height

5 x 5, 0.65 mm pitch

PLASTIC QUAD FLATPACK - NO LEAD

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



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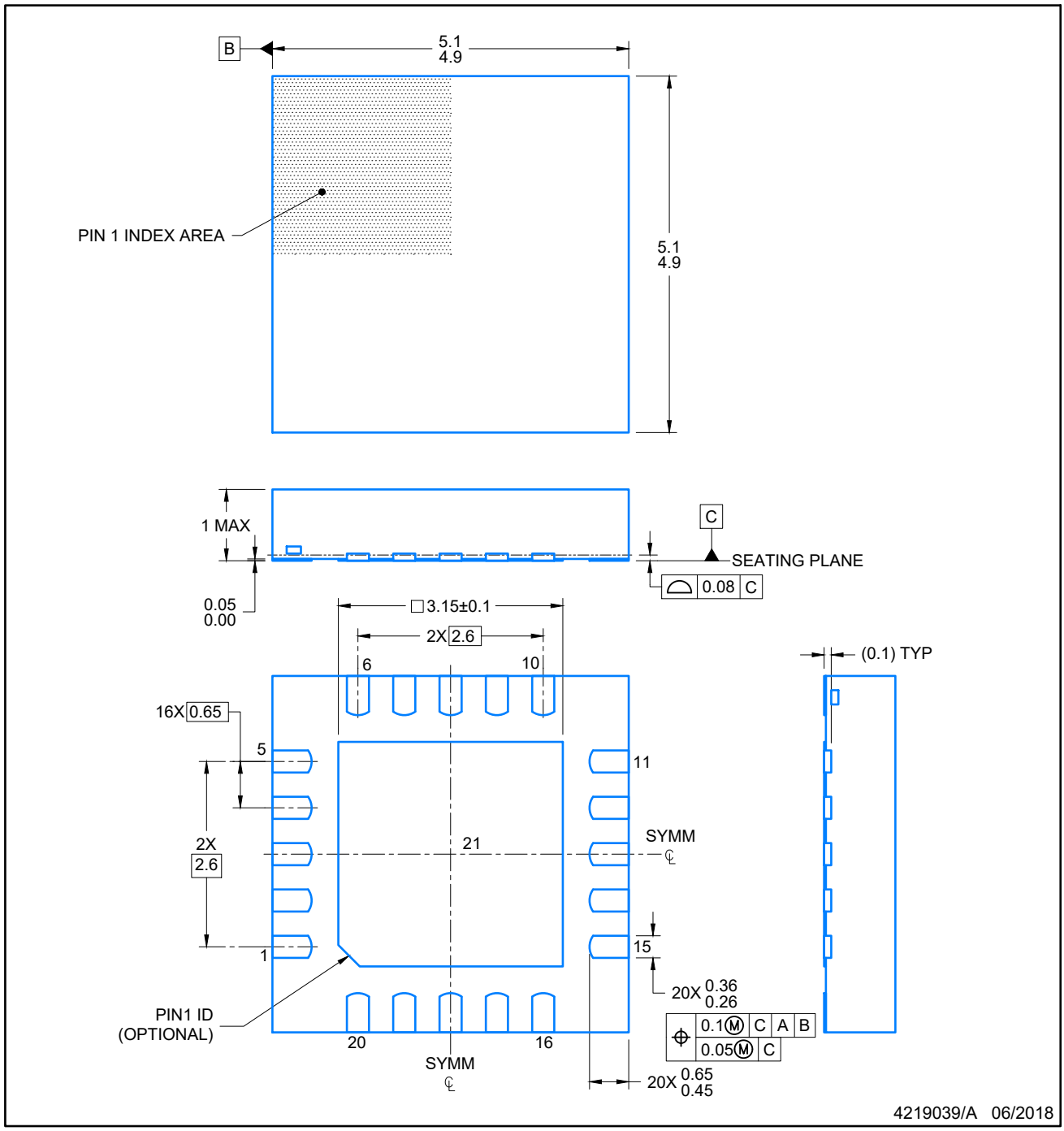
PACKAGE OUTLINE

RGW0020A

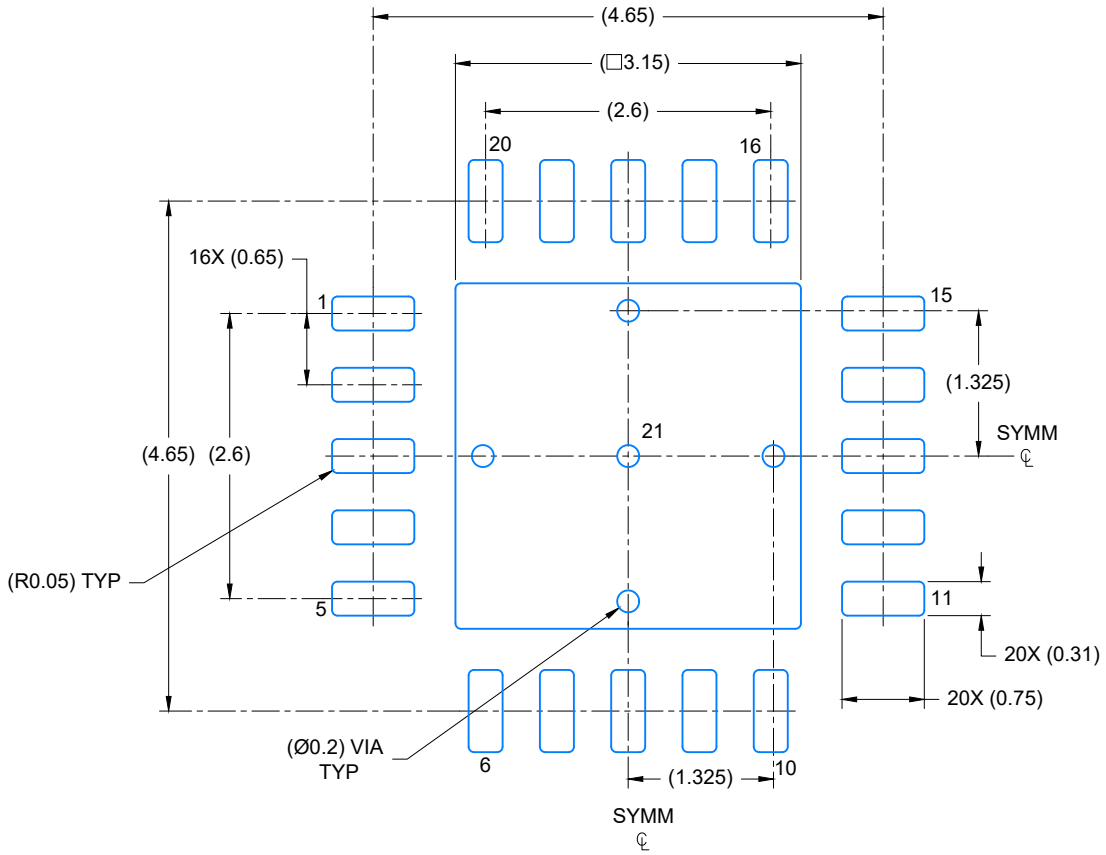
VQFN - 1 mm max height

PLASTIC QUAD FLATPACK-NO LEAD



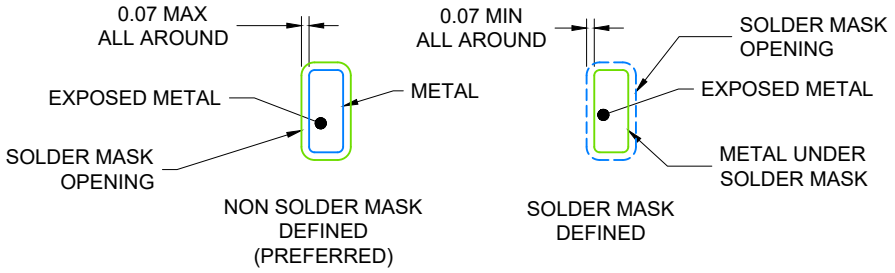
NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for optimal thermal and mechanical performance.



LAND PATTERN EXAMPLE

SCALE: 15X



SOLDER MASK DETAILS

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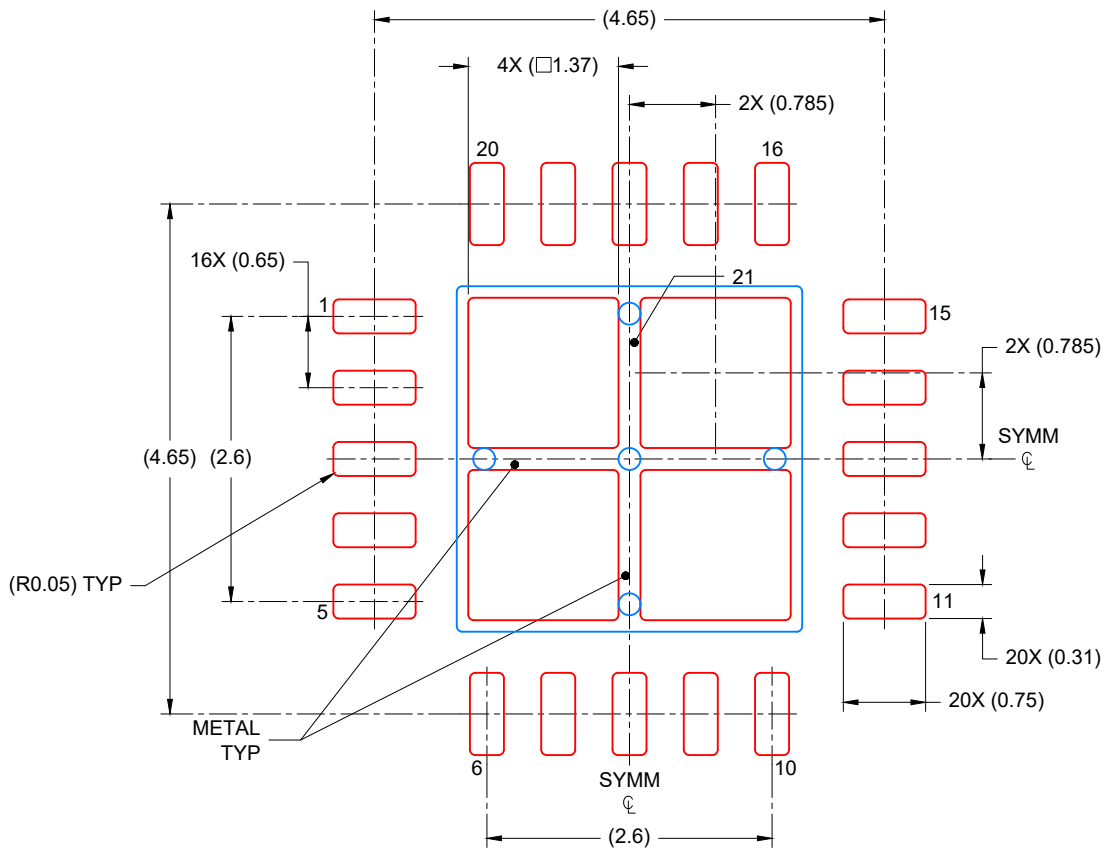
NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

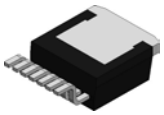
EXPOSED PAD
75% PRINTED COVERAGE BY AREA
SCALE: 15X

4219039/A 06/2018

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

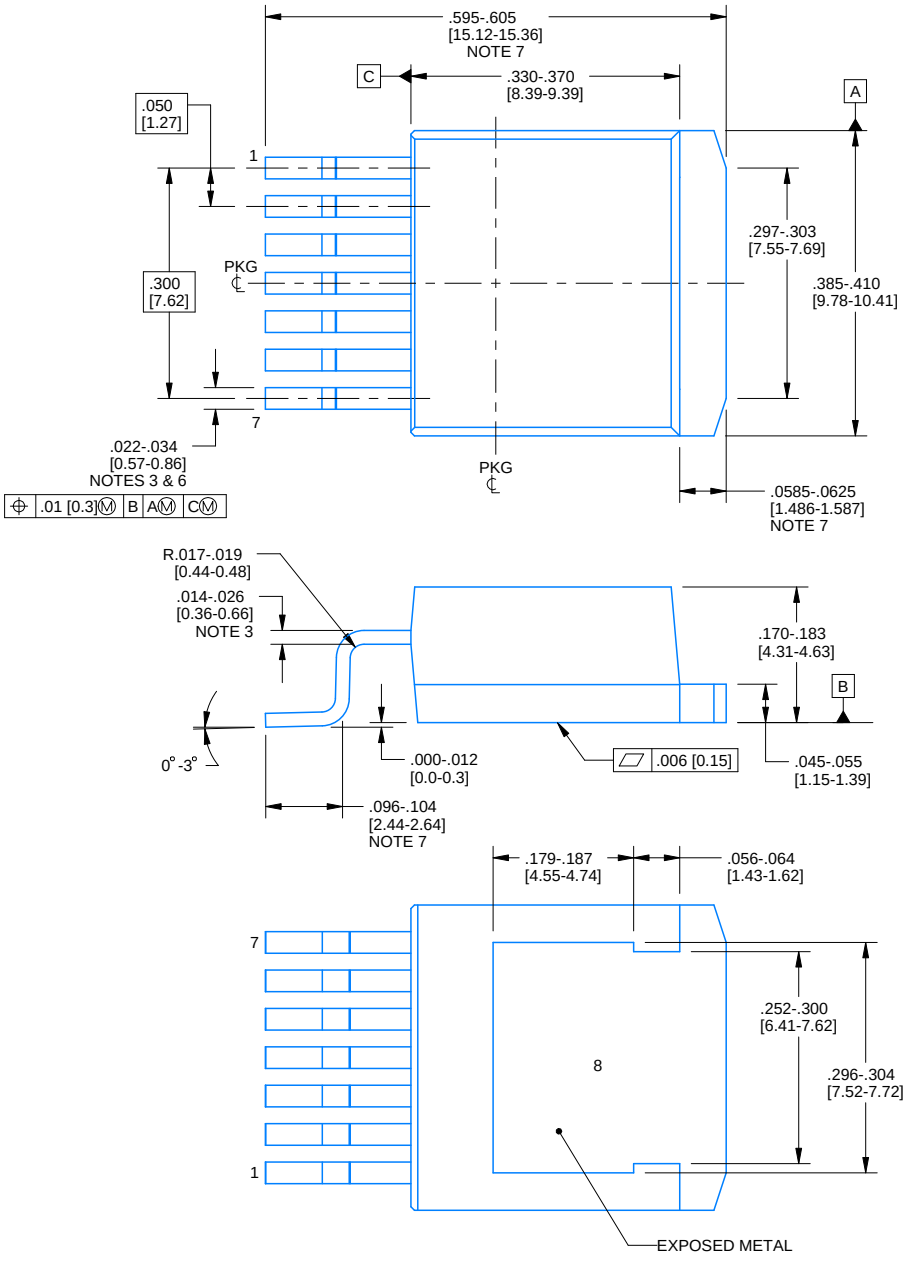
KTW0007A



PACKAGE OUTLINE

TO-263 - 5 mm max height

TRANSISTOR OUTLINE



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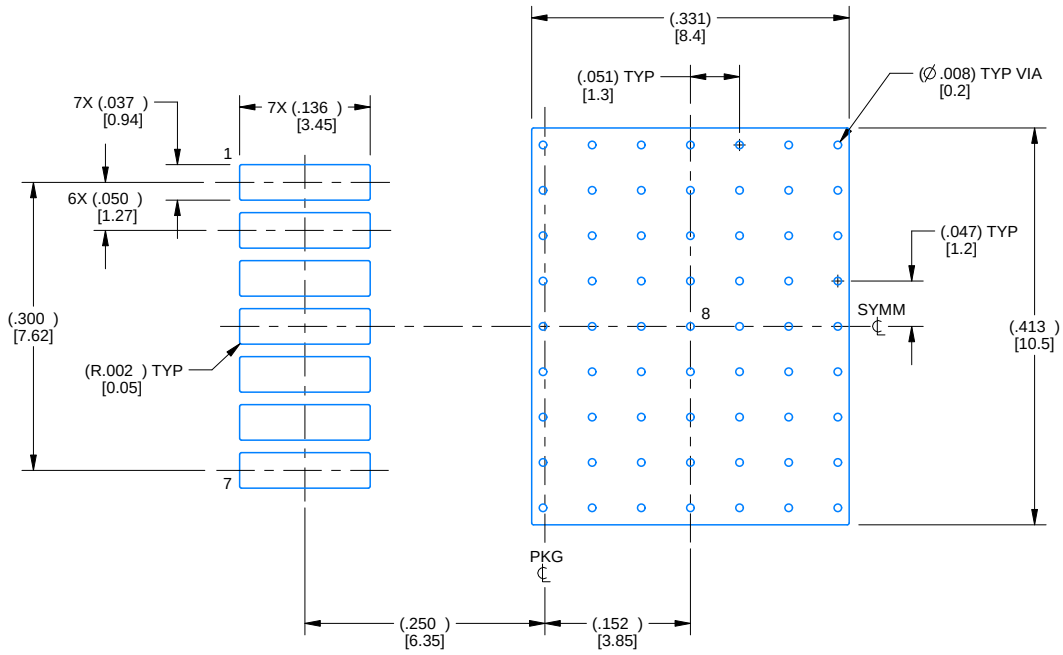
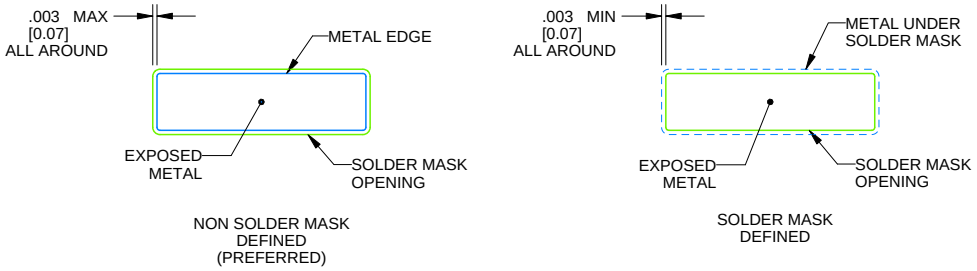
NOTES:

1. All linear dimensions are in inches [millimeters]. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Lead width and height dimensions apply to the plated lead.
4. Leads are not allowed above the Datum B.
5. Stand–off height is measured from lead tip with reference to Datum B.
6. Lead width dimension does not include dambar protrusion. Allowable dambar protrusion shall not cause the lead width to exceed the maximum bdimension by more than 0.003”.
7. Falls within JEDEC MO–169 with the exception of the dimensions indicated.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 5X



SOLDER MASK DETAILS

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NOTES: (continued)

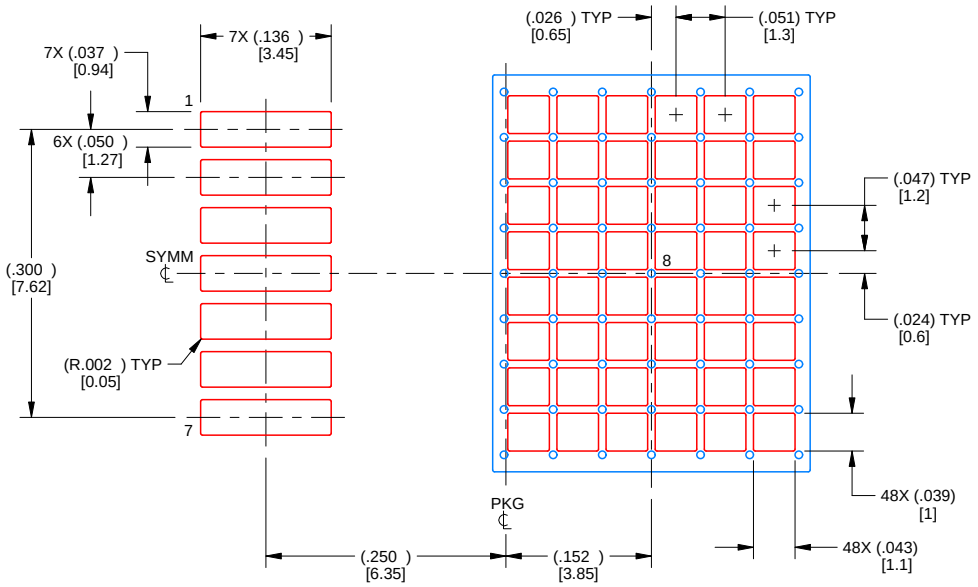
8. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature numbers SLMA002(www.ti.com/lit/slm002) and SLMA004 (www.ti.com/lit/slma004).
9. Vias are optional depending on application, refer to device data sheet. It is recommended that vias under paste be filled, plugged or tented.

EXAMPLE STENCIL DESIGN

KTW0007A

TO-263 - 5 mm max height

TRANSISTOR OUTLINE



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 5X

PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
PAD 8: 60%

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NOTES: (continued)

10. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
11. Board assembly site may have different recommendations for stencil design.

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