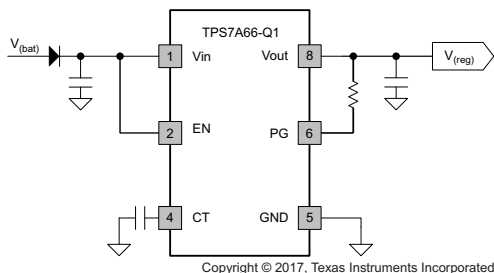


TPS7A6x-Q1 High-Voltage Ultralow- $I_{(q)}$ Low-Dropout Regulator

1 Features

- Qualified for Automotive Applications
- AEC-Q100 Test Guidance With the Following:
 - Device Temperature Grade 1
 - Device Temperature Grade 0 (TPS7A6650EDGNRQ1 Only)
 - Device HBM ESD Classification Level H2
 - Device CDM ESD Classification Level C4
- Device Junction Temperature Range: -40°C to $+150^{\circ}\text{C}$
- 4-V to 40-V Wide V_{in} Input Voltage Range With up to 45-V Transient
- Output Current: 150 mA
- Low Quiescent Current, $I_{(q)}$:
 - 2 μA When EN = Low (Shutdown Mode)
 - 12 μA Typical at Light Loads
- Low ESR Ceramic Output Stability Capacitor (2.2 μF –100 μF)
- 300-mV Dropout Voltage at 150 mA (Typical, $V_{(in)} = 4\text{ V}$)
- Fixed (3.3-V and 5-V) and Adjustable (1.5-V to 5-V) Output Voltages (Adjustable for TPS7A66-Q1 Only)
- Low Input Voltage Tracking
- Integrated Power-On Reset:
 - Programmable Reset-Pulse Delay
 - Open-Drain Reset Output
- Integrated Fault Protection:
 - Thermal Shutdown
 - Short-Circuit Protection
- Input Voltage Sense Comparator (TPS7A69-Q1 Only)
- Packages:
 - 8-Pin SOIC-D for TPS7A69-Q1
 - 8-Pin HVSSOP-DGN for TPS7A6601-Q1

Hardware-Enable Option



2 Applications

- Infotainment Systems With Sleep Mode
- Body Control Modules
- Always-On Battery Applications:
 - Gateway Applications
 - Remote Keyless Entry Systems
 - Immobilizers

3 Description

The TPS7A66-Q1 and TPS7A69-Q1 are low-dropout linear regulators designed for up to 40-V V_{in} operations. With only 12- μA quiescent current at no load, they are quite suitable for standby microprocessor control-unit systems, especially in automotive applications.

The devices feature integrated short-circuit and overcurrent protection. The devices implement reset delay on power up to indicate the output voltage is stable and in regulation. One can program the delay with an external capacitor. A low-voltage tracking feature allows for a smaller input capacitor and can possibly eliminate the need of using a boost converter during cold-crank conditions.

The devices operate in the -40°C to 125°C temperature range. The TPS7A6650EDGNRQ1 device is qualified to AEC-Q100 grade 0, operating in the -40°C to 150°C temperature range. These features suit the devices well for power supplies in various automotive applications.

Device Information⁽¹⁾

PART NUMBER	PACKAGE	BODY SIZE (NOM)
TPS7A66-Q1	HVSSOP (8)	3.00 mm × 3.00 mm
TPS7A69-Q1	SOIC (8)	4.90 mm × 3.91 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Input-Voltage-Sensing Option

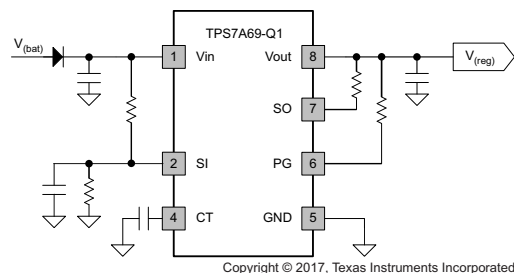


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4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision E (November 2014) to Revision F	Page
• Changed <i>AEC-Q100 Test Guidance</i> Features bullet and deleted temperature range from first two AEC-Q100 sub-bullets	1
• Changed $V_{(vin)}$ to V_{IN} , V_{in} to V_{IN} , $V_{(vout)}$ to V_{OUT} , V_{out} to V_{OUT} , and $V_{(CT)}$ to V_{CT} throughout document.....	1
• Added <i>Device Junction Temperature Range</i> Features bullet	1
• Changed associated devices to TPS7A66-Q1 and TPS7A69-Q1 throughout document	1
• Changed MSOP to HVSSOP throughout document	1
• Changed CT, EN, FB/DNC, PG, SO, and VOUT descriptions in <i>Pin Functions</i> table	4
• Changed pin names FB/NU to FB/DNC, V_{in} to V_{IN} , and V_{out} to V_{OUT} in <i>Pin Configuration and Functions</i> section	4
• Changed SI parameter name description and added maximum specification to SI and FB, SO, PG rows in <i>Absolute Maximum Ratings</i> table	4
• Added parameter names to CT and FB, SO, PG rows in <i>Absolute Maximum Ratings</i> table	4
• Added <i>lockout</i> to <i>Undervoltage lockout detection</i> parameter name.....	6
• Added <i>up to</i> to I_{LKG} test conditions	6
• Added V_{OUT} to unit of $V_{(TH-POR)}$ and $V_{(Thres)}$	6
• Added CT to $V_{(th)}$ parameter name.....	6
• Added header for first section of <i>Switching Characteristics</i> table	7
• Added <i>UVLO Thresholds vs Temperature</i> and <i>Enable Thresholds vs Temperature</i> figures.....	8
• Added <i>CT Charging Current</i> ($V_{CT} = 0$) and <i>CT Charging Threshold</i> figures.....	9
• Changed <i>Device Functional Modes</i> section	17

Changes from Revision D (October 2014) to Revision E	Page
• Corrected voltage unit in Handling Ratings table from V to kV	5

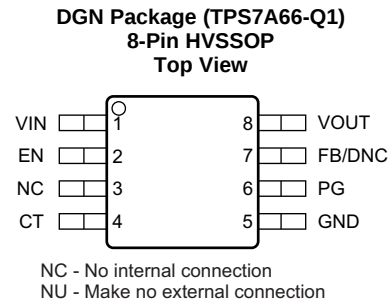
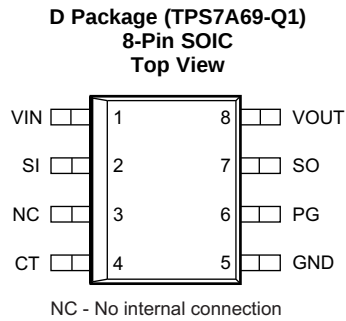
Changes from Revision C (December 2013) to Revision D	Page
• Changed CDM ESC classification level	1
• Changed FB/NC pin to FB/NU in Pin Functions table Added NC and NU notes to pinout drawings	4
• Removed ESD and T_{stg} specifications from the Absolute Maximum Ratings table	4
• Added ESD Ratings table	5
• Numerous changes throughout the Electrical Characteristics table	6
• Added Switching Characteristics table	7
• Moved an oscilloscope trace to the Applications Information section	10
• Changed de-glitch time in Power-On Reset (PG) section	13
• Changed reset delay timer default delay to 290 μs from 150 μs	13
• Changed voltage at which Power-on reset initializes to 91.6% of $V_{(Vout)}$	13
• Changed selectable output voltage range and calculation for FB resistor divider	15

Changes from Revision B (August 2013) to Revision C	Page
• Corrected part number in the Description section by adding -Q1	1
• Changed Operating ambient temperature to Operating junction temperature	4
• Added PSRR graph to Typical Characteristics.....	10
• Deleted a paragraph from the Thermal Protection section.....	16

Changes from Revision A (March 2013) to Revision B	Page
• Added two conditions to $V_{dropout}$ in the Electrical Characteristics table	6

Changes from Original (December 2012) to Revision A	Page
• Deleted the ORDERING INFORMATION table.....	4
• Changed From: T_A Operating ambient temperature range –40 to 125°C To: T_J Operating ambient temperature range –40 to 150°C	4

5 Pin Configuration and Functions



Pin Functions

PIN NAME	PIN NO.		TYPE	DESCRIPTION
	SOIC-D	HVSSOP-DGN		
CT	4	4	O	Reset-pulse delay adjustment. Connecting a capacitor from this pin to GND changes the PG reset delay; see the Reset Delay Timer (CT) section for more details.
EN	—	2	I	Enable pin. The device enters the standby state when the enable pin becomes lower than the enable threshold.
FB/DNC	—	7	I	Feedback pin when using external resistor divider or DNC pin when using the device with a fixed output voltage.
GND	5	5	G	Ground reference
NC	3	3	—	Not-connected pin
PG	6	6	O	Power good. This open-drain pin must connect to VOUT via an external resistor. V_{PG} is logic level high when V_{OUT} is above the power-on-reset threshold.
SI	2		I	Sense input pin to supervise input voltage. Connect via an external voltage divider to VIN and GND.
SO	7		O	Sense output. This open-drain pin must connect to VOUT via an external resistor. V_{SO} is logic level low when V_{SI} falls below the sense-low threshold.
VIN	1	1	P	Input power-supply voltage
VOUT	8	8	O	Regulated output voltage
Thermal pad	Pad	—	—	Thermal pad for HVSSOP-DGN package

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted) ⁽¹⁾

		MIN	MAX	UNIT
VIN, EN	Unregulated input ⁽²⁾⁽³⁾	−0.3	45	V
VOUT	Regulated output	−0.3	7	V
SI	Sense input ⁽²⁾	−0.3	V_{IN}	V
CT	Reset delay input	−0.3	25	V
FB, SO, PG	Feedback, sense output, power good	−0.3	V_{OUT}	V
T_J	Operating junction temperature range	−40	150	°C
T_{stg}	Storage temperature	−65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

(2) All voltage values are with respect to GND

(3) Absolute maximum voltage, withstand 45 V for 200 ms

6.2 ESD Ratings

			MIN	MAX	UNIT
$V_{(ESD)}$ Electrostatic discharge	Human body model (HBM), per AEC Q100-002 ⁽¹⁾		0	4	kV
	Charged device model (CDM), per AEC Q100-011	Corner pins (1, 4, 5, and 8)	0	1	
		Other pins	0	1	

(1) AEC Q100-002 indicates HBM stressing is done in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	TYP	MAX	UNIT
V_{IN}	Unregulated input	4		40	V
V_{EN}, V_{SI}	High voltage (I/O)	0		40	V
V_{CT}	CT pin voltage	0		20	V
V_{OUT}	Regulated output	1.5		5.5	V
V_{PG}, V_{SO}, V_{FB}	Low voltage (I/O)	0		5.5	V
C_{IN}	Input capacitor ⁽¹⁾		10		μ F
C_{OUT}	Output capacitor ⁽¹⁾	2.2		100	μ F
T_J	Operating junction temperature	–40		150	°C

(1) Values on this row refer to the nominal value of the capacitor.

6.4 Thermal Information

THERMAL METRIC ⁽¹⁾		TPS7A66-Q1	TPS7A69-Q1	UNIT
		HVSSOP (8 PINS)	SOIC (8 PINS)	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	63.4	113.2	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	53.0	59.6	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	37.4	59.57	°C/W
ψ_{JT}	Junction-to-top characterization parameter	3.7	12.8	°C/W
ψ_{JB}	Junction-to-board characterization parameter	37.1	52.9	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	13.5	NA	°C/W

(1) For more information about traditional and new thermal metrics, see the [Semiconductor and IC Package Thermal Metrics](#) application report.

6.5 Electrical Characteristics

 $V_{IN} = 14\text{ V}$, $1\text{ m}\Omega < \text{ESR} < 2\text{ }\Omega$, $T_J = -40^\circ\text{C}$ to 150°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
SUPPLY VOLTAGE AND CURRENT (VIN)						
VIN	Input voltage	Fixed 5-V output, IO = 1 mA	5.5		40	V
		Fixed 3.3-V output, IO = 1 mA	4		40	
I(q)	Quiescent current	VIN = 5.5 V to 40 V, EN = ON, IO = 0.2 mA		12	20	μA
ISleep	Input sleep current	No load current and EN = OFF			4	μA
I(EN)	EN pin current	V(EN) = 40 V			1	μA
V(bg)	Band gap	Reference voltage for FB	1.199	1.223	1.247	V
V(VinUVLO)	Undervoltage lockout detection	Ramp VIN down until output turns OFF			2.6	V
V(UVLOhys)	Undervoltage hysteresis			1		V
ENABLE INPUT (EN)						
VIL	Logic input low level		0		0.4	V
VIH	Logic input high level		1.7			V
REGULATED OUTPUT (VOUT)						
VOUT	Regulated output	IO = 1 mA, TJ = 25°C	-1%		1%	
		VIN = 6 V to 40 V, IO = 1 mA to 150 mA, fixed 5-V version	-2%		2%	
		VIN = 4 V to 40 V, IO = 1 mA to 150 mA, fixed 3.3-V version	-2%		2%	
		VIN = VOUT + 0.45 V and Vin ≥ 4 V, IO = 1 mA to 150 mA, adjustable version ⁽¹⁾	-2%		2%	
V(line-reg)	Line regulation	VIN = 5.5 V to 40 V, IO = 50 mA			5	mV
V(load-reg)	Load regulation	IO = 1 mA to 150 mA			20	mV
V(dropout)	Dropout voltage	V(dropout) = VIN – VOUT, IOUT = 80 mA		180	240	mV
		VIN – VOUT, IOUT = 150 mA		300	450	
		VIN = 3 V, V(dropout) = VIN – VOUT, IO = 5 mA	12	27.5	58	
		VIN = 3 V, V(dropout) =VIN –VOUT, IO = 30 mA	44	80	145	
IO	Output current	VOUT in regulation	0		150	mA
I(lreg-CL)	Output current limit	VOUT short to ground		500	800	mA
PSRR	Power supply ripple rejection ⁽²⁾	VIN = 12 V, IL = 10 mA, output capacitance = 2.2 μF				dB
		Frequency = 100 Hz		60		
		Frequency = 100 kHz		40		
VOLTAGE SENSING PRE-WARNING						
Vl(S-th)	Sense low threshold	V(SI) decreasing	1.089	1.123	1.157	V
Vl(S-th,hys)	Sense threshold hysteresis		50	100	150	mV
VOL(S)	Sense output low voltage	(V(SI) ≤ 1.06 V, VIN ≥ 4 V, R(SO) = 10 kΩ to VOUT			0.4	V
Ioh(S)	Sense output leakage	(V(SO) = 5 V, V(SI) ≥ 1.5 V)			1	μA
Il(S)	Sense input current		-1	0.1	1	μA
RESET (PG)						
VOL	Reset output, low voltage	IOL = 0.5 mA			0.4	V
Iikg	Leakage current	Reset pulled up to VOUT through a 10-kΩ resistor			1	μA
V(TH-POR)	Power-on-reset threshold	VOUT increasing	89.6	91.6	93.6	% of VOUT
V(Thres)	Hysteresis			2		% of VOUT
RESET DELAY (CT)						
I(Chg)	Delay-capacitor charging current	VCT = 0 V		1.4		μA
V(th)	CT threshold to release PG high			1		V
OPERATING TEMPERATURE RANGE						
TJ	Junction temperature		-40		150	°C
T(shutdown)	Junction shutdown temperature			175		°C
T(hyst)	Hysteresis of thermal shutdown			20		°C

(1) Adjustable version with precision external feedback resistor with tolerance of less than $\pm 1\%$.

(2) Design information – not tested.

6.6 Switching Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
TIMING FOR SENSE INPUT AND OUTPUT (SI, SO)						
$t_{(SDeg\text{glitch},\text{rise})}$	SI or SO rising deglitch time		50		260	μs
$t_{(SDeg\text{glitch},\text{drop})}$	SI or SO falling deglitch time		30		240	μs
TIMING FOR RESET (PG)						
$t_{(POR)}$	Power-on-reset delay	Where C = delay capacitor value; capacitance C = 100 nF ⁽¹⁾	50	100	180	ms
$t_{(POR\text{-fixed})}$		No capacitor on pin	100	290	650	μs
$t_{(Deg\text{glitch})}$	Reset deglitch time		20	250		μs

- (1) This information only is not tested in production and equation basis is $(C \times 1) / 1 \times 10^{-6} = t_d$ (delay time).
Where C = Delay capacitor value. Capacitance C range = 100 pF to 100 nF.

6.7 Typical Characteristics

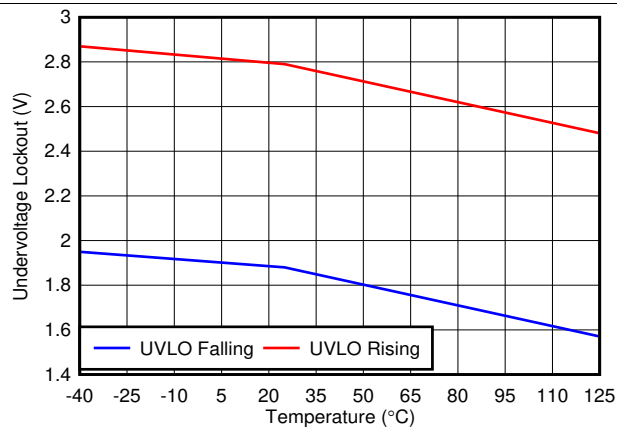


Figure 1. UVLO Thresholds vs Temperature

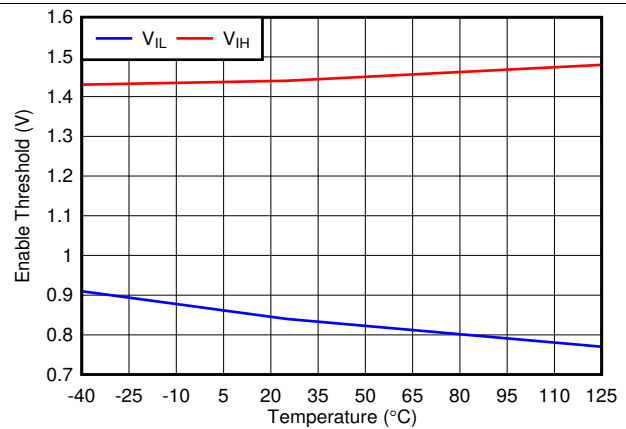


Figure 2. Enable Thresholds vs Temperature

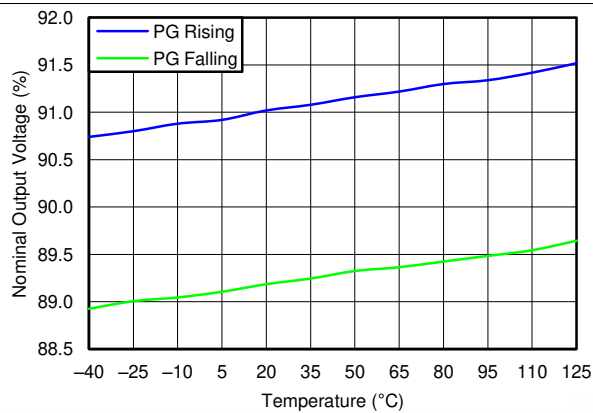


Figure 3. Power-Good Threshold Voltage vs Temperature
($V_{IN} = 14\text{ V}$, No Load)

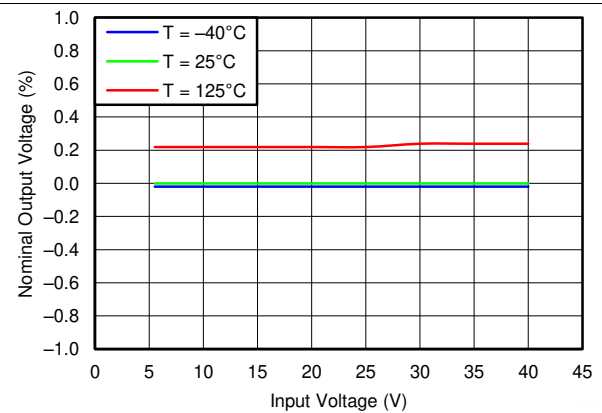


Figure 4. Line Regulation ($V_{IN} = 14\text{ V}$, $I_L = 1\text{ mA}$)

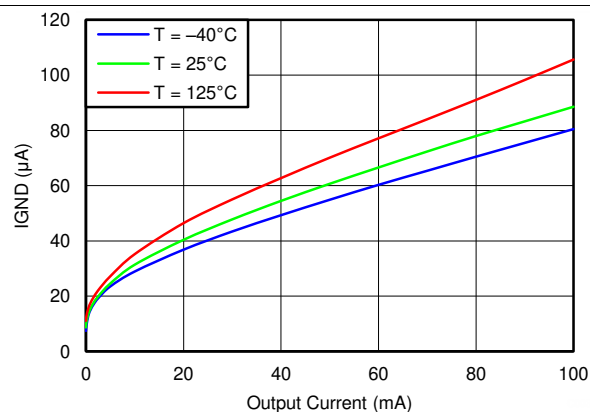


Figure 5. Ground Current vs Output Current ($V_{IN} = 14\text{ V}$)

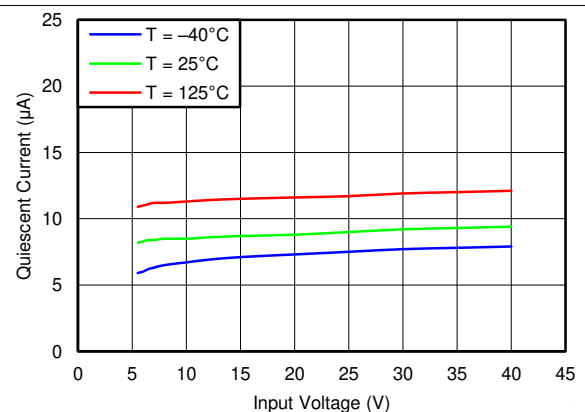


Figure 6. Quiescent Current vs Input Voltage ($I_L = 0$)

Typical Characteristics (continued)

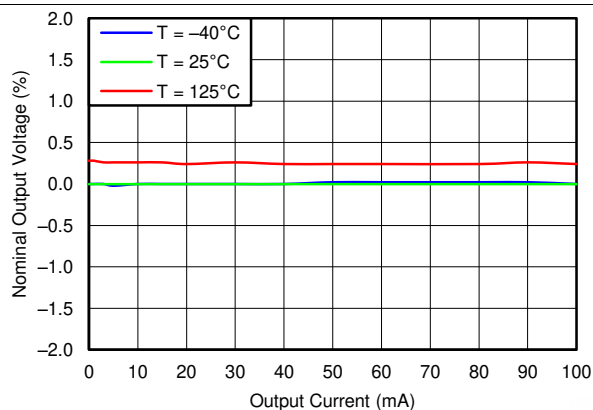


Figure 7. Load Regulation ($V_{IN} = 14\text{ V}$)

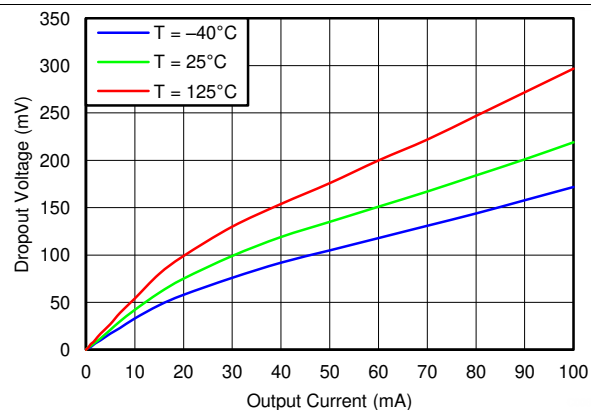


Figure 8. Dropout Voltage vs Output Current ($V_{IN} = 4\text{ V}$)

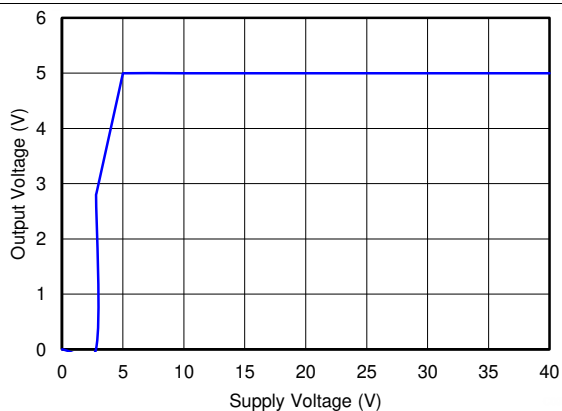


Figure 9. Output Voltage vs Supply Voltage
(Fixed 5-V Version, $I_L = 0$)

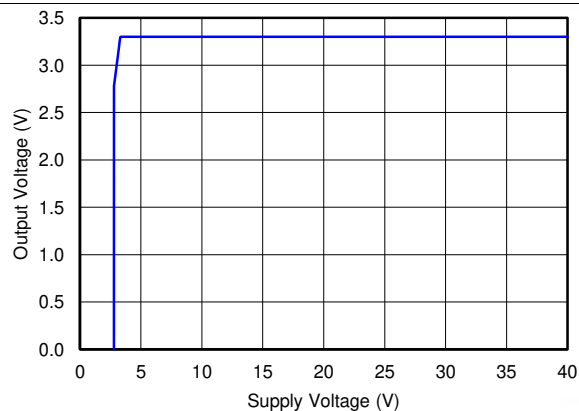


Figure 10. Output Voltage vs Supply Voltage
(Fixed 3.3-V Version, $I_L = 0$)

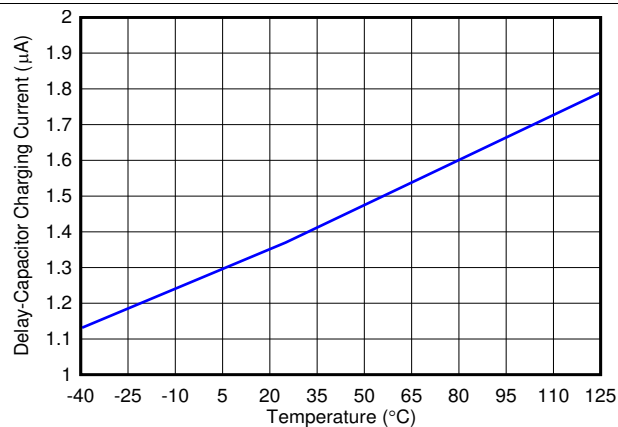


Figure 11. CT Charging Current ($V_{CT} = 0$)

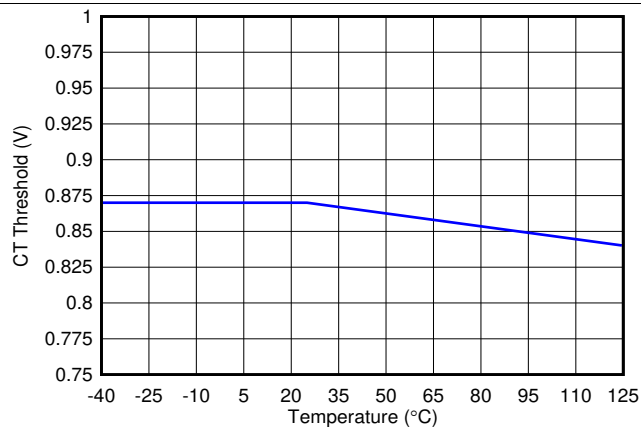


Figure 12. CT Charging Threshold

Typical Characteristics (continued)

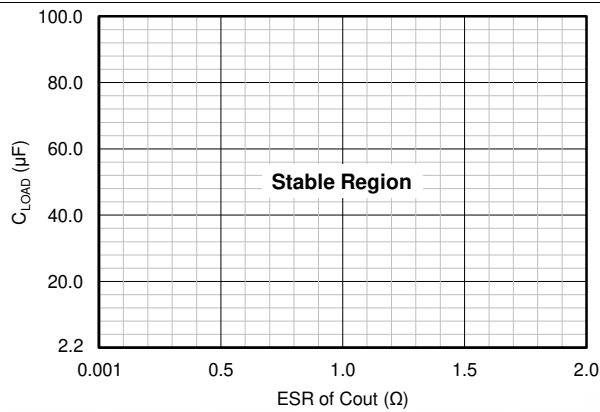


Figure 13. Load Capacitance vs ESR Stability

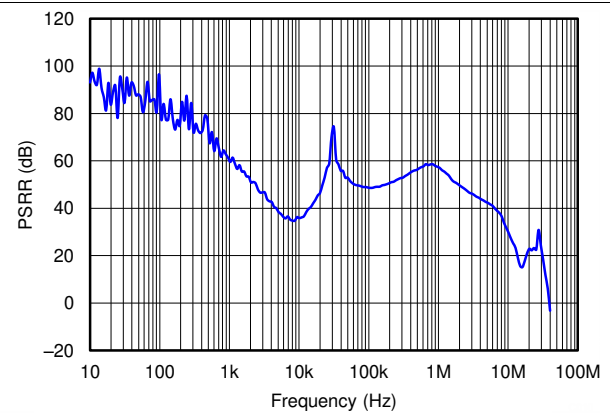
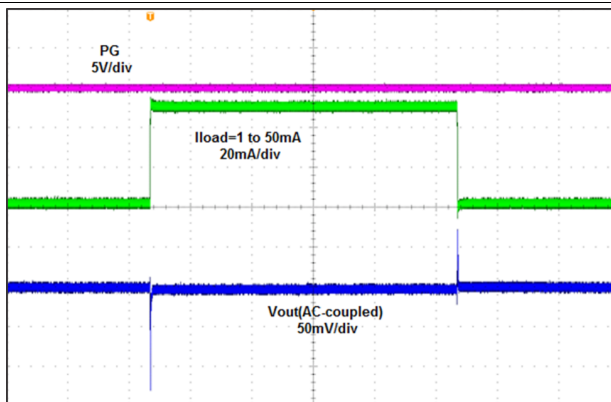
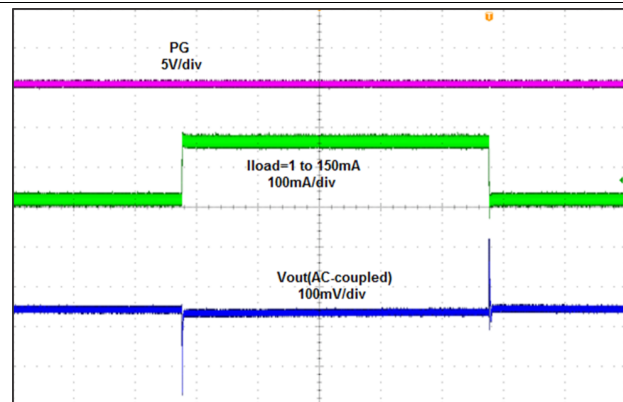


Figure 14. Power-Supply Rejection Ratio vs Frequency



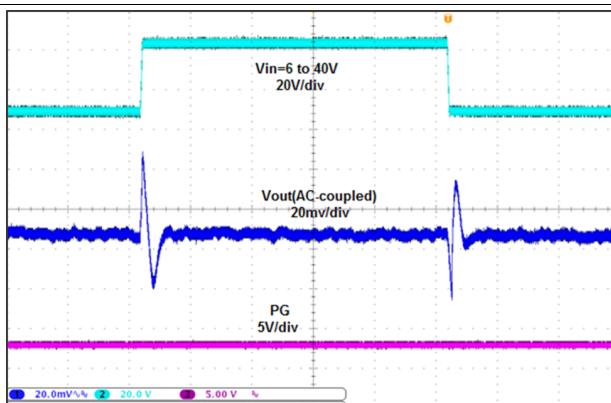
All oscilloscope waveforms were taken at room temperature.

Figure 15. Load Transient Response, 10 ms/div



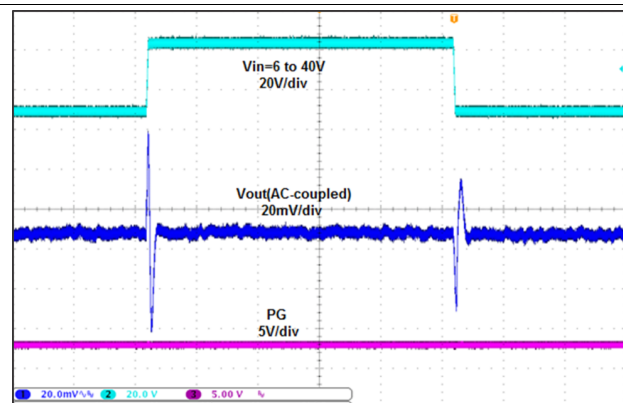
All oscilloscope waveforms were taken at room temperature.

Figure 16. Load Transient Response, 10 ms/div



All oscilloscope waveforms were taken at room temperature.

Figure 17. Line Transient Response, $I_L = 1 \text{ mA}$, $1 \text{ V}/\mu\text{s}$



All oscilloscope waveforms were taken at room temperature.

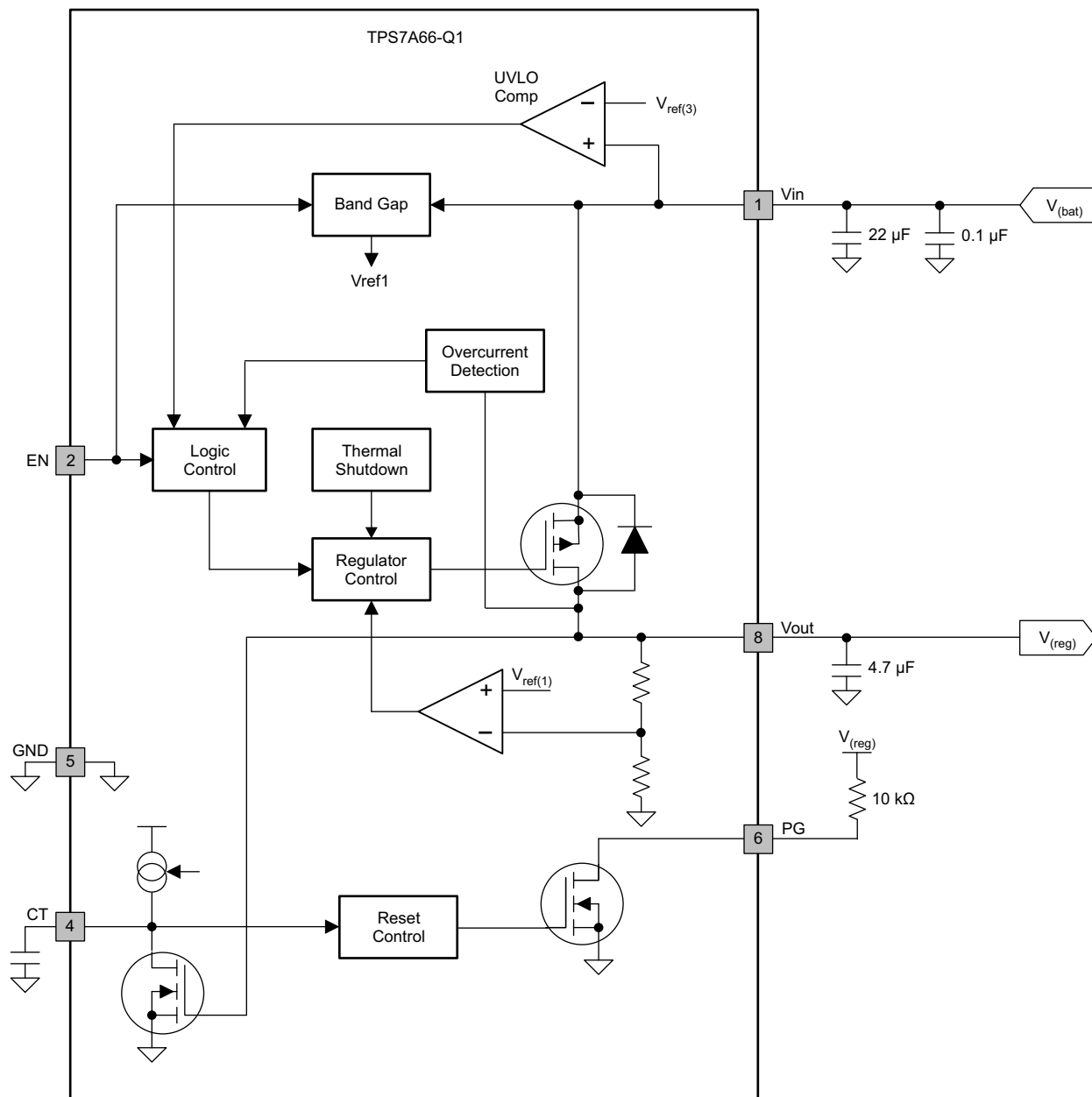
Figure 18. Line Transient Response, $I_L = 10 \text{ mA}$, $1 \text{ V}/\mu\text{s}$

7 Detailed Description

7.1 Overview

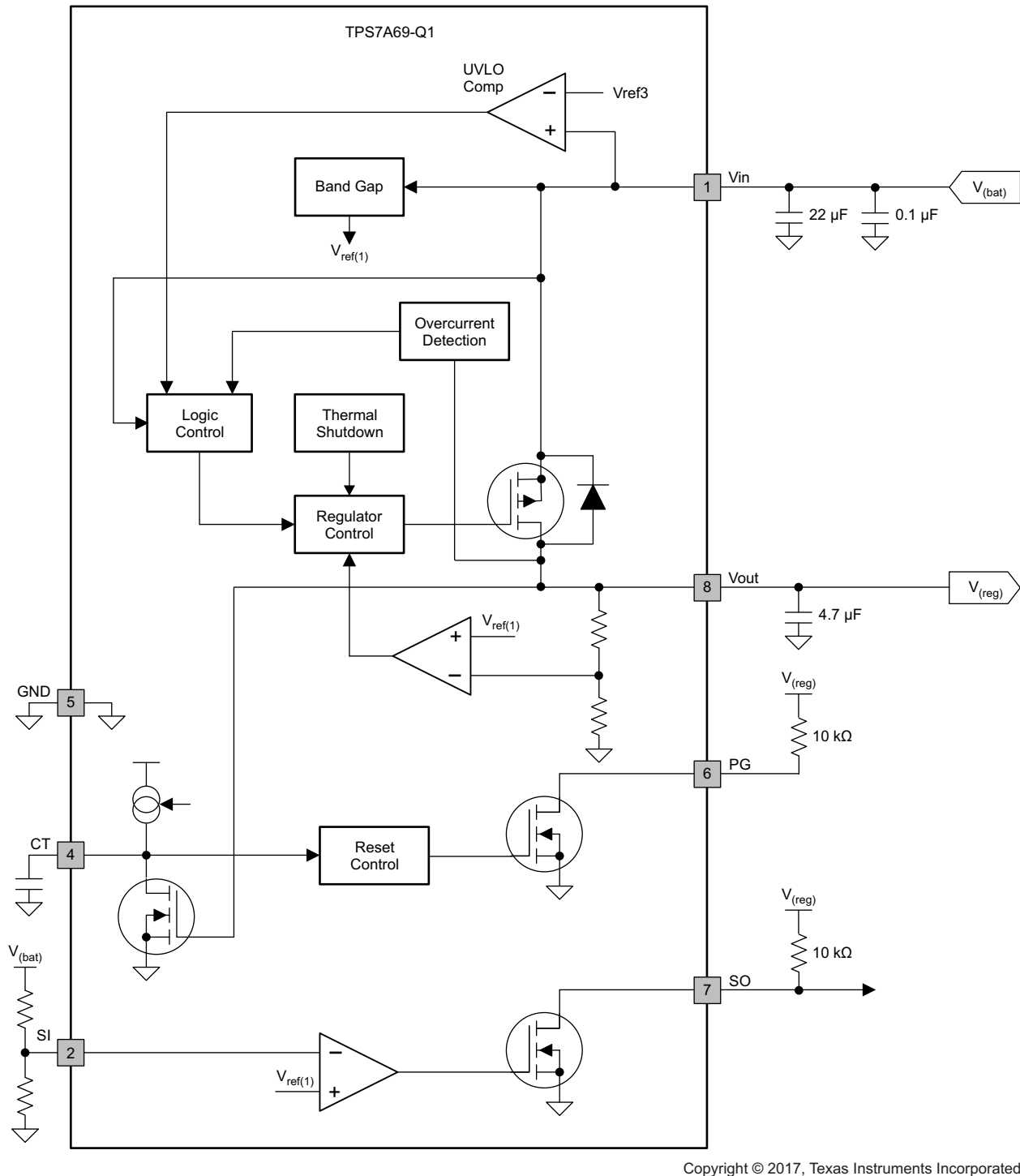
This device is a combination of a low-dropout linear regulator with reset function. The power-on reset initializes once the V_{OUT} output exceeds 91.6% of the target value. The power-on-reset delay is a function of the value set by an external capacitor on the CT pin before releasing the PG pin high.

7.2 Functional Block Diagrams



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Figure 19. TPS7A66-Q1 Functional Block Diagram

Functional Block Diagrams (continued)


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Figure 20. TPS7A69-Q1 Functional Block Diagram

7.3 Feature Description

7.3.1 Enable (EN)

This is a high-voltage-tolerant pin; high input activates the device and turns the regulator ON. One can connect this input to the VIN pin for self-bias applications.

7.3.2 Regulated Output (V_{OUT})

This is the regulated output based on the required voltage. The output has current limitation. During initial power up, the regulator has a soft start incorporated to control initial current through the pass element and the output capacitor.

In the event the regulator drops out of regulation, the output tracks the input minus a drop based on the load current. When the input voltage drops below the UVLO threshold, the regulator shuts down until the input voltage recovers above the minimum start-up level.

7.3.3 Power-On Reset (PG)

This is an output with an external pullup resistor to the regulated supply. The output remains low until the regulated V_{OUT} has exceeded approximately 90% of the set value and the power-on-reset delay has expired. The on-chip oscillator presets the delay. The regulated output falling below the 90% level asserts this output low after a short de-glitch time of approximately 250 μs (typical).

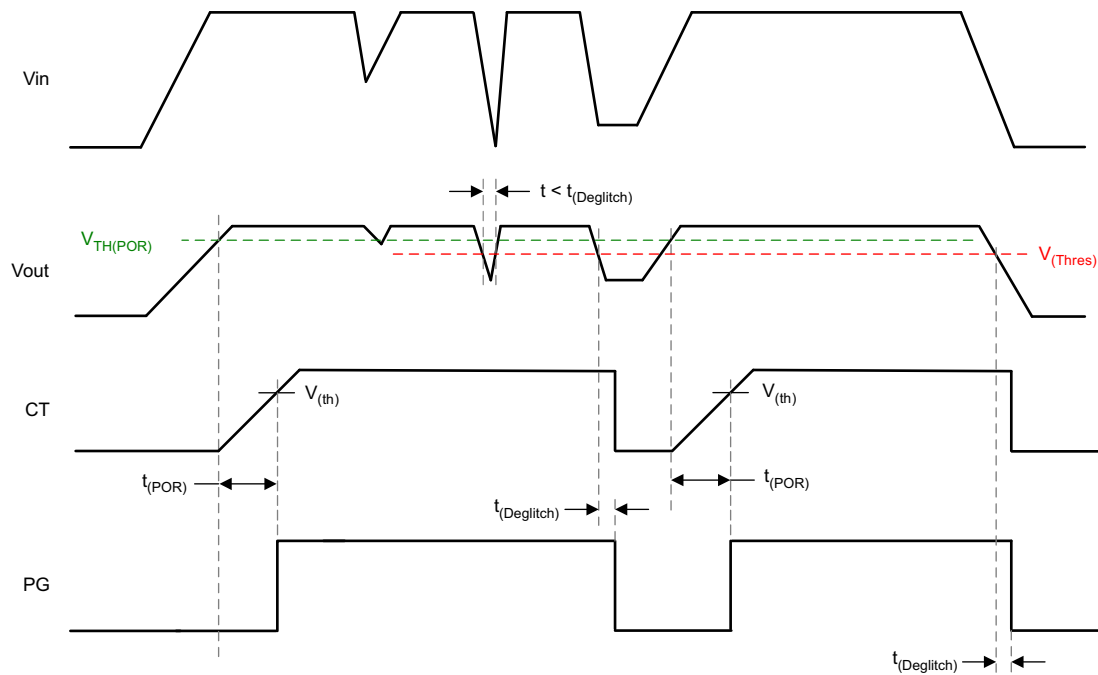
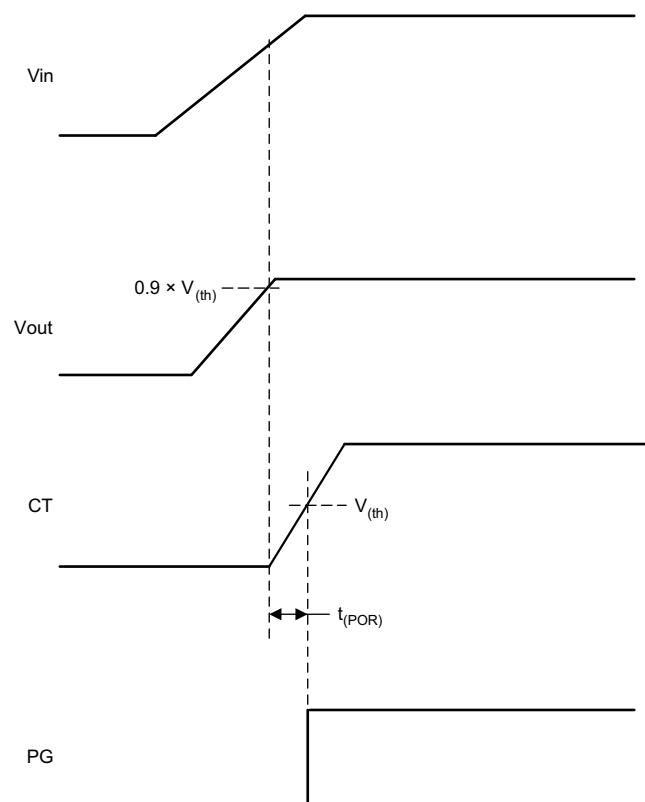
7.3.4 Reset Delay Timer (CT)

An external capacitor on this pin sets the timer delay before the reset pin is asserted high. The constant output current charges an external capacitor until the voltage exceeds a threshold to trip an internal comparator. If this pin is open, the default delay time is 290 μs (typ). After releasing the PG pin high, the capacitor on this pin discharges, thus allowing the capacitor to charge from approximately 0.2 V for the next power-on-reset delay-timer function.

An external capacitor, CT, defines the reset-pulse delay time, t_(POR), with the charge time of:

$$t_{(POR)} = \frac{C_{(CT)} \times 1\text{ V}}{1\text{ }\mu\text{A}} \quad (1)$$

The power-on reset initializes once the output V_{OUT} exceeds 91.6% of the programmed value. The power-on-reset delay is a function of the value set by an external capacitor on the CT pin before the releasing of the PG pin high.

Feature Description (continued)

Figure 21. Conditions for Activation of Reset

Figure 22. External Programmable Reset Delay

Feature Description (continued)

7.3.5 Sense Comparator (SI and SO for TPS7A69-Q1)

The sense comparator compares the input signal with an internal voltage reference of 1.223 V for rising and 1.123 V for falling threshold. The use of an external voltage divider makes this comparator very flexible in the application.

The device can supervise the input voltage either before or after the protection diode and give additional information to the microprocessor, like low-voltage warnings.

The regulator operates in low-power mode when the output load is below 2 mA (typical, 1-mA to 10-mA range). In this mode, the regulator output tolerance is approximately $V_{OUT} \pm 1\%$.

7.3.6 Adjustable Output Voltage (FB for TPS7A6601-Q1)

One can select an output voltage between 1.5 V and 5 V by using an external resistor divider. Calculate the output voltage using the following equation, where $V_{(FB)} = 1.223$ V. The recommendation for R1 and R2 is that both be less than 100 k Ω .

$$V_{(Vout)} = V_{(FB)} \times \left(1 + \frac{R1}{R2} \right) \quad (2)$$

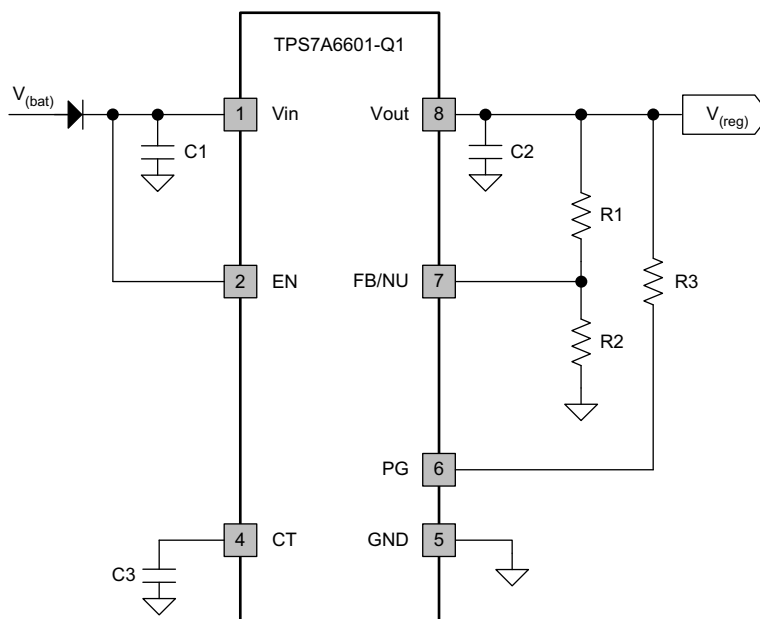


Figure 23. External Feedback Resistor Divider

7.3.7 Undervoltage Shutdown

There is an internally fixed undervoltage shutdown threshold. Undervoltage shutdown activates when the input voltage on VIN drops below $V_{(VinUVLO)}$. This ensures the regulator is not latched into an unknown state during low input supply voltage. If the input voltage has a negative transient which drops below the UVLO threshold and recovers, the regulator shuts down and powers up with a normal power-up sequence once the input voltage is above the required levels.

7.3.8 Low-Voltage Tracking

At low input voltages, the regulator drops out of regulation and the output voltage tracks input minus a voltage based on the load current (I_O) and switch resistance ($R_{(SW)}$). This allows for a smaller input capacitor and can possibly eliminate the need of using a boost convertor during cold-crank conditions.

Feature Description (continued)

7.3.9 Thermal Shutdown

These devices incorporate a thermal shutdown (TSD) circuit as a protection from overheating. For continuous normal operation, the junction temperature should not exceed the TSD trip point. If the junction temperature exceeds the TSD trip point, the output turns off. When the junction temperature falls below the TSD trip point, the output turns on again.

Thermal protection disables the output when the junction temperature rises to approximately 170°C, allowing the device to cool. Cooling of the junction temperature to approximately 150°C enables the output circuitry. Depending on power dissipation, thermal resistance, and ambient temperature, the thermal protection circuit may cycle on and off. This cycling limits the dissipation of the regulator, protecting it from damage as a result of overheating.

The purpose of the design of the internal protection circuitry of the TPS7A66-Q1, TPS7A69-Q1 is for protection against overload conditions, not as a replacement for proper heat-sinking. Continuously running the TPS7A66-Q1 or TPS7A69-Q1 into thermal shutdown degrades device reliability.

7.4 Device Functional Modes

[Table 1](#) provides a quick comparison between the regulation, disabled, and current limit modes of operation.

Table 1. Device Functional Modes Comparison

OPERATING MODE	PARAMETER			
	V_{IN}	$EN^{(1)}$	I_O	T_J
Regulation ⁽²⁾	$V_{IN} > V_{OUT(nom)} + V_{(dropout)}$	$V_{EN} > V_{IH}$	$I_O < I_{(Ireg-CL)}$	$T_J \leq T_{J(maximum)}$
Disabled ⁽³⁾	$V_{IN} < V_{(VinUVLO)}$	$V_{EN} < V_{IL}$	—	$T_J > T_{sd}$
Current limit operation	—	—	$I_O \geq I_{(Ireg-CL)}$	—

(1) EN is only required for the TPS7A66-Q1 devices.

(2) All table conditions must be met.

(3) The device is disabled when any condition is met.

7.4.1 Regulation

The device regulates the output to the nominal output voltage when all the conditions in [Table 1](#) are met.

7.4.2 Disabled

When disabled, the pass device is turned off and the internal circuits are shut down.

7.4.3 Operation With $V_{(VinUVLO)} < V_{IN} < V_{IN(min)}$

When the input voltage is ramping up the device typically turns on when the input voltage is greater than $V_{(VinUVLO)}$ plus $V_{(UVLOhys)}$. When the input voltage is ramping down the device is specified to turn off when the input voltage becomes less than or equal to $V_{(VinUVLO)}$.

8 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

The TPS7A66-Q1 and TPS7A69-Q1 devices are 150-mA low-dropout linear regulators designed for up to 40-V V_{IN} operation with only 12 μ A quiescent current at no load. One can use the Pspice transient model, which is downloadable from the product folder (see [Related Links](#)), for evaluating the base function of the devices. In addition, there are specific EVMs designed for these devices. Both the EVM and its user guide are available on the product folder as well.

8.2 Typical Applications

[Figure 24](#) and [Figure 26](#) depict typical application circuits for the TPS7A66-Q1 and TPS7A69-Q1, respectively. One may use different values of external components, depending on the end application. An application may require a larger output capacitor during fast load steps in order to prevent reset from occurring. TI recommends a low-ESR ceramic capacitor with dielectric of type X5R or X7R.

8.2.1 TPS7A66-Q1 Typical Application

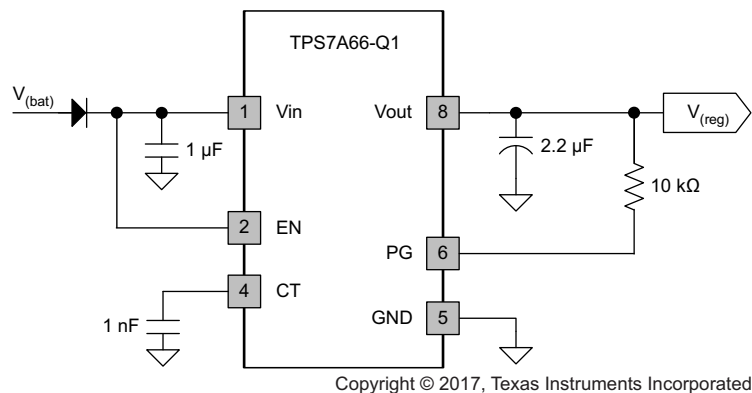


Figure 24. Typical Application Schematic for TPS7A66-Q1

8.2.1.1 Design Requirements

For this design example, use the parameters listed in [Table 2](#) as the design parameters.

Table 2. Design Parameters

DESIGN PARAMETER	EXAMPLE VALUE
Input voltage range	4 V to 40 V
Output voltage	3.3 V
Output current rating	150 mA
Output capacitor range	2.2 μ F to 100 μ F
Output capacitor ESR range	1 m Ω to 2 Ω
CT capacitor range	100 pF to 100 nF

8.2.1.2 Detailed Design Procedure

To begin the design process, determine the following:

- Input voltage range
- Output voltage
- Output current rating
- Input capacitor
- Output capacitor
- Power-up-reset delay time

8.2.1.2.1 Input Capacitor

The device requires an input decoupling capacitor, the value of which depends on the application. The typical recommended value for the decoupling capacitor is 10 μF . The voltage rating must be greater than the maximum input voltage.

8.2.1.2.2 Output Capacitor

The device requires an output capacitor to stabilize the output voltage. The capacitor value should be between 2.2 μF and 100 μF . The ESR range should be between 1 m Ω and 2 Ω . TI recommends selecting a ceramic capacitor with low ESR to improve the load transient response.

8.2.1.3 Application Curve

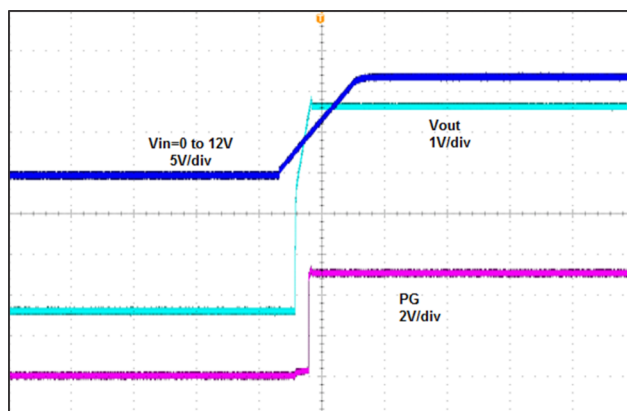


Figure 25. Power Up (5 V), 20 ms/div, $I_L = 20 \text{ mA}$

8.2.2 TPS7A69-Q1 Typical Application

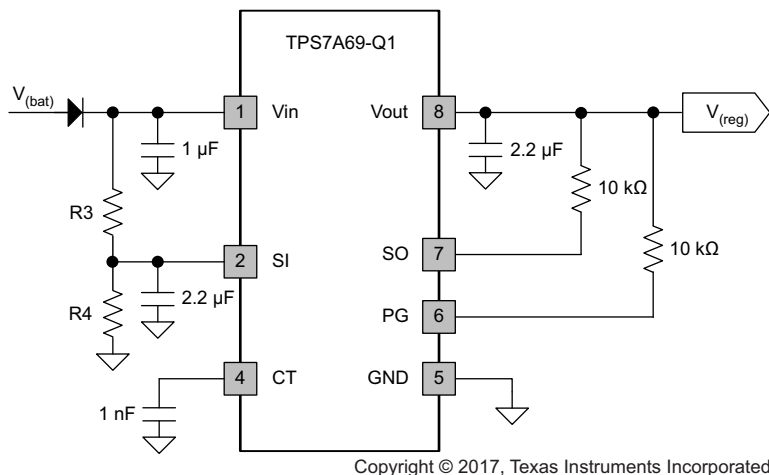


Figure 26. Typical Application Schematic for TPS7A69-Q1

8.2.2.1 Design Requirements

For this design example, use the parameters listed in [Table 2](#) as the input parameters.

Table 3. Design Parameters

DESIGN PARAMETER	EXAMPLE VALUE
Input voltage range	4 V to 40 V
Output voltage	3.3 V
Output current rating	150 mA
Output capacitor range	2.2 μF to 100 μF
Output capacitor ESR range	1 mΩ to 2 Ω
CT capacitor range	100 pF to 100 nF
Low-voltage tracking threshold	6 V to 9 V

8.2.2.2 Detailed Design Procedure

To begin the design process, determine the following:

- Input voltage range
- Output voltage
- Output current rating
- Input capacitor
- Output capacitor
- Power-up-reset delay time
- Low-voltage tracking threshold

8.2.2.2.1 Low-Voltage Tracking Threshold

After determining the low-voltage tracking threshold, calculate the ratio of the resistor divider connected to VIN, SI, and GND by the following equation:

$$\frac{R3}{R4} = \frac{V_{(LT)}}{1.223} - 1 \quad (3)$$

TI recommends that the values of both R3 and R4 be less than 100 kΩ.

8.2.2.3 Application Curve

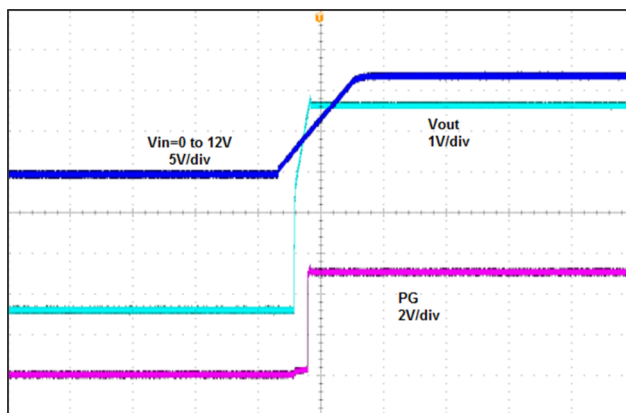


Figure 27. Power Up (5 V), 20 ms/div, I_L = 20 mA

9 Power Supply Recommendations

Design of the device is for operation from an input voltage supply with a range between 4 V and 28 V. This input supply must be well regulated. If the input supply is located more than a few inches from the TPS7A66-Q1 or TPS7A69-Q1 device, TI recommends adding an electrolytic capacitor with a value of 22 μ F and a ceramic bypass capacitor at the input.

10 Layout

10.1 Layout Guidelines

The high impedance of the FB pin makes the regulator sensitive to parasitic capacitances that may couple undesirable signals from nearby components (especially from logic and digital devices, such as microcontrollers and microprocessors); these capacitive-coupled signals may produce undesirable output voltage transients. In these cases, TI recommends the use of a fixed-voltage version of the TPS7A66-Q1, or isolation of the FB node by flooding the local PCB area with ground-plane copper to minimize any undesirable signal coupling.

10.1.1 Package Mounting

Solder pad footprint recommendations for the TPS7A66-Q1 and TPS7A69-Q1 are available at the end of this product data sheet and at www.ti.com.

10.1.2 Board Layout Recommendations to Improve PSRR and Noise Performance

For the layout of TPS7A66-Q1 and TPS7A69-Q1, place the input and output capacitors close to the devices as shown in [Figure 28](#) and [Figure 29](#), respectively. In order to enhance the thermal performance, TI recommends surrounding the device with some vias.

To improve ac performance such as PSRR, output noise, and transient response, TI recommends a board design with separate ground planes for VIN and VOUT, with each ground plane connected only at the GND pin of the device. In addition, the ground connection for the output capacitor should connect directly to the GND pin of the device.

Minimize equivalent series inductance (ESL) and ESR in order to maximize performance and ensure stability. Place every capacitor as close as possible to the device and on the same side of the PCB as the regulator itself.

Do not place any of the capacitors on the opposite side of the PCB from where the regulator is installed. TI strongly discourages the use of vias and long traces because they may impact system performance negatively and even cause instability.

If possible, and to ensure the maximum performance specified in this product data sheet, use the same layout pattern used for the TPS7A66-Q1 and TPS7A69-Q1 evaluation board, available at www.ti.com.

10.2 Layout Examples

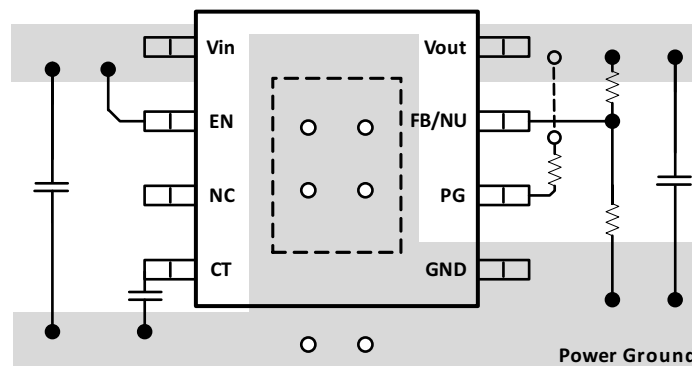


Figure 28. TPS7A66-Q1 Board Layout Diagram

Layout Examples (continued)

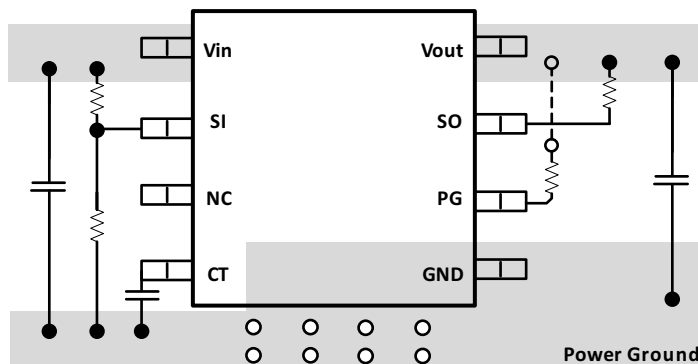


Figure 29. TPS7A69-Q1 Board Layout Diagram

10.3 Power Dissipation and Thermal Considerations

Calculate power dissipated in the device using [Equation 4](#).

$$P_D = I_O \times (V_{(Vin)} - V_{(Vout)}) + I_{(q)} \times V_{(Vin)} \quad (4)$$

where:

P_D = continuous power dissipation

I_O = output current

V_{IN} = input voltage

V_{OUT} = output voltage

As $I_{(q)} \ll I_O$, therefore ignore the term $I_{(q)} \times V_{IN}$ in [Equation 4](#).

For a device under operation at a given ambient air temperature (T_A), calculate the junction temperature (T_J) using [Equation 5](#).

$$T_J = T_A + (R_{\theta JA} \times P_D) \quad (5)$$

where:

$R_{\theta JA}$ = junction-to-ambient air thermal impedance

$$\Delta T = T_J - T_A = (R_{\theta JA} \times P_D) \quad (6)$$

11 Device and Documentation Support

11.1 Related Links

The table below lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to order now.

Table 4. Related Links

PARTS	PRODUCT FOLDER	ORDER NOW	TECHNICAL DOCUMENTS	TOOLS & SOFTWARE	SUPPORT & COMMUNITY
TPS7A66-Q1	Click here	Click here	Click here	Click here	Click here
TPS7A69-Q1	Click here	Click here	Click here	Click here	Click here

11.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

11.3 Community Resources

[TI E2E™ support forums](#) are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's [Terms of Use](#).

11.4 Trademarks

E2E is a trademark of Texas Instruments.

All other trademarks are the property of their respective owners.

11.5 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

11.6 Glossary

[SLYZ022](#) — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

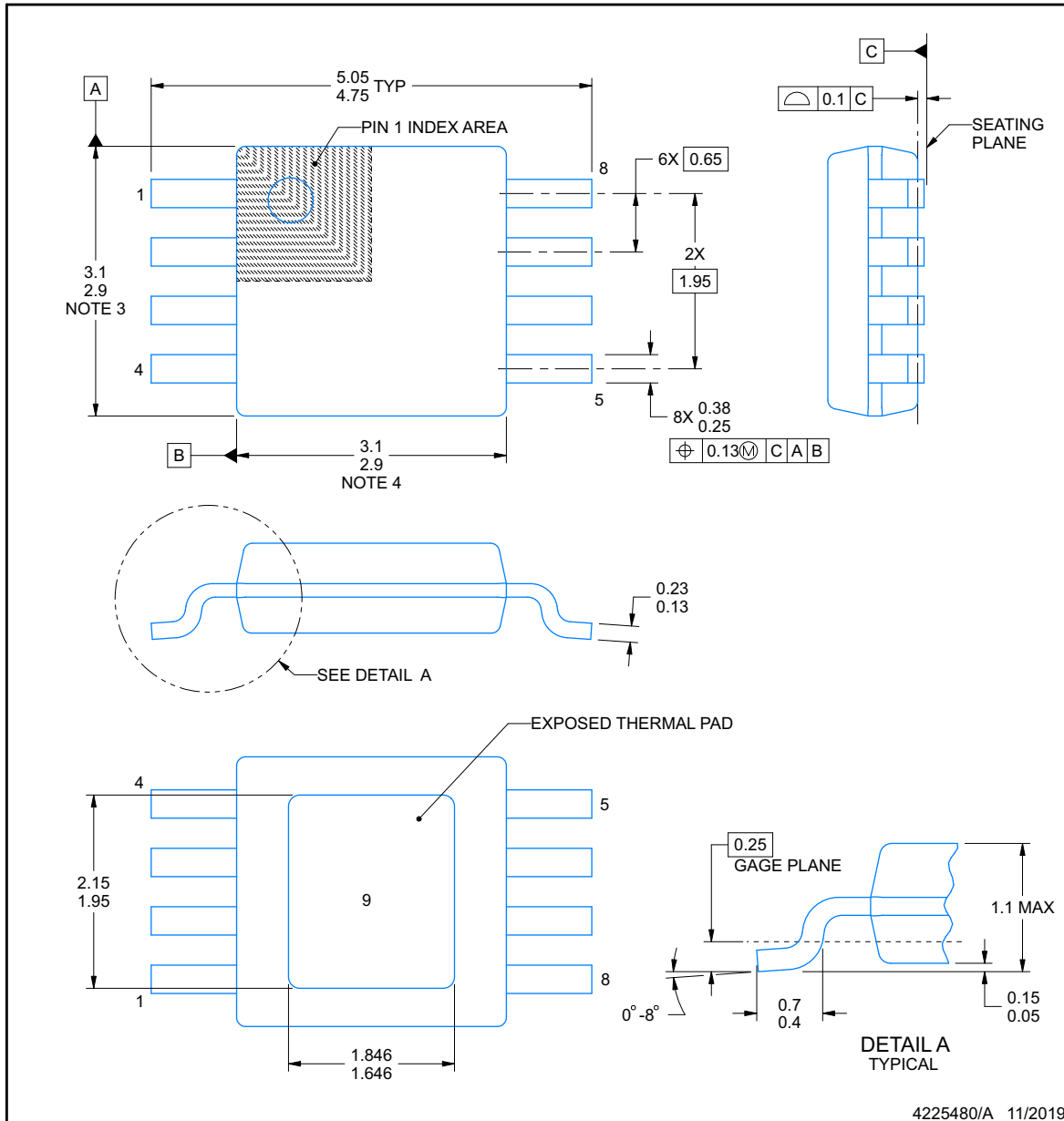
12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most-current data available for the designated devices. This data is subject to change without notice and without revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

DGN0008G

PowerPAD™ VSSOP - 1.1 mm max height

SMALL OUTLINE PACKAGE



4225480/A 11/2019

NOTES:

PowerPAD is a trademark of Texas Instruments.

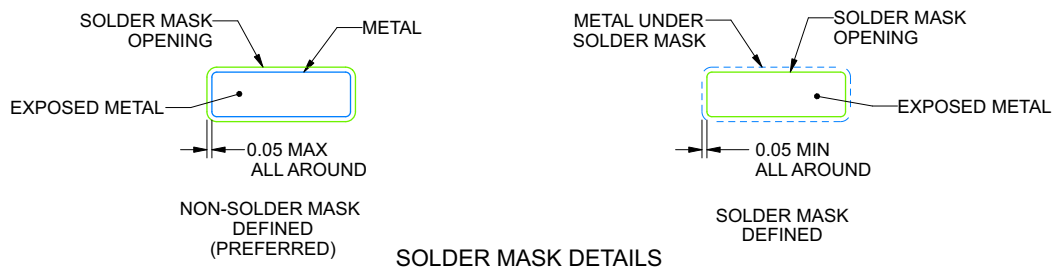
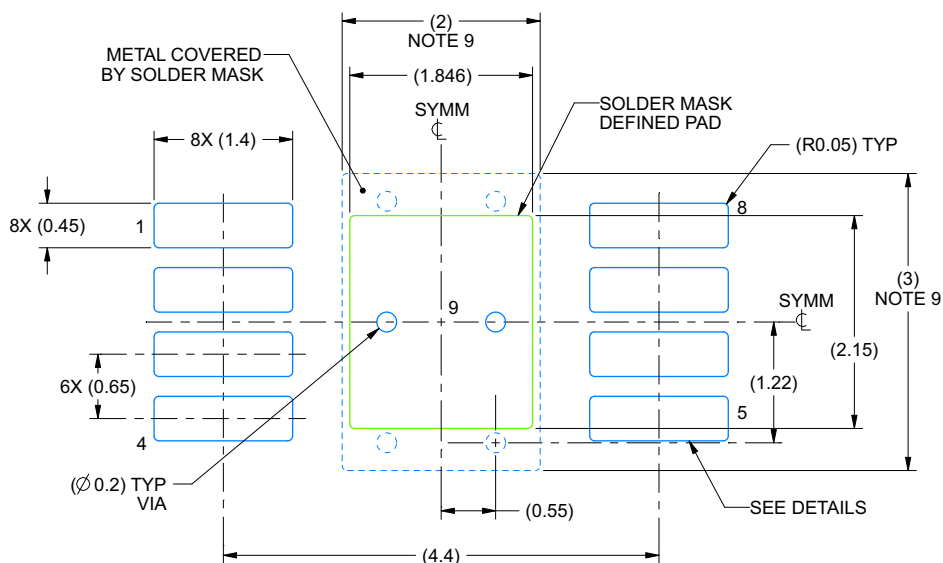
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-187.

EXAMPLE BOARD LAYOUT

DGN0008G

PowerPAD™ VSSOP - 1.1 mm max height

SMALL OUTLINE PACKAGE



4225480/A 11/2019

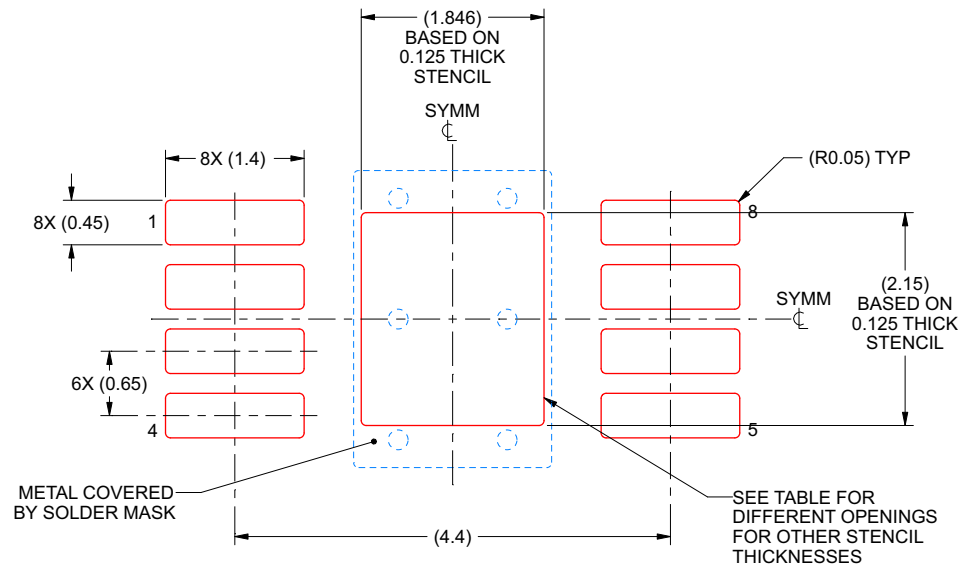
NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.
9. Size of metal pad may vary due to creepage requirement.

EXAMPLE STENCIL DESIGN

DGN0008G
PowerPAD™ VSSOP - 1.1 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE
EXPOSED PAD 9:
100% PRINTED SOLDER COVERAGE BY AREA
SCALE: 15X

STENCIL THICKNESS	SOLDER STENCIL OPENING
0.1	2.06 X 2.40
0.125	1.846 X 2.15 (SHOWN)
0.15	1.69 X 1.96
0.175	1.56 X 1.82

4225480/A 11/2019

NOTES: (continued)

10. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
11. Board assembly site may have different recommendations for stencil design.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package Pins	Package qty Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TPS7A6601QDGNRQ1	Active	Production	HVSSOP (DGN) 8	2500 LARGE T&R	Yes	NIPDAUAG	Level-2-260C-1 YEAR	-40 to 125	PA4Q
TPS7A6601QDGNRQ1.A	Active	Production	HVSSOP (DGN) 8	2500 LARGE T&R	Yes	NIPDAUAG	Level-2-260C-1 YEAR	-40 to 125	PA4Q
TPS7A6633QDGNRQ1	Active	Production	HVSSOP (DGN) 8	2500 LARGE T&R	Yes	NIPDAUAG	Level-2-260C-1 YEAR	-40 to 125	PA2Q
TPS7A6633QDGNRQ1.A	Active	Production	HVSSOP (DGN) 8	2500 LARGE T&R	Yes	NIPDAUAG	Level-2-260C-1 YEAR	-40 to 125	PA2Q
TPS7A6650QDGNRQ1	Active	Production	HVSSOP (DGN) 8	2500 LARGE T&R	Yes	NIPDAUAG	Level-2-260C-1 YEAR	-40 to 125	PA1Q
TPS7A6650QDGNRQ1.A	Active	Production	HVSSOP (DGN) 8	2500 LARGE T&R	Yes	NIPDAUAG	Level-2-260C-1 YEAR	-40 to 125	PA1Q
TPS7A6933QDRQ1	Active	Production	SOIC (D) 8	2500 LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 125	6933
TPS7A6933QDRQ1.A	Active	Production	SOIC (D) 8	2500 LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 125	6933
TPS7A6950QDRQ1	Active	Production	SOIC (D) 8	2500 LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 125	6950
TPS7A6950QDRQ1.A	Active	Production	SOIC (D) 8	2500 LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 125	6950

⁽¹⁾ **Status:** For more details on status, see our [product life cycle](#).

⁽²⁾ **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

⁽³⁾ **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

⁽⁴⁾ **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

⁽⁵⁾ **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

⁽⁶⁾ **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative

and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

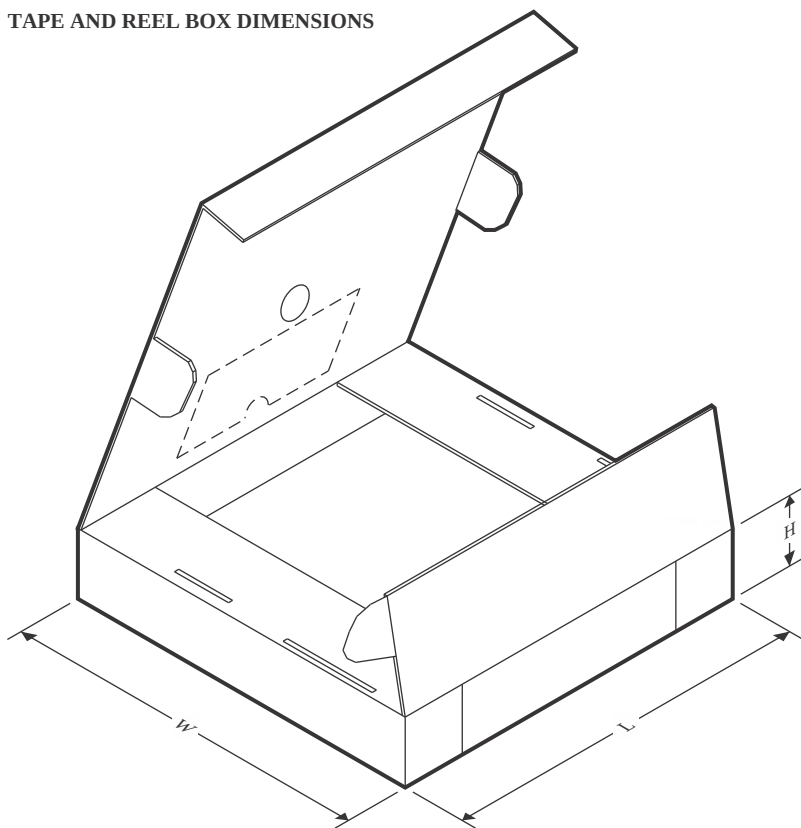
TAPE AND REEL INFORMATION



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS7A6601QDGNRQ1	HVSSOP	DGN	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
TPS7A6633QDGNRQ1	HVSSOP	DGN	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
TPS7A6650QDGNRQ1	HVSSOP	DGN	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
TPS7A6933QDRQ1	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TPS7A6950QDRQ1	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS7A6601QDGNRQ1	HVSSOP	DGN	8	2500	366.0	364.0	50.0
TPS7A6633QDGNRQ1	HVSSOP	DGN	8	2500	366.0	364.0	50.0
TPS7A6650QDGNRQ1	HVSSOP	DGN	8	2500	366.0	364.0	50.0
TPS7A6933QDRQ1	SOIC	D	8	2500	353.0	353.0	32.0
TPS7A6950QDRQ1	SOIC	D	8	2500	353.0	353.0	32.0



PACKAGE OUTLINE

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT

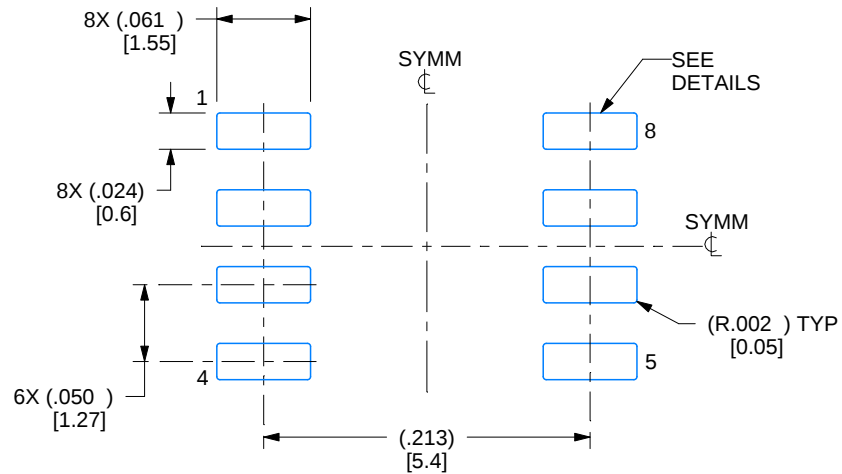


1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.

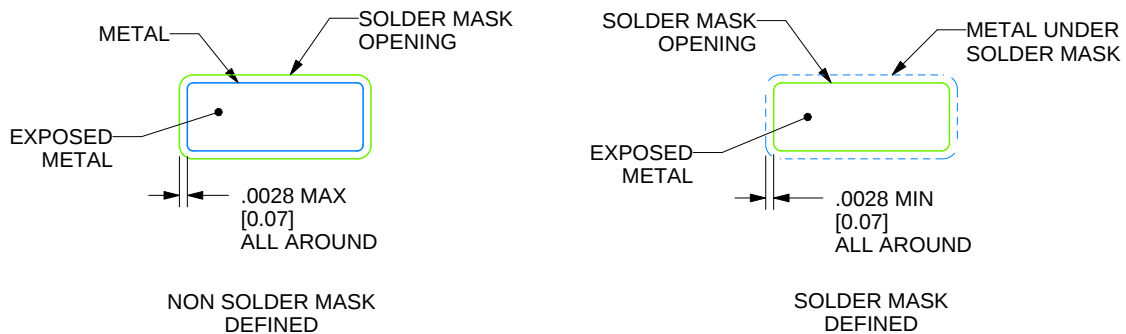
D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X



SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

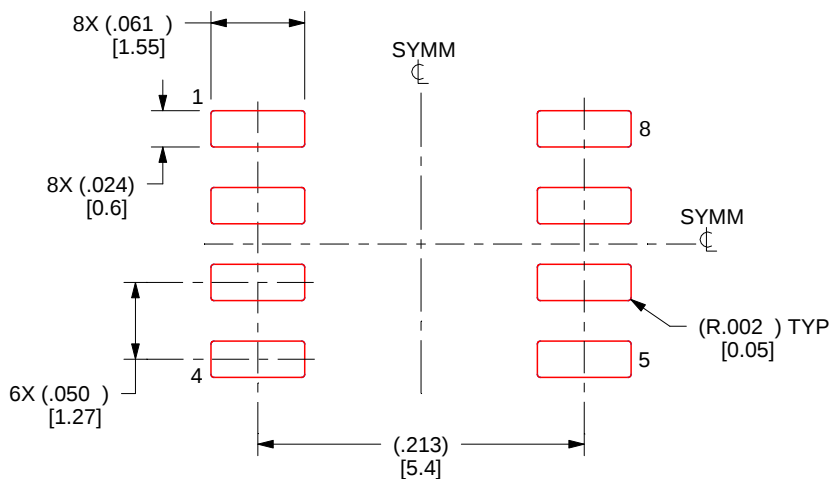
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

4214825/C 02/2019

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

GENERIC PACKAGE VIEW

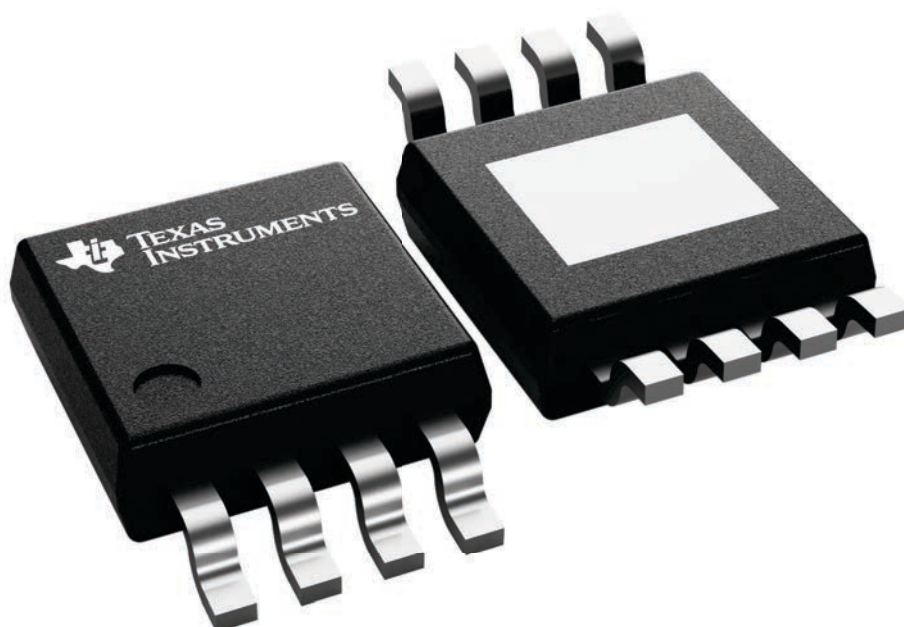
DGN 8

PowerPAD™ HVSSOP - 1.1 mm max height

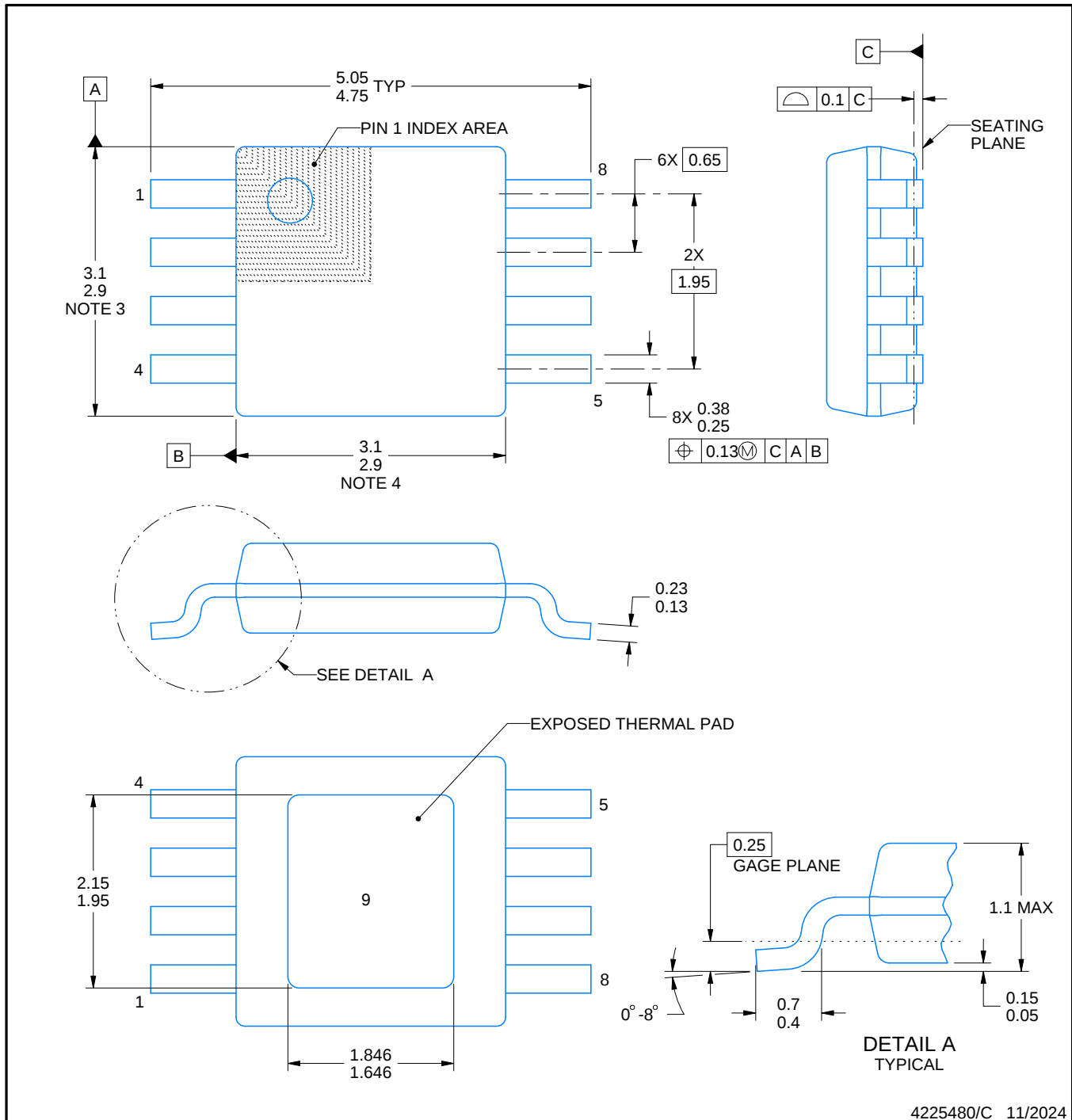
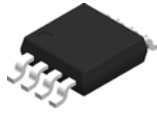
3 x 3, 0.65 mm pitch

SMALL OUTLINE PACKAGE

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



4225482/B



4225480/C 11/2024

NOTES:

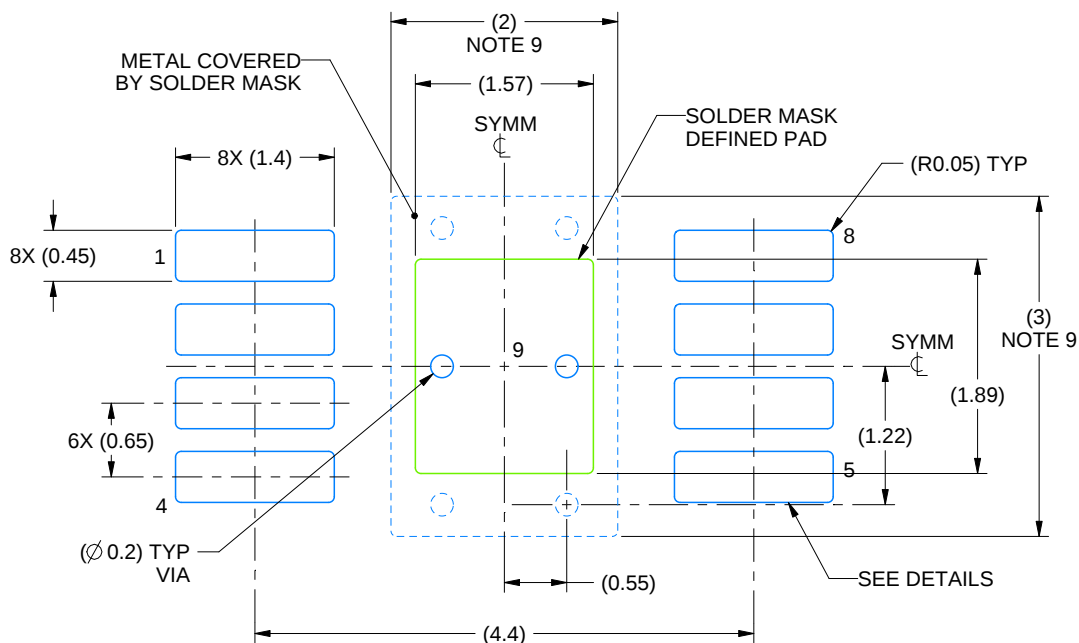
PowerPAD is a trademark of Texas Instruments.

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-187.

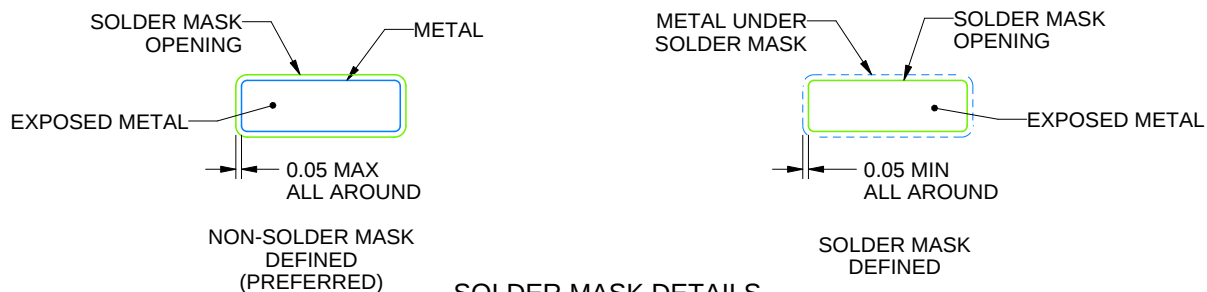
DGN0008G

PowerPAD™ HVSSOP - 1.1 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 15X



SOLDER MASK DETAILS

4225480/C 11/2024

NOTES: (continued)

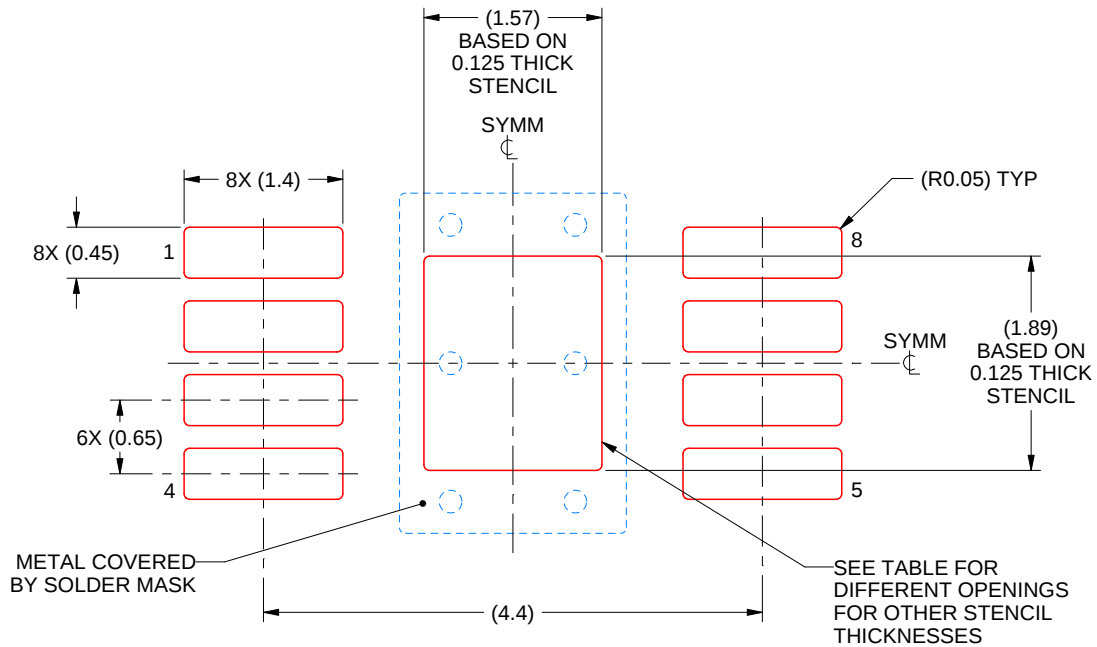
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.
9. Size of metal pad may vary due to creepage requirement.

EXAMPLE STENCIL DESIGN

DGN0008G

PowerPAD™ HVSSOP - 1.1 mm max height

SMALL OUTLINE PACKAGE



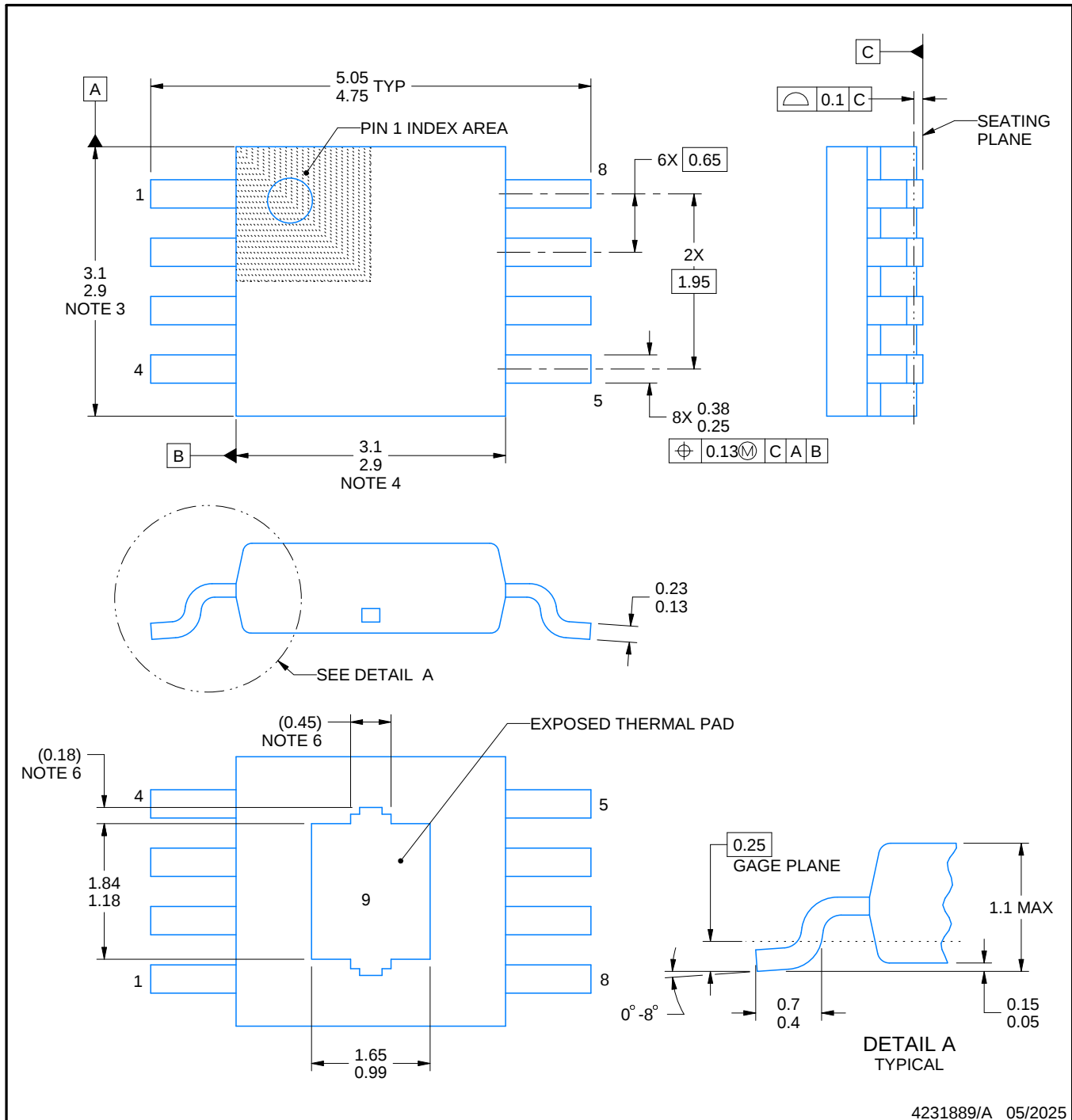
SOLDER PASTE EXAMPLE
EXPOSED PAD 9:
100% PRINTED SOLDER COVERAGE BY AREA
SCALE: 15X

STENCIL THICKNESS	SOLDER STENCIL OPENING
0.1	1.76 X 2.11
0.125	1.57 X 1.89 (SHOWN)
0.15	1.43 X 1.73
0.175	1.33 X 1.60

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NOTES: (continued)

10. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
11. Board assembly site may have different recommendations for stencil design.



4231889/A 05/2025

NOTES:

PowerPAD is a trademark of Texas Instruments.

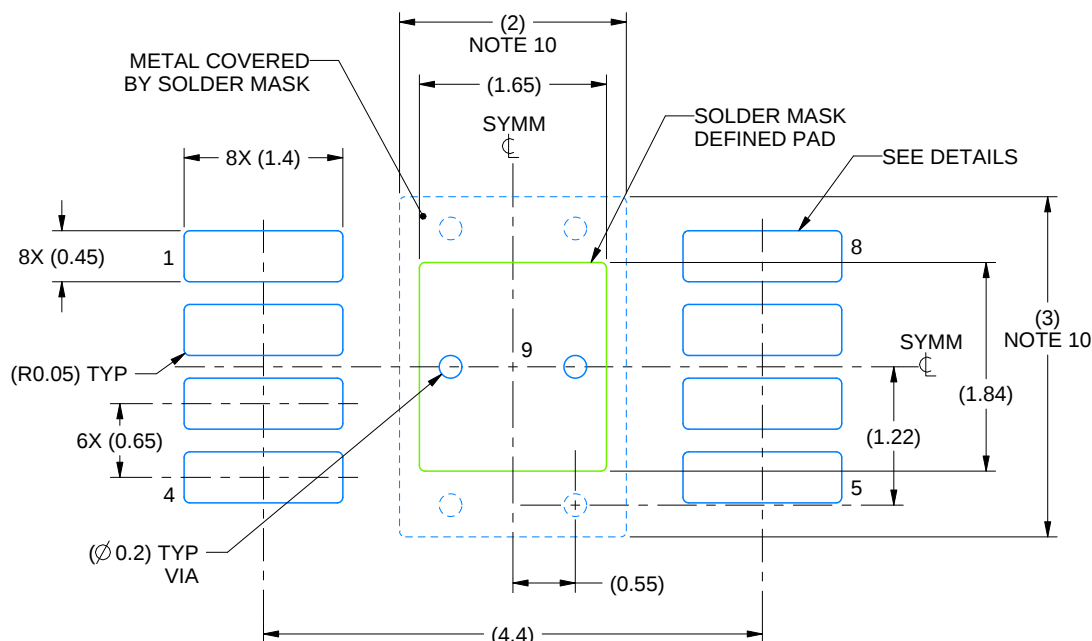
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-187.
6. Features may differ or may not be present.

EXAMPLE BOARD LAYOUT

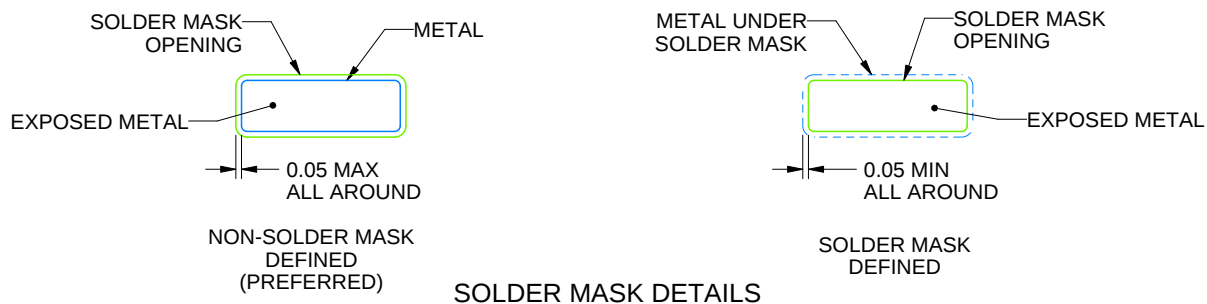
DGN0008K

PowerPAD™ VSSOP - 1.1 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 15X



SOLDER MASK DETAILS

4231889/A 05/2025

NOTES: (continued)

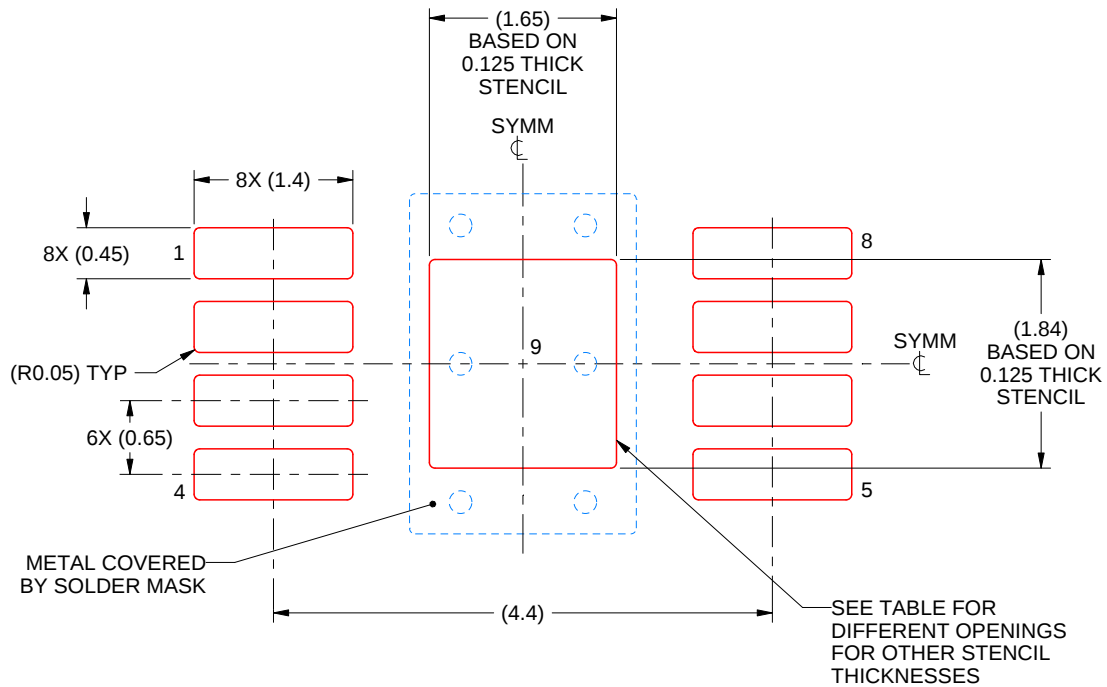
7. Publication IPC-7351 may have alternate designs.
8. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
9. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.
10. Size of metal pad may vary due to creepage requirement.

EXAMPLE STENCIL DESIGN

DGN0008K

PowerPAD™ VSSOP - 1.1 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE
EXPOSED PAD 9:
100% PRINTED SOLDER COVERAGE BY AREA
SCALE: 15X

STENCIL THICKNESS	SOLDER STENCIL OPENING
0.1	1.84 X 2.06
0.125	1.65 X 1.84 (SHOWN)
0.15	1.51 X 1.68
0.175	1.39 X 1.56

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NOTES: (continued)

11. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
12. Board assembly site may have different recommendations for stencil design.

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