TPS7B7802-Q1 Automotive, Dual-Channel LDO With Diagnostics and I²C Interface

1 Features

- AEC-Q100 qualified for automotive applications:
  - Temperature grade 1: -40°C to 125°C, T_A
  - Junction temperature; -40°C to 150°C, T_J
- Wide input voltage range:
  - Absolute maximum range: -40V to 45V
  - Operating range: 4.5V to 40V
- Output voltage:
  - Wide range of output voltage can be set using external resistors: 2V to 40V
  - Output voltage range programmed using I²C without external resistors: 2V to 27.4V in 100mV steps
  - Power switch mode can be set using I²C (internal FB mode) or tying FB to GND (external FB resistor mode)
- Supports up to 300mA of load current per channel
- High accuracy current sense (≤ ±15%) to detect low load currents (≤25mA) without further calibration.
- Adjustable current limit via I²C programming
- Low dropout voltage: 315mV (max) at 100mA
- Stable over a wide range of ceramic output capacitor values:
  - C_{OUT} Range: 4.7µF to 100µF
  - ESR Range : 1mΩ to 500mΩ
- Integrated protection features:
  - Reverse current protection
  - Reverse polarity protection
  - Overtemperature protection
  - Protection against output short-circuit to ground and battery
- Integrated diagnostic and monitoring features using I²C interface:
  - Input and Output voltage Monitoring
  - Load Current Monitoring
  - Junction Temperature monitoring
  - Open circuit detection
  - Output under-voltage and over-voltage detection.

2 Applications

- Powering Low Noise Amplifiers in Automotive Head Unit
- Powering Camera Modules in Surround view system
- Microphone Power

3 Description

The TPS7B7802-Q1 is a monolithic dual channel, high voltage low-dropout regulator with an integrated ADC and I²C interface. The device has a wide input voltage operating range, and is designed to protect against a 45V input voltage load dump scenario. This device is an excellent choice to power remotely located LNAs (associated with AM/FM/GNSS antenna), microphone and camera modules over coax cables. In harsh automotive environments, coax cables are potentially exposed to various fault conditions, increasing risk of failure. Such conditions include short to ground, short to battery, and overtemperature. TPS7B7802-Q1 comes with integrated protection features against each of these fault conditions, as well as protection against reverse polarity. The device incorporates a topology containing two back-to-back P-channel metal-oxide semiconductor field-effect transistors (MOSFETs). This PMOS topology eliminates the need for an external diode that is otherwise required to prevent the flow of reverse current. Each channel can provide up to 300mA of output current and an adjustable output voltage from 2V to 40V.

This device can uniquely identify and diagnose several fault conditions. This diagnosis information can be inferred from a register via I²C communication and the error pin. The integrated 10-bit ADC allows the user to continuously monitor the input voltage, output voltage, junction temperature and load current. The device features a high accuracy current sense circuitry across the current range (≤ ±15%, 1mA to 300mA) for both channels. This feature allows the device to precisely detect and distinguish between open, normal and short-circuit conditions without further calibration. Each channel also offers adjustable current limit, that can be set using I²C communication.

This device operates over −40°C to +125°C ambient temperature range and is available in a thermally conductive package with wettable flanks.

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Package Information

PART NUMBER	PACKAGE(1)	PACKAGE SIZE(2)
TPS7B7802-Q1	RTJ (WQFN, 20)	4mm × 4mm

(1) For more information, see the *Mechanical, Packaging, and Orderable Information*.
(2) The package size (length × width) is a nominal value and includes pins, where applicable.

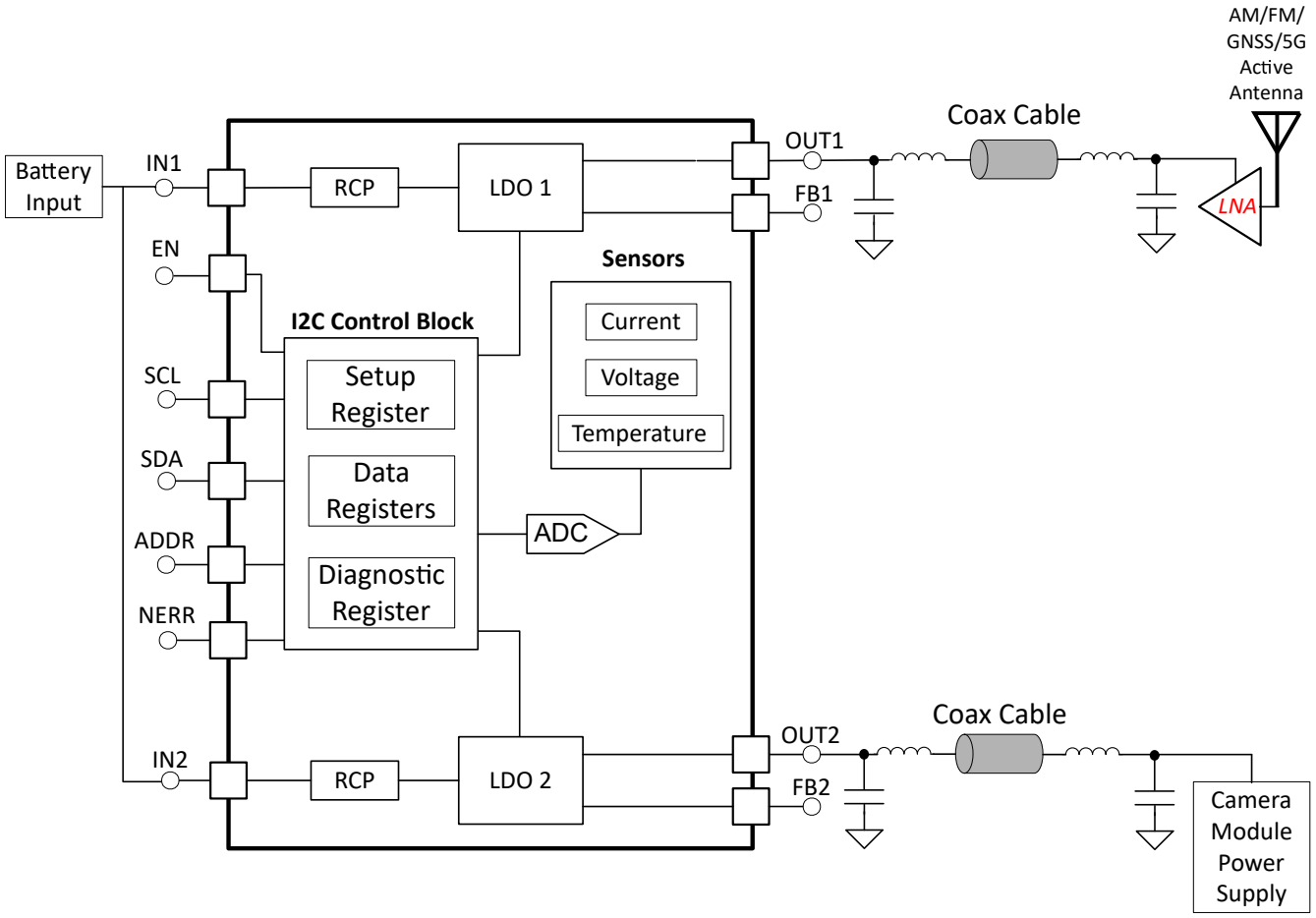

Figure 3-1. Typical Application

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4 Pin Configuration and Functions

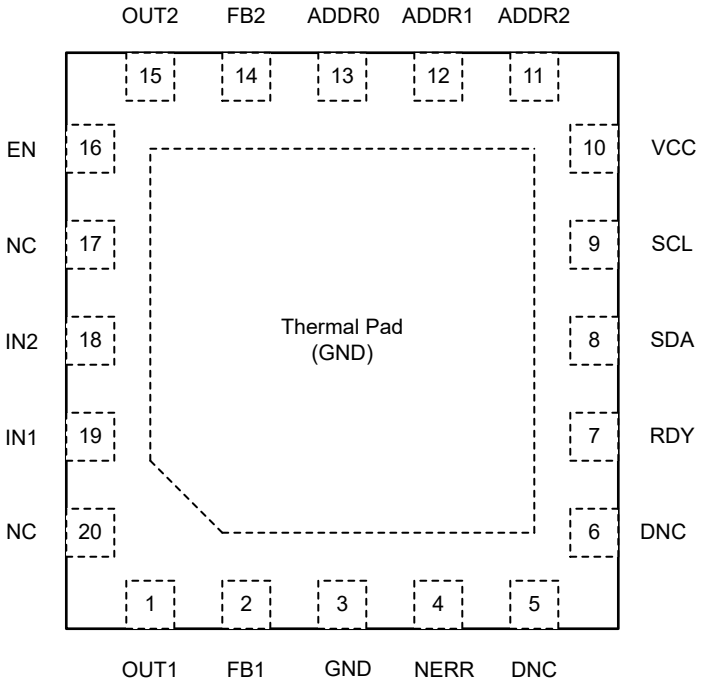

Figure 4-1. Dual-Channel TPS7B7802-Q1 RTJ Package, 20-Pin WQFN With PowerPAD (Top View)

Table 4-1. Pin Functions

PIN		TYPE[1]	DESCRIPTION
NO.	NAME		
1	OUT1	O	Output of LDO1. Needs to be Bypassed to GND with at least a 4.7µF ceramic capacitor. Place this output capacitor as close to this pin as possible.
2	FB1	I	Feedback pin of LDO1. If output voltage is not set internally, this pin must be connected through an appropriate resistor divider to OUT1. If using internal resistor divider treat this as an NC pin. See the *Output Voltage Setting* section for more details.
3	GND	G	Ground. Connect exposed pad to GND
4	NERR	O	Open-Drain, Active-Low Fault Output. NERR asserts low when any diagnostic bit, that is not masked, is asserted. Connect a pullup resistor between NERR and a logic supply.
5	DNC	-	Do not connect this pin to a voltage source. Do not leave this pin floating. Connect this pin to GND.
6	DNC	-	Do not connect this pin to a voltage source. Do not leave this pin floating. Connect this pin to GND.
7	RDY	O	This is an active high, open drain based pin. Connect this pin to a positive voltage with a pullup resistor. The pin internally assumes a high impedance state when V_{IN} ≥ Digital $UVLO_{RISING}$ specification. Logic high on this Pin indicates that device is ready for I^2C communication.
8	SDA	I/O	I^2C Serial Data I/O. Connect a pullup resistor between pin and a logic supply.
9	SCL	I	I^2C Clock Input. Connect a pullup resistor from pin and a logic supply.
10	VCC	O	This is an internal 1.8V regulator output that powers an internal control circuit. Connect a 1µF ceramic capacitor between VCC and GND.
11	ADRR2	I	Address Pins, selects I^2C addresses for the device.
12	ADRR1	I	
13	ADRR0	I	
14	FB2	I	Feedback pin of LDO2. If output voltage is not set internally, this pin must be connected through an appropriate resistor divider to OUT2. If using internal resistor divider treat this as an NC pin. See the *Output Voltage Setting* section for more details.
15	OUT2	O	Output of LDO2. Needs to be Bypassed to GND with at least a 4.7µF ceramic capacitor. Place this output capacitor as close to this pin as possible.
16	EN	I	Enable Input. When EN goes low, device output channels get disabled. Device requires this pin be pulled to a Logic high as well as Digital enabling for Output channels to regulate.

Table 4-1. Pin Functions (continued)

PIN		TYPE[1]	DESCRIPTION
NO.	NAME		
17	NC	-	Not Connected. Connect to GND
18	IN2	I	Supply Input to LDO2. Must be connected to IN1 pin, close to the device.
19	IN1	I	Supply Input to LDO1. Bypass this to GND with a ceramic capacitor to improve performance. IN1 and IN2 pins must be connected together, close to the device.
20	NC	-	Internally not connected. Connect to GND for optimized thermal performance

(1) I = Input, O = Output, I/O = Input or Output, G = Ground.

5 Specifications

5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
V_{IN1}, V_{IN2}	Unregulated input Voltage(2)	–40	45	V
EN	Enable Input	–0.3	45	V
V_{OUT1}, V_{OUT2}	Regulated output(2)	–0.3	45	V
FB1, FB2	Feedback	–0.3	45	V
ADDR0, ADDR1, ADDR2, RDY, SDA, SCL and NERR		-0.3	5.5	V
V_{CC}	Internal Sub-Regulator Voltage	-0.3	2	V
T_J	Operating junction temperature range	–40	150	°C
T_{stg}	Storage temperature	–65	150	°C

(1) Operation outside the *Absolute Maximum Ratings* may cause permanent device damage. *Absolute Maximum Ratings* do not imply functional operation of the device at these or any other conditions beyond those listed under *Recommended Operating Conditions*. If used outside the *Recommended Operating Conditions* but within the *Absolute Maximum Ratings*, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.
(2) Absolute maximum voltage, withstand 45 V for 200 ms

5.2 ESD Ratings

				VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per AEC Q100-002 (1) (2)		±2000	V
		Charged-device model (CDM), per AEC Q100-011	All pins	±500	
			Corner pins	±750	

(1) AEC Q100-002 indicates that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.
(2) The human body model is a 100pF capacitor discharged through a 1.5-kΩ resistor into each pin.

5.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	TYP	MAX	UNIT
V_{IN1}, V_{IN2}	Input voltage	4.5		40	V
V_{OUT1}, V_{OUT2}	Output voltage set using I^2C	2		27.4	V
	Output Voltage set using external feedback resistors	2		40	V
I_{OUT1}, I_{OUT2}	Output current	0		300	mA
V_{EN}	High voltage (I/O)	0		40	V
V_{FB1}, V_{FB2}	Feedback Voltage	0		2	V
ADDR0, ADDR1, ADDR2	Address pins	0		5	V
SDA, SCL	Serial Clock and data pins	0		5	V
RDY	Ready pin to indicate I^2C communication status.	0		5	V
NERR	Error pin voltage	0		5	V
V_{CC}		0		2	V
$R_{PULL-UP}$	Error, SDA, SCL and RDY pin external pullup resistor	1			kΩ
R_{FB}	FB resistor			100	kΩ
C_{IN}	Input capacitor(1)	1	2.2		µF
C_{OUT}	Output capacitor(2)	4.7		100	µF
ESR	Output capacitor ESR requirements	1		500	mΩ
T_J	Operating junction temperature	–40		150	°C

(1) For robust EMI performance the minimum input capacitance is 500 nF
(2) Effective output capacitance of 2µF minimum required for stability.

5.4 Thermal Information

THERMAL METRIC (1) (2)		TPS7B7802-Q1	
		RTJ	Unit
		20 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	40	°C/W
$R_{\theta JCtop}$	Junction-to-case (top) thermal resistance	28	
$R_{\theta JB}$	Junction-to-board thermal resistance	17	
ψ_{JT}	Junction-to-top characterization parameter	0.3	
ψ_{JB}	Junction-to-board characterization parameter	17	
$R_{\theta JCbot}$	Junction-to-case (bottom) thermal resistance	1.5	

(1) The thermal data is based on the JEDEC standard high-K board layout, JESD 51-7. This board is a two-signal, two-plane, four-layer board with 2-oz. copper on the external layers. The copper pad is soldered to the thermal land pattern. Incorporate correct attachment procedure.
(2) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package* *Thermal Metrics* application note.

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5.5 Electrical Characteristics

Specified at T_J = –40°C to +150°C, V_{IN} = 12V, V_{EN} = 3V, I_{OUT} = 100µA, C_{OUT} = 4.7µF, C_{IN} = 1µF (Unless otherwise noted). Typical values are at T_J = 25°C. Both LDO Channels identical

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{FBX}	Feedback Voltage	V_{FBx} = V_{OUTx}, V_{INx} = 5V	1.96	2.0	2.04	V
$I_{FB\ LKG\ X}$	Feedback Pin Leakage				1	µA
I_Q	Quiescent current, ADC enabled	V_{INX} = 12V, I_{OUT1} = 0µA, I_{OUT2} = 0µA, V_{OUTX} = 8V		500	1000	µA
I_{GND}	Ground Current, ADC enabled	V_{INX} = 12V, I_{OUT1} = 100µA, I_{OUT2} = 0µA, V_{OUTX} = 8V			1100	µA
		V_{INx} = 12V, I_{OUT1} = 300mA, I_{OUT2} = 0mA, V_{OUTx} = 8V			4800	µA
		V_{INX} = 12V, I_{OUT1} = 300mA, I_{OUT2} = 300mA, V_{OUTX} = 8V			8800	µA
$I_{DISABLED}$	Quiescent Current when device is disabled	V_{INx} = 40V, V_{EN} = 0V, ADC disabled			35	µA
$V_{UVLO(RISING)}$	Rising Input Supply UVLO	V_{IN} rising, I_{OUT} = 1mA	4.25	4.35	4.45	V
$V_{UVLO(FALLING)}$	Falling Input Supply UVLO	V_{IN} falling, I_{OUT} = 1mA	3.8	3.9	4.0	V
$V_{UVLO(HYST)}$	$V_{UVLO(IN)}$ Hysteresis			450		mV
Digital UVLO $_{(RISING)}$	V_{IN} rising. Min V_{IN} for I^2C Communication		1.5	2	3.2	V
Digital UVLO $_{(FALLING)}$	V_{IN} falling. Max V_{IN} at which register map resets to default state		1.75	2.3	2.8	V
$V_{EN\ L}$	Enable Logic input low level				0.7	V
$V_{EN\ H}$	Enable Logic input high level		2			V
I_{EN}	EN pin leakage current	V_{EN} = V_{INx} = 12V			0.3	µA
V_{IL}	SDA, SCL Logic low level				0.4	V
V_{IH}	SDA, SCL Logic high level		1.4			V
V_{OL}	SDA, Output Logic low level	I_{SINK} = 3mA			0.4	V
f_{SCL}	I^2C Clock Frequency or Data Rate				1	MHz
$V_{ADDR\ L}$	ADDRx Logic low level				0.4	V
$V_{ADDR\ H}$	ADDRx Logic high level		1.4			V
$I_{LEAKAGE}$	SDA, SCL & ADDRx pins				0.5	µA
V_{OUT}	Regulated output	0.5mA ≤ I_{OUT} ≤ 300mA, V_{OUT} + 2V ≤ V_{IN} ≤ 40V, for range of V_{OUT} set using I^2C	–2.5		2.5	%
$\Delta V_{OUT(\Delta VIN)}$	Line regulation	I_{OUT} = 0.5mA, V_{OUT} + 2V < V_{IN} < 40V, V_{OUT} ≥ 2V			0.25	%
$\Delta V_{OUT(\Delta IOUT)}$	Load regulation	0.5mA ≤ I_{OUT} ≤ 300mA, V_{IN} = V_{OUT} + 2V, V_{OUT} ≥ 2V			0.25	%
V_{DO}	Dropout voltage	V_{IN} = 5V, V_{FB} = 1.8V, I_{OUT} = 300mA			950	mV
		V_{IN} = 12V, V_{FB} = 1.8V, I_{OUT} = 300mA			950	mV
PSRR	Power supply ripple rejection	V_{IN} = 12V, V_{RIPPLE} = $1V_{P-P}$, V_{OUT} = 8V, I_{OUT} = 100mA, f = 100Hz		80		dB
V_n	Output noise voltage (RMS)	Bandwidth = 10Hz to 100kHz, V_{OUT} = 2V, I_{OUT} = 100mA		76		µV
V_{IN}	Input Voltage accuracy measured through the ADC	4.5V ≤ V_{IN} ≤ 40V	-2	0.5	2	%
V_{OUT}	Output Voltage accuracy measured through the ADC	2V ≤ V_{OUT} ≤ 40V	-2.5	0.5	2.5	%
I_{OUT}	Output current accuracy measured through the ADC	High current range I_{OUT} > 25mA	-13		13	%
		Low current range 1mA < I_{OUT} ≤ 5mA	-15		15	%
		Low current range 5mA < I_{OUT} ≤ 25mA	-12		12	%
I_{CL}	Output current limit	Current limit accuracy for the range 25mA ≤ I_{CL} ≤ 125mA, in 25mA steps. Measured at V_{OUT} = V_{FB}	–10		10	mA
		Current limit accuracy for the range 150mA ≤ I_{CL} ≤ 400mA, in 25mA steps. Measured at V_{OUT} = V_{FB}	–7.5		7.5	%
		V_{OUT} forced at 0.9 × $V_{OUT(nom)}$, V_{IN} = $V_{OUT(nom)}$ + 1V, Current limit set to 1101	323.5	350	376.5	mA
		V_{OUT} forced at 0.9 × $V_{OUT(nom)}$, V_{IN} = $V_{OUT(nom)}$ + 1V, Current limit set to 0011	92.5	100	107.5	
		V_{OUT} forced at 0.9 × $V_{OUT(nom)}$, V_{IN} = $V_{OUT(nom)}$ + 1V, Current limit set to 0000	18	25	32	

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Specified at T_J = –40°C to +150°C, V_{IN} = 12V, V_{EN} = 3V, I_{OUT} = 100µA, C_{OUT} = 4.7µF, C_{IN} = 1µF (Unless otherwise noted). Typical values are at T_J = 25°C. Both LDO Channels identical

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_{ST_CL}	Current limit at Start-up	Startup Current limit accuracy for the range 25mA ≤ I_{CL} ≤ 125mA, in 25mA steps.	–10		10	mA
		Startup Current limit accuracy for the range 150mA ≤ I_{CL} ≤ 400mA, in 25mA steps. Measured at V_{OUT} = V_{FB}	–7.5		7.5	%
		Startup Current limit set to 0000	18	25	32	mA
		Startup Current limit set to 1101	323.5	350	376.5	
$I_{OL\ CHX}$	Open load Threshold	Accuracy for the range 8mA ≤ I_{OL} ≤ 15mA	–12.5		12.5	%
		Accuracy for the range 0mA ≤ I_{OL} ≤ 7mA	–1		1	mA
		$I_{OL\ CHX}$ set to 1111, V_{INx}= V_{EN} = 12V	13.1	15	16.9	
		$I_{OL\ CHX}$ set to 0001, V_{INx}= V_{EN} = 12V	0	1	2	
I_{OUT_WARN}	Output Current Warning	Output Current warning accuracy in the range 10mA ≤ $I_{OUT\ WARN}$ ≤ 110mA	-7.5		7.5	mA
		Output Current warning accuracy in the range 130mA ≤ $I_{OUT\ WARN}$ ≤ 310mA	-7.5		7.5	%
		Output current warning register set to 1111	285	310	335	mA
T_J	Junction Temperature Reading	Junction Temperature Accuracy over the range –40°C ≤ T_J < 150°C		±2.5		°C
	Junction Temperature Warn Setting	T_J warn register setting 101	120	125	130	°C
$t_{BLANKING}$	Blanking Time	Blanking Time register setting 100		8.5		msec
V_{PG} Thresholds	Over Voltage PG Threshold	V_{OUT} Rising	105	110	115	%
	Under Voltage PG Threshold	V_{OUT} Falling	83	88	93	%
	Hysteresis			2		%
I_R	Reverse Current at V_{IN}	V_{IN} = 0V, V_{OUT} = 20V			5	µA
	Reverse current detection	V_{OUTX} – V_{INX} at which reverse current is detected with V_{OUTX} rising, V_{INX} = 12V	5	25	45	mV
	Reverse current response time	V_{IN} = 12V, V_{OUTX} rising, V_{OUTx} - V_{INx} = 100mV			15	µs
I_{RN2}	Reverse Current at Negative V_{IN}	V_{IN} = –20V, V_{OUT} = 0V			5	µA
$V_{ERR\ LOW}$	Error pin low level voltage	I_{ERR} = 3mA			0.4	V
$I_{ERR\ LKG}$	Error pin leakage current	V_{ERR} = 5V, no fault detected			1	µA
$V_{RDY\ LOW}$	RDY Pin low level voltage	V_{IN} = 2.2V, I_{RDY} = 3mA			0.4	V
$I_{RDY\ LKG}$	RDY Pin leakage current				1	µA
$T_{SD(SHUTDOWN)}$	Junction shutdown temperature			175		°C
$T_{SD(HYST)}$	Hysteresis of thermal shutdown			14		°C

5.6 Timing Requirements - I²C Standard Mode

over operating free-air temperature range (unless otherwise noted)

		MIN	TYP	MAX	UNIT
f_{SCL}	SCL clock frequency			100	kHz
t_{BUF}	Bus free time between STOP and START condition	4.7			µs
t_{HD_STA}	Hold time (repeated) START condition	4			µs
t_{SU_STA}	Set-up time for a repeated START condition	4.7			µs
t_{SU_STO}	Set-up time for STOP condition	4			µs
t_{HD_DAT}	Data hold time	0			µs
t_{SU_DAT}	Data set-up time	250			ns
t_{LOW}	LOW period of the SCL clock	4.7			µs
t_{HIGH}	HIGH period of the SCL clock	4			µs
t_r	Rise time for both SDA and SCL signals			1000	ns
t_f	Fall time of both SDA and SCL signals			300	ns
t_{VD_DAT}	Data valid time	0		3.45	µs

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over operating free-air temperature range (unless otherwise noted)

		MIN	TYP	MAX	UNIT
t_{VD_ACK}	Data valid acknowledge time	0		3.45	µs

5.7 Timing Requirements - I²C Fast Mode

over operating free-air temperature range (unless otherwise noted)

		MIN	TYP	MAX	UNIT
f_{SCL}	SCL clock frequency			400	kHz
t_{BUF}	Bus free time between STOP and START condition	1.3			µs
t_{HD_STA}	Hold time (repeated) START condition	0.6			µs
t_{SU_STA}	Set-up time for a repeated START condition	0.6			µs
t_{SU_STO}	Set-up time for STOP condition	0.6			µs
t_{HD_DAT}	Data hold time	0			µs
t_{SU_DAT}	Data set-up time	100			ns
t_{LOW}	LOW period of the SCL clock	1.3			µs
t_{HIGH}	HIGH period of the SCL clock	0.6			µs
t_r	Rise time for both SDA and SCL signals			300	ns
t_f	Fall time of both SDA and SCL signals			300	ns
t_{VD_DAT}	Data valid time	0		0.9	µs
t_{VD_ACK}	Data valid acknowledge time	0		0.9	µs

5.8 Timing Requirements - I²C Fast Mode Plus

over operating free-air temperature range (unless otherwise noted)

		MIN	TYP	MAX	UNIT
f_{SCL}	SCL clock frequency			1000	kHz
t_{BUF}	Bus free time between STOP and START condition	0.5			µs
t_{HD_STA}	Hold time (repeated) START condition	0.26			µs
t_{SU_STA}	Set-up time for a repeated START condition	0.26			µs
t_{SU_STO}	Set-up time for STOP condition	0.26			µs
t_{HD_DAT}	Data hold time	0			µs
t_{SU_DAT}	Data set-up time	50			ns
t_{LOW}	LOW period of the SCL clock	0.5			µs
t_{HIGH}	HIGH period of the SCL clock	0.26			µs
t_r	Rise time for both SDA and SCL signals			120	ns
t_f	Fall time of both SDA and SCL signals			120	ns
t_{VD_DAT}	Data valid time			0.45	µs
t_{VD_ACK}	Data valid acknowledge time			0.45	µs

5.9 Switching Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Timing Characteristics						
tstartup	Startup time	Time from EN high to V_{OUT} = 95% × V_{ADJ}, V_{ADJ} = 5V		500		µs

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6 Detailed Description

6.1 Overview

The TPS7B7802-Q1 device is a dual channel LDO that operates with a wide input voltage range of 4.5V to 40V (Abs Max V_{IN} of 45V for load dump protection). The device offers protection against a host of fault conditions such as short-to-ground (via current limit), short-to-battery (via RCP), reverse-polarity and thermal overstress (via TSD). The device comes with a fully integrated 10-bit ADC and an I^2C interface. These features enable the user to monitor I_{OUT} & V_{OUT} of both channels, V_{IN}, device junction temperature and diagnostic information on fault conditions. Device output voltage can be set to a value in the range of 2V to 27.4V via I^2C digital programming. For a wider range, external resistors can be used to set a value of the range of 2V to 40V. Alternatively, each of the channels can be configured to operate as a switch.

6.2 Functional Block Diagram

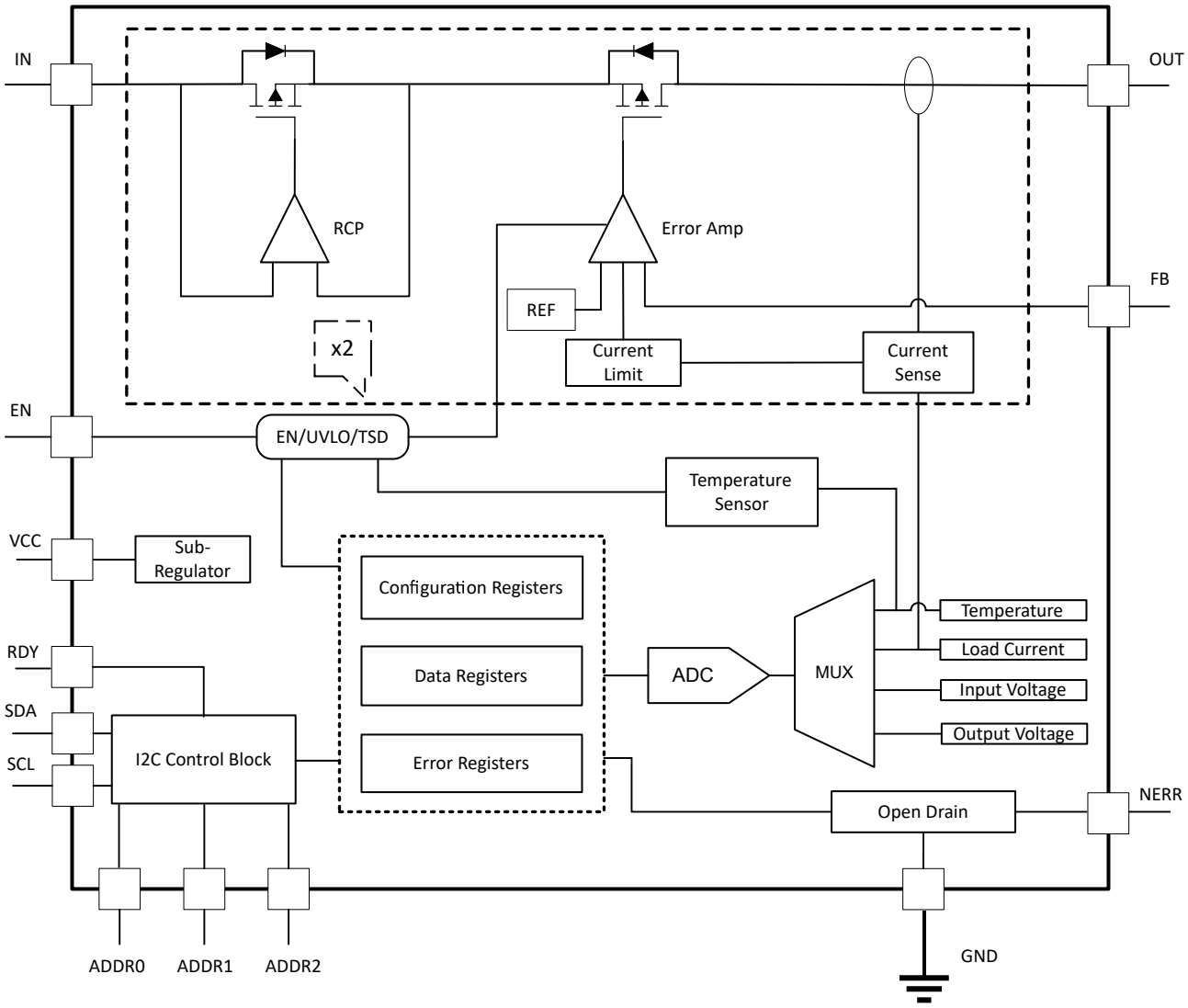

Figure 6-1. Functional Block Diagram

6.3 Feature Description

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6.3.1 Input Under-Voltage Lockout (UVLO)

This device has an internally fixed input under-voltage lockout (UVLO) threshold. When V_{IN} falls below this $UVLO_{(FALLING)}$ threshold, UVLO activates and disables the LDO. This activation makes sure that the regulator is not latched into an unknown state during low input voltage supply. A negative transient that takes the input voltage below the $UVLO_{(FALLING)}$ threshold, shuts the regulator down. When the input voltage recovers beyond the $UVLO_{(RISING)}$ threshold the regulator powers up in the standard power-up sequence.

The values in the UVLO1 and UVLO2 bits of the *Latch Error Register* and *Run-Time Error Register* in the *Register Map* help monitor if a input voltage UVLO event occurs. So long as the channels are enabled, the UVLOx bits toggle to '1' if V_{IN} dips below the $UVLO_{(FALLING)}$ specification.

This device also has a separate digital UVLO specification with regard to I^2C communication and register map reset. The Digital $UVLO_{(Rising)}$ threshold is the minimum input voltage required to begin I^2C communication with the part. V_{IN} has to be higher than this threshold for the user to populate the configuration registers or read out the status & data registers. The Digital $UVLO_{(Falling)}$ is the falling V_{IN} threshold at which the register map resets to the default settings. If V_{IN} falls to a value higher than this specification, the device retains the I^2C settings that are programmed prior to the transient in V_{IN}. The default settings are provided in the *Default settings* table, and are the settings with which the device starts-up unless over-written by the user. A negative transient that takes the input voltage below the digital $UVLO_{(FALLING)}$ threshold shuts the regulator down and resets the register map to the default settings. Any user specified settings in the register map prior to this transient are not recoverable.

$UVLO_{(FALLING)}$, $UVLO_{(RISING)}$, digital $UVLO_{(Rising)}$ and digital $UVLO_{(Falling)}$ parameters are all specified in the *Electrical Characteristics table*

6.3.2 Enable

The enable pin for this device is an active high pin. With sufficient input voltage provided ($V_{IN} \geq 4.5V$), for the device to be enabled, two conditions have to be satisfied. The voltage on the EN pin has to be higher than the $V_{EN\ H}$ threshold and the part must also be digitally enabled. To digitally enable the part, the EN bits in the *Configuration-3 register* of the *Register Map* have to be set to 1. When the device is regulating, toggling the respective digital ENx bit to 0 disables the appropriate output channel. Taking the EN pin voltage lower than $V_{EN\ L}$ threshold disables both the output channels, regardless of the digital ENx bit settings. Disabling the device, as well as the internal ADC, reduces the quiescent current consumption of the device to less than the $I_{DISABLED}$ specification. To disable the internal ADC, set the ADC-EN bit in the configuration-3 register of the register map to 0.

$V_{EN\ H}$, $V_{EN\ L}$ and $I_{DISABLED}$ are all specified in the *Electrical Characteristics*.

6.3.3 Output Voltage Setting

The TPS7B7802-Q1 device allows the user to setup the output voltage of each of the channels in two ways, either externally or internally. To setup V_{OUTX} externally, use external feedback resistors between the FBx and OUTx pins of the corresponding channel. The range of output voltage with this method is $2V \leq V_{OUTX} \leq 40V$. The FBx bit in the *Configuration Register 3* of the *Register Map* must be programmed to '1' to externally setup the channel output voltages. Connecting the FBx pin to ground, configures the corresponding channel of the device as a switch.

Setting up the output voltages internally, via I2C, eliminates the need of external resistors. The FBx bits, described above, must be programmed to '0'. An output voltage value in the range $2V \leq V_{OUTX} \leq 27.4V$ must then be selected for both channels. The selected values must be programmed into the *Configuration Register 0* and *Configuration Register 1* of the register map. The device allows the user to configure each of the channels as a switch via I^2C. See the *Register Details* section for more details. In this mode the FBx pins are disconnected from the internal circuitry.

6.3.4 Soft Start

The device starts-up in a current limit mode, which allows the output voltage of the both channels to ramp-up in a controlled manner. The ramp rate of the appropriate output channel is given by :

$$\frac{\Delta V_{OUT\ X}}{\Delta t} = \frac{I_{STARTUP\ CL}}{C_{OUT}} \quad (1)$$

The start-up current limit value of both channels are independently programmable in the *Configuration-0* and *Configuration-1* registers. A current value in the range 25mA ≤ $I_{STARTUP\_CL}$ ≤ 400mA must be selected for each channel. See the *Register Details* section for additional details. For the device startup to be successful, for each channel, the $I_{STARTUP\_CL}$ value selected must be higher than the expected steady state load current.

6.3.5 Voltage Monitoring

The TPS7B7802-Q1 device offers input and output voltage monitoring of each channel. The device comes with a fully integrated 10-bit ADC, which helps sample each of these parameters. The digital measurements of V_{IN}, V_{OUT1} and V_{OUT2} are stored in and read from the *Input Voltage Measurement*, *Output Voltage Measurement Ch-1* and *Output Voltage Measurement Ch-2* registers of the *Register Map*, respectively. The accuracy of these measurements is specified in the *Electrical Characteristics*.

The TPS7B7802-Q1 device also helps inform the user of under & over-voltage conditions on each of the output channels. The OUTUVx and OUTOVx bits of the *Latch Register* and *Run-Time Register* in the register map, help infer the status of V_{OUT} in both channels. The bits retain a value of '0', only if the output voltage remains within the over voltage and under voltage PG thresholds specified in the *Electrical Characteristics*. If the output voltage on either or both channels goes below the under voltage PG threshold, then the appropriate OUTUVx bit toggles to '1'. If the output voltage on either or both channels goes beyond the over voltage PG threshold, then the appropriate OUTOVx bit toggles to '1'. See the *Run-Time* and *Latch* register description sections for more details.

6.3.6 Current Monitoring

The TPS7B7802-Q1 device allows the user to monitor the load current, in both output channels, in multiple ways. The 10-bit ADC measurements of the output currents are accessible from specific registers listed in the *Register Map*. For load currents in the range 0mA ≤ I_{OUT} ≤ 400mA, the measurements are stored in the *Ch-1 High Range Current Measurement* & *Ch-2 High Range Current Measurement* registers. The resolution of the measurements in these registers is 390µA. For load currents in the range 0mA ≤ I_{OUT} ≤ 25mA, the digital measurements are stored in the *Ch-1 Low Range Current Measurement* & *Ch-2 Low Range Current Measurement* registers. Although there is an overlap in the current ranges, at light loads, we recommend that the low current range registers be used to retrieve the measurements. The resolution of the measurements in these registers is lower at 25µA. See the *Register Details* section for additional details.

The TPS7B7802-Q1 offers open load detection. Open load threshold in the range 0mA ≤ $I_{OL\ TH}$ ≤ 15mA, must be independently selected for each channel and programmed into the *Configuration Register-2*. If the load current in either or both channels falls below the selected thresholds, the device regards such a condition as an open load. The appropriate OLx bit in the *Latch Error Register* and *Run-Time Error Register* in the register map toggle to '1'. See the Configuration Register-2 description *section* for additional details.

The TPS7B7802-Q1 also offers overload detection. An over-current warn threshold in the range 10mA ≤ $I_{WARN\ TH}$ ≤ 310mA, must be independently selected for each channel and programmed into the *Configuration - 0* and *Configuration - 1* registers. If the load current in either or both channels exceeds the selected thresholds, the device regards such a condition as an overload. The appropriate IWRNx bit in the *Latch Error Register* and *Run-Time Error Register* in the register map toggle to '1'. See the *Register Details* section for additional information.

6.3.7 Reverse Current Protection

Fault conditions occur in an automotive environment that result in the output voltage exceeding the input voltage. Example situations include LDO output shorting to a power supply that is higher than V_{IN} or if V_{IN} suddenly collapses because of a power loss. Both these situations leave V_{OUT} at a higher value than the V_{IN}. In typical LDOs, such scenarios results in the flow of a large reverse current and potentially damaging the silicon through heating, electromigration or latch-up events. The TPS7B7802-Q1 device has an integrated protection feature that blocks the flow of reverse current. A topology containing back-to-back P-channel MOSFETs are used in this device, one of which serves as the 'blocking' FET and the other as the 'pass' FET. The gate of the blocking

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FET is driven by a voltage comparator, which shuts down the FET if V_{OUT} is detected to be higher than V_{IN}. The threshold at which the comparator trips and the response time of this protection feature are specified in the I_R section of the *Electrical Characteristics* table. The deglitch time period of this comparator is typically around 100µs. The reverse voltage comparator along with the orientation of the body diode of the blocking FET protect the device against the flow of reverse current. The above described components are all shown in the *Functional Block Diagram*.

Monitor the status of the IREV1 and IREV2 bits of the *Latch Error Register* and *Run-Time Error Register* in the *Register Map*. The appropriate IREVx bit toggles to '1', if the V_{OUT} of the channel exceeds V_{IN} by the threshold value. The device continues to monitor V_{IN} and V_{OUT}, does not latch-off or require an EN toggle. The device resumes normal regulation once the fault condition is removed.

6.3.8 Current Limit

To protect the device and downstream components from overcurrent flow, the TPS7B7802-Q1 device comes with an internal current limiting protection circuit. The device also allows the user to program the current limit value from the range 25mA ≤ I_{CL} ≤ 400mA, independently for each channel. The selected value must be programmed into the *Configuration Register 2* section of the *Register Map*. See the *register description section* for more details. The device implements a brick-wall scheme current limit. When the device hits a current limit condition in either or both channels and sources the programmed I_{CL} current, the output voltage is not regulated. The load impedance determines the output voltage value.

Monitor the status of the ILIM1 and ILIM2 bits of the *Latch Error Register* and *Run-Time Error Register* in the register map. The appropriate ILIMx bit toggles to '1', if a current limit condition is detected either or both channels of the device.

6.3.9 Junction Temperature Monitoring

The TPS7B7802-Q1 device allows the user to monitor the junction temperature in two different ways. The 10-bit ADC measurement of the junction temperature is stored in the *T_J measurement register* of the *Register Map*. See the *register description section* for more details. The TPS7B7802-Q1 device also offers over-temperature detection. An over-temperature warn threshold must be programmed into the *Configuration Register 3*. If the junction temperature of the device exceeds this programmed threshold, the device regards this as a over-temperature event. The TWRN bit in the *Latch Error Register* and *Run-Time Error Register* in the register map toggle to '1' when such a event happens. See the register description *section* for additional details.

6.3.10 Thermal Protection

Once the junction temperature rises to approximately 175℃, a thermal protection circuit activates and disables the device. The TSD bit in the *Latch Error Register* and *Run-Time Error Register* in the *Register Map* toggle to '1' when such a event happens. See the register details *section* for additional details. This feature helps prevent the temperature within the device from reaching unsafe levels. The disabling allows the part to cool, and once the junction temperature falls to approximately 160℃, the device is enabled again. Although the device is enabled at such high temperatures, the device parameters and performance are specified up to a junction temperature of 150°C. Power dissipation, thermal resistance, and ambient temperature are the parameters that determine if the thermal protection circuit becomes enabled. When enabled, unless the power dissipation or the ambient temperature (or both) are reduced, the protection circuit continues to cycle the part between on and off states.

The internal protection circuitry of the TPS7B7802-Q1 is designed to protect against overload conditions. This circuitry is not intended to replace proper heat sinking. Continuously running the TPS7B7802-Q1 into thermal shutdown degrades device reliability.

6.3.11 Protection Features and Diagnostic Capabilities

Below is the summary list of protection features that are built into the TPS7B7802-Q1 device :

1. Reverse Polarity Protection : The -40V absolute maximum rating of the IN pin helps the device survive a possible incorrect battery terminals connection.
2. Current Limit/Short to ground Protection : The device provides protection against the flow of excess current. See the *Current Limit* section for additional details.

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3. Thermal Protection : The device provides protection against excess rise in junction temperature. See the *Thermal Protection* section for additional details.
4. Short to Battery Protection : The 45V absolute maximum rating of the OUT pin and the *Reverse Current Protection* feature helps the device survive a possible output short-to-battery event.

Below is the summary list of the fault conditions that the TPS7B7802-Q1 device helps detect :

1. Output under and over voltage conditions : The OUTUVx and OUTOVx bits in the error registers help monitor the under and over voltage events respectively in each channel. See the *Voltage Monitoring* section for additional details.
2. Input under voltage : The UVLO bits in the error register helps inform the user if the input voltage has collapsed below the UVLO threshold. See the *UVLO* section for additional details.
3. Over load and open load conditions : The ILIMx, IWRNx and OLx bits in the error registers help monitor current limit, excess load current and open load conditions respectively. See the *Current Limit* and *Current Monitoring* sections for additional details.
4. Reverse current flow : The IREVx bits in the error registers helps inform the user if there is reverse current flow. See the *Reverse Current Protection* section for additional details.
5. Excess Junction Temperature : The TSD and TWRN bits in the error registers help monitor thermal shutdown and excess junction temperature conditions respectively. See the *Thermal Protection* and *Junction Temperature Monitoring* sections for additional details.

6.3.12 NERR Pin

The TPS7B7802-Q1 device has an open-drain based NERR pin. This pin assumes a logic low state when the device detects any of the fault conditions listed in the *Protection Features and Diagnostic Capabilities* section. The user has the flexibility to configure the NERR pin to either follow the runtime profile of the fault condition or assume a latched state. Setting the 'Latch' bit in the *Configuration Register 3* to '0' makes the NERR pin follow the runtime profile of the fault condition. The pin assumes a logic low level if a fault condition occurs and recovers to a logic high if the fault condition is removed. Setting the 'Latch' bit to '1' makes the NERR pin assume a latched logic low state if a fault condition occurs. The pin retains the latched state even if the fault condition is removed. To clear the latched state, the fault condition must be removed and followed up by any one of the actions below:

- Overwriting the Latch Error Register with the appropriate digital word to reset the '1's to 0. See the *Latch Error Register Field Descriptions* section for more details.
- Power cycling the device (or taking V_{IN} below Digital $UVLO_{FALLING}$ threshold).
- Using the SWRRST in control byte 1. See the *Read Cycle* section for more details.

The *Error Mask Register* in the *Register Map* helps hide or mask the fault conditions from having any impact on the NERR pin. To use this feature, the user must set to '1' the bits corresponding to the appropriate fault conditions in the Error Mask Register. If these selected fault conditions occur, the NERR pin does not assume a logic low state. For example,with OUTOV1 bit in the Mask Register set to '1', the NERR pin does not go to logic-low even if an over-voltage event occurs on V_{OUT1}. However, the OUTOV1 bits in the *Latch Register* and *Run-Time Register* continue to get updated if an over-voltage event occurs on channel-1 output. See the *Error Mask Register Field Descriptions* for more details.

6.3.13 Blanking Time

The TPS7B7802-Q1 device offers a programmable blanking time feature, to help prevent the device from flagging transient events as faults. Blanking time initiates every time a channel is fully enabled or when the device recovers from thermal shutdown. The blanking time period for the device is programmable in the range $0ms \le t_{BLANKING} \le 85ms$. This is a device level setting, and the two channels cannot have independent $t_{BLANKING}$ settings. See the Configuration Register 3 Field Descriptions section for additional details. During the blanking time period, the bits in the Latch Error Register and Run-Time Error Register do not get updated even if the corresponding fault conditions occur. The bits get updated only if the fault conditions continue to exist after the blanking time period has expired. Only updates to the TSD, UVLO1 and UVLO2 bits in these registers are

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exempt from blanking time. Please note that the blanking time is initiated every time a channel is enabled. Thus, if the two channels are enabled at separate times, then device blanking time period initiates/resets for each channel enable separately.

6.3.14 Switch Mode

The device channels can be configured to operate as a switch via I^2C. For this, the appropriate FBx bit in the *Configuration Register 3* of the *Register Map* must be programmed to '0'. This disconnects the FBx pins on the package from the internal circuitry. The output voltage Ch-x field in the appropriate *Configuration Register 0/1* must also be populated with the digital word 0xFF. See the *Register Details* section for more details.

To externally configure the device as a switch, the appropriate FBx bit in the *Configuration Register 3* must be programmed to '1'. The appropriate FB pin on the package must then be grounded.

In the switch mode, the device is still able to perform diagnostics for open load, current limit and reverse current fault conditions. The device does not register this mode as an over-voltage or under-voltage fault event.

6.4 Device Functional Modes

Table 6-1 shows the conditions that lead to the different modes of operation. See the *Electrical Characteristics* table for parameter values.

Table 6-1. Device Functional Mode Comparison

OPERATING MODE	PARAMETER				
	V_{IN}	V_{EN}	I_{OUT}	T_J	I^2C Setting
Normal operation	V_{IN} > Max {$V_{OUT1\ (Nom)}$, $V_{OUT2\ (Nom)}$} + V_{DO} and $V_{IN} \geq V_{IN(min)}$	$V_{EN} > V_{EN\ H}$	Max{I_{OUT1}, I_{OUT2}} ≤ 300mA	$T_J \leq 150°C$	For Channel X : Set Bit ENX = 1 in configuration register - 3
Dropout operation (either of the conditions in the V_{IN} or I^2C setting columns, when true, puts the device in dropout)	For Channel X to be in dropout : $V_{IN(min)} < V_{IN} < V_{OUTX\ (Nom)} + V_{DO}$. For both channels to be in dropout : $V_{IN(min)} < V_{IN} <$ Min {$V_{OUT1\ (Nom)}$, $V_{OUT2\ (Nom)}$} + V_{DO}	$V_{EN} > V_{EN\ H}$	Max{I_{OUT1}, I_{OUT2}} ≤ 300mA	$T_J \leq 150°C$	For Channel X : Set bit ENX = 1 and Output Voltage Ch-X bits to 0xFF in the configuration registers.
Disabled (any true condition disables the device)	$V_{IN} < V_{UVLO\ (Falling)}$	$V_{EN} < V_{EN\ L}$	Not applicable	$T_J > T_{SD\ (shutdown)}$	For Channel X : Set Bit ENX = 0 in configuration register - 3

6.4.1 Normal Operation

The individual channels of the device provide a regulated when the following conditions are met

- Sufficient input voltage must be provided. V_{IN} must be higher than the nominal/target output voltage plus the required dropout voltage. Both conditions, $V_{IN} \geq 4.5V$ and $V_{IN} > V_{OUT(Nom)} + V_{DO}$, must be satisfied.
- The load current in the corresponding channel must be less than the programmed current limit value, $I_{OUT} < I_{CL}$.
- The device junction temperature T_J is less than 150°C.
- The device must be properly enabled. The enable pin voltage must be higher than the enable rising threshold, $V_{EN} > V_{EN\ H}$. The enable bit if the corresponding channel in the *Register Map* must be set to 1. See the *Enable* section for more details.

6.4.2 Dropout

If V_{IN} is lower than the nominal/target channel V_{OUT} plus the required dropout voltage, the device channel operates in dropout mode. This is conditional on all other criteria being met for normal operation. In dropout mode, the output voltage is no longer in regulation and the transient performance (line & load) significantly degrades. The pass transistor operates in the triode/ohmic region, V_{OUT} tracks V_{IN} and the channel effectively behaves as a switch. The PSRR current sense accuracy also degrades in dropout mode. See the *Switch Mode*

section for more details on how to operate the device in switch mode. While operating in dropout, if sufficient V_{IN} provided, the device exits dropout and enters regulation mode. The pass transistor transitions into saturation from the triode region. During this short transition period when the device is exiting dropout, the output voltage potentially has a significant overshoot.

6.4.3 Operation with V_{IN} < 4.5V

See the *Input Under-Voltage Lockout (UVLO)* section for details on device performance when V_{IN} is less than 4.5V.

6.4.4 Disable

To selectively disable individual channels, set the appropriate ENx bit in the *Configuration-3 register* of the *Register Map* to 0. Taking the EN pin voltage lower than $V_{EN\ L}$ threshold, disables both the output channels regardless of the digital ENx bit settings. The device also disables when V_{IN} falls below the $UVLO_{(FALLING)}$ threshold. When disabled, the quiescent current consumption of the device reduces. The internal ADC must also be disabled for the quiescent current consumption of the device to reduce less than $I_{DISABLED}$ specification. The $V_{EN\ L}$, $UVLO_{(FALLING)}$ and $I_{DISABLED}$ parameters are specified in the *Electrical Characteristics*.

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6.5 Programming

6.5.1 I²C Interface

The TPS7B7802-Q1 device has an integrated inter-integrated circuit (I^2C) compatible interface for serial communication. I^2C is a two-wire serial communication protocol. The two wires are called the serial data line (SDA) and serial clock line (SCL). The SCL line carries the clock signal and the SDA line carries the Data packets. The Protocol enables communication between one or more controller devices (for example, MCU) and target devices (for example, ADC, LDO, and so forth). Every target device is associated with a unique address, and by sending this address on the SDA line, the controller can communicate with the appropriate target device. The TPS7B7802-Q1 device is designed to be configured as a target device only.

Devices on the I^2C bus drive the bus lines low by connecting the lines to ground; the devices never drive the bus lines high. Instead, the bus wires are pulled high by pullup resistors to a common voltage level VDD; thus, the bus wires are always high when a device is not driving the lines low. The SDA line is used to transmit data to and from target devices and this is done synchronously with a clock signal that is carried by the SCL line. This is a half-duplex form of communication since at any given time only a single controller or target can be transmitting data. The clock signal on the SCL line can be generated only by the controller. The SDA line however can be pulled low by both the controller and target. All participating devices have SDA and SCL pins that are open-drain.

The Open Drain connections on the SDA/SCL lines occur through NMOS transistors. An example bus is shown in Figure 6-2.

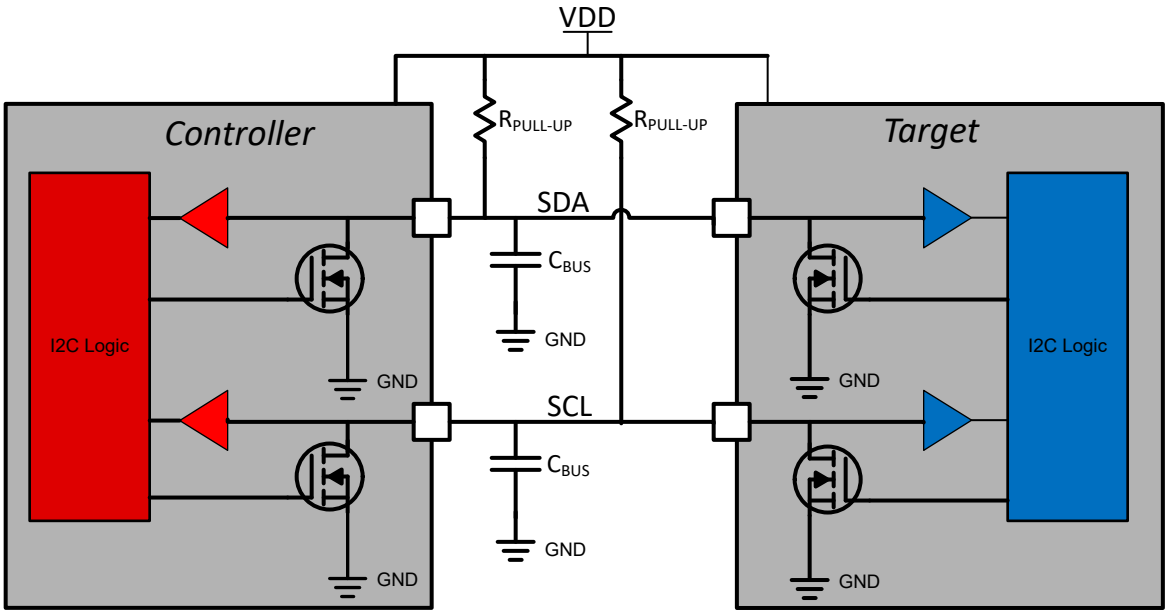

Figure 6-2. Typical I^2C Bus

The Data and Clock transmission occurs in Binary format and the voltage on the SDA/SCL line is set high (to VDD) or low (to GND/V_{OL}) by turning the NMOS off or on. A typical voltage profile on the SDA/SCL lines is show in Figure 6-3.

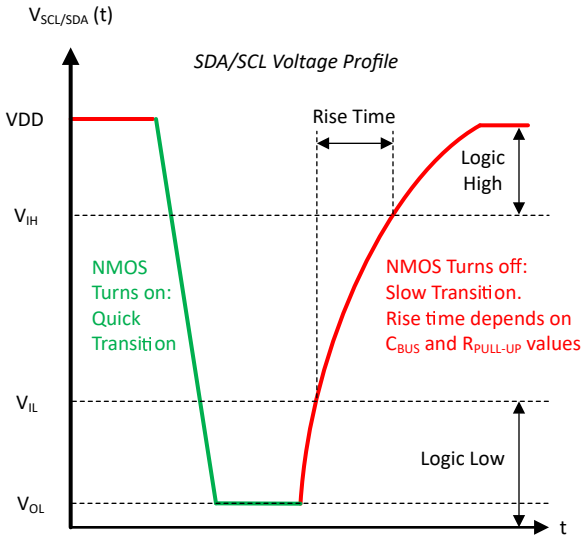

Figure 6-3. SDA/SCL Voltage Profile

When the NMOS turns on, the line is pulled to a low voltage level. Due to the finite resistance of the NMOS device, the voltage on the line settles at V_{OL}. This is typically a fast transition. When the NMOS turns off, the line is pulled to VDD via $R_{PULL-UP}$. This transition from low to high is slower and depends also on C_{BUS}, the amount of capacitance on the bus line.

On the SCL/SDA lines, TPS7B7802-Q1 interprets any voltage above V_{IH} to be a logic high and below V_{IL} to be a logic low. The pull-down drive strength of the NMOS devices (I_{SINK}), $R_{PULL-UP}$ and C_{BUS}, all play a critical role in determining the speed of communication. The $R_{PULL-UP}$ value is a trade-off between speed and power consumption. Small values reduce $R_{PULL-UP}$ *C_{BUS} delay and improve speed. Larger resistor values increase the delay but reduce power consumption. I_{SINK} values scale with size of the NMOS devices.

6.5.1.1 I²C Interface Speed

The TPS7B7802-Q1 device can support three different I²C speed modes. The names of the modes, speeds and some electrical specification details are provided in Table 6-2 below.

Table 6-2. I²C Speed Mode details

I²C Mode	Maximum Bit Rate	I²C Standard		TPS7B7802-Q1	
		Min I_{SINK}	Max C_{BUS}	Min I_{SINK}	Max C_{BUS}
Standard Mode	100Kbps	3mA	400pF	3mA	400pF
Fast Mode	400Kbps	3mA	400pF	3mA	400pF
Fast Mode Plus	1Mbps	20mA	550pF	3mA	*120pF*

To support a speed of 1MHz on a line carrying C_{BUS} = 550pF, I2C specifications recommended that I_{SINK}≥ 20mA. However, the NMOS transistors in TPS7B7802-Q1 are not sized carry I_{SINK} values greater than 6mA. This is why the C_{BUS} on the SDA/SCL lines that TPS7B7802-Q1 can support in the Fast Mode Plus mode (1MHz) proportionally reduces to maximum value of 80pF. For the standard and fast modes, TPS7B7802-Q1 is compliant with the I²C specifications.

6.5.2 I²C Data Transfer Protocol

I²C communication is always initiated by the controller device. Every participating device (controller and Target) need to have a unique address. Up to 8 TPS7B7802-Q1 devices can be used in a system since this device has 3 ADDR pins and 8 unique addresses can be configured. Upon startup, the controller is expected to address the TPS7B7802-Q1 device and configure the internal registers by writing data into them. The controller can begin communication only when the bus is idle. The bus is considered idle when both the SDA and SCL lines are high

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after a STOP condition. A summary of the process involved in I^{2}C communication between the controller and target is provided below:

1. Controller sending data to target
   - Controller initiates a START condition, addresses a target and designates the target as a receiver.
   - Controller, acting as a transmitter, sends data to the target (receiver).
   - Controller terminates the data transfer with a STOP condition.
2. Controller receiving Data from Target
   - Controller initiates a START condition, addresses a target and designates the target as a transmitter.
   - Controller then addresses specific register in Target to read data from.
   - Target, acting as a transmitter, sends data to the Controller (receiver).
   - Controller terminates the data transfer with a STOP condition.

6.5.2.1 START and STOP

With the bus idle and both the SDA & SCL lines high, to initiate a ***START*** sequence, the controller pulls the SDA low and then pulls the SCL line low. This sequence allows the controller to claim control over the communication line. After the data transfer has been completed, to terminate communication, the controller begins the ***STOP*** sequence by first releasing the SCL line allowing the line to be pulled high, followed by releasing the SDA line to a logic high level. This releases the bus for other controllers to begin communication. The controller can issue another START after the data transfer to retain control of the SDA line. This is called a ***repeated START*** sequence, and can be used in the place of back-to-back STOP START sequences.

6.5.2.2 Logical 1's and 0's

I^{2}C uses binary bits, the sequence of ones and zeros, to transmit data. A logical one can be sent when the SDA line is released and pulled high to VDD using the pullup resistor. Similarly, a logical zero can be sent when the SDA line is pulled low to GND. The ones and zeros are received when the SCL is pulsed. For the bit to be valid, the voltage level of the SDA line cannot change between a rising and falling edges of the SCL line. Changes in SDA between the rising and falling edges of SCL are interpreted as START or STOP conditions on the I^{2}C bus.

6.5.2.3 Data Format

I^{2}C communication on the SDA line can be broken up into frames. Each frame is made up a byte of information. Every byte is made up of 8 bits. The Byte can carry the address of a Target, address of a register within the Target, or Data that needs to be written to or read from a Target. The data is always transmitted MSB first.

In the address byte, the seven most significant bits carry the address information. The LSB of the address byte is the R/$\overline{W}$ bit and this helps designate the target to be a transmitter (R/$\overline{W}$ bit set to 1) or a receiver (R/$\overline{W}$ bit set to 0).

Every byte of data is followed by one ACK (Acknowledge) bit where the receiver pulls the SDA line down during an SCL pulse. The ACK signal allows the receiver to indicate to the transmitter that the byte is received successfully and that communication can continue. Figure 6-4 shows an example displaying a START sequence, an address frame, a data frame, ACK and a STOP sequence.

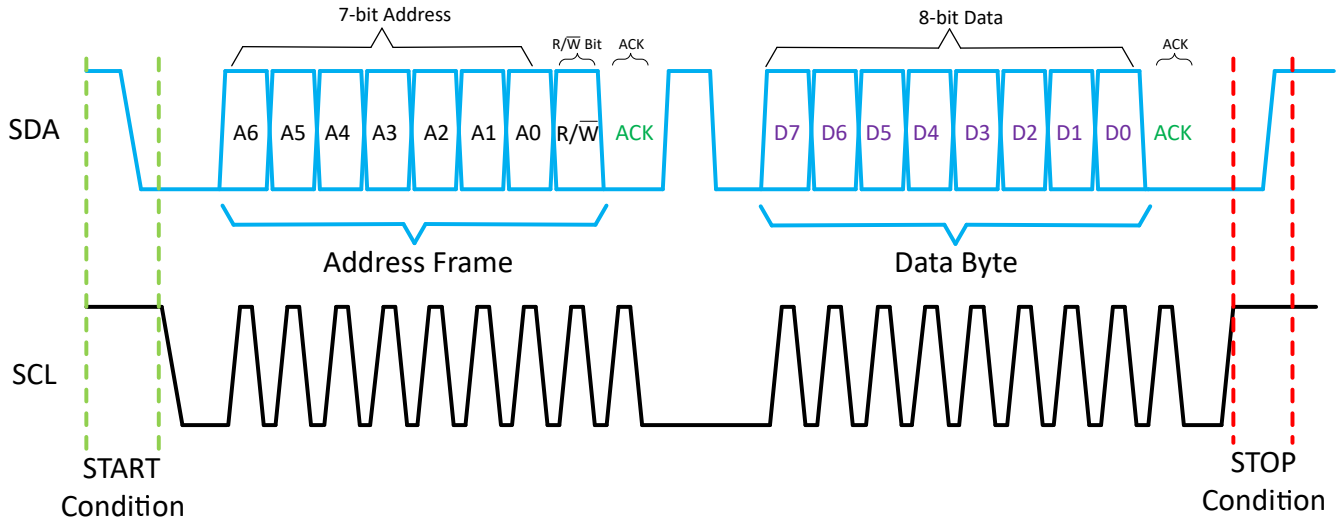

Figure 6-4. Typical Transmission Sequence

If the SDA line remains high after a byte, then this condition is called NACK (No ACK). Some situations that result in a NACK are listed below:

- No receiver is present on the bus with the transmitted address, so there is no device to respond with an acknowledge.
- If the receiver is performing some real-time function, then communication with the controller cannot occur.
- If the receiver gets data or command that is not understandable.
- If the receiver gets more bits than can be accepted.
- A controller-receiver must signal the end of the transfer to the target transmitter.

6.5.3 Address Frame

After initiating the START, the controller must send the 7-bit address to begin communication. For TPS7B7802-Q1 device, the first 4 of the 7 address bits (MSBs) are factory preset to '1001'. The remaining three LSB bits of the address bits can mimic the logic levels applied the three ADDRX pins of TPS7B7802-Q1, allowing the controller to communicate with up to 8 TPS7B7802-Q1 devices. Figure 6-5 shows an example address frame that include the START and ACK sequences.

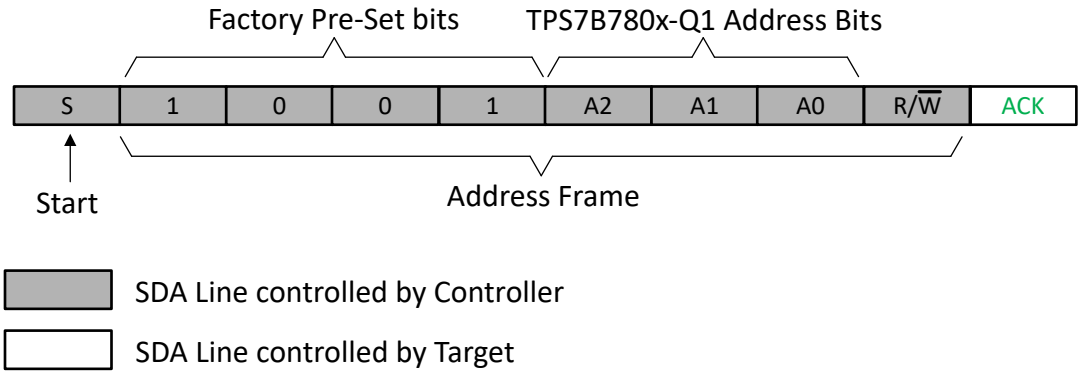

Figure 6-5. Address Frame Structure

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6.5.4 Write Cycle

The TPS7B7802-Q1 device must be setup correctly by writing into the four configuration registers (CFGR0-3). For a detailed description on all the registers, please refer to the Register Map section. Table 6-3 lists the addresses and Read/Write (R/W) accessibility of all the registers in the TPS7B7802-Q1 device. The registers listed in Table 6-3 are 16 bits in size. Therefore 2 bytes of data can be read from or write into (if permissible) these registers.

Table 6-3. Register Map Summary

Index	Register Name	Address (Hex)	Address (Binary)				Read/Write
			A3	A2	A1	A0	
1	CFGR0	0	0	0	0	0	R/W
2	CFGR1	1	0	0	0	1	R/W
3	CFGR2	2	0	0	1	0	R/W
4	CFGR3	3	0	0	1	1	R/W
5	Data Register for device V_{IN}	4	0	1	0	0	R
6	Data Register for Ch1V_{OUT}	5	0	1	0	1	R
7	Data Register for Ch1I_{OUT-H}	6	0	1	1	0	R
8	Data Register for Ch1I_{OUT-L}	7	0	1	1	1	R
9	Data Register for Junction Temperature	8	1	0	0	0	R
10	Data Register for device V_{IN}	9	1	0	0	1	R
11	Data Register for Ch2V_{OUT}	A	1	0	1	0	R
12	Data Register for Ch2I_{OUT-H}	B	1	0	1	1	R
13	Data Register for Ch2I_{OUT-L}	C	1	1	0	0	R
14	Latched Status Register	D	1	1	0	1	R/W
15	Run Time Status Register	E	1	1	1	0	R
16	Mask Register	F	1	1	1	1	R/W

After addressing the desired target, to write into a particular register, we recommend that the 8-bit frame ‘Control Byte 0’ be utilized. Figure 6-6 shows the structure of this frame and Table 6-4 describes the function of each bit.

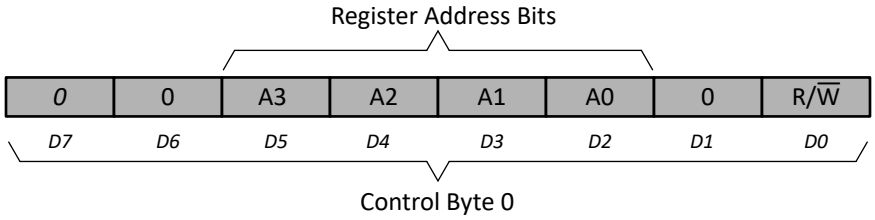

Figure 6-6. Structure of Control Byte 0

Table 6-4. Control Byte 0 Description

Bit	Field	Description
D7	Control Byte ID	0: Control Byte 0 (This Byte helps the user read/write data into registers). 1: Control Byte 1 (This Byte helps perform specific ADC functions).
D6	NA	Must be '0' for normal operation.
D5	A3	Register Address Bits
D4	A2	
D3	A1	
D2	A0	
D1	NA	Must be '0' for normal operation.
D0	R/$\overline{W}$	1: Data from register whose address correlates to the address bits can be read. 0: Data can be written into register whose address correlates to the address bits.

Table 6-5 lists an example configuration of the TPS7B7802-Q1 device. Figure 6-7 describes the process of populating the four configuration registers to get the configuration listed in Table 6-5. The Mask and the Latched Status register can be written into, in a similar way. The hex/binary codes corresponding to the various target values and the composition of configuration registers CFGR0-3 are provided in the Register Map section.

Table 6-5. Example setup

Parameter	Channel 1		Channel 2	
	Target Value	Binary Code	Target Value	Binary Code
Current Limit at Start-up	200mA	0111	300mA	1011
Load current warn threshold	310mA	1111	250mA	1100
Output Voltage	12V	0110 0100	10V	0101 0000
Open load threshold	10mA	1010	15mA	1111
Current Limit	350mA	1101	400mA	1111
Junction Temp warn threshold	130°C	110		
ADC Enable	Enable	1		
Runtime/Latch Error	Runtime	0		
Blanking Time	8.5ms	100		
Digital Enable	Enable	1	Enable	1
External Feedback setting	No	0	No	0

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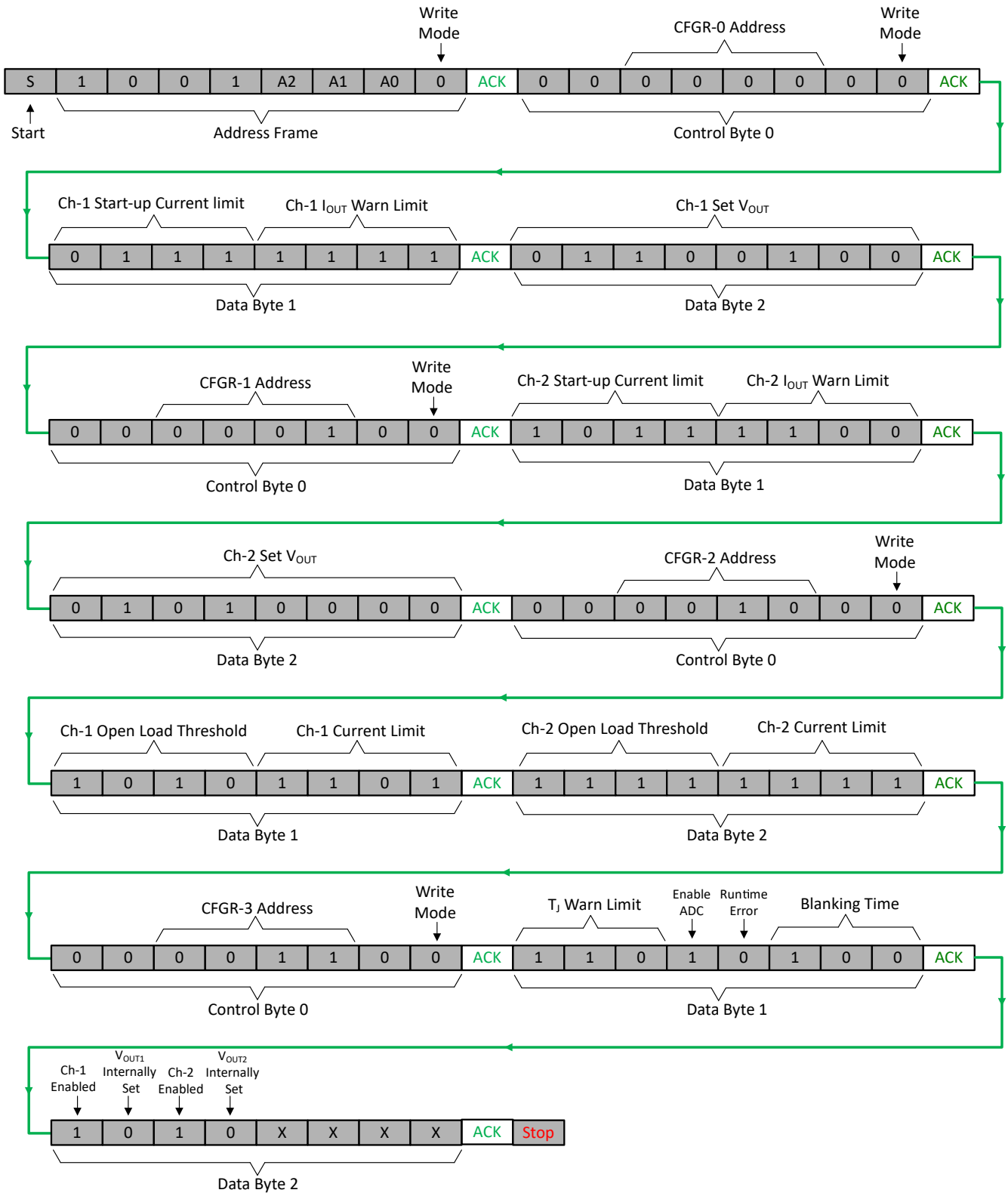

Figure 6-7. Write Cycle Example

The write accessible registers can be populated in any sequence and the STOP (or repeated START) sequence can be initiated at any time. To begin the re-write after a STOP, the target has to be addressed again the write cycle described above has to be repeated.

If data is attempted to be written into a read only accessible register, the TPS7B7802-Q1 device responds with a NACK. This is shown in Figure 6-8, where Control Byte 0 is sent with a write instruction to a read-only register (V_{IN} register of LDO Ch-1) and TPS7B7802-Q1 the device responds with a NACK. The TPS7B7802-Q1 device continues to respond with a NACK, until the controller issues a STOP followed by a correct address frame.

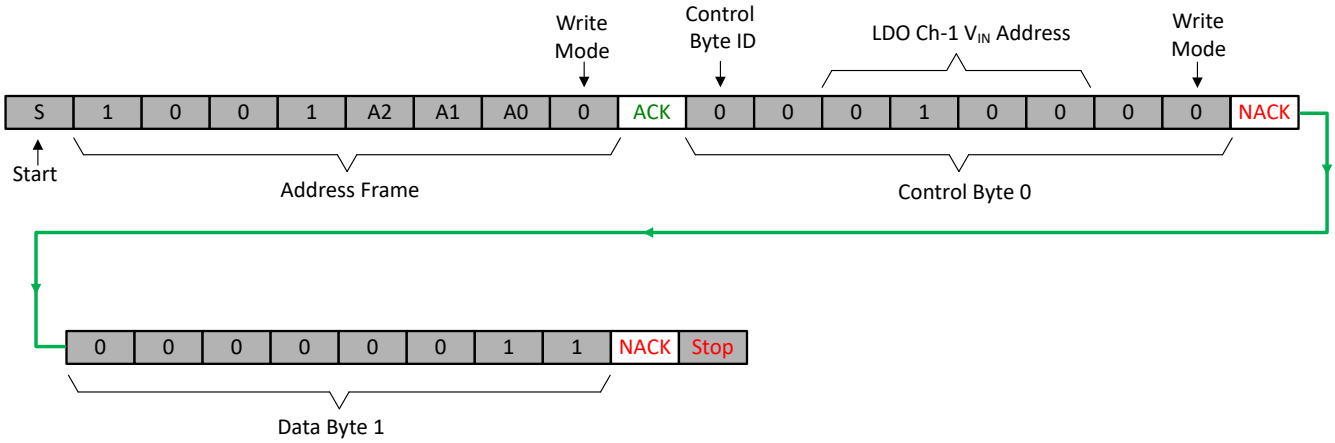

Figure 6-8. Incorrect Write Cycle

6.5.5 Read Cycle

All registers described in the register map of TPS7B7802-Q1 are read accessible. Many of them carry ADC measurements of Voltages, Currents and Temperature. The 8-bit frame 'Control Byte 1' can be used to provide different types of instructions to the ADC to populate these registers. Figure 6-9 shows the structure of this Control Byte 1 frame and Table 6-6 describes the function of each bit.

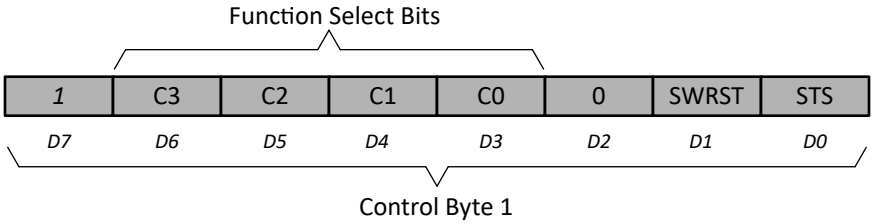

Figure 6-9. Control Byte 1

The MSB value of the frame immediately following the address ACK (see Figure 6-8 and Figure 6-10) allows the TPS7B7802-Q1 to distinguish between Control Byte 1 (bit = 1) and Control Byte 0 (bit = 0). For both Control Byte 0 & 1, the address frame needs to be sent in the write cycle mode (LSB of address frame = 0).

Table 6-6. Control Byte 1 Description

Bit	Field	Description
D7	Control Byte ID	0: Control Byte 0 (This Byte helps the user read/write data into registers). 1: Control Byte 1 (This Byte helps perform specific ADC functions).
D6	C3	ADC Function Selection Bits
D5	C2	
D4	C1	
D3	C0	
D2	NA	Must be '0' for normal operation.
D1	SWRST	Software reset bit. All registers are set to default values if a '1' is written to this bit.

Table 6-6. Control Byte 1 Description (continued)

Bit	Field	Description
D0	STS	Stop Bit for Data converter functions. If this Bit is set to '1', the data converter functions are aborted. This does not reset any registers.

Depending on the function bits settings, the ADC can be instructed to make a one-time or continuous measurement of the parameters and update the corresponding registers. Table 6-7 below provides the different functions the ADC can perform and the time required to do so and populate the registers.

Table 6-7. ADC Functions

ADC Function Selection Bits				C3C0 (Decimal)	Function Description	Measurement Time
C3	C2	C1	C0			
0	1	0	0	4	Measure all Device Vitals: sequential single measurement of V_{IN}, V_{OUT1}, I_{OUTH1}, I_{OUTL1} , T_J, V_{IN}, V_{OUT2}, I_{OUTH2} & I_{OUTL2}	50µS
0	1	0	1	5	Measure LDO Ch-1 Vitals: sequential single measurement of V_{IN1}, V_{OUT1}, I_{OUTH1}, I_{OUTL1} & T_J	25µS
0	1	1	0	6	Measure LDO Ch-2 Vitals: sequential single measurement of V_{IN2}, V_{OUT2}, I_{OUTH2}, I_{OUTL2} & T_J	25µS
0	1	1	1	7	Measure Temperature Only	10µS
1	0	0	0	8	Measure LDO1 Vitals Continuously*	*n**25µS
1	0	0	1	9	Measure LDO2 Vitals Continuously*	*n**25µS
1	0	1	0	10	Measure all device vitals continuously.	*n**50µS

Figure 6-10 below describes an example where control byte 1 has been used to instruct the ADC to make a one-time measurement of all the vitals of LDO Ch-1 and update/populate registers 5-9 of Table 6-3 . After receiving the ACK corresponding to the Control Byte 1 from the target, the controller must wait for a period of time to allow the ADC to populate the appropriate registers. The 'Measurement Time' column of Table 6-7 provides the typical amount of wait time for different ADC functions.

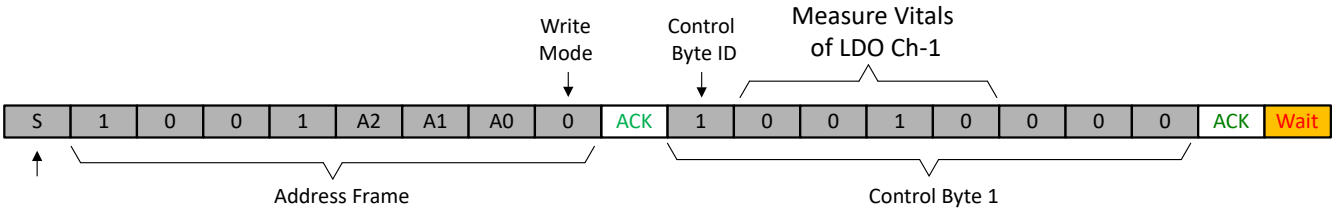

Figure 6-10. Control byte 1 with wait time

To read the data from registers, we recommend that Control Byte 0 be used in the manner described in the steps below:

1. After the controller initiates the START, the target address frame needs to transmitted in the write mode (LSB = 0).
2. The Control Byte 0 is to then be sent in the ***read*** mode (LSB of this frame = 1). The register address in the control byte 0 frame is that of the target register whose data is to be read by the user/controller. After receiving the ACK from the target, the controller must issue a STOP or repeated START sequence.
3. The controller is to then send the ***target address frame*** in the read mode (LSB = 1). Anytime the controller wishes to change from being a transmitter to a receiver or vice-versa, the controller must issue a STOP (or a repeated START) sequence. After the ACK has been sent from the target, the controller begins to receive Data from the target register that selected in the previous step.
4. If a STOP is not issued, the controller continues to receive data from the subsequent registers of the register map. The read continues to cycle through the register map until the controller decides to end the cycle.

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Once the controller has received the data required, the cycle can be ended by issuing a NACK followed by a STOP.

Figure 6-11 below shows an example of the described process where the controller issues Control Byte 1 to instruct the ADC to make a one-time measurement of LDO Ch-1 & Ch-2 vitals and all this data, beginning with V_{IN} register of LDO Ch-1 to I_{OUT-L} register of LDO Ch-2, is read by the controller.

During the read cycle, TPS7B7802-Q1 has the ability to retain the address of the target register provided in the Control Byte 0 (in Figure 6-11, this is the V_{IN} register of LDO Ch-1) even if the device is disabled. After a read cycle has been initiated, even if the LDO undergoes a disable-enable sequence, the TPS7B7802-Q1 retains the target register address previously set, and data can be directly begun to be read by the controller from this register without the need of sending a control bye 0 again. The TPS7B7802-Q1 retains this address so long as the device does not undergo a power cycle (or enter UVLO), a software reset (SWRST in Control Byte 1) or if overwritten by a new control byte 0 sequence.

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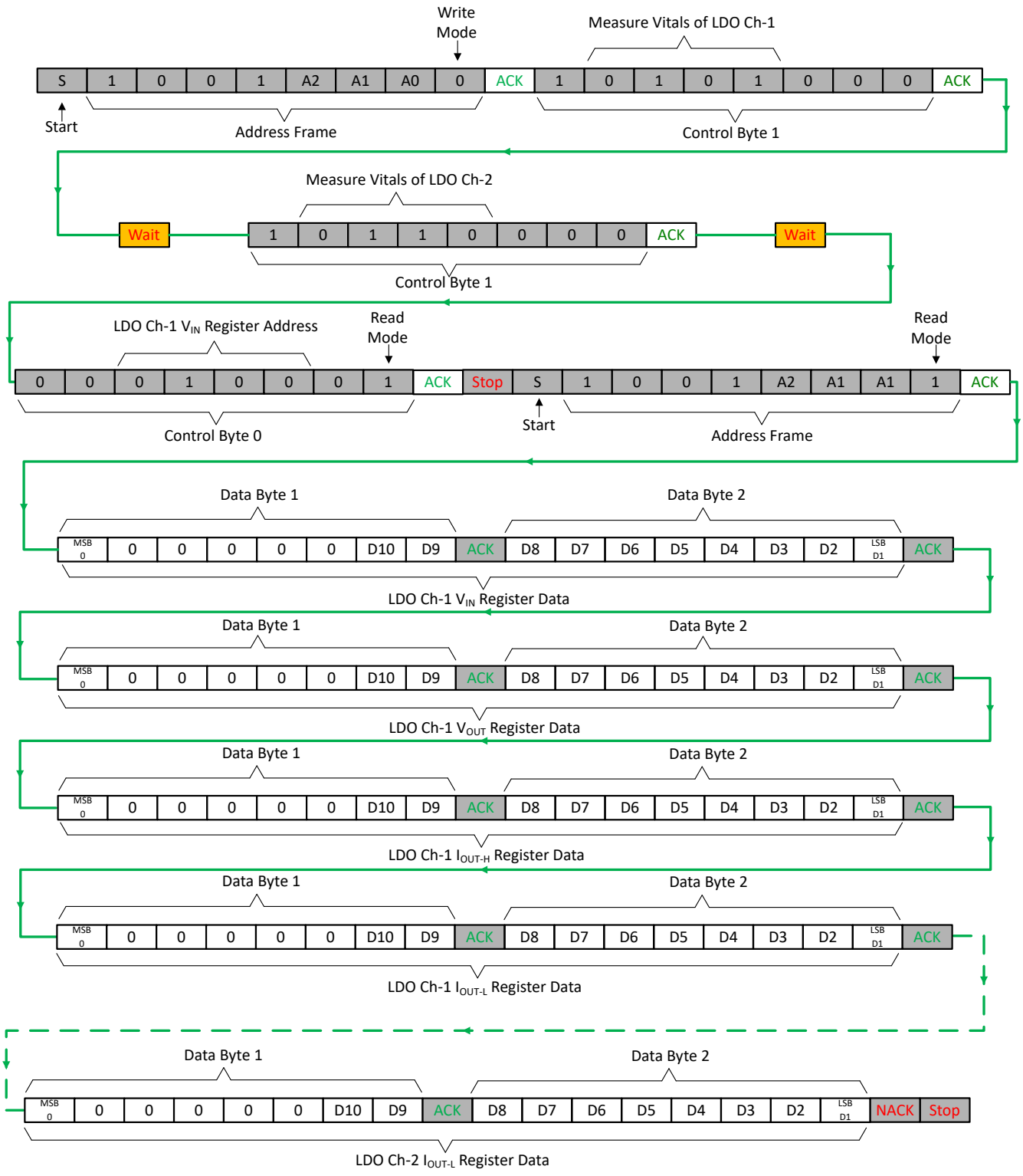

Figure 6-11. Read Cycle Example

7 Register Map

Table 7-1. Register Map

REGISTER NAME	ADDRESS	BIT 15	BIT 14	BIT 13	BIT 12	BIT 11	BIT 10	BIT 9	BIT 8	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0	R/W ACCESSIBILITY
CFR-0	0x0	Start Up Current Limit Ch-1				I_{OUT} warn threshold Ch-1				Output Voltage Ch-1								R/W
CFR-1	0x1	Start Up Current Limit Ch-2				I_{OUT} warn threshold Ch-2				Output Voltage Ch-2								R/W
CFR-2	0x2	I_{OUT} Open Threshold Ch-1				Current Limit Ch-1				I_{OUT} Open Threshold Ch-2				Current Limit Ch-2				R/W
CFR-3	0x3	T_J Warn Threshold			ADC-EN	Latch	Blanking Time			EN1	FB1	EN2	FB2	Reserved				R/W
VIN	0x4	0	0	0	0	0	0	Input Voltage Measurement										R
VOUT-1	0x5	0	0	0	0	0	0	Output Voltage Measurement Ch-1										R
IOUTH-1	0x6	0	0	0	0	0	0	High Range Load Current Measurement Ch-1										R
IOUTL-1	0x7	0	0	0	0	0	0	Low Range Load Current Measurement Ch-1										R
TEMP	0x8	0	0	0	0	0	0	Device Junction Temperature Measurement										R
VIN	0x9	0	0	0	0	0	0	Input Voltage Measurement										R
VOUT-2	0xA	0	0	0	0	0	0	Output Voltage Measurement Ch-2										R
IOUTH-2	0xB	0	0	0	0	0	0	High Range Load Current Measurement Ch-2										R
IOUTL-2	0xC	0	0	0	0	0	0	Low Range Load Current Measurement Ch-2										R
LAT_ST	0xD	TSD	TWRN	ILIM1	IWRN1	OL1	IREV1	UVLO1	OUTUV1	OUTOV1	ILIM2	IWRN2	OL2	IREV2	UVLO2	OUTUV2	OUTOV2	R/W
RT_ST	0xE	TSD	TWRN	ILIM1	IWRN1	OL1	IREV1	UVLO1	OUTUV1	OUTOV1	ILIM2	IWRN2	OL2	IREV2	UVLO2	OUTUV2	OUTOV2	R
MASK	0xF	TSD	TWRN	ILIM1	IWRN1	OL1	IREV1	UVLO1	OUTUV1	OUTOV1	ILIM2	IWRN2	OL2	IREV2	UVLO2	OUTUV2	OUTOV2	R/W

7.1 Default Settings

On device power up, Channel 1&2 of the device come up configured with following default settings provided below in Table 7-2. The user can overwrite these default settings and re-configure the device.

Table 7-2. Default settings

Channel 1&2 Settings		
Description	**Digital Word**	**Analog Value**
Startup Current Limit	0111	200mA
I_{OUT} Warn threshold	1010	210mA
Output Voltage V_{OUTX}	0001 1110	5V
I_{OUT} Open Load Threshold	0101	5mA
I_{OUT} Current Limit	1001	250mA
T_J Warn Threshold	101	120°C
ADC Enable	ADCEN = 1	ADC Enabled
Latch Bit	0	0 (Runtime Error Detection)
Blanking Time	100	8.5msec
Enable Bit	EN1 = 0, EN2 = 1	-
Feedback Bit	FB1 = 0, FB2 = 1	V_{OUT2} to be set via external resistors

ADVANCE INFORMATION

7.2 Register Details

Configuration Register 0 (Address = 0x1) [Reset = 0x7A1E]

Figure 7-1. Configuration Register 0

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Startup Current Limit Ch-1[3:0]				I_{OUT} Warn Threshold Ch-1[3:0]				Output Voltage Ch-1[7:0]							
R/W-0b0111				R/W-0b1010				R/W-0b00011110							

Table 7-3. Configuration Register 0 Field Descriptions

Bit	Field	Type	Reset	Description
15:12	Startup Current Limit Ch-1[3:0]	R/W	0b0111	This register helps set the channel 1 current limit value at startup in the range 25mA ≤ $I_{STARTUP\_CL}$ ≤ 400mA in 25mA increments. 25mA & 400mA values are set with digital word 0b0000 and 0b1111 respectively. Intermediate values can be with the following equation: $I_{STARTUP\_CL}$ = (D[3:0] + 1)*25mA. As an example, D[3:0] = 0b0111 = 7 and $I_{STARTUP\_CL}$ = 8×25mA = 200mA.
11:8	I_{OUT} Warn Threshold Ch-1[3:0]	R/W	0b1010	This register helps set the channel 1 load current warning threshold value from the range 10mA ≤ I_{WARN_TH} ≤ 310mA in 20mA increments. 10mA is set with 0b0000 & 310mA is set with 0b1111. All other intermediate values can be set with the following equation: I_{WARN_TH} = (D[3:0])*20mA + 10mA. As an example, D[3:0] = 0b1010 = 10 and $I_{STARTUP\_CL}$ = 10×20mA + 10mA = 210mA.
7:0	Output Voltage Ch-1[7:0]	R/W	0b00011110	This register helps set the channel 1 output voltage value from the range 2V ≤ V_{OUT} ≤ 27.4V in 100mV increments. 2V and 27.4V are set with 0x00 & 0xFE respectively. All other intermediate values can be set with the following equation: V_{OUT} = (D[7:0])*0.1V + 2V. As an example, D[7:0] = 0b0001 1110 = 30 and V_{OUT} = 30×0.1 + 2 = 5V. Setting digital word 0xFF configures the channel as a switch.

ADVANCE INFORMATION

Configuration Register 1 (Address = 0x1) [Reset = 0x7A1E]

Figure 7-2. Configuration Register 1

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Startup Current Limit Ch-2[3:0]				I_{OUT} Warn Threshold Ch-2[3:0]				Output Voltage Ch-2[7:0]							
R/W-0b0111				R/W-0b1010				R/W-0b00011110							

Table 7-4. Configuration Register 1 Field Descriptions

Bit	Field	Type	Reset	Description
15:12	Startup Current Limit Ch-2[3:0]	R/W	0b0111	This register helps set the channel 2 current limit value at startup in the range 25mA ≤ $I_{STARTUP\_CL}$ ≤ 400mA in 25mA increments. 25mA & 400mA values are set with digital word $[0000]_2$ and 0b1111 respectively. Intermediate values can be with the following equation: $I_{STARTUP\_CL}$ = (D[3:0] + 1)*25mA. As an example, D[3:0] = 0b0111 = 7 and $I_{STARTUP\_CL}$ = 8×25mA = 200mA.
11:8	I_{OUT} Warn Threshold Ch-2[3:0]	R/W	0b1010	This register helps set the channel 2 load current warning threshold value from the range 10mA ≤ I_{WARN_TH} ≤ 310mA in 20mA increments. 10mA is set with 0b0000 & 310mA is set with 0b1111. All other intermediate values can be set with the following equation: I_{WARN_TH} = (D[3:0])*20mA + 10mA. As an example, D[3:0] = 0b1010 = 10 and $I_{STARTUP\_CL}$ = 10×20mA + 10mA = 210mA.
7:0	Output Voltage Ch-2[7:0]	R/W	0b00011110	This register helps set the channel 2 output voltage value from the range 2V ≤ V_{OUT} ≤ 27.4V in 100mV increments. 2V and 27.4V are set with 0x00 & 0xFE respectively. All other intermediate values can be set with the following equation: V_{OUT} = (D[7:0])*0.1V + 2V. As an example, D[7:0] = 0b0001 1110 = 30 and V_{OUT} = 30×0.1 + 2 = 5V. Setting digital word 0xFF configures the channel as a switch.

ADVANCE INFORMATION

Configuration Register 2 (Address = 0x2) [Reset = 0x5959]

Figure 7-3. Configuration Register 2

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
I_{OUT} Open Threshold Channel 1				Current Limit Channel 1				I_{OUT} Open Threshold Channel 2				Current Limit Channel 2			
R/W-0b0101				R/W-0b1001				R/W-0b0101				R/W-0b1001			

Table 7-5. Configuration Register 2 Field Descriptions

Bit	Field	Type	Reset	Description
15:12	I_{OUT} Open Threshold Channel 1[3:0]	R/W	0b0101	This register helps set the channel 1 open load threshold value in the range 0mA ≤ I_{OPEN_TH} ≤ 15mA in 1mA increments. 0mA & 15mA values are set with digital word 0b0000 and 0b1111 respectively. Intermediate values can be with the following equation: I_{OPEN_TH} = D[3:0] mA. As an example, D[3:0] = 0b0101 = 5 and I_{OPEN_TH} = 5mA.
11:8	Current Limit Channel 1[3:0]	R/W	0b1001	This register helps set the channel 1 current limit value in the range 25mA ≤ I_{CL} ≤ 400mA in 25mA increments. 25mA & 400mA values are set with digital word 0b0000 and 0b1111 respectively. Intermediate values can be with the following equation: I_{CL} = (D[3:0] + 1)*25mA. As an example, D[3:0] = 0b1001 = 9 and I_{CL} = 10×25mA = 250mA.
7:4	I_{OUT} Open Threshold Channel 2[3:0]	R/W	0b0101	This register helps set the channel 2 open load threshold value in the range 0mA ≤ I_{OPEN_TH} ≤ 15mA in 1mA increments. 0mA & 15mA values are set with digital word 0b0000 and 0b1111 respectively. Intermediate values can be with the following equation: I_{OPEN_TH} = D[3:0] mA. As an example, D[3:0] = 0b0101 = 5 and I_{OPEN_TH} = 5mA.
3:0	Current Limit Channel 2[3:0]	R/W	0b1001	This register helps set the channel 2 current limit value in the range 25mA ≤ I_{CL} ≤ 400mA in 25mA increments. 25mA & 400mA values are set with digital word 0b0000 and 0b1111 respectively. Intermediate values can be with the following equation: I_{CL} = (D[3:0] + 1)*25mA. As an example, D[3:0] = 0b1001 = 9 and I_{CL} = 10×25mA = 250mA.

ADVANCE INFORMATION

Configuration Register 3 (Address = 0x3) [Reset = 0xB430]

Figure 7-4. Configuration Register 3

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
T_J Warn Threshold			ADC-EN	Latch	Blanking Time			EN1	FB1	EN2	FB2	Reserved			
R/W-0b101			R/W-0b1	R/W-0b0	R/W-0b100			R/W-0b0	R/W-0b0	R/W-0b1	R/W-0b1	0b0000			

Table 7-6. Configuration Register 3 Field Descriptions

Bit	Field	Type	Reset	Description
15:13	T_J Warn Threshold[2:0]	R/W	0b101	This register helps set the junction temperature warn threshold value in the range 70℃ ≤ T_{J_WARN} ≤ 140℃ in 10℃ increments. 70℃ & 140℃ values are set with digital word 0b000 and 0b111 respectively. Intermediate values can be set with the following equation: T_{J_WARN} = (D[2:0])*10℃ + 70℃. As an example, D[2:0] = 0b101 = 5 and T_{J_WARN} = 5×10℃ + 70℃ = 120℃.
12	ADC-EN	R/W	0b1	This bit allows the user to disable the ADC (by setting the bit to 0) and reduce quiescent current consumption.
11	Latch	R/W	0b0	This bit, if set to 1, configures the NERR pin to follow the status of bits in the LAT_ST register. If set to 0, the NERR pin follows the status of bits in the RT_ST register.
10:8	Blanking Time	R/W	0b100	This register helps set the blanking time value in the range 0msec ≤ T_{BLANK} ≤ 100msec. Digital entries of 0b000, 0b001, 0b010, 0b011, 0b100, 0b101, 0b110 & 0b111 in this register correspond to blanking times of 0msec, 0.85msec, 1.7msec, 3.4msec, 8.5msec, 17msec, 34msec & 85msec respectively. Blanking time is triggered on enable (of either channel) and recovery from thermal shutdown. The bits in the status registers get updated only if the corresponding fault condition exists after the blanking time has elapsed. The blanking time is applicable to all bits in the status register, with the exception of TSD, UVLO1 and UVLO2 bits. These bits do not have any blanking time.
7	EN1	R/W	0b0	Allows the user to enable (if bit set to 1) or disable (if bit set to 0) channel 1 via I^2C. For channel 1 of the device to provide a regulated output voltage, the enable pin voltage needs to be V_{EN} ≥ 2V and the digital EN1 bit needs to be set to 1.
6	FB1	R/W	0b0	Allows user to set channel 1 output voltage using external resistors (if set to 1) or via I^2C (if set to 0) using CFR-0.
5	EN2	R/W	0b1	Allows the user to enable (if bit set to 1) or disable (if bit set to 0) channel 2 via I^2C. For channel 2 of the device to provide a regulated output voltage, the enable pin voltage needs to be V_{EN} ≥ 2V and the digital EN2 bit needs to be set to 1.
4	FB2	R/W	0b1	Allows user to set channel 2 output voltage using external resistors (if set to 1) or via I^2C (if set to 0) using CFR-1.
3:0	Reserved	-	0b0000	These bits are reserved and always read as 0.

ADVANCE INFORMATION

Input Voltage Measurement (Address = 0x4) [Reset = 0x0000]

Figure 7-5. Device Input Voltage Measurement

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved						Input Voltage Measurement									
0b00000						R-0x000									

Table 7-7. Input Voltage Measurement Field Descriptions

Bit	Field	Type	Reset	Description
15:10	Reserved	-	0b00000	These bits are undefined and must not be accessed.
9:0	Input Voltage Measurement [9:0]	R	0x000	This register stores the 10-bit ADC measurement of the device input voltage value in the range 0V ≤ V_{IN} ≤ 45V in approx. 43.8mV increments. IN1 & IN2 pins must be connected together. 0V & 45V values are associated with digital words 0x000 and 0x3FF respectively. Intermediate measurement values in the range 2V ≤ V_{IN} ≤ 42V and the associated digital word are related by the following equation: V_{IN_MEAS} = (D[9:0] + 3)*0.0432V. As an example, if the register reading is D[9:0] = 0x113 = 275, then channel V_{IN} = (275 + 3)*0.0432V = 12V.

ADVANCE INFORMATION

Output Voltage Measurement Ch-1 (Address = 0x5) [Reset = 0x0000]

Figure 7-6. Output Voltage Measurement Ch-1

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved						Output Voltage Measurement Ch-1									
0b00000						R-0x000									

Table 7-8. Output Voltage Measurement Ch-1 Field Descriptions

Bit	Field	Type	Reset	Description
15:10	Reserved	-	0b00000	These bits are undefined and must not be accessed.
9:0	Output Voltage Measurement Ch-1[9:0]	R	0x000	This register stores the 10-bit ADC measurement of the channel 1 output voltage value in the range 0V ≤ V_{OUT} ≤ 45V in approx. 43.8mV increments. 0V & 45V values are associated with digital words 0x000 and 0x3FF respectively. Intermediate measurement values in the range 2V ≤ V_{OUT} ≤ 42Vand the associated digital word are related by the following equation: V_{OUT_MEAS} = (D[9:0] + 3)*0.0432V. As an example, if the register reading is D[9:0] = 0x0B6 = 182, then channel V_{OUT_MEAS} = (182 + 3)*0.0432V = 8V.

ADVANCE INFORMATION

High Range Load Current Measurement Ch-1 (Address = 0x6) [Reset = 0x0000]

Figure 7-7. High Range Load Current Measurement Ch-1

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved						High Range Load Current Measurement Ch-1									
0b00000						R-0x000									

Table 7-9. High Range Load Current Measurement Ch-1 Field Descriptions

Bit	Field	Type	Reset	Description
15:10	Reserved	-	0b00000	These bits are undefined and must not be accessed.
9:0	High Range Load Current Measurement Ch-1[9:0]	R	0x000	This register stores the 10-bit ADC measurement of the channel 1 output current value in the range 0mA ≤ I_{OUT} ≤ 400mA in 397µA increments. 0mA & 400mA values are associated with digital words 0x000 and 0x3FF respectively. Intermediate measurement values and the associated digital word are related by the following equation: I_{OUTH_MEAS} = (D[9:0])*0.397mA. As an example, if the register reading is D[9:0] = 0x0FC = 252, then channel I_{OUTH_MEAS} = 252×0.397mA = 100mA.

ADVANCE INFORMATION

Low Range Load Current Measurement Ch-1 (Address = 0x7) [Reset = 0x0000]

Figure 7-8. Low Range Load Current Measurement Ch-1

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved						Low Range Load Current Measurement Ch-1									
0b00000						R-0x000									

Table 7-10. Low Range Load Current Measurement Ch-1 Field Descriptions

Bit	Field	Type	Reset	Description
15:10	Reserved	-	0b00000	These bits are undefined and must not be accessed.
9:0	Low Range Load Current Measurement Ch-1[9:0]	R	0x000	This register stores the 10-bit ADC measurement of the channel 1 output current value in the range 0mA ≤ I_{OUT} ≤ 25mA in approx. 24.3µA increments. 0mA & 25mA values are associated with digital words 0x000 and 0x3FF respectively. Intermediate measurement values and the associated digital word are related by the following equation: I_{OUTL_MEAS} = {(D[9:0])*0.02375) - 0.02138} mA. As an example, if the register reading is D[9:0] = 0x337 = 823, then channel I_{OUTL_MEAS} = {(823×0.02375) - 0.02138}mA = 19.5mA.

ADVANCE INFORMATION

Junction Temperature Measurement (Address = 0x8) [Reset = 0x0000]

Figure 7-9. Junction Temperature Measurement

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved						Device Junction Temperature Measurement									
0b00000						R-0x000									

Table 7-11. Junction Temperature Measurement Field Descriptions

Bit	Field	Type	Reset	Description
15:10	Reserved	-	0b00000	These bits are undefined and must not be accessed.
9:0	Device Junction Temperature Measurement[9:0]	R	0x000	This register stores the 10-bit ADC measurement of the junction temperature value in the range -50°C ≤ T_J ≤ 150°C in 1°C increments. -50°C & 150°C values are associated with digital words 0x332 and 0x265 respectively. Intermediate measurement values and the associated digital word are related by the following equation: T_{J_MEAS} = 763 - D[9:0]. As an example, if the register reading is D[9:0] = 0x297 = 663, then device T_{J_MEAS} = 763 - 663 = 100°C.

ADVANCE INFORMATION

Input Voltage Measurement (Address = 0x9) [Reset = 0x0000]

Figure 7-10. Device Input Voltage Measurement

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved						Input Voltage Measurement									
0b00000						R-0x000									

Table 7-12. Input Voltage Measurement Field Descriptions

Bit	Field	Type	Reset	Description
15:10	Reserved	-	0b00000	These bits are undefined and must not be accessed.
9:0	Input Voltage Measurement [9:0]	R	0x000	This register stores the 10-bit ADC measurement of the device input voltage value in the range 0V ≤ V_{IN} ≤ 45V in approx. 43.8mV increments. IN1 & IN2 pins must be connected together. 0V & 45V values are associated with digital words 0x000 and 0x3FF respectively. Intermediate measurement values in the range 2V ≤ V_{IN} ≤ 42V and the associated digital word are related by the following equation: V_{IN_MEAS} = (D[9:0] + 3)*0.0432V. As an example, if the register reading is D[9:0] = 0x113 = 275, then channel V_{IN} = (275 + 3)*0.0432V = 12V.

ADVANCE INFORMATION

Output Voltage Measurement Ch-2 (Address = 0xA) [Reset = 0x0000]

Figure 7-11. Output Voltage Measurement Ch-2

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved						Output Voltage Measurement Ch-2									
0b00000						R-0x000									

Table 7-13. Output Voltage Measurement Ch-2 Field Descriptions

Bit	Field	Type	Reset	Description
15:10	Reserved	-	0b00000	These bits are undefined and must not be accessed.
9:0	Output Voltage Measurement Ch-2[9:0]	R	0x000	This register stores the 10-bit ADC measurement of the channel 2 output voltage value in the range 0V ≤ V_{OUT} ≤ 45V in approx. 43.8mV increments. 0V & 45V values are associated with digital words 0x000 and 0x3FF respectively. Intermediate measurement values in the range 2V ≤ V_{OUT} ≤ 42V and the associated digital word are related by the following equation: V_{OUT_MEAS} = (D[9:0] + 3)*0.0432V. As an example, if the register reading is D[9:0] = 0x071 = 113, then channel V_{OUT_MEAS} = (113 + 3)*0.0432V = 5V.

ADVANCE INFORMATION

High Range Load Current Measurement Ch-2 (Address = 0xB) [Reset = 0x0000]

Figure 7-12. High Range Load Current Measurement Ch-2

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved						High Range Load Current Measurement Ch-2									
0b00000						R-0x000									

Table 7-14. High Range Load Current Measurement Ch-2 Field Descriptions

Bit	Field	Type	Reset	Description
15:10	Reserved	-	0b00000	These bits are undefined and must not be accessed.
9:0	High Range Load Current Measurement Ch-2[9:0]	R	0x000	This register stores the 10-bit ADC measurement of the channel 2 output current value in the range 0mA ≤ I_{OUT} ≤ 400mA in approx. 397µA increments. 0mA & 400mA values are associated with digital words 0x000 and 0x3FF respectively. Intermediate measurement values and the associated digital word are related by the following equation: I_{OUTH_MEAS} = (D[9:0])*0.397mA. As an example, if the register reading is D[9:0] = 0x0FC = 252, then channel I_{OUTH_MEAS} = 252×0.397mA = 100mA.

ADVANCE INFORMATION

Low Range Load Current Measurement Ch-2 (Address = 0xC) [Reset = 0x0000]

Figure 7-13. Low Range Load Current Measurement Ch-2

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved						Low Range Load Current Measurement Ch-2									
0b00000						R-0x000									

Table 7-15. Low Range Load Current Measurement Ch-2 Field Descriptions

Bit	Field	Type	Reset	Description
15:10	Reserved	-	0b00000	These bits are undefined and must not be accessed.
9:0	Low Range Load Current Measurement Ch-2[9:0]	R	0x000	This register stores the 10-bit ADC measurement of the channel 2 output current value in the range 0mA ≤ I_{OUT} ≤ 25mA in 24.3µA increments. 0mA & 25mA values are associated with digital words 0x000 and 0x3FF respectively. Intermediate measurement values and the associated digital word are related by the following equation: I_{OUTL_MEAS} = {(D[9:0])*0.02375) - 0.02138} mA. As an example, if the register reading is D[9:0] = 0x337 = 823, then channel I_{OUTL_MEAS} = {(823×0.02375) - 0.02138}mA = 19.5mA.

ADVANCE INFORMATION

Latch Error Register (Address = 0xD) [Reset = 0x0000]

Figure 7-14. Latch Error Register

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TSD	TWRN	ILIM1	IWRN1	OL1	IREV1	UVLO1	OUTUV1	OUTOV1	ILIM2	IWRN2	OL2	IREV2	UVLO2	OUTUV2	OUTOV2
R/W-0b0	R/W-0b0	R/W-0b0	R/W-0b0	R/W-0b0	R/W-0b0	R/W-0b0	R/W-0b0	R/W-0b0	R/W-0b0	R/W-0b0	R/W-0b0	R/W-0b0	R/W-0b0	R/W-0b0	R/W-0b0

Table 7-16. Latch Error Register Field Descriptions

Bit	Field	Type	Reset	Description
15	TSD	R/W	0b0	Every bit in this register latches to a '1' when the corresponding fault condition occurs. The bits retain logic states even if the fault conditions are removed. The bits can be reset by overwriting with the appropriate digital word. Pulling V_{IN} < $UVLO_{DIG}$ or using the SWRRST in Control Byte 1 resets all registers to the default state. This bit latches to '1' when the device undergoes thermal shutdown.
14	TWRN	R/W	0b0	This bit latches to '1' when the device junction temperature exceeds value set in T_J Warn Threshold register in CFR-3.
13	ILIM1	R/W	0b0	This bit latches to logic ‘1’, when the load current in channel 1 equals or exceeds the value set in Current Limit Ch-1 register in CFR-2.
12	IWRN1	R/W	0b0	This bit latches to logic ‘1’, when the load current in channel 1 equals or exceeds the value set in I_{OUT} warn threshold Ch-1 register in CFR-0.
11	OL1	R/W	0b0	This bit latches to logic ‘1’, when the load current in channel 1 equals or falls below the value set in I_{OUT} Open Threshold Ch-1 register in CFR-2.
10	IREV1	R/W	0b0	This bit latches to logic ‘1’, when reverse current has been detected in channel 1.
9	UVLO1	R/W	0b0	This bit latches to logic ‘1’, when input voltage drops below $UVLO_{FALLING}$.
8	OUTUV1	R/W	0b0	This bit latches to logic ‘1’, when channel 1 output voltage falls by 10% (typ) of the nominal value.
7	OUTOV1	R/W	0b0	This bit latches to logic ‘1’, when channel 1 output voltage exceeds the nominal value by 10% (typ).
6	ILIM2	R/W	0b0	This bit latches to logic ‘1’, when the load current in channel 2 equals or exceeds the value set in Current Limit Ch-2 register in CFR-2.
5	IWRN2	R/W	0b0	This bit latches to logic ‘1’, when the load current in channel 2 equals or exceeds the value set in I_{OUT} warn threshold Ch-2 register in CFR-1.
4	OL2	R/W	0b0	This bit latches to logic ‘1’, when the load current in channel 2 equals or falls below the value set in I_{OUT} Open Threshold Ch-2 register in CFR-2.
3	IREV2	R/W	0b0	This bit latches to logic ‘1’, when reverse current has been detected in channel 2.
2	UVLO2	R/W	0b0	This bit latches to logic ‘1’, when input voltage drops below $UVLO_{FALLING}$.
1	OUTUV2	R/W	0b0	This bit latches to logic ‘1’, when channel 2 output voltage falls by 10% (typ) of the nominal value..
0	OUTOV2	R/W	0b0	This bit latches to logic ‘1’, when channel 2 output voltage exceeds the nominal value by 10% (typ).

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Run-Time Error Register (Address = 0xE) [Reset = 0x0000]

Figure 7-15. Run-Time Error Register

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TSD	TWRN	ILIM1	IWRN1	OL1	IREV1	UVLO1	OUTUV1	OUTOV1	ILIM2	IWRN2	OL2	IREV2	UVLO2	OUTUV2	OUTOV2
R-0b0	R-0b0	R-0b0	R-0b0	R-0b0	R-0b0	R-0b0	R-0b0	R-0b0	R-0b0	R-0b0	R-0b0	R-0b0	R-0b0	R-0b0	R-0b0

Table 7-17. Run-Time Error Register Field Descriptions

Bit	Field	Type	Reset	Description
15	TSD	R	0b0	Every bit in this register follows the corresponding fault condition profile in runtime. The bits toggle to '1' when the corresponding fault conditions occur and automatically reset to 0 when the fault condition is removed. This bit toggles to '1' when device undergoes thermal shutdown.
14	TWRN	R	0b0	This bit toggles to '1' when the device junction temperature exceeds value set in T_J Warn Threshold register in CFR-3.
13	ILIM1	R	0b0	This bit toggles to logic '1', when the load current in channel 1 equals or exceeds the value set in Current Limit Ch-1 register in CFR-2.
12	IWRN1	R	0b0	This bit toggles to logic '1', when the load current in channel 1 equals or exceeds the value set in I_{OUT} warn threshold Ch-1 register in CFR-0.
11	OL1	R	0b0	This bit toggles to logic '1', when the load current in channel 1 equals or falls below the value set in I_{OUT} Open Threshold Ch-1 register in CFR-2.
10	IREV1	R	0b0	This bit toggles to logic '1', when reverse current has been detected in channel 1.
9	UVLO1	R	0b0	This bit toggles to logic '1', when input voltage drops below $UVLO_{FALLING}$.
8	OUTUV1	R	0b0	This bit toggles to logic '1', when channel 1 output voltage falls by 10% (typ) of the nominal value.
7	OUTOV1	R	0b0	This bit toggles to logic '1', when channel 1 output voltage exceeds the nominal value by 10% (typ).
6	ILIM2	R	0b0	This bit toggles to logic '1', when the load current in channel 2 equals or exceeds the value set in Current Limit Ch-2 register in CFR-2.
5	IWRN2	R	0b0	This bit toggles to logic '1', when the load current in channel 2 equals or exceeds the value set in I_{OUT} warn threshold Ch-2 register in CFR-1.
4	OL2	R	0b0	This bit toggles to logic '1', when the load current in channel 2 equals or falls below the value set in I_{OUT} Open Threshold Ch-2 register in CFR-2.
3	IREV2	R	0b0	This bit toggles to logic '1', when reverse current has been detected in channel 2.
2	UVLO2	R	0b0	This bit toggles to logic '1', when input voltage drops below $UVLO_{FALLING}$.
1	OUTUV2	R	0b0	This bit toggles to logic '1', when channel 2 output voltage falls by 10% (typ) of the nominal value.
0	OUTOV2	R	0b0	This bit toggles to logic '1', when channel 2 output voltage exceeds the nominal value by 10% (typ).

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Error Mask Register (Address = 0xF) [Reset = 0x0000]

Figure 7-16. Error Mask Register

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TSD	TWRN	ILIM1	IWRN1	OL1	IREV1	UVLO1	OUTUV1	OUTOV1	ILIM2	IWRN2	OL2	IREV2	UVLO2	OUTUV2	OUTOV2
R/W-0b0	R/W-0b0	R/W-0b0	R/W-0b0	R/W-0b0	R/W-0b0	R/W-0b0	R/W-0b0	R/W-0b0	R/W-0b0	R/W-0b0	R/W-0b0	R/W-0b0	R/W-0b0	R/W-0b0	R/W-0b0

Table 7-18. Error Mask Register Field Descriptions

Bit	Field	Type	Reset	Description
15	TSD	R/W	0b0	The bits in this register provide the user the flexibility of selecting the fault conditions that causes the NERR pin to pull to logic low. If a bit is set to '1', then the corresponding fault condition is masked from the NERR pin, which remains at logic high even if the fault condition occurs. If the bit is set to '0', then the fault condition is unmasked and the NERR pin is pulled to logic low when the fault condition occurs. This bit, if set to '1', masks the NERR pin from the thermal shutdown fault condition.
14	TWRN	R/W	0b0	This bit, if set to '1', causes the NERR pin to remain at logic high even if the junction temperature exceeds the value set in T_J Warn Threshold register in CFR-3.
13	ILIM1	R/W	0b0	This bit, if set to '1', causes the NERR pin to remain at logic high even if the load current in the channel 1 equals or exceeds the value set in Current Limit Ch-1 register in CFR-2.
12	IWRN1	R/W	0b0	This bit, if set to '1', causes the NERR pin to remain at logic high even if the load current in channel 1 equals or exceeds the value set in I_{OUT} warn threshold Ch-1 register in CFR-0.
11	OL1	R/W	0b0	This bit, if set to '1', causes the NERR pin to remain at logic high even if the load current in the channel 1 equals or falls below the value set in I_{OUT} Open Threshold Ch-1 register in CFR-2.
10	IREV1	R/W	0b0	This bit, if set to '1', causes the NERR pin to remain at logic high even if reverse current has been detected in channel 1.
9	UVLO1	R/W	0b0	This bit, if set to '1', causes the NERR pin to remain at logic high even if input voltage drops below $UVLO_{FALLING}$.
8	OUTUV1	R/W	0b0	This bit, if set to '1', causes the NERR pin to remain at logic high even if channel 1 output voltage falls by 10% (typ) of the nominal value.
7	OUTOV1	R/W	0b0	This bit, if set to '1', causes the NERR pin to remain at logic high even if channel 1 output voltage exceeds the nominal value by 10% (typ).
6	ILIM2	R/W	0b0	This bit, if set to '1', causes the NERR pin to remain at logic high even if the load current in the channel 2 equals or exceeds the value set in Current Limit Ch-2 register in CFR-2.
5	IWRN2	R/W	0b0	This bit, if set to '1', causes the NERR pin to remain at logic high even if the load current in the channel 2 equals or exceeds the value set in I_{OUT} warn threshold Ch-2 register in CFR-1.
4	OL2	R/W	0b0	This bit, if set to '1', causes the NERR pin to remain at logic high even if the load current in the channel 2 equals or falls below the value set in I_{OUT} Open Threshold Ch-2 register in CFR-2.
3	IREV2	R/W	0b0	This bit, if set to '1', causes the NERR pin to remain at logic high even if reverse current has been detected in channel 2.
2	UVLO2	R/W	0b0	This bit, if set to '1', causes the NERR pin to remain at logic high even if input voltage drops below $UVLO_{FALLING}$.
1	OUTUV2	R/W	0b0	This bit, if set to '1', causes the NERR pin to remain at logic high even if channel 2 output voltage falls by 10% (typ) of the nominal value.

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Table 7-18. Error Mask Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
0	OUTOV2	R/W	0b0	This bit, if set to '1', causes the NERR pin to remain at logic high even if channel 2 output voltage exceeds the nominal value by 10% (typ).

8 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

8.1 Application Information

The TPS7B780x-Q1 family of devices is a single-or dual-channel 300mA LDO regulator with an integrated 10-bit ADC and I^2C interface. These features enable the user to configure output voltage, current limit, and other settings for both channels, and to monitor V_{IN}, device junction temperature, I_{OUT} & V_{OUT} of both channels, and diagnostic information on fault conditions.

Use the PSPICE transient model to evaluate the base function of the devices. Go to www.ti.com to download the PSPICE model and user's guide for the devices.

8.2 Typical Application

Figure 8-1 shows the typical application circuit for the TPS7B780x-Q1 family of devices. Different values of external components can be used depending on the end application. Applications likely to experience fast load current steps can benefit from additional output capacitance to help reduce output voltage dips during load transients. TI recomends low-ESR ceramic capacitors with X5R or X7R dielectrics for both input and output capacitors.

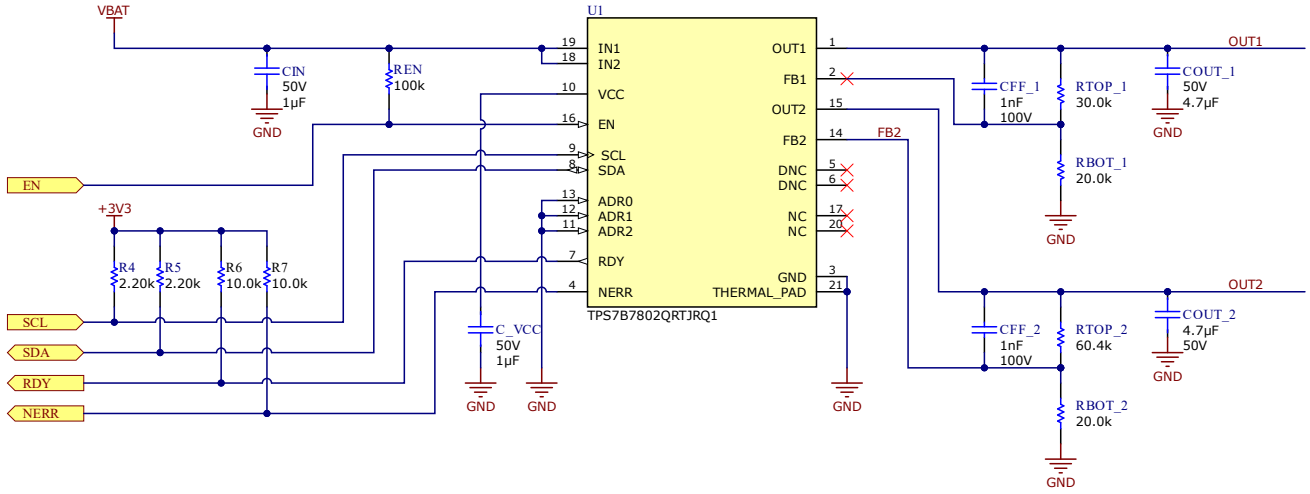

Figure 8-1. Typical Application Schematic for the TPS7B7802-Q1

8.2.1 Design Requirements

For this design example, use the parameters listed in Table 8-1 as the input parameters.

Table 8-1. Design Parameters

PARAMETER	VALUE
Input voltage range	4.5 to 40V
Output voltage	2 to (V_{IN} - V_{DO})
Output capacitor range	4.7 - 100µF
Output Capacitor ESR range	0.001 - 0.5Ω
Programmable current limit (typ, using I^2C)	25 - 350mA

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8.2.2 Detailed Design Procedure

8.2.2.1 Input and Output Capacitor Selection

The TPS7B78xx-Q1 requires an output capacitor of 4.7µF or larger (2.2µF or larger capacitance) for stability and an equivalent series resistance (ESR) between 0.001Ω and 0.5Ω. For best transient performance, use X5R- and X7R-type ceramic capacitors because these capacitors have minimal variation in value and ESR over temperature. When choosing a capacitor for a specific application, be mindful of the DC bias characteristics for the capacitor. Higher output voltages cause a significant derating of the capacitor. For best performance, the maximum recommended output capacitance is 100µF.

Although an input capacitor is not required for stability, good analog design practice is to connect a capacitor from IN to GND. Some input supplies have a high impedance, thus placing the input capacitor on the input supply helps reduce the input impedance. This capacitor counteracts reactive input sources and improves transient response, input ripple, and PSRR. If the input supply has a high impedance over a large range of frequencies, several input capacitors can be used in parallel to lower the impedance over frequency. For robust EMI performance the minimum input capacitance is 500nF. Use a higher-value capacitor if large, fast, rise-time load transients are anticipated, or if the device is located several inches from the input power source.

8.2.2.2 Adjustable Device Feedback Resistor Selection

The adjustable-version device requires external feedback divider resistors to set the output voltage. V_{OUT} is set using the feedback divider resistors, R_1 and R_2, according to the following equation:

$$V_{OUT} = V_{FB} \times (1 + R_1 / R_2) \quad (2)$$

To ignore the FB pin current error term in the V_{OUT} equation, set the feedback divider current to 100x the FB pin current listed in the *Electrical Characteristics* table. This setting provides the maximum feedback divider series resistance, as shown in the following equation:

$$R_1 + R_2 \leq V_{OUT} / (I_{FB} \times 100) \quad (3)$$

8.2.2.3 Feed-Forward Capacitor

For the adjustable-voltage version device, a feed-forward capacitor (C_{FF}) can be connected from the OUT pin to the FB pin. C_{FF} improves transient, noise, and PSRR performance, but is not required for regulator stability. Recommended C_{FF} values are listed in the *Recommended Operating Conditions* table. A higher capacitance C_{FF} can be used; however, the start-up time increases. For a detailed description of C_{FF} tradeoffs, see the *Pros and Cons of Using a Feedforward Capacitor with a Low-Dropout Regulator* application note.

C_{FF} and R_1 form a zero in the loop gain at frequency f_Z, while C_{FF}, R_1, and R_2 form a pole in the loop gain at frequency f_P. C_{FF} zero and pole frequencies can be calculated from the following equations:

$$f_Z = 1 / (2 \times \pi \times C_{FF} \times R_1) \quad (4)$$

$$f_P = 1 / (2 \times \pi \times C_{FF} \times (R_1 \parallel R_2)) \quad (5)$$

8.2.2.4 Power Dissipation (P_D)

Circuit reliability requires consideration of the device power dissipation, location of the circuit on the printed circuit board (PCB), and correct sizing of the thermal plane. The PCB area around the regulator must have few or no other heat-generating devices that cause added thermal stress.

To first-order approximation, power dissipation in the regulator depends on the input-to-output voltage difference and load conditions. The following equation calculates power dissipation (P_D).

$$P_D = (V_{IN} - V_{OUT}) \times I_{OUT} \quad (6)$$

Note

Power dissipation can be minimized, and therefore greater efficiency can be achieved, by correct selection of the system voltage rails. For the lowest power dissipation use the minimum input voltage required for correct output regulation.

For devices with a thermal pad, the primary heat conduction path for the device package is through the thermal pad to the PCB. Solder the thermal pad to a copper pad area under the device. This pad area must contain an array of plated vias that conduct heat to additional copper planes for increased heat dissipation.

The maximum power dissipation determines the maximum allowable ambient temperature (T_A) for the device. According to the following equation, power dissipation and junction temperature are most often related by the junction-to-ambient thermal resistance ($R_{\theta JA}$) of the combined PCB and device package and the temperature of the ambient air (T_A).

$$T_J = T_A + (R_{\theta JA} \times P_D) \quad (7)$$

Thermal resistance ($R_{\theta JA}$) is highly dependent on the heat-spreading capability built into the particular PCB design, and therefore varies according to the total copper area, copper weight, and location of the planes. The junction-to-ambient thermal resistance listed in the *Thermal Information* table is determined by the JEDEC standard PCB and copper-spreading area, and is used as a relative measure of package thermal performance.

8.2.2.5 Estimating Junction Temperature

The JEDEC standard now recommends the use of psi (Ψ) thermal metrics to estimate the junction temperatures of the linear regulator when in-circuit on a typical PCB board application. These metrics are not thermal resistance parameters and instead offer a practical and relative way to estimate junction temperature. These psi metrics are determined to be significantly independent of the copper area available for heat-spreading. The *Thermal Information* table lists the primary thermal metrics, which are the junction-to-top characterization parameter (ψ_{JT}) and junction-to-board characterization parameter (ψ_{JB}). These parameters provide two methods for calculating the junction temperature (T_J), as described in the following equations. Use the junction-to-top characterization parameter (ψ_{JT}) with the temperature at the center-top of device package (T_T) to calculate the junction temperature. Use the junction-to-board characterization parameter (ψ_{JB}) with the PCB surface temperature 1mm from the device package (T_B) to calculate the junction temperature.

$$T_J = T_T + \psi_{JT} \times P_D \quad (8)$$

where:

- P_D is the dissipated power
- T_T is the temperature at the center-top of the device package

$$T_J = T_B + \psi_{JB} \times P_D \quad (9)$$

where

- T_B is the PCB surface temperature measured 1mm from the device package and centered on the package edge

For detailed information on the thermal metrics and how to use them, see the *Semiconductor and IC Package Thermal Metrics* application note.

8.3 Power Supply Recommendations

The device is designed to operate from an input voltage supply with a range between 4.5 and 40V. This input supply must be well regulated. If the input supply is located more than a few inches from the TPS7B780x-Q1 device, TI recommends adding an 1µF MLCC bypass capacitor at the input.

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8.4 Layout

8.4.1 Layout Guidelines

For best overall performance, place all circuit components on the same side of the circuit board and as near as practical to the respective LDO pin connections. Place ground return connections to the input and output capacitor, and to the LDO ground pin as close to each other as possible, connected by a wide, component-side, copper surface. To avoid negative system performance, do not use vias and long traces to the input and output capacitors. The grounding and layout scheme illustrated in Figure 8-2 minimizes inductive parasitics, and thereby reduces load-current transients, minimizes noise, and increases circuit stability. Because of the wide bandwidth and high output current capability, inductance present on the output negatively impacts load transient response. For best performance, minimize trace inductance between the output and load. A low ESL capacitor combined with low trace inductance limits the total inductance present on the output and optimizes the high-frequency PSRR. To improve performance, use a ground reference plane, either embedded in the PCB or placed on the bottom side of the PCB opposite the components. This reference plane serves to verify the accuracy of the output voltage, shield noise, and behaves similar to a thermal plane to spread (or sink) heat from the LDO device when connected to the thermal pad. In most applications, this ground plane is necessary to meet thermal requirements

8.4.2 Layout Example

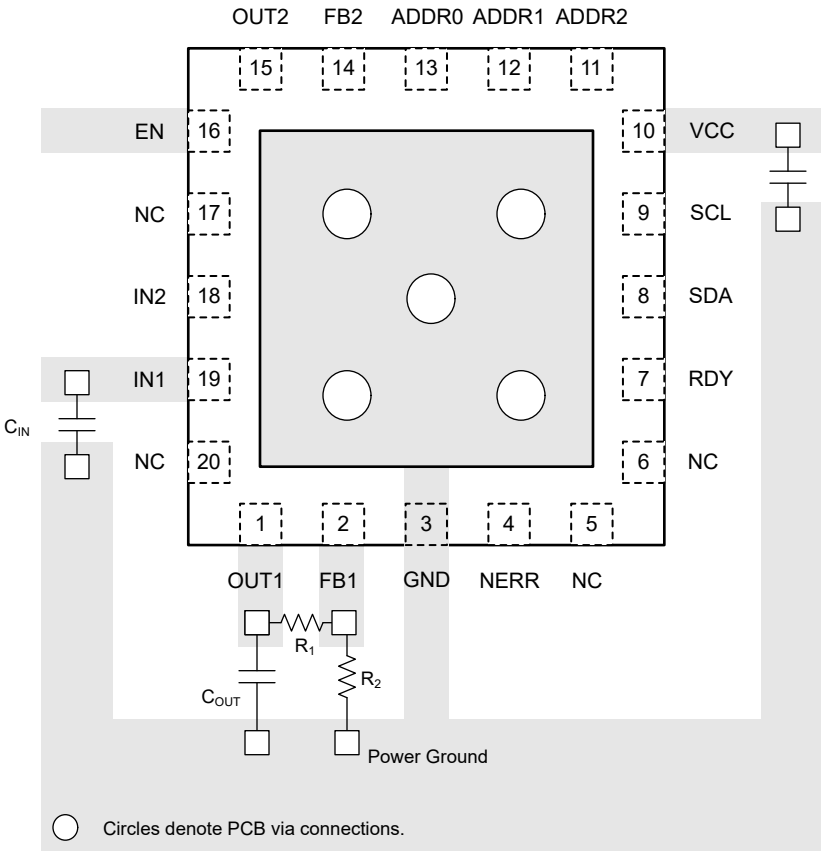

Figure 8-2. TPS7B780x-Q1 Layout Example

9 Device and Documentation Support

TI offers an extensive line of development tools. Tools and software to evaluate the performance of the device, generate code, and develop solutions are listed below.

9.1 Device Support

9.1.1 Device Nomenclature

Table 9-1. Device Nomenclature

PRODUCT	V_{OUT}
TPS7B78**xxQRTJRQ1**	In the WQFN (RTJ) package : **xx** represents channel count. 02 refers to dual channel version. **Q** indicates that this device is a grade-1 device in accordance with the AEC-Q100 standard. **R** is the packaging large reel quantity. **Q1** indicates that the device is an automotive grade (AEC-Q100) device.

9.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

9.3 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

9.4 Trademarks

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9.5 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

9.6 Glossary

TI Glossary — This glossary lists and explains terms, acronyms, and definitions.

10 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

DATE	REVISION	NOTES
June 2026	*	Initial Release

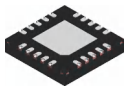
ADVANCE INFORMATION

11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

11.1 Mechanical Data

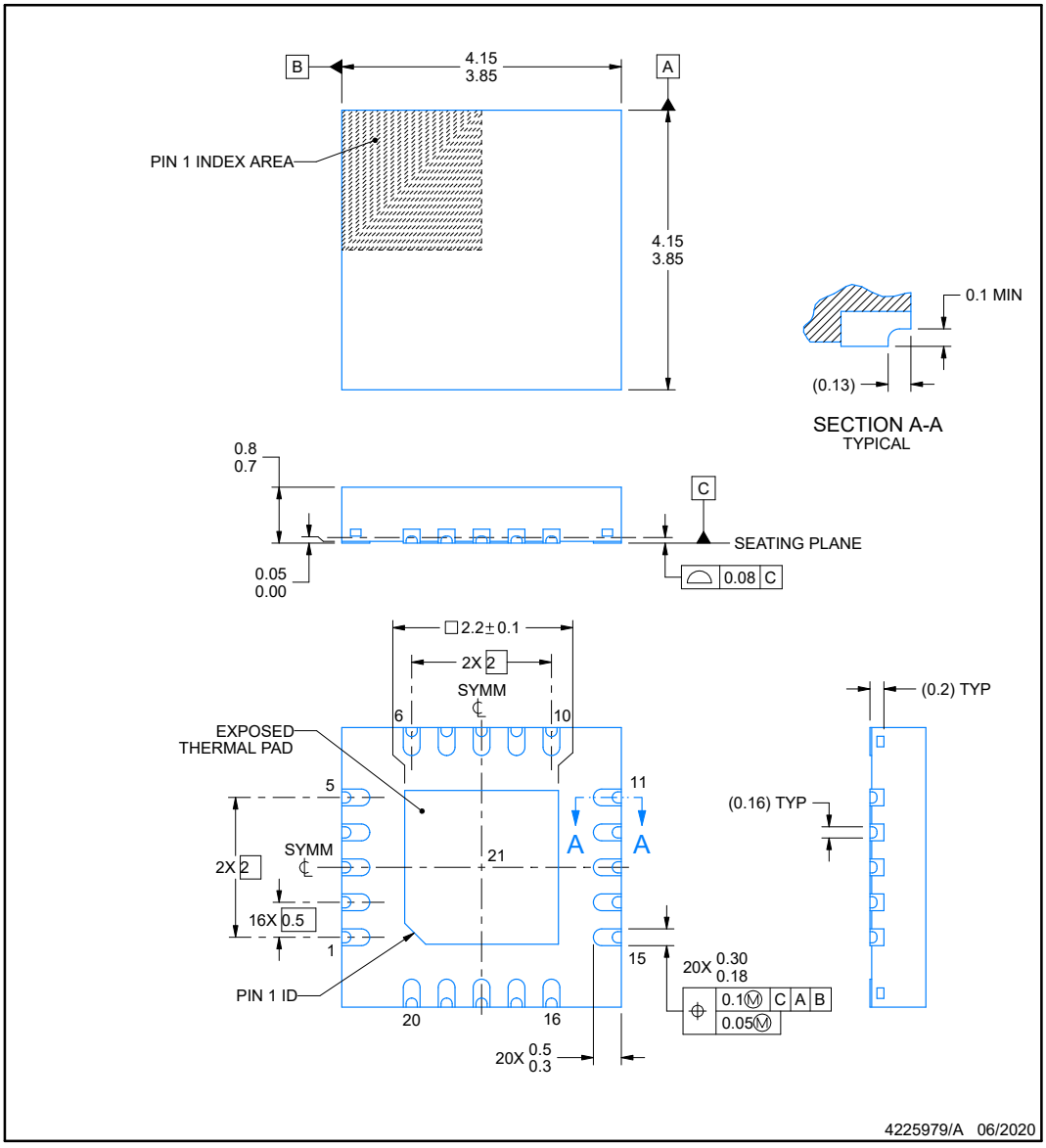
RTJ0020K



PACKAGE OUTLINE

WQFN - 0.8 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



NOTES:

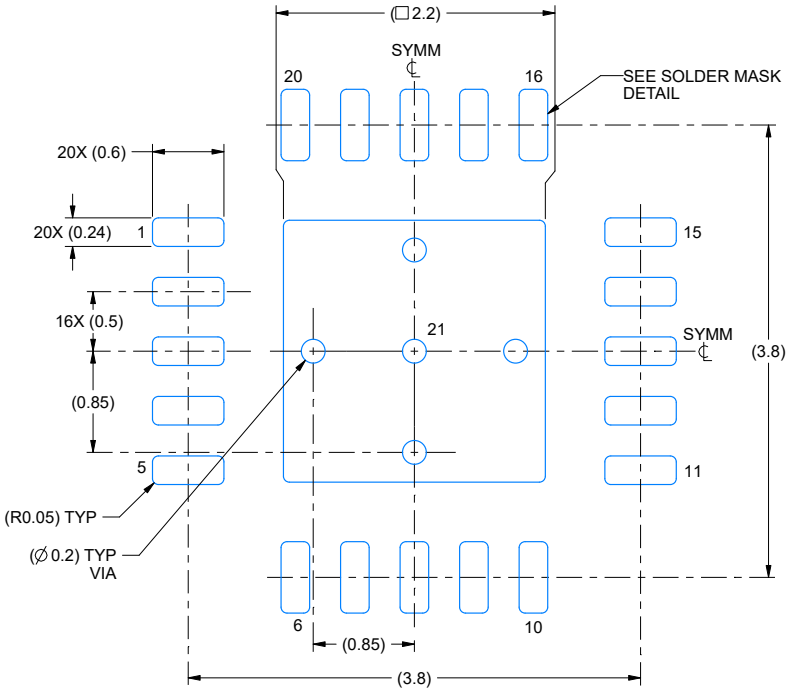
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.

ADVANCE INFORMATION

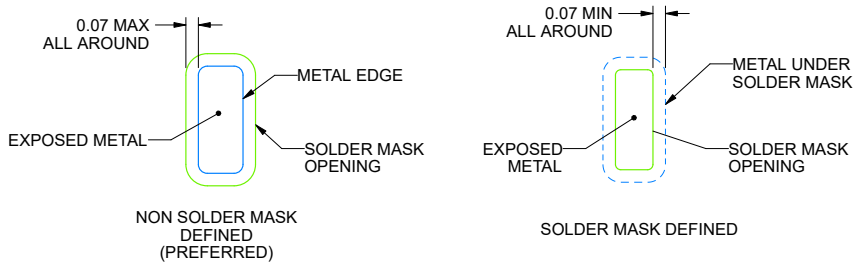
EXAMPLE BOARD LAYOUT

RTJ0020K — **WQFN - 0.8 mm max height**

PLASTIC QUAD FLATPACK - NO LEAD



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 20X



SOLDER MASK DETAILS

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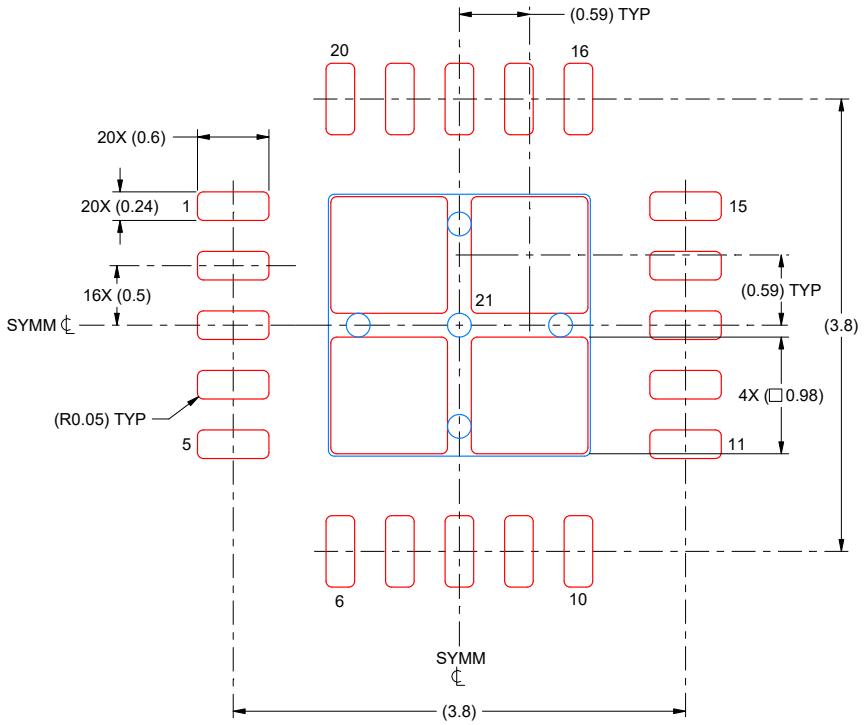
NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.

EXAMPLE STENCIL DESIGN

RTJ0020K — **WQFN - 0.8 mm max height**

PLASTIC QUAD FLATPACK - NO LEAD



SOLDER PASTE EXAMPLE
BASED ON 0.125 MM THICK STENCIL
SCALE: 20X

EXPOSED PAD 21
79% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE

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NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

GENERIC PACKAGE VIEW

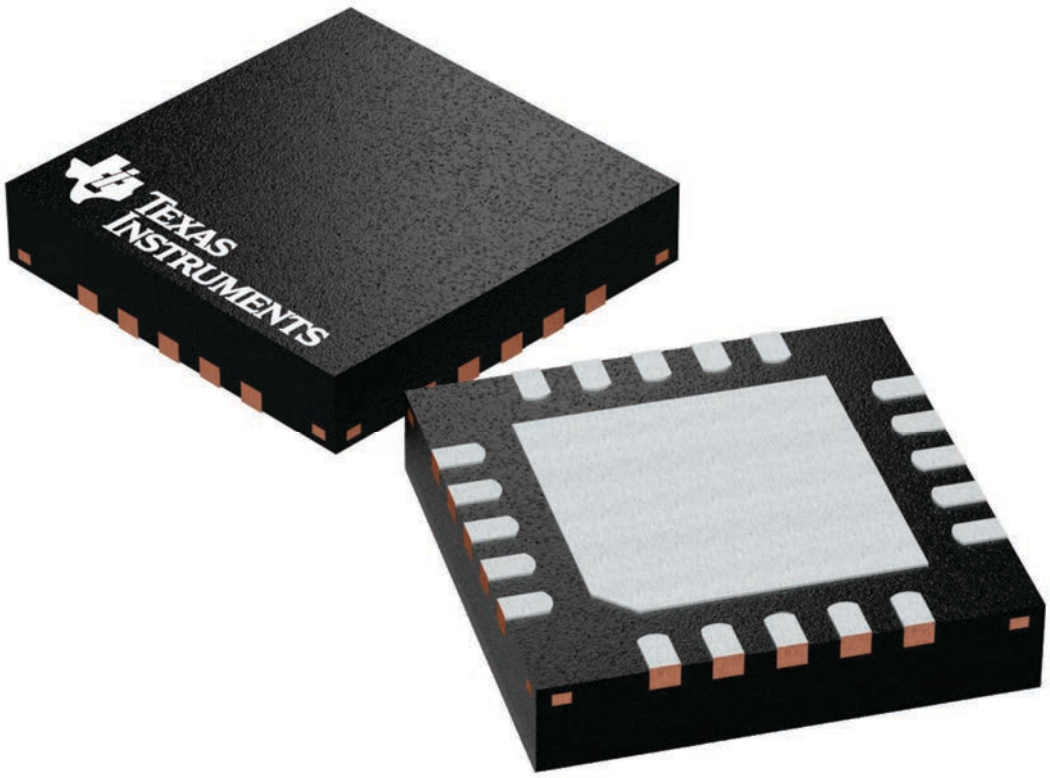
RTJ 20

WQFN - 0.8 mm max height

4 x 4, 0.5 mm pitch

PLASTIC QUAD FLATPACK - NO LEAD

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



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Last updated 10/2025