# TPS7B81-Q1 Automotive, 150mA, Off-Battery, Ultra-Low $I_Q$ (3µA), Low-Dropout Regulator

## 1 Features

- AEC-Q100 qualified for automotive applications:
  - Temperature grade 1: –40°C to +125°C, $T_A$
  - Temperature grade 1: –40°C to +150°C, $T_J$
- 3V to 40V wide $V_{IN}$ input voltage range with up to 45V transient
- Maximum output current: 150mA
- Low quiescent current $I_Q$:
  - 300nA typical when EN = low (shutdown mode)
  - 2.7µA typical at light loads
  - 4.5µA maximum at light loads
- 1.5% output-voltage accuracy over line, load and temperature
- Maximum dropout voltage: 540mV at 150mA load current for fixed 5V output version
- Stable with low-ESR (0.001Ω to 5Ω) ceramic output-stability capacitor (1µF to 200µF)
- Fixed output voltage: 5V, 3.3V, and 2.5V
- Integrated fault protection:
  - Thermal shutdown
  - Short-circuit and overcurrent protection
- Functional Safety-Capable
  - Documentation available to aid functional safety system design
- Packages:
  - DGN (8-pin HVSSOP), $R_{\theta JA}$ = 63.9°C/W
  - DRV (6-pin WSON), $R_{\theta JA}$ = 72.8°C/W
  - DRV (6-pin WSON wettable flank), $R_{\theta JA}$ = 72.8°C/W
  - KVU (5-pin TO-252), $R_{\theta JA}$ = 38.8°C/W

## 2 Applications

- Automotive head units
- Headlights
- Battery management systems (BMS)
- Inverter and motor controls

## 3 Description

In automotive battery-connected applications, low quiescent current ($I_Q$) is important to conserve energy and to extend battery lifetime. Always-on systems must have ultra-low $I_Q$ over an extended temperature range to enable sustained operation when the vehicle ignition is off.

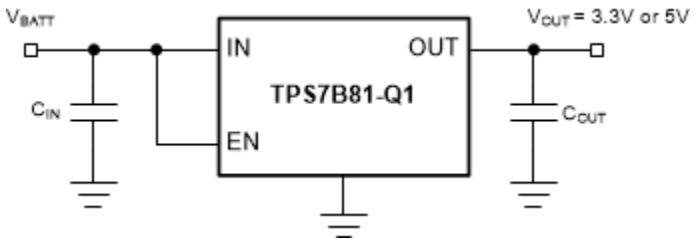
The TPS7B81-Q1 is a low-dropout (LDO) linear regulator designed for up to 40V $V_{IN}$ applications. With only a 2.7µA typical quiescent current at light load, the device is an optimum design for powering microcontrollers and controller area network and local interconnect network (CAN/LIN) transceivers in standby systems.

The device features integrated short-circuit and overcurrent protection. This device operates in ambient temperatures from –40°C to +125°C and with junction temperatures from –40°C to +150°C. Additionally, this device is available in several packages of varying size and thermal conductivity. The compact WSON package comes in a wettable flank option. The TO-252 package enables sustained operation despite significant dissipation across the device. These features make the device well suited as a power supply for various battery-connected automotive applications.

**Package Information**

| PART NUMBER | PACKAGE(1) | PACKAGE SIZE(2) |
|---|---|---|
| TPS7B81-Q1 | DGN (HVSSOP, 8) | 3mm × 3mm |
| | DRV (WSON, 6) | 2mm × 2mm |
| | DRV (WSON wettable flank, 6) | 2mm × 2mm |
| | KVU (TO-252, 5) | 6.1mm × 6.6mm |

(1) For more information, see the *Mechanical, Packaging, and Orderable Information*.
(2) The package size (length × width) is a nominal value and includes pins, where applicable.




**Typical Application Schematic**

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# 4 Pin Configuration and Functions

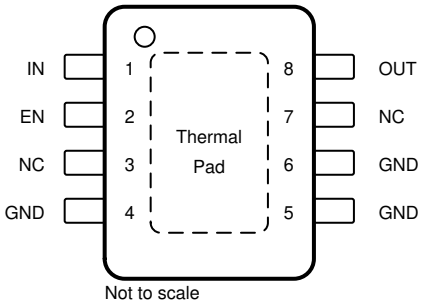



**Figure 4-1. DGN Package, 8-Pin HVSSOP PowerPAD™ (Top View)**

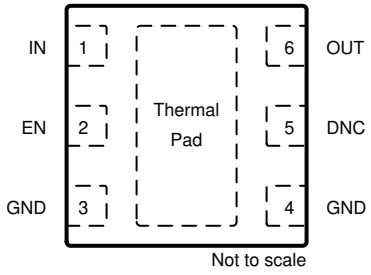



**Figure 4-2. DRV Package, 6-Pin WSON PowerPAD™ (Top View)**

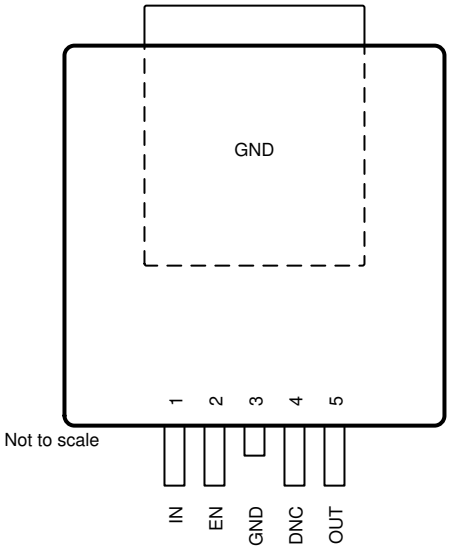



**Figure 4-3. KVU Package, 5-Pin TO-252 (Top View)**

**Table 4-1. Pin Functions**

| PIN | | | | TYPE | DESCRIPTION |
|---|---|---|---|---|---|
| NAME | NO. | | | | |
| | DGN | DRV | KVU | | |
| DNC | — | 5 | 4 | — | Do not connect to a biased voltage. Tie this pin to ground or leave floating. |
| EN | 2 | 2 | 2 | I | Enable input pin. Drive EN greater than $V_{IH}$ to turn on the regulator. Drive EN less than $V_{IL}$ to put the low-dropout (LDO) into shutdown mode. |
| GND | 4, 5, 6 | 3,4 | 3, TAB | — | Ground reference |
| IN | 1 | 1 | 1 | I | Input power-supply pin. For best transient response and to minimize input impedance, use the recommended value or larger ceramic capacitor from IN to ground as listed in the *Recommended Operating Conditions* table and the *Input Capacitor* section. Place the input capacitor as close to the output of the device as possible. |
| NC | 3, 7 | — | — | — | Not internally connected |
| OUT | 8 | 6 | 5 | O | Regulated output voltage pin. A capacitor is required from OUT to ground for stability. For best transient response, use the nominal recommended value or larger ceramic capacitor from OUT to ground; see the *Recommended Operating Conditions* table and the *Output Capacitor* section. Place the output capacitor as close to output of the device as possible. |
| Thermal pad | | | | — | Connect the thermal pad to a large-area GND plane for improved thermal performance. |

# 5 Specifications

## 5.1 Absolute Maximum Ratings

over operating ambient temperature range (unless otherwise noted)(1) (2)

| | | MIN | MAX | UNIT |
|---|---|---|---|---|
| $V_{IN}$ | Unregulated input(3) | –0.3 | 45 | V |
| $V_{EN}$ | Enable input(3) | –0.3 | $V_{IN}$ | V |
| $V_{OUT}$ | Regulated output | –0.3 | 7 | V |
| $T_J$ | Junction temperature range | –40 | 150 | °C |
| $T_{stg}$ | Storage temperature range | –40 | 150 | °C |

(1) Operation outside the *Absolute Maximum Ratings* may cause permanent device damage. *Absolute Maximum Ratings* do not imply functional operation of the device at these or any other conditions beyond those listed under *Recommended Operating Conditions*. If used outside the *Recommended Operating Conditions* but within the *Absolute Maximum Ratings*, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.
(2) All voltage values are with respect to GND.
(3) Absolute maximum voltage, can withstand 45V for 200ms.

## 5.2 ESD Ratings

| | | | | VALUE | UNIT |
|---|---|---|---|---|---|
| $V_{(ESD)}$ | Electrostatic discharge | Human-body model (HBM), per AEC Q100-002(1) | | ±2000 | V |
| | | Charged-device model (CDM), per AEC Q100-011 | Corner pins | ±750 | |
| | | | Other pins | ±500 | |

(1) AEC Q100-002 indicates that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

## 5.3 Recommended Operating Conditions

over operating ambient temperature range (unless otherwise noted)

| | | MIN | MAX | UNIT |
|---|---|---|---|---|
| $V_{IN}$ | Unregulated input voltage | 3 | 40 | V |
| $V_{EN}$ | Enable input voltage | 0 | $V_{IN}$ | V |
| $C_{OUT}$ | Output capacitor requirements(1) | 1 | 200 | µF |
| ESR | Output capacitor ESR requirements(2) | 0.001 | 5 | Ω |
| $T_A$ | Ambient temperature range | –40 | 125 | °C |
| $T_J$ | Junction temperature range | –40 | 150 | °C |

(1) The output capacitance range specified in the table is the effective value.
(2) Relevant ESR value at f = 10kHz.

## 5.4 Thermal Information

| THERMAL METRIC[1] | | TPS7B81-Q1 | | | UNIT |
|---|---|---|---|---|---|
| | | DGN (HVSSOP) | DRV (WSON) | KVU (TO-252) | |
| | | 8 PINS | 6 PINS | 5 PINS | |
| $R_{\theta JA}$ | Junction-to-ambient thermal resistance | 63.9 | 72.8 | 31.1 | °C/W |
| $R_{\theta JC(top)}$ | Junction-to-case (top) thermal resistance | 50.2 | 85.8 | 39.9 | °C/W |
| $R_{\theta JB}$ | Junction-to-board thermal resistance | 22.6 | 37.4 | 9.9 | °C/W |
| $\psi_{JT}$ | Junction-to-top characterization parameter | 1.8 | 2.7 | 4.2 | °C/W |
| $\psi_{JB}$ | Junction-to-board characterization parameter | 22.3 | 37.3 | 9.9 | °C/W |
| $R_{\theta JC(bot)}$ | Junction-to-case (bottom) thermal resistance | 12.1 | 13.8 | 2.8 | °C/W |

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application note.

## 5.5 Electrical Characteristics

over operating ambient temperature range, $T_J$ = –40°C to +150°C, $V_{IN}$ = 14V, and 10µF ceramic output capacitor (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| **SUPPLY VOLTAGE AND CURRENT (IN)** | | | | | | | |
| $V_{IN}$ | Input voltage | | | $V_{OUT(Nom)}$ + $V_{(Dropout)}$ | | 40 | V |
| $I_{(SD)}$ | Shutdown current | EN = 0V | | | 0.3 | 1 | µA |
| $I_{(Q)}$ | Quiescent current | $V_{IN}$ = 6V to 40V, EN ≥ 2V, $I_{OUT}$ = 0mA | | | 1.9 | 3.5 | µA |
| | | $V_{IN}$ = 6V to 40V, EN ≥ 2V, $I_{OUT}$ = 0.2mA | DGN package | | 2.7 | 6.5 | |
| | | | DRV and KVU packages | | 2.7 | 4.5 | |
| $V_{(IN, UVLO)}$ | $V_{IN}$ undervoltage detection | Ramp $V_{IN}$ down until the output turns off | | | | 2.7 | V |
| | | Hysteresis | | | 200 | | mV |
| **ENABLE INPUT (EN)** | | | | | | | |
| $V_{IL}$ | Logic-input low level | | | | | 0.7 | V |
| $V_{IH}$ | Logic-input high level | | | 2 | | | V |
| $I_{EN}$ | Enable current | | | | 10 | | nA |
| **REGULATED OUTPUT (OUT)** | | | | | | | |
| $V_{OUT}$ | Regulated output | $V_{IN}$ = $V_{OUT}$ + $V_{(Dropout)}$ to 40V, $I_{OUT}$ = 1mA to 150mA | | –1.5% | | 1.5% | |
| $V_{(Line-Reg)}$ | Line regulation | $V_{IN}$ = 6V to 40V, $I_{OUT}$ = 10mA | | | | 10 | mV |
| $V_{(Load-Reg)}$ | Load regulation | $V_{IN}$ = 14V, $I_{OUT}$ = 1mA to 150mA | DGN package | | | 20 | mV |
| | | | DRV and KVU packages | | | 10 | |

## 5.5 Electrical Characteristics (continued)

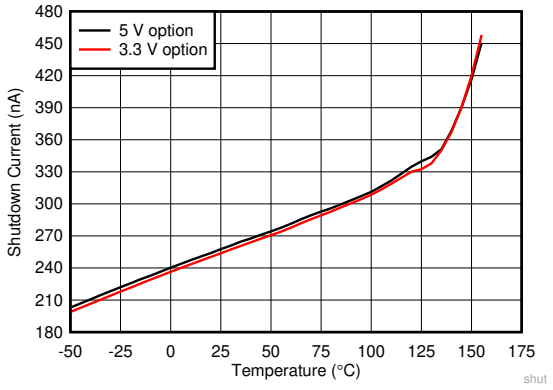
over operating ambient temperature range, $T_J$ = –40°C to +150°C, $V_{IN}$ = 14V, and 10µF ceramic output capacitor (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | | | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|---|
| $V_{(Dropout)}$ | Dropout voltage(1) | $V_{OUT}$ = 5V | $I_{OUT}$ = 150mA | DGN package | | 270 | 540 | mV |
| | | | | DRV and KVU packages | | 325 | 585 | |
| | | | $I_{OUT}$ = 100mA | DGN package | | 180 | 350 | |
| | | | | DRV and KVU packages | | 200 | 390 | |
| | | $V_{OUT}$ = 3.3V | $I_{OUT}$ = 150mA | DGN package | | | 650 | |
| | | | | DRV and KVU packages | | 345 | 675 | |
| | | | $I_{OUT}$ = 100mA | | | 255 | 450 | |
| $I_{OUT}$ | Output current | $V_{OUT}$ in regulation, $V_{IN}$ = 7V for the fixed 5V option, $V_{IN}$ = 5.8V for the fixed 3.3V option | | | 0 | | 150 | mA |
| $I_{(CL)}$ | Output current limit | $V_{OUT}$ short to 90% × $V_{OUT}$ | | | 180 | 510 | 690 | mA |
| PSRR | Power-supply ripple rejection | $V_{(Ripple)}$ = 0.5$V_{PP}$, $I_{OUT}$ = 10mA, frequency = 100Hz, $C_{OUT}$ = 2.2µF | | | | 60 | | dB |
| **OPERATING TEMPERATURE RANGE** | | | | | | | | |
| $T_{(SD)}$ | Junction shutdown temperature | | | | | 175 | | °C |
| $T_{(HYST)}$ | Hysteresis of thermal shutdown | | | | | 20 | | °C |

(1) Dropout is not valid for the 2.5V output because of the minimum input voltage limits.

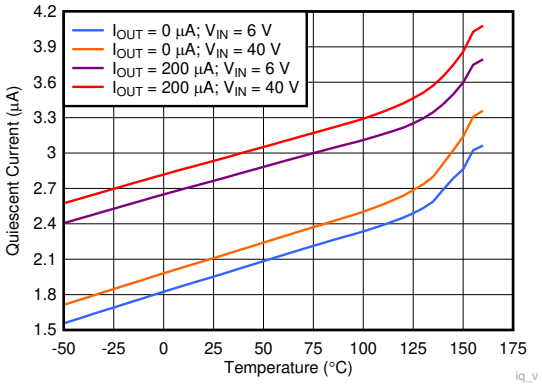
## 5.6 Typical Characteristics

at $T_J$ = –40°C to +150°C, $V_{IN}$ = 14V, and $V_{EN}$ ≥ 2V (unless otherwise noted)



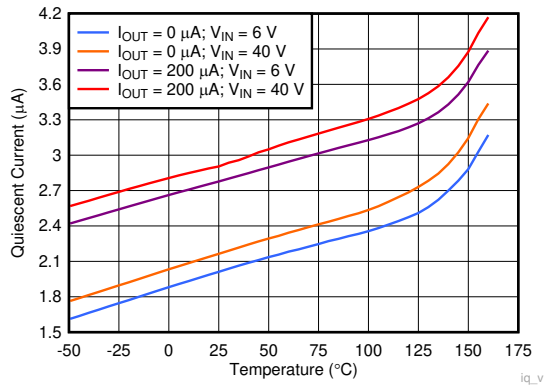

$V_{EN}$ = 0V

**Figure 5-1. Shutdown Current vs Ambient Temperature**



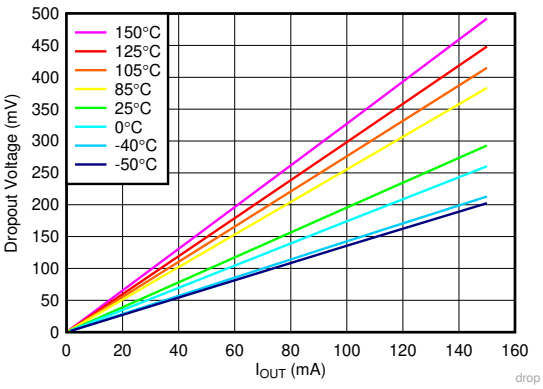

$V_{OUT}$ = 5V

**Figure 5-2. Quiescent Current vs Ambient Temperature**



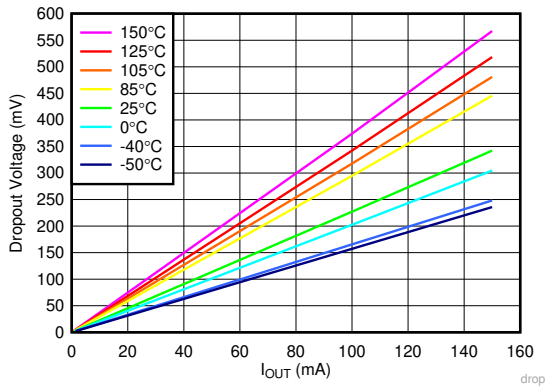

$V_{OUT}$ = 3.3V

**Figure 5-3. Quiescent Current vs Ambient Temperature**



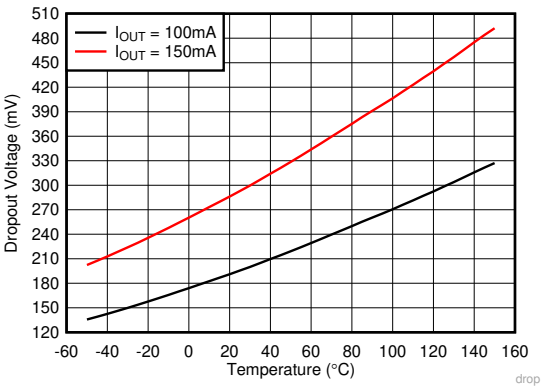

$V_{OUT}$ = 5V, DRV package

**Figure 5-4. Dropout Voltage vs Output Current**




$V_{OUT}$ = 3.3V, DRV package

**Figure 5-5. Dropout Voltage vs Output Current**

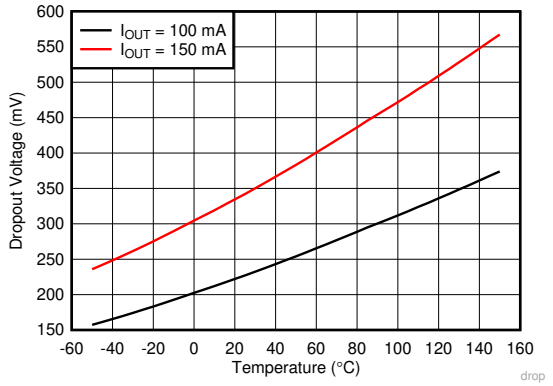



$V_{OUT}$ = 5V

**Figure 5-6. Dropout Voltage vs Ambient Temperature**

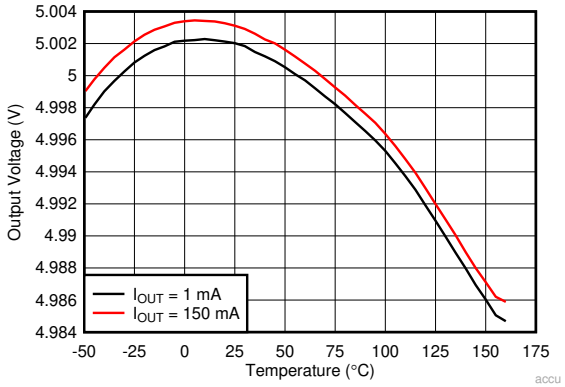
## 5.6 Typical Characteristics (continued)

at $T_J$ = –40°C to +150°C, $V_{IN}$ = 14V, and $V_{EN}$ ≥ 2V (unless otherwise noted)



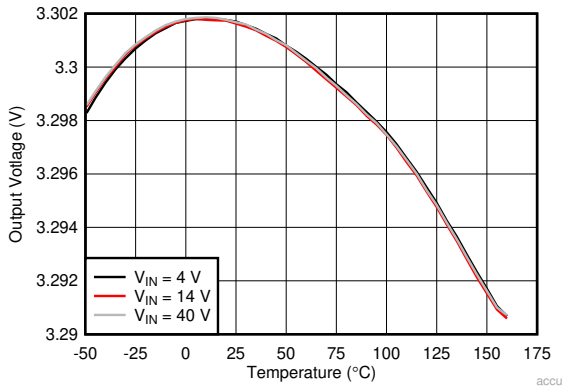

$V_{OUT}$ = 3.3V

**Figure 5-7. Dropout Voltage vs Ambient Temperature**



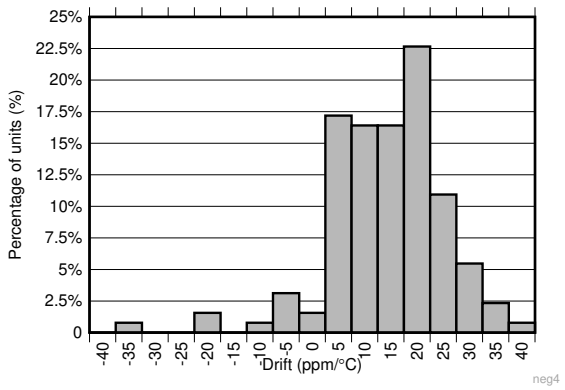

$V_{OUT}$ = 5V

**Figure 5-8. Output Voltage vs Ambient Temperature**



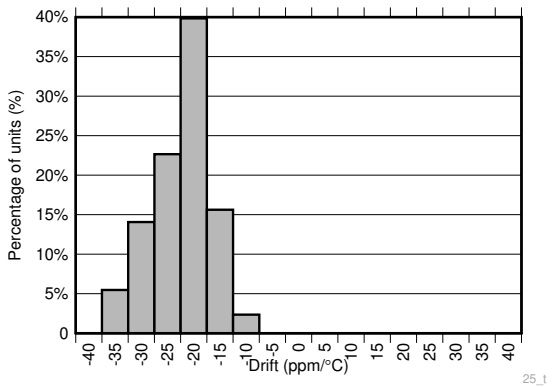

$V_{OUT}$ = 3.3V, $I_{OUT}$ = 1mA

**Figure 5-9. Output Voltage vs Ambient Temperature**



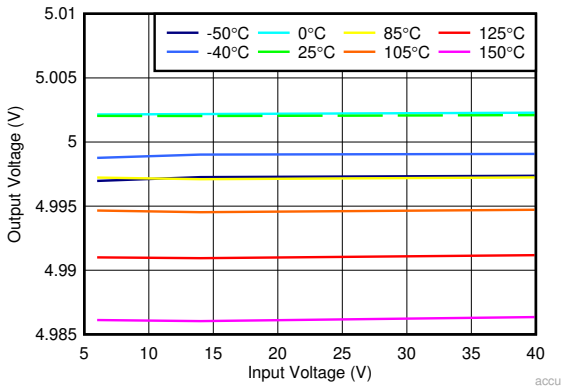

3.3V and 5V options, $I_{OUT}$ = 1mA

**Figure 5-10. Temperature Drift Histogram (–40°C to +25°C)**




3.3V and 5V options, $I_{OUT}$ = 1mA

**Figure 5-11. Temperature Drift Histogram (25°C to 150°C)**

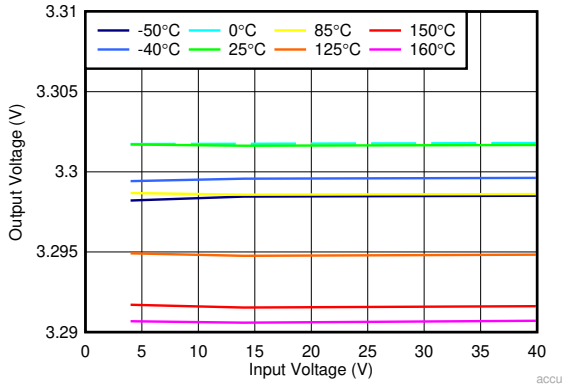



$V_{OUT}$ = 5V, $I_{OUT}$ = 1mA

**Figure 5-12. Output Voltage vs Input Voltage**

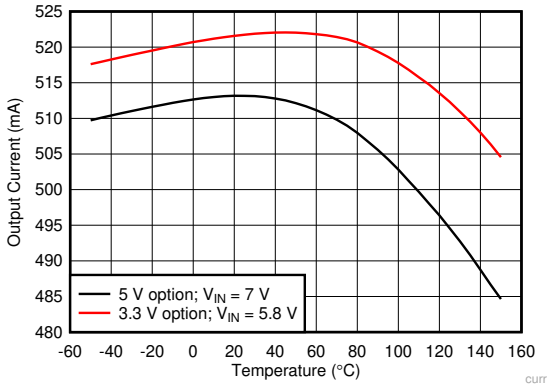
## 5.6 Typical Characteristics (continued)

at $T_J$ = –40°C to +150°C, $V_{IN}$ = 14V, and $V_{EN}$ ≥ 2V (unless otherwise noted)




$V_{OUT}$ = 3.3V, $I_{OUT}$ = 1mA

**Figure 5-13. Output Voltage vs Input Voltage**




$V_{OUT}$ is shorted to 90% × $V_{OUT(NOM)}$

**Figure 5-14. Output Current Limit vs Ambient Temperature**

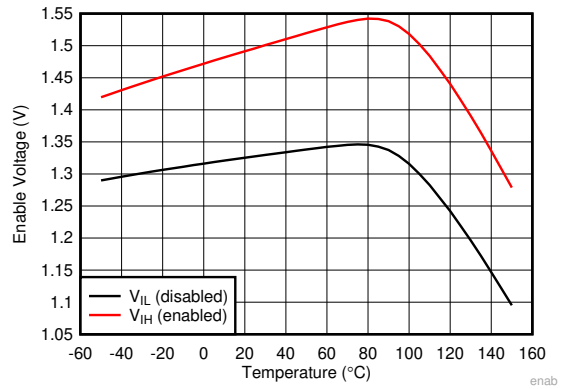



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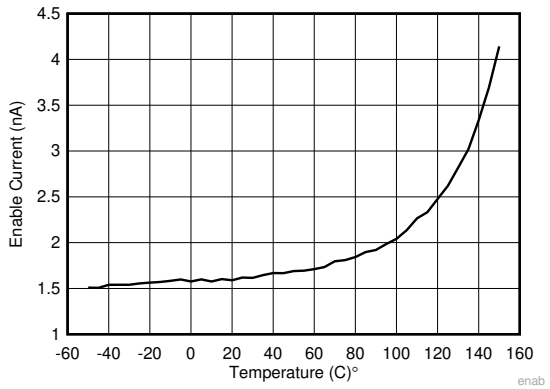
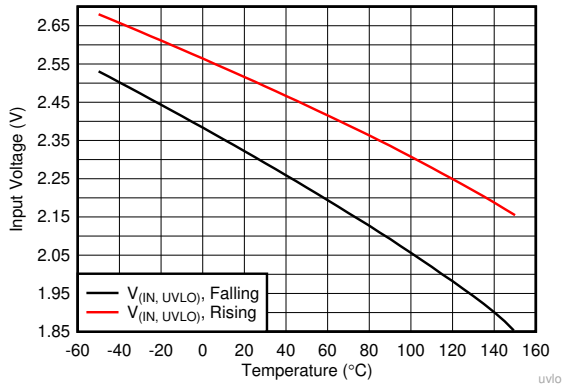
**Figure 5-15. Enable Voltage vs Ambient Temperature**



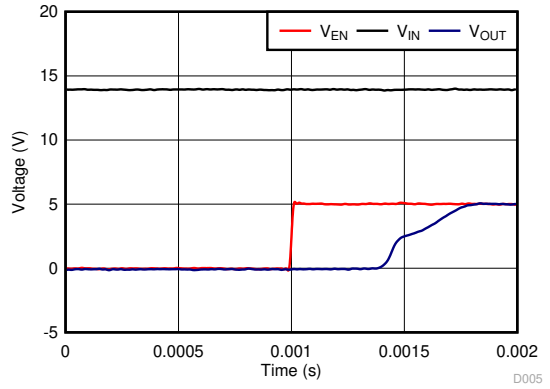

A.

**Figure 5-16. Enable Current vs Ambient Temperature**




A.

**Figure 5-17. UVLO vs Ambient Temperature**

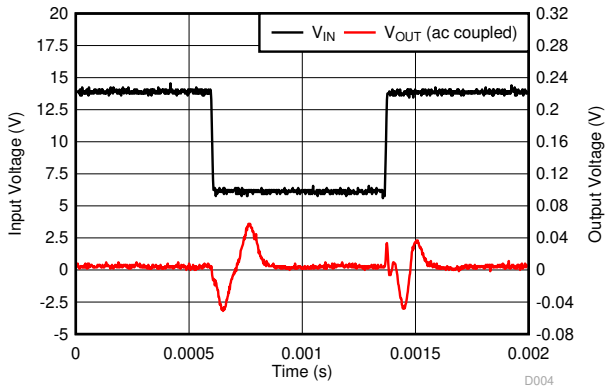



$V_{OUT}$ = 5V, $C_{IN}$ = 1µF, $C_{OUT}$ = 1µF

**Figure 5-18. Startup With Enable**

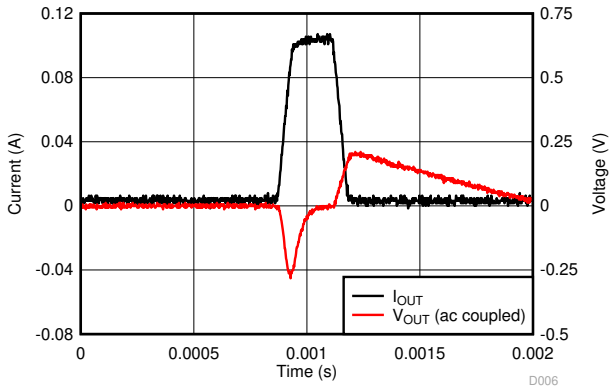
## 5.6 Typical Characteristics (continued)

at $T_J$ = –40°C to +150°C, $V_{IN}$ = 14V, and $V_{EN}$ ≥ 2V (unless otherwise noted)



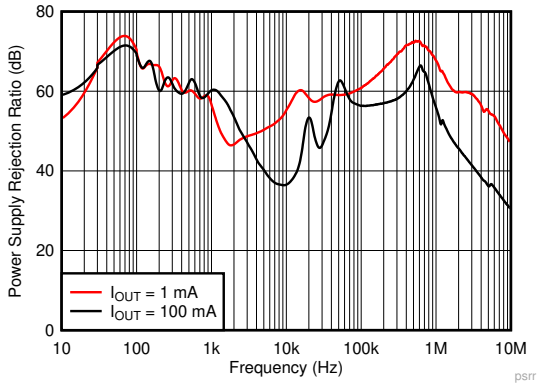

$V_{OUT}$ = 3.3V, $C_{IN}$ = 0µF, $C_{OUT}$ = 1µF, $I_{OUT}$ = 100mA, slew rate = 1V/µs

**Figure 5-19. Line Transient**



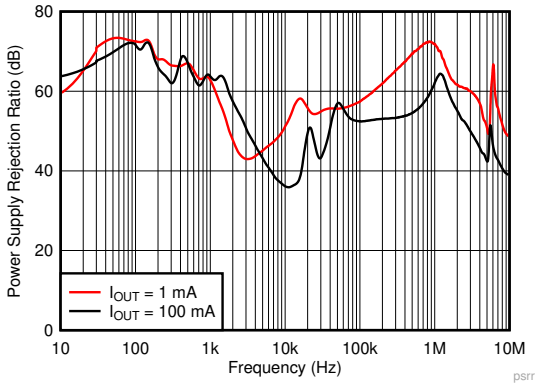

$V_{OUT}$ = 5V, $C_{IN}$ = 1µF, $C_{OUT}$ = 1µF, $I_{OUT}$ = 1mA → 100mA → 1mA, slew rate = 1mA/µs

**Figure 5-20. Load Transient**



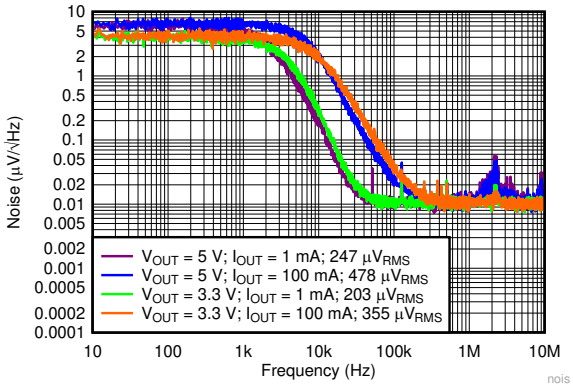

$V_{OUT}$ = 5V, $C_{IN}$ = 0µF, $C_{OUT}$ = 10µF

**Figure 5-21. PSRR vs Frequency**




$V_{OUT}$ = 3.3V, $C_{IN}$ = 0µF, $C_{OUT}$ = 10µF

**Figure 5-22. PSRR vs Frequency**




$C_{IN}$ = 0.1µF, $C_{OUT}$ = 10µF

**Figure 5-23. Noise vs Frequency**

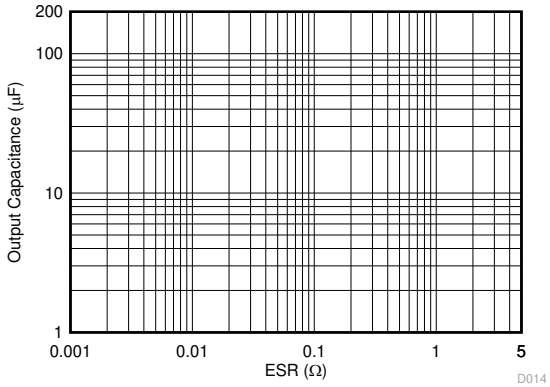


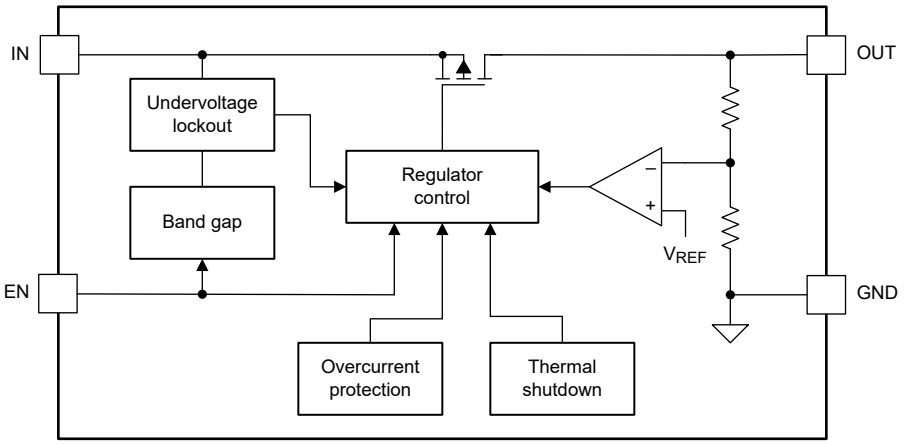

**Figure 5-24. Output Capacitance vs ESR Stability**

# 6 Detailed Description

## 6.1 Overview

The TPS7B81-Q1 is a 40V, 150mA, low-dropout (LDO) linear regulator with ultra-low quiescent current. This voltage regulator consumes only 3µA of quiescent current at light load, and is designed for the automotive always-on application.

## 6.2 Functional Block Diagram




## 6.3 Feature Description

### 6.3.1 Device Enable (EN)

The EN pin is a high-voltage-tolerant pin. A high input activates the device and turns the regulation on. Connect this pin to an external microcontroller or a digital circuit to enable and disable the device, or connect to the IN pin for self-bias applications.

### 6.3.2 Undervoltage Shutdown

This device has an integrated undervoltage lockout (UVLO) circuit to shut down the output if the input voltage ($V_{IN}$) falls below an internal UVLO threshold ($V_{(UVLO)}$). This feature ensures that the regulator does not latch into an unknown state during low-input-voltage conditions. If the input voltage has a negative transient that drops below the UVLO threshold and recovers, the regulator shuts down and powers up with a normal power-up sequence when the input voltage is above the required level.

### 6.3.3 Current Limit

This device features current-limit protection to keep the device in a safe operating area when an overload or output short-to-ground condition occurs. This feature protects the device from excessive power dissipation. For example, during a short-circuit condition on the output, the fault protection limits the current through the pass element to $I_{(LIM)}$ to protect the device from excessive power dissipation.

### 6.3.4 Thermal Shutdown

This device incorporates a thermal shutdown (TSD) circuit as protection from overheating. For continuous normal operation, the junction temperature must not exceed the TSD trip point. If the junction temperature exceeds the TSD trip point, the output turns off. When the junction temperature falls below the TSD trip point minus the thermal shutdown hysteresis, the output turns on again.

## 6.4 Device Functional Modes

### 6.4.1 Operation With $V_{IN}$ Lower Than 3V

The device normally operates with input voltages above 3V. The device can also operate at lower input voltages; the maximum UVLO voltage is 2.7V. The device does not operate at input voltages below the actual UVLO voltage.

### 6.4.2 Operation With $V_{IN}$ Larger Than 3V

When $V_{IN}$ is greater than 3V, if $V_{IN}$ is also higher than the output set value plus the device dropout voltage, $V_{OUT}$ is equal to the set value. Otherwise, $V_{OUT}$ is equal to $V_{IN}$ minus the dropout voltage.

**Table 6-1. Device Functional Mode Comparison**

| OPERATING MODE | PARAMETER | | | |
|---|---|---|---|---|
| Normal mode | $V_{IN} > V_{OUT(nom)} + V_{(Dropout)}$ and $V_{IN} \geq 3V$ | $V_{EN} > V_{IH}$ | $I_{OUT} < I_{CL}$ | $T_J < 160°C$ |
| Dropout mode | $3V \leq V_{IN} < V_{OUT(nom)} + V_{(Dropout)}$ | $V_{EN} > V_{IH}$ | $I_{OUT} < I_{CL}$ | $T_J < 160°C$ |
| Disabled mode (any true condition disables the device) | $V_{IN} < V_{(IN, UVLO)}$ | $V_{EN} < V_{IL}$ | — | $T_J > 160°C$ |

# 7 Application and Implementation

**Note**

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

## 7.1 Application Information

The TPS7B81-Q1 is a 150mA, 40V, low-dropout (LDO) linear regulator with ultra low quiescent current. The PSpice transient model is available for download on the product folder and can be used to evaluate the basic function of the device.

### *7.1.1 Power Dissipation*

Circuit reliability demands that proper consideration is given to device power dissipation, location of the circuit on the printed circuit board (PCB), and correct sizing of the thermal plane. The PCB area around the regulator must be as free as possible of other heat-generating devices that cause added thermal stresses.

As a first-order approximation, power dissipation in the regulator depends on the input-to-output voltage difference and load conditions. $P_D$ can be approximated using Equation 1:

$$P_D = (V_{OUT} - V_{IN}) \times I_{OUT} \quad (1)$$

An important note is that power dissipation can be minimized, and thus greater efficiency achieved, by proper selection of the system voltage rails. Proper selection allows the minimum input-to-output voltage differential to be obtained. The low dropout of the device allows for maximum efficiency across a wide range of output voltages.

The main heat conduction path for the device is through the thermal pad on the package. As such, the thermal pad must be soldered to a copper pad area under the device. This pad area contains an array of plated vias that conduct heat to any inner plane areas or to a bottom-side copper plane.

The maximum power dissipation determines the maximum allowable junction temperature ($T_J$) for the device. Power dissipation and junction temperature are most often related by the junction-to-ambient thermal resistance ($R_{\theta JA}$) of the combined PCB, device package, and the temperature of the ambient air ($T_A$), according to Equation 2. The equation is rearranged for output current in Equation 3.

$$T_J = T_A + R_{\theta JA} \times P_D \quad (2)$$

$$I_{OUT} = \left(T_J - T_A\right) \div \left[R_{\theta JA} \times (V_{IN} - V_{OUT})\right] \quad (3)$$

Unfortunately, this thermal resistance ($R_{\theta JA}$) is highly dependent on the heat-spreading capability built into the particular PCB design, and therefore varies according to the total copper area, copper weight, and location of the planes. The $R_{\theta JA}$ recorded in the v table is determined by the JEDEC standard, PCB, and copper-spreading area, and is only used as a relative measure of package thermal performance. Note that for a well-designed thermal layout, $R_{\theta JA}$ is actually the sum of the package junction-to-case (bottom) thermal resistance ($R_{\theta JCbot}$) plus the thermal resistance contribution by the PCB copper.

Figure 7-1 through Figure 7-6 show the functions of $R_{\theta JA}$ and $\psi_{JB}$ vs copper area and thickness. These plots are generated with a 101.6mm x 101.6mm x 1.6mm PCB of two and four layers. For the four layer board, inner planes use 1oz copper thickness. Outer layers are simulated with both 1oz and 2oz copper thickness. A 2x 1 array of thermal vias of 300µm drill diameter and 25µm Cu plating is located beneath the thermal pad of the device. The thermal vias connect the top layer, the bottom layer and, in the case of the 4-layer board, the first inner GND plane. Each of the layers has a copper plane of equal area.

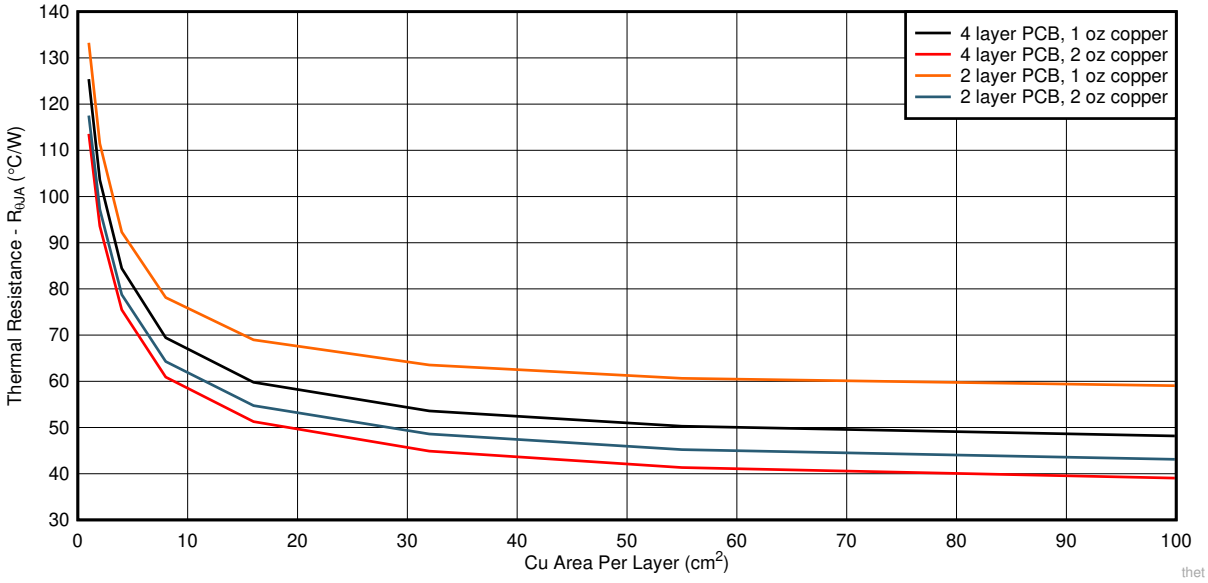



**Figure 7-1. $R_{\theta JA}$ versus Cu Area for the WSON (DRV) Package**

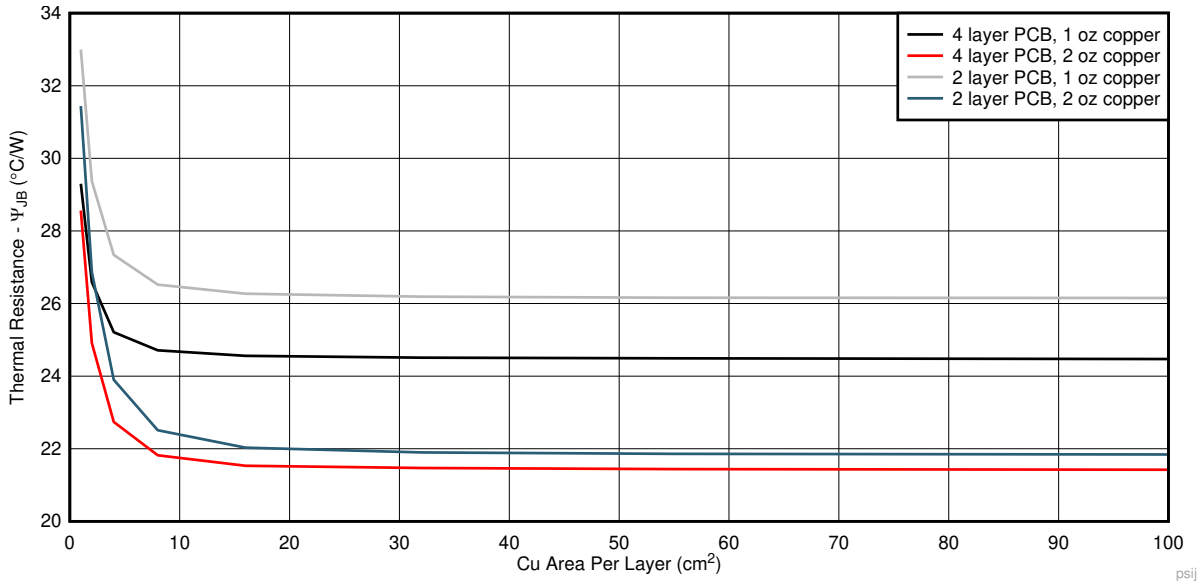



**Figure 7-2. $\psi_{JB}$ versus Cu Area for the WSON (DRV) Package**

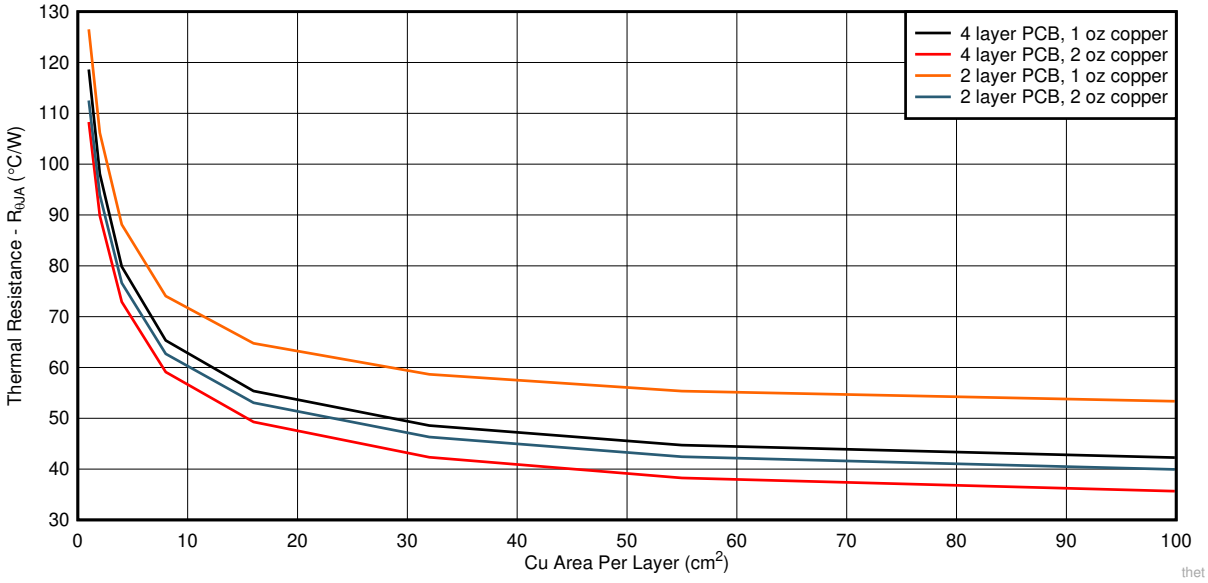



**Figure 7-3. $R_{\theta JA}$ versus Cu Area for the HVSSOP (DGN) Package**

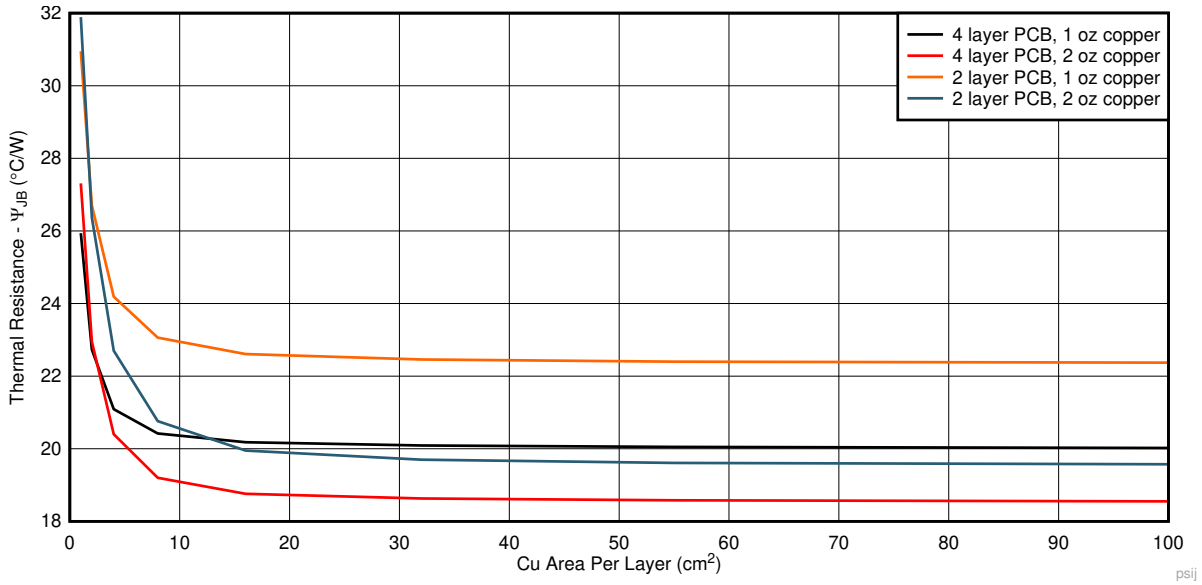



**Figure 7-4. $\Psi_{JB}$ versus Cu Area for the HVSSOP (DGN) Package**

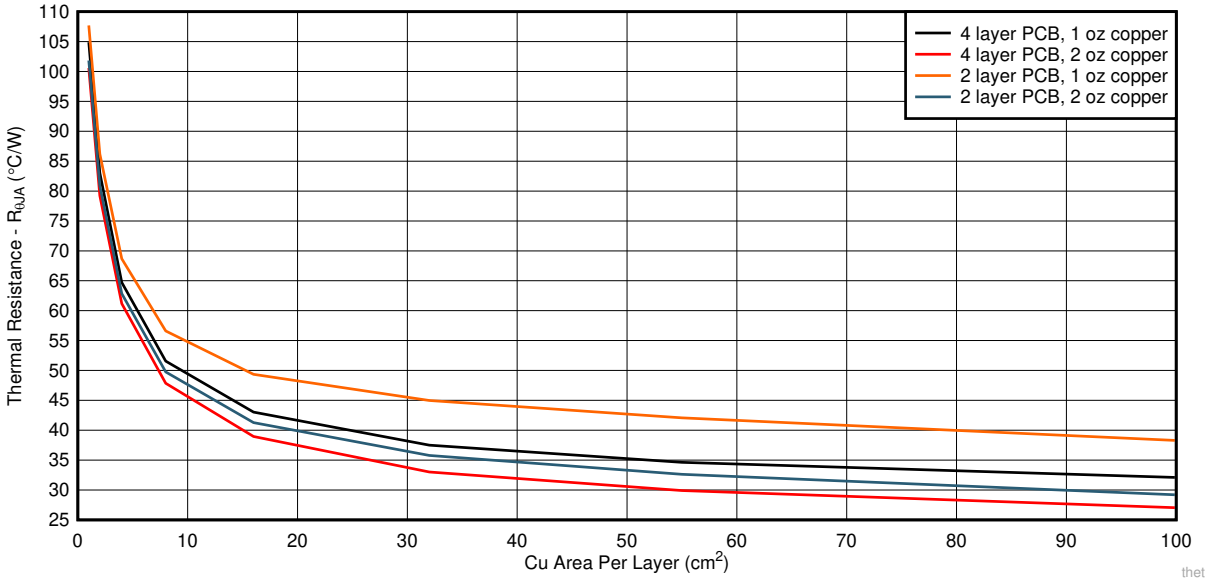



**Figure 7-5. $R_{\theta JA}$ versus Cu Area for the TO-252 (KVU) Package**

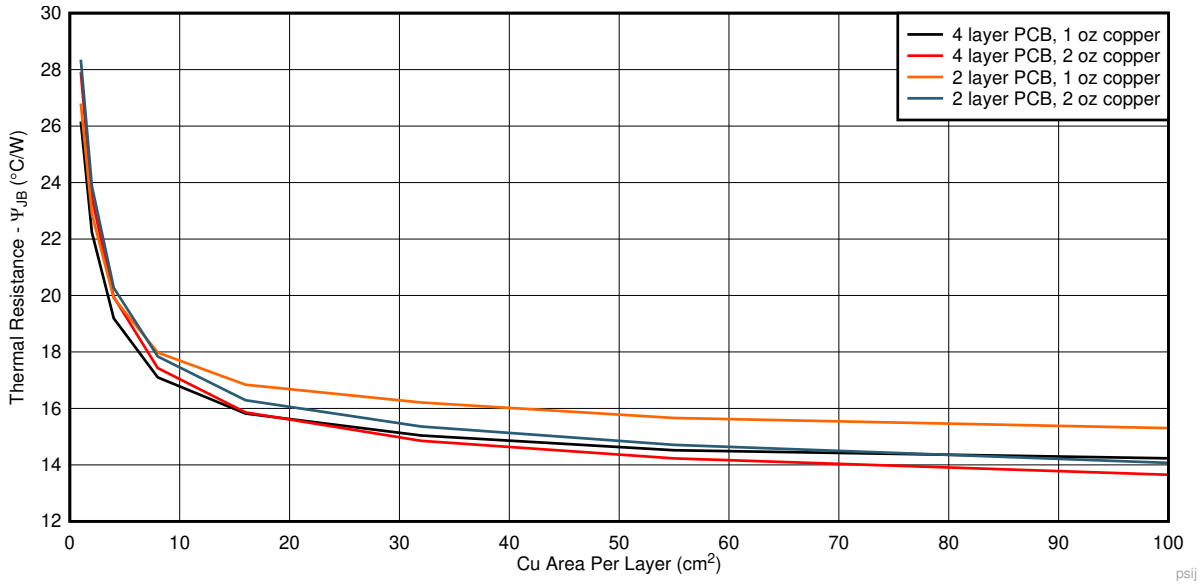



**Figure 7-6. $\Psi_{JB}$ versus Cu Area for the TO-252 (KVU) Package**

#### 7.1.1.1 Estimating Junction Temperature

The JEDEC standard now recommends the use of psi (Ψ) thermal metrics to estimate the junction temperatures of the LDO when in-circuit on a typical PCB board application. These metrics are not strictly speaking thermal resistances, but rather offer practical and relative means of estimating junction temperatures. These psi metrics are determined to be significantly independent of the copper-spreading area. The key thermal metrics ($\Psi_{JT}$ and $\Psi_{JB}$) are given in the *Section 5.4* table and are used in accordance with Equation 4.

$$\Psi_{JT}: T_J = T_T + \Psi_{JT} \times PD$$
$$\Psi_{JB}: T_J = T_B + \Psi_{JB} \times PD \quad (4)$$

where:

- $P_D$ is the power dissipated as explained in Equation 1
- $T_T$ is the temperature at the center-top of the device package
- $T_B$ is the PCB surface temperature measured 1mm from the device package and centered on the package edge

## 7.2 Typical Application

Figure 7-7 shows a typical application circuit for the TPS7B81-Q1. Different external component values can be used, depending on the end application. An application may require a larger output capacitor during fast load steps to prevent a large drop on the output voltage. TI recommends using a low-equivalent series resistance (ESR) ceramic capacitor with an X5R- or X7R-type dielectric.

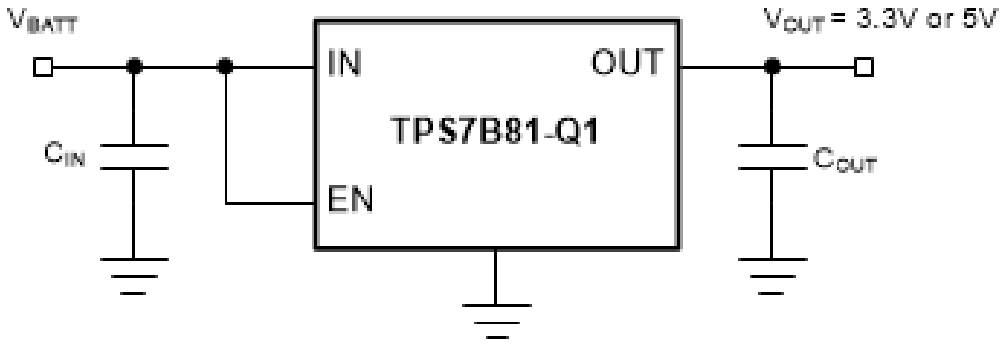



**Figure 7-7. TPS7B81-Q1 Typical Application Schematic**

### 7.2.1 Design Requirements

Use the parameters listed in Table 7-1 for this design example.

**Table 7-1. Design Requirements Parameters**

| PARAMETER | VALUE |
|---|---|
| Input voltage range | 3V to 40V |
| Output voltage | 5V or 3.3V |
| Output current | 150mA maximum |

### 7.2.2 Detailed Design Procedure

To begin the design process, determine the following:

- Input voltage range
- Output voltage
- Output current

#### 7.2.2.1 Input Capacitor

Although an input capacitor is not required for stability, good analog design practice is to connect a 10µF to 22µF capacitor from IN to GND. This capacitor counteracts reactive input sources and improves transient response, input ripple rejection, and PSRR. The voltage rating must be greater than the maximum input voltage.

#### 7.2.2.2 Output Capacitor

To confirm the stability of the TPS7B81-Q1, the device requires an output capacitor with a value in the range from 1µF to 200µF and with an ESR range between 0.001Ω and 5Ω. TI recommends selecting a ceramic capacitor with low ESR to improve the load transient response.

### *7.2.3 Application Curve*

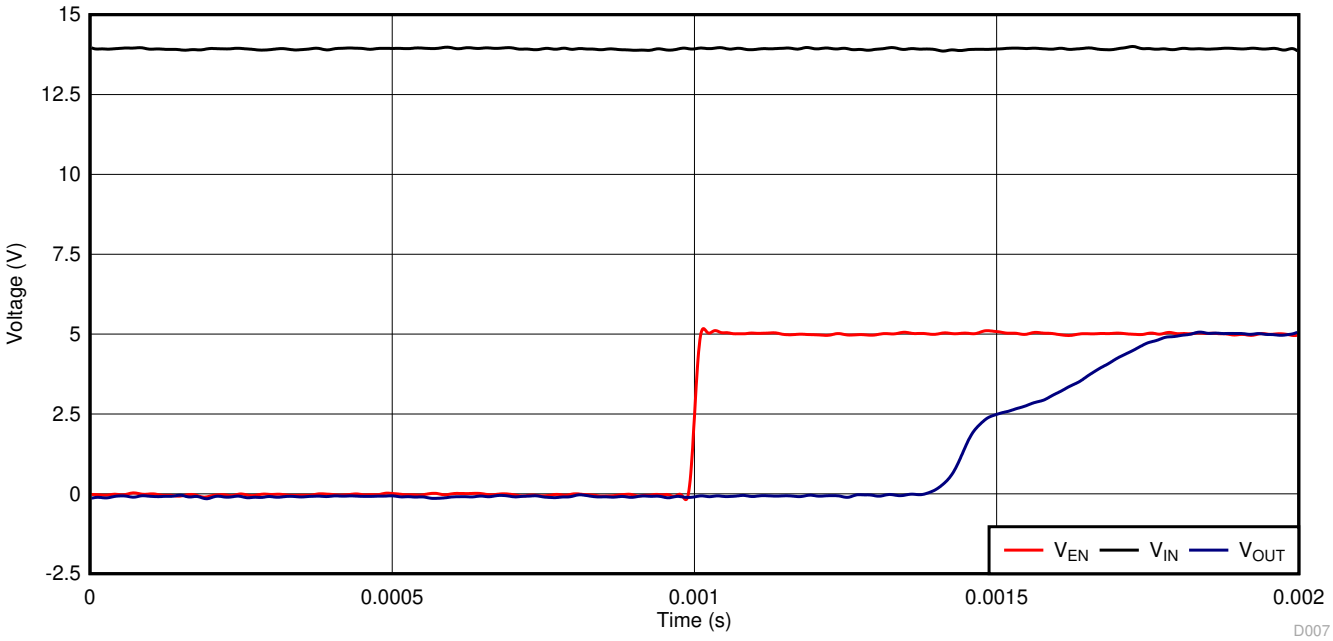



**Figure 7-8. TPS7B81-Q1 Power-Up Waveform (5V)**

## 7.3 Power Supply Recommendations

The device is designed to operate from an input-voltage supply range from 3V to 40V. The input supply must be well regulated. If the input supply is located more than a few inches from the TPS7B81-Q1, TI recommends adding a capacitor with a value greater than or equal to 10µF with a 0.1µF bypass capacitor in parallel at the input.

## 7.4 Layout

### *7.4.1 Layout Guidelines*

Layout is an important step for LDO power supplies, especially for high-voltage and large-output-current supplies. If the layout is not carefully designed, the regulator can fail to deliver enough output current because of thermal limitations. To improve the thermal performance of the device, and to maximize the current output at high ambient temperature, spread the copper under the thermal pad as far as possible and put enough thermal vias on the copper under the thermal pad. Figure 7-9 shows an example layout.

### 7.4.2 Layout Example

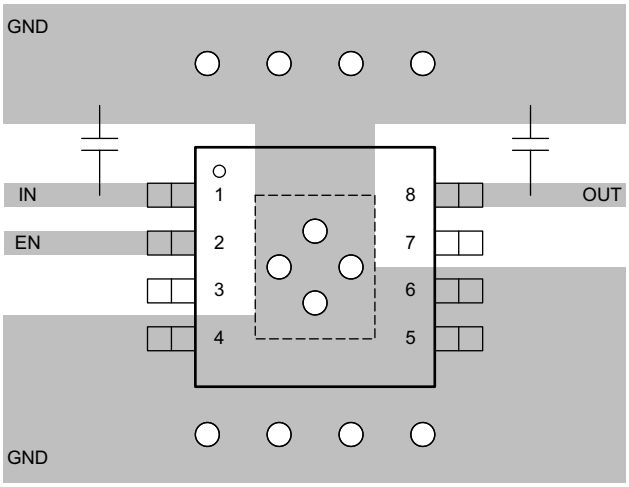



**Figure 7-9. TPSB81-Q1 Example Layout Diagram**

# 8 Device and Documentation Support

## 8.1 Device Support

### *8.1.1 Device Nomenclature*

**Table 8-1. Available Options**

| PRODUCT[1] | DESCRIPTION |
|---|---|
| TPS7B81**xx**Q**(W)yyyz**Q1 | **xx** is the nominal output voltage (for example, 50 = 5.0V, 33 = 3.3V).<br>**Q** indicates that this device is a grade-1 device in accordance with the AEC-Q100 standard.<br>**yyy** is the package designator.<br>**z** is the reel quantity.<br>**Q1** indicates that this device is an automotive grade (AEC-Q100) device. |

(1) For the most current package and ordering information see the Package Option Addendum at the end of this document, or see the TI website at www.ti.com.

## 8.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

## 8.3 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

## 8.4 Trademarks

PowerPAD™ and TI E2E™ are trademarks of Texas Instruments.
All trademarks are the property of their respective owners.

## 8.5 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

## 8.6 Glossary

TI Glossary — This glossary lists and explains terms, acronyms, and definitions.

# 9 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

| Changes from Revision E (June 2025) to Revision F (September 2025) | Page |
|---|---|
| • Added WSON with wettable flanks (DRV) package to document | 1 |
| • Added *Device Nomenclature* section | 20 |

| Changes from Revision D (June 2020) to Revision E (June 2025) | Page |
|---|---|
| • Added functional safety bullets to *Features* section | 1 |
| • Changed power FET from NMOS to PMOS in *Functional Block Diagram* | 11 |

# 10 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

## PACKAGING INFORMATION

| Orderable part number | Status (1) | Material type (2) | Package \| Pins | Package qty \| Carrier | RoHS (3) | Lead finish/ Ball material (4) | MSL rating/ Peak reflow (5) | Op temp (°C) | Part marking (6) |
|---|---|---|---|---|---|---|---|---|---|
| TPS7B8125QDGNRQ1 | Active | Production | HVSSOP (DGN) \| 8 | 2500 \| LARGE T&R | Yes | NIPDAUAG | Level-2-260C-1 YEAR | -40 to 150 | 26GX |
| TPS7B8125QDGNRQ1.A | Active | Production | HVSSOP (DGN) \| 8 | 2500 \| LARGE T&R | Yes | NIPDAUAG | Level-2-260C-1 YEAR | -40 to 150 | 26GX |
| TPS7B8133QDGNRQ1 | Active | Production | HVSSOP (DGN) \| 8 | 2500 \| LARGE T&R | Yes | NIPDAUAG | Level-2-260C-1 YEAR | -40 to 150 | 1VTX |
| TPS7B8133QDGNRQ1.A | Active | Production | HVSSOP (DGN) \| 8 | 2500 \| LARGE T&R | Yes | NIPDAUAG | Level-2-260C-1 YEAR | -40 to 150 | 1VTX |
| TPS7B8133QDRVRQ1 | Active | Production | WSON (DRV) \| 6 | 3000 \| LARGE T&R | Yes | NIPDAU | Level-2-260C-1 YEAR | -40 to 150 | 1X2H |
| TPS7B8133QDRVRQ1.A | Active | Production | WSON (DRV) \| 6 | 3000 \| LARGE T&R | Yes | NIPDAU | Level-2-260C-1 YEAR | -40 to 150 | 1X2H |
| TPS7B8133QKVURQ1 | Active | Production | TO-252 (KVU) \| 5 | 2500 \| LARGE T&R | Yes | SN | Level-3-260C-168 HR | -40 to 150 | 7B8133Q1 |
| TPS7B8133QKVURQ1.A | Active | Production | TO-252 (KVU) \| 5 | 2500 \| LARGE T&R | Yes | SN | Level-3-260C-168 HR | -40 to 150 | 7B8133Q1 |
| TPS7B8133QWDRVRQ1 | Active | Production | WSON (DRV) \| 6 | 3000 \| LARGE T&R | Yes | SN | Level-1-260C-UNLIM | -40 to 150 | 3NGH |
| TPS7B8150QDGNRQ1 | Active | Production | HVSSOP (DGN) \| 8 | 2500 \| LARGE T&R | Yes | NIPDAUAG | Level-2-260C-1 YEAR | -40 to 150 | 1VUX |
| TPS7B8150QDGNRQ1.A | Active | Production | HVSSOP (DGN) \| 8 | 2500 \| LARGE T&R | Yes | NIPDAUAG | Level-2-260C-1 YEAR | -40 to 150 | 1VUX |
| TPS7B8150QDRVRQ1 | Active | Production | WSON (DRV) \| 6 | 3000 \| LARGE T&R | Yes | NIPDAU | Level-2-260C-1 YEAR | -40 to 150 | 1WNH |
| TPS7B8150QDRVRQ1.A | Active | Production | WSON (DRV) \| 6 | 3000 \| LARGE T&R | Yes | NIPDAU | Level-2-260C-1 YEAR | -40 to 150 | 1WNH |
| TPS7B8150QKVURQ1 | Active | Production | TO-252 (KVU) \| 5 | 2500 \| LARGE T&R | Yes | SN | Level-3-260C-168 HR | -40 to 150 | 7B8150Q1 |
| TPS7B8150QKVURQ1.A | Active | Production | TO-252 (KVU) \| 5 | 2500 \| LARGE T&R | Yes | SN | Level-3-260C-168 HR | -40 to 150 | 7B8150Q1 |
| TPS7B8150QWDRVRQ1 | Active | Production | WSON (DRV) \| 6 | 3000 \| LARGE T&R | Yes | SN | Level-1-260C-UNLIM | -40 to 150 | 3NHH |

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.



**OTHER QUALIFIED VERSIONS OF TPS7B81-Q1 :**

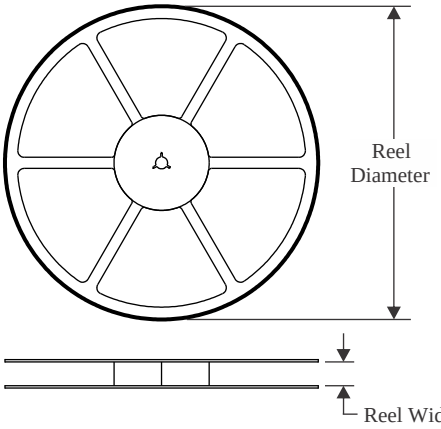
- Catalog : TPS7B81

NOTE: Qualified Version Definitions:

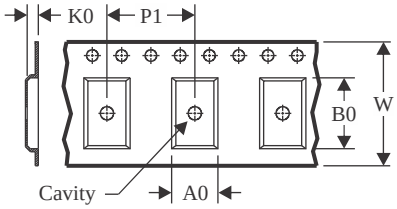
- Catalog - TI's standard catalog product

## TAPE AND REEL INFORMATION

**REEL DIMENSIONS**

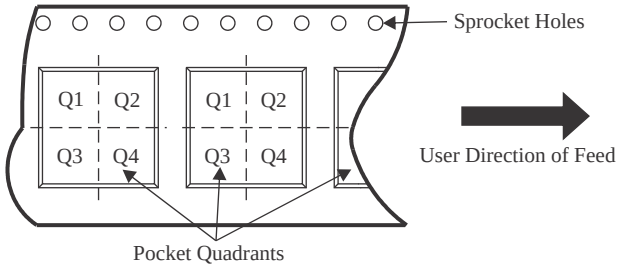



**TAPE DIMENSIONS**




| | |
|---|---|
| A0 | Dimension designed to accommodate the component width |
| B0 | Dimension designed to accommodate the component length |
| K0 | Dimension designed to accommodate the component thickness |
| W | Overall width of the carrier tape |
| P1 | Pitch between successive cavity centers |

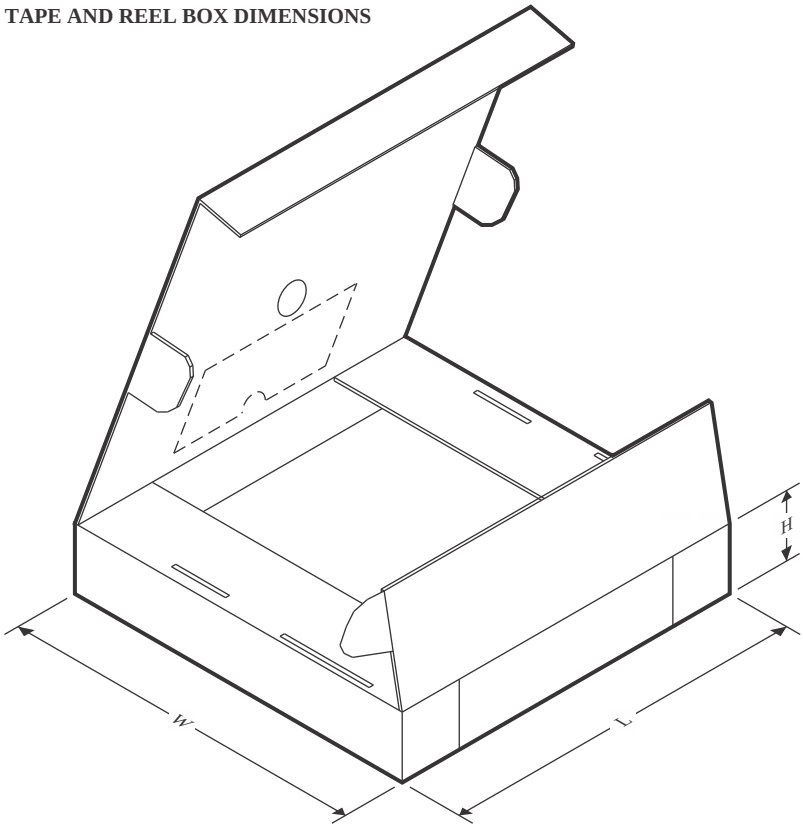
**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**




*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| TPS7B8125QDGNRQ1 | HVSSOP | DGN | 8 | 2500 | 330.0 | 12.4 | 5.3 | 3.4 | 1.4 | 8.0 | 12.0 | Q1 |
| TPS7B8133QDGNRQ1 | HVSSOP | DGN | 8 | 2500 | 330.0 | 12.4 | 5.3 | 3.4 | 1.4 | 8.0 | 12.0 | Q1 |
| TPS7B8133QDRVRQ1 | WSON | DRV | 6 | 3000 | 180.0 | 8.4 | 2.3 | 2.3 | 1.15 | 4.0 | 8.0 | Q2 |
| TPS7B8133QKVURQ1 | TO-252 | KVU | 5 | 2500 | 330.0 | 16.4 | 6.9 | 10.5 | 2.7 | 8.0 | 16.0 | Q2 |
| TPS7B8133QWDRVRQ1 | WSON | DRV | 6 | 3000 | 180.0 | 8.4 | 2.3 | 2.3 | 1.15 | 4.0 | 8.0 | Q2 |
| TPS7B8150QDGNRQ1 | HVSSOP | DGN | 8 | 2500 | 330.0 | 12.4 | 5.3 | 3.4 | 1.4 | 8.0 | 12.0 | Q1 |
| TPS7B8150QDRVRQ1 | WSON | DRV | 6 | 3000 | 180.0 | 8.4 | 2.3 | 2.3 | 1.15 | 4.0 | 8.0 | Q2 |
| TPS7B8150QKVURQ1 | TO-252 | KVU | 5 | 2500 | 330.0 | 16.4 | 6.9 | 10.5 | 2.7 | 8.0 | 16.0 | Q2 |
| TPS7B8150QWDRVRQ1 | WSON | DRV | 6 | 3000 | 180.0 | 8.4 | 2.3 | 2.3 | 1.15 | 4.0 | 8.0 | Q2 |

TAPE AND REEL BOX DIMENSIONS

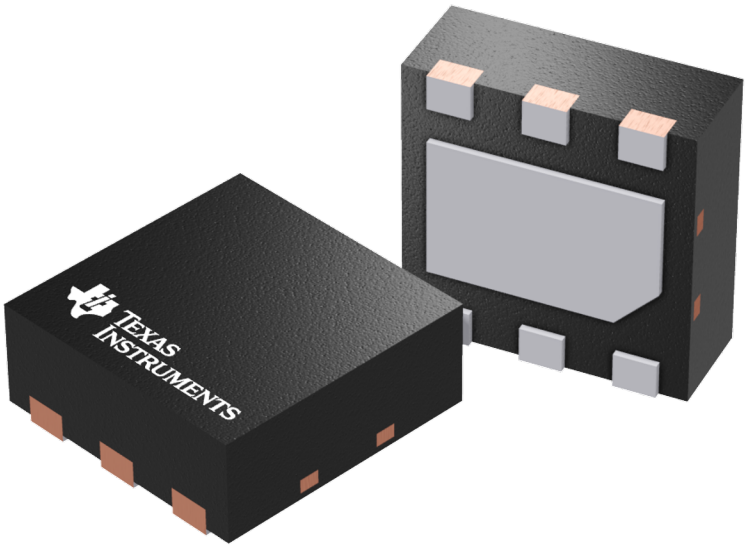



*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|---|---|---|---|---|---|---|---|
| TPS7B8125QDGNRQ1 | HVSSOP | DGN | 8 | 2500 | 366.0 | 364.0 | 50.0 |
| TPS7B8133QDGNRQ1 | HVSSOP | DGN | 8 | 2500 | 366.0 | 364.0 | 50.0 |
| TPS7B8133QDRVRQ1 | WSON | DRV | 6 | 3000 | 210.0 | 185.0 | 35.0 |
| TPS7B8133QKVURQ1 | TO-252 | KVU | 5 | 2500 | 340.0 | 340.0 | 38.0 |
| TPS7B8133QWDRVRQ1 | WSON | DRV | 6 | 3000 | 210.0 | 185.0 | 35.0 |
| TPS7B8150QDGNRQ1 | HVSSOP | DGN | 8 | 2500 | 366.0 | 364.0 | 50.0 |
| TPS7B8150QDRVRQ1 | WSON | DRV | 6 | 3000 | 210.0 | 185.0 | 35.0 |
| TPS7B8150QKVURQ1 | TO-252 | KVU | 5 | 2500 | 340.0 | 340.0 | 38.0 |
| TPS7B8150QWDRVRQ1 | WSON | DRV | 6 | 3000 | 210.0 | 185.0 | 35.0 |

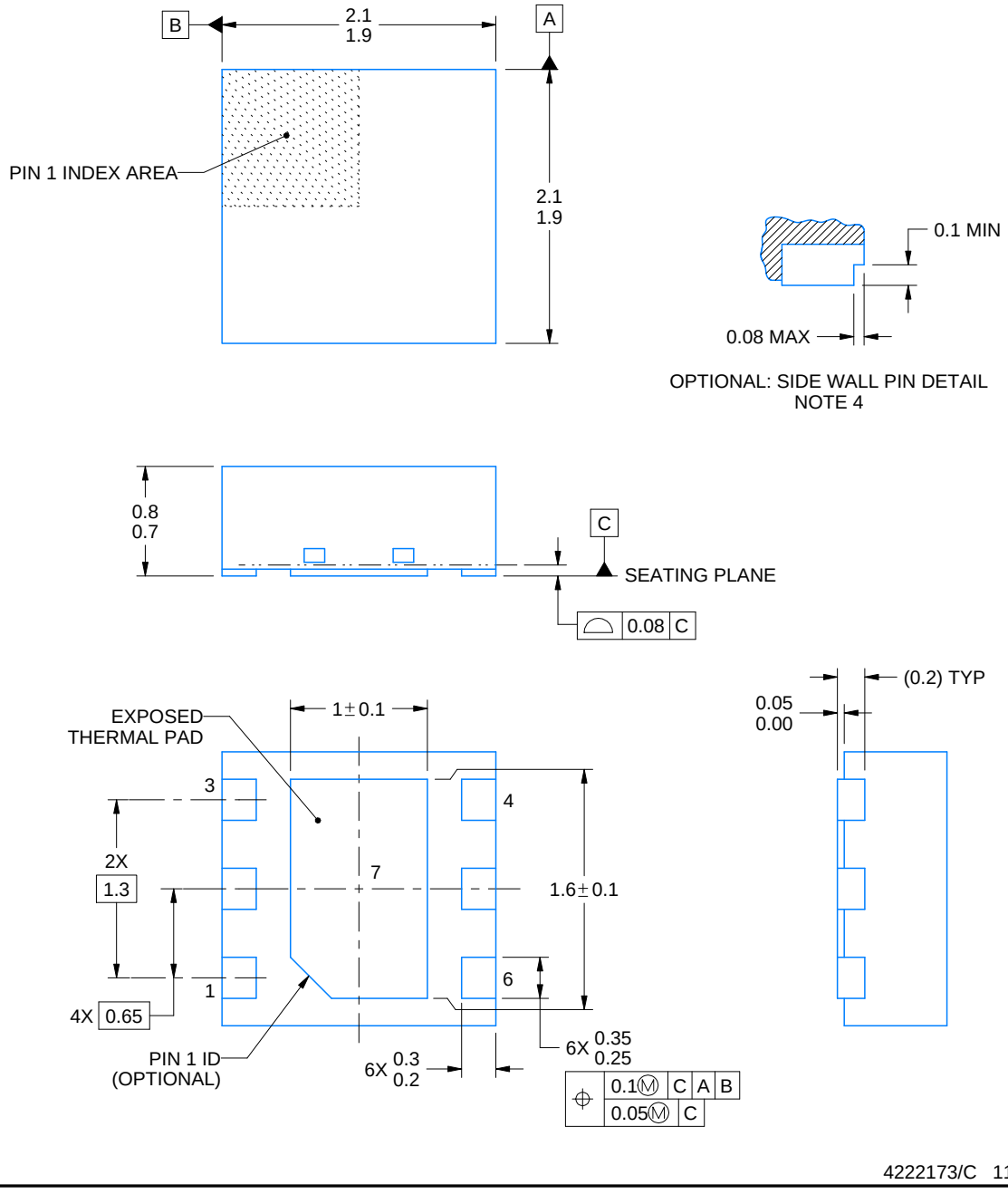
# DRV 6 WSON - 0.8 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



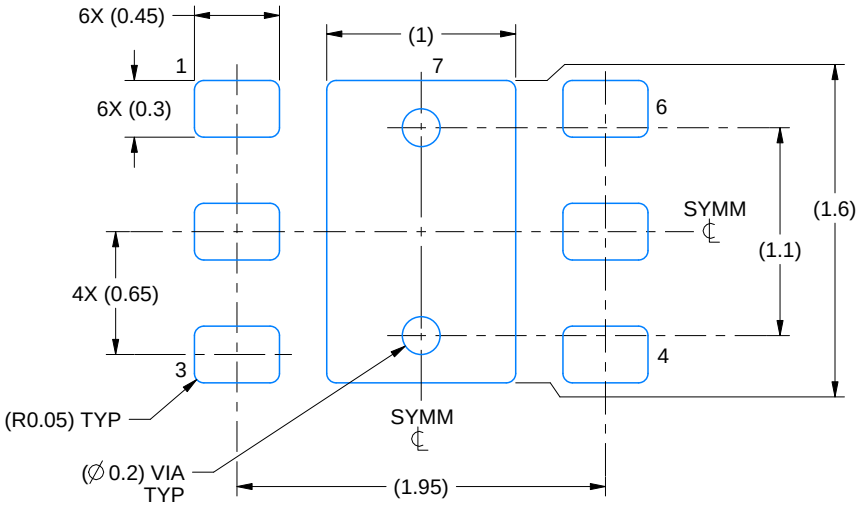

Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

PLASTIC SMALL OUTLINE - NO LEAD

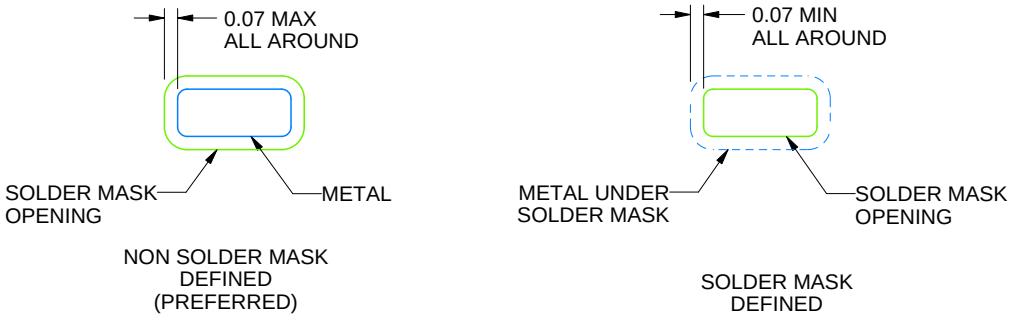



NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.
4. Minimum 0.1 mm solder wetting on pin side wall. Available for wettable flank version only.




LAND PATTERN EXAMPLE
SCALE:25X




SOLDER MASK DETAILS

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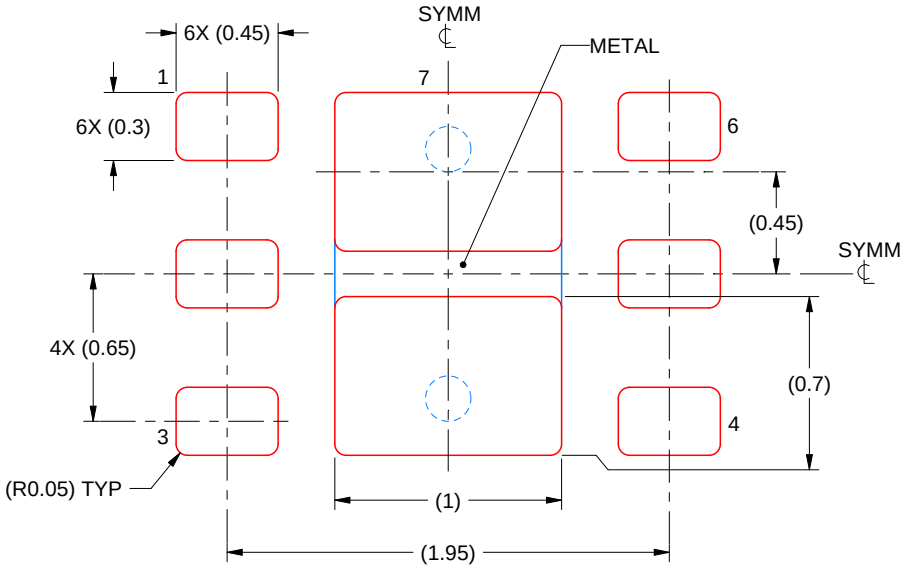
NOTES: (continued)

5. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
6. Vias are optional depending on application, refer to device data sheet. If some or all are implemented, recommended via locations are shown.




SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

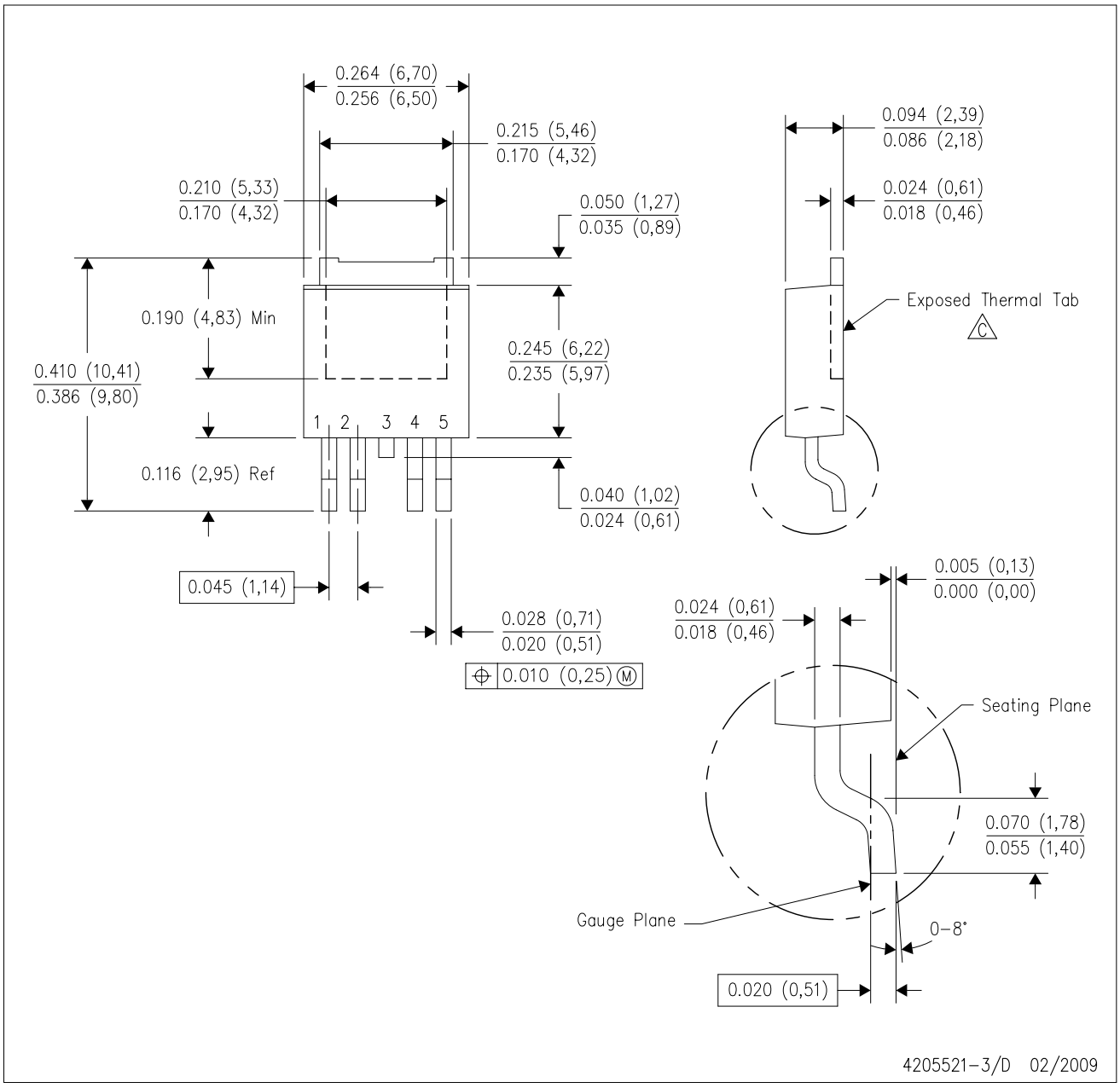
EXPOSED PAD #7
88% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:30X

4222173/C 11/2025

NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

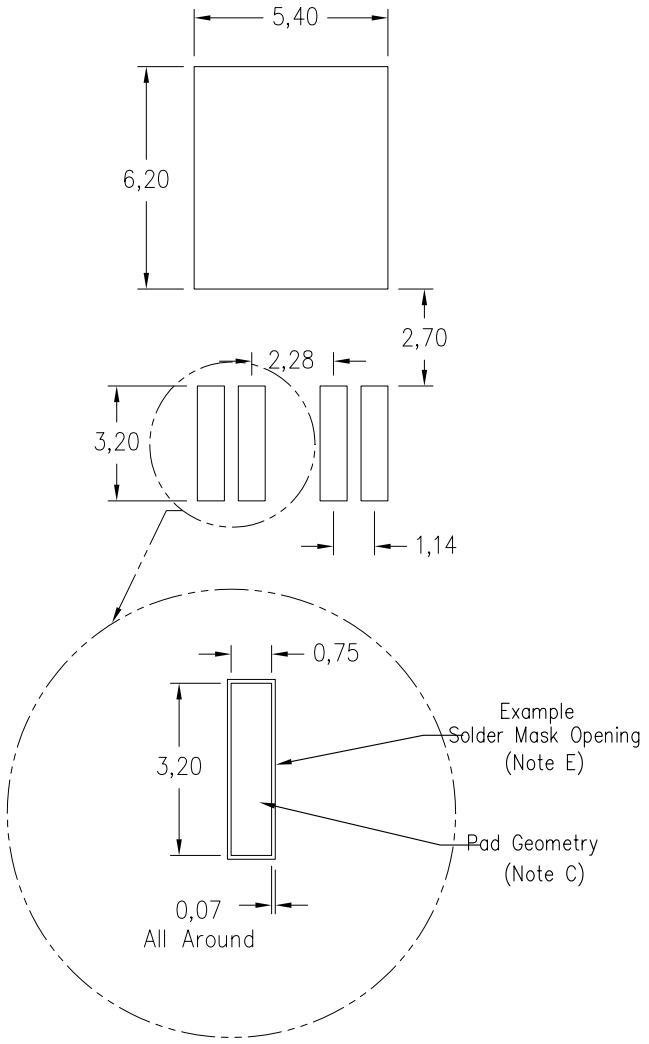
KVU (R–PSFM–G5) PLASTIC FLANGE–MOUNT PACKAGE



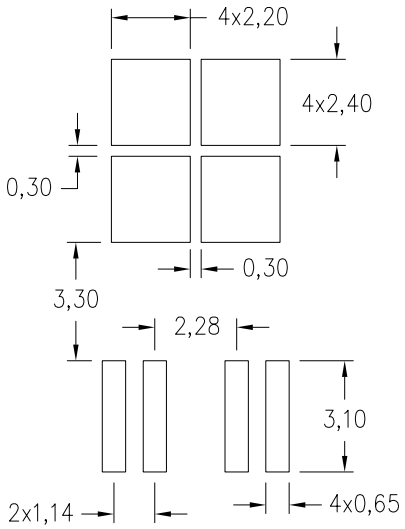

NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. The center lead is in electrical contact with the exposed thermal tab.
D. Body Dimensions do not include mold flash or protrusions. Mold flash and protrusion shall not exceed 0.006 (0,15) per side.
E. Falls within JEDEC TO–252 variation AD.

# KVU (R–PSFM–G5) PLASTIC FLANGE MOUNT PACKAGE

Example Board Layout




Stencil Openings
Based on a stencil thickness
of .127mm (.005inch).




63% solder coverage on center pad

4211592–3/B 03/12

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–SM–782 is an alternate information source for PCB land pattern designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for recommended solder mask tolerances and via tenting recommendations for vias placed in thermal pad.

# GENERIC PACKAGE VIEW

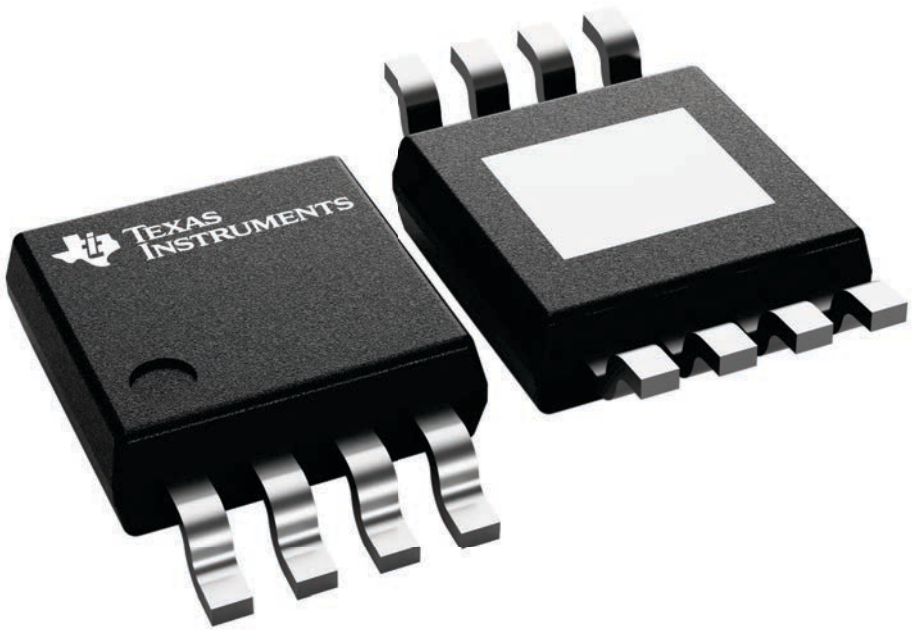
## DGN 8

## PowerPAD™ HVSSOP - 1.1 mm max height

**3 x 3, 0.65 mm pitch**

SMALL OUTLINE PACKAGE

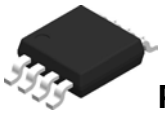
This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.




4225482/B

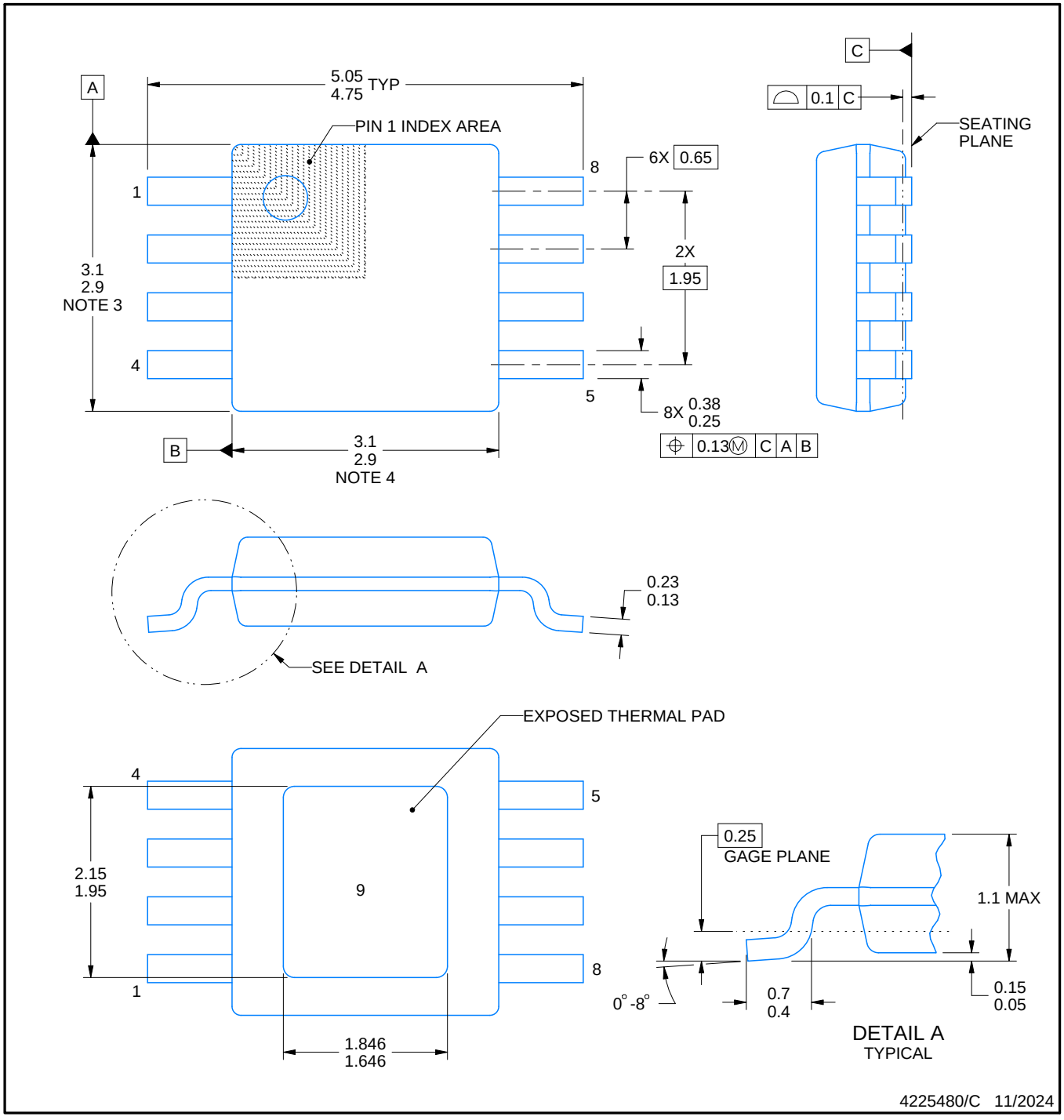
# PACKAGE OUTLINE

## DGN0008G



## PowerPAD™ HVSSOP - 1.1 mm max height

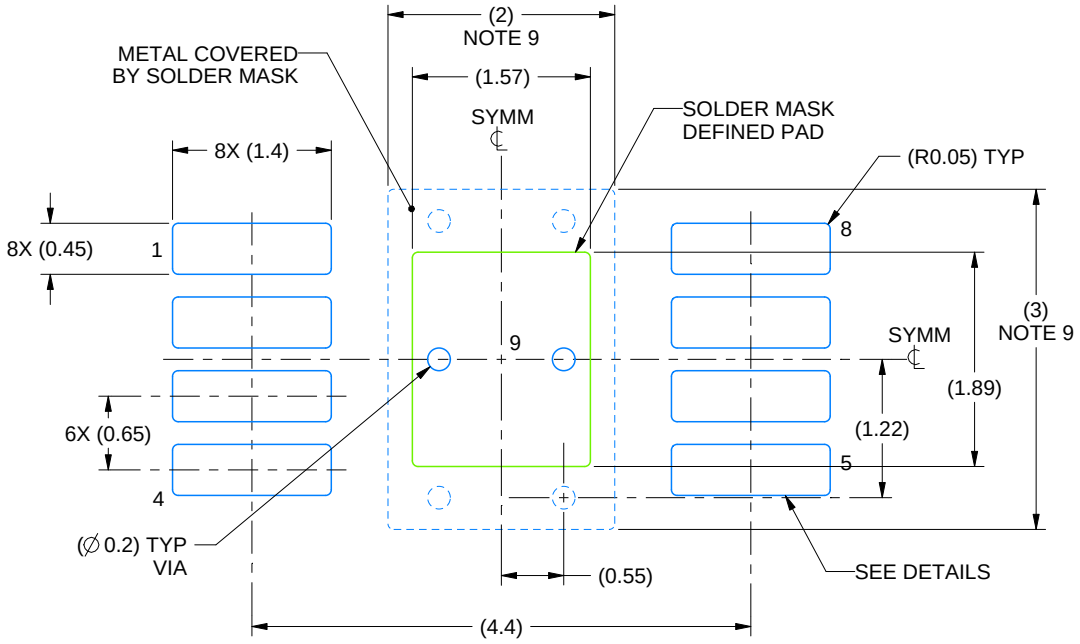
SMALL OUTLINE PACKAGE



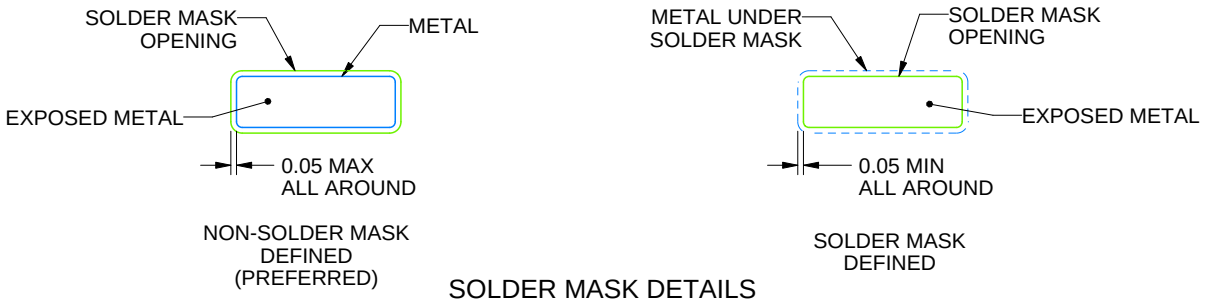

PowerPAD is a trademark of Texas Instruments.

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-187.




LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 15X




SOLDER MASK DETAILS

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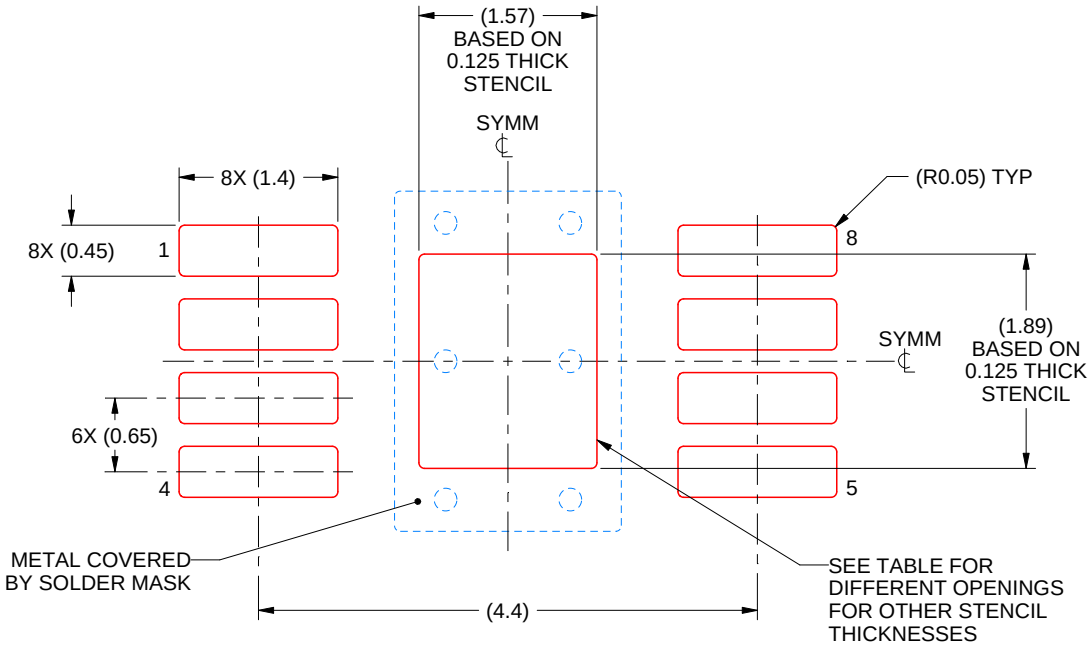
NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.
9. Size of metal pad may vary due to creepage requirement.




SOLDER PASTE EXAMPLE
EXPOSED PAD 9:
100% PRINTED SOLDER COVERAGE BY AREA
SCALE: 15X

| STENCIL THICKNESS | SOLDER STENCIL OPENING |
|---|---|
| 0.1 | 1.76 X 2.11 |
| 0.125 | 1.57 X 1.89 (SHOWN) |
| 0.15 | 1.43 X 1.73 |
| 0.175 | 1.33 X 1.60 |

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NOTES: (continued)

10. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
11. Board assembly site may have different recommendations for stencil design.

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