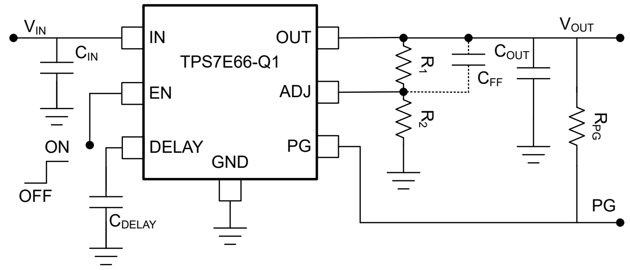
TPS7E66-Q1 Automotive, 40V, 150mA, Ultra-Low I_Q Low-Dropout Regulator with Power-Good

1 Features

- AEC-Q100 qualified for automotive applications:
  - Temperature grade 1: –40°C to +125°C, T_A
  - Junction temperature: –40°C to +150°C, T_J
- Input voltage range: 3.0V to 40V (42V maximum)
- Available output voltage options:
  - Fixed: 1.8V to 12V
  - Adjustable: 1.2V to 38V
- Output current: up to 150mA
- ±1.2% accuracy across line, load and temperature
- Ultra-low I_Q: 2.8μA (typical) at I_{OUT} = 0mA
- Stable with 2.2μF or larger ceramic capacitors
  - ESR range: 0Ω to 1Ω
- Power-good with de-glitch filter and programmable delay
- Dropout voltage: 460mV (typical) at 150mA
- High PSRR:
  - 70dB at 1kHz
  - 45dB at 100kHz
- Over-current, over-power and over-temperature limiting
- Package:
  - 6-pin WSON wettable flank (DRV) [$R_{\theta JA}$: 90.2°C/W]
  - 8-pin HVSSOP (DGN) [$R_{\theta JA}$: 58.5°C/W]

2 Applications

- Automotive head units
- Hybrid, electric & powertrain systems
- Headlights
- Telematics control unit
- Body control module (BCM)



Typical Application

3 Description

The TPS7E66-Q1 low-dropout (LDO) linear voltage regulator is a low quiescent current device designed to connect to the battery in the automotive applications and supports wide input voltage range from 3V to 40V. The wide output range is from 1.2V to 38V for the adjustable configuration and from 1.8V to 12V for the fixed configuration and up-to 150mA of load current. With only an 2.8μA quiescent current at no-load, the device is a good design for powering always-on components such as microcontrollers (MCUs) and controller area network (CAN) transceivers in standby systems.

The TPS7E66-Q1 supports very tight DC accuracy of ±1.2% over line, load and temperature range. The device responds quickly to line, load transients and has fast recovery from cold-crank conditions. The device also features controlled no-load quiescent current in dropout operation.

The TPS7E66-Q1 is equipped with power-good for monitoring of the output voltage. The power-good delay can be adjusted by using external capacitors. The LDO has built-in protection mechanism for over-current, over-temperature and over-power delivery for reliable operation of the LDO. The TPS7E66-Q1 is stable with an output capacitor range from 2.2μF to 100μF.

The TPS7E66-Q1 is available in a 2.0mm × 2.0mm, 6-pin WSON (wettable flank) (DRV-WF), and 3.0mm × 4.9mm, 8-pin HVSSOP (DGN) package for fixed and adjustable outputs.

Package Information

PART NUMBER	PACKAGE(1)	PACKAGE SIZE(2)
TPS7E66-Q1	DRV (WSON, 6)	2.0mm × 2.0mm
	DGN (HVSSOP, 8)	3.0mm × 4.9mm

(1) For more information, see the *Section 10*.
(2) The package size (length × width) is a nominal value and includes pins, where applicable.

Table of Contents

4 Pin Configuration and Functions

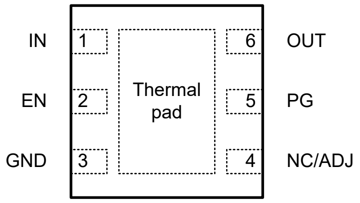


Figure 4-1. DRV Package (Fixed/ADJ), 6-Pin WSON (Top View)

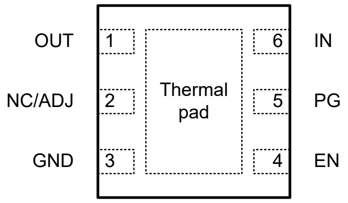


Figure 4-2. DRV Package, A-version (Fixed/ADJ), 6-Pin WSON (Top View)

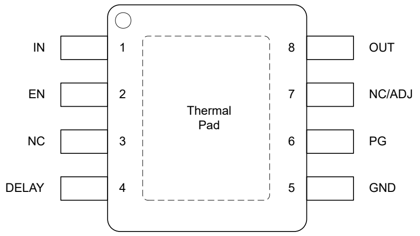


Figure 4-3. DGN Package (Fixed/ADJ), 8-Pin HVSSOP (Top View)

Table 4-1. Pin Functions

PIN		DESCRIPTION
NAME	**TYPE**	
GND	—	Ground pin.
IN	Input	Input supply pin. See the *Recommended Operating Conditions* table and the *Input and Output Capacitor Selection* section for more information.
OUT	Output	Output of the regulator. A capacitor is required from OUT to ground for stability. For best transient response, use the nominal recommended value or larger ceramic capacitor from OUT to ground; see the *Section 5.3* table and the *Input and Output Capacitor Selection* section. Place the output capacitor as close to output of the device as possible.
EN	Input	Enable pin. Driving the enable pin high enables the device. Driving this pin low disables the device. High and low thresholds are listed in the *Electrical Characteristics* table. This pin has a weak internal pullup and can be left floating to enable the device or the pin can be connected to the input pin. Refer to *Enable (EN)* section.
ADJ	Input	When using the adjustable device, this pin sets the output voltage with the help of a feedback divider. In the adjustable configuration, this pin must be connected through a resistor divider to the output for the device to function.
PG	Output	Power-good output, in open-drain topology. A pullup resistor is required on the PG pin. If the power-good functionality is not being used, ground this pin or leave floating. See the *Power-Good (PG)* section for more information.
DELAY	Input	Power-good delay adjustment pin. Connect a capacitor from this pin to GND to set the PG reset delay. Leave this pin floating for a default ($t_{DELAY(PG)}$) delay. See the *Power-Good (PG)* and *Adjustable Power-Good Delay Timer (DELAY)* section for more information. If this functionality is not desired, leave this pin floating because connecting this pin to GND causes a permanent increase in the GND current.
NC	—	Not internally connected. Leave this pin open or connected to any potential. Tie this pin to ground for improved thermal performance.
Thermal pad		Thermal pad. Connect the pad to GND for the best possible thermal performance. See the Layout section for more information.

5 Specifications

5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
Voltage	V_{IN}	–0.3	42.0	V
	V_{OUT} (for fixed device only)	–0.3	2 × $V_{OUT(nom)}$ or V_{IN} + 0.3 or 15.0 (whichever is lower)	V
	V_{OUT} (for adjustable device only)	–0.3	V_{IN} + 0.3 (2)	V
	V_{ADJ} (Feedback voltage)	–0.3	3.6	V
	V_{EN} (Enable voltage)	–0.3	42.0	V
	V_{PG} (Power-good voltage)	–0.3	42.0	V
	V_{DELAY} (PG delay voltage)	–0.3	3.6	V
Current	I_{OUT} (Output current)	Internally limited		mA
	PG (sink current into device)		5	mA
Temperature	T_J, Operating junction	–55	150	°C
	T_{stg}, Storage	–65	150	°C

(1) Operation outside the *Absolute Maximum Ratings* may cause permanent device damage. Absolute Maximum Ratings do not imply functional operation of the device at these or any other conditions beyond those listed under *Recommended Operating Conditions*. If used outside the *Recommended Operating Conditions* but within the *Absolute Maximum Ratings*, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.

(2) The absolute maximum rating is V_{IN} + 0.3V or 42.0V, whichever is smaller.

5.2 ESD Ratings

				VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per AEC Q100-002(1)		±2000	V
		Charged device model (CDM), per AEC Q100-011	Corner pins	±750	
			Other pins	±750	

(1) AEC Q100-002 indicates that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

5.3 Recommended Operating Conditions

over operating junction temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
V_{IN}	Input supply voltage range	3.0		40	V
V_{OUT}	Output voltage range (Fixed only)(1)	1.8		12	V
V_{OUT}	Output voltage range (Adjustable only)(1)	1.2		38	V
V_{EN}	Enable voltage range	0		40	V
V_{PG}	Power-good voltage range	0		40	V
I_{OUT}	Output current	0		150	mA
C_{IN}	Input capacitor (2)		0.47		µF
C_{OUT}	Output capacitor (3)	2.2		100	µF
C_{ADJ}	Parasitic ADJ to GND capacitor(4)			15	pF
C_{FF}	Feed-forward capacitor (5)		10		nF
T_J	Operating junction temperature	–40		150	°C

(1) This output voltage range does not include device accuracy or accuracy of the feedback resistors.

(2) An input capacitor is not required for LDO stability. However, an input capacitance with an effective value of 0.1µF minimum is recommended to counteract the effect of source resistance and inductance, which can in some cases cause symptoms of system level instability such as ringing or oscillation, especially in the presence of load transients.

(3) All capacitor values listed are the nominal value and the effective capacitance is assumed to derate up-to 50% of the nominal capacitor value.

(4) The upper limit for the capacitor on the ADJ pin with respect to GND impacts the stable operation of the voltage regulator in adjustable configuration. For C_{ADJ} capacitor higher than limits mentioned in *Recommended Operating Conditions* table, use C_{FF} capacitor.

(5) The C_{FF} capacitor improves transient, noise, and PSRR performance, but is not required for regulator stability. Using a higher capacitance C_{FF} is permissible but start-up time increases.

5.4 Thermal Information

THERMAL METRIC [1]		TPS7E66-Q1		UNIT
		DRV (WSON) [2]	DGN (HVSSOP) [2]	
		6 PINS	8 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	90.2	58.5	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	113.5	96.8	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	55.7	32.4	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	13.0	11.7	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	55.3	32.4	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	30.6	12.6	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application note.

(2) Thermal performance results are based on the JEDEC standard of 2s2p PCB configuration. These thermal metric parameters are further improved by 35-55% based on thermally optimized PCB layout designs. See the analysis of the Impact of board layout on LDO thermal performance application note.

5.5 Electrical Characteristics

Over operating junction temperature range (T_J = –40°C to +150°C), V_{IN} = 3.0V or $V_{IN} = V_{OUT(nom)}$ + 0.5V (whichever is greater), I_{OUT} = 1mA, V_{EN} = 2.0V, C_{IN} = 1.0µF, C_{OUT} = 2.2µF, and PG pin pulled up-to V_{IN} with 100kΩ, unless otherwise noted. Typical values are at T_J = 25°C.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{ADJ}	ADJ (Feedback) voltage			1.2		V
V_{UVLO+}	Rising input supply UVLO	V_{IN} rising		2.8	2.91	V
V_{UVLO-}	Falling input supply UVLO	V_{IN} falling	2.6	2.7		V
$V_{UVLO(HYST)}$	V_{UVLO} hysteresis			100		mV
V_{OUT}	Output voltage	$V_{IN} = V_{OUT}$ + 0.5V, I_{OUT} = 1mA, T_J = 25℃	–0.3		0.3	%
V_{OUT}	Output voltage	V_{OUT} + 1.0V ≤ V_{IN} ≤ 40V, I_{OUT} = 35mA, T_J = 25℃	–0.7		0.7	%
		V_{OUT} + 1.0V ≤ V_{IN} ≤ 40V, I_{OUT} = 35mA	–1.2		1.2	
		1mA ≤ I_{OUT} ≤ 150mA, 1.0V ≤ $V_{IN} – V_{OUT}$ ≤ 25V	–1.2		1.2	
$\Delta V_{OUT}(\Delta V_{IN})$	Line regulation	I_{OUT} = 1mA, V_{OUT} + 0.5V ≤ V_{IN} ≤ 40V			10	mV
$\Delta V_{OUT}(\Delta I_{OUT})$	Load regulation	1mA ≤ I_{OUT} ≤ 150mA, $V_{IN} = V_{OUT}$ + 1.0V, 1.2V ≤ V_{OUT} < 5.0V			9	mV
		1mA ≤ I_{OUT} ≤ 150mA, $V_{IN} = V_{OUT}$ + 1.0V, 5.0V ≤ V_{OUT} < 12.0V			18	mV
$\Delta \%V_{OUT}/\Delta I_{OUT}$	Load regulation	1mA ≤ I_{OUT} ≤ 150mA, $V_{IN} = V_{OUT}$ + 1.0V, 12.0V ≤ V_{OUT}			1.0	%/A
V_{DO}	Dropout voltage	I_{OUT} = 150mA		0.46	0.85	V
		I_{OUT} = 150mA, for adjustable		0.49	0.9	
V_{DO}	Dropout voltage	I_{OUT} = 100mA		0.3	0.55	V
		I_{OUT} = 100mA, for adjustable		0.32	0.56	
I_{LIM}	Output current limit	V_{OUT} forced at 0.9 × $V_{OUT(nom)}$, $V_{IN} = V_{OUT(nom)}$ + 1.0V	180	250	325	mA
I_{SC}	Short-circuit current limit	R_{LOAD} = 20mΩ	10	30	55	mA
I_{PLIMIT}	Supported current at max headroom	V_{IN} = 40V, V_{OUT} = 1.2V			15	mA
$V_{HEADROOM}$	Max headroom at full load	V_{OUT} = 1.2V			25	V

5.5 Electrical Characteristics (continued)

Over operating junction temperature range (T_J = –40°C to +150°C), V_{IN} = 3.0V or V_{IN} = $V_{OUT(nom)}$ + 0.5V (whichever is greater), I_{OUT} = 1mA, V_{EN} = 2.0V, C_{IN} = 1.0μF, C_{OUT} = 2.2μF, and PG pin pulled up-to V_{IN} with 100kΩ, unless otherwise noted. Typical values are at T_J = 25°C.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_{ADJ}	ADJ (Feedback) current	V_{IN} = 40V			25	nA
I_Q	Quiescent current	3.0V ≤ V_{IN} ≤ $V_{OUT(nom)}$ – 0.2V , I_{OUT} = 0mA		12.5	25	μA
		I_{OUT} = 0mA		2.8	6.0	
		V_{OUT} + 0.5V ≤ V_{IN} ≤ 40V , I_{OUT} = 0mA			7.6	
I_{GND}	Ground current	I_{OUT} = 1mA		16.5	25	μA
I_{GND}	Ground current	V_{IN} = V_{OUT} + 1.0V, I_{OUT} = 150mA			370	μA
$I_{SHUTDOWN}$	Shutdown current	V_{EN} = 0V, T_J = 25℃		0.45		μA
		V_{OUT} + 0.5V ≤ V_{IN} ≤ 40V , V_{EN} = 0V			1.5	
$T_{start\text{-}up}$	Start-up time	V_{IN}, V_{EN} tied together, V_{IN} ramped to $V_{OUT(nom)}$ + 0.5V, I_{OUT} = 0mA		500		μs
I_{EN}	EN pin current	0V ≤ V_{EN} ≤ 40V, V_{IN} and V_{EN} tied together			0.3	μA
		0V ≤ V_{IN} ≤ 40V, V_{EN} = 0V	–0.5			
$V_{IL(EN)}$	EN pin low-level input voltage (disable device)				0.46	V
$V_{IH(EN)}$	EN pin high-level input voltage (enable device)		1.1			
$V_{HYST(EN)}$	EN pin hysteresis (enable device)			0.13		V
PSRR	Power-supply ripple rejection	V_{IN} – V_{OUT} = 2.0V, I_{OUT} = 150mA, f = 100kHz		45		dB
V_n	Output noise voltage	Bandwidth = 10Hz to 100kHz, V_{IN} – V_{OUT} = 2.0V, I_{OUT} = 150mA		650		μVRMS
$V_{IT\text{-}(PG)}$	Falling PG pin threshold	For falling V_{OUT}	86	89	92	%
$V_{IT+(PG)}$	Rising PG pin threshold	For rising V_{OUT}	90	93	96	%
$V_{OL(PG)}$	PG pin low-level output voltage	V_{OUT} < $V_{IT\text{-}(PG)}$, V_{IN} = 3.0V, I_{PG} = –1mA (current into device)			0.4	V
$I_{lkg(PG)}$	PG pin leakage current	V_{OUT} > $V_{IT+(PG)}$, V_{PG} = 40V		0.04	0.5	μA
Delay(PG)	PG pin delay time			150		μs
Deglitch(PG)	PG pin deglitch time			135		μs
$I_{(PGDL\_CHG)}$	PG delay capacitor charging current	V_{PGDL} = 63% of V_{PGDL} (typ)		2.86		μA
$V_{(PGDL\_TH)}$	PG delay threshold to release PG high			2.26		V
T_{sd+}	Thermal shutdown temperature increasing	Shutdown, temperature increasing	163			°C
T_{sd-}	Thermal shutdown temperature decreasing	Reset, temperature decreasing	150			°C
$R_{Discharge}$	Output discharge resistance	V_{IN} = 3.0V, V_{EN} = 0V, T_J = 25℃, I_{OUT} = 1mA		780		Ω
I_{SINK}	Sink current on output	V_{OUT} = $V_{OUT(nom)}$ × 1.05, T_J = 25℃		3.3		mA

5.6 Typical Characteristics

at operating junction temperature T_J = 25°C, V_{IN} = 3.0V or V_{IN} = V_{OUT}(nom) + 1.0V (whichever is greater), C_{IN} = 1µF, C_{OUT} = 2.2µF, and I_{OUT} = 1mA (unless otherwise noted)

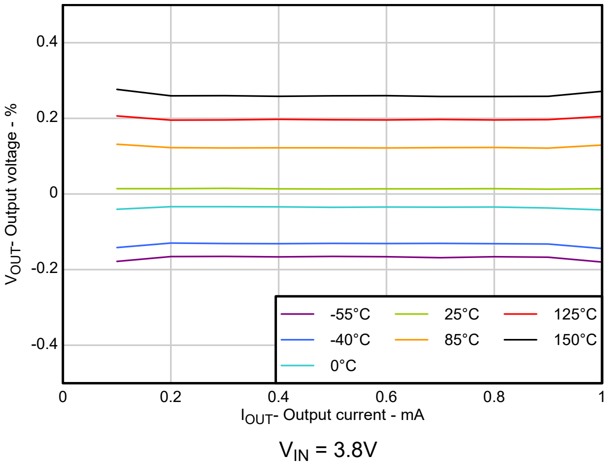


Figure 5-1. V_{OUT} Accuracy vs I_{OUT}

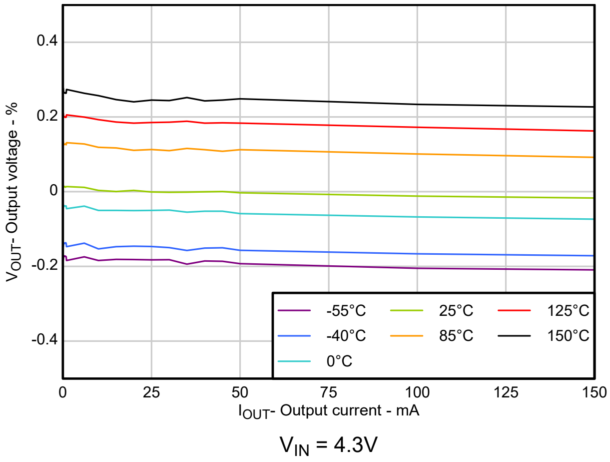


Figure 5-2. V_{OUT} Accuracy vs I_{OUT}

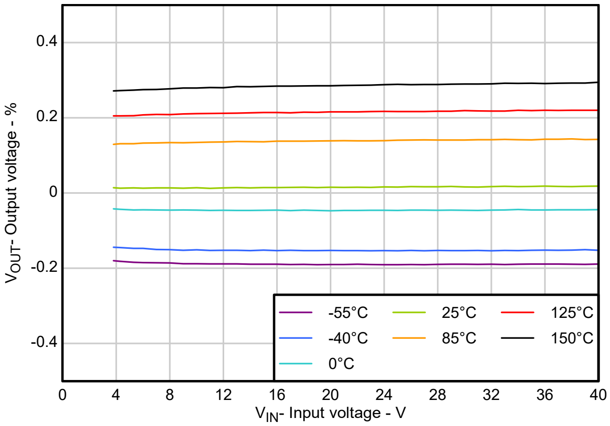


Figure 5-3. V_{OUT} Accuracy vs V_{IN}

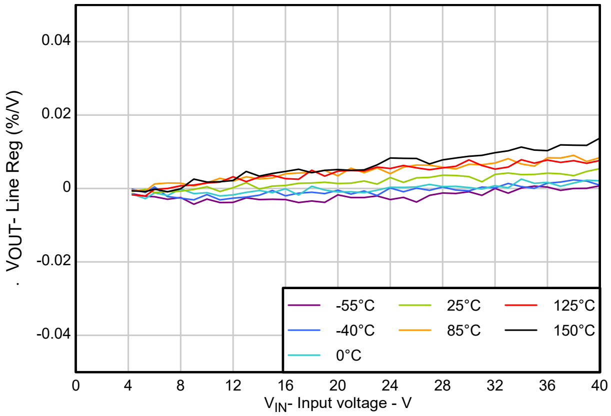


Figure 5-4. Line Regulation

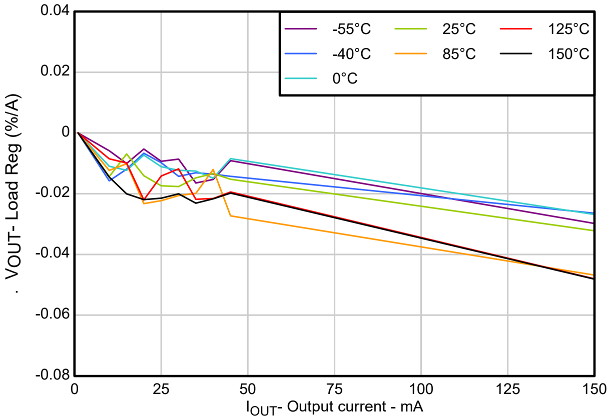


Figure 5-5. Load Regulation

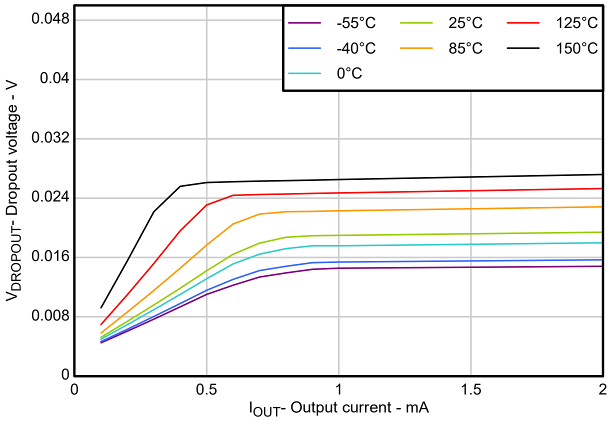


Figure 5-6. V_{DO} vs I_{OUT}(mA)

5.6 Typical Characteristics (continued)

at operating junction temperature T_J = 25°C, V_{IN} = 3.0V or V_{IN} = V_{OUT}(nom) + 1.0V (whichever is greater), C_{IN} = 1µF, C_{OUT} = 2.2µF, and I_{OUT} = 1mA (unless otherwise noted)

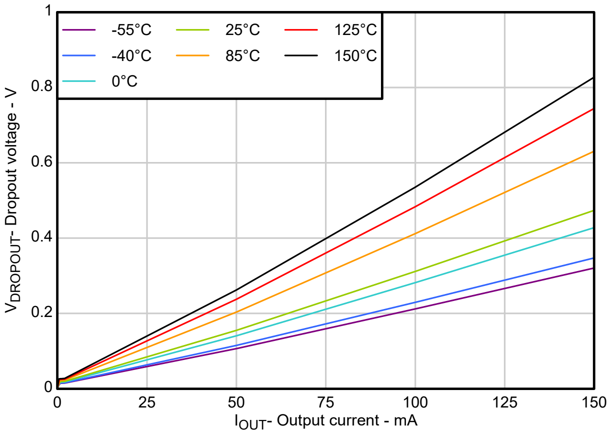


Figure 5-7. V_{DO} vs I_{OUT}(mA)

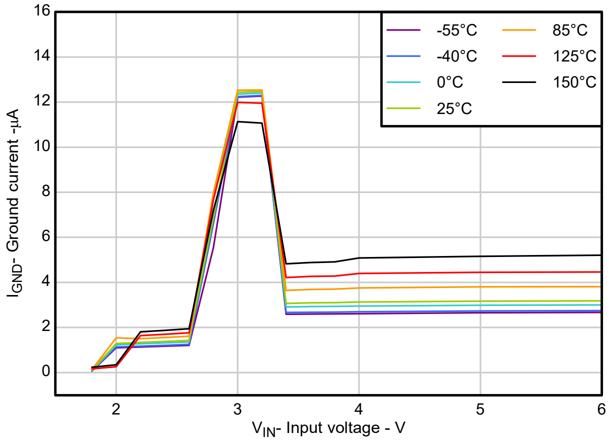


Figure 5-8. I_{GND} vs V_{IN}

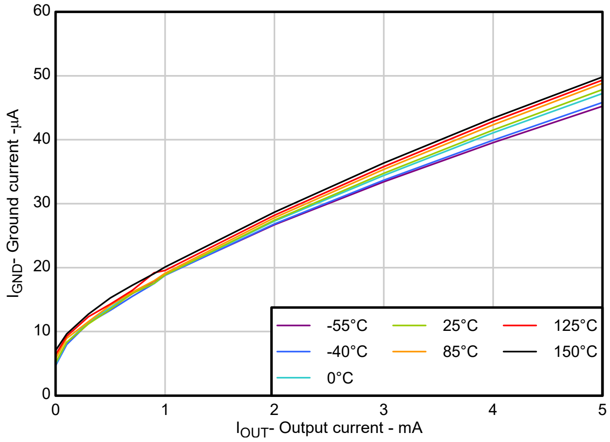


Figure 5-9. I_{GND} vs I_{OUT}

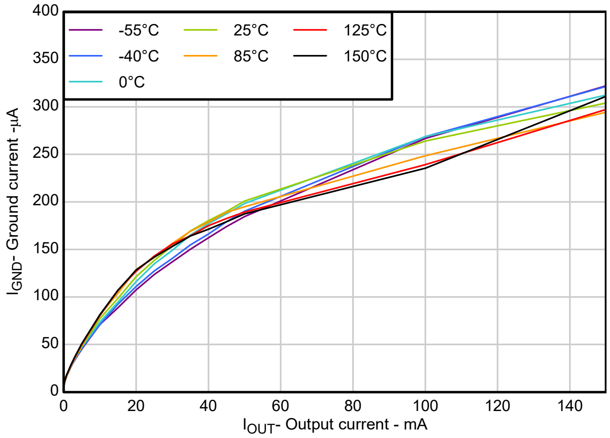


Figure 5-10. I_{GND} vs I_{OUT}

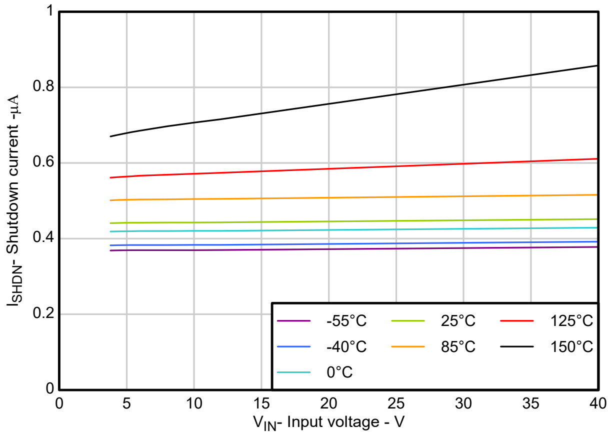
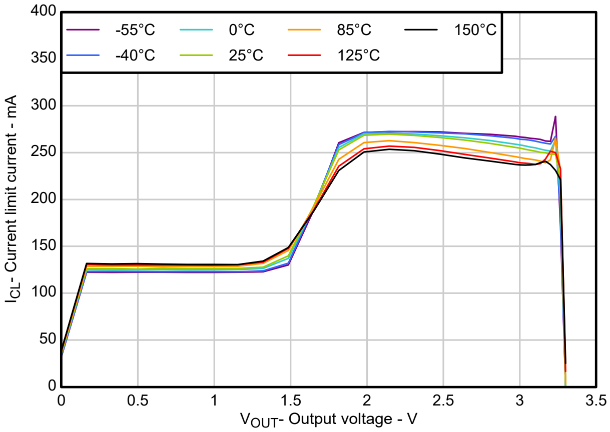


Figure 5-11. I_{SHDN} vs V_{IN}

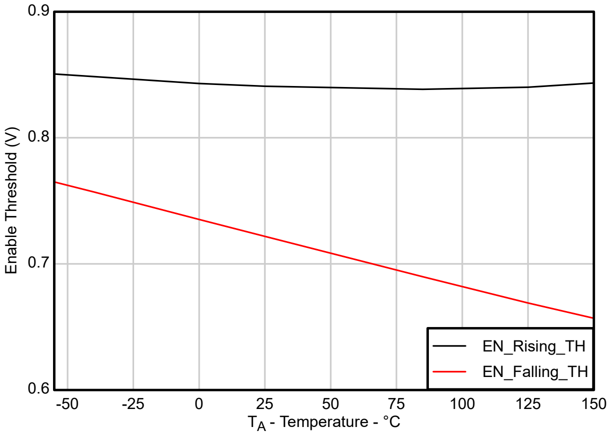


V_{IN} = 4.3V

Figure 5-12. Foldback Current Limit I_{CL} vs Temperature

5.6 Typical Characteristics (continued)

at operating junction temperature T_J = 25°C, V_{IN} = 3.0V or V_{IN} = V_{OUT}(nom) + 1.0V (whichever is greater), C_{IN} = 1µF, C_{OUT} = 2.2µF, and I_{OUT} = 1mA (unless otherwise noted)



V_{IN} = 5.3V

Figure 5-13. EN Threshold $V_{IH(EN)}$/$V_{IL(EN)}$ vs Temperature

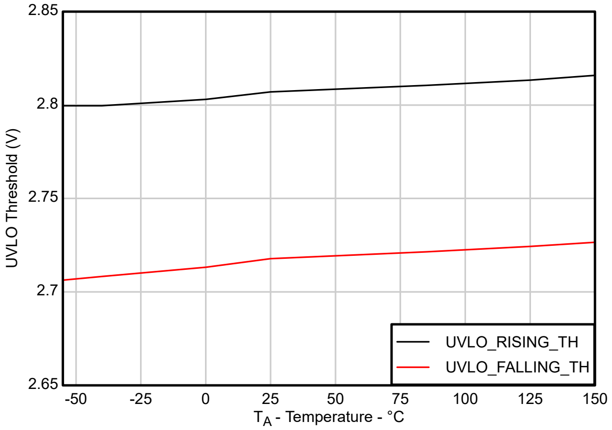
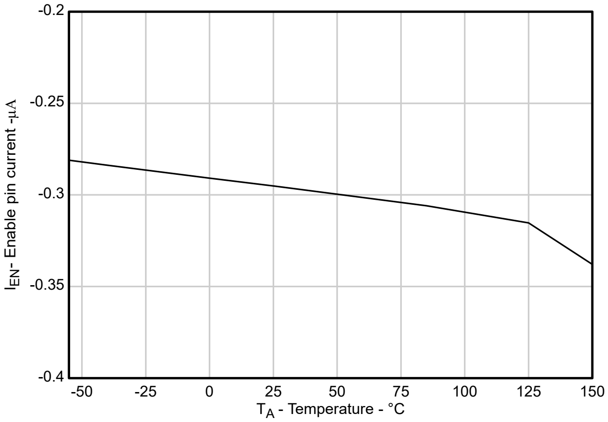
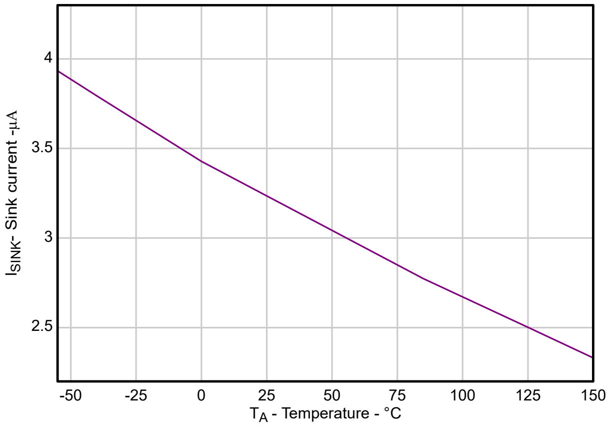


Figure 5-14. UVLO Threshold (V_{UVLO+}/V_{UVLO-}) vs Temperature



V_{IN} = 4.3V

Figure 5-15. EN Leakage Current I_{EN} vs Temperature

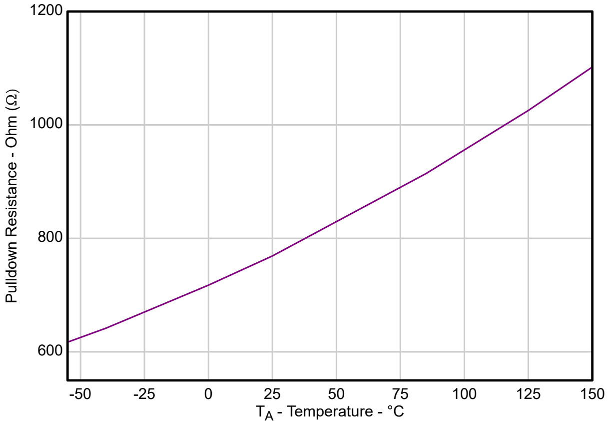


V_{IN} = 4.3V, V_{OUT} = 1.05 × $V_{OUT(nom)}$

Figure 5-16. Sink Current on Output (I_{SINK}) vs Temperature

5.6 Typical Characteristics (continued)

at operating junction temperature T_J = 25°C, V_{IN} = 3.0V or V_{IN} = V_{OUT}(nom) + 1.0V (whichever is greater), C_{IN} = 1µF, C_{OUT} = 2.2µF, and I_{OUT} = 1mA (unless otherwise noted)



V_{IN} = 3.0V, I_{OUT} = 1mA

Figure 5-17. Pull-down Resistance on Output ($R_{Discharge}$) vs Temperature

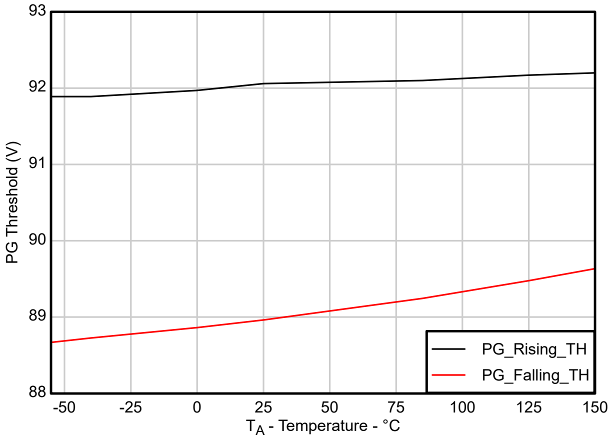
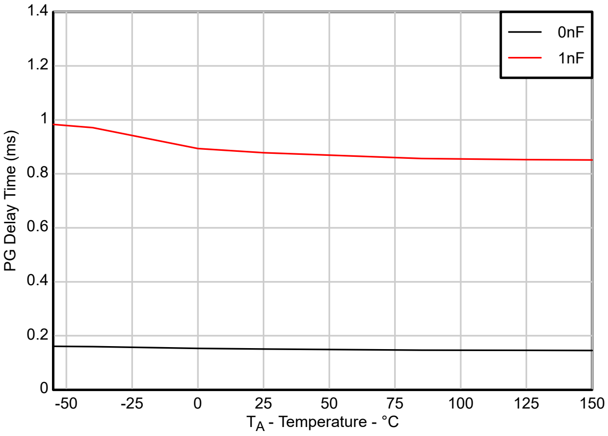


Figure 5-18. PG Threshold ($V_{IT+(PG)}$/$V_{IT-(PG)}$) vs Temperature



C_{DELAY} = 0nA, 1nF

Figure 5-19. PG Delay time vs Temperature

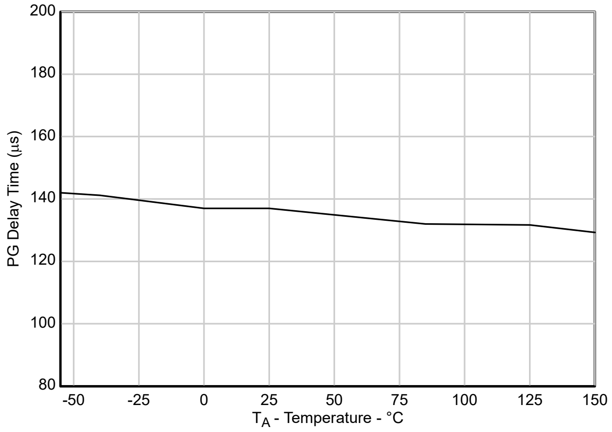
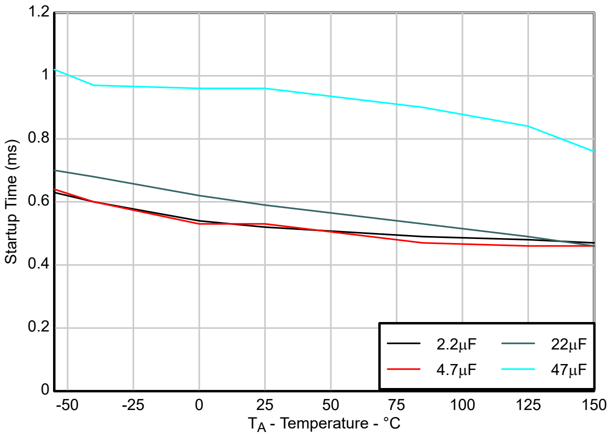


Figure 5-20. PG Deglitch time vs Temperature

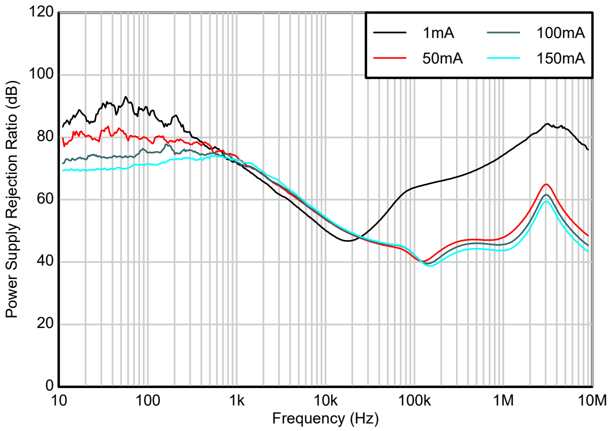
5.6 Typical Characteristics (continued)

at operating junction temperature T_J = 25°C, V_{IN} = 3.0V or V_{IN} = V_{OUT}(nom) + 1.0V (whichever is greater), C_{IN} = 1µF, C_{OUT} = 2.2µF, and I_{OUT} = 1mA (unless otherwise noted)



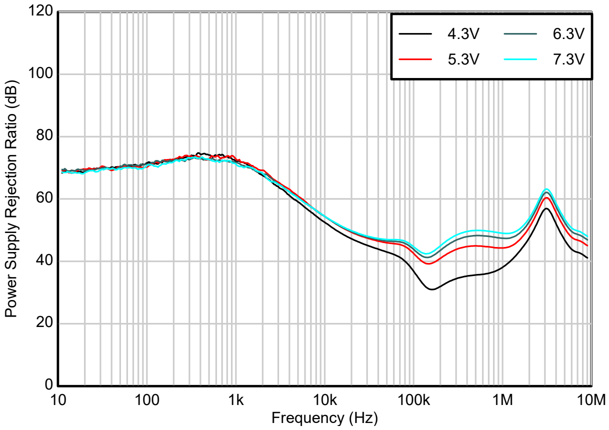
V_{IN} = 4.3V, V_{OUT} = 3.3V

Figure 5-21. Start-up Time vs C_{OUT}



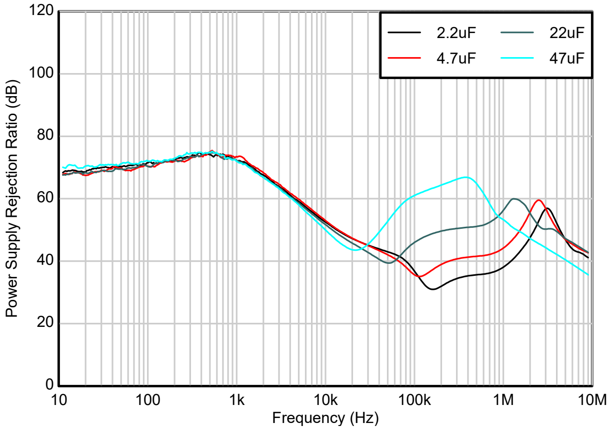
V_{IN} = 5.3V, V_{OUT} = 3.3V, C_{OUT} = 2.2µF

Figure 5-22. PSRR vs I_{OUT}



V_{OUT} = 3.3V, I_{OUT} = 150mA, C_{OUT} = 2.2µF

Figure 5-23. PSRR vs V_{IN}

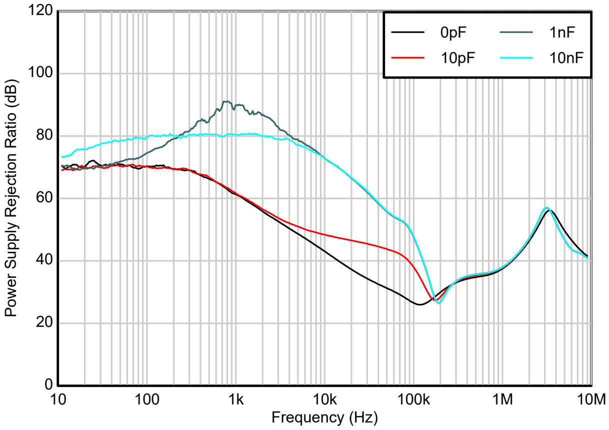


V_{IN} = 4.3V, V_{OUT} = 3.3V, I_{OUT} = 150mA

Figure 5-24. PSRR vs C_{OUT}

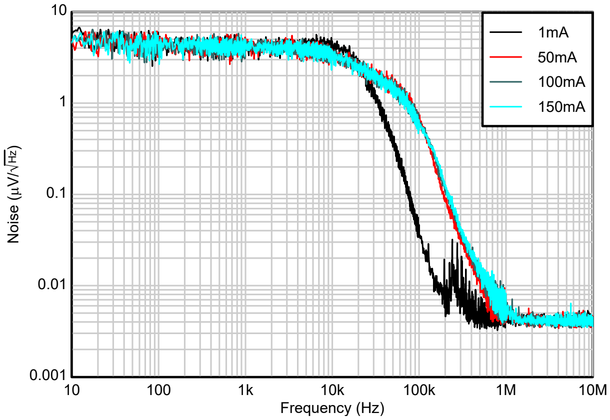
5.6 Typical Characteristics (continued)

at operating junction temperature T_J = 25°C, V_{IN} = 3.0V or V_{IN} = V_{OUT}(nom) + 1.0V (whichever is greater), C_{IN} = 1µF, C_{OUT} = 2.2µF, and I_{OUT} = 1mA (unless otherwise noted)



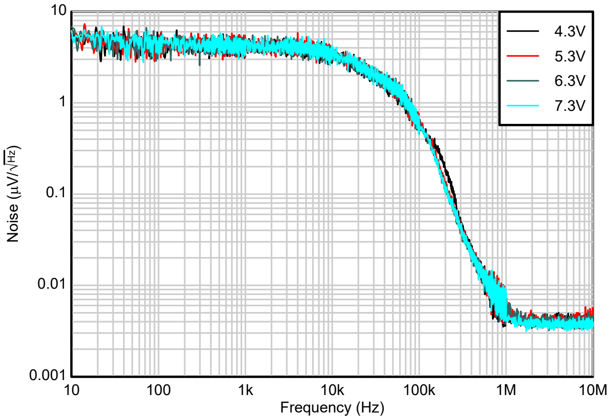
V_{IN} = 4.3V, V_{OUT} = 3.3V, COUT = 2.2µF, I_{OUT} = 150mA

Figure 5-25. PSRR vs C_{FF}



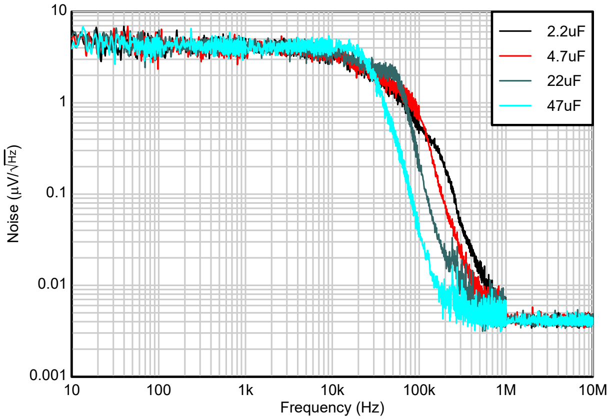
V_{IN} = 5.3V, V_{OUT} = 3.3V, C_{OUT} = 2.2µF

Figure 5-26. Noise vs I_{OUT}



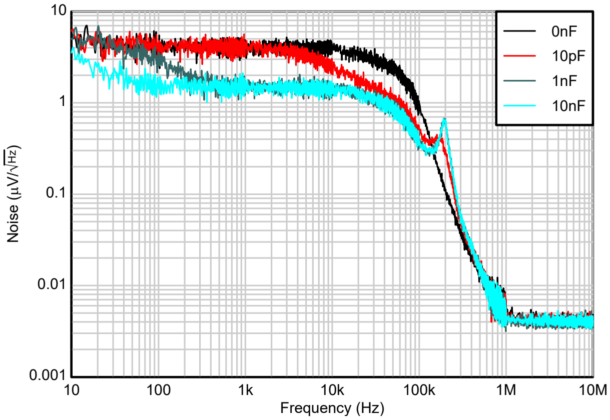
V_{OUT} = 3.3V, I_{OUT} = 150mA, C_{OUT} = 2.2µF

Figure 5-27. Noise vs V_{IN}



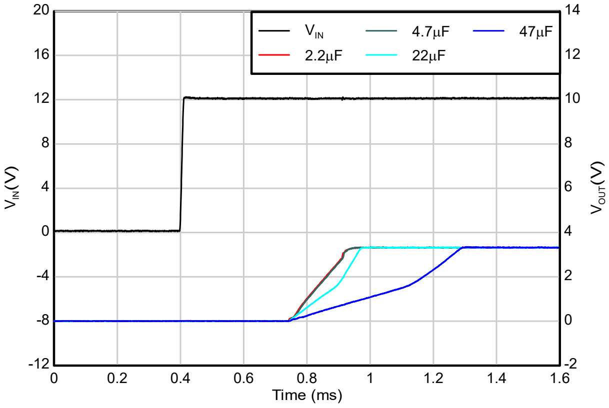
V_{IN} = 4.3V, V_{OUT} = 3.3V, I_{OUT} = 150mA

Figure 5-28. Noise vs C_{OUT}



V_{IN} = 4.3V, V_{OUT} = 3.3V, COUT = 2.2µF, I_{OUT} = 150mA

Figure 5-29. Noise vs C_{FF}

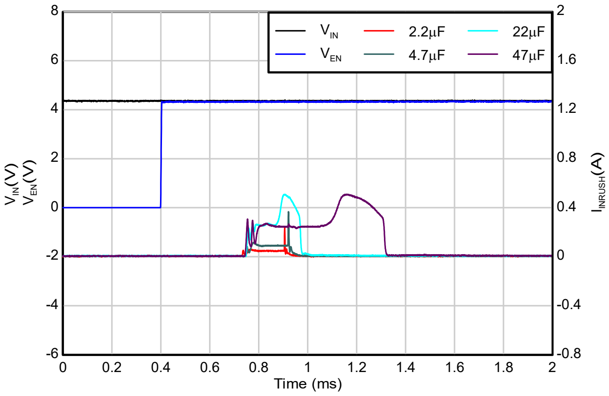


V_{IN} = 12V, V_{OUT} = 3.3V, I_{OUT} = 1mA

Figure 5-30. Start-up vs C_{OUT}

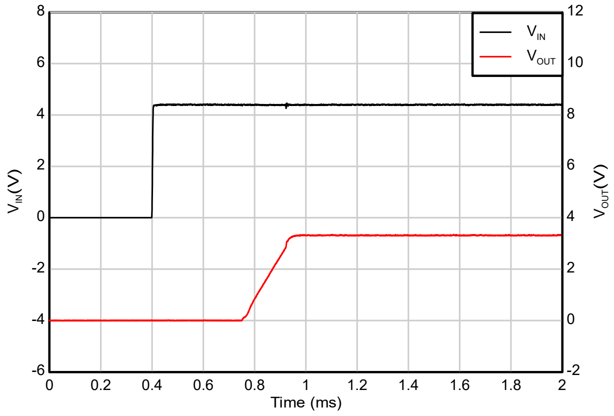
5.6 Typical Characteristics (continued)

at operating junction temperature T_J = 25°C, V_{IN} = 3.0V or V_{IN} = V_{OUT}(nom) + 1.0V (whichever is greater), C_{IN} = 1µF, C_{OUT} = 2.2µF, and I_{OUT} = 1mA (unless otherwise noted)



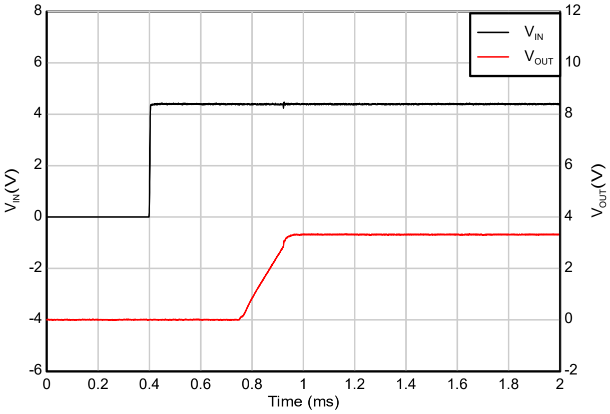
V_{IN} = 4.3V, V_{OUT} = 3.3V, I_{OUT} = 0mA

Figure 5-31. Inrush Current vs C_{OUT}



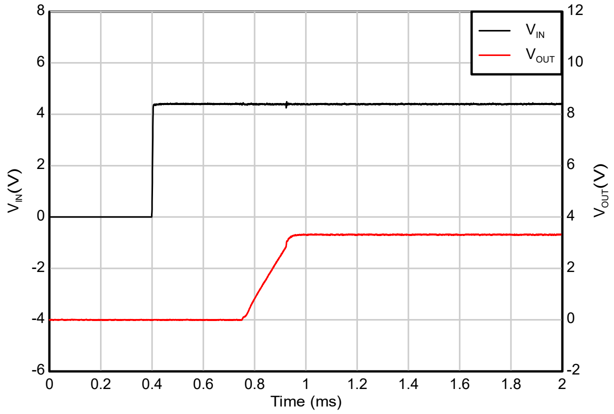
V_{IN} = 4.3V, V_{OUT} = 3.3V, I_{OUT} = 1mA

Figure 5-32. Start-up with EN & V_{IN} tied together



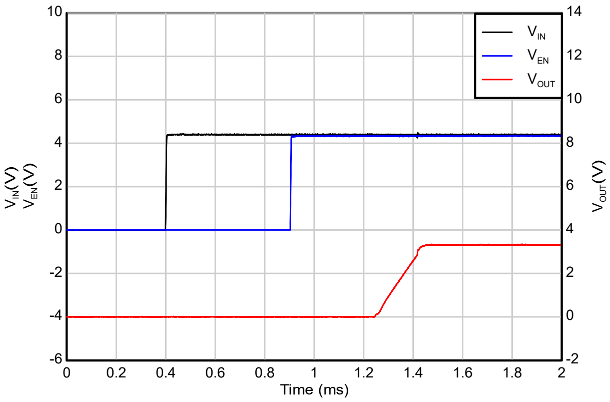
V_{IN} = 4.3V, V_{OUT} = 3.3V, I_{OUT} = 10mA

Figure 5-33. Start-up with EN & V_{IN} tied together



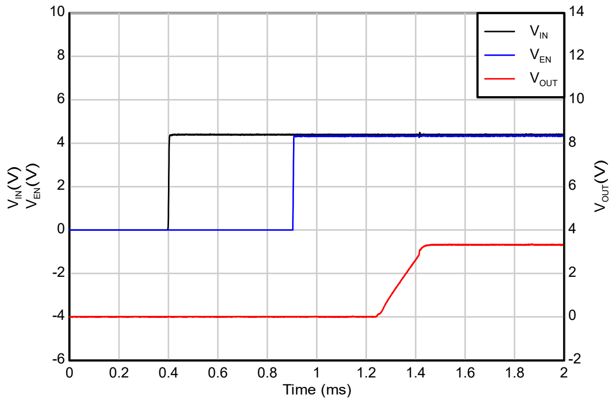
V_{IN} = 4.3V, V_{OUT} = 3.3V, I_{OUT} = 50mA

Figure 5-34. Start-up with EN & V_{IN} tied together



V_{IN} = 4.3V, V_{OUT} = 3.3V, I_{OUT} = 1mA

Figure 5-35. Start-up with sequencing (EN after V_{IN})

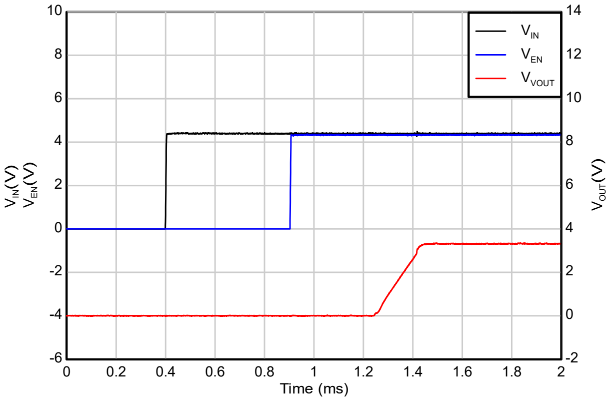


V_{IN} = 4.3V, V_{OUT} = 3.3V, I_{OUT} = 10mA

Figure 5-36. Start-up with sequencing (EN after V_{IN})

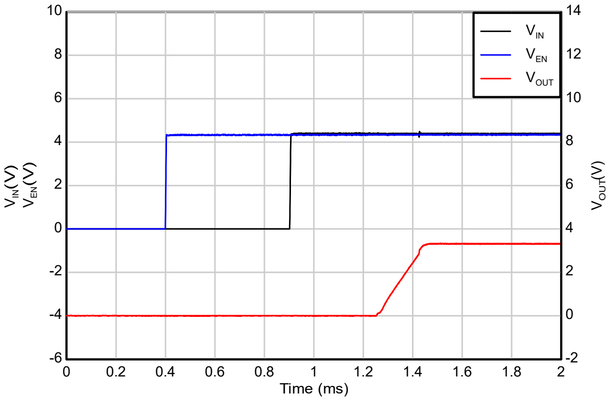
5.6 Typical Characteristics (continued)

at operating junction temperature T_J = 25°C, V_{IN} = 3.0V or V_{IN} = V_{OUT}(nom) + 1.0V (whichever is greater), C_{IN} = 1µF, C_{OUT} = 2.2µF, and I_{OUT} = 1mA (unless otherwise noted)



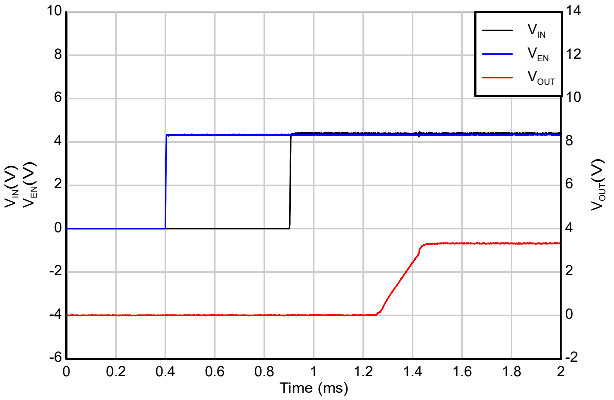
V_{IN} = 4.3V, V_{OUT} = 3.3V, I_{OUT} = 50mA

Figure 5-37. Start-up with sequencing (EN after V_{IN})



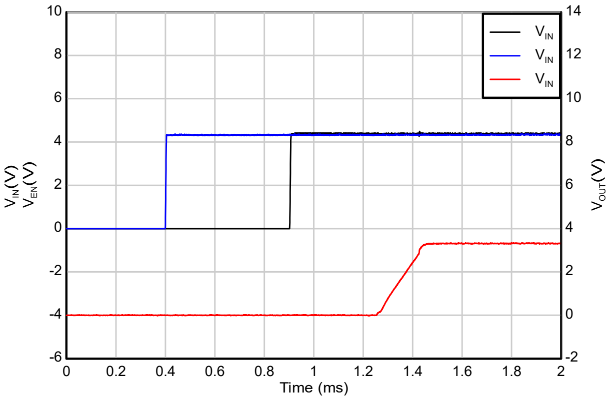
V_{IN} = 4.3V, V_{OUT} = 3.3V, I_{OUT} = 1mA

Figure 5-38. Start-up with sequencing (V_{IN} after EN)



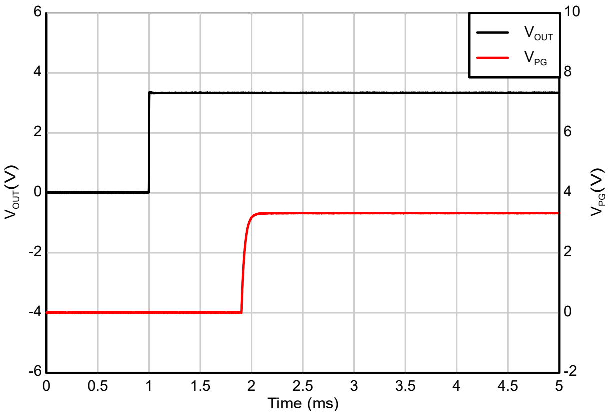
V_{IN} = 4.3V, V_{OUT} = 3.3V, I_{OUT} = 10mA

Figure 5-39. Start-up with sequencing (V_{IN} after EN)



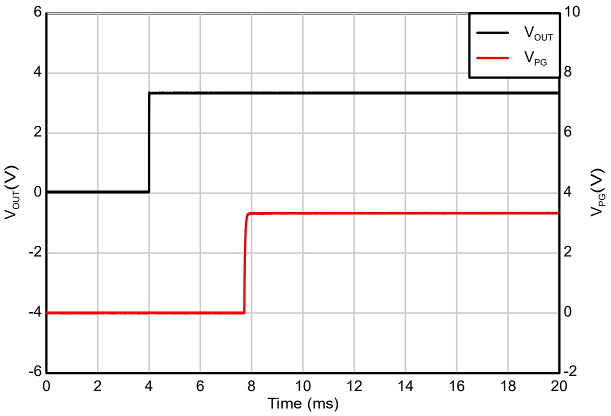
V_{IN} = 4.3V, V_{OUT} = 3.3V, I_{OUT} = 50mA

Figure 5-40. Start-up with sequencing (V_{IN} after EN)



V_{IN} = 4.3V, V_{OUT} = 3.3V, C_{DELAY} = 1nF

Figure 5-41. PG Delay with C_{DELAY} = 1nF

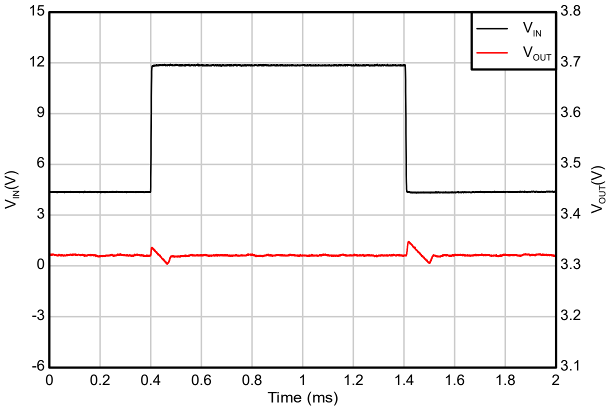


V_{IN} = 4.3V, V_{OUT} = 3.3V, C_{DELAY} = 4.7nF

Figure 5-42. PG Delay with C_{DELAY} = 4.7nF

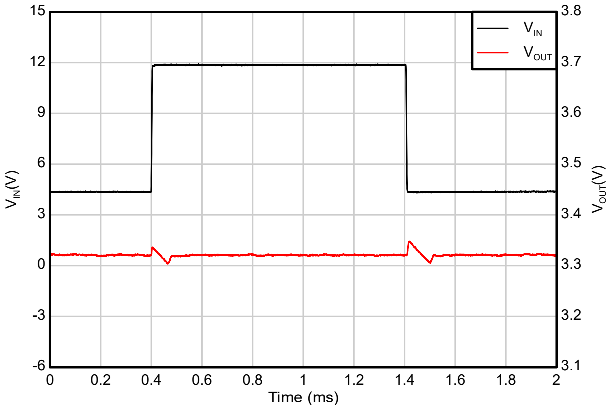
5.6 Typical Characteristics (continued)

at operating junction temperature T_J = 25°C, V_{IN} = 3.0V or V_{IN} = V_{OUT}(nom) + 1.0V (whichever is greater), C_{IN} = 1µF, C_{OUT} = 2.2µF, and I_{OUT} = 1mA (unless otherwise noted)



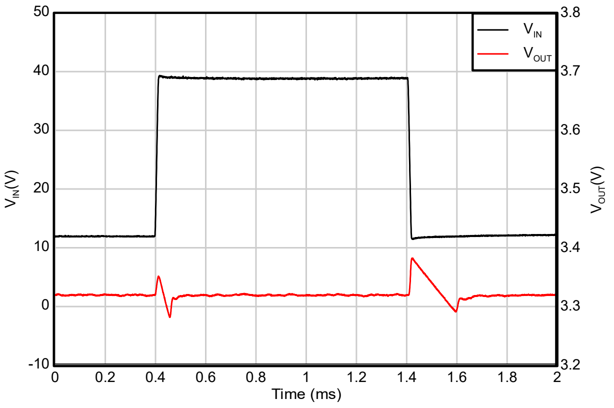
V_{IN} = 4.3V to 12V, V_{OUT} = 3.3V, I_{OUT} = 1mA, dV_{IN}/dt = 2V/µs

Figure 5-43. Line Transient (4.3V to 12V)



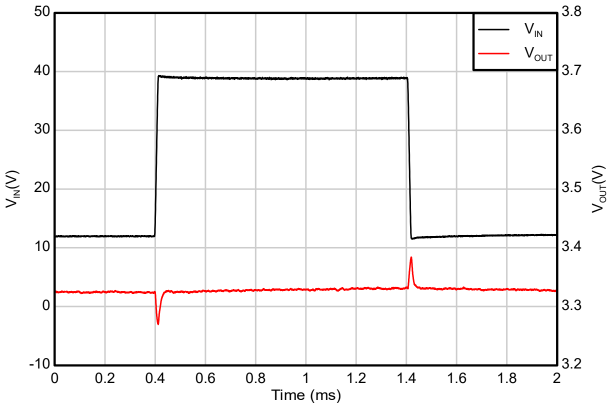
V_{IN} = 4.3V to 12V, V_{OUT} = 3.3V, I_{OUT} = 150mA, dV_{IN}/dt = 2V/µs

Figure 5-44. Line Transient (4.3V to 12V)



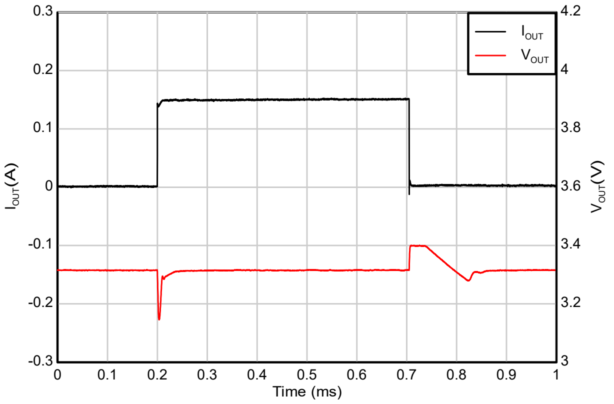
V_{IN} = 12V to 40V, V_{OUT} = 3.3V, I_{OUT} = 1mA, dV_{IN}/dt = 2V/µs

Figure 5-45. Line Transient (12V to 40V)



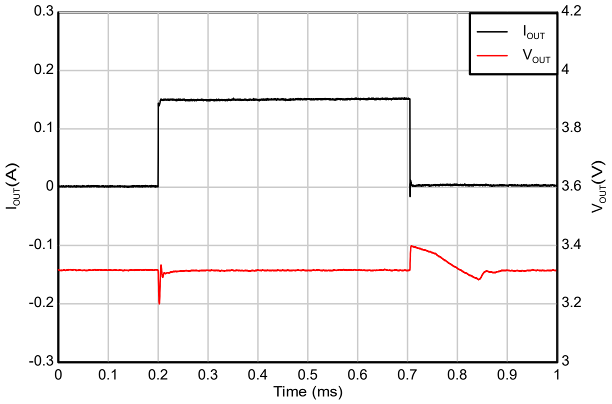
V_{IN} = 12V to 40V, V_{OUT} = 3.3V, I_{OUT} = 150mA, dV_{IN}/dt = 2V/µs

Figure 5-46. Line Transient (12V to 40V)



V_{IN} = 4.3V, V_{OUT} = 3.3V, I_{OUT} = 0mA to 150mA, dI_{OUT}/dt = 2A/µs

Figure 5-47. Load Transient (0mA to 150mA)

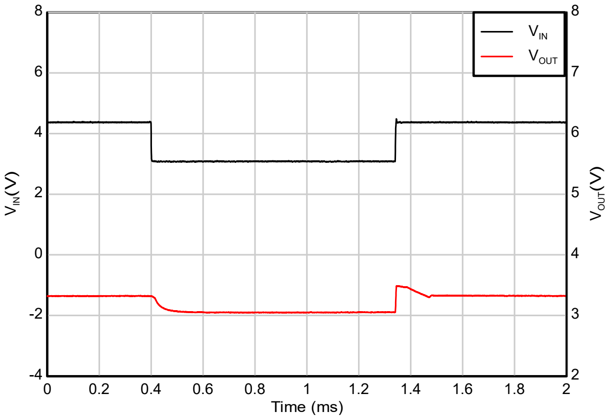


V_{IN} = 4.3V, V_{OUT} = 3.3V, I_{OUT} = 1mA to 150mA, dI_{OUT}/dt = 2A/µs

Figure 5-48. Load Transient (1mA to 150mA)

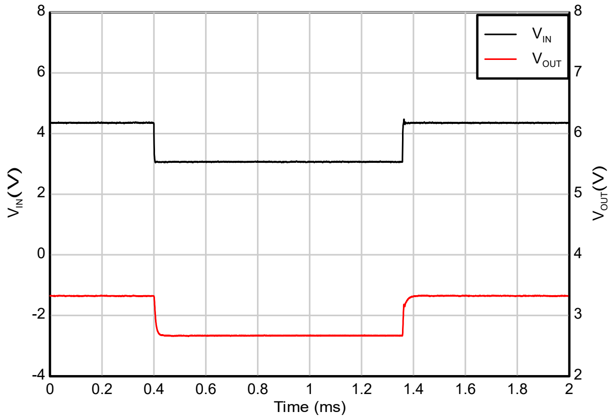
5.6 Typical Characteristics (continued)

at operating junction temperature T_J = 25°C, V_{IN} = 3.0V or V_{IN} = V_{OUT}(nom) + 1.0V (whichever is greater), C_{IN} = 1µF, C_{OUT} = 2.2µF, and I_{OUT} = 1mA (unless otherwise noted)



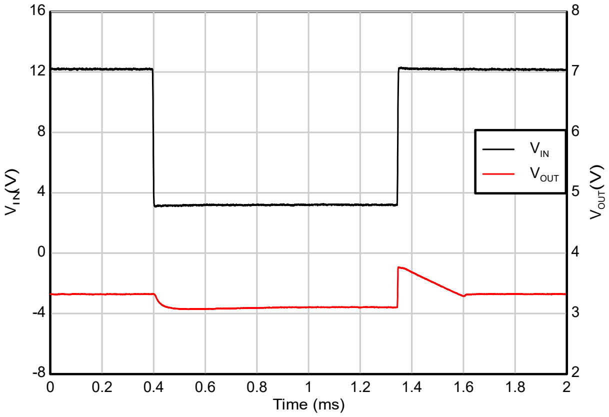
V_{IN} = 4.3V to 3V, V_{OUT} = 3.3V, I_{OUT} = 1mA, dV_{IN}/dt = 2V/µs

Figure 5-49. Dropout Recovery (4.3V to 3V)



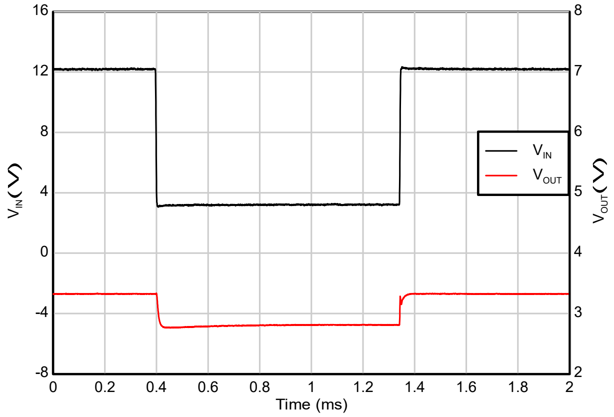
V_{IN} = 4.3V to 3V, V_{OUT} = 3.3V, I_{OUT} = 150mA, dV_{IN}/dt = 2V/µs

Figure 5-50. Dropout Recovery (4.3V to 3V)



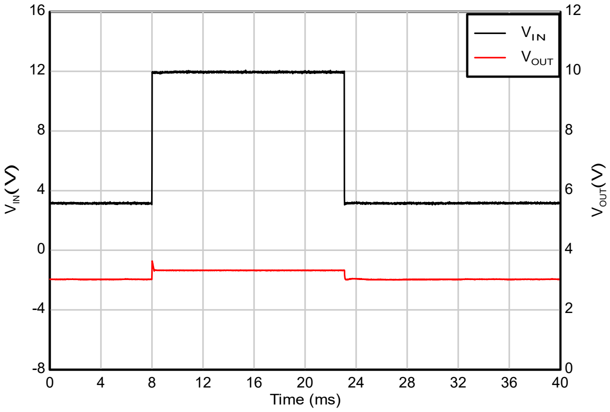
V_{IN} = 12V to 3V, V_{OUT} = 3.3V, I_{OUT} = 1mA, dV_{IN}/dt = 2V/µs

Figure 5-51. Dropout Recovery (12V to 3V)



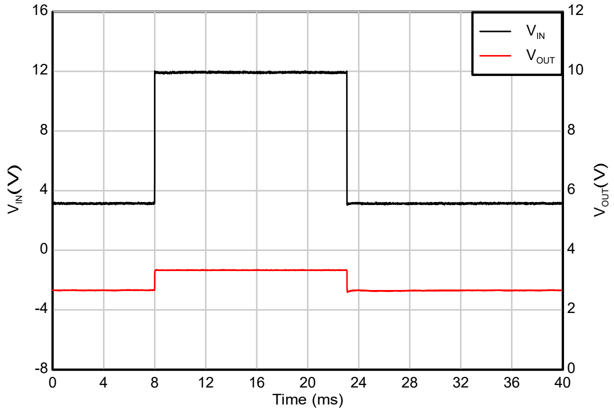
V_{IN} = 12V to 3V, V_{OUT} = 3.3V, I_{OUT} = 100mA, dV_{IN}/dt = 2V/µs

Figure 5-52. Dropout Recovery (12V to 3V)



V_{IN} = 3V to 12V, V_{OUT} = 3.3V, I_{OUT} = 1mA

Figure 5-53. Cold-crank Recovery

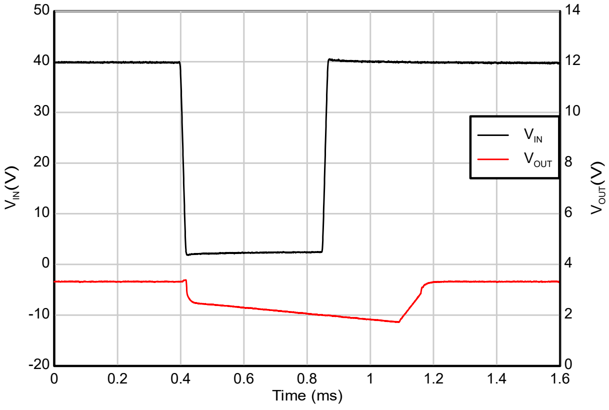


V_{IN} = 4.3V to 3V, V_{OUT} = 3.3V, I_{OUT} = 150mA

Figure 5-54. Cold-crank Recovery

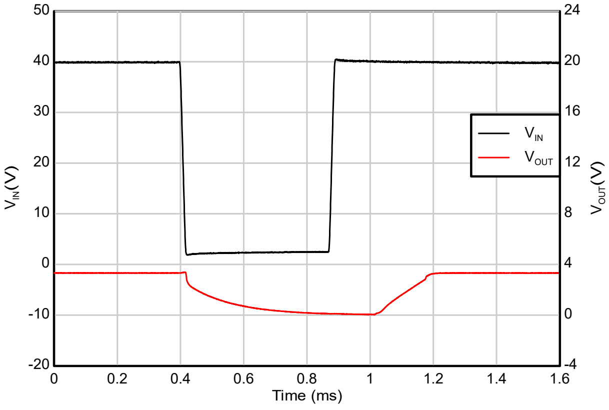
5.6 Typical Characteristics (continued)

at operating junction temperature T_J = 25°C, V_{IN} = 3.0V or V_{IN} = V_{OUT}(nom) + 1.0V (whichever is greater), C_{IN} = 1µF, C_{OUT} = 2.2µF, and I_{OUT} = 1mA (unless otherwise noted)



V_{IN} = 40V to 2V, V_{OUT} = 3.3V, I_{OUT} = 1mA

Figure 5-55. Brown-out Recovery (40V to 2V)



V_{IN} = 40V to 2V, V_{OUT} = 3.3V, I_{OUT} = 50mA

Figure 5-56. Brown-out Recovery (40V to 2V)

6 Detailed Description

6.1 Overview

The TPS7E66-Q1 low-dropout regulator (LDO) consumes ultra-low quiescent current (2.8µA [typical], in fixed configuration) at no-load current. The device offers a wide input voltage range (from 3.0V to 40V), wide output range (from 1.2V to 38V, in adjustable configuration) and up to 150mA of load current. The device is stable with the output capacitor range from 2.2µF to 100µF. The device also provide power-good functionality with delay and de-glitch mechanisms. The delay for power-good can be programmed also using external components on the delay pin.

The low quiescent current across the complete load current range makes the TPS7E66-Q1 designed for powering off-battery loads. The TPS7E66-Q1 has an internal soft-start mechanism that provides an uniform start-up with controlled inrush current. This LDO also has over-current (fold-back), over-power and thermal protection during a load-short or fault condition on the output for better reliability.

6.2 Functional Block Diagrams

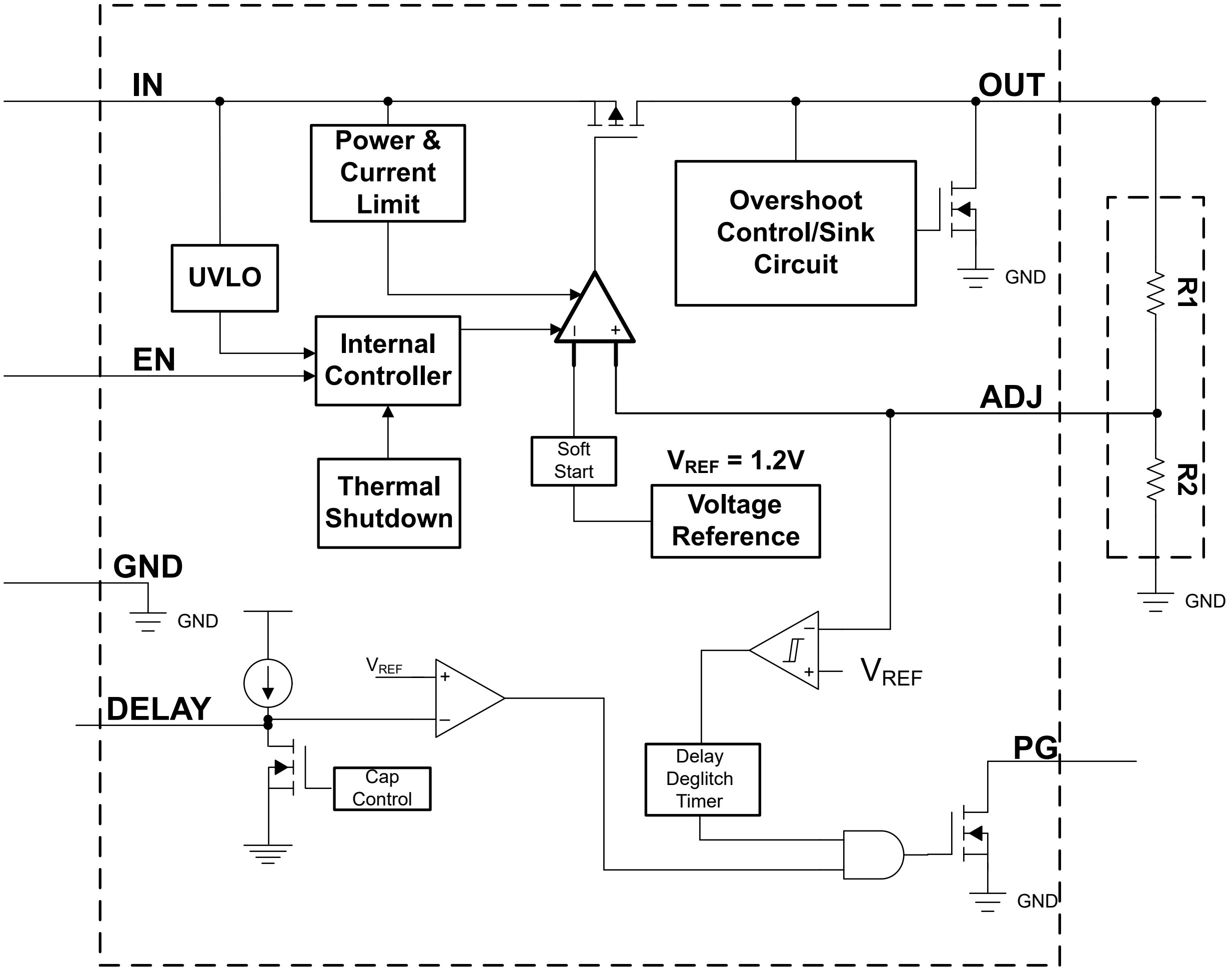


Figure 6-1. Functional Block Diagram: Adjustable Version

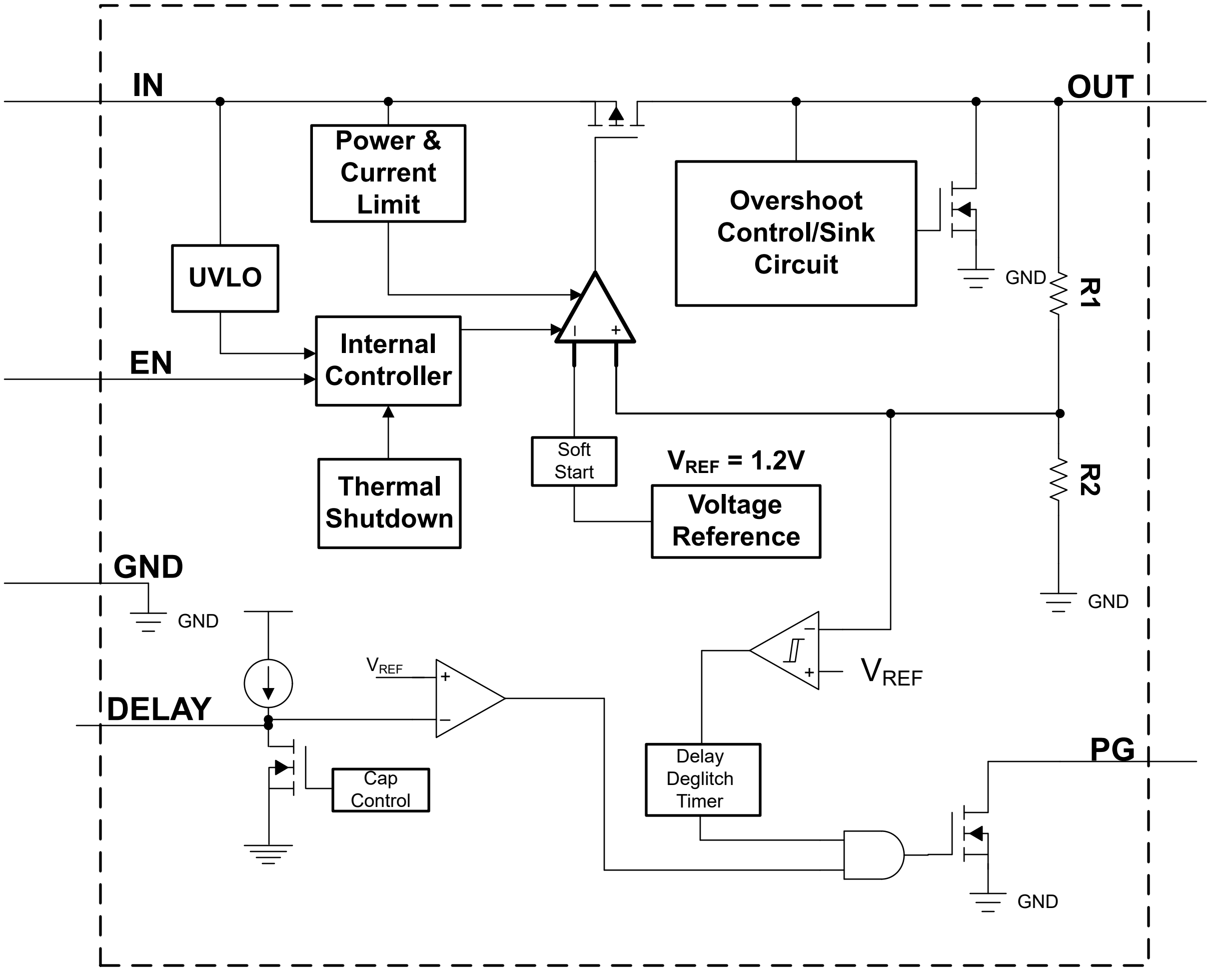


Figure 6-2. Functional Block Diagram: Fixed Version

6.3 Feature Description

6.3.1 Enable (EN)

The enable pin for the device is an active-high pin. The output voltage is enabled when the voltage of the enable pin is greater than the high-level input voltage (V_{IH}) of the EN pin and disabled with the enable pin voltage is less than the low-level input voltage (V_{IL}) of the EN pin. High and low thresholds are listed in the *Electrical Characteristics*. If independent control of the output voltage is not needed, connect the enable pin to the input of the device.

The EN pin also has a weak internal pull-up and the EN pin can be left floating to enable the device. The internal pull-up current on the EN pin is captured in the *Electrical Characteristics* table as Enable pull-up current. However, care must be taken to verify that pin leakage (from board pollution or some other source) does not inadvertently pull this pin low. Leakage must be restricted to 25nA or less to avoid unintentional disabling of the device.

6.3.2 Dropout Voltage

Dropout voltage (V_{DO}) is defined as the input voltage minus the output voltage (V_{IN} – V_{OUT}) at the rated output current (I_{RATED}), where the pass transistor is fully on. I_{RATED} is the maximum I_{OUT} listed in the *Recommended Operating Conditions* table. The pass transistor is in the ohmic or triode region of operation, and acts as a switch. The dropout voltage indirectly specifies a minimum input voltage greater than the nominal programmed output voltage at which the output voltage is expected to stay in regulation. If the input voltage falls to less than the nominal output regulation, then the output voltage falls as well.

For a CMOS regulator, the dropout voltage is determined by the drain-source on-state resistance ($R_{DS(ON)}$) of the pass transistor. Therefore, if the linear regulator operates at less than the rated current, the dropout voltage for that current scales accordingly. The following equation calculates the $R_{DS(ON)}$ of the device.

$$R_{DS(ON)} = \frac{V_{DO}}{I_{RATED}} \tag{1}$$

6.3.3 Power-Good (PG)

The power-good (PG) pin is an open-drain output and can be connected to a regulated supply through an external pullup resistor. The maximum pullup voltage is listed as V_{PG} in the *Recommended Operating Conditions* table. For the PG pin to have a valid output, the voltage on the IN pin must be greater than $V_{UVLO(+)}$, as listed in the *Electrical Characteristics* table. When V_{OUT} exceeds $V_{IT+(PG)}$, the PG output is high impedance and the PG pin voltage pulls up to the connected regulated supply. When the regulated output falls below $V_{IT-(PG)}$, the open-drain output turns on and pulls the PG output low. If output voltage monitoring is not needed, the PG pin can be left floating or connected to ground. By connecting a pullup resistor to an external supply, any downstream device can receive power-good (PG) as a logic signal that can be used for sequencing. Make sure that the external pullup supply voltage results in a valid logic signal for the receiving device.

When using a feed-forward capacitor (C_{FF}) for the adjustable device, the time constant for the LDO start-up is increased whereas the power-good output time constant stays the same, possibly resulting in an invalid status of the power-good output. To avoid this issue, and to receive a valid PG output, make sure that the time constant of both the LDO start-up and the power-good output match, which can be done by adding a capacitor in parallel with the power-good pullup resistor. For more information, see the Pros and Cons of Using a Feedforward Capacitor with a Low-Dropout Regulator application note.

6.3.4 Adjustable Power-Good Delay Timer (DELAY)

The power-good delay period is a function of the external capacitor on the DELAY pin. The adjustable delay configures the amount of time required before the PG pin becomes high. This delay is configured by connecting an external capacitor from this pin to GND. Typical Power-Good Timing Diagram illustrates the typical timing diagram for the power-good delay pin. If the DELAY pin is left floating, the power-good delay is $t_{(Delay\_PG)}$. For more information on how to program the PG delay, see the *Setting the Adjustable Power-Good Delay* section.

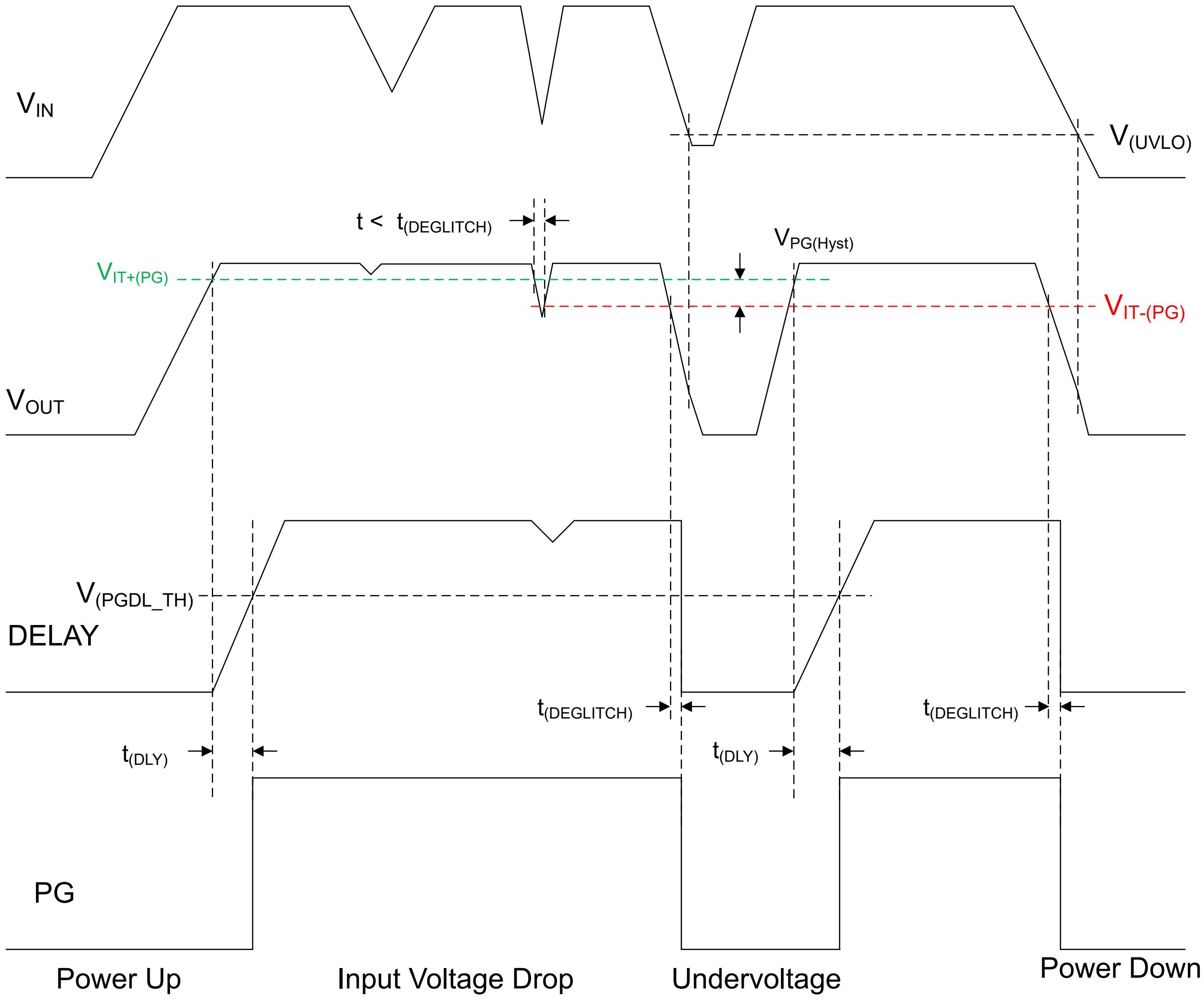


Figure 6-3. Typical Power-Good Timing Diagram

$$V_{PG(Hyst)} = V_{IT+(PG)} - V_{IT-(PG)} \tag{2}$$

6.3.5 Undervoltage Lockout

The device has an independent undervoltage lockout (UVLO) circuit that monitors the input voltage, allowing a controlled and consistent turn on and off of the output voltage. To prevent the device from turning off if the input drops during turn on, the UVLO has in-built hysteresis. The UVLO limits are specified in the *Electrical Characteristics* table.

6.3.6 Thermal Shutdown

The device contains a thermal shutdown protection circuit to disable the device when the junction temperature (T_J) of the pass transistor rises to T_{SD+} (typical). Thermal shutdown hysteresis verifies that the device resets (turns on) when the temperature falls to T_{SD-} (typical).

The thermal time-constant of the semiconductor die is fairly short, thus the device can cycle on and off when thermal shutdown is reached until power dissipation is reduced. Power dissipation during startup can be high from large V_{IN} – V_{OUT} voltage drops across the device or from high inrush currents charging large output capacitors. Under some conditions, the thermal shutdown protection disables the device before startup completes.

For reliable operation, limit the junction temperature to the maximum listed in the *Recommended Operating Conditions* table. Operation above this maximum temperature causes the device to exceed the operational specifications. Although the internal protection circuitry of the device is designed to protect against thermal overall conditions, this circuitry is not intended to replace proper heat sinking. Continuously running the device into thermal shutdown or above the maximum recommended junction temperature reduces long-term reliability.

6.3.7 Foldback Current Limit

The device has an internal current limit circuit that protects the regulator during transient high-load current faults or shorting events. The current limit is a hybrid brickwall-foldback scheme. The current limit transitions from a brickwall scheme to a foldback scheme at the foldback voltage ($V_{FOLDBACK}$). In a high-load current fault with the output voltage above $V_{FOLDBACK}$, the brickwall scheme limits the output current to the current limit (I_{CL}). When the voltage drops below $V_{FOLDBACK}$, a foldback current limit activates that scales back the current as the output voltage approaches GND. When the output is shorted, the device supplies a typical current called the short-circuit current limit (I_{SC}). I_{CL} and I_{SC} are listed in the *Electrical Characteristics* table.

The output voltage is not regulated when the device is in current limit. When a current limit event occurs, the device begins to heat up because of the increase in power dissipation. When the device is in brickwall current limit, the pass transistor dissipates power $[(V_{IN} – V_{OUT}) \times I_{CL}]$. When the device output is shorted and the output is below $V_{FOLDBACK}$, the pass transistor dissipates power $[(V_{IN} – V_{OUT}) \times I_{SC}]$. If thermal shutdown is triggered, the device turns off. After the device cools down, the internal thermal shutdown circuit turns the device back on. If the output current fault condition continues, the device cycles between current limit and thermal shutdown. For more information on current limits, see the *Know Your Limits* application note.

Foldback Current Limit shows a diagram of the foldback current limit.

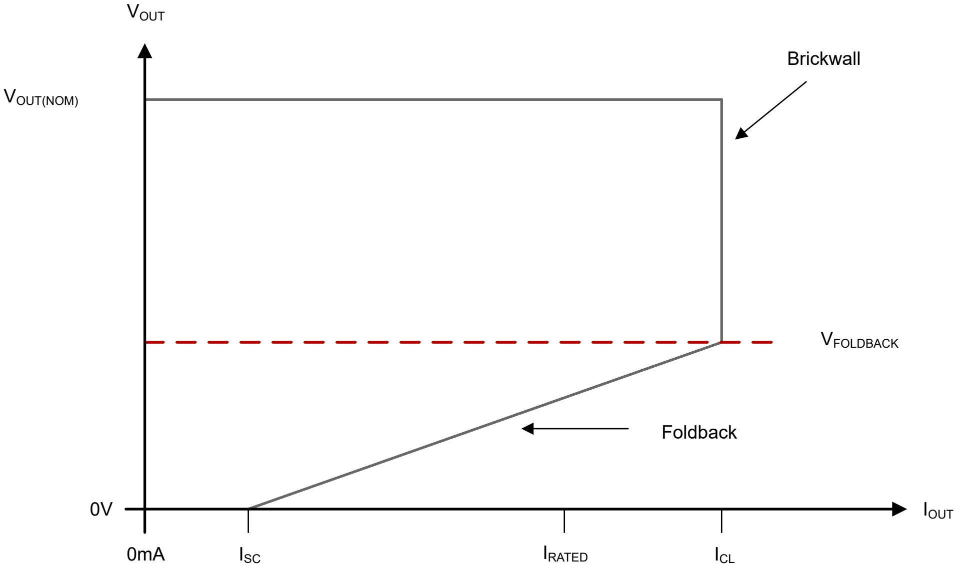


Figure 6-4. Foldback Current Limit

6.3.8 Power Limit

The device has an internal over-power limit circuit that limits the power dissipated across the LDO with-in the internal SOA (safe operating area) limits. The SOA limits for the LDO factors in safe operation for both silicon components, and bondwires used in packaging. These limits verify reliable operation of the device and prevent the device failure from overheating, breakdown, or other damaging effects.

The power dissipated (P_{Dissip}) across the LDO is defined by voltage drop across LDO (V_{IN} - V_{OUT}) and load current (I_L) flowing through.

$$P_{Dissip} = (V_{IN} - V_{OUT}) \times I_{OUT} \tag{3}$$

The power limiting circuit, monitors both the voltage drop (headroom, V_{IN} - V_{OUT}) across LDO and output load current (I_{OUT}) flowing through. If P_{Dissip} crosses the defined SOA limits, the power limiting circuit, limits the load current (I_{OUT}) flowing through. The output voltage is not regulated when the device is in Power limit operation. The maximum supported current (I_{PLIMIT}) at full headroom (V_{IN} - V_{OUT} = 40V) and Max supported headroom ($V_{PHEADROOM}$) at full load current are captured in *Electrical Characteristics*.

Power Limiting shows a diagram of the power limiting.

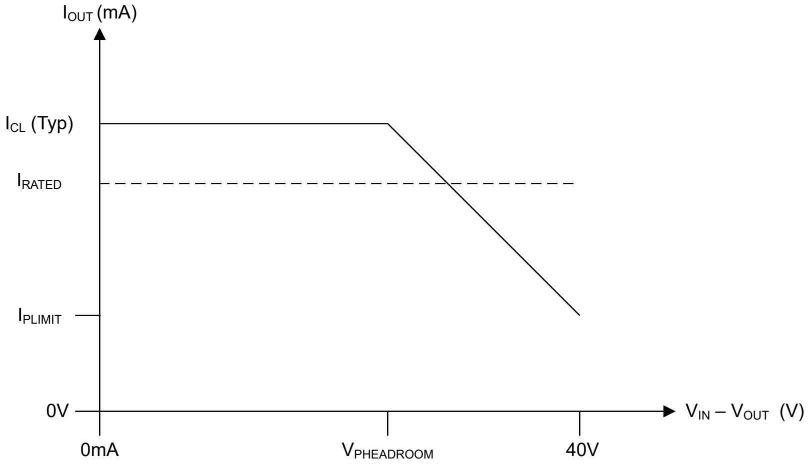


Figure 6-5. Power Limiting

6.3.9 Output Pulldown

The device has an output pulldown circuit. V_{OUT} pulldown sink to ground capability is listed in the *Electrical Characteristics* table. The output pulldown activates under the following conditions:

- $V_{EN} < V_{IL(EN)}$
- $1.0V < V_{IN} < V_{UVLO}$

The output pulldown resistance for this device is 750Ω typical. The pulldown resistance, $V_{IL(EN)}$ and V_{UVLO} thresholds are listed in the *Electrical Characteristics* table.

Do not rely on the output pulldown circuit for discharging a large amount of output capacitance after the input supply has collapsed because reverse current can flow from the output to the input. This reverse current flow can cause damage to the device. See the *Reverse Current* section for more details.

6.4 Device Functional Modes

Device Functional Mode Comparison provides a quick comparison between the normal and dropout modes of operation.

Table 6-1. Device Functional Mode Comparison

OPERATING MODE	PARAMETER	
	V_{IN}	I_{OUT}
Normal	$V_{IN} > V_{OUT(nom)} + V_{DO}$	$I_{OUT} < I_{CL}$
Dropout	$V_{IN} < V_{OUT(nom)} + V_{DO}$	$I_{OUT} < I_{CL}$

6.4.1 Device Functional Mode Comparison

The *Device Functional Mode Comparison* table shows the conditions that lead to the different modes of operation. See the *Electrical Characteristics* table for parameter values.

Table 6-2. Device Functional Mode Comparison

OPERATING MODE	PARAMETER			
	V_{IN}	V_{EN}	I_{OUT}	T_J
Normal operation	$V_{IN} > V_{OUT(nom)} + V_{DO}$ and $V_{IN} > V_{IN(min)}$	$V_{EN} > V_{EN(HI)}$	$I_{OUT} < I_{OUT(max)}$	$T_J < T_{SD(shutdown)}$
Dropout operation	$V_{IN(min)} < V_{IN} < V_{OUT(nom)} + V_{DO}$	$V_{EN} > V_{EN(HI)}$	$I_{OUT} < I_{OUT(max)}$	$T_J < T_{SD(shutdown)}$
Disabled (any true condition disables the device)	$V_{IN} < V_{UVLO}$	$V_{EN} < V_{EN(LOW)}$	Not applicable	$T_J > T_{SD(shutdown)}$

6.4.2 Normal Operation

The device regulates to the nominal output voltage under the following conditions:

- The input voltage is greater than the nominal output voltage plus the dropout voltage ($V_{OUT(nom)} + V_{DO}$)
- The headroom across the LDO ($V_{IN} - V_{OUT}$) is less than $V_{PHEADROOM}$ for required I_{OUT}, such that power limit is not engaged
- The output current is less than the current limit ($I_{OUT} < I_{CL}$)
- The device junction temperature is greater than –40°C and less than +150°C
- The device junction temperature is less than the thermal shutdown temperature ($T_J < T_{SD}$)
- The enable voltage has previously exceeded the enable rising threshold voltage and has not yet decreased to less than the enable falling threshold

6.4.3 Dropout Operation

The device operates in dropout mode when the input voltage is lower than the nominal output voltage plus the specified dropout voltage. However, make sure all other conditions are met for normal operation. In dropout operation, the pass transistor is in the ohmic or triode region of operation, and acts as a switch. Because of this operation, the transient performance of the device becomes significantly degraded. Line or load transients in dropout potentially result in large output voltage deviations.

When the device is in a steady dropout state, the pass transistor is driven into the ohmic or triode region. This state is defined as when the device is in dropout, directly after being in a normal regulation state, but *not* during start up. During dropout, $V_{IN} < V_{OUT(NOM)} + V_{DO}$. When the input voltage returns to a value ≥ $V_{OUT(NOM)} + V_{DO}$, the output voltage overshoots for a short period of time. During this time, the device pulls the pass transistor back into the linear region. $V_{OUT(NOM)}$ is the nominal output voltage and V_{DO} is the dropout voltage.

The TPS7E66-Q1 keeps the IQ controlled in dropout operation to much lower values (12µA (typ) in no-load dropout) compared to conventional linear voltage regulators which avoids the battery drainage, once the battery levels falls below the required input voltage levels.

6.4.4 Disabled

The output of the device can be shutdown by forcing the voltage of the enable pin to less than the maximum EN pin low-level input voltage (see the *Electrical Characteristics* table). When disabled, the pass transistor is turned off, internal circuits are shutdown, and the output voltage is actively discharged to ground by an internal discharge circuit from the output to ground.

7 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

7.1 Application Information

7.1.1 Adjustable Device Feedback Resistor Selection

The adjustable-version device requires external feedback divider resistors to set the output voltage. V_{OUT} is set using the feedback divider resistors, R_1 and R_2, according to the following equation:

$$V_{OUT} = V_{ADJ} \times (1 + R_1 / R_2) \tag{4}$$

V_{ADJ} (or V_{FB}) is the feedback voltage and refers to the voltage on the ADJ pin. During normal operation of the adjustable device, the devices regulates such that the V_{ADJ} is equal to the device's internal reference voltage.

To ignore the ADJ pin current error term in the V_{OUT} equation, set the feedback divider current to 100x the ADJ pin current (I_{ADJ}) listed in the *Electrical Characteristics* table. This setting provides the maximum feedback divider series resistance, as shown in the following equation:

$$R_1 + R_2 \leq \frac{V_{OUT}}{\left[I_{ADJ} \times 100\right]} \tag{5}$$

7.1.2 Recommended Capacitor Types

The device is designed to be stable using low equivalent series resistance (ESR) ceramic capacitors at the input and output. Multilayer ceramic capacitors have become the industry standard for these types of applications and are recommended, but must be used with good judgment. Ceramic capacitors that employ X7R-, X5R-, and C0G-rated dielectric materials provide relatively good capacitive stability across temperature, whereas the use of Y5V-rated capacitors is discouraged because of large variations in capacitance.

Regardless of the ceramic capacitor type selected, the effective capacitance varies with operating voltage and temperature. Generally expect the effective capacitance to decrease by as much as 50%. The input and output capacitors recommended in the *Electrical Characteristics* table account for an effective capacitance of approximately 50% of the nominal value.

7.1.3 Input and Output Capacitor Selection

The TPS7E66-Q1 requires an output capacitor of 2.2µF or larger (1.0µF or larger capacitance) for stability and an equivalent series resistance (ESR) between 0.0Ω and 1.0Ω. For best transient performance, use X5R- and X7R-type ceramic capacitors because these capacitors have minimal variation in value and ESR over temperature. When selecting a capacitor for a specific application, be mindful of the DC bias characteristics for the capacitor. Higher output voltages cause a significant derating of the capacitor. For best performance, the maximum recommended output capacitor is 100µF.

Although an input capacitor is not required for stability, good analog design practice is to connect a capacitor from IN to GND. Some input supplies have a high impedance, thus placing the input capacitor on the input supply helps reduce the input impedance. This capacitor counteracts reactive input sources and improves transient response, input ripple, and PSRR. If the input supply has a high impedance over a large range of frequencies, several input capacitors can be used in parallel to lower the impedance over frequency. Use a higher-value capacitor if large, fast, rise-time load transients are anticipated, or if the device is located several inches from the input power source.

7.1.4 Reverse Current

Excessive reverse current potentially damages this device. Reverse current flows through the intrinsic body diode of the PMOS pass transistor instead of the normal conducting channel. At high magnitudes, this current flow degrades the long-term reliability of the device.

Conditions where reverse current occur are outlined in this section, all of which exceed the absolute maximum rating of $V_{OUT} \leq V_{IN}$ + 0.3V. These conditions are:

- If the device has a large C_{OUT} and the input supply collapses with little or no load current
- The output is biased when the input supply is not established
- The output is biased above the input supply

If reverse current flow is expected in the application, use external protection to protect the device. Reverse current is not limited in the device, so external limiting is required if extended reverse voltage operation is anticipated. Limit reverse current to 5% or less of the rated output current of the device in the event this current cannot be avoided.

Example Circuit for Reverse Current Protection Using a Schottky Diode shows one approach for protecting the device.

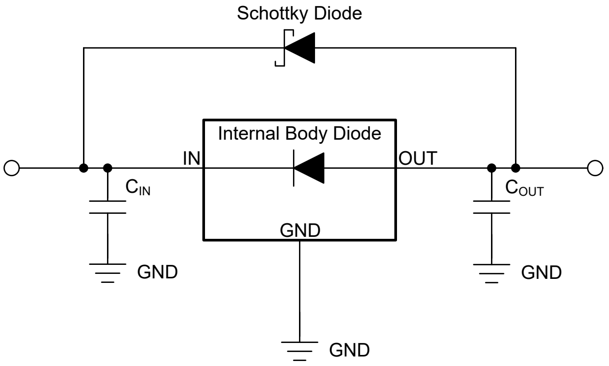


Figure 7-1. Example Circuit for Reverse Current Protection Using a Schottky Diode

7.1.5 Feed-Forward Capacitor

For the adjustable-voltage version device, a feed-forward capacitor (C_{FF}) can be connected from the OUT pin to the ADJ pin. C_{FF} improves transient, noise, and PSRR performance, but is not required for regulator stability. Recommended C_{FF} values are listed in the *Recommended Operating Conditions* table. A higher capacitance C_{FF} can be used; however, the start-up time increases. For a detailed description of C_{FF} tradeoffs, see the *Pros and Cons of Using a Feedforward Capacitor with a Low-Dropout Regulator* application note.

C_{FF} and R_1 form a zero in the loop gain at frequency f_Z, while C_{FF}, R_1, and R_2 form a pole in the loop gain at frequency f_P. C_{FF} zero and pole frequencies can be calculated from the following equations:

$$f_Z = \frac{1}{[2 \times \pi \times C_{FF} \times R_1]} \tag{6}$$

$$f_P = \frac{1}{[2 \times \pi \times C_{FF} \times (R_1 \| R_2)]} \tag{7}$$

7.1.6 Estimating Junction Temperature

The JEDEC standard now recommends using psi (Ψ) thermal metrics to estimate the LDO junction temperatures when in-circuit on a typical PCB board application. These metrics are not strictly speaking thermal resistances, but rather offer practical and relative means of estimating junction temperatures. These psi metrics are determined to be significantly independent of the copper-spreading area. The key thermal metrics (Ψ_{JT} and Ψ_{JB}) are used in accordance with Equation 8 and are given in the *Thermal Information* table.

$$\Psi_{JT}: T_J = T_T + \Psi_{JT} \times P_D$$
$$\Psi_{JB}: T_J = T_B + \Psi_{JB} \times P_D \tag{8}$$

where:

- P_D is the power dissipated as explained in Equation 8
- T_T is the temperature at the center-top of the device package
- T_B is the PCB surface temperature measured 1mm from the device package and centered on the package edge

The *Thermal Information* table lists the primary thermal metrics, which are the junction-to-top characterization parameter (ψ_{JT}) and junction-to-board characterization parameter (ψ_{JB}). These parameters provide two methods for calculating the junction temperature (T_J), as described in the following equations. Use the junction-to-top characterization parameter (ψ_{JT}) with the temperature at the center-top of device package (T_T) to calculate the junction temperature. Use the junction-to-board characterization parameter (ψ_{JB}) with the printed circuit board (PCB) surface temperature 1mm from the device package (T_B) to calculate the junction temperature.

$$T_J = T_T + \Psi_{JT} \times P_D \tag{9}$$

where:

- P_D is the dissipated power
- T_T is the temperature at the center-top of the device package

$$T_J = T_B + \Psi_{JB} \times P_D \tag{10}$$

where:

- T_B is the PCB surface temperature measured 1mm from the device package and centered on the package edge

For detailed information on the thermal metrics and how to use the metrics, see the *Semiconductor and IC Package Thermal Metrics* application note.

7.1.7 Power Dissipation (P_D)

Circuit reliability requires proper consideration of the device power dissipation, location of the circuit on the printed circuit board (PCB), and correct sizing of the thermal plane. Verify the PCB area around the regulator has few or no other heat-generating devices that cause added thermal stress.

To first-order approximation, power dissipation in the regulator depends on the input-to-output voltage difference and load conditions. The following equation calculates power dissipation (P_D).

$$P_D = (V_{IN} - V_{OUT}) \times I_{OUT} \tag{11}$$

Note

Power dissipation is minimized, and thus greater efficiency achieved, by proper selection of the system voltage rails. Proper selection allows the minimum input-to-output voltage differential to be obtained. The low dropout of the device allows for maximum efficiency across a wide range of output voltages.

For devices with a thermal pad, the primary heat conduction path for the device package is through the thermal pad to the PCB. Solder the thermal pad to a copper pad area under the device. This pad area contains an array of plated vias that conduct heat to additional copper planes for increased heat dissipation.

The maximum power dissipation determines the maximum allowable ambient temperature (T_A) for the device. Power dissipation and junction temperature are most often related by the $R_{\theta JA}$ of the combined PCB and device package and the T_A. $R_{\theta JA}$ is the junction-to-ambient thermal resistance and T_A is the temperature of the ambient air. The following equation describes this relationship.

$$T_J = T_A + \left(R_{\theta JA} \times P_D\right) \tag{12}$$

The following equation rearranges this relationship for output current.

$$I_{OUT} = \frac{\left(T_J - T_A\right)}{\left[R_{\theta JA} \times \left(V_{IN} - V_{OUT}\right)\right]} \tag{13}$$

Thermal resistance ($R_{\theta JA}$) is highly dependent on the heat-spreading capability built into the particular PCB design. This resistance therefore varies according to the total copper area, copper weight, and location of the planes. The junction-to-ambient thermal resistance listed in the *Thermal Information* table is determined by the JEDEC standard PCB and copper-spreading area. $R_{\theta JA}$ is used as a relative measure of package thermal performance. For packages with thermal pad and a well-designed thermal layout, $R_{\theta JA}$ is actually the sum of the package's $R_{\theta JCbot}$ plus the thermal resistance contribution by the PCB copper. $R_{\theta JCbot}$ is the junction-to-case (bottom) thermal resistance, as given in the *Thermal Information* table.

7.1.8 Power Dissipation Versus Ambient Temperature

TPS7E66-Q1 Allowable Power Dissipation is based off of a JESD51-7 4-layer, high-K board. The allowable power dissipation is estimated using the following equation. As discussed in the *An empirical analysis of the impact of board layout on LDO thermal performance* application note, thermal dissipation can be improved in the JEDEC high-K layout by adding top layer copper and increasing the number of thermal vias. If a good thermal layout is used, the allowable thermal dissipation can be improved by up to 50%.

$$T_A + \left(R_{\theta JA} \times P_D\right) \le 150\ ^\circ\mathrm{C} \tag{14}$$

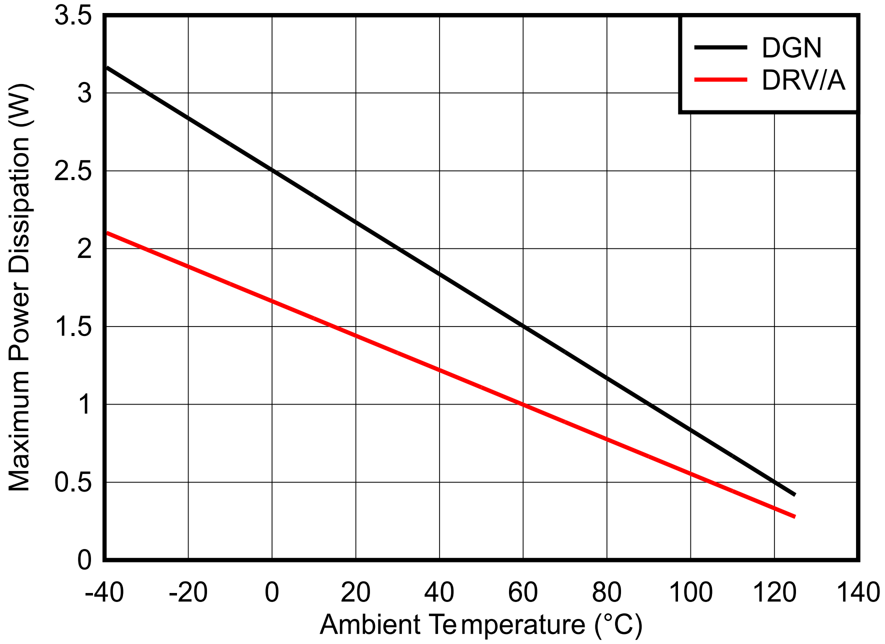


Figure 7-2. TPS7E66-Q1 Allowable Power Dissipation

7.2 Typical Application

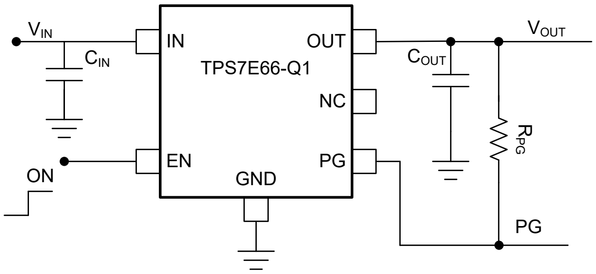


Figure 7-3. Typical Application Circuit (Fixed-Voltage Version)

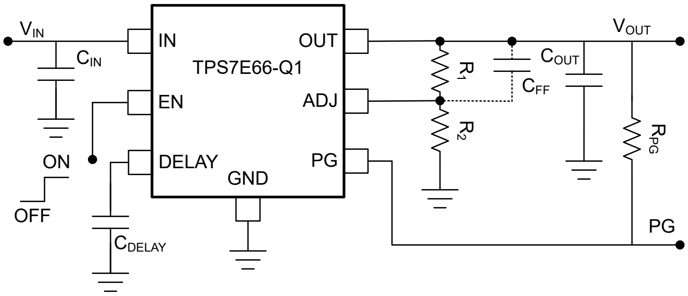


Figure 7-4. Typical Application Circuit (Adjustable-Voltage Version)

NOTE: Dotted lines indicate an optional input capacitor and feed-forward capacitor. See the *Input and Output Capacitor Selection* and *Feed-Forward Capacitor* sections and the *Recommended Operating Conditions* table.

Table 7-1. Adjustable Output Voltage for Resistors R_1 and R_2

OUTPUT VOLTAGE (V)	R_1 (MΩ)	R_2 (MΩ)
1.8	0.499	1
2.8	1.33	1
5.0	3.16	1

7.2.1 Design Requirements

Design Parameters summarizes the design requirements for Figure 7-3.

Table 7-2. Design Parameters

PARAMETER	DESIGN REQUIREMENT
Input voltage	12V
Output voltage	3.3V
Output current	100mA
Output capacitor	2.2µF

7.2.2 Selecting Feedback Resistors

For this design example, V_{OUT} is set to 3.3V. The following equations set the feedback divider resistors for the desired output voltage:

$$V_{OUT} = V_{ADJ} \times \left(1 + \frac{R_1}{R_2}\right) \tag{15}$$

$$R_1 + R_2 \le \frac{V_{OUT}}{(I_{ADJ} \times 100)} \tag{16}$$

For improved output accuracy, use Equation 16 and I_{ADJ} = 10nA as listed in the *Electrical Characteristics* table to calculate the upper limit for series feedback resistance ($R_1 + R_2 \leq 3.3M\Omega$).

The control-loop error amplifier drives the FB pin to the same voltage as the internal reference (V_{ADJ} = 1.2V, as listed in the *Electrical Characteristics* table). Use Equation 15 to determine the ratio of R_1 / R_2 = 1.75 Use this ratio and solve Equation 16 for R_1. Now calculate the upper limit for $R_1 \leq 2.1M\Omega$. Select a standard value resistor for R_1 = 1.75MΩ.

Reference Equation 17 and solve for R_2:

$$R_2 = \frac{R_1}{\left[\left(\frac{V_{OUT}}{V_{ADJ}}\right) - 1\right]} \tag{17}$$

From Equation 17, R_2 = 1MΩ is determined. Select a standard value resistor for R_2 = 1MΩ. V_{OUT} = 3.3V. Verify that the feedback divider current is greater than the minimum value in the *Recommended Operating Conditions* table.

The following equation calculates the feedback divider current.

$$I_{FB\_Divider} = \frac{V_{OUT}}{(R_1 + R_2)} \tag{18}$$

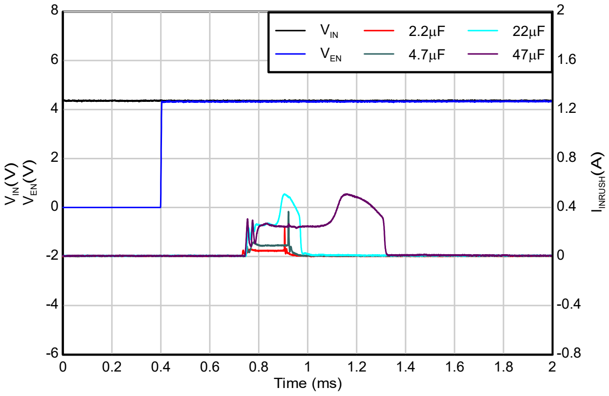
7.2.3 Setting the Adjustable Power-Good Delay

The power-good delay time can be set in two ways: either by floating the DELAY pin or by connecting a capacitor from this pin to GND. When the DELAY pin is floating, the time defaults to $t_{DELAY(PG)}$, listed in Electrical Characteristics. The delay time is set by the following equation if a capacitor is connected between the DELAY pin and GND.

$$t = t_{Delay(PG)} + C_{DELAY}\left(\frac{V_{PGDL\_TH}}{I_{PGDL\_CHG}}\right) \tag{19}$$

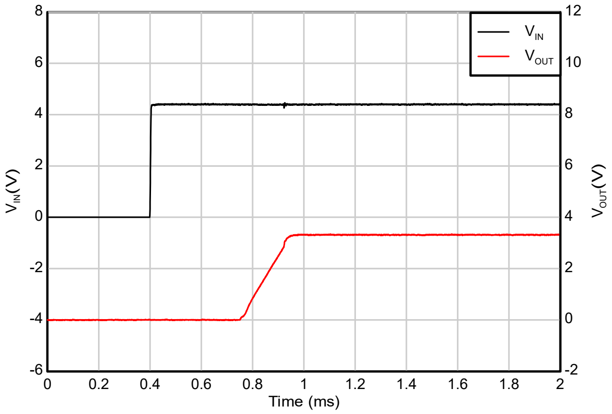
7.2.4 Application Curves

at operating junction temperature T_J = 25°C, V_{IN} = 3.0V or V_{IN} = V_{OUT}(nom) + 1.0V (whichever is greater), C_{IN} = 1µF, C_{OUT} = 2.2µF, C_{DELAY} = 0nF, and I_{OUT} = 1mA (unless otherwise noted)



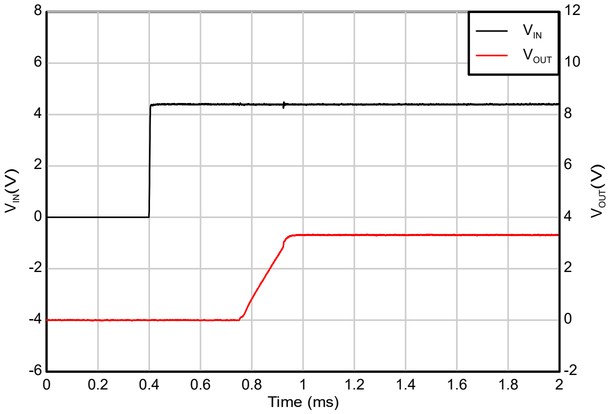
V_{IN} = 4.3V, V_{OUT} = 3.3V, I_{OUT} = 0mA

Figure 7-5. Inrush Current vs C_{OUT}



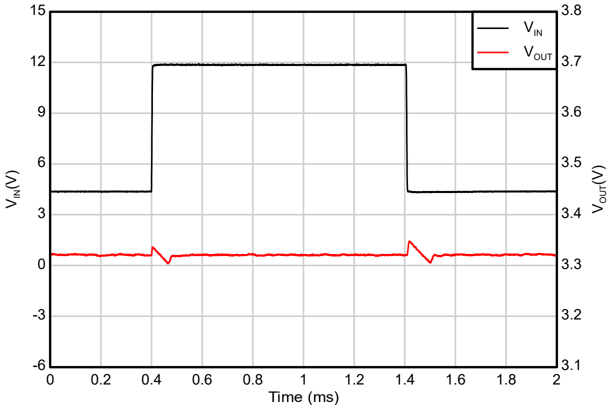
V_{IN} = 4.3V, V_{OUT} = 3.3V, I_{OUT} = 1mA

Figure 7-6. Start-up with EN & V_{IN} tied together



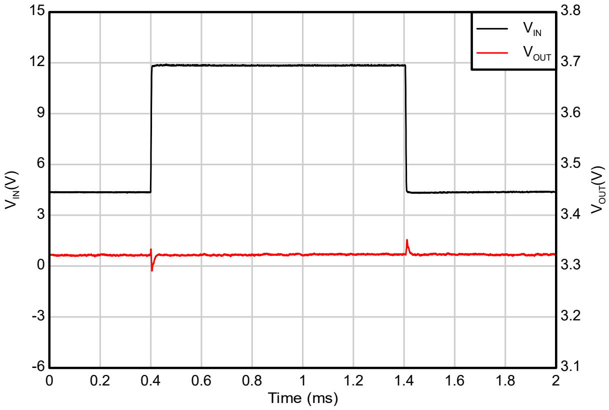
V_{IN} = 4.3V, V_{OUT} = 3.3V, I_{OUT} = 50mA

Figure 7-7. Start-up with EN & V_{IN} tied together



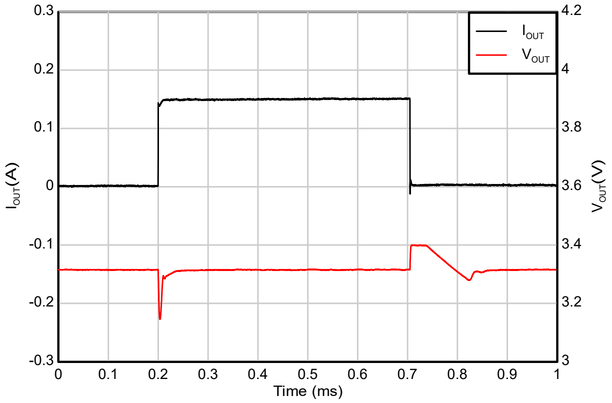
V_{IN} = 4.3V to 12V, V_{OUT} = 3.3V, I_{OUT} = 1mA, dV_{IN}/dt = 2V/µs

Figure 7-8. Line Transient (4.3V to 12V)



V_{IN} = 4.3V to 12V, V_{OUT} = 3.3V, I_{OUT} = 150mA, dV_{IN}/dt = 2V/µs

Figure 7-9. Line Transient (4.3V to 12V)

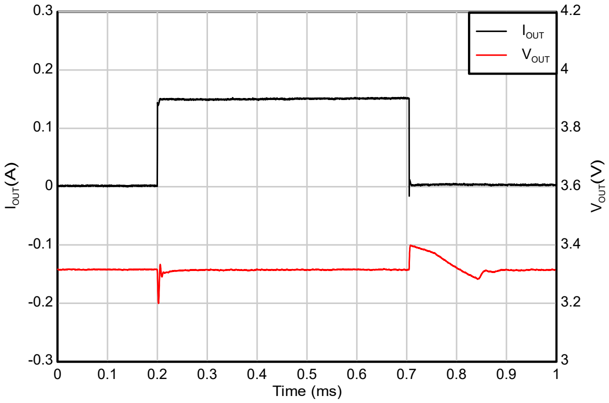


V_{IN} = 4.3V, V_{OUT} = 3.3V, I_{OUT} = 0mA to 150mA, dI_{OUT}/dt = 2A/µs

Figure 7-10. Load Transient (0mA to 150mA)

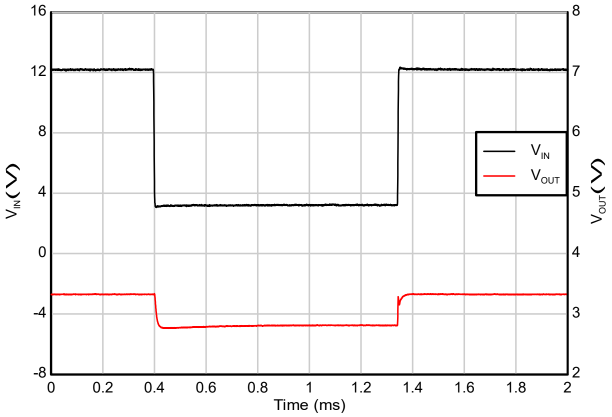
7.2.4 Application Curves (continued)

at operating junction temperature T_J = 25°C, V_{IN} = 3.0V or V_{IN} = V_{OUT}(nom) + 1.0V (whichever is greater), C_{IN} = 1µF, C_{OUT} = 2.2µF, C_{DELAY} = 0nF, and I_{OUT} = 1mA (unless otherwise noted)



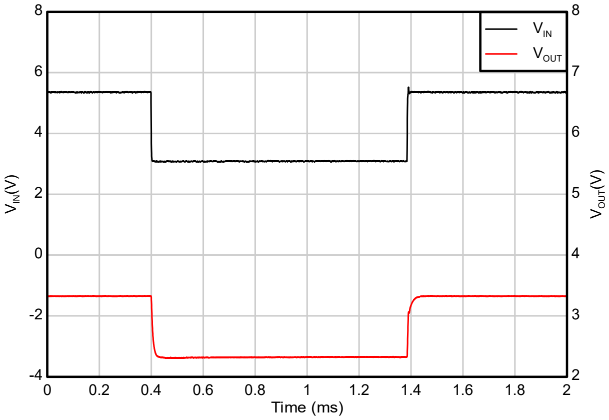
V_{IN} = 4.3V, V_{OUT} = 3.3V, I_{OUT} = 1mA to 150mA, dI_{OUT}/dt = 2A/µs

Figure 7-11. Load Transient (1mA to 150mA)



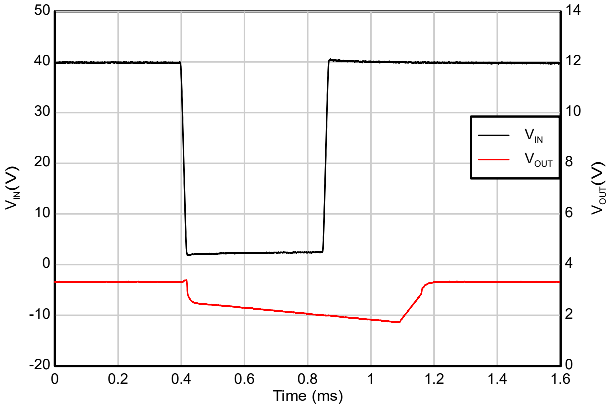
V_{IN} = 12V to 3V, V_{OUT} = 3.3V, I_{OUT} = 100mA, dV_{IN}/dt = 2V/µs

Figure 7-12. Dropout Recovery (12V to 3V)



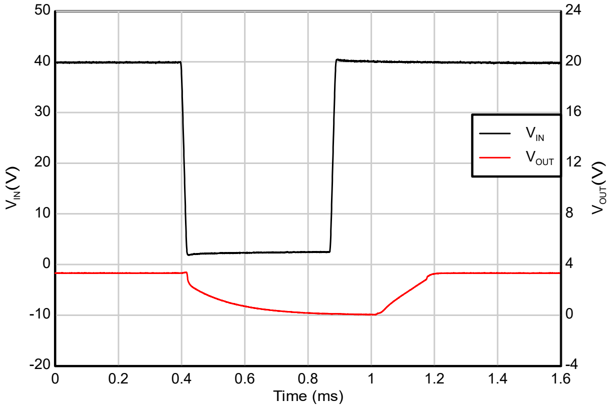
V_{IN} = 5.3V to 3V, V_{OUT} = 3.3V, I_{OUT} = 300mA, dV_{IN}/dt = 2V/µs

Figure 7-13. Dropout Recovery (5.3V to 3V)



V_{IN} = 40V to 2V, V_{OUT} = 3.3V, I_{OUT} = 1mA

Figure 7-14. Brown-out Recovery (40V to 2V)



V_{IN} = 40V to 2V, V_{OUT} = 3.3V, I_{OUT} = 50mA

Figure 7-15. Brown-out Recovery (40V to 2V)

7.3 Power Supply Recommendations

The TPS7E66-Q1 is designed to operate from an input voltage supply range from 3.0V to 40V. The input voltage range provides adequate headroom for the device to have a regulated output. If the input supply is noisy, additional input capacitors with low ESR help improve output noise performance.

7.4 Layout

7.4.1 Layout Guidelines

For best overall performance, follow the guidelines in this section. Place all circuit components on the same side of the printed circuit board (PCB) and as near as practical to the respective LDO pin connections. Place ground return connections for the input and output capacitors as close to the GND pin as possible, using wide, component-side, copper planes. Do not use vias and long traces to create LDO circuit connections to the input capacitor, output capacitor, or resistor divider. This practice negatively affects system performance. This grounding and layout scheme minimizes inductive parasitics, and thereby reduces load current transients, minimizes noise, and increases circuit stability. A ground reference plane is also recommended and is embedded in the PCB or located on the bottom side of the PCB opposite the components. This reference plane serves to provide accuracy of the output voltage and shield the LDO from noise. To improve the thermal performance of the device, and to maximize the current output at high ambient temperature, spread the copper under the thermal pad as far as possible and place enough thermal vias on the copper under the thermal pad. Figure 7-17 and Figure 7-16 show example layouts for TPS7E66-Q1 packages.

7.4.2 Layout Example

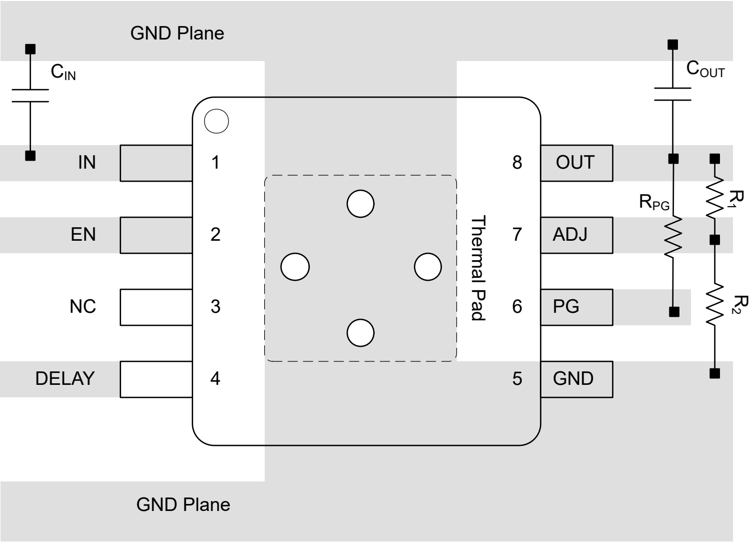


Figure 7-16. Example Layout for TPS7E66-Q1 DGN Package

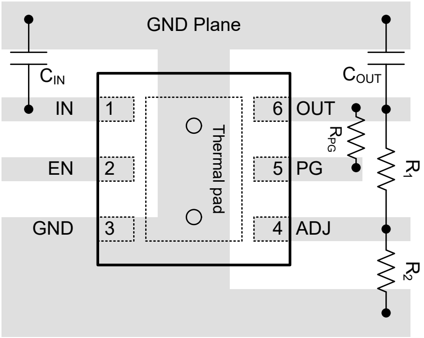


Figure 7-17. Example Layout for TPS7E66-Q1 DRV Package

8 Device and Documentation Support

8.1 Documentation Support

8.1.1 Related Documentation

For related documentation see the following:

- Texas Instruments, *Know Your Limits* application note
- Texas Instruments *Low Quiescent Current LDOs for Battery Connected Automotive Systems* application note

8.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

8.3 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

8.4 Trademarks

TI E2E™ is a trademark of Texas Instruments.
All trademarks are the property of their respective owners.

8.5 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

8.6 Glossary

TI Glossary	This glossary lists and explains terms, acronyms, and definitions.

9 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision * (October 2025) to Revision A (April 2026)	**Page**
• Changed the document status from *Advance Information* to *Production Data*	1

10 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TPS7E6601AQWDRVRQ1	Active	Production	WSON (DRV) | 6	3000 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 150	3V5H
TPS7E6630QWDRVRQ1	Active	Production	WSON (DRV) | 6	3000 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 150	3UWH
TPS7E6633AQWDRVRQ1	Active	Production	WSON (DRV) | 6	3000 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 150	3V7H
TPS7E6633QWDRVRQ1	Active	Production	WSON (DRV) | 6	3000 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 150	3UXH
TPS7E6650AQWDRVRQ1	Active	Production	WSON (DRV) | 6	3000 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 150	3V8H
TPS7E6650QWDRVRQ1	Active	Production	WSON (DRV) | 6	3000 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 150	3UZH

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

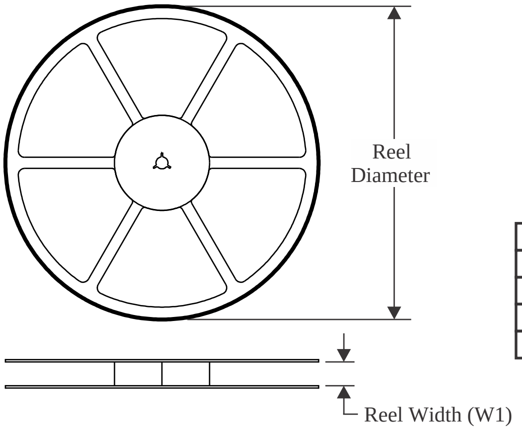
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

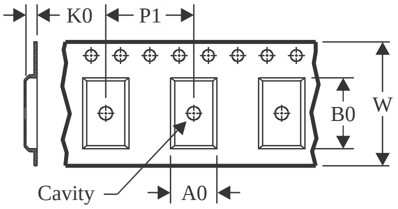
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

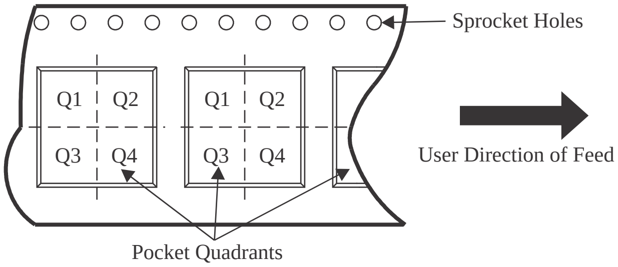


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

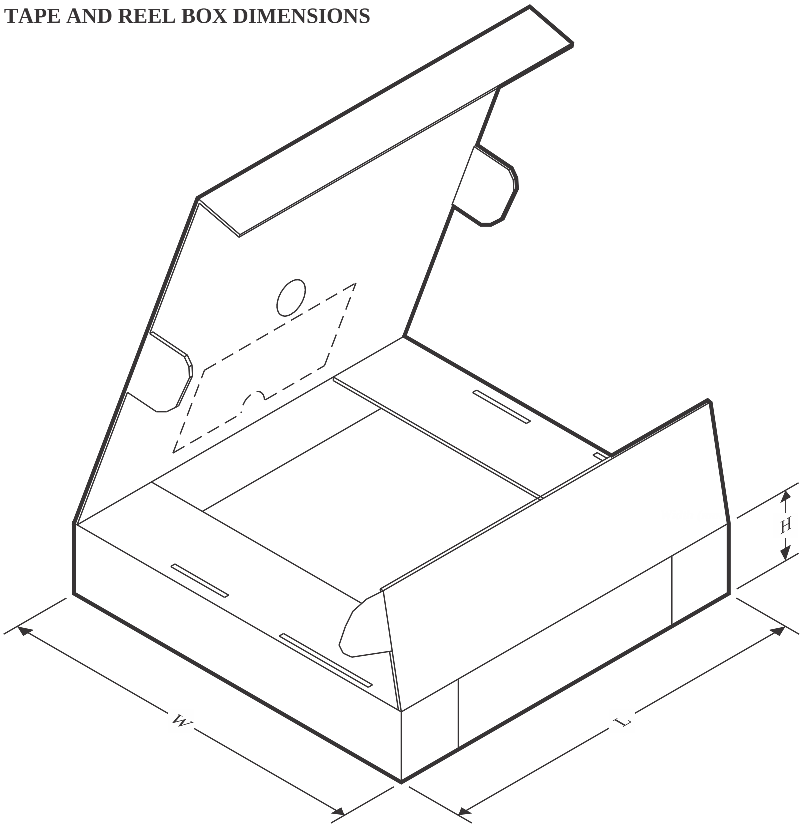
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS7E6601AQWDRVRQ1	WSON	DRV	6	3000	180.0	8.4	2.3	2.3	1.15	4.0	8.0	Q2
TPS7E6633AQWDRVRQ1	WSON	DRV	6	3000	180.0	8.4	2.3	2.3	1.15	4.0	8.0	Q2
TPS7E6650AQWDRVRQ1	WSON	DRV	6	3000	180.0	8.4	2.3	2.3	1.15	4.0	8.0	Q2
TPS7E6650QWDRVRQ1	WSON	DRV	6	3000	180.0	8.4	2.3	2.3	1.15	4.0	8.0	Q2

TAPE AND REEL BOX DIMENSIONS



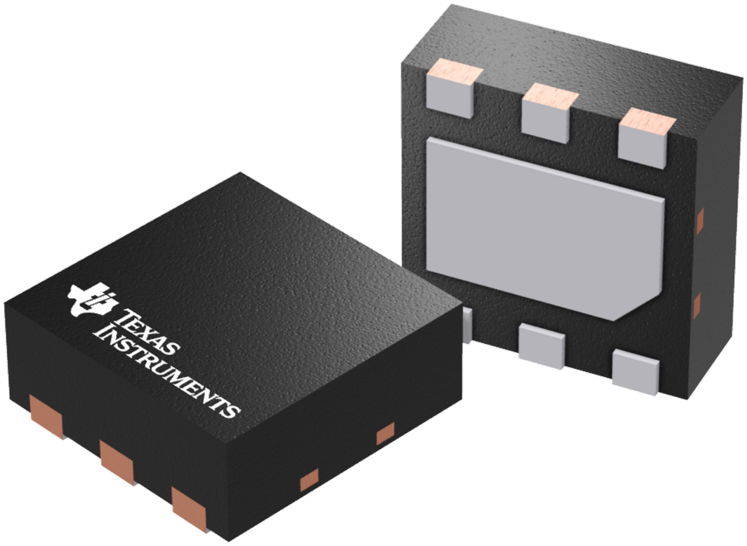
*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS7E6601AQWDRVRQ1	WSON	DRV	6	3000	210.0	185.0	35.0
TPS7E6633AQWDRVRQ1	WSON	DRV	6	3000	210.0	185.0	35.0
TPS7E6650AQWDRVRQ1	WSON	DRV	6	3000	210.0	185.0	35.0
TPS7E6650QWDRVRQ1	WSON	DRV	6	3000	210.0	185.0	35.0

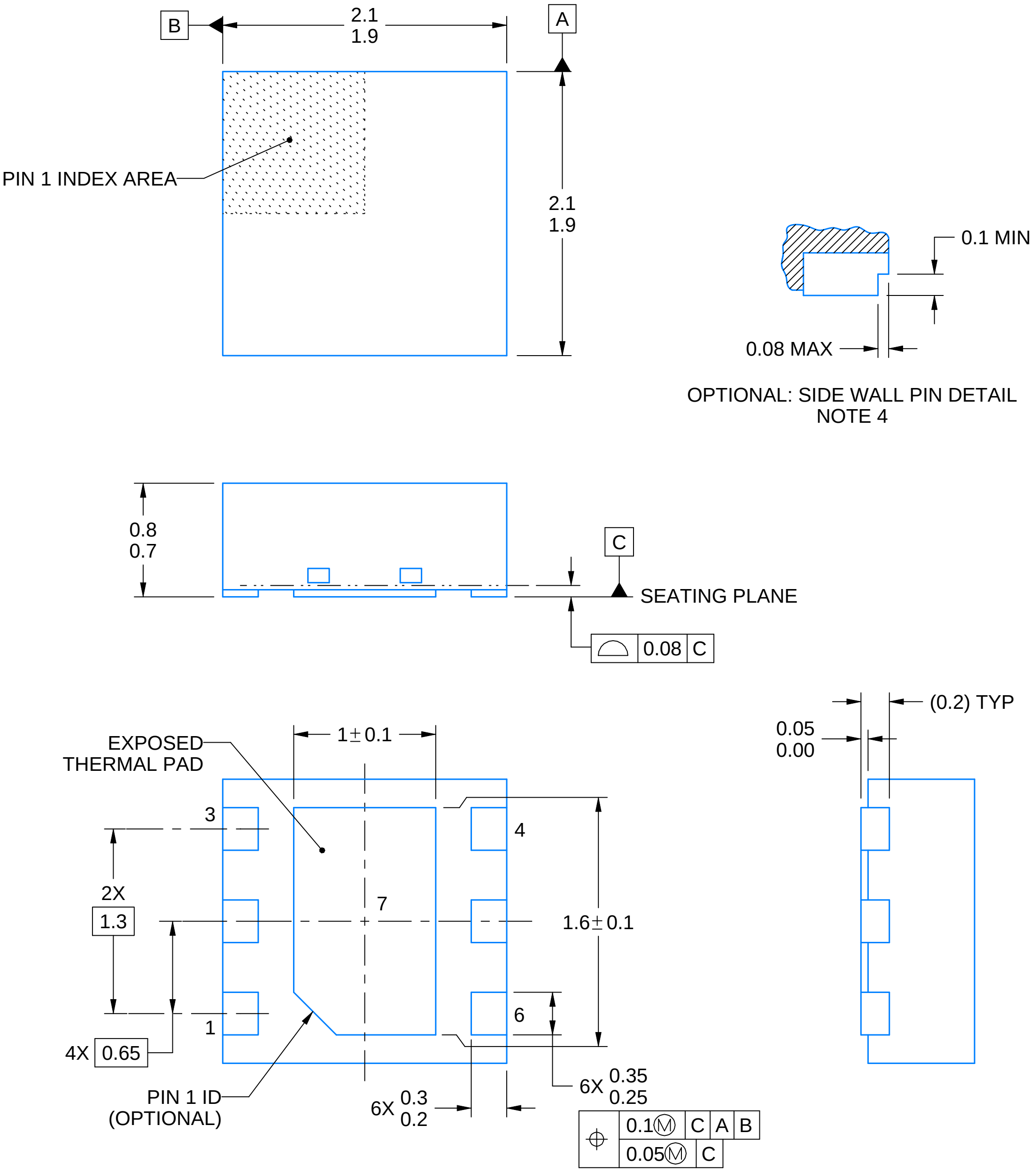
DRV 6

WSON - 0.8 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



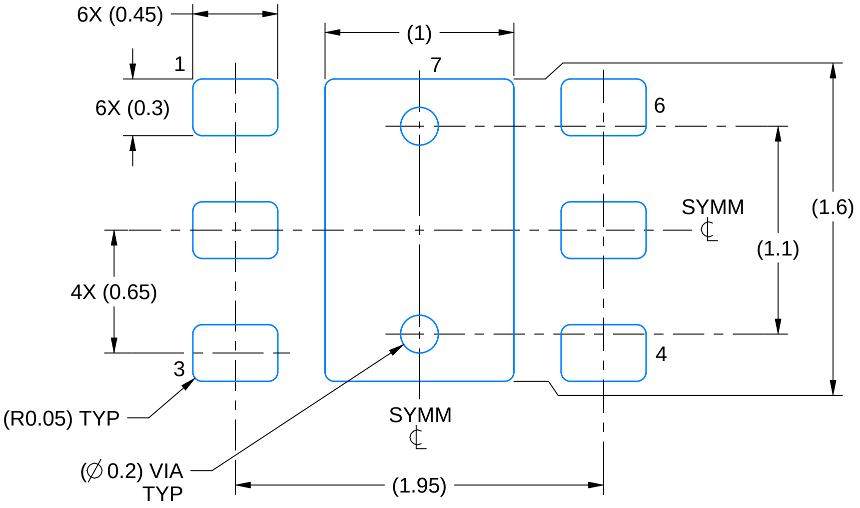
Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



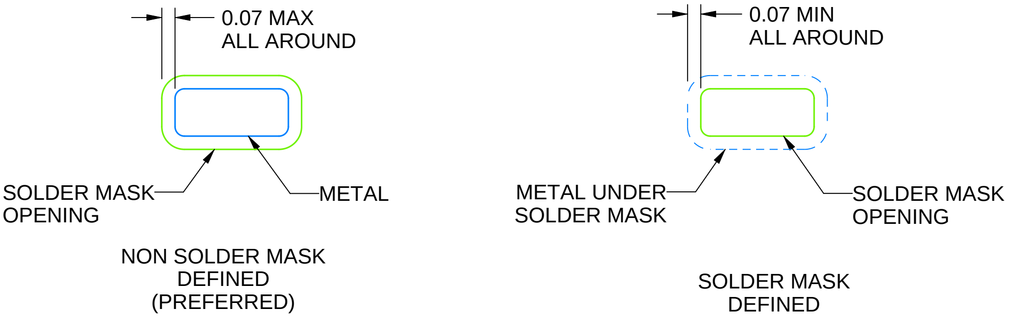
4222173/C 11/2025

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.
4. Minimum 0.1 mm solder wetting on pin side wall. Available for wettable flank version only.



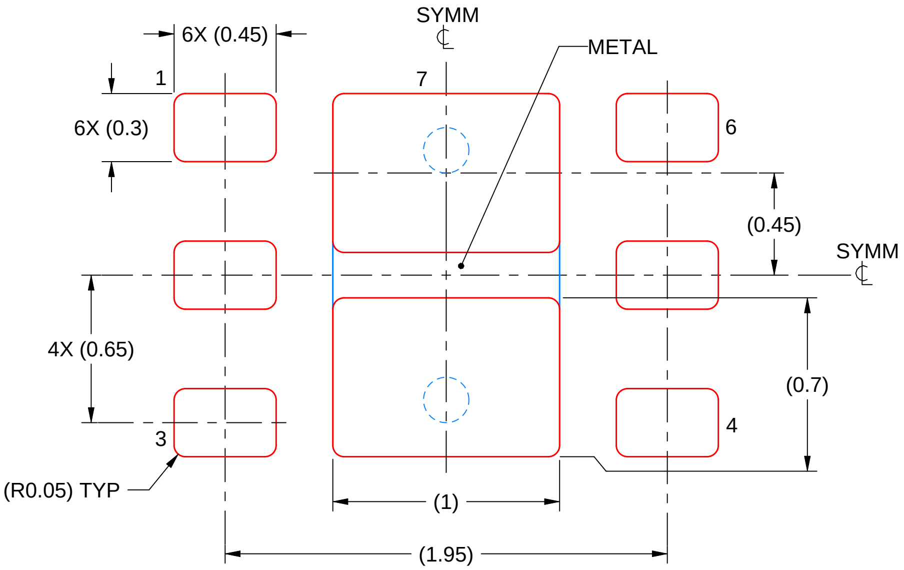
LAND PATTERN EXAMPLE
SCALE:25X



SOLDER MASK DETAILS

NOTES: (continued)

5. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
6. Vias are optional depending on application, refer to device data sheet. If some or all are implemented, recommended via locations are shown.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD #7
88% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:30X

NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATASHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES “AS IS” AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, regulatory or other requirements.

These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you fully indemnify TI and its representatives against any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI’s products are provided subject to TI’s Terms of Sale, TI’s General Quality Guidelines, or other applicable terms available either on ti.com or provided in conjunction with such TI products. TI’s provision of these resources does not expand or otherwise alter TI’s applicable warranties or warranty disclaimers for TI products. Unless TI explicitly designates a product as custom or customer-specified, TI products are standard, catalog, general purpose devices.

TI objects to and rejects any additional or different terms you may propose.

Copyright © 2026, Texas Instruments Incorporated

Last updated 10/2025