TPS7H1301-SP 3V to 6.3V Input, 400mA, -6V to -0.6V Radiation-Hardend Charge Pump Voltage Inverter with Integrated Low Dropout Regulator

ADVANCE INFORMATION

1 Features

- Total ionizing dose (TID) characterized
  - Radiation hardness assurance (RHA) availability of up to 100krad(Si)
- Single-event effects (SEE) characterized
  - Single-event latchup (SEL), single-event burnout (SEB), and single-event gate rupture (SEGR) immune up to linear energy transfer (LET) = 75MeV·cm^2 /mg
  - Single-event functional interrupt (SEFI) and single-event transient (SET) characterized up to LET = 75MeV·cm^2 /mg
- Inverts a positive input voltage and regulates the negative supply
- Up to 400mA output current
- 2.5Ω (typical) inverter output impedance, V_{IN} = 5V
- ±1.5% regulation output accuracy
- 500kHz (typical) fixed-frequency, adjustable negative output voltage operation (TPS7H1301)
- 1MHz (typical) fixed frequency, fixed -1.8V output (TPS7H1302)
- 45dB (typical) LDO PSRR at 100kHz with 100mA load current
- Plastic packages outgas tested per ASTM E595
- Available in military (–55°C to 125°C) temp range

2 Applications

- Satellite electrical power systems (EPS)
- Command and data handling (C&DH)
- Optical imaging payload
- Radar imaging payload
- Power for analog circuits
  - Data converters: ADCs and DACs (analog-to-digital and digital-to-analog converters)
  - Op amps (operational amplifiers)
  - Imaging sensors

3 Description

The TPS7H1301SP, -SEP (TPS7H1301) and TPS7H1302SP, -SEP (TPS7H1302) are charge pump positive-to-negative voltage inverters with an integrated negative low-dropout regulator (LDO). Both devices accept a positive input supply voltage range of 3V to 6.3V and deliver up to 400mA of output current, with integrated enable and power-good functionality.

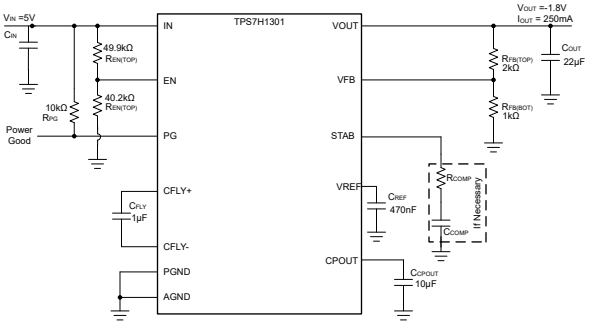
The TPS7H1301 features a 500kHz (typical) charge pump switching frequency and provides adjustable output voltage regulation. Its STAB pin enables direct access to the negative LDO error amplifier for external compensation, offering design flexibility for optimized transient response.

The TPS7H1302 delivers a fixed -1.8V output voltage with a 1MHz (typical) charge pump switching frequency. By eliminating the need for external feedback resistors, the TPS7H1302 reduces both external component count and overall solution size.

Package Information

PART NUMBER (1)	GRADE	PACKAGE (2)
5962R2421501VXC (4)	QMLV-RHA	14-pin ceramic 8.03mm × 9.12mm Mass = 1.22g
5962R2421502VXC (3)		
TPS7H1301HBL/EM (4)	Engineering Sample	
TPS7H1302HBL/EM (3)		
5962R2421501PYE (3)	QMLP-RHA	28-pin plastic 4.40mm × 9.70mm Mass = 198mg
5962R2421502PYE (3)		
TPS7H1301MPWPTSEP (3)	SEP	
TPS7H1302MPWPTSEP (3)		

(1) For additional information view the Device Options Table
(2) Dimension and mass values are nominal.
(3) Product preview.
(4) Advanced information



Typical Application Circuit TPS7H1301

ADVANCE INFORMATION

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4 Device Options Table

Generic Part Number	Radiation Rating [1]	Grade	Package	Orderable Part Number
TPS7H1301SP	TID characterization up to 100 krad(Si) and DSEE free up to LET = 75 MeV·cm^2 /mg	QMLV-RHA	14-pin ceramic flat pack (CFP) HBL	5962R2421501VXC [4]
		QMLP-RHA	28-pin plastic HTSSOP (PWP)	5962R2421501PYE [3]
	None	Engineering Sample [2]	14-pin ceramic flat pack (CFP) HBL	TPS7H1301HBL/EM [4]
TPS7H1302SP	TID characterization up to 100 krad(Si) and DSEE free up to LET = 75 MeV·cm^2 /mg	QMLV-RHA	14-pin ceramic flat pack (CFP) HBL	5962R2421502VXC [3]
		QMLP-RHA	28-pin plastic HTSSOP (PWP)	5962R2421502PYE [3]
	None	Engineering Sample [2]	14-pin ceramic flat pack (CFP) HBL	TPS7H1302HBL/EM [3]
TPS7H1301-SEP	TID of 50krad(Si) RLAT, DSEE free to 43MeV·cm^2 /mg	Space Enhanced Plastic	28-pin plastic HTSSOP (PWP)	TPS7H1301PWPTSEP [3]
TPS7H1302-SEP	TID of 50krad(Si) RLAT, DSEE free to 43MeV·cm^2 /mg	Space Enhanced Plastic	28-pin plastic HTSSOP (PWP)	TPS7H1302PWPTSEP [3]

(1) TID is total ionizing dose and DSEE is destructive single event effects. Additional information is available in the associated TID reports and SEE reports for each product.
(2) These units are intended for engineering evaluation only. The units are processed to a non-compliant flow (such as no burn-in and only 25°C testing). These units are not designed for qualification, production, radiation testing, or flight use. Parts are not warranted as to performance over temperature or operating life.
(3) Product preview
(4) Advanced information

ADVANCE INFORMATION

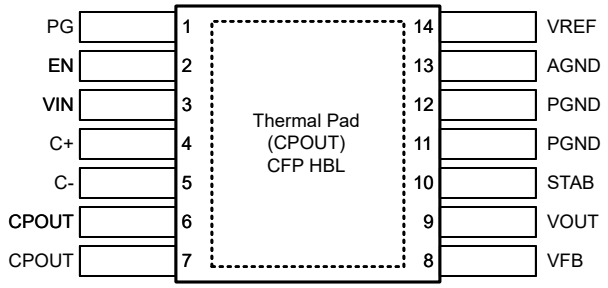
5 Device Comparison Table

Generic Part Number	Charge Pump F_{SW}	Output Voltage Range	External Compensation
TPS7H1301	500kHz	-6V to -0.6V	Yes
TPS7H1302	1000kHz	-1.8V (fixed)	No

6 Pin Configuration and Functions

TPS7H1301

HBL Package
14-pin CFP
Top View



PWP Package
28-pin HTSSOP
Top View

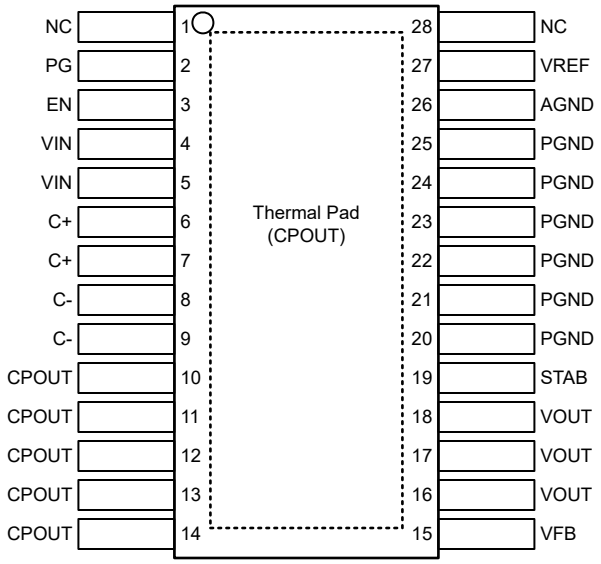


Table 6-1. Pin Functions

PIN			TYPE[1]	DESCRIPTION
NAME	HBL (14) No.	PWP (28) No.		
PG	1	2	O	Power good indicator. The PG pin is connected to the drain terminal of an internal MOSFET that pulls the applied external voltage to GND when criteria for power good indication is not satisfied. Use a pull-up resistor to pull this pin up to VIN or the desired logic level. It is recommended to pull down PG to ground; if unused the PG pin can be leaft floating.
EN	2	3	I	Enable. Driving this pin to logic high enables the device; driving the pin to logic low disables the device. If enable functionality is not required, connect this pin to VIN. Do not float this pin.
VIN	3	4,5	P	Positive power supply input; connect a 10µF low-ESR ceramic capacitor to VIN and PGND.
C+	4	6,7	P	Positive terminal for flying capacitor, connect a 1µF low-ESR ceramic capacitor to C+ and C-. Capacitance values smaller than 1µF increase charge pump output ripple; higher fly capacitor values cause excessive inrush current.
C-	5	8,9	P	Negative terminal for flying capacitor.
CPOUT	6,7	10 to 14	P	Negative unregulated charge pump output voltage. Connect a 10µF low-ESR ceramic capacitor to CPOUT and PGND.
VREF	14	27	O	Reference pin, outputs a nominal -0.6V. Connect a 470nF ceramic capacitor between VREF and AGND.
AGND	13	26	P	Analog ground (0V) connection.
PGND	11, 12	21 to 26	P	Power ground (0V) connection for charge pump.
STAB	10	20	O	The STAB pin is directly connected to the output from the internal OTA (operational transconductance) error amplifier to aid in measuring or optimizing the control loop. Standard compensation networks can be applied to the STAB (see Section 10.2.2.5); however, an output capacitance of 22µF typically achieve high stability margins, without the need for an external compensation network.

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Table 6-1. Pin Functions (continued)

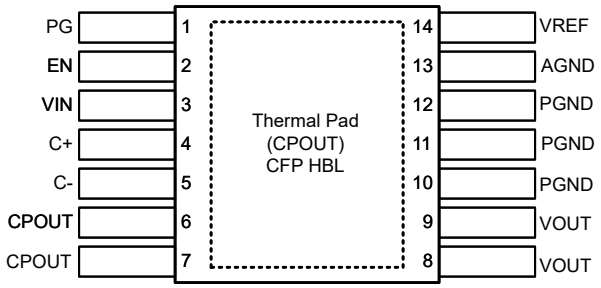
PIN			TYPE(1)	DESCRIPTION
NAME	HBL (14) No.	PWP (28) No.		
VOUT	9	16 to 19	P	Output power pin. The regulated output voltage. A single 22µF ceramic capacitor is recommended. Capacitance values between 10µF and 100µF are generally supported; depending on output capacitor, input voltage, output voltage setting and load current, use of the STAB pin can further improve stability performance.
VFB	8	15		The output voltage feedback input through voltage dividers. See Section 9.3.5 for guidance on how to adjust the output of the LDO.
NC	N/A	1, 28	—	No connect. These pins are not internally connected. It is recommended to connect these pins to PGND to prevent charge buildup; however, these pins can also be left open or tied to any voltage between CPOUT and V_{IN}
Thermal pad	—		—	Low electrical impedance path to CPOUT. It is recommended to connect this metal thermal pad to a large plane for effective heat dissipation. Note: this pad is driven to the CPOUT voltage, not PGND.
Metal lid	Lid	N/A	—	The lid is internally connected to the thermal pad and CPOUT through the seal ring.

(1) I = Input, O = Output, I/O = Input or Output, - = Other

ADVANCE INFORMATION

TPS7H1302

HBL Package
14-pin CFP
Top View



PWP Package
28-pin HTSSOP
Top View

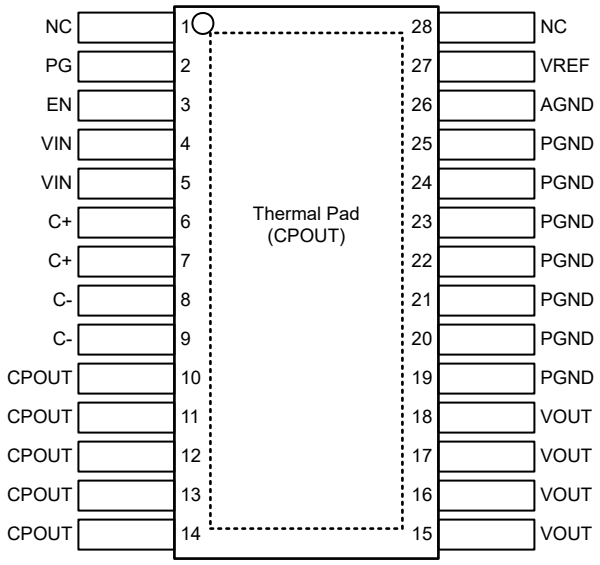


Table 6-2. Pin Functions

PIN			TYPE[1]	DESCRIPTION
NAME	HBL (14) No.	PWP (28) No.		
PG	1	2	O	Power good indicator. The PG pin is connected to the drain terminal of an internal MOSFET that pulls the applied external voltage to GND when criteria for power good indication is not satisfied. Use a pull-up resistor to pull this pin up to VIN or the desired logic level. It is recommended to pull down PG to ground; if unused the PG pin can be leaft floating.
EN	2	3	I	Enable. Driving this pin to logic high enables the device; driving the pin to logic low disables the device. If enable functionality is not required, connect this pin to VIN. Do not float this pin.
VIN	3	4,5	P	Positive power supply input.
C+	4	6,7	P	Positive terminal for flying capacitor.
C-	5	8,9	P	Negative terminal for flying capacitor.
CPOUT	6,7	10 to 14	P	Negative unregulated output voltage.
VREF	14	27	O	Reference pin, outputs a nominal -0.6V. Connect a 470nF ceramic capacitor.
AGND	13	26	P	Analog ground (0V) connection.
PGND	10 to 12	19 to 25	P	Power ground (0V) connection for charge pump.
VOUT	8, 9	15 to 18	P	Output power pin. The regulated output voltage. A single 22µF ceramic capacitor is recommended. Capacitance values between 10µF and 100µF are generally supported.
NC	N/A	1, 28	—	No connect. This pin is not internally connected. It is recommended to connect these pins to PGND to prevent charge buildup; however, these pins can also be left open or tied to any voltage between CPOUT and V_{IN}
Thermal pad	—		—	Internally connected to CPOUT. It is recommended to connect this metal thermal pad to a large plane for effective heat dissipation. Note: this pad is driven to the CPOUT voltage, not PGND.
Metal lid	Lid	N/A	—	The lid is internally connected to the thermal pad and CPOUT through the seal ring.

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7 Specifications

7.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
Input Voltage	IN	–0.3	7.5	V
	EN	–0.3	7.5	
	PG	–0.3	7.5	
Output Voltage	VREF	–3.6	0.3	V
	FB (TPS7H1301 only)	CPOUT	0.3	
	STAB (TPS7H1301 only)	CPOUT	CPOUT +7.5	
	C1+	GND-0.3	VIN	
	C1-	CPOUT	GND+0.3	
	CPOUT	–6.8	0.3	
	OUT	–6.8	0.3	
Input Current	IN	0	600	mA
Output Current	OUT	0	600	mA
T_{STG}	Storage temperature	–65	150	°C
T_J	Junction temperature	–55	150	°C

(1) Operation outside the Absolute Maximum Ratings may cause permanent device damage. Absolute Maximum Ratings do not imply functional operation of the device at these or any other conditions beyond those listed under Recommended Operating Conditions. If used outside the Recommended Operating Conditions but within the Absolute Maximum Ratings, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.

7.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001 (1)	±1000	V
		Charged-device model (CDM), per ANSI/ESDA/JEDEC JS-002 (2)	±500	

(1) JEDEC document JEP155 states that 500V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250V CDM allows safe manufacturing with a standard ESD control process.

7.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
Input Voltage	IN	3		6.3	V
	EN	0		7	V
	PG	0		7	V
Output Voltage	OUT (TPS7H1301)	–6		–0.6	V
	CPOUT(1)	–6.3		-2	V
	OUT (TPS7H1302)		-1.8		V
I_{OUT}	Output Current	0		400	mA
T_J	Junction temperature	–55		125	°C

(1) Selection of capacitors for CFLY and CPOUT affect overall charge pump resistance, voltage droop, and overall voltage present on CPOUT; see the Application Section for droop voltage calculation equation.

7.4 Thermal Information

THERMAL METRIC(1)		TPS7H1301-SP TPS7H1302-SP	TPS7H1301-SP, SEP TPS7H1302-SP, SEP	UNIT
		CFP HBL	PWP (HTSSOP)	
		14	28	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	25.1	24.4	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	6.3	15.8	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	9.3	6.4	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	1.4	0.2	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	9.1	6.4	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	0.5	0.7	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application note.

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7.5 Electrical Characteristics

Over 3V ≤ V_{IN} ≤ 6.3V, $V_{OUT\ (set)}$ = -1.8, I_{OUT} = 10mA, C_{REF} = 47nF, over operating temperature range (T_A = -55℃ to 125℃), typical values are at T_A = 25℃, unless otherwise noted; includes RLAT at T_A = 25℃ if sub-group number is present for QML RHA and SEP devices[4].

PARAMETER		TEST CONDITIONS		Subgroup	MIN	TYP	MAX	UNIT
POWER SUPPLIES and CURRENTS								
I_Q	Quiescent Current	T{S7H1301 IOUT = 0A, V_{EN} = 7V		1, 2, 3		15	45	mA
		TPS7H1302 IOUT = 0A, V_{EN} = 7V		1, 2, 3		12	45	
I_{SHDN}	Shutdown Current	V_{EN} = 0V, I_{OUT} = 0A		1, 2, 3		0.8	1.5	mA
I_{FB}	Feedback leakage current	TPS7H1301 V_{FB} = -0.7V		1, 2, 3		25	100	nA
ENABLE								
$V_{EN(rising)}$	Enable rising threshold (turn-on)			1, 2, 3	0.57	0.6	0.625	V
$V_{EN(falling)}$	Enable falling threshold (turn-off)			1, 2, 3	0.445	0.5	0.555	V
$t_{EN(delay)}$	EN propagation delay	EN high to PG high at VIN = 5V VIN = -1.8V		1, 2, 3		14	18	ms
$I_{EN(LKG)}$	Enable leakage current	V_{EN} = 7V		1, 2, 3		25	100	nA
$T_{SD(enter)}$	Thermal shutdown enter temperature					160		℃
$T_{SD(exit)}$	Thermal shutdown exit temperature					130		℃
POWER GOOD								
$V_{PG(rise)}$	Power good rising threshold as a percent of V_{OUT}	Slew rate V_{OUT} = 10V/s		1, 2, 3	92%	95%	98%	
$V_{PG(fall)}$	Power good falling threshold as a percent of V_{OUT}	Slew rate V_{OUT} = 10V/s		1, 2, 3	87%	90%	93%	
$V_{PG(OL)}$	Power good output low	$I_{PG(SINK)}$ = 2mA		1, 2, 3		90	190	mV
$V_{IN(MIN\_PG)}$	Minimum V_{IN} for valid PG (V_{PG} = 0.5V)	$I_{PG(sink)}$ = 0.5mA		1, 2, 3		0.8	1	V
$I_{PG(LKG)}$	Power good leakage	TPS7H1301 V_{PG} = 7V, V_{FB} = –0.7V		1, 2, 3		0.05	2	µA
CHARGE PUMP								
$R_{DISCHARGE}$	CPOUT discharge resistance	C_{CPOUT} = 10µF	V_{CPOUT} = –0.3V			75		Ω
$t_{DISCHARGE}$	CPOUT discharge time (CPOUT = –0.3V) to GND	C_{CPOUT} = 10µF				6.5		ms
f_{SW}	Switching frequency (TPS7H1301)[1]			9, 10, 11	400	500	600	kHz
f_{SW}	Switching frequency (TPS7H1302)[2]			9, 10, 11	800	1000	1200	kHz
$f_{SW(FB)}$	Foldback frequency switching frequency (1301)					125		kHz
$f_{SW(FB)}$	Foldback frequency switching frequency (1302)					250		kHz
$R_{DS(ON)}$	Switch array MOSFET1 drain source resistance	I_{RDSON} = 100mA V_{IN} = 5V	T_A = 125℃	2		355	385	mΩ
			T_A = 25℃	1		265	295	
			T_A = -55℃	3		235	265	

7.5 Electrical Characteristics (continued)

Over 3V ≤ V_{IN} ≤ 6.3V, $V_{OUT\ (set)}$ = -1.8, I_{OUT} = 10mA, C_{REF} = 47nF, over operating temperature range (T_A = -55℃ to 125℃), typical values are at T_A = 25℃, unless otherwise noted; includes RLAT at T_A = 25℃ if sub-group number is present for QML RHA and SEP devices[4].

PARAMETER		TEST CONDITIONS		Subgroup	MIN	TYP	MAX	UNIT
$R_{CP(OUT)}$	Output resistance to CPOUT (TPS7H1301)[1]	I_L = 150mA	V_{IN} = 3V			4.5		Ω
		I_L = 250mA	V_{IN} = 5V			3.5		
			V_{IN} = 6.3V			3.1		
$R_{CP(OUT)}$	Output resistance to CPOUT (TPS7H1302)[2]	I_L = 150mA	V_{IN} = 3V			4.8		Ω
		I_L = 250mA	V_{IN} = 5V			3.7		
			V_{IN} = 6.3V			3.3		
V_{DROOP}	Droop Voltage V_{DROOP} = VIN - $\|V_{CPOUT}\|$ (TPS7H1301)[1]	V_{IN} = 3V	I_{OUT} = 10mA			135		mV
			I_{OUT} = 250mA			1260		
		V_{IN} = 5V	I_{OUT} = 10mA			105		
			I_{OUT} = 400mA			1400		
		V_{IN} = 6.3V	I_{OUT} = 10mA			93		
			I_{OUT} = 400mA			1240		
V_{DROOP}	Droop Voltage V_{DROOP} = VIN - $\|V_{CPOUT}\|$ (TPS7H1302)[2]	V_{IN} = 3V	I_{OUT} = 10mA			144		mV
			I_{OUT} = 250mA			1344		
		V_{IN} = 5V	I_{OUT} = 10mA			111		
			I_{OUT} = 400mA			1591		
		V_{IN} = 6.3V	I_{OUT} = 10mA			100		
			I_{OUT} = 400mA			1420		
DROPOUT								
I_{DO}	Dropout current (TPS7H1301)[3]	$V_{OUT(set)}$ = –1.8V, $I_{OUT(meas.)}$ = 98% × $V_{OUT(NOM)}$	V_{IN} = 3V	1, 2, 3	75	125		mA
			V_{IN} = 3.3V	1, 2, 3	100	150		
			V_{IN} = 4V	1, 2, 3	200	300		
			V_{IN} = 5V	1, 2, 3	400			
			V_{IN} = 6V	1, 2, 3	400			
		$V_{OUT(set)}$ = –5V, $I_{OUT(meas.)}$ = 98% × $V_{OUT(NOM)}$	V_{IN} = 5.5V	1, 2, 3	40	50		
			V_{IN} = 6V	1, 2, 3	250	300		
	Dropout current (TPS7H1302)[3]	$V_{OUT(set)}$ = –1.8V, $I_{OUT(meas.)}$ = 98% × $V_{OUT(NOM)}$	V_{IN} = 5.5V	1, 2, 3	40	50		
			V_{IN} = 6V	1, 2, 3	250	300		
ACCURACY								
V_{ACC}	Output voltage accuracy	–5V ≤ V_{OUT} ≤ $V_{CP(OUT)}$ - V_{DO}, 1mA ≤ I_{OUT} ≤ 400mA		1, 2, 3	–1.5%		1.5%	
$\Delta V_{OUT}/\Delta V_{IN}$	Line regulation	3.3V ≤ V_{IN} ≤ 6.3V	ΔV = 3V, I_{OUT} = 150mA	1, 2, 3		100	1300	µV/V
$\Delta V_{OUT}/\Delta I_{OUT}$	Load regulation (1301)	10mA ≤ I_{OUT} ≤400mA, V_{IN} = 5V, V_{OUT} = -1.8V		1, 2, 3		8	35	mV/A
	Load regulation (1302)	10mA ≤ I_{OUT} ≤400mA, V_{IN} = 5V, V_{OUT} = -1.8V	10mA ≤ I_{OUT} ≤400mA, V_{IN} = 5V, V_{OUT} = -1.8V	1, 2, 3		24	70	mV/A
V_{REF}	Internal reference voltage			1, 2, 3	–0.606	–0.6	–0.594	V

ADVANCE INFORMATION

7.5 Electrical Characteristics (continued)

Over 3V ≤ V_{IN} ≤ 6.3V, $V_{OUT\ (set)}$ = -1.8, I_{OUT} = 10mA, C_{REF} = 47nF, over operating temperature range (T_A = -55℃ to 125℃), typical values are at T_A = 25℃, unless otherwise noted; includes RLAT at T_A = 25℃ if sub-group number is present for QML RHA and SEP devices(4).

PARAMETER		TEST CONDITIONS		Subgroup	MIN	TYP	MAX	UNIT
RIPPLE, NOISE AND PSRR								
$PSRR_{LDO}$	LDO power-supply rejection ratio	V_{CPOUT} = –5V, V_{OUT} = –1.8V, I_{OUT} = 250mA	f_{ripple} = 100Hz			60		dB
			f_{ripple} = 1kHz			58		dB
			f_{ripple} = 10kHz			47		dB
			f_{ripple} = 100kHz			45		dB
			f_{ripple} = 500kHz			26		dB
			f_{ripple} = 1MHz			26		dB
$V_{RIP(CP)}$	Voltage ripple at charge pump (BW < 2Mhz)	I_{OUT} = 400mA V_{CPOUT} = -5V V_{OUT} = -1.8V				32		mV_{PP}
$V_{RIP(OUT)}$	Voltage ripple at device output (BW < 2Mhz)	I_{OUT} = 400mA V_{CPOUT} = -5V V_{OUT} = -1.8V				3		mV_{PP}
V_{N_OUT}	Output noise voltage (bandwidth from 10Hz to 100kHz)	V_{CPOUT}= –5V, V_{OUT} = –1.8V, I_{OUT} = 250mA				20		μV_{RMS}

(1) C_{FLY} = 1µF, C_{CPOUT} = 10µF, C_{OUT} = 22µF
(2) C_{FLY} = 0.47µF, C_{CPOUT} = 4.7µF, C_{OUT} = 22µF
(3) See Parameter Measurement Information
(4) See the 5962R2421501 SMD for additional information on the QML RHA devices and see the VID for additional information on the SEP devices.

ADVANCE INFORMATION

7.6 Quality Conformance Inspection

MIL-STD-883, Method 5005 - Group A

SUBGROUP	DESCRIPTION	TEMP (°C)
1	Static tests at	25
2	Static tests at	125
3	Static tests at	–55
4	Dynamic tests at	25
5	Dynamic tests at	125
6	Dynamic tests at	–55
7	Functional tests at	25
8A	Functional tests at	125
8B	Functional tests at	–55
9	Switching tests at	25
10	Switching tests at	125
11	Switching tests at	–55

ADVANCE INFORMATION

7.7 Typical Characteristics

V_{IN} = 5V, V_{OUT} = -1.8V, T_A= 25ºC ,C_{REF} = 470nF, C_{FLY} = 1µF, C_{CPOUT} = 10µF and C_{OUT} = 22µF, no R_{COMP}, no C_{COMP} unless otherwise noted.

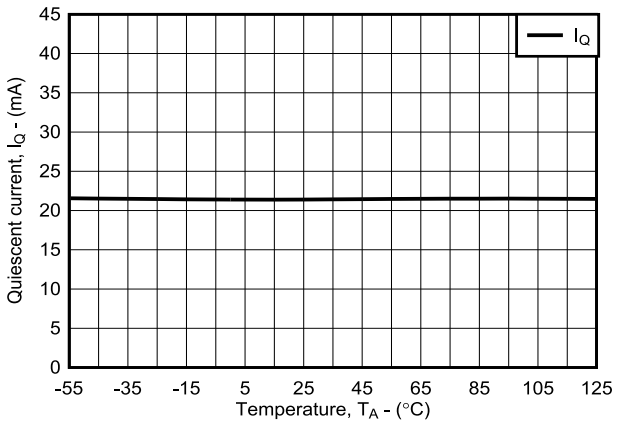


Figure 7-1. Quiescent Current vs. Temperature

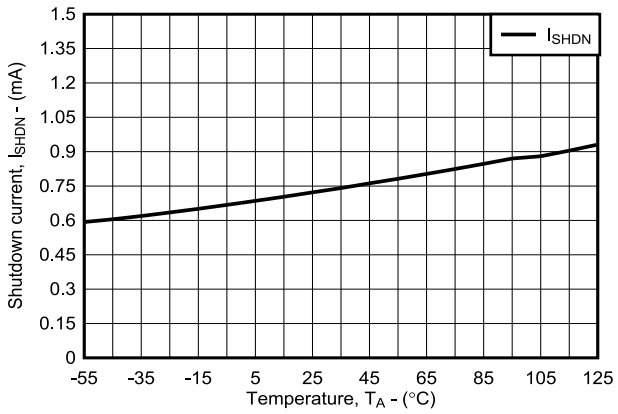


Figure 7-2. Shutdown Current vs. Temperature

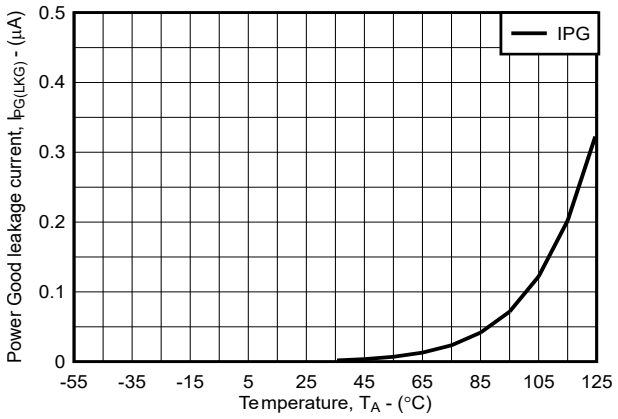


Figure 7-3. Power Good Input Leakage Current vs. Temperature

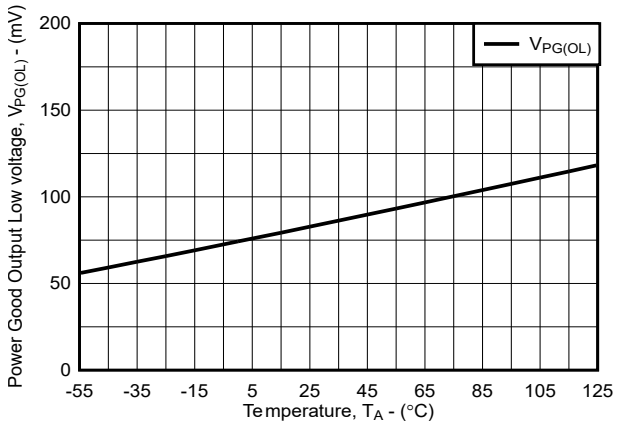


Figure 7-4. Power Good Output Low vs. Temperature

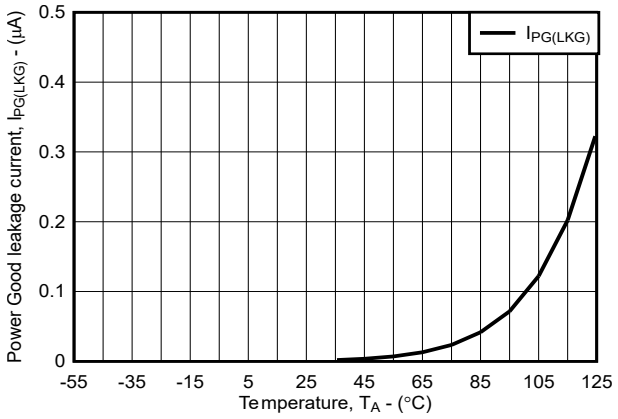


Figure 7-5. Enable Leakage vs Current

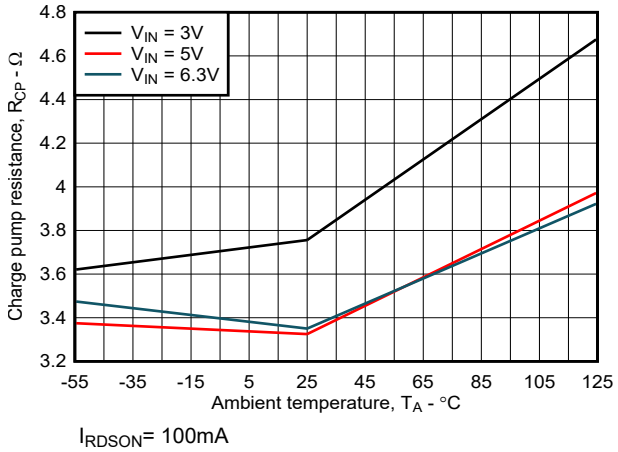
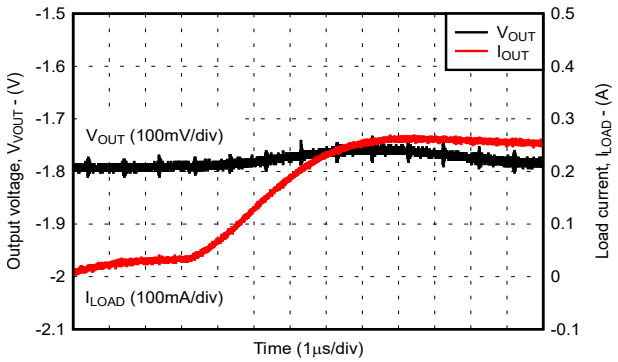


Figure 7-6. Charge pump resistance, R_{CP} vs Temperature

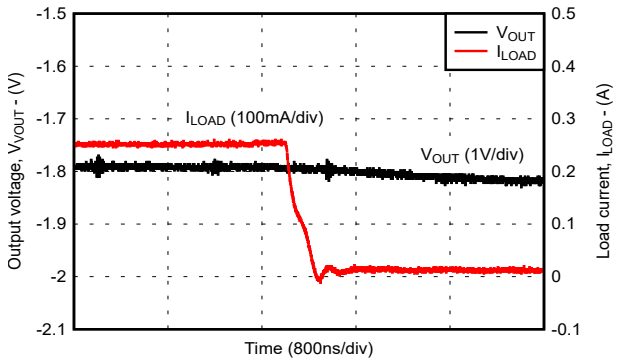
7.7 Typical Characteristics (continued)

V_{IN} = 5V, V_{OUT} = -1.8V, T_A= 25ºC ,C_{REF} = 470nF, C_{FLY} = 1µF, C_{CPOUT} = 10µF and C_{OUT} = 22µF, no R_{COMP}, no C_{COMP} unless otherwise noted.



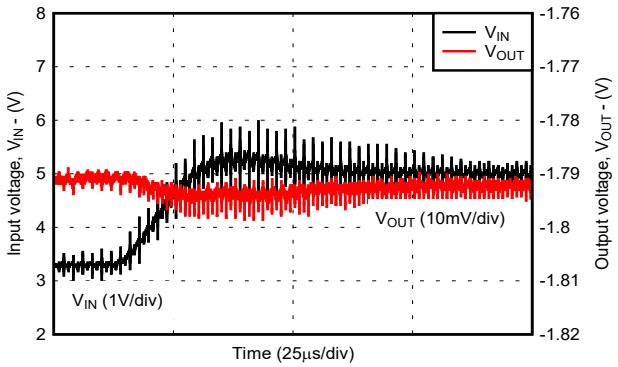
Slew Rate = 1A/µs

Figure 7-7. Load Step Rising



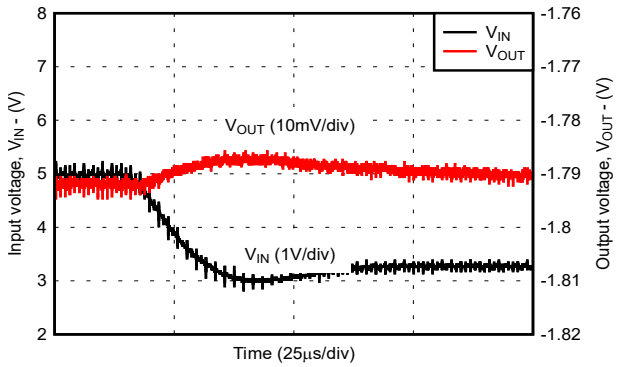
Slew Rate = 1A/µs

Figure 7-8. Load Step Falling



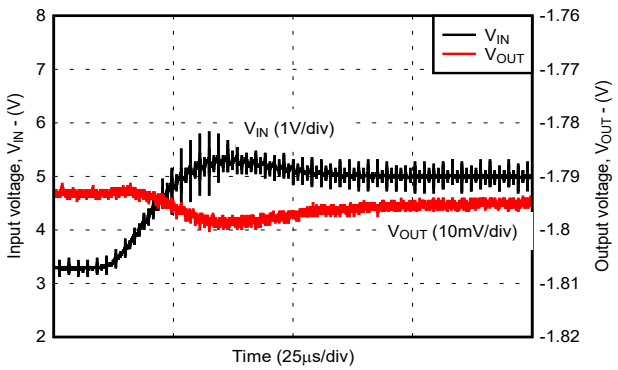
Slew Rate = 10V/ms I_{LOAD}=250mA

Figure 7-9. Line Step Rising



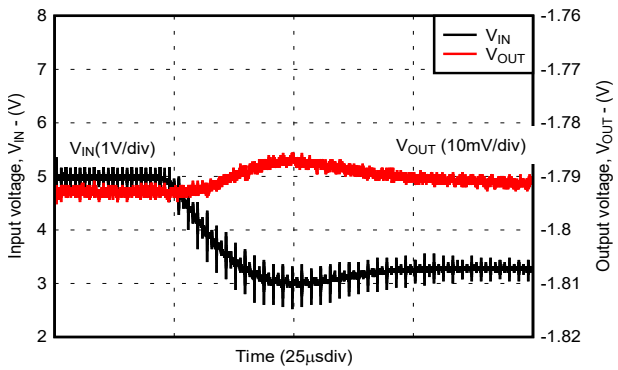
Slew Rate = 10V/ms I_{LOAD}=250mA

Figure 7-10. Line Step Falling



Slew Rate = 10V/ms I_{LOAD}=10mA

Figure 7-11. Line Step Rising



Slew Rate = 10V/ms I_{LOAD}=10mA

Figure 7-12. Line Step Falling

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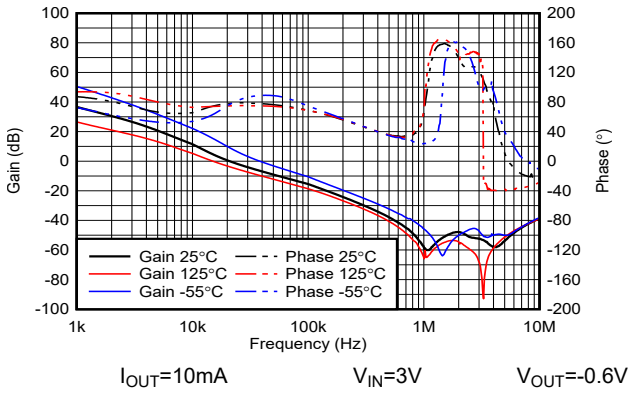
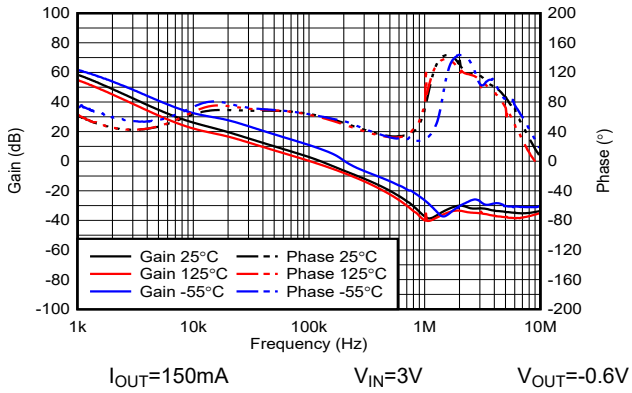
7.7 Typical Characteristics (continued)

V_{IN} = 5V, V_{OUT} = -1.8V, T_A= 25ºC ,C_{REF} = 470nF, C_{FLY} = 1µF, C_{CPOUT} = 10µF and C_{OUT} = 22µF, no R_{COMP}, no C_{COMP} unless otherwise noted.



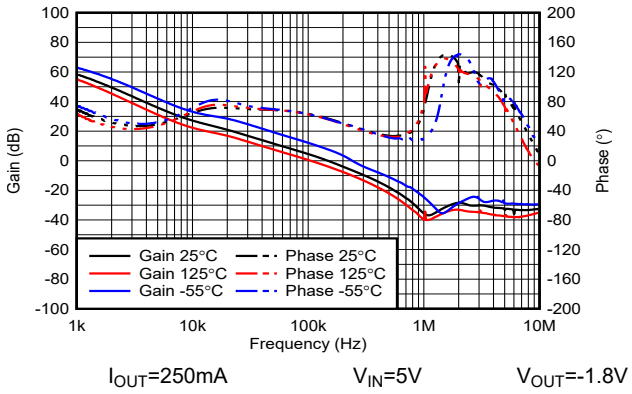
I_{OUT}=10mA V_{IN}=3V V_{OUT}=-0.6V

Figure 7-13. Gain and Phase vs Frequency (Bode)



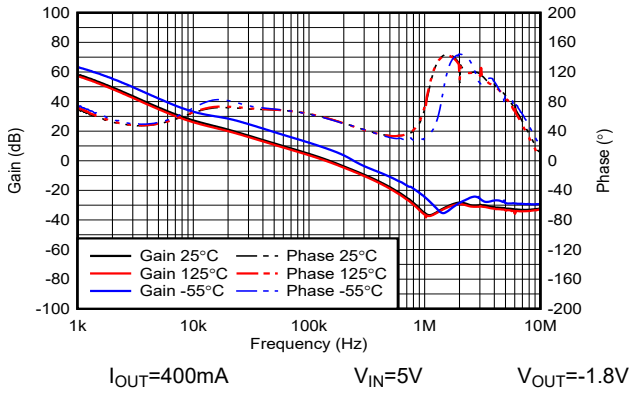
I_{OUT}=150mA V_{IN}=3V V_{OUT}=-0.6V

Figure 7-14. Gain and Phase vs Frequency (Bode)



I_{OUT}=250mA V_{IN}=5V V_{OUT}=-1.8V

Figure 7-15. Gain and Phase vs Frequency (Bode)



I_{OUT}=400mA V_{IN}=5V V_{OUT}=-1.8V

Figure 7-16. Gain and Phase vs Frequency (Bode)

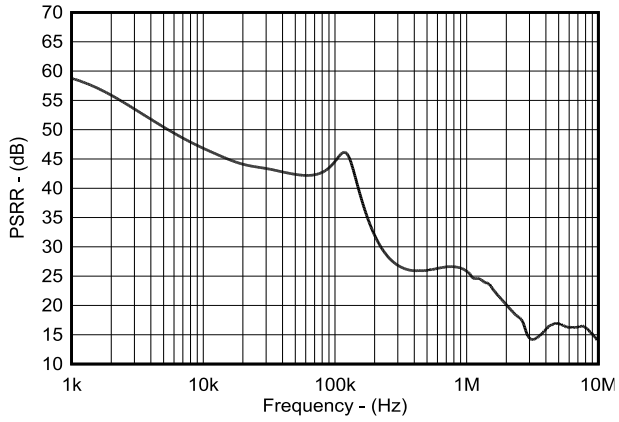
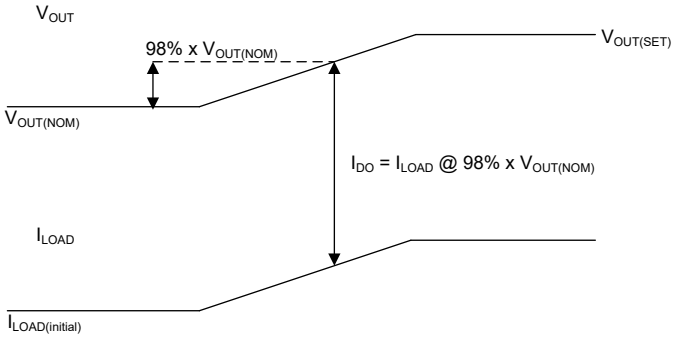


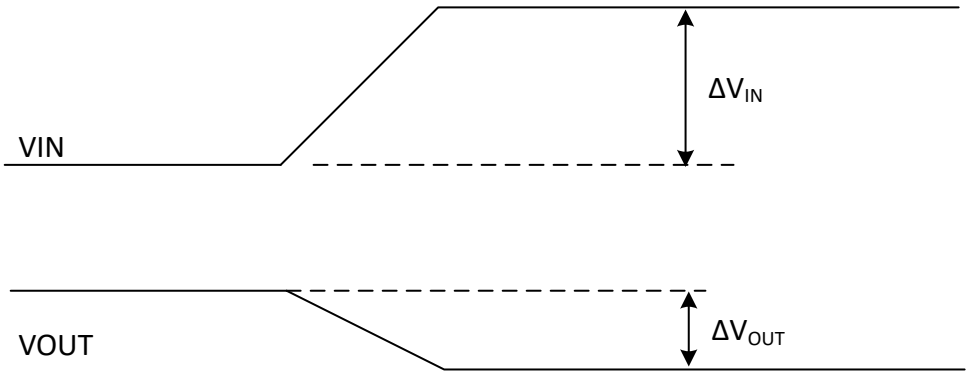
Figure 7-17. PSRR vs Frequency

8 Parameter Measurement Information



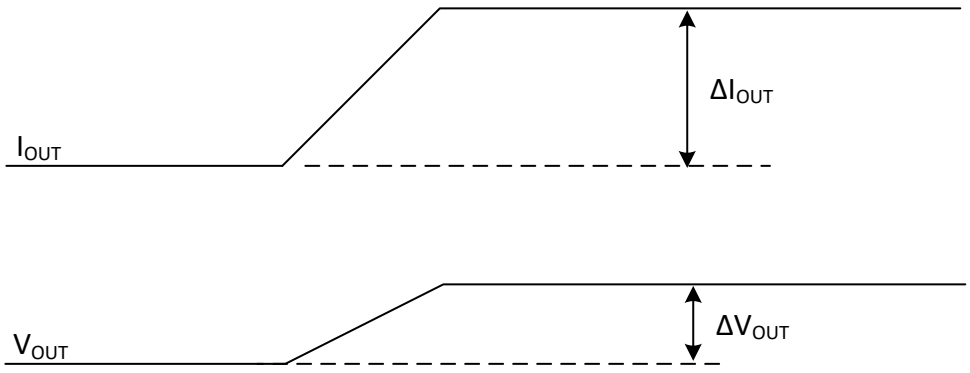
A. $V_{OUT(SET)}$ is the output voltage the regulator is configured using the feedback resistors, $V_{OUT(NOM)}$ is the measured output voltage. I_{load} is the load current applied on V_{OUT}. When V_{OUT} falls to 98% of the nominal value ($V_{OUT(NOM)}$), the dropout current is recorded.

Figure 8-1. Dropout Current Measurement



A. Line regulation ΔV_{OUT} / ΔV_{IN} = 100µV/V (typ). For example a 1V change in V_{IN} (ΔV_{IN} = 1V), results in a 100µV change in V_{OUT} (ΔV_{OUT} = 100µV). Line regulation is a DC parameter; therefore this waveform can only be considered valid after transients die out or for a slow V_{IN} slew rate.

Figure 8-2. Line Regulation Measurement



A. Load regulation: ΔV_{OUT} / ΔI_{OUT} = 0.4mV/A (typ). For example a 100mA change in I_{OUT} (ΔI_{OUT} = 100mA), results in a 0.4mV change in V_{OUT} (ΔV_{OUT} = 0.4mV). Load regulation is a DC parameter; therefore this waveform can be considered valid after transients die out or for a slow I_{OUT} slew rate.

Figure 8-3. Load Regulation Measurement

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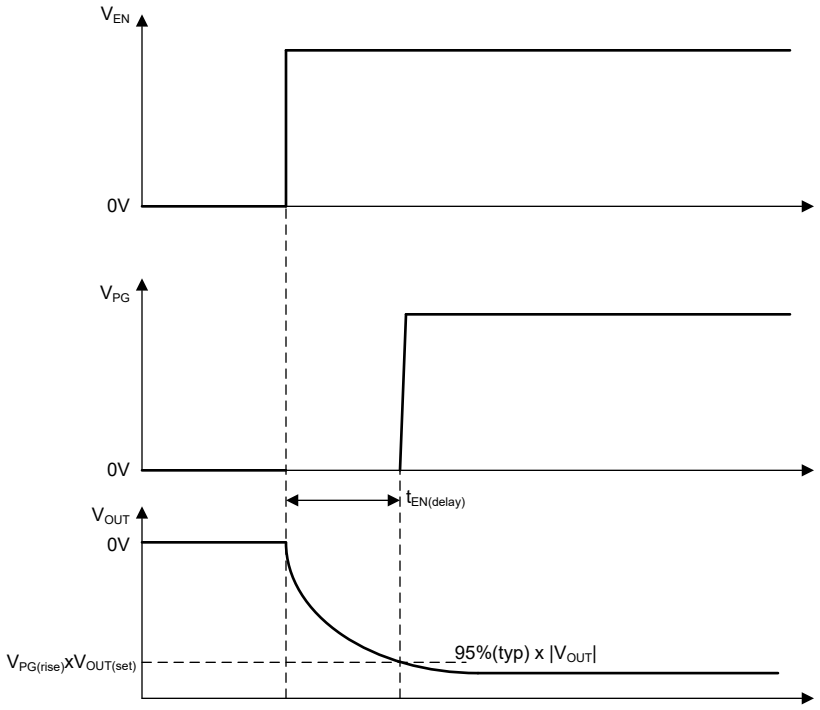

Figure 8-4. Enable Power Good Timing Measurement

9 Detailed Description

9.1 Overview

The TPS7H1301 (adjustable output) and TPS7H1302 (fixed output) generate a precision negative regulated voltage by integrating a low-dropout (LDO) regulator with an inverting charge pump. This architecture enables in situ negative voltage generation without requiring auxiliary negative supplies from the satellite bus or bulky inverting buck-boost converters, making the TPS7H1301/2 suited for negative voltage applications requiring up to 400mA of load current. LDO regulation of the charge pump output (C_{CPOUT}) enables dropout-free operation for loads up to 200mA while reducing output voltage ripple to less than 1_{mVp-p}.

TPS7H1301 (Adjustable Output) The TPS7H1301 provides access to the error amplifier output via the STAB pin for external compensation if needed. The device is internally compensated to typically achieve 6dB gain margin and 50° phase margin without external components. The charge pump operates at 500kHz and is optimized for use with a 1µF ceramic flying capacitor (C_{FLY}) and a 10µF charge pump output capacitor (C_{CPOUT}). The output voltage is easily programmed from -6V to -0.6V with ±1.5% accuracy using external feedback resistors connected to the FB pin.

TPS7H1302 (Fixed Output) The TPS7H1302 provides a fixed -1.8V output, ±1.5% accuracy using internal feedback resistors; which eliminates external voltage-setting resistors and reducing component count. The charge pump operates at 1MHz, enabling a more compact implementation with reduced capacitor values: 0.47µF for C_{FLY} and 4.7µF for C_{CPOUT}. The higher switching frequency and integrated feedback network provide a space-efficient implementation with robust stability.

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9.2 Functional Block Diagram

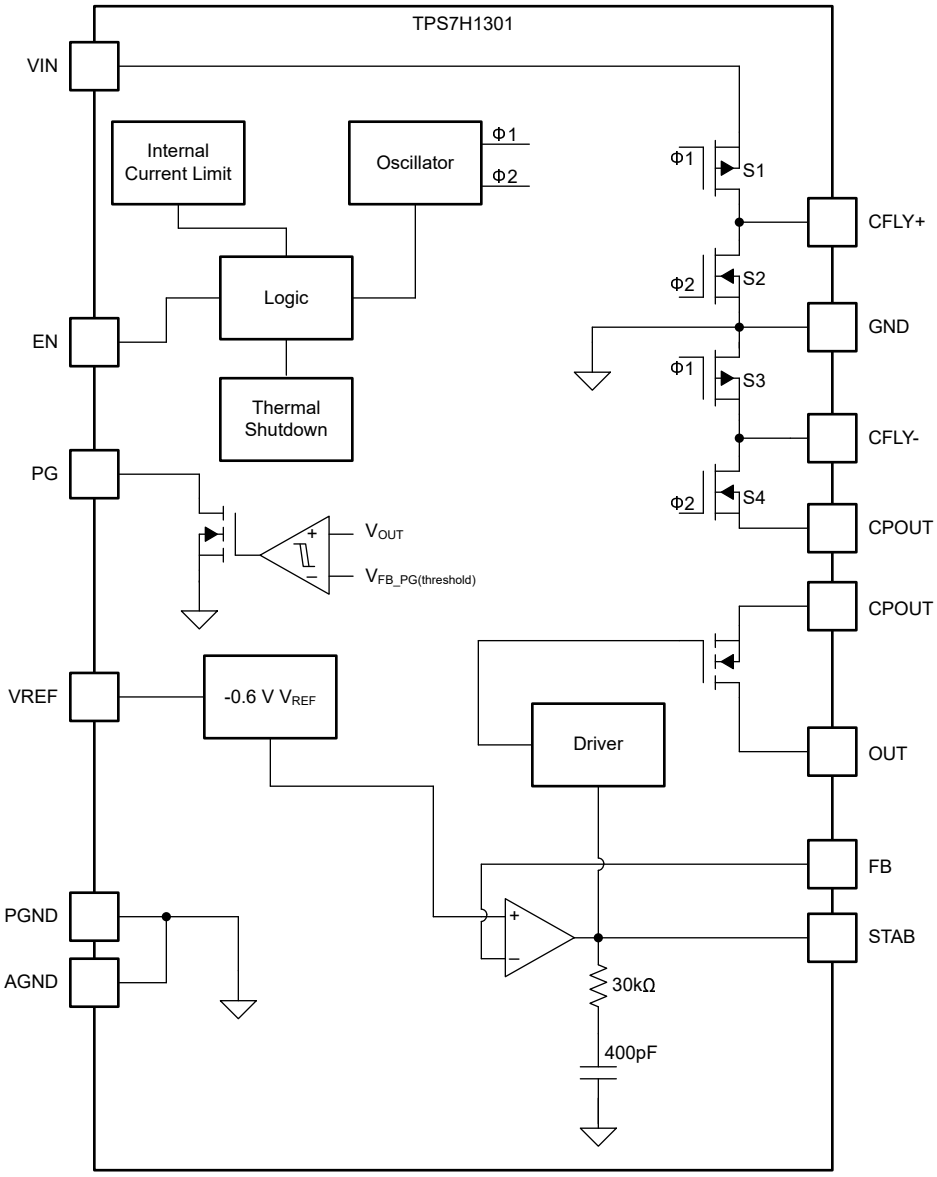

Figure 9-1. TPS7H1301 Functional Block Diagram

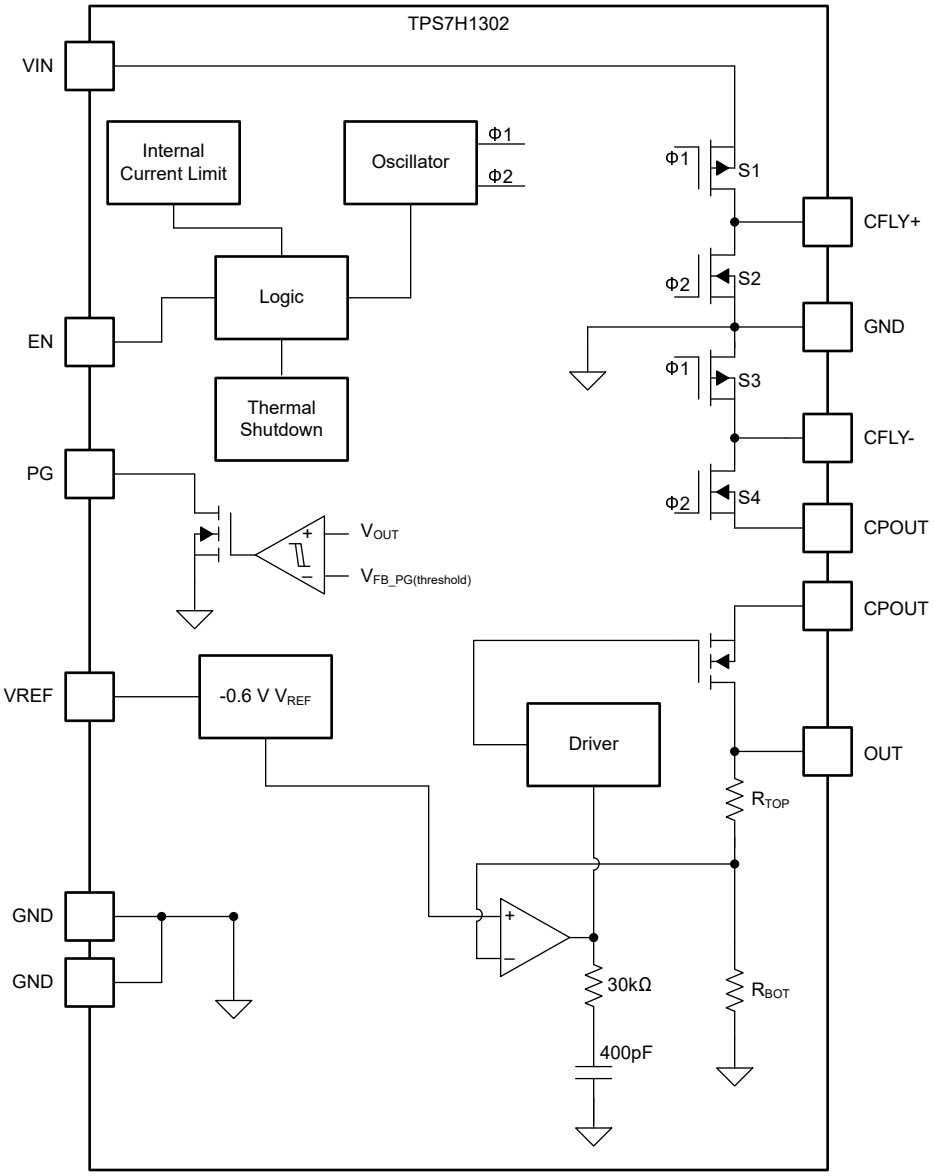

Figure 9-2. TPS7H1302 Functional Block Diagram

9.3 Feature Description

9.3.1 Enable

When the enable pin is low, the device enters shutdown mode and does not regulate the output voltage. Normally, an external resistor divider from V_{IN} to GND is used to feed EN.

Connection of the Enable pin directly to V_{IN} is possible; refer to Equation 1 for resistor sizing guidance at the desired turn-on voltage.

$$V_{IN(rising)} = V_{EN(rising)} \times (R_{EN\_TOP} + R_{EN\_BOT}) / R_{EN\_BOT} \quad (1)$$

Similarly, a VIN(falling) voltage can also be calculated using Equation 2. The $V_{IN(rising)}$ and $V_{IN(falling)}$ can be thought of as configurable UVLO (undervoltage lockout) thresholds.

$$V_{IN(falling)} = V_{EN(falling)} \times (R_{EN\_TOP} + R_{EN\_BOT}) / R_{EN\_BOT} \quad (2)$$

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While the TPS7H1301 and TPS7H1302 commence turn on at a V_{EN} voltage of 0.6V (typ), TI recommends that the final value be above 0.8V. A final turn on value in excess of 0.8V provides appropriate margin above the enable threshold during normal operation to prevent SEFIs during exposure to heavy ions. This recommendation is achieved by satisfying Equation 3.

$$V_{IN(final)} \times R_{EN\_BOT} / (R_{EN\_TOP} + R_{EN\_BOT}) = V_{EN(final)} > 0.8V \quad (3)$$

Alternatively, the EN pin can be driven directly from a microcontroller or FPGA. The low voltage threshold of the enable pin aids in supporting 1.1V, 1.8V, 2.5V, and 3.3V logic levels. Similarly, a final V_{EN} above 0.8V for direct logic level driving is recommended (achieved with standard logic levels).

9.3.2 Charge Pump

The charge pump is implemented as an inverting charge pump that converts V_{IN} to a negative voltage (referenced to PGND)

9.3.2.1 Charge Pump Operation

The voltage inverter portion of the TPS7H1301 and TPS7H1302 contains four large CMOS switches that are switched in sequence to invert the input supply voltage. Energy transfer and storage are provided by external capacitors. Figure 9-1 shows the voltage switches: S1 and S2 are in Φ1, while S3 and S4 are in Φ2. Φ1 and Φ2 are 180° out of phase. Φ1 connects switch S1 to the positive terminal of C_{FLY} to V_{IN}, and S3 connects the negative terminal of C_{FLY} to PGND; switches S2 and S4 are open and isolate node C_{CPOUT} from CFLY. In the second time interval, S1 and S3 are open, which isolates node V_{IN} from C_{FLY}; at the same time, S2 and S4 are closed, and the charge from C_{FLY} commences charging C_{CPOUT}, which equals $-V_{IN}$ when there is no load current and a sufficient number of initial cycles have deposited enough charge in C_{CPOUT}. When a load is added, the output voltage drop (V_{DROOP}) is determined by the parasitic resistance (RDSON of the MOSFET switches and equivalent series resistance (ESR) of the C_{FLY} and C_{CPOUT} capacitor) and the charge transfer loss between the capacitors (see Equation 4 to calculate V_{DROOP}, charge pump R_{CP} can be calculated using Equation 5, typical charge pump values are shown in Charge Pump Resistance).

$$V_{DROOP} = I_{LOAD} \times R_{CP} \quad (4)$$

$$R_{CP} = \frac{1}{(f_{SW} \times C_{FLY})} + 8 \times R_{DS(ON)} + 4 \times R_{ESR(CFLY)} + R_{ESR(CPOUT)} \quad (5)$$

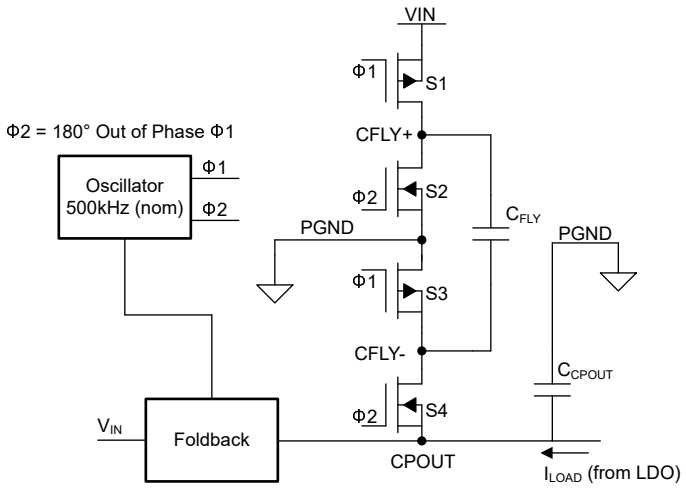

Figure 9-3. Inverting Charge Pump

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9.3.2.2 Foldback Switching

When the voltage at CPOUT (V_{CPOUT}) falls below 60% to 80% of the input voltage magnitude (V_{IN}), the oscillator switching frequency reduces to 25% of the nominal switching frequency. This frequency foldback typically occurs during device start-up and short-circuit events where V_{CPOUT} drops below 70% of V_{IN} magnitude..

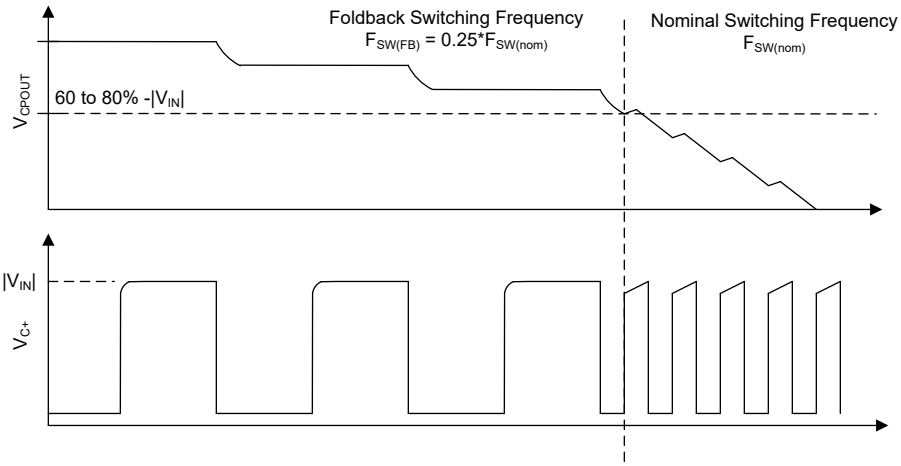

Figure 9-4. Foldback Frequency

9.3.3 Startup

During startup, the TPS7H1301 and TPS7H1302 charge pump begins switching in Frequency Foldback mode. Simultaneously, the negative LDO enters a quasi soft-start mode that limits load current until the Frequency Foldback sequence exits (when $|V_{CPOUT}|$ > 60 to 80% $|V_{IN}|$).

During Frequency Foldback, V_{CPOUT} continues approaching the negative magnitude of V_{IN} while the voltage at V_{OUT} remains at the initial condition. After exiting Frequency Foldback, the OTA of the negative LDO activates, load current begins flowing, and Power Good criteria evaluation commences.

9.3.4 Power Good

The Power Good terminal features an open-drain configuration and can be used to sequence multiple LDOs. The PG terminal remains pulled low until the output voltage reaches 95% (typ) of the final regulation level. Once this threshold is met, the PG pin releases and is pulled high through an external pull-up resistor.

Since the PG pin uses an open-drain architecture, the PG pin can be pulled up to any voltage within the recommended maximum limit of 7V, providing flexible interfacing options for system-level power sequencing applications.

9.3.5 Output Voltage

The TPS7H1301 output voltage is user-programmable within the range of -6V to -0.6V. Programming is accomplished using an external resistor divider network with:

- R_{TOP}: Connected between V_{OUT} and V_{FB}
- R_{BOTTOM}: Connected between V_{FB} and GND

Use Equation 6 to determine V_{OUT}.

$$V_{OUT} = \frac{\left(R_{FB(TOP)} + R_{FB(BOT)}\right) \times V_{FB}}{R_{FB(BOT)}} \quad (6)$$

where

- V_{FB} = 0.6V (typ)

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The TPS7H1302 has a fixed output voltage of -1.8V and is not user configurable.

9.3.6 Dropout

For load currents below 150mA both the TPS7H1301 and TPS7H1302 does not enter dropout conditions due the mininmum input voltage (V_{IN}) and drop voltage (V_{Droop}) providing sufficient head room.

The TPS7H1301 and TPS7H1302 integration of a charge pump and LDO, presents unique considerations in regards to LDO dropout. Firstly when V_{OUT} is sufficiently lower than than the magnitude of V_{IN} the output of the charge pump is sufficiently large enough to provide enough input voltage headroom across load current. Typically, an input voltage of 5V with an output voltage of -1.8V or higher satisfies this no dropout condition.

Secondly, when the magnitudes of VIN and VOUT are relatively close, the load current is determinent as to when the LDO enters dropout.

Dropout current, I_{DO}, is defined as the load current when the output voltage falls to 98% of the initial value at the configured output voltage. See Dropout Current Measurement for the test waveforms used to measure dropout.

During dropout conditions, the pass transistor operates in the ohmic (triode) region and functions as a resistive switch. The dropout voltage specification defines the minimum input voltage margin above the nominal programmed output voltage required to maintain output regulation. When the input voltage falls below this minimum threshold (VIN < VOUT + VDO), the output voltage concurrently decreases proportionally, falling out of regulation.

9.3.7 Output Voltage Accuracy

Voltage Reference and Output Accuracy

Both the TPS7H1301 and TPS7H1302 feature precise voltage references that are essential for minimizing the intrinsic error of the LDO.

Output Voltage Accuracy Specification

Output voltage accuracy defines the minimum and maximum output voltage error relative to the expected nominal output voltage. The accuracy specifications in the Section 7.5 table apply to the operating region where 3V ≤ VIN ≤ 6.3V.

TPS7H1301 Accuracy:

- **±1.5% specification** applies across:
  - Complete temperature range: -55℃ to 125℃
  - Full input voltage range: 3V to 6.3V
  - Output voltage range: -5V to -0.6V
  - Full load range: 10mA ≤ I_{OUT} ≤ 400mA
- **±3% specification** applies when VOUT is below -5V

TPS7H1302 Accuracy:

- **±1.5% specification** applies across:
  - Complete temperature range: -55℃ to 125℃
  - Full load range: 10mA ≤ I_{OUT} ≤ 400mA
  - Full input voltage range: 3V to 6V

Important Measurement Details:

A few additional details to the measurement are noted:

- **Comprehensive Testing**: The V_{IN}, I_{OUT}, and temperature ranges verify the specification applies across all load and temperature combinations through testing multiple bias conditions covering various corners.
- **Minimum Load Current**: Test conditions specify a minimum of 10mA (not 0mA) for robust accuracy measurements. However, in normal applications, neither the TPS7H1301 nor TPS7H1302 requires a minimum load current for stability.

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- **Included Error Terms**: TI does not recommend adding the following error terms to the V_{ACC} specification, as the following characteristics are inherently covered by the V_{ACC} parameter:
  - V_{FB} accuracy
  - Feedback pin leakage ($I_{FB(LKG)}$) with R_{TOP} resistor applied
  - $\Delta V_{OUT}/\Delta V_{IN}$ (line regulation)
  - $\Delta V_{OUT}/\Delta I_{OUT}$ (load regulation)
  - V_{OUT} temperature coefficient
- **Additional Error Sources**: Errors from feedback resistor tolerances can be added to the V_{ACC} specification.

9.3.8 Output Noise

Output Noise

LDO output noise is defined as the internally-generated intrinsic noise produced by the semiconductor circuits within the regulator. The TPS7H1301 and TPS7H1302 devices exhibit typical output noise of 20µVRMS measured over a bandwidth of 10Hz to 100kHz.

Impact of External Compensation (TPS7H1301 only)

When an external compensation network is connected to the STAB pin, the applied network reduces the control loop bandwidth. This reduction in loop bandwidth can diminish the ability of the internal circuitry to suppress internally generated noise, potentially resulting in higher output noise levels compared to the standard configuration.

9.3.9 Power Supply Rejection Ratio

The Power Supply Rejection Ratio (PSRR) of the TPS7H1301 and TPS7H1302 quantifies the ability of the device to attenuate input noise present at V_{CPOUT} from appearing at the regulated output V_{OUT}. PSRR is mathematically defined as the ratio of input voltage variation to the corresponding output voltage variation, typically expressed in decibels (dB). PSRR is mathematically defined in Equation 7.

$$\text{PSRR} = 20 \times \log_{10}\left(\frac{V_{CPOUT(AC)}}{V_{OUT(AC)}}\right) \quad (7)$$

Noise Source Characteristics

The primary source of input noise in these devices originates from the switching ripple generated by the internal inverting charge pump circuit. This switching noise manifests at the fundamental switching frequency and associated switching frequency harmonics:

- TPS7H1301: 500kHz (typ) switching frequency
- TPS7H1302: 1000kHz (typ) switching frequency

Impact of External Compensation (TPS7H1301 only)

When an external compensation network is implemented, the resulting reduction in control loop bandwidth directly affects PSRR performance. A narrower loop bandwidth limits the ability of the regulator to reject input disturbances, particularly at higher frequencies, leading to diminished overall PSRR performance compared to the standard configuration.

9.3.10 Stability

9.3.10.1 Stability of the TPS7H1301

Stability Margins and Design Requirements

Traditional stability margins for space-rated integrated circuits typically impose more stringent requirements than those for industrial and consumer electronics applications. Standard criteria include a minimum gain margin of 6dB and phase margin of 50°. The TPS7H1301 incorporates internal compensation circuitry designed to maintain conservative stability margins across most operating conditions, eliminating the need for external compensation components. When applications require enhanced stability performance or when using specific

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output capacitor types, the optional STAB pin allows for external compensation network adjustment to optimize loop stability.

Intrinsic Stability Performance

The TPS7H1301 features wide intrinsic stability margins, providing robust performance across varying load conditions, temperature ranges, and input voltage variations. This inherent stability reduces design complexity and component count while facilitating reliable operation in demanding space applications. Figure 9-5 illustrates the internal compensation with R_{COMP} and C_{COMP} these are specified by design to be 30kΩ and 400pF.

External Compensation Capability

For applications requiring enhanced stability margins or operating under extreme conditions, the STAB pin provides access to an external RC compensation network. This compensation architecture, illustrated in Figure 9-5, connects directly to the output stage of the error amplifier, positioning the external network strategically before the buffer stage of the pass element.

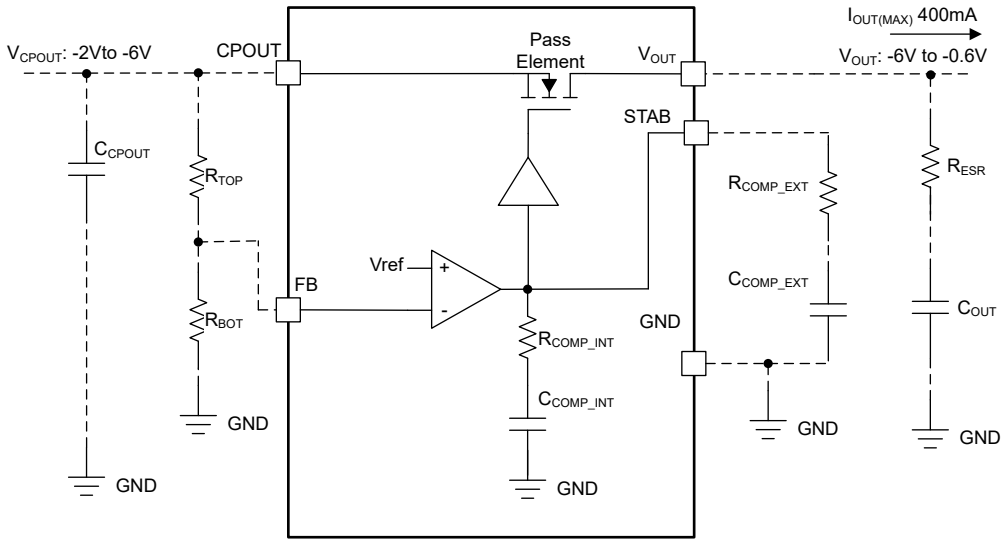

Figure 9-5. Simplified Compensation Schematic

9.3.10.2 Stability of the TPS7H1302

Intrinsic Stability

The TPS7H1302 is designed with same wide intrinsic stability margins of the TPS7H1301, providing robust performance across varying load conditions, temperature ranges, and input voltage variations. This inherent stability reduces design complexity and component count is further reduced by incorporating the feedback resistor nework while facilitating reliable operation in demanding space applications. Figure 9-6 illustrates the internal compensation with R_{COMP} and C_{COMP} these are specified by design to be 30kΩ and 400pF.

ADVANCE INFORMATION

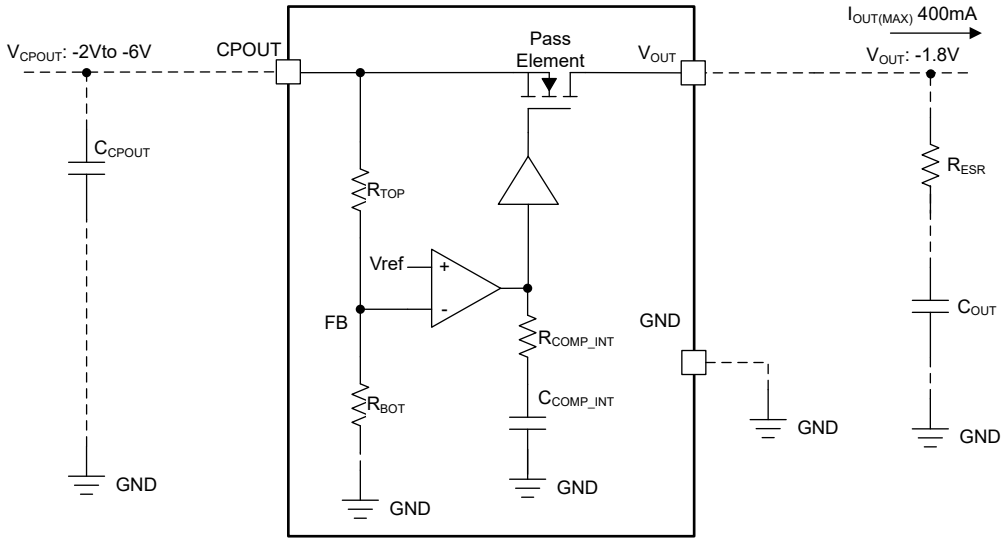

Figure 9-6. TPS7H1302 Simplified Compensation Schematic

9.3.11 Thermal Shutdown

Upon exceeding the TPS7H1301 and TPS7H1302 thermal shutdown temperature limit, the integrated thermal shutdown circuitry activates to turn-off the device when the die temperature exceeds $T_{SD(enter)}$. As the die cools below $T_{SD(exit)}$, the device resumes regulation. The typical $T_{SD(enter)}$ of 160°C and $T_{SD(exit)}$ of 130°C provides a large hysteresis (30°C typical). The large hysteresis is intended to allow the device to sufficiently cool before attempting to resume regulation.

ADVANCE INFORMATION

9.4 Device Functional Modes

9.4.1 Enable Disable

The table below shows the device functional modes:

Table 9-1. Device Functional Modes

EN PIN	DEVICE STATUS
High	Regulation mode
Low	Shutdown mode

10 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

10.1 Application Information

10.2 Typical Application

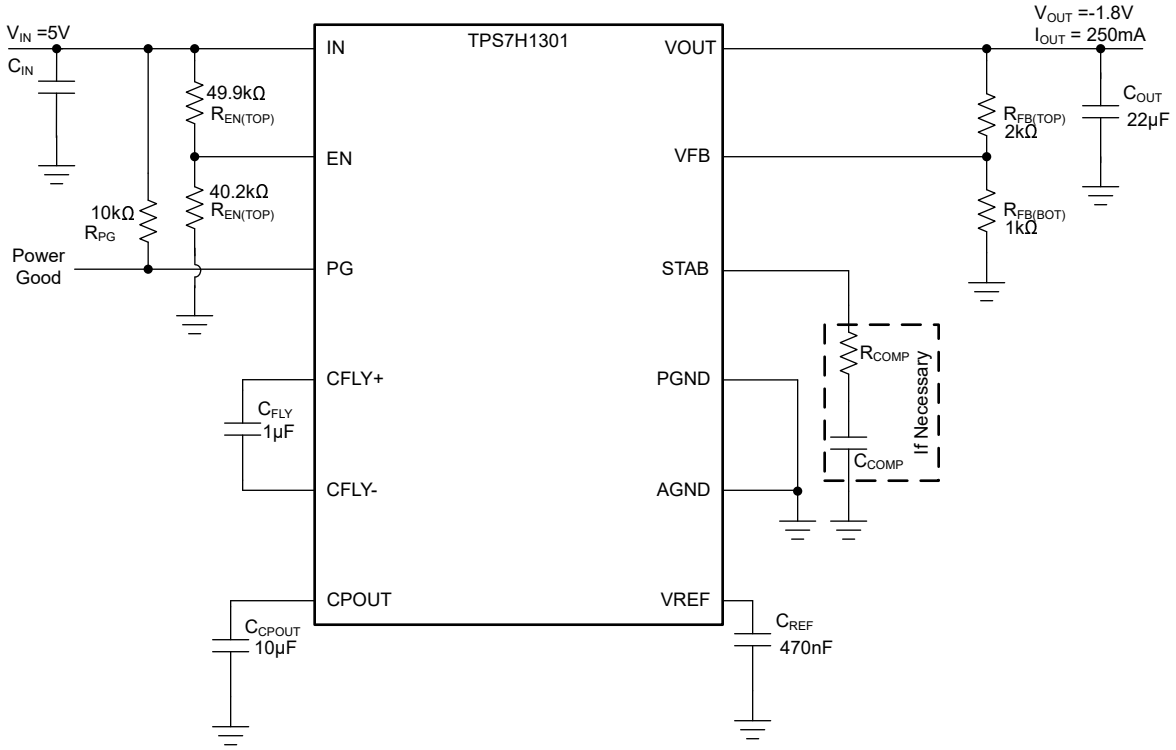

Figure 10-1. Typical Application

10.2.1 Design Requirements

This example highlights a desing using the TPS7H1301EVM evaluation moduel (EVM). For more details, please refer to the EVM user's guide, TPS7H1301EVM-CVAL Evauation Module (EVM) User's Guide (SNVU944). A few parameters must be known to start the design process. These parameters are typically determined at the system level. For this example, we start with the following known parameters:

Table 10-1. Design Parameters

PARAMETER	VALUE
V_{IN}	5V
V_{OUT}	-1.8V
I_{OUT}	250mA
V_{EN}	1.6V

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10.2.2 Detailed Design Procedure

10.2.2.1 Capacitor Selection

Capacitor selection is essential for the operation of the TPS7H130x and is dependent on the role the capacitor functions for the THPS7H130X. Selected capacitors are 25V ceramic; capacitors for C_{FLY} and C_{CPOUT} prioritize low-ESR values, place all capacitors as close to the TPS7H130X as permissiable.

10.2.2.1.1 Input Capacitor (C_{IN}) Selection

TI recommends placing a 10µF 25V (or higher) ceramic capacitor as close as possible to the input pin of the TPS7H130x; additional capacitance and bypass capacitance are considered optional.

The input capacitor (C_{IN}) serves as a charge reservoir that facilitates rapid charge transfer from the supply to the flying capacitors during the charge phase. This capacitor prevents input voltage sag at the beginning of each charge phase when flying capacitors connect to the input. Additionally, the input capacitor filters input noise, protecting sensitive internal analog circuitry that derives bias from the input line.

Effect on Input Ripple

Input capacitance has a direct and proportional relationship with input voltage ripple:

- Increasing input capacitance → Proportionally decreases input voltage ripple
- Decreasing input capacitance → Proportionally increases input voltage ripple

10.2.2.1.2 C_{FLY}

C_{FLY} is the charge pump capacitor that transfers charge from the input to the charge pump output (CPOUT pin).

For typical high-current applications, TI recommends a nominally rated 1µF or two in parallel 0.680µF ceramic output capacitors for stable operation. Polarized capacitors (tantalum, aluminum, electrolytic, and so forth) must not be used for the flying capacitor, as polarized capacitors can become reverse-biased during operation.

If C_{FLY} is sized too small, the charge pump is unable to support high current applications; conversely if C_{FLY} is too large, the charge pump can overwhelm C_{IN} and C_{CPOUT} capacitors, resulting in increased input and output voltage ripple.

Dropout Current is reliant on the charge pump resistance and voltage droop, which is directly affected by the choice of C_{FLY}; selecting a capacitor that is too small or too high ESR increases charge pump output resistance, such that the resulting voltage droop lowers the available headroom for the integrated LDO.

Consideration of C_{FLY} capacitor characteristics, such as DC bias, temperature coefficient are essential in assessing the contribution of the capacitor to charge pump resistance; Equation 8 calculates the fly capacitors contribution to the overall charge pump output resistance and V_{DROOP}. Note, that the min switching frequency (f_{SW}) from the Electrical Characteristics table is the more conservative esitimation parameter; as min f_{SW} results in a higher charge pump resistance..

$$R_{CFLY} = \frac{1}{f_{SW} \times C_{CFLY(min)}} + 4 \times R_{ESR(CFLY)} \quad (8)$$

As Equation 8 shows, a typical reduction in output capacitance due to DC Bias and temperature typically reduces overall C_{FLY} capacitance by 15% to 25% and thus increases charge pump output resistance.

To calculate $C_{FLY(min)}$ consult the capacitor manufacturer data and apply the overall tolerance, DC Bias, and temperature derating: For example, a 25V 1µF X7R capacitor with the following parameters:

- Case Size: 0805
- Tolerance: -5%
- DC Bias @ 5V: -4.56%
- Temperature derating @ 125ºC: -14.56%
- R_{ESR} @ 400kHz: 10mΩ

Table 10-2 is an example tradeoff for selecting either a solitary 1µF (nom.) capacitor or two 0.68µF (nom) capacitors; the overall contribution of C_{FLY} to the resistance of the charge pump is compared against component count (additional board area).

Table 10-2. C_{FLY} Comparison

Attribute	1µF	2x 0.68µF
QTY	1	2 (parallel)
Case Size	0805	0805
Voltage Rating	25V	25V
Dielectric	X7R	X7R
Derating Parameters		
Tolerance	-5%	-5%
DC Bias @ 5V	-4.56%	-2.6%
Tempco. @ 125ºC	-14.56%	-13.47%
Results		
Effective Capacitance	0.775µF	1.073µF
ESR	10mΩ	6.9mΩ (effective res.)
R_{CFLY}	3.45Ω	2.55Ω

To calculate the minimum capacitance for C_{FLY} use :

$$C_{FLY(min)} = C_{FLY(nom)} \times (Tol.) \times (DC\ Bias) \times (Temp) \quad (9)$$

Applying Equation 9 for the 1µF (nom.) capacitor:

$$C_{FLY(min)} = 1\mu F \times (1 - 0.05) \times (1 - 0.0456) \times (1 - 0.1456) = 0.775\mu F \quad (10)$$

The worst case contribution of C_{FLY} is calculated by applying Equation 8 (1µF (nom.) example)

$$R_{CFLY} = \frac{1}{400kHz \times 0.775\mu F} + 4 \times 10m\Omega = 3.45\Omega \quad (11)$$

Table 10-2 shows that the additional component count of the two 0.68µF capacitors offers a significant reduction in the contribution of C_{FLY} to overall charge pump output resistance. Applications at higher operating temperatures, operating currents, or lower V_{IN} benefit from more from overall lower charge pump output resistance. This design examples uses a V_{IN} of 5V and a I_{LOAD} of 250mA is sufficiently served by the 1µF C_{FLY} capacitor.

10.2.2.1.3 CPOUT Capacitor

The Charge Pump Output Capacitor (C_{CPOUT}) is recommended to be configured with a 10µF 16V (or greater) ceramic capacitor with a low ESR value. The ESR of C_{CPOUT} does contribute the output resistance of the charge pump and can be added to the contributions of the charge pump FET $R_{DS(ON)}$, C_{FLY} ESR, and trace resistance at pins C+ and C-.

Sizing of C_{CPOUT} also affects the output ripple. When using values other than 10µF, TI recommends sizing C_{FLY} and C_{IN} to further optimize performance.

10.2.2.1.4 Bypass Capacitors

Bypass capacitors are not required for use with the TPS7H130x; however, given the hard switching nature of the charge pump voltage inverter section, 100nF or smaller bypass capacitors at CFLY, CPOUT, and VOUT offers high frequency noise reduction.

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10.2.2.1.5 Output Capacitor

TI recommends using a 22µF ceramic 25V capacitor with a low ESR (<50mΩ) for VOUT; this capacitor serves the output of the negative LDO. Output capacitors with excessively high ESR, impacts overall LDO stability.

10.2.2.2 Charge Pump Output Resistance

Restating Equation 5 from Section 9.3.2.1 gives the total charge pump output resistance and is referenced as Equation 12 in this section for convenience; which accounts for C_{FLY}, the integrated FETs, and the ESR of C_{CPOUT} contribution to the overall charge pump output resistance.

$$R_{CP} = \frac{1}{(f_{SW} \times C_{FLY})} + 8 \times R_{DS(ON)} + 4 \times R_{ESR(CFLY)} + R_{ESR(CPOUT)} \quad (12)$$

Using the maximum $R_{DS(ON)}$ values for the switches is a conservative approach to prevent underestimating charge pump output resistance and the resultant voltage drop under load current (V_{DROOP}).

10.2.2.3 Output Noise

Consider the following for performance in noise sensitive applications:

- Implement appropriate bypass capacitors and filtering components for high-frequency noise suppression
- Evaluate the trade-off between stability compensation and noise performance when using external STAB pin networks

10.2.2.4 PSRR Design Implications

For applications requiring high PSRR performance:

- Consider the frequency-dependent nature of PSRR when evaluating system performance
- Account for the trade-off between stability margins (via external compensation) and PSRR capability
- Consider C_{OUT} influence (frequency response)
- Account for application load and resultant LDO headroom
- Pay particular attention to noise rejection at the switching frequencies and harmonics
- Refer to the PSRR vs. frequency graphs for detailed performance characteristics across the operational bandwidth

ADVANCE INFORMATION

10.2.2.5 Stability Design Considerations

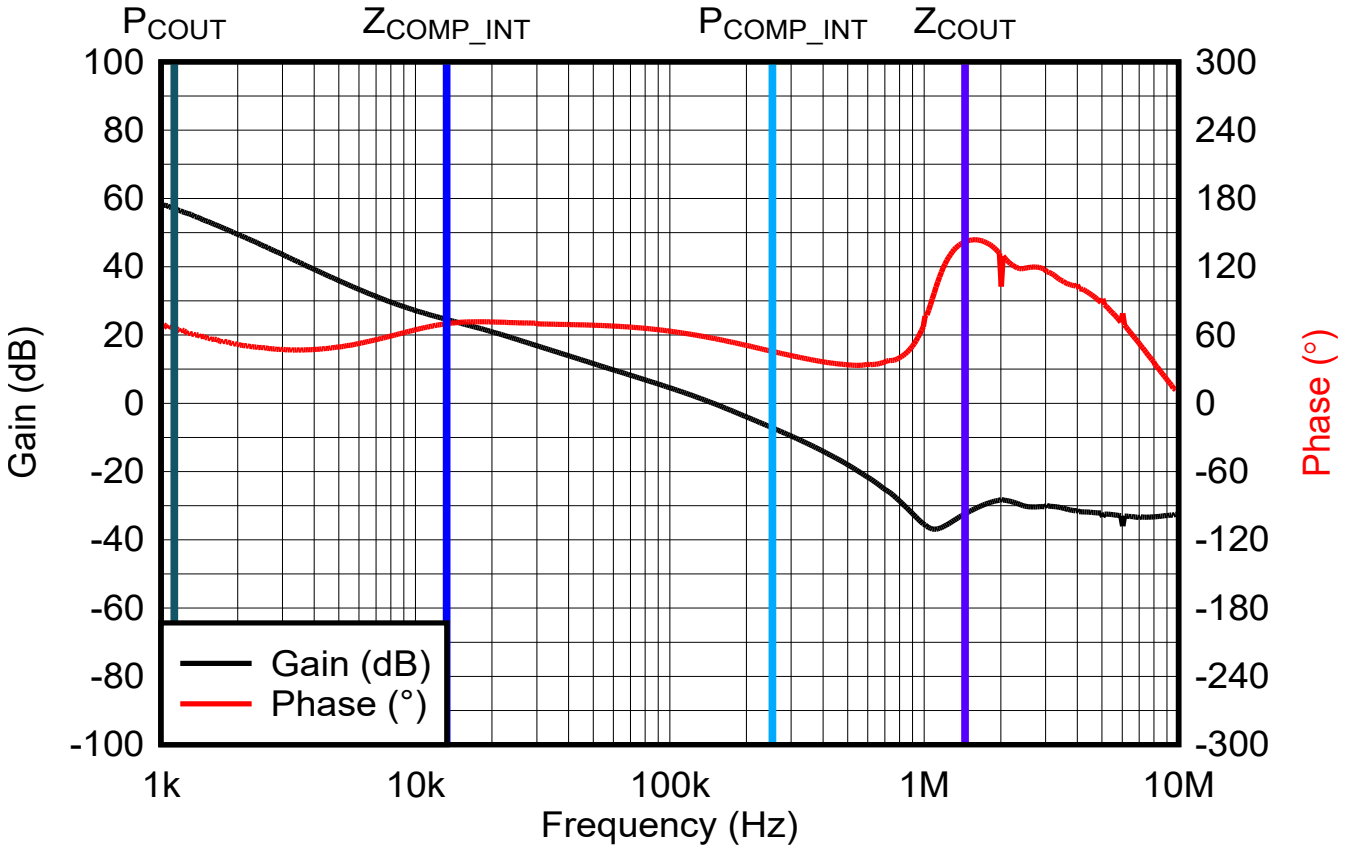

Figure 10-2. Simplified Pole Zero Analysis

The stability of the LDO is influenced primarily by the dominant load pole and zero for the output capacitor (P_{COUT}, Z_{COUT}) and the internal compensation network (P_{COMP_INT}, Z_{COMP_INT}). Figure 10-2 illustrates where the pole and zero of the output capacitor and the internal compensation pole and zero of the LDO are located.

The pole and zero of the output capacitor are calculated using Equation 13 and Equation 14:

$$P_{COUT} = \frac{1}{2\pi \times R_{LOAD} \times C_{OUT}} \quad (13)$$

$$Z_{C_{OUT}} = \frac{1}{2\pi \times ESR_{C_{OUT}} \times C_{OUT}} \quad (14)$$

Applying Equation 13 and Equation 14 results in the following location of the respective pole and zero:

$$P_{COUT} = \frac{1}{2\pi \times 7.2\Omega \times 22\mu F} = 1003Hz \quad (15)$$

$$Z_{C_{OUT}} = \frac{1}{2\pi \times 5m\Omega \times 22\mu F} = 1.446MHz \quad (16)$$

The internal compensation network pole and zero are calculated using Equation 17 and Equation 18:

$$P_{COMP\_INT} = \frac{C_{COMP\_INT} + C_{OTA}}{2\pi \times R_{COMP} \times C_{COMP\_INT} \times C_{OTA}} \quad (17)$$

$$Z_{COMP\_INT} = \frac{1}{2\pi \times R_{COMP} \times C_{COMP\_INT}} \quad (18)$$

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Applying Equation 17 and Equation 18 results in the following location of the respective pole and zero:

$$P_{COMP\_INT} = \frac{400pF + 20pF}{2\pi \times 30k\Omega \times 400pF \times 20pF} = 253kHz \quad (19)$$

$$Z_{COMP\_INT} = \frac{1}{2\pi \times 30k\Omega \times 400pF} = 13.3kHz \quad (20)$$

When applying an external compensation network utilizing the STAB pin utilize Equation 21 and Equation 22:

$$P_{COMP\_EXT} = \frac{\left(C_{COMPT\_INT} \backslash\backslash C_{COMP\_EXT}\right) + C_{OTA}}{2\pi \times \left(R_{COMP\_INT} \backslash\backslash R_{COMP\_EXT}\right) \times \left(C_{COMP\_INT} \backslash\backslash C_{COMP\_EXT}\right) \times C_g} \quad (21)$$

$$Z_{COMP\_EXT} = \frac{1}{2\pi \times \left(R_{COMP\_INT} \backslash\backslash R_{COMP\_EXT}\right) \times \left(C_{COMP\_INT} \backslash\backslash C_{COMP\_EXT}\right)} \quad (22)$$

10.2.3 Application Curves

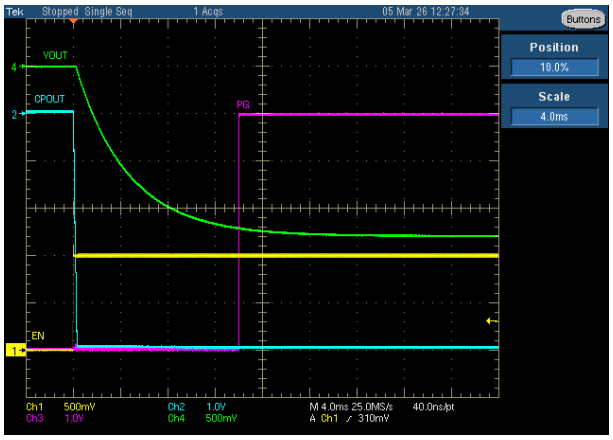

Figure 10-3. Startup

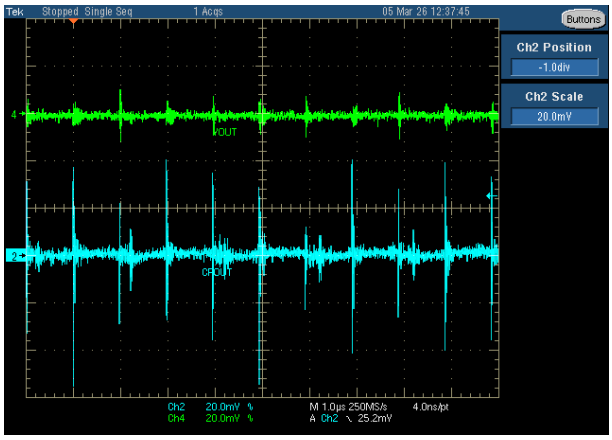

Figure 10-4. Charge Pump Output, V_{CPOUT} and Output Voltage, V_{OUT}

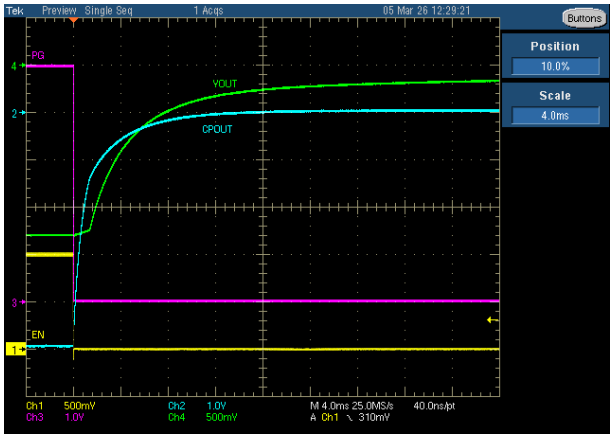

Figure 10-5. Shutdown

10.3 Power Supply Recommendations

The TPS7H1301 and TPS7H1302 are designed to operate from an input voltage supply range between 3V and 6.3V. This input supply must be well regulated and capable of supplying the required input current. If the input supply is located far from the TPS7H1301/2, additional bulk capacitance can be required.

ADVANCE INFORMATION

10.4 Layout

10.4.1 Layout Guidelines

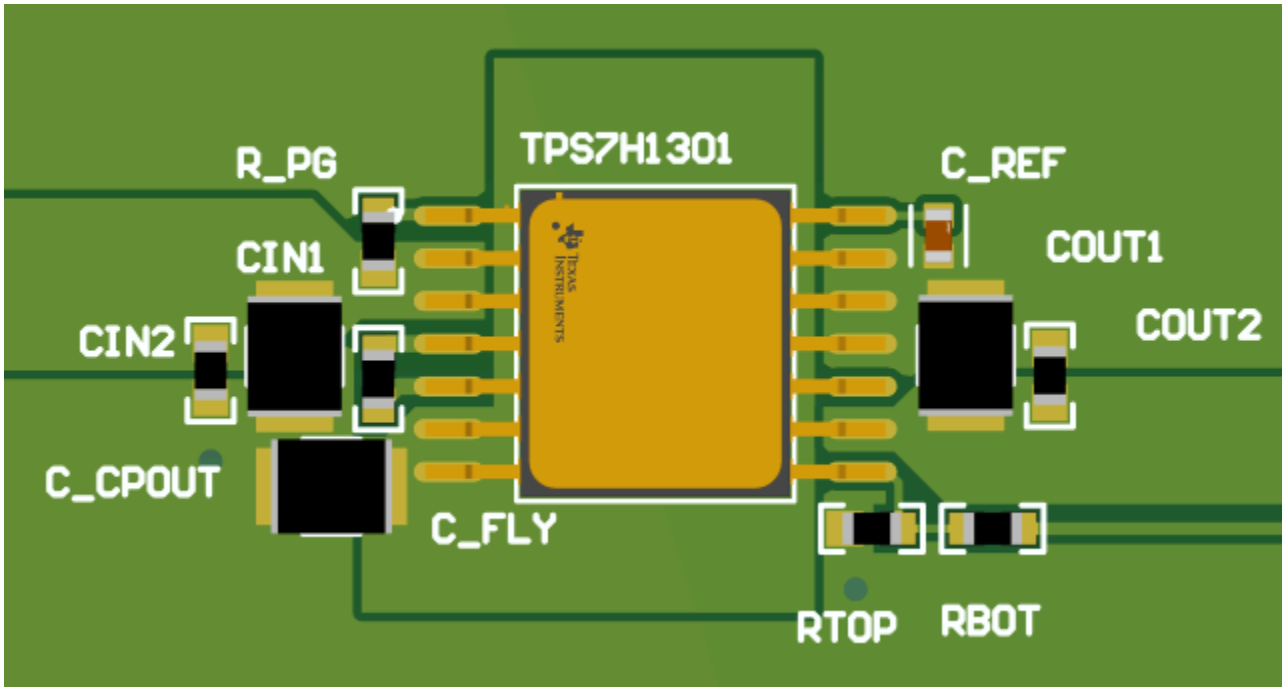

Figure 10-6. Layout Example TPS7H1301

ADVANCE INFORMATION

10.4.2 Layout Example

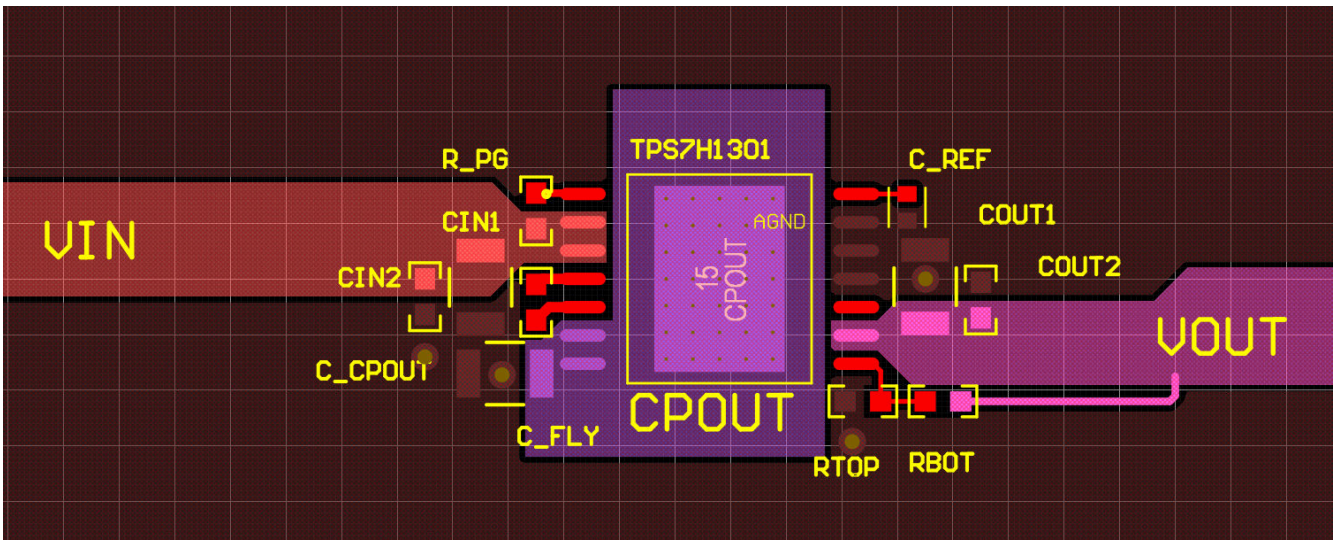

Figure 10-7. TPS7H1301 Layout Example

11 Device and Documentation Support

11.1 Device Support

11.2 Documentation Support

11.2.1 Related Documentation

For related documentation see the following:

- Texas, Instruments, TPS7H1301EVM-CVAL Evaluation Module (EVM)

11.3 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

11.4 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

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11.6 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

11.7 Glossary

TI Glossary	This glossary lists and explains terms, acronyms, and definitions.

12 Revision History

DATE	REVISION	NOTES
March 2026	*	Initial Release

13 Mechanical, Packaging, and Orderable Information

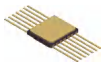
The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

ADVANCE INFORMATION

ADVANCE INFORMATION

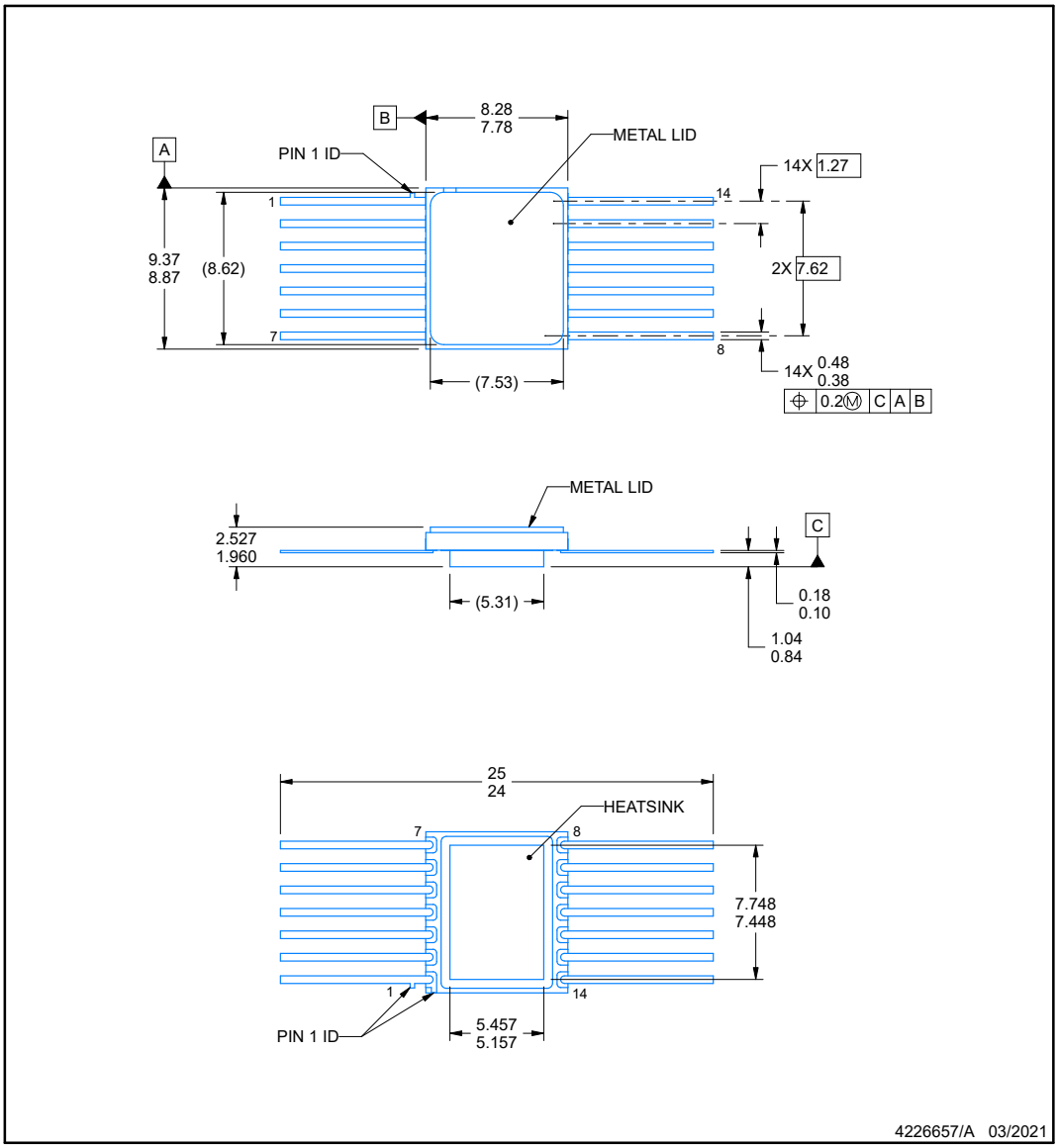
PACKAGE OUTLINE

HBL0014A



CFP - 2.527 mm max height

CERAMIC DUAL FLATPACK



4226657/A 03/2021

NOTES:

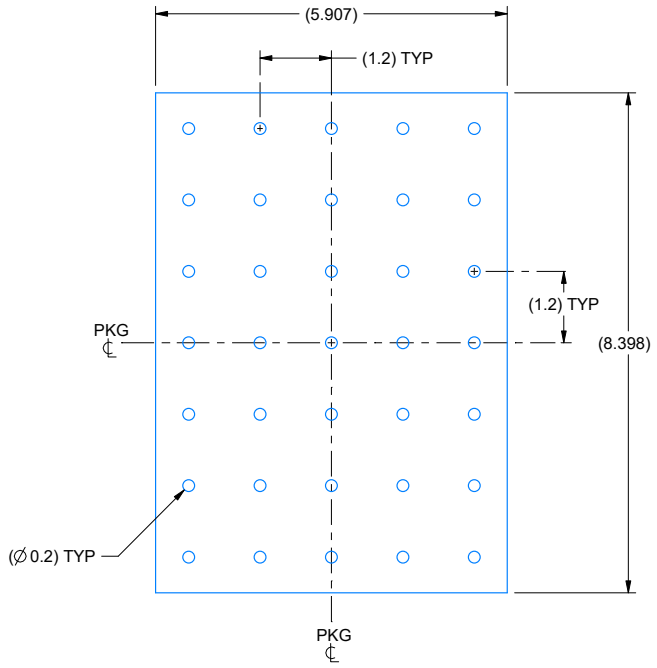
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This package is hermetically sealed with a metal lid. Lid is connected to Heatsink and pin 6
4. The terminals are gold plated.

EXAMPLE BOARD LAYOUT

HBL0014A

CFP - 2.527 mm max height

CERAMIC DUAL FLATPACK



HEATSINK LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:10X

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Last updated 10/2025