TPS7H410x-SP and TPS7H410x-SEP Radiation-Hardened, 3V to 7V Input, 3A per Channel, Multichannel, Synchronous Buck Converter

1 Features

- Total ionizing dose (TID) characterized
  - Radiation hardness assurance (RHA) availability up to 100krad(Si)
- Single-event effects (SEE) characterized
  - Single-event latchup (SEL), single-event burnout (SEB), and single-event gate rupture (SEGR) immune up to linear energy transfer (LET) = 75MeV-cm^2/mg*
  - Single-event functional interrupt (SEFI) and single-event transient (SET) characterized up to LET = 75MeV-cm^2/mg*
- Input voltage range from 3V to 7V
- Up to 3A of maximum output current per channel or more when channels are paralleled
- Typical efficiency of 91.1% (typ.) at VIN = 5V, V_{OUT} = 1.8V, I_{OUT} = 1A at f_{SW} = 500kHz
- Integrated 62mΩ (HS) and 55mΩ (LS) MOSFETs (typ. at V_{IN} = 5V)
- Flexible switching frequency:
  - 100kHz to 1MHz, internal oscillator
  - External synchronization capability
- Accurate voltage reference of 599.48mV ± 1% over line, temperature, and TID
- Monotonic start-up into pre-biased outputs
- Per channel (CHx)
  - Adjustable slope compensation (RSCx)
  - Adjustable soft-start (SS_TRx)
  - Power-good output monitor for undervoltage and overvoltage (PWRGDx)
  - Input enable (ENx)
- Sequence up and reverse sequence down when using EN_SEQ (only valid for TPS7H4104)
- Plastic packages outgas tested per ASTM E595
- Available in military (–55°C to 125°C) temp range

*See TPS7H4104 SEE and TPS7H4102 SEE radiation report for test conditions and full information

2 Applications

- Space satellite point of load supply
- Satellite electrical power systems (EPS)
- Radiation hardened power supplies

3 Description

The TPS7H4104 and TPS7H4102 are 7V, 3A per channel, multichannel, peak-current mode, synchronous buck converters optimized for use in area sensitive, space environment applications. The device incorporates four (TPS7H4104) or two (TPS7H4102) identical channels that can be use to step down the power input voltage into independent voltages up to 3A per phase or interleaved to increment the output current up to 12A (TPS7H4104) or 6A (TPS7H4102).

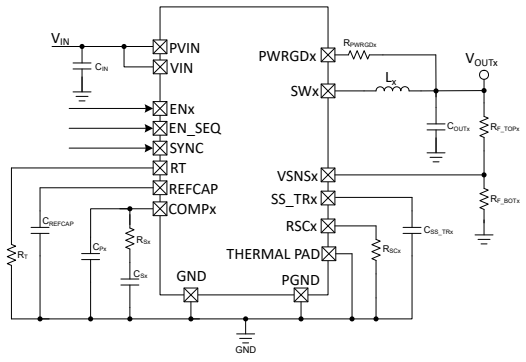
Each channel incorporates the high-side and low-side power MOSFETs with programmable soft-start and slope compensation. Additionally, per channel power-good flags and enable signals are provided. The TPS7H4104 also includes an EN_SEQ input that enables a sequential power-up and a reverse-sequence power-down.

Various current limit mechanisms are included for robust current limiting during fault conditions. Thermal shutdown disables the device when the die temperature exceeds thermal limit.

Device Information

PART NUMBER(1)	GRADE	PACKAGE(2)
5962R2320801PYE(3)	QMLP-RHA	64-pin plastic 10mm × 10mm Mass = 283mg
TPS7H4104MPAPTSEP	SEP	
TPS7H4102MPAPTSEP		

(1) For additional information view the Device Comparison Table
(2) The mass is a nominal value and the body size (length × width) is a nominal value and does not include pins.
(3) Product preview.



Note: EN_SEQ is only available for TPS7H4104

Simplified Schematic

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4 Device Comparison Table

Table 4-1. Device Options

Generic Part Number	Number of Channels	Radiation Rating(1)	Grade(2)	Package	Orderable Part Number
TPS7H4104-SP	4	TID of 100krad(Si) RLAT, DSEE free to 75MeV-cm^2/mg	QMLP-RHA	64-pin HTQFP PAP	5962R2320801PYE(3)
TPS7H4104-SEP		TID of 50krad(Si) RLAT, DSEE free to 43MeV-cm^2/mg	Space Enhanced Plastic		TPS7H4104MPAPTSEP
TPS7H4102-SP	2	TID of 100krad(Si) RLAT, DSEE free to 75MeV-cm^2/mg	QMLP-RHA		5962R2320802PYE(3)
TPS7H4102-SEP		TID of 50krad(Si) RLAT, DSEE free to 43MeV-cm^2/mg	Space Enhanced Plastic		TPS7H4102MPAPTSEP

(1) TID is total ionizing dose and DSEE is destructive single event effects. Additional information is available in the associated TID reports and SEE reports for each product.
(2) For additional information about part grade, view TI Part Ratings
(3) Product preview.

5 Pin Configuration and Functions

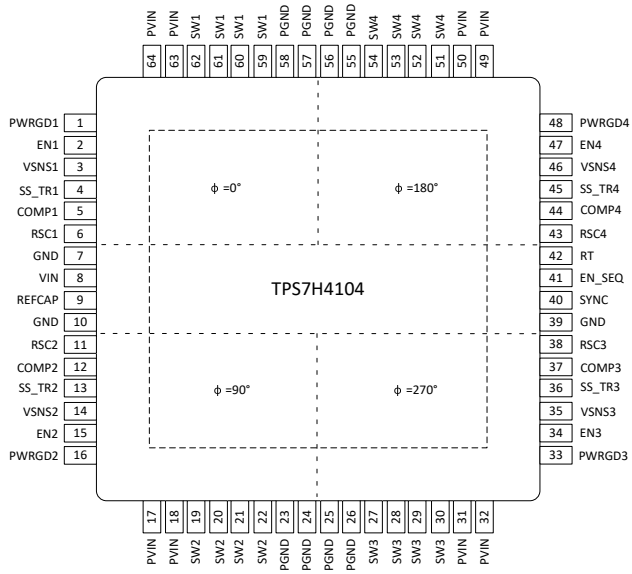


Figure 5-1. TPS7H4104
PAP Package
64-Pin HTQFP
Top View

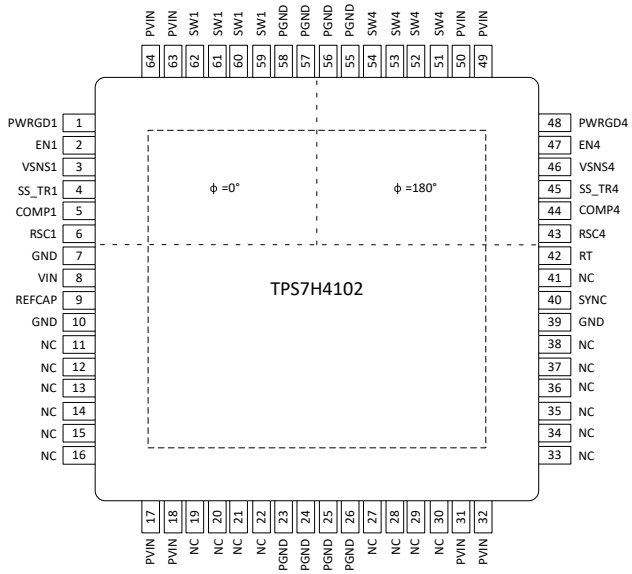


Figure 5-2. TPS7H4102
PAP Package
64-Pin HTQFP
Top View

Table 5-1. Pin Functions

PIN			I/O[1]	DESCRIPTION
NAME	TPS7H4104	TPS7H4102		
PWRGD1	1		O	Power Good pin for CH # 1. This is an open drain output. Connect this pin trough a pull-up resistor to the desired logic level (≤ 7V). PWRGD1 is asserted when V_{OUT1} is within 6% (typ.) of programmed value. PWRGD1 is deasserted when V_{OUT1} is outside 9% (typ.) of programmed value or during a fault condition (such as thermal shutdown).
EN1	2		I	Enable # 1. Pull this pin high [> $V_{ENx\_RISING\ (MAX)}$] to enable the CH # 1. Pull this pin low [< $V_{ENx\_FALLING\ (MIN)}$] to disable the CH # 1. Use a voltage divider between VIN and GND to adjust the turn-on voltage level for CH # 1 as needed.
VSNS1	3		I	Inverting input of the gm error amplifier for CH # 1. Connect this pin as close to the load as possible trough a voltage divider to program the desired output voltage for CH # 1.
SS_TR1	4		I/O	Soft Start and tracking for CH # 1. Connect an external capacitor to control the rise time (or inrush current) for V_{OUT1} during start-up. This pin can also be used for tracking and sequencing.
COMP1	5		I/O	Compensation pin for CH # 1. Output of the transconductance error amplifier and input to the inner current loop comparator of CH # 1. Connect the frequency compensation components for CH # 1 to this pin.
RSC1	6		I/O	Slope compensation for CH # 1 pin. A resistor from RSC1 to GND sets the slope compensation for CH # 1.
GND	7, 10, 39		—	Ground. Return for all internal control circuitry. Connect this pin to PGND for proper operation.
VIN	8		I	Input voltage. Power for all internal control circuitry for CH # 1 to CH # 4. Voltage is recommended to be the same voltage as PVIN and is therefore recommended to externally connect to PVIN. Place a de-coupling capacitor as close as possible to this pin.
REFCAP	9		O	Reference capacitor pin. A 470nF external capacitor is required for the internal bandgap reference. A voltage of 1.235V(typ.) is present at this pin. Do not connect any external circuitry to this pin.
RSC2	11	—	I/O	Slope compensation for CH # 2 pin. A resistor from RSC2 to GND sets the slope compensation for CH # 2.

Table 5-1. Pin Functions (continued)

PIN			I/O[1]	DESCRIPTION
NAME	TPS7H4104	TPS7H4102		
COMP2	12	—	I/O	Compensation pin for CH # 2. Output of the transconductance error amplifier and input to the inner current loop comparator of CH # 2. Connect the frequency compensation components for CH # 2 to this pin.
SS_TR2	13	—	I/O	Soft Start and tracking for CH # 2. Connect an external capacitor to control the rise time (or inrush current) for V_{OUT2} during start-up. This pin can also be used for tracking and sequencing.
VSNS2	14	—	I	Inverting input of the gm error amplifier for CH # 2. Connect this pin as close to the load as possible trough a voltage divider to program the desired output voltage for CH # 2.
EN2	15	—	I	Enable # 2. Pull this pin high [> $V_{ENx\_RISING\ (MAX)}$] to enable the CH # 2. Pull this pin low [< $V_{ENx\_FALLING\ (MIN)}$] to disable the CH # 2. Use a voltage divider between VIN and GND to adjust the turn-on voltage level for CH # 2 as needed.
PWRGD2	16	—	O	Power Good pin for CH # 2. This is an open drain output. Connect this pin trough a pull-up resistor to the desired logic level (≤ 7V). PWRGD2 is asserted when V_{OUT2} is within 6% (typ.) of its programmed value. PWRGD2 is deasserted when V_{OUT2} is outside 9% (typ.) of its programmed value or during a fault condition (such as thermal shutdown).
PVIN	17, 18, 31, 32, 49, 50,63, 64		I	Power Stage input voltage for CH # 1 to CH # 4. Power for the power stages of CH # 1 to CH # 4. Connect localized input capacitor close to each set of PVIN pins.
SW2	19-22	—	O	Switching node # 2 pins . Switch phase node output for CH # 2. Connect this pins to the LC filter for V_{OUT2}. The relative phase for SW2 is 90°.
PGND	23-26, 55-58		—	Power stage ground for CH # 1 to CH # 4. Return for low-side power MOSFETs of CH # 1 to CH # 4. Connect all PGND and GND together.
SW3	27-30	—	O	Switching node # 3 pins . Switch phase node output for CH # 3. Connect this pins to the LC filter for V_{OUT3}. The relative phase for SW3 is 270°.
PWRGD3	33	—	O	Power Good pin for CH # 3. This is an open drain output. Connect this pin trough a pull-up resistor to the desired logic level (≤ 7V). PWRGD3 is asserted when V_{OUT3} is within 6% (typ.) of its programmed value. PWRGD3 is deasserted when V_{OUT3} is outside 9% (typ.) of its programmed value or during a fault condition (such as thermal shutdown).
EN3	34	—	I	Enable # 3. Pull this pin high [> $V_{ENx\_RISING\ (MAX)}$] to enable the CH # 3. Pull this pin low [< $V_{ENx\_FALLING\ (MIN)}$] to disable the CH # 3. Use a voltage divider between VIN and GND to adjust the turn-on voltage level for CH # 3 as needed.
VSNS3	35	—	I	Inverting input of the gm error amplifier for CH # 3. Connect this pin as close to the load as possible trough a voltage divider to program the desired output voltage for CH # 3.
SS_TR3	36	—	I/O	Soft Start and tracking for CH # 3. Connect an external capacitor to control the rise time (or inrush current) for V_{OUT3} during start-up. This pin can also be used for tracking and sequencing.
COMP3	37	—	I/O	Compensation pin for CH # 3. Output of the transconductance error amplifier and input to the inner current loop comparator of CH # 3. Connect the frequency compensation components for CH # 3 to this pin.
RSC3	38	—	I/O	Slope compensation for CH # 3 pin. A resistor from RSC3 to GND sets the slope compensation for CH # 3.
SYNC	40		I	SYNC is an input for an external clock. The frequency of the external clock should match the switching frequency that is set by the resistor between RT and GND by a factor of 4. (f_{SYNC} = 4 x f_{SW})
EN_SEQ	41	—	I	Enable Sequence. Pull this pin high [$V_{EN\_SEQ\_RISING\ (MAX)}$] to start a sequence up, starting from CH # 1 to CH # 4. To start a reverse sequence down pull this pin low [< $V_{EN\_SEQ\_FALLING\ (MIN)}$], starting from CH # 4 to CH # 1. When the sequencer feature is not being used (EN_SEQ = OPEN) and SYNC is externally driven, a 470nF between EN_SEQ and GND is required.
RT	42		I/O	A resistor connected between RT and GND sets the Switching frequency of the converter. The Switching frequency range is 100kHz to 1MHz. When an external clock is used, RT must be selected such that the set switching frequency coincides with the frequency of the external applied clock. In case of a loss clock the device switches to the internal clock at the programmed frequency.
RSC4	43		I/O	Slope compensation for CH # 4 pin. A resistor from RSC4 to GND sets the slope compensation for CH # 4.

Table 5-1. Pin Functions (continued)

PIN			I/O[1]	DESCRIPTION
NAME	TPS7H4104	TPS7H4102		
COMP4	44		I/O	Compensation pin for CH # 4. Output of the transconductance error amplifier and input to the inner current loop comparator of CH # 4. Connect the frequency compensation components for CH # 4 to this pin.
SS_TR4	45		I/O	Soft Start and tracking for CH # 4. Connect an external capacitor to control the rise time (or inrush current) for V_{OUT4} during start-up. This pin can also be used for tracking and sequencing.
VSNS4	46		I	Inverting input of the gm error amplifier for CH # 4. Connect this pin as close to the load as possible trough a voltage divider to program the desired output voltage for CH # 4.
EN4	47		I	Enable # 4. Pull this pin high [> $V_{ENx\_RISING\ (MAX)}$] to enable the CH # 4. Pull this pin low [< $V_{ENx\_FALLING\ (MIN)}$] to disable the CH # 4. Use a voltage divider between VIN and GND to adjust the turn-on voltage level for CH # 4 as needed.
PWRGD4	48		O	Power Good pin for CH # 4. This is an open drain output. Connect this pin trough a pull-up resistor to the desired logic level (≤ 7 V). PWRGD4 is asserted when V_{OUT4} is within 6% (typ.) of the programmed value. PWRGD4 is deasserted when V_{OUT4} is outside 9% (typ.) of the programmed value or during a fault condition (such as thermal shutdown).
SW4	51-54		O	Switching node # 4 pins . Switch phase node output for CH # 4. Connect this pins to the LC filter for V_{OUT4}. The relative phase for CH4 is 180°.
SW1	59-62		O	Switching node # 1 pins . Switch phase node output for CH # 1. Connect this pins to the LC filter for V_{OUT1}. The relative phase for CH1 is 0°.
NC	—	11-22, 27-38, 41	—	No connect. These pins are not internally connected. . Users are recommended to connect these pins to GND to prevent charge buildup; however, these pins can also be left open or tied to any voltage between GND and VIN.

(1) I = Input, O = Output, I/O = Input or Output, — = Other

6 Specifications

6.1 Absolute Maximum Ratings

over operating temperature (unless otherwise noted)(1) (2)

		MIN	MAX	UNIT
Input voltage	VIN, PVINx, ENx, PWRGDx, SYNC, EN_SEQ	–0.3	7.5	V
	RT, RSCx, COMPx, VSNSx, SS_TRx	–0.3	3.6	
Output voltage	SWx	–1	7.5	V
	SWx, 10-ns transient	–3	7.5	
	REFCAP	–0.3	2	
Vdiff	GND to exposed thermal pad	–0.2	0.2	V
Source current	SWx		Current limit	A
	PVINx		Current limit	
	PGNDx		Current limit	
	RT	–200	200	µA
Sink current	SWx		Current limit	A
	PGNDx		Current limit	
	COMPx	–220	220	µA
	PWRGDx	–0.1	5	mA
Operating junction temperature		–55	150	°C
Storage temperature, T_{stg}		–65	150	

(1) Operation outside the Absolute Maximum Ratings may cause permanent device damage. Absolute Maximum Ratings do not imply functional operation of the device at these or any other conditions beyond those listed under Recommended Operating Conditions. If used outside the Recommended Operating Conditions but within the Absolute Maximum Ratings, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.
(2) All voltages values are with respect to GND.

6.2 ESD Ratings

			VALUE	UNIT
V_{ESD}	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins(1)	±1000	V
		Charged device model (CDM), per ANSI/ESDA/JEDEC JS-002, all pins(2)	±250	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating temperature range (unless otherwise noted) (1)

		MIN	NOM	MAX	UNIT
Input voltage	VIN, PVINx(2)	3		7	V
	ENx, PWRGDx, SYNC, EN_SEQ	0		7	
	RSCx, COMPx, RTx, SS_TRx	0		3.3	
	VSNSx	0	0.6	1	
Output voltage	SWx	0		7	V
	SS_TRx	0	1.5	1.7	
	COMPx	0		2.1	
Output current	HSx_{AVG}	0		2.18	A
	LSx_{AVG}	0		2.5	
	SWx_{AVG}	0		3	
	RT	–100		100	µA
Input current	PWRGD	0		2	mA
Operating junction temperature	T_J	–55		125	°C

(1) All voltages values are with respect to GND.
(2) VIN must be equal to PVIN and startup at the same time. Normally this is achieved by tying them to the same voltage rail.

6.4 Thermal Information

THERMAL METRIC(1)		TPS7H410x QFP PAP 64 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	19	℃/W
$R_{\theta JC\_TOP}$	Junction-to-case (top) thermal resistance	6.2	
$R_{\theta JC\_BOT}$	Junction-to-case (bottom) thermal resistance	0.27	
$R_{\theta JB}$	Junction-to-board thermal resistance	4.6	
ψ_{JT}	Junction-to-top characterization parameter	0.1	
ψ_{JB}	Junction-to-board characterization parameter	4.5	

(1) For more information about the traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report (SPRA953).

6.5 Electrical Characteristics

Over 3V ≤ VIN ≤ 7V, PVIN = VIN, open loop configuration, over operating temperature range T_A = –55°C to 125°C, typical values are at T_A = 25°C, valid for all phases, unless otherwise noted; includes RLAT at T_A= 25°C if sub-group number is present for QML RHA and SEP devices.

PARAMETER		TEST CONDITIONS		SUB-GROUP(1)	MIN	TYP	MAX	UNIT
POWER SUPPLIES AND CURRENTS								
V_{UVLOR_VIN}	VIN internal UVLO rising threshold	I_{OUTx} = 0A, V_{ENx} = 1V, PVIN = 5V		1, 2, 3	2.63	2.7	2.83	V
V_{UVLOF_VIN}	VIN internal UVLO falling threshold	I_{OUTx} = 0A, V_{ENx} = 1V, PVIN = 5V		1, 2, 3	2.47	2.52	2.6	
V_{UVLOR_PVIN}	PVIN internal UVLO rising threshold	I_{OUTx} = 0A, V_{ENx} = 1V, VIN = 5V		1, 2, 3	2.37	2.44	2.58	V
V_{UVLOF_PVIN}	PVIN internal UVLO falling threshold	I_{OUTx} = 0A, V_{ENx} = 1V, VIN = 5V		1, 2, 3	1.96	2	2.11	
I_{SHDN_VIN}	VIN shutdown supply current	V_{ENx} = 0V		1, 2, 3		6	8.5	mA
I_{SHDN_PVIN}	PVIN shutdown supply current	V_{ENx} = 0V		1, 2, 3		2.3	4.3	
I_{Q_VIN}	VIN operating quiescent current (non switching)	V_{ENx} = 7V, VSNSx = 1V		1, 2, 3		6.7	15	
I_{Q_PVIN}	PVIN operating quiescent current (non switching)	V_{ENx} = 7V, VSNSx = 1V		1, 2, 3		2.1	3.7	
ENABLE and EN_SEQ								
V_{ENx_RISING}	Enable rising threshold (turn-on)	PVINx = VIN = 5V		1, 2, 3	0.573	0.606	0.645	V
$V_{ENx\_FALLING}$	Enable falling threshold (turn-off)	PVINx = VIN = 5V		1, 2, 3	0.473	0.5	0.532	
$V_{EN\_SEQ\_RISING}$	Enable sequence rising threshold (sequence up)	Rise time ≥ 100ns(2)	See Figure 8-3	1, 2, 3		71%	80%	× VIN
$V_{EN\_SEQ\_FALLING}$	Enable sequence falling threshold (sequence down)	Fall time ≥ 100ns(2)		1, 2, 3	17%	25%		
V_{CHx_ON}	Sequence UP deemed good voltage	See Figure 8-3 (2)				87.4%		× V_{REFx}
V_{CHx_OFF}	Sequence DOWN deemed no-good voltage					15.4%		
$t_{ENx\_VIN\_RISING\_PD}$	Enable propogation delay when ENx and VIN are tied together	VIN = ENx high to SW high	See Figure 7-2	1, 2, 3		0.85	1.7	ms
$t_{ENx\_RISING\_PD}$	Enable propogation delay	ENx high to SW high when VIN > V_{UVLOR_VIN} for at least 1.7ms	See Figure 7-3	1, 2, 3		50	100	µs
$t_{ENx\_FALLING\_PD}$	Disabled propagation delay	ENx low to SW high impedance	See Figure 7-4	1, 2, 3		9.5	35	
I_{ENx_LKG}	Enable input leakage current	V_{ENx} = 7V		1, 2, 3		0.05	154	nA
VOLTAGE REFERENCE								
V_{REFx}	Internal voltage reference (including error amplifier V_{IOx})	See(3)		1, 2, 3	591.5	599.48	603.5	mV
V_{REFCAP}	REFCAP voltage			1, 2, 3	1.2	1.235	1.248	V
ERROR AMPLIFIER								
I_{VSNSx_LKG}	VSNSx input leakage current	VSNSx = 600mV, V_{COMP} = 1V		1, 2, 3			30	nA
gm_{EAx}	Error amplifier transconductance	–10µA < I_{COMP} < 10µA, V_{COMP} = 1V	T_A = -55℃	11	1257	1913	2630	µS
			T_A = 25℃	9	1153	1672	2191	
			T_A = 125℃	10	1029	1343	1657	
$EA_{x\_DC\text{-}GAIN}$	Error amplifier DC gain	VSNSx = 600mV				16000		V/V
EA_{x_ISRC}	Error amplifier source	V_{COMP} = 1V, ±100mV input overdrive		1, 2, 3	88	137	200	µA
EA_{x_ISNK}	Error amplifier sink				87	135	200	
EA_{x_RO}	Error amplifier output resistance					10.8		MΩ
EA_{x_BW}	Error amplifier bandwidth					9.57		MHz
gm_{PSx}	Power stage transconductance	V_{COMPx} = 500mV		1, 2, 3	5.78	8.35	10.46	S
$gm_{PSx\_MATCHING}$	Power stage transconductance matching across all phases	V_{COMPx} = 500mV				1%		

6.5 Electrical Characteristics (continued)

Over 3V ≤ VIN ≤ 7V, PVIN = VIN, open loop configuration, over operating temperature range T_A = –55°C to 125°C, typical values are at T_A = 25°C, valid for all phases, unless otherwise noted; includes RLAT at T_A= 25°C if sub-group number is present for QML RHA and SEP devices.

PARAMETER		TEST CONDITIONS		SUB-GROUP(1)	MIN	TYP	MAX	UNIT
OVERCURRENT PROTECTION								
I_{OC_HSx}	High-side switch overcurrent threshold	Slew rate = 25mA/µs		1, 2, 3	5.0	5.6	6.3	A
$I_{OC\_LS\_SOURCINGx}$	Low-side switch overcurrent sourcing threshold			1, 2, 3	4.2	6	7.8	A
$I_{OC\_LS\_SINKINGx}$	Low-side switch overcurrent sinking threshold			1, 2, 3	1.5	2.55	3.9	A
$COMPx_{CLAMP}$	COMP voltage clamp			1, 2, 3	1.7	1.9	2.13	V
SOFT START AND TRACKING								
I_{SS_TRx}	Soft start charge current	V_{SS_TRx} ≥ 90mV		1, 2, 3	1.4	2.28	2.83	µA
$R_{SS\_TRx\_DISCHARGE}$	Soft start discharge pull-down resistor	V_{SS_TRx} = 110mV		1, 2, 3	230	364	513	Ω
$SS\_TRx_{START\_UP}$	Maximum voltage on SS before startup(4)			1, 2, 3		22	50	mV
SLOPE COMPENSATION								
SCx	Slope compensation	f_{SW} = 100kHz	R_{SCx} = 1.02MΩ			–0.26		A/µs
		f_{SW} = 500kHz	R_{SCx} = 634kΩ			–0.36		A/µs
			R_{SCx} = 213kΩ			–1.26		A/µs
			R_{SCx} = 147kΩ			–1.81		A/µs
		f_{SW} = 1000kHz	R_{SCx} = 97.6kΩ			–2.8		A/µs
MINIMUM ON, OFF AND DEAD TIME								
t_{ONx_MIN}	Minimum on time	10% of rising edge to 90% of falling edge of V_{SWx}, I_{OUT} = 400mA	VIN = 3V	9, 10, 11		163	260	ns
			VIN = 5V	9, 10, 11		182	270	
			VIN = 7V	9, 10, 11		216	320	
t_{OFFx_MIN}	Minimum off time	90% of falling edge to 10% of rising edge of V_{SWx}				216		ns
t_{DEADx}	Dead time					33		ns
SWITCHING FREQUENCY AND SYNCHRONIZATION								
f_{SW}	RT programmed switching frequency	R_{RT} = 511kΩ		4, 5, 6	97	103	120	kHz
		R_{RT} = 90.9kΩ		4, 5, 6	446	502	564	
		R_{RT} = 37.4kΩ		4, 5, 6	812	1040	1280	
t_{SYNC_DLY}	SYNC to SW delay	V_{IN} = 3V	See Figure 7-5	9, 10, 11		221	314	ns
		V_{IN} = 5V		9, 10, 11		194	240	
		V_{IN} = 7V		9, 10, 11		184	238	
V_{SYNC_VIH}	SYNC input high	V_{IN} = 3V		1, 2, 3	1.4			V
		V_{IN} = 5V		1, 2, 3	1.8			
		V_{IN} = 7V		1, 2, 3	2			
V_{SYNC_VIL}	SYNC input low			1, 2, 3			0.8	V
f_{SYNC}	SYNC input frequency range			4, 5, 6	400		4000	kHz
D_{SYNC}	SYNC input duty cycle range	external clock duty cycle		4, 5, 6	40%		60%	
$t_{CLK\_I\_E}$	Internal clock to external clock detection time	RT populated	See Figure 8-8	9, 10, 11		1	3	× T_{SW}
$t_{CLK\_E\_I}$	External clock to internal clock detection time	RT populated	See Figure 8-9	9, 10, 11		2	6	× T_{SYNC}

6.5 Electrical Characteristics (continued)

Over 3V ≤ VIN ≤ 7V, PVIN = VIN, open loop configuration, over operating temperature range T_A = –55°C to 125°C, typical values are at T_A = 25°C, valid for all phases, unless otherwise noted; includes RLAT at T_A= 25°C if sub-group number is present for QML RHA and SEP devices.

PARAMETER		TEST CONDITIONS		SUB-GROUP(1)	MIN	TYP	MAX	UNIT
POWER GOOD								
$PWRGDx_{UV\_FAULT}$	VSNSx falling threshold (fault)	See Figure 8-4		1, 2, 3	89%	91%	92%	
$PWRGDx_{UV\_GOOD}$	VSNSx rising threshold (good)			1, 2, 3	92%	94%	96%	
$PWRGDx_{OV\_FAULT}$	VSNSx rising threshold (fault)	See Figure 8-5		1, 2, 3	107%	109%	111%	
$PWRGDx_{OV\_GOOD}$	VSNSx falling threshold (good)			1, 2, 3	103%	106%	109%	
I_{PWRGDx_LKG}	Output open high leakage	V_{SENSEx} = V_{REFx} , V_{PWRGD} = 7V		1, 2, 3		2	520	nA
$V_{PWRGDx\_V\ OL}$	Power good output low	$I_{PWRGD\_\ SINK}$ ≤ 2mA		1, 2, 3		310	400	mV
VIN_{MIN_PWRGDx}	Minimum VIN for valid PWRGD output	Measured when V_{PWRGD} ≤ 0.5V at 100µA See Figure 8-6		1, 2, 3		0.6	1	V
THERMAL SHUTDOWN								
T_{SD_ENTER}	Thermal shutdown enter temperature	I_{OUTx} = 0A				163		°C
T_{SD_EXIT}	Thermal shutdown exit temperature	I_{OUTx} = 0A				134		
T_{SD_HYS}	Thermal shutdown hysteresis	I_{OUTx} = 0A				29		
MOSFET								
$R_{DS\_ON\_HSx}$	High-side switch resistance	PVIN = VIN = 3V, I_{OUTx} = 500mA	T_A = –55°C	3		54	71	mΩ
			T_A = 25°C	1		70	88	
			T_A = 125°C	2		89	103	
		PVIN = VIN = 5V, I_{OUTx} = 500mA	T_A = –55°C	3		49	63	
			T_A = 25°C	1		62	80	
			T_A = 125°C	2		78	92	
		PVIN = VIN = 7V, I_{OUTx} = 500mA	T_A = –55°C	3		47	60	
			T_A = 25°C	1		59	76	
			T_A = 125°C	2		74	88	
$R_{DS\_ON\_LSx}$	Low-side switch resistance	PVIN = VIN = 3V, I_{OUTx} = 500mA	T_A = –55°C	3		44	55	mΩ
			T_A = 25°C	1		58	68	
			T_A = 125°C	2		75	85	
		PVIN = VIN = 5V, I_{OUTx} = 500mA	T_A = –55°C	3		42	51	
			T_A = 25°C	1		55	64	
			T_A = 125°C	2		71	80	
		PVIN = VIN = 7V, I_{OUTx}= 500mA	T_A = –55°C	3		41	50	
			T_A = 25°C	1		54	63	
			T_A = 125°C	2		69	79	

(1) Subgroups are applicable for QML parts. For subgroup definitions, see the Quality Conformance Inspection table.
(2) Valid only for the TPS7H4104
(3) Use this V_{REFx} value to set the output voltage. Measured in a non-switching configuration as shown in Figure 7-1.
(4) The device does not begin startup until the voltage on SS discharges below $SS\_TRx_{START\_UP}$ to provide proper soft start functionality

6.6 Quality Conformance Inspection

MIL-STD-883, Method 5005 - Group A

SUBGROUP	DESCRIPTION	TEMP (°C)
1	Static tests at	25
2	Static tests at	125
3	Static tests at	–55
4	Dynamic tests at	25
5	Dynamic tests at	125
6	Dynamic tests at	–55
7	Functional tests at	25
8A	Functional tests at	125
8B	Functional tests at	–55
9	Switching tests at	25
10	Switching tests at	125
11	Switching tests at	–55

6.7 Typical Characteristics

PVIN = VIN, REFCAP = 470nF, L=3.3µH (model: MPX1D1250L3R3), unless otherwise noted.

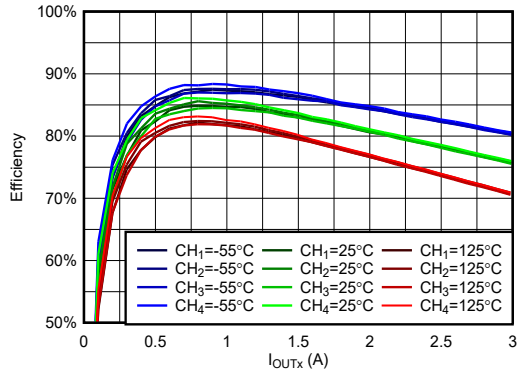


Figure 6-1. Efficiency vs Load at VIN = 3.3V,V_{OUTx} = 0.8V, f_{SW} = 100kHz

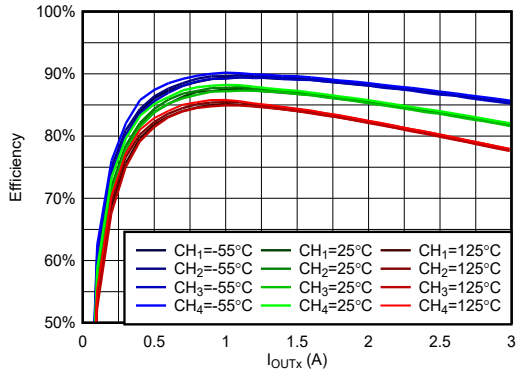


Figure 6-2. Efficiency vs Load at VIN = 3.3V,V_{OUTx} = 1.2V, f_{SW} = 100kHz

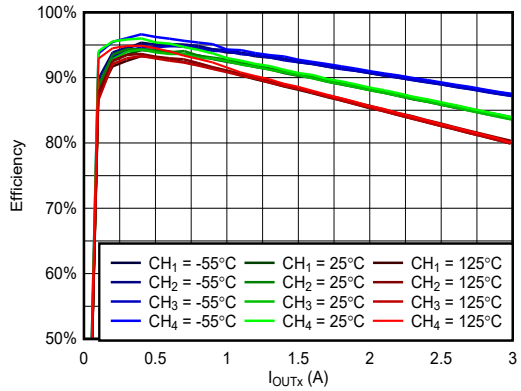


Figure 6-3. Efficiency vs Load at VIN = 3.3V,V_{OUTx} = 1.5V, f_{SW} = 100kHz

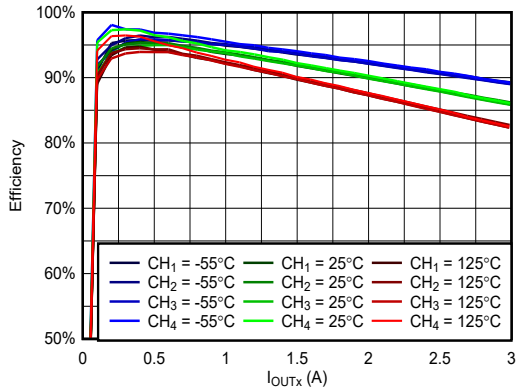


Figure 6-4. Efficiency vs Load at VIN = 3.3V,V_{OUTx} = 1.8V, f_{SW} = 100kHz

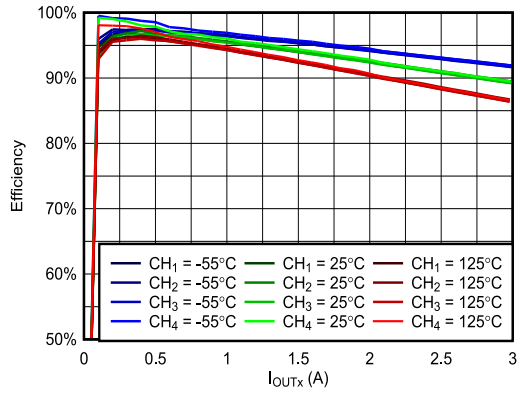


Figure 6-5. Efficiency vs Load at VIN = 3.3V,V_{OUTx} = 2.5V, f_{SW} = 100kHz

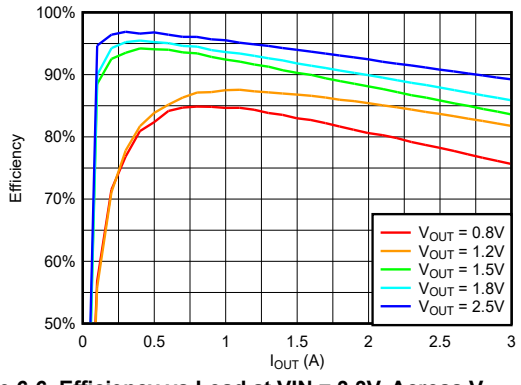


Figure 6-6. Efficiency vs Load at VIN = 3.3V, Across V_{OUT} at f_{SW} = 100kHz for Channel # 1 at 25℃

6.7 Typical Characteristics (continued)

PVIN = VIN, REFCAP = 470nF, L=3.3µH (model: MPX1D1250L3R3), unless otherwise noted.

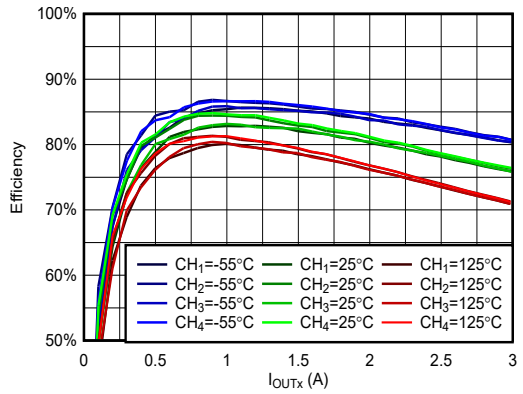


Figure 6-7. Efficiency vs Load at VIN = 5V,V_{OUTx} = 0.8V, f_{SW} = 100kHz

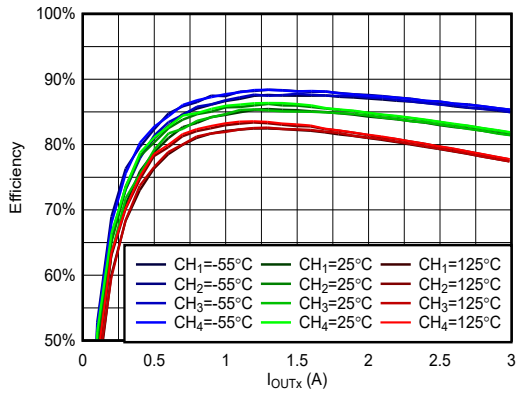


Figure 6-8. Efficiency vs Load at VIN = 5V,V_{OUTx} = 1.2V, f_{SW} = 100kHz

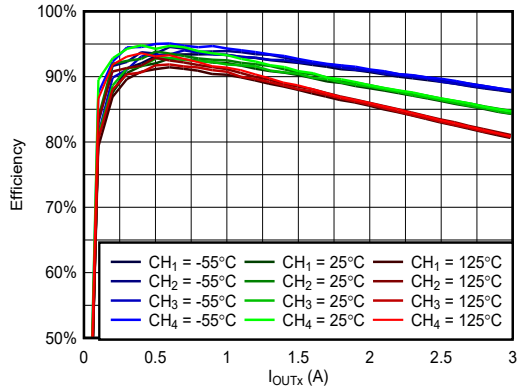


Figure 6-9. Efficiency vs Load at VIN = 5V,V_{OUTx} = 1.5V, f_{SW} = 100kHz

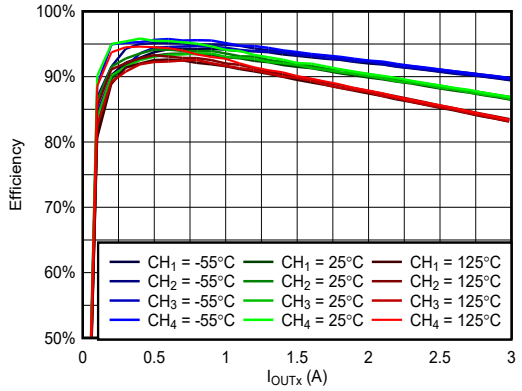


Figure 6-10. Efficiency vs Load at VIN = 5V,V_{OUTx} = 1.8V, f_{SW} = 100kHz

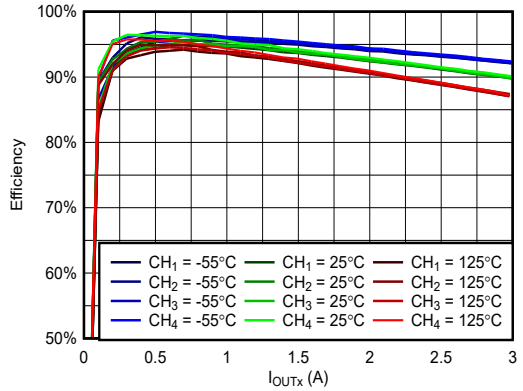


Figure 6-11. Efficiency vs Load at VIN = 5V,V_{OUTx} = 2.5V, f_{SW} = 100kHz

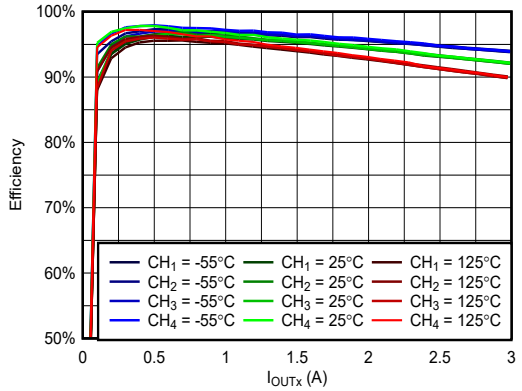


Figure 6-12. Efficiency vs Load at VIN = 5V,V_{OUTx} = 3.3V, f_{SW} = 100kHz

6.7 Typical Characteristics (continued)

PVIN = VIN, REFCAP = 470nF, L=3.3µH (model: MPX1D1250L3R3), unless otherwise noted.

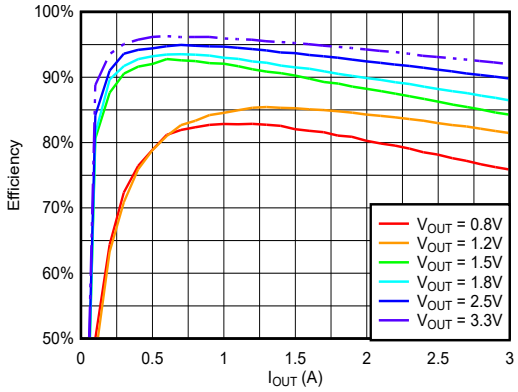


Figure 6-13. Efficiency vs Load at VIN = 5V, Across V_{OUT} at f_{SW} = 100kHz for Channel # 1 at 25℃

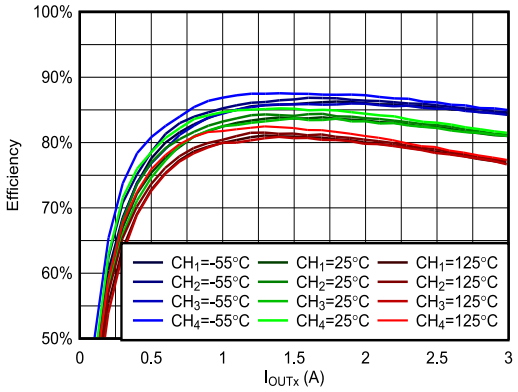


Figure 6-14. Efficiency vs Load at VIN = 7V,V_{OUTx} = 1.2V, f_{SW} = 100kHz

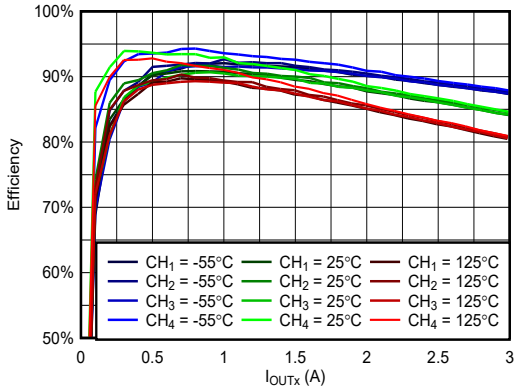


Figure 6-15. Efficiency vs Load at VIN = 7V,V_{OUTx} = 1.5V, f_{SW} = 100kHz

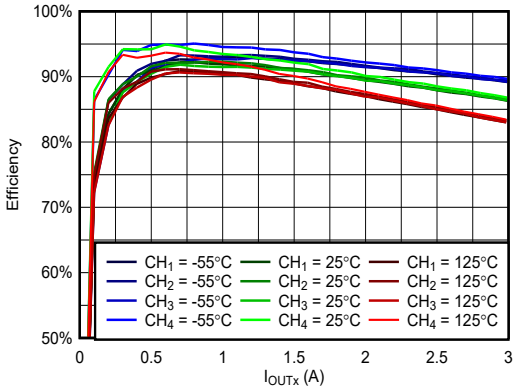


Figure 6-16. Efficiency vs Load at VIN = 7V,V_{OUTx} = 1.8V, f_{SW} = 100kHz

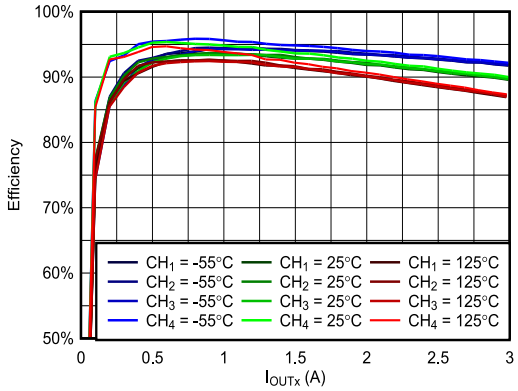


Figure 6-17. Efficiency vs Load at VIN = 7V,V_{OUTx} = 2.5V, f_{SW} = 100kHz

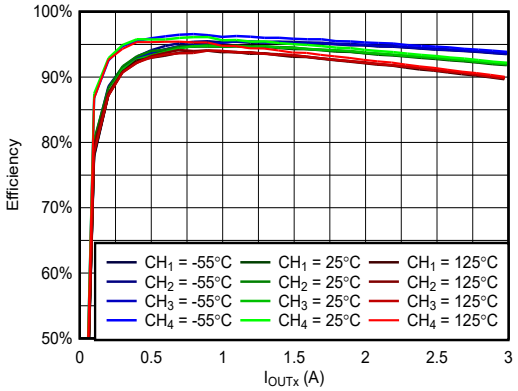


Figure 6-18. Efficiency vs Load at VIN = 7V,V_{OUTx} = 3.3V, f_{SW} = 100kHz

6.7 Typical Characteristics (continued)

PVIN = VIN, REFCAP = 470nF, L=3.3µH (model: MPX1D1250L3R3), unless otherwise noted.

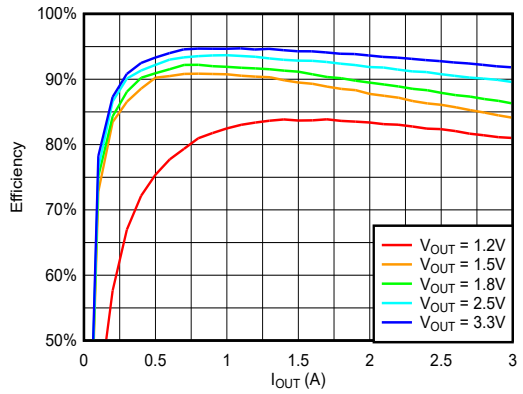


Figure 6-19. Efficiency vs Load at VIN = 7V, Across V_{OUT} at f_{SW} = 100kHz for Channel # 1 at 25℃

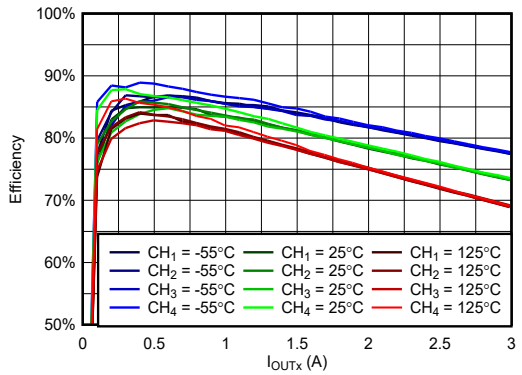


Figure 6-20. Efficiency vs Load at VIN = 3.3V,V_{OUTx} = 0.8V, f_{SW} = 500kHz

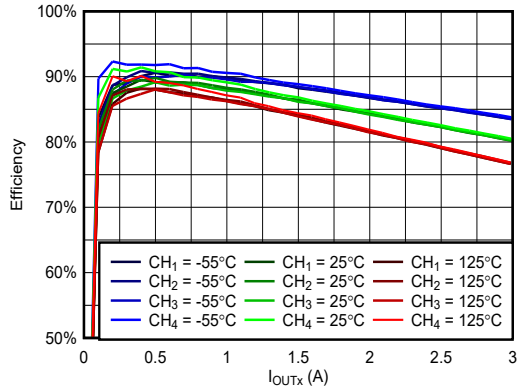


Figure 6-21. Efficiency vs Load at VIN = 3.3V,V_{OUTx} = 1.2V, f_{SW} = 500kHz

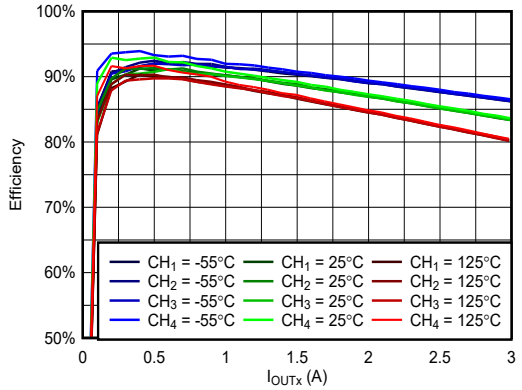


Figure 6-22. Efficiency vs Load at VIN = 3.3V,V_{OUTx} = 1.5V, f_{SW} = 500kHz

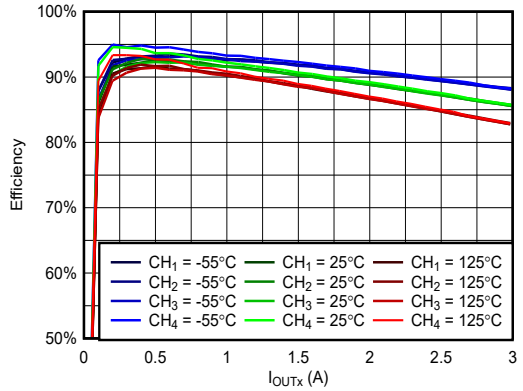


Figure 6-23. Efficiency vs Load at VIN = 3.3V,V_{OUTx} = 1.8V, f_{SW} = 500kHz

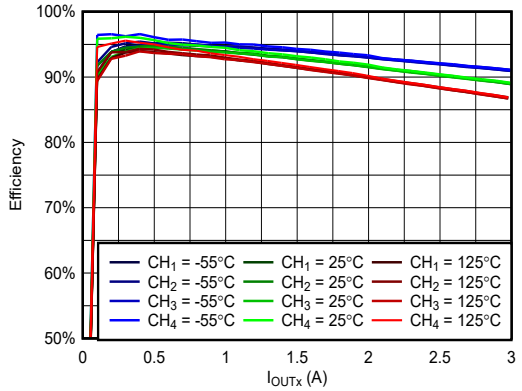


Figure 6-24. Efficiency vs Load at VIN = 3.3V,V_{OUTx} = 2.5V, f_{SW} = 500kHz

6.7 Typical Characteristics (continued)

PVIN = VIN, REFCAP = 470nF, L=3.3µH (model: MPX1D1250L3R3), unless otherwise noted.

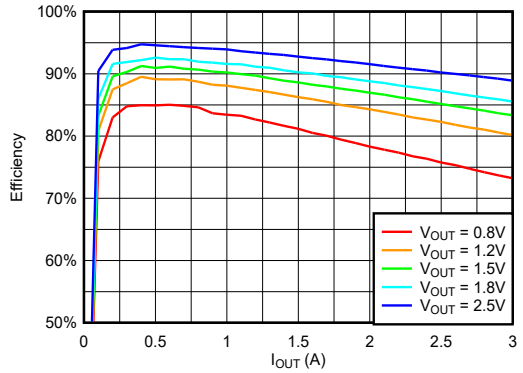


Figure 6-25. Efficiency vs Load at VIN = 3.3V, Across V_{OUT} at f_{SW} = 500kHz for Channel # 1 at 25℃

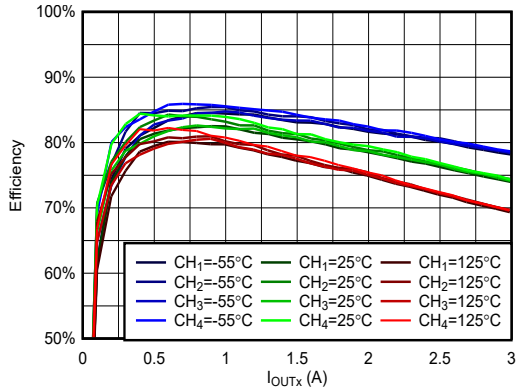


Figure 6-26. Efficiency vs Load at VIN = 5V,V_{OUTx} = 0.8V, f_{SW} = 500kHz

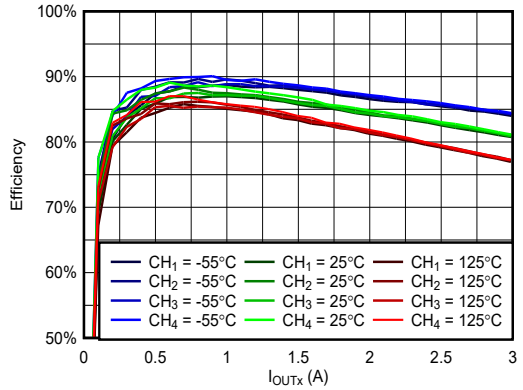


Figure 6-27. Efficiency vs Load at VIN = 5V,V_{OUTx} = 1.2V, f_{SW} = 500kHz

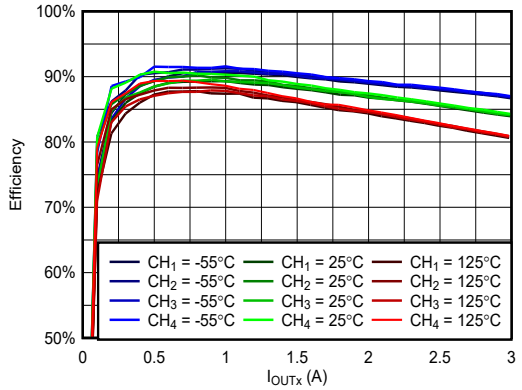


Figure 6-28. Efficiency vs Load at VIN = 5V,V_{OUTx} = 1.5V, f_{SW} = 500kHz

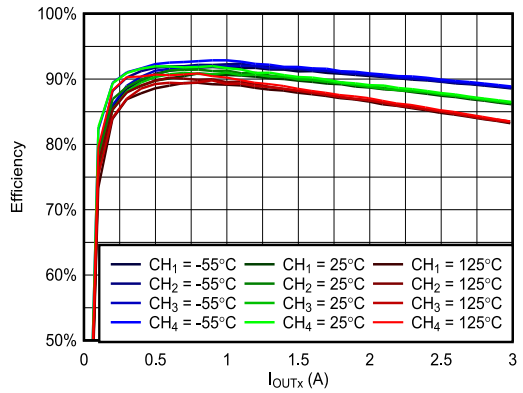


Figure 6-29. Efficiency vs Load at VIN = 5V,V_{OUTx} = 1.8V, f_{SW} = 500kHz

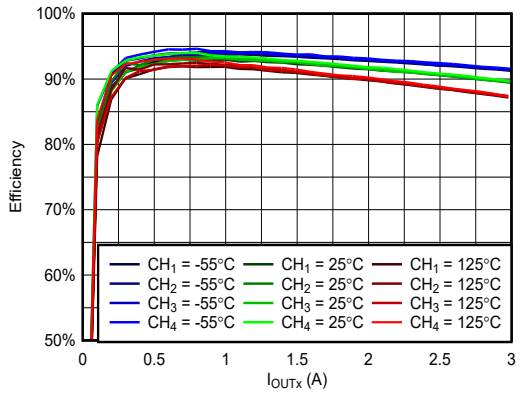


Figure 6-30. Efficiency vs Load at VIN = 5V,V_{OUTx} = 2.5V, f_{SW} = 500kHz

6.7 Typical Characteristics (continued)

PVIN = VIN, REFCAP = 470nF, L=3.3µH (model: MPX1D1250L3R3), unless otherwise noted.

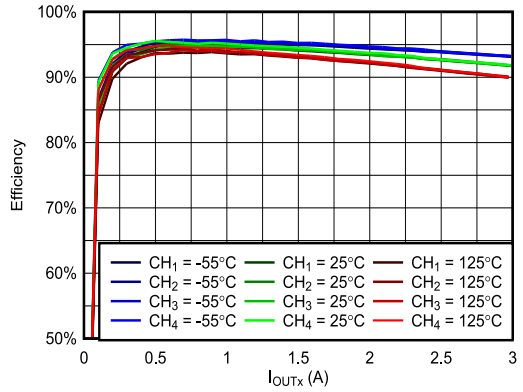


Figure 6-31. Efficiency vs Load at VIN = 5V,V_{OUTx} = 3.3V, f_{SW} = 500kHz

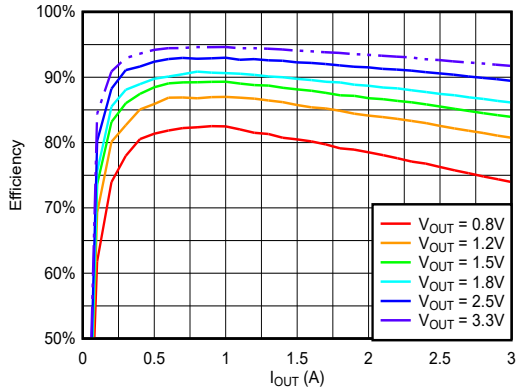


Figure 6-32. Efficiency vs Load at VIN = 5V, Across V_{OUT} at f_{SW} = 500kHz for Channel # 1 at 25℃

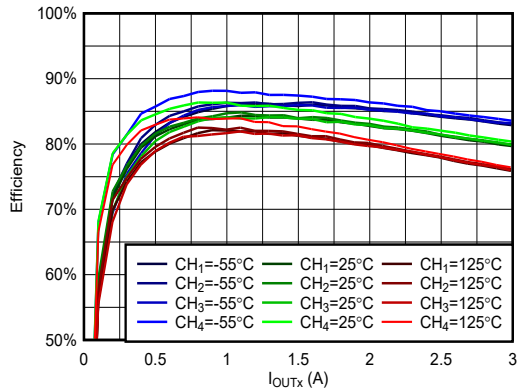


Figure 6-33. Efficiency vs Load at VIN = 7V,V_{OUTx} = 1.2V, f_{SW} = 500kHz

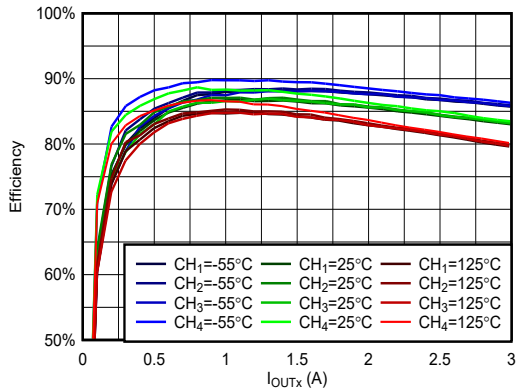


Figure 6-34. Efficiency vs Load at VIN = 7V,V_{OUTx} = 1.5V, f_{SW} = 500kHz

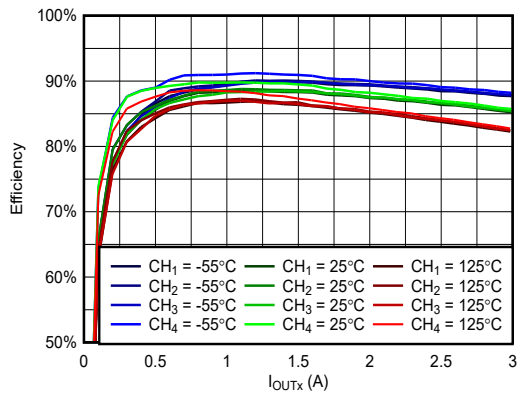


Figure 6-35. Efficiency vs Load at VIN = 7V,V_{OUTx} = 1.8V, f_{SW} = 500kHz

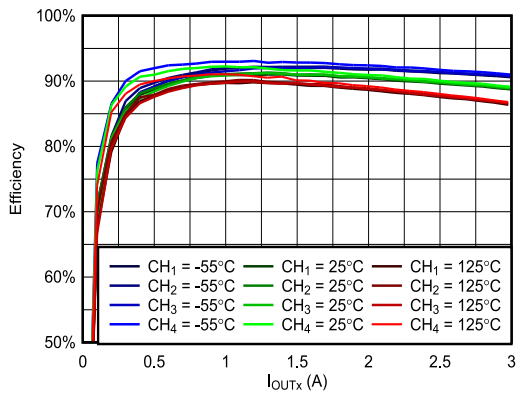


Figure 6-36. Efficiency vs Load at VIN = 7V,V_{OUTx} = 2.5V, f_{SW} = 500kHz

6.7 Typical Characteristics (continued)

PVIN = VIN, REFCAP = 470nF, L=3.3µH (model: MPX1D1250L3R3), unless otherwise noted.

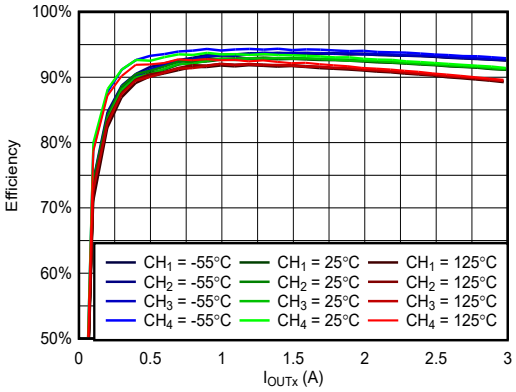


Figure 6-37. Efficiency vs Load at VIN = 7V,V_{OUTx} = 3.3V, f_{SW} = 500kHz

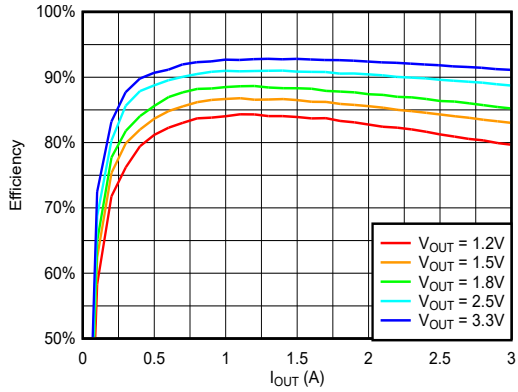


Figure 6-38. Efficiency vs Load at VIN = 7V, Across V_{OUT} at f_{SW} = 500kHz for Channel # 1 at 25℃

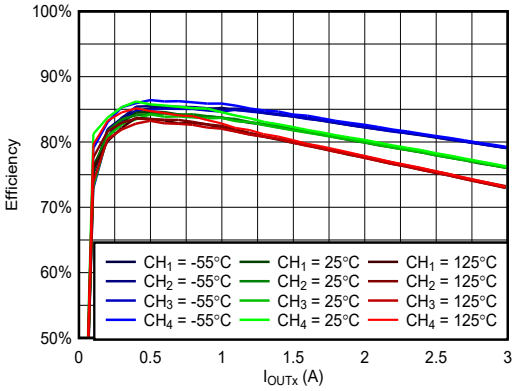


Figure 6-39. Efficiency vs Load at VIN = 3.3V,V_{OUTx} = 1.2V, f_{SW} = 1MHz

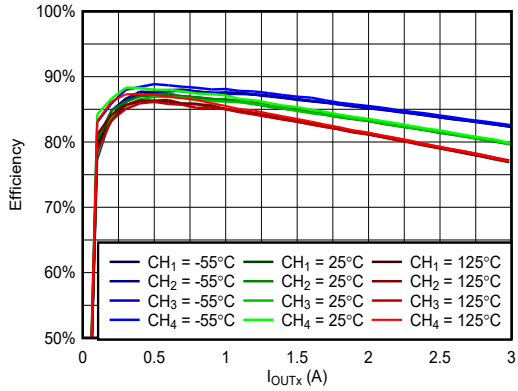


Figure 6-40. Efficiency vs Load at VIN = 3.3V,V_{OUTx} = 1.5V, f_{SW} = 1MHz

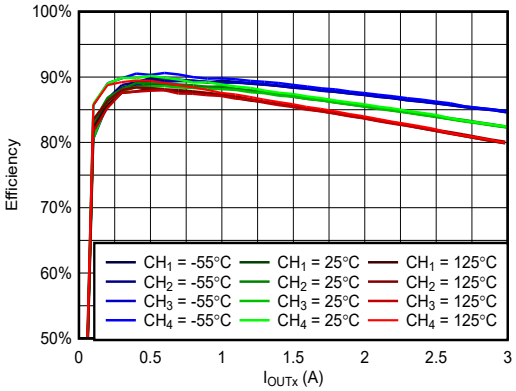


Figure 6-41. Efficiency vs Load at VIN = 3.3V,V_{OUTx} = 1.8V, f_{SW} = 1MHz

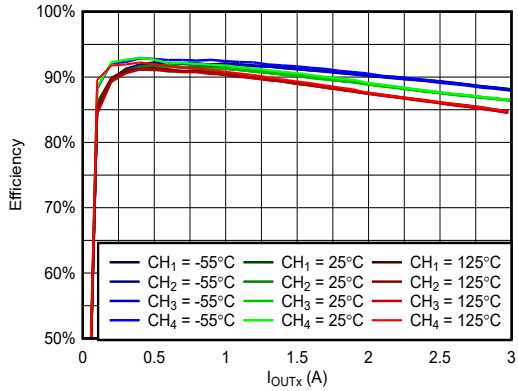


Figure 6-42. Efficiency vs Load at VIN = 3.3V,V_{OUTx} = 2.5V, f_{SW} = 1MHz

6.7 Typical Characteristics (continued)

PVIN = VIN, REFCAP = 470nF, L=3.3µH (model: MPX1D1250L3R3), unless otherwise noted.

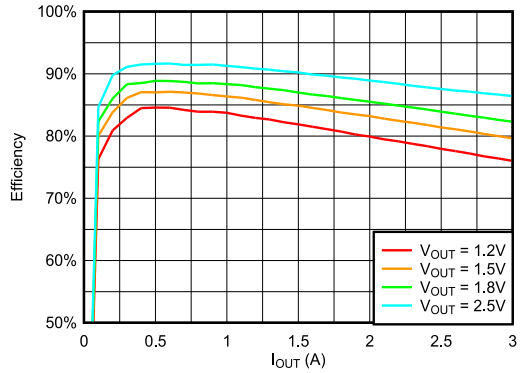


Figure 6-43. Efficiency vs Load at VIN = 3.3V, Across V_{OUT} at f_{SW} = 1MHz for Channel # 1 at 25℃

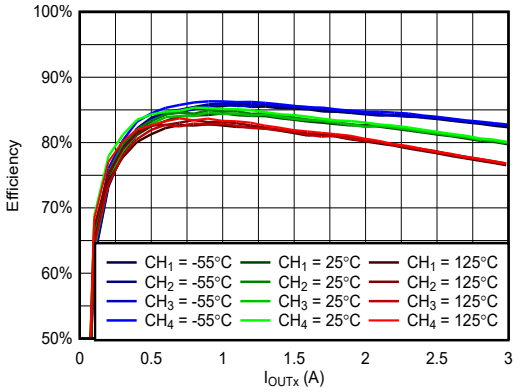


Figure 6-44. Efficiency vs Load at VIN = 5V,V_{OUTx} = 1.5V, f_{SW} = 1MHz

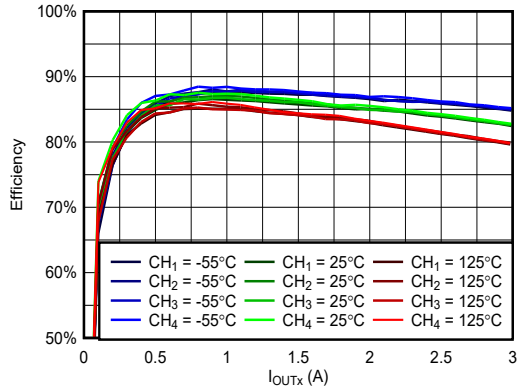


Figure 6-45. Efficiency vs Load at VIN = 5V,V_{OUTx} = 1.8V, f_{SW} = 1MHz

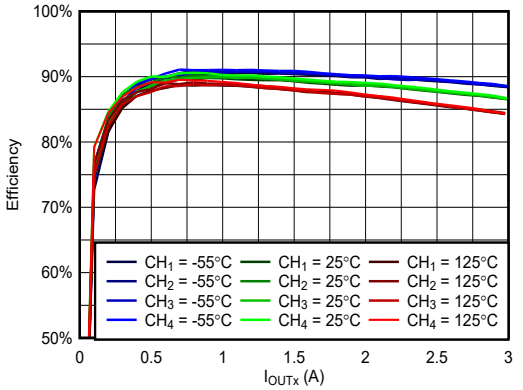


Figure 6-46. Efficiency vs Load at VIN = 5V,V_{OUTx} = 2.5V, f_{SW} = 1MHz

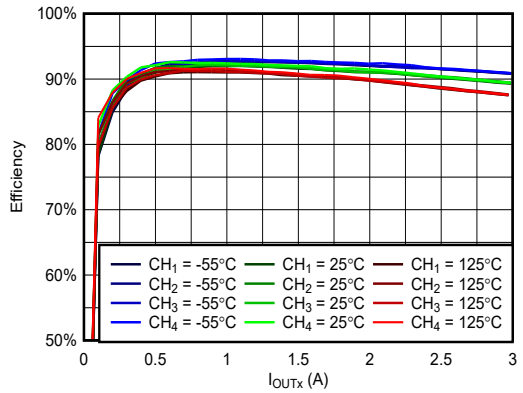


Figure 6-47. Efficiency vs Load at VIN = 5V,V_{OUTx} = 3.3V, f_{SW} = 1MHz

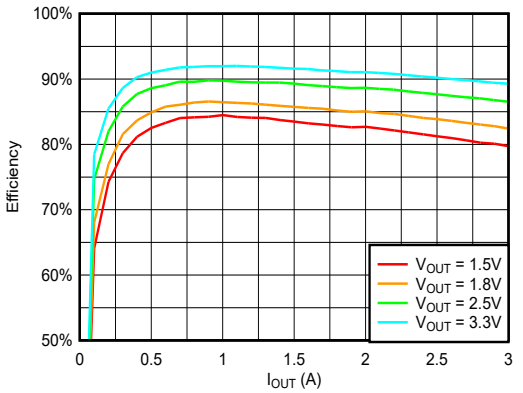


Figure 6-48. Efficiency vs Load at VIN = 5V, Across V_{OUT} at f_{SW} = 1MHz for Channel # 1 at 25℃

6.7 Typical Characteristics (continued)

PVIN = VIN, REFCAP = 470nF, L=3.3µH (model: MPX1D1250L3R3), unless otherwise noted.

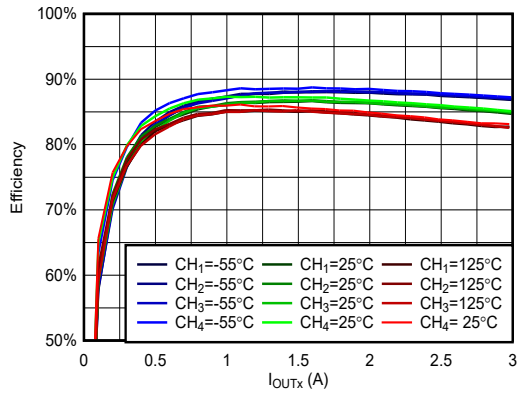


Figure 6-49. Efficiency vs Load at VIN = 7V,V_{OUTx} = 2.5V, f_{SW} = 1MHz

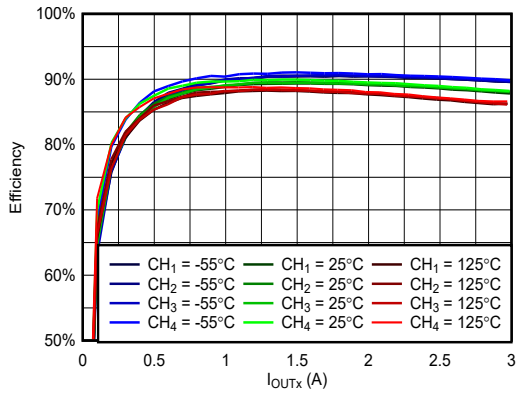


Figure 6-50. Efficiency vs Load at VIN = 7V,V_{OUTx} = 3.3V, f_{SW} = 1MHz

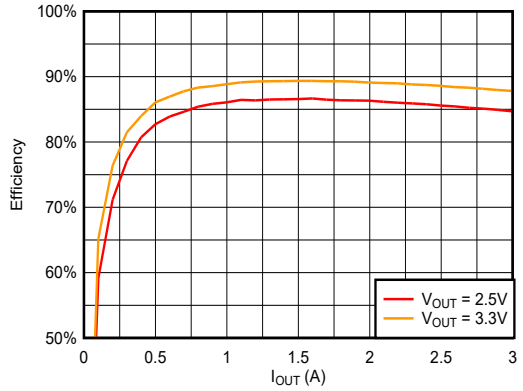


Figure 6-51. Efficiency vs Load at VIN = 7V, Across V_{OUT} at f_{SW} = 1MHz for Channel # 1 at 25℃

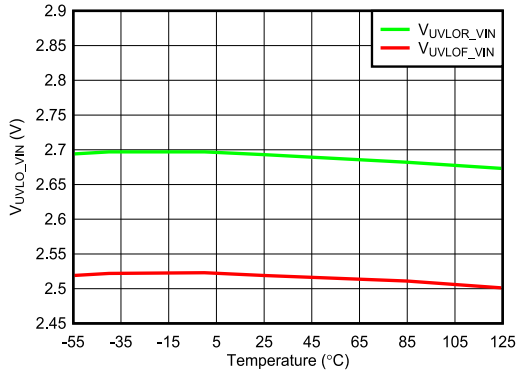


Figure 6-52. RISING and FALLING VIN UVLO Threshold vs Temperature

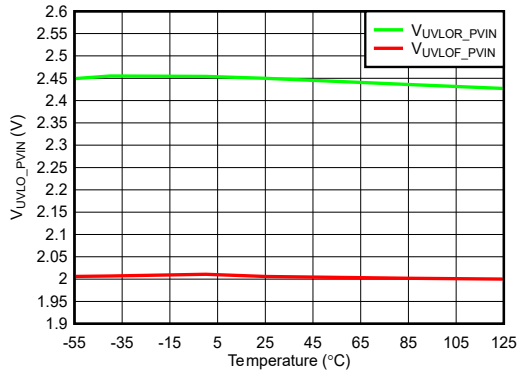


Figure 6-53. RISING and FALLING PVIN UVLO vs Temperature

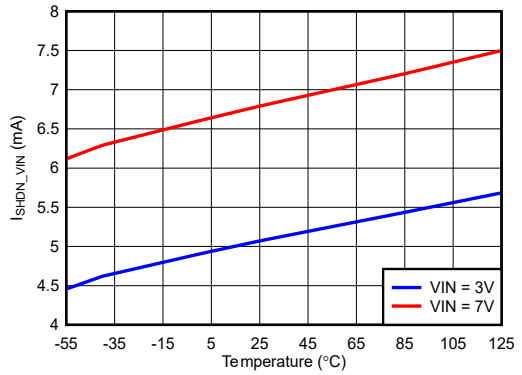


Figure 6-54. VIN Shutdown Current vs Temperature

6.7 Typical Characteristics (continued)

PVIN = VIN, REFCAP = 470nF, L=3.3µH (model: MPX1D1250L3R3), unless otherwise noted.

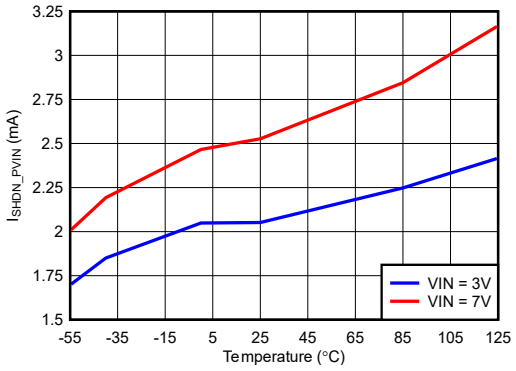


Figure 6-55. PVIN Shutdown Current vs Temperature

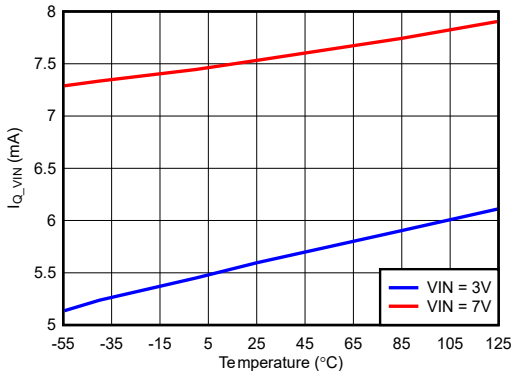


Figure 6-56. VIN Quiescent Current vs Temperature

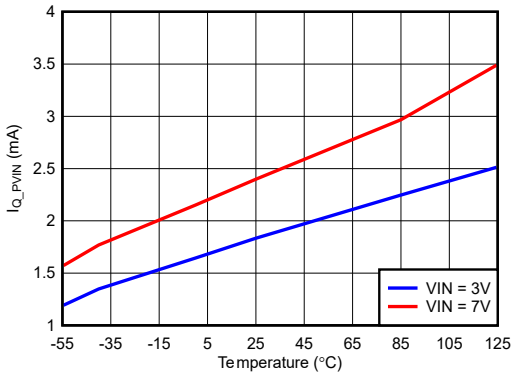


Figure 6-57. PVIN Shutdown Current vs Temperature

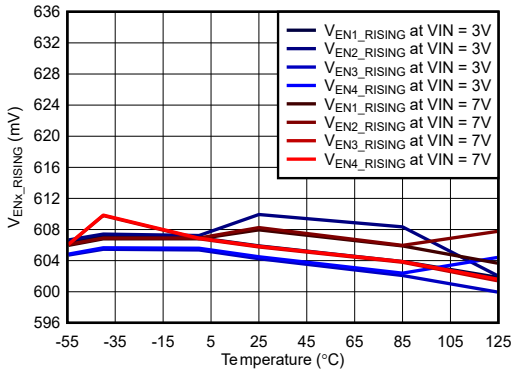


Figure 6-58. EN Rising Threshold vs Temperature

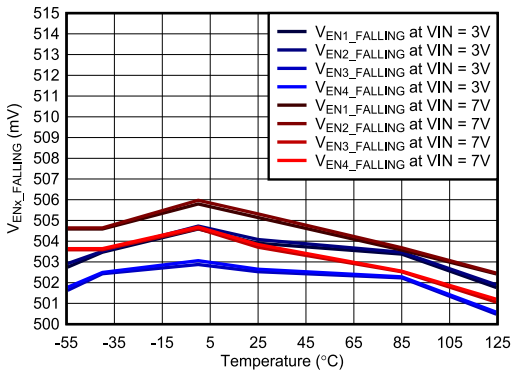


Figure 6-59. EN Falling Threshold vs Temperature

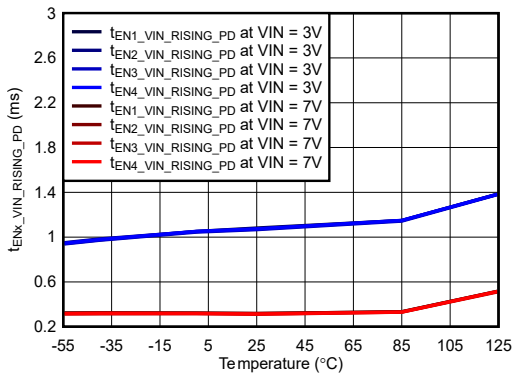


Figure 6-60. EN Rising Voltage Propagation Delay when EN is tied to VIN vs Temperature

6.7 Typical Characteristics (continued)

PVIN = VIN, REFCAP = 470nF, L=3.3µH (model: MPX1D1250L3R3), unless otherwise noted.

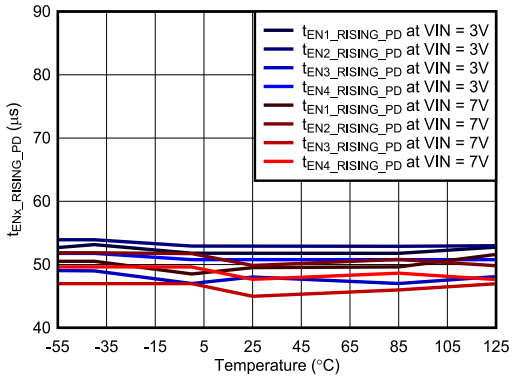


Figure 6-61. EN Rising Voltage Propagation Delay vs Temperature

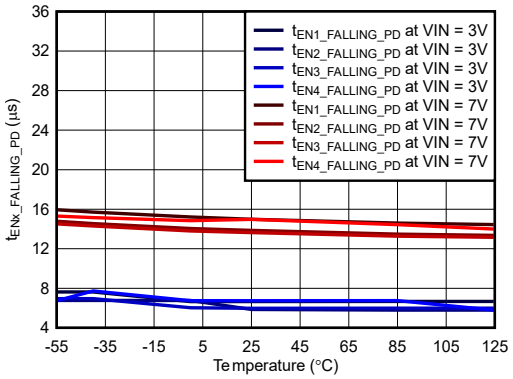


Figure 6-62. EN Falling Voltage Propagation Delay vs Temperature

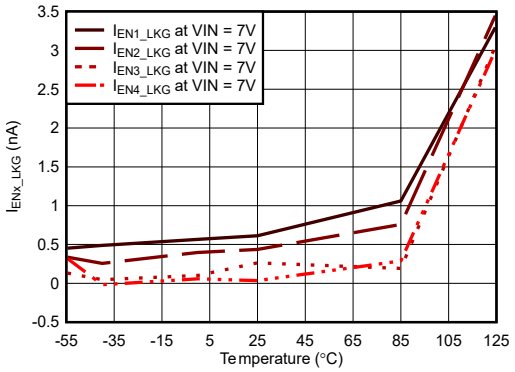


Figure 6-63. EN Leakage Current vs Temperature

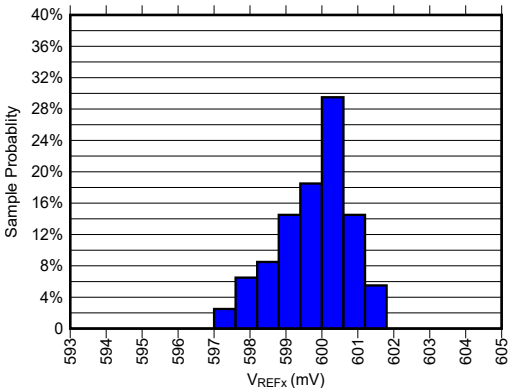


Figure 6-64. VREFx Voltage Distribution at Temperature of -55℃

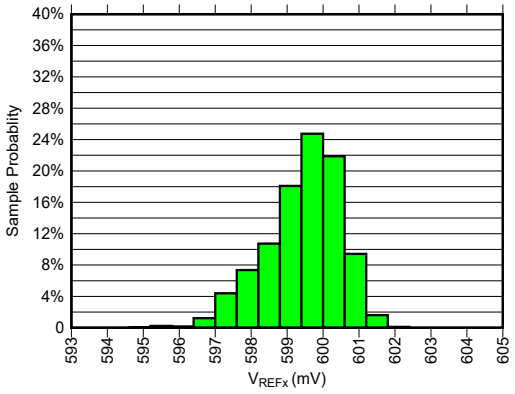


Figure 6-65. VREFx Voltage Distribution at Temperature of 25℃

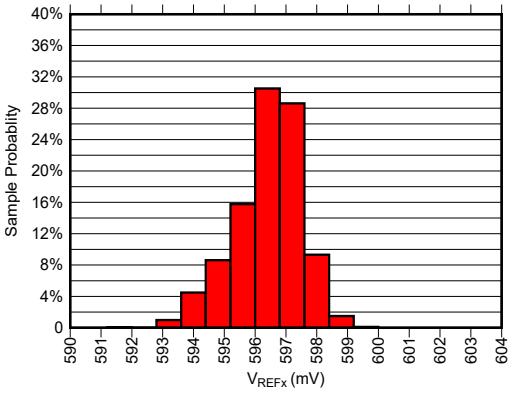


Figure 6-66. VREFx Voltage Distribution at Temperature of 125℃

6.7 Typical Characteristics (continued)

PVIN = VIN, REFCAP = 470nF, L=3.3µH (model: MPX1D1250L3R3), unless otherwise noted.

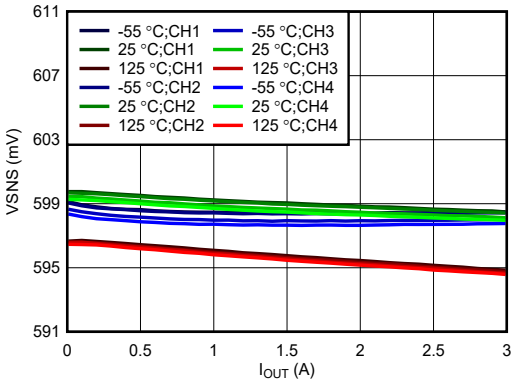


Figure 6-67. VSNS vs Load at f_{SW}=500kHz

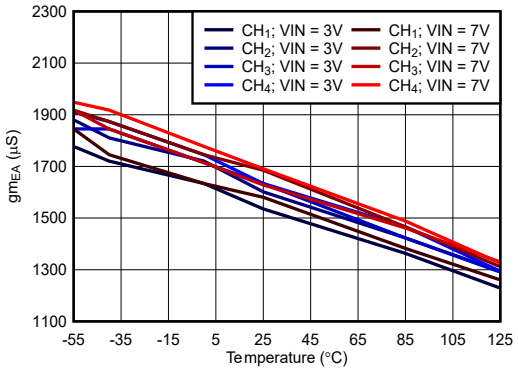


Figure 6-68. Error Amplifier Transconductance vs Temperature

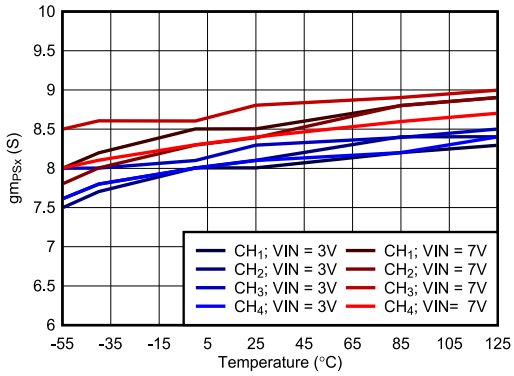


Figure 6-69. Power Stage Transconductance vs Temperature

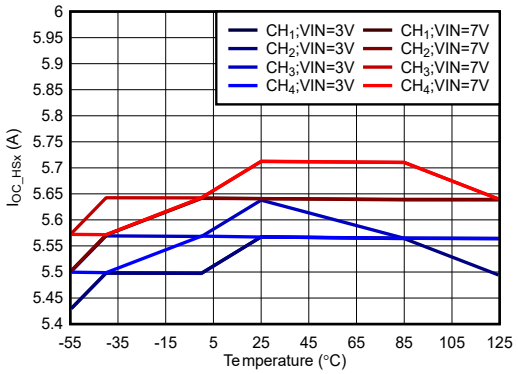


Figure 6-70. High Side Switch Overcurrent Threshold vs Temperature

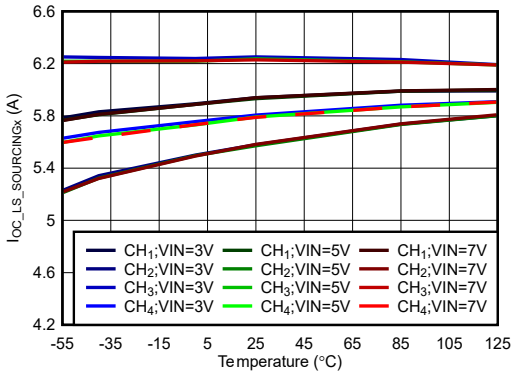


Figure 6-71. Low Side Sourcing Switch Overcurrent Threshold vs Temperature

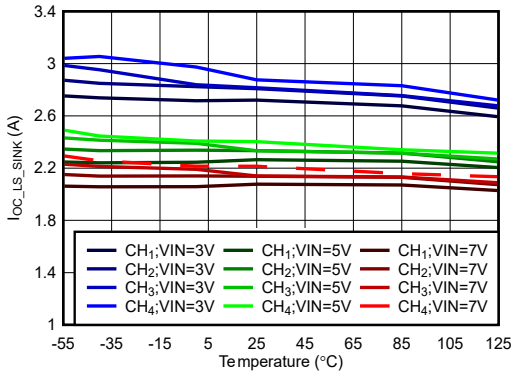


Figure 6-72. Low Side Sinking Switch Overcurrent Threshold vs Temperature

6.7 Typical Characteristics (continued)

PVIN = VIN, REFCAP = 470nF, L=3.3µH (model: MPX1D1250L3R3), unless otherwise noted.

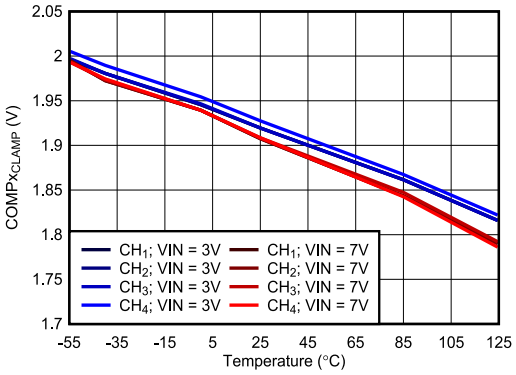


Figure 6-73. COMPx Clamp Voltage vs Temperature

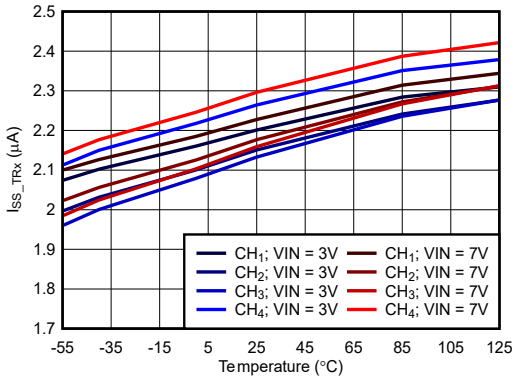


Figure 6-74. Soft Start Charge Current vs Temperature

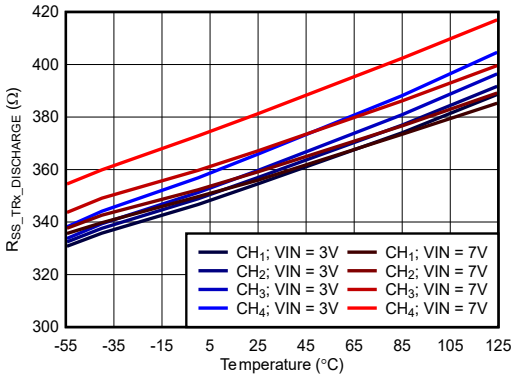


Figure 6-75. Soft Start Discharge Pull-Down Resistor vs Temperature

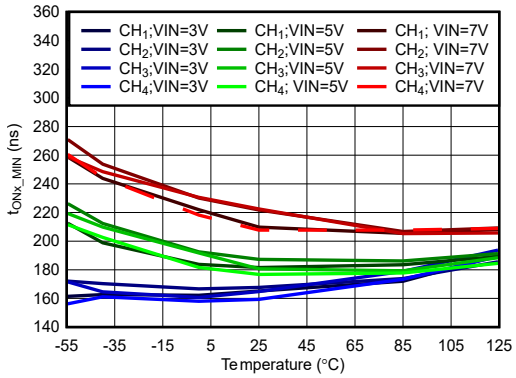


Figure 6-76. Minimum On Time vs Temperature

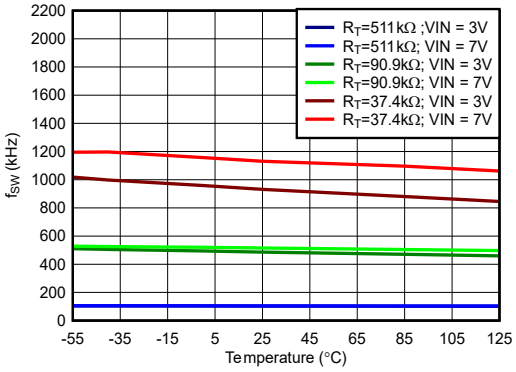


Figure 6-77. RT programmed switching frequency

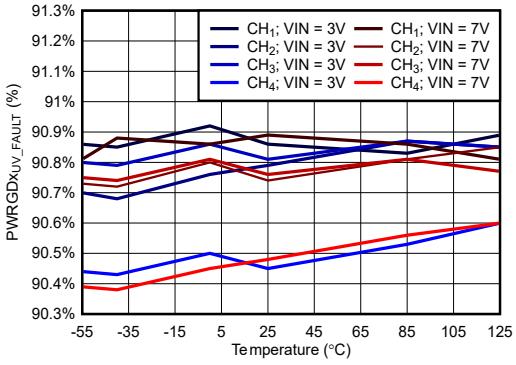


Figure 6-78. VSNSx Falling Threshold for PWRGD Fault vs Temperature

6.7 Typical Characteristics (continued)

PVIN = VIN, REFCAP = 470nF, L=3.3µH (model: MPX1D1250L3R3), unless otherwise noted.

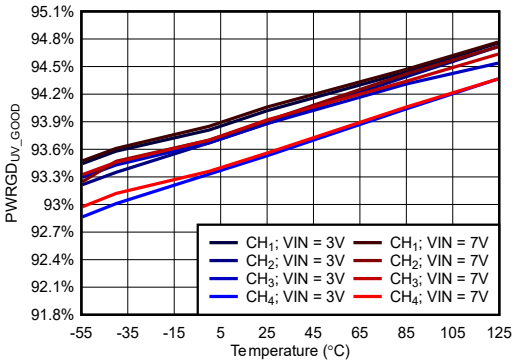


Figure 6-79. VSNSx Rising Threshold for PWRGD Good vs Temperature

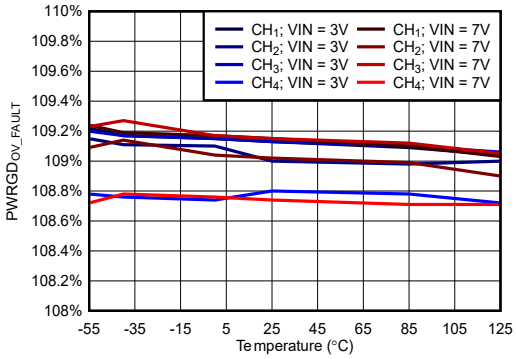


Figure 6-80. VSNSx Rising Threshold for PWRGD Fault vs Temperature

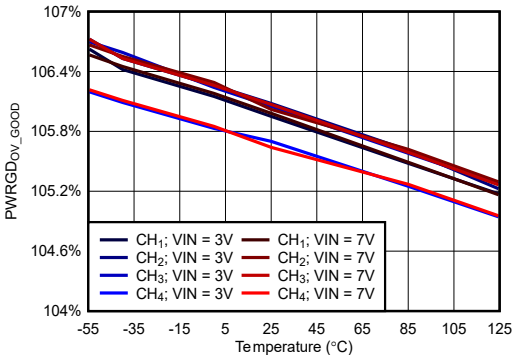


Figure 6-81. VSNSx Falling Threshold for PWRGD Good vs Temperature

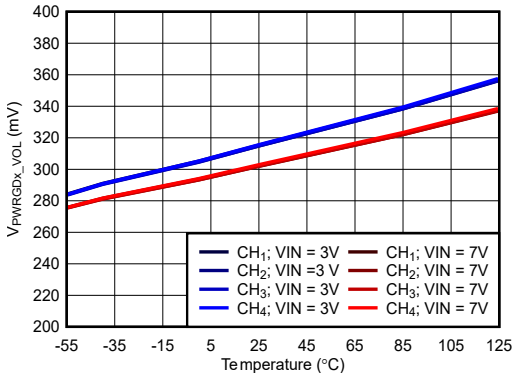
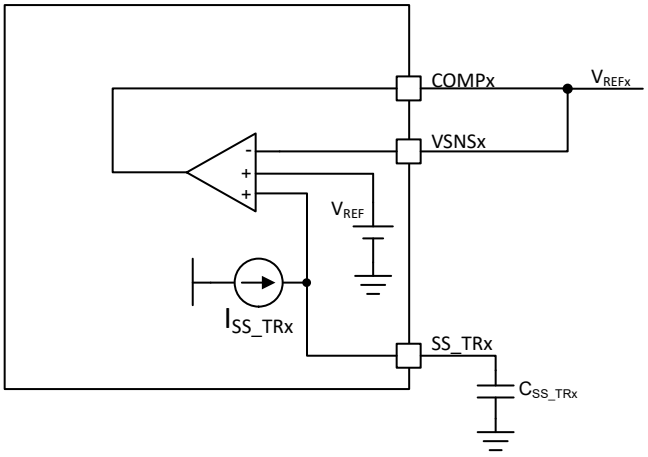


Figure 6-82. Power Good Output Low Voltage vs Temperature

7 Parameter Measurement Information



A. This accurate reference voltage value includes the error amplifier offset, V_{IOx}. Use this value to set the output voltage. This measurement is done across all four channels.

Figure 7-1. Reference Voltage Measurement (V_{REFx})

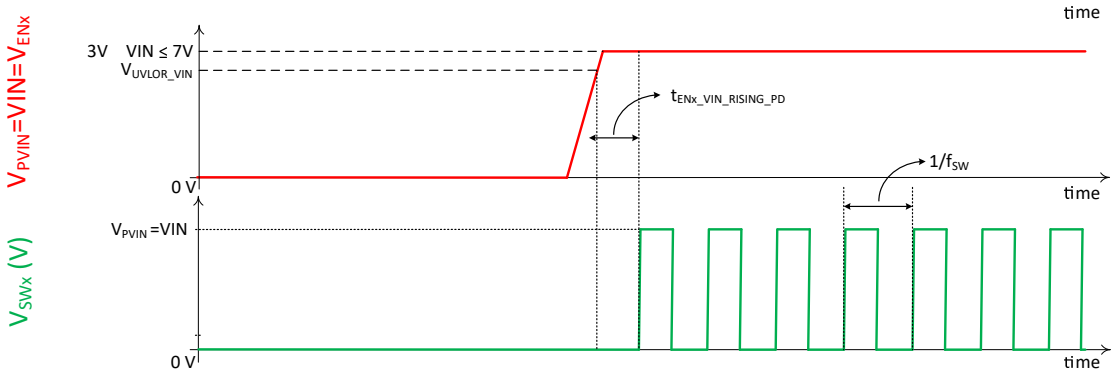


Figure 7-2. Rising Enable Propagation Delay When ENx is Tied to PVIN = VIN ($t_{ENx\_VIN\_RISING\_PD}$)

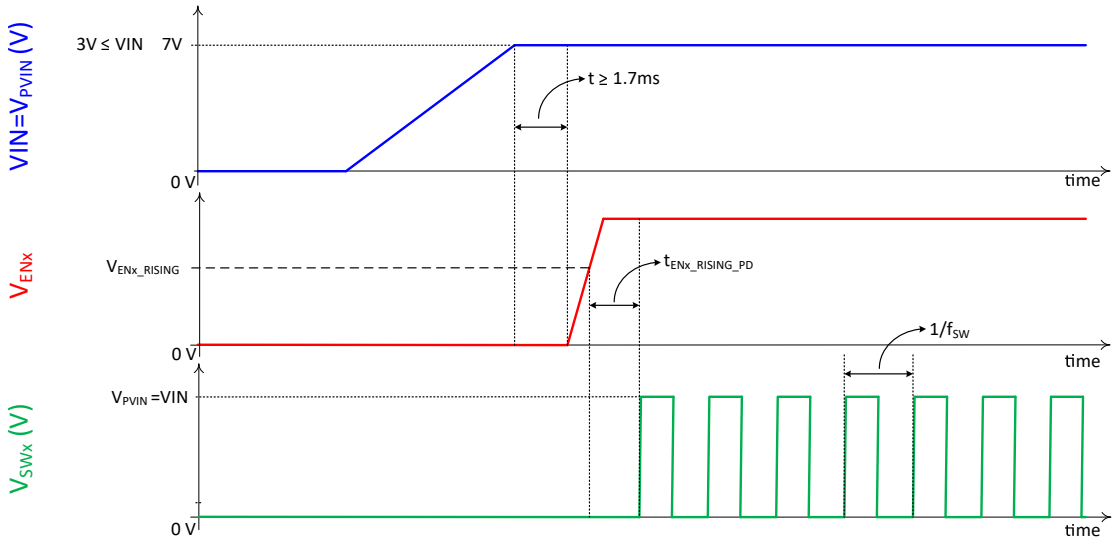


Figure 7-3. Rising Enable Propagation Delay When ENx is Driven Independently From PVIN = VIN ($t_{ENx\_RISING\_PD}$)

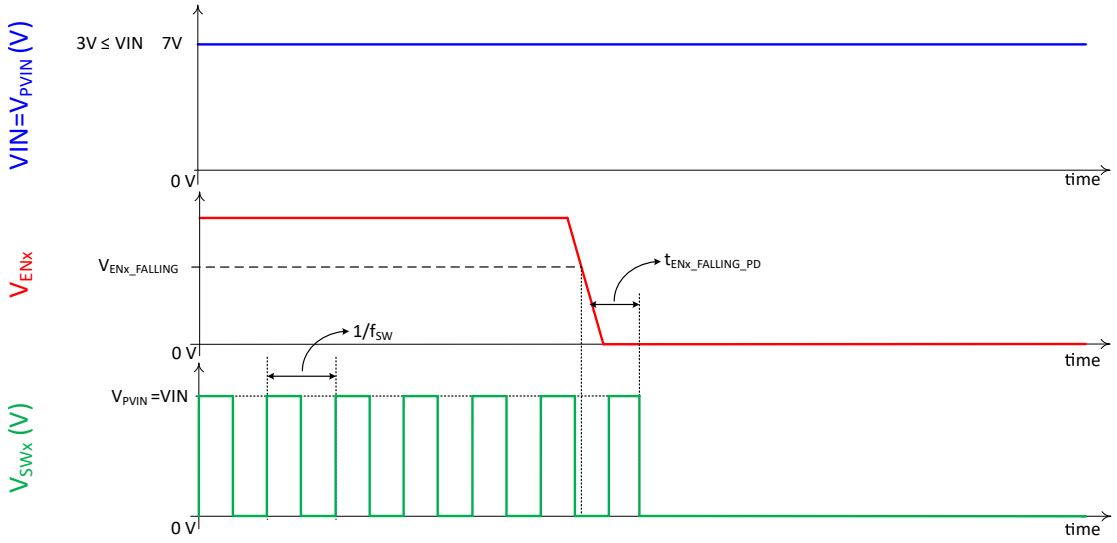


Figure 7-4. Falling Enable Propagation Delay ($t_{ENx\_FALLING\_PD}$)

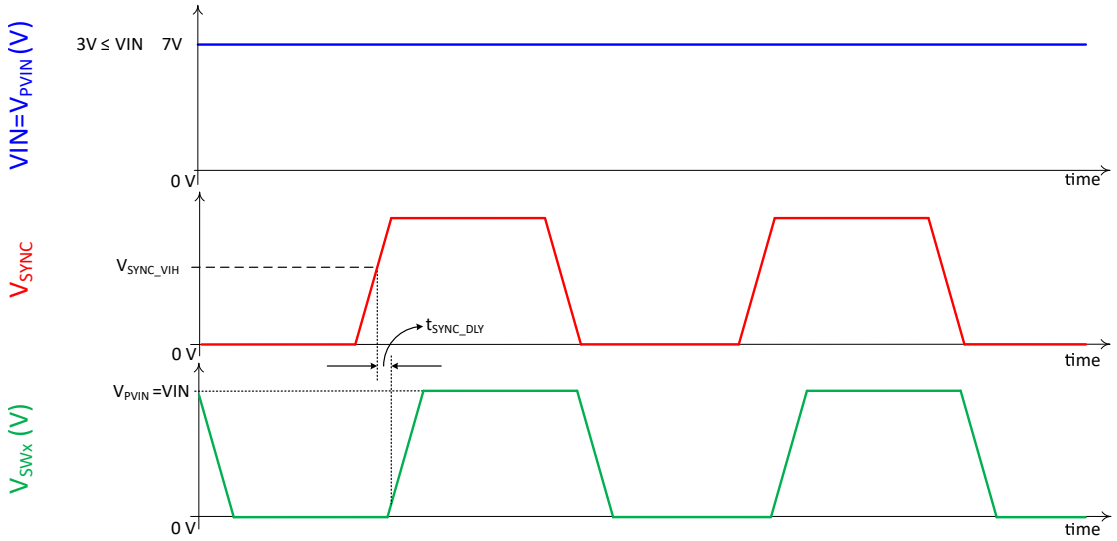


Figure 7-5. SYNC to SWITCH Delay (t_{SYNC_DLY})

8 Detailed Description

8.1 Overview

The TPS7H4104 and TPS7H4102 devices are: 3V to 7V, 3A/channel, quad/dual channel, synchronous step-down (buck) converter. Each channel has two integrated MOSFETs, a PMOS for the high side, and an NMOS for the low side. Each channel also has independent:

- Power good flag (PWRGDx).
- Programmable slope compensation (RSCx).
- Programmable soft-start (SSx).
- Low logic compatible enable inputs (ENx).

Each channel can be used independently or interleaved to service loads greater than 3A, up to 12A for the TPS7H4104 and 6A for the TPS7H4102. Each phase is internally operated at a relative fixed phase-shift of 90 degrees. The channels on the top and bottom both have a 180 degrees phase shift between them for interleaving of dual/single 6A channel.

Note

For the purpose of this document the x at the end of a signal name is used to generalize all possible values the signal can take, x can take a value from 1 to 4 (used to specify the channel in discussion). If a signal does not contain an x or a given value (between 1 to 4) at the end, the signal is a shared (or global) signal to all channels. For example the signals: VIN, PVIN, RT, SYNC, EN_SEQ (only valid for the TPS7H4104), GND, PGND and REFCAP are all signals common to all channels.

To improve performance during line and load transients, the device implements a constant frequency, peak current mode (PCM) control, which also simplifies external frequency compensation. The wide switching frequency range (100kHz to 1MHz) allows for efficiency and size optimization when selecting the output filter components (L_x & C_{OUTx}). The MOSFETs have been sized to optimize efficiency for lower duty cycle applications.

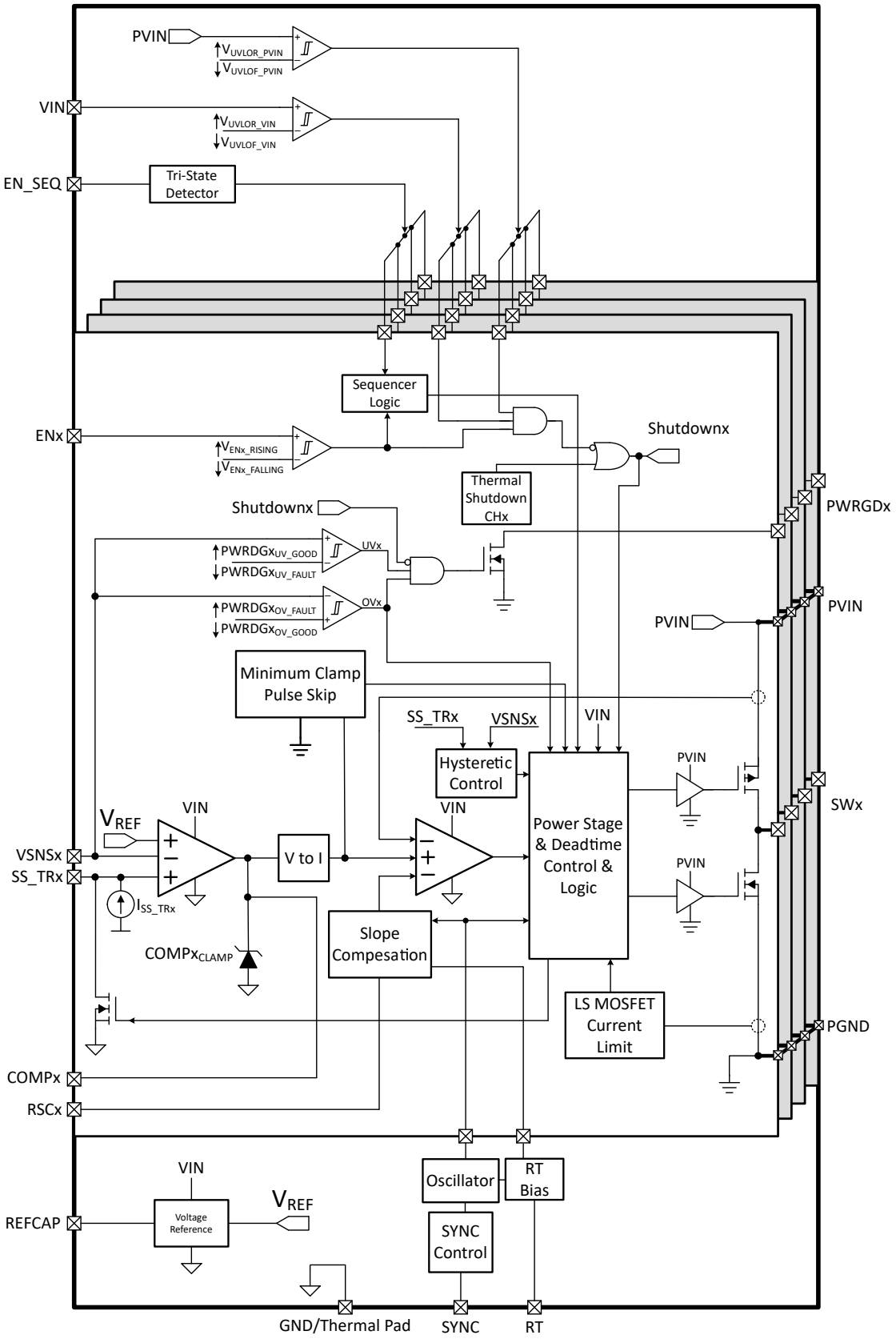
The device is designed for safe monotonic start-up into pre-biased loads. The default start-up is when VIN is greater than 2.7V (typ.). Each channel incorporates an independent enable signal (ENx). This pins are connected to the non-inverting input of a voltage comparator with hysteresis (typically 106mV). The maximum combined (VIN + PVIN) operating current for the TPS7H4104 is 12mA with all channels disabled and 18.7mA with all channels enabled and non-switching.

The device incorporates a power-good comparator (PWRGDx) with hysteresis, which monitors the output voltage through the VSNSx (or feedback) pin. The PWRGDx pin is an open-drain NMOS MOSFET, which is pulled low when the VSNSx pin voltage is less than 91% (typ.) or greater than 109% (typ.) of the internal voltage reference (V_{REFx}) and asserts high (trough an external pull-up) when the VSNSx pin voltage is between 94% to 106% of V_{REFx} (typical).

The SS_TRx (soft-start/tracking) pins are used to minimize inrush current (during start-up, when C_{OUTx} is discharged) or provide power-supply sequencing during power-up. A small-value capacitor or resistor divider can be connected to the pin for soft-start or critical power-supply sequencing requirements. During start-up, if VSNSx is greater than the voltage at SS_TRx, the device enters into a pulse-skipping mode. This happens due to the minimum on-time (t_{ONx_MIN} = 182ns typ. at VIN = 5V).

The device is protected from output over-voltage, overload, and thermal fault conditions. The device minimizes excessive output over-voltage transients by taking advantage of the over-voltage circuit in the power-good comparators. When the over-voltage comparator is activated, the high-side MOSFET is turned off and prevented from turning on until the VSNSx pin voltage is lower than 106% of the V_{REFx}. The device implements both high-side MOSFET overload protection and bidirectional low-side MOSFET overload protections, which help control the inductor current and avoid current runaway. The device also shuts down if any channel junction temperature is higher than thermal shutdown trip point, typically 163°C. The device is restarted under control of the soft-start circuit automatically when the junction temperature drops 29°C (typ.) below the thermal shutdown trip point.

8.2 Functional Block Diagram



8.3 Feature Description

8.3.1 VIN and Power VIN Pins (VIN and PVIN)

The VIN pin provides power to internal control circuitry. The PVIN pins provide the input voltage (and power to the loads) to all the internal half-bridges (CH # 1 to CH # 4). Both pins have an input voltage range of 3V to 7V. The pins must be at the same nominal voltage and they must power up and power down at the same time. Generally this is achieved by providing them from the same voltage source (tied together).

Both VIN and PVIN have individual UVLO (under voltage lockout) rising thresholds, V_{UVLOR_VIN} (2.7V typ.) and V_{UVLOR_PVIN} (2.44V typ.), respectively. This is to make sure the device internal bias is sufficient for proper operation. Additionally, VIN and PVIN have individual UVLO falling thresholds, V_{UVLOF_VIN} (2V typ.) and V_{UVLOF_PVIN} (2.52V typ.), respectively. If the voltage falls and these values are reached, the device turns off. As PVIN and VIN are tied together in the application, the dominant UVLO for the device (or I.C.) will be the VIN UVLO as is the higher threshold value during a rising and falling voltage.

If desired, the user can adjust the effective UVLO by using an external resistive voltage divider, connected between VIN and ENx. For more details refer to Section 8.3.4.1.

Note

In the TPS7H4102 the PVIN pins 17, 18, 31 and 32 do not conduct much current with a maximum of 2.27mA. For this reason the pins do not need to be connected to a plane, rather a trace is sufficient.

8.3.2 Voltage Reference

The device generates an internal nominal 1.235V bandgap reference voltage, V_{REFCAP}. This is the voltage present on the REFCAP pin during steady state operation. A 470nF capacitor to ground is required at the REFCAP pin for proper electrical operation as well as to provide robust SET performance of the device. This bandgap voltage is used to derive the reference voltage for the error amplifier, common to the four error amplifiers.

The reference voltage that is fed into the error amplifier is utilized to set the output voltage. However, error amplifiers have an intrinsic offset, which contribute to the overall accuracy error. V_{REFx} is measured with the error amplifier in unity gain, such the measurement includes the offset error. V_{REFx} is typically 599.48mV at 25°C and is designed to be accurate to ± 1% across line (input voltage), temperature and TID. Because V_{REFx} is measured in an open loop configuration, the effects of switching frequency and load are not included in the specification. However, these effects are minimal when compared to the already considered effects.

8.3.3 Setting V_{OUTx}

The output voltage is set with a resistor voltage divider. From the output voltage node (V_{OUTx}) into the VSNSx pin a top resistor is connected, and from VSNSx to GND the bottom resistor. Refer to Figure 8-1 for connection configuration. TI recommends to use 0.1% tolerance resistors.

Start with a 10kΩ for R_{F_TOPx} and use Equation 1 to calculate the bottom feedback resistance (R_{F_BOTx}). To improve efficiency at light loads, consider using larger-value resistors. If the values are too high, the regulator is more susceptible to noise and to output voltage errors from VSNSx input current.

$$R_{F\_BOTx} = \left(\frac{V_{REFx}}{V_{OUTx\_TARGET} - V_{REFx}}\right) \times R_{F\_TOPx} \quad (1)$$

where:

- V_{REFx}= 599.48mV (typ. at 25°C) .
  - For more details on the V_{REFx} refer to *VOLTAGE REFERENCE* section in Section 6.5.
  - If desired to minimize the output voltage error across temperature we can re-center the reference as:

$$V_{REFx} = \frac{V_{REFx(MIN)} + V_{REFx(MAX)}}{2} = 597.5mV \quad (2)$$

- V_{OUTx_TARGET} is the desired nominal output voltage.
- R_{F_TOPx} is the selected top resistor for the resistive voltage divider.

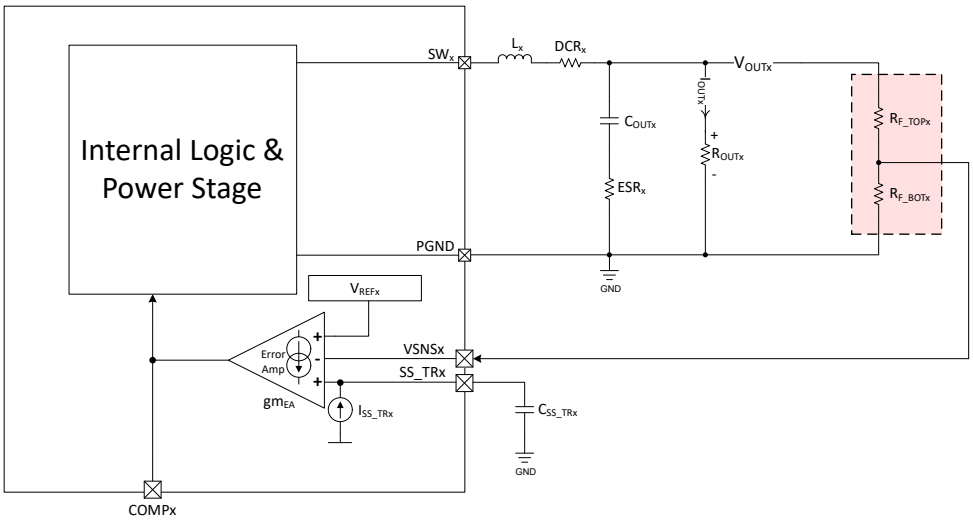


Figure 8-1. V_{OUTx} programming with Resistive Divider

8.3.3.1 V_{OUTx} with Error

Once the top and bottom resistors are known, the expected nominal output voltage using Equation 3 cn be calculated. As the reference and the resistor values have deviations from the nominal values (or uncertainties), the designer can calculate the expected output voltage error using Equation 4. Equation 4 was derived using the derivative method, and assumes the error variables are uncorrelated, and both resistors (R_{F_TOPx} and R_{F_BOTx}) have the same tolerance. The real output voltage range can be calculated using Equation 5.

$$V_{OUTx\_NOMINAL} = \left(1 + \frac{R_{F\_TOPx}}{R_{F\_BOTx}}\right) \times V_{REFx} \tag{3}$$

$$V_{OUTx\_ERROR}\ (V) = \pm \sqrt{\frac{V_{REFx}^2 \times \left[\left(2 \times R_{TOL}^2 \times R_{F\_TOPx}^2\right) + \left(V_{REFx\_ACC}^2 \times \left(R_{F\_TOPx} + R_{F\_BOTx}\right)^2\right)\right]}{R_{F\_BOTx}^2}} \tag{4}$$

$$V_{OUTx\_REAL} = V_{OUTx\_NOMINAL} \pm V_{OUTx\_ERROR} \tag{5}$$

where:

- R_{F_TOPx} is the selected top resistor for the resistive voltage divider in Ohms (Ω).
- R_{F_BOTx} is the selected bottom resistor for the resistive voltage divider in Ohms (Ω).
- V_{REFx} = 599.48mV (typ. at 25°C) or 598.39mV (center across temperature).
- V_{REFx_ACC} is the reference accuracy as a numeric value (0.01). The accuracy across voltage and temperature is ± 1%, for more details refer to *VOLTAGE REFERENCE* in Section 6.5.
- R_{TOL} is the resistor tolerance (same for the top and bottom resistors) as a numeric value. For example, for a 0.1% tolerance resistors, we use 0.001.

8.3.3.2 Minimum Output Voltage

Due to internal leading edge blanking time, internal circuitry propagation delays, and internal reference voltage (V_{REFx}), there exist a minimum achievable output voltage (V_{OUTx}). The minimum output voltage is calculated as:

$$V_{OUTx\_MIN} \cong \begin{cases} V_{IN} \times t_{ONx\_MIN} \times f_{SW}, \ if \ \geq V_{REFx} \\ V_{REFx}, \ Otherwise \end{cases} \quad (6)$$

Where:

- V_{OUTx_MIN} is the minimum achievable output voltage
- V_{IN} is the input voltage of the I.C. (same as PVIN)
- t_{ONx_MIN} is the minimum on-time
  - Refer to *MINIMUM ON, OFF and DEAD TIM E* section in Section 6.5 for more details.
- f_{SW} is the switching frequency
  - Refer to *SWITCHING FREQUENCY AND SYNCHRONIZATION* section in Section 6.5 for more details.
- V_{REFx} is the internal reference voltage
  - Refer to *VOLTAGE REFERENCE* section in Section 6.5 for more details.

Table 8-1 shows the calculated minimum output voltage at selected cases of V_{IN} and f_{SW}.

Table 8-1. Calculated Minimum Output Voltages

f_{SW} (kHz)	V_{IN} (V) (4)	V_{OUTx_MIN} (V)
100 (1)	3	V_{REFx} (5)
	5	
	7	
500 (2)	3	
	5	0.761
	7	1.263
1000 (3)	3	0.983
	5	1.701
	7	2.822

(1) The maximum switching frequency value for R_{RT} = 511kΩ was used for the calculation.
(2) The maximum switching frequency value for R_{RT} = 90.9kΩ was used for the calculation.
(3) The maximum switching frequency value for R_{RT} = 37.4kΩ was used for the calculation.
(4) The maximum value for the t_{ONx_MIN} for the specified voltage was used for the calculation.
(5) V_{REFx} is the internal reference voltage.

8.3.3.3 Maximum Output Voltage

The TPS7H410x has a maximum output voltage due to the minimum off time, t_{OFFx_MIN}. This minimum off time is not due to the re-charge rate of the bootstrap capacitor like in NMOS/NMOS buck regulators. Instead, the minimum off time is to make sure switching noise and internal circuitry behavior does not cause excessive duty cycle jitter. The maximum output voltage is approximated by Equation 7

$$V_{OUTx\_MAX} \cong V_{IN} \times \left[1 - \left(t_{OFF_{MIN}} \times f_{SW}\right)\right] \quad (7)$$

Where:

- V_{OUTx_MAX} is the maximum achievable output voltage
- V_{IN} is the input voltage of the I.C. (same as PVIN)
- t_{OFFx_MIN} is the minmum off-time
  - Refer to *MINIMUM ON, OFF and DEAD TIME* section in Section 6.5 for more details.
- f_{SW} is the switching frequency
  - Refer to *SWITCHING FREQUENCY AND SYNCHRONIZATION* section in Section 6.5 for more details.

Table 8-2 shows the calculated maximum output voltage at selected cases of V_{IN} and f_{SW}.

Table 8-2. Calculated Maximum Output Voltages

f_{SW} (kHz)	V_{IN} (V) (4)	V_{OUTx_MAX} (V)
100 (1)	3	2.922
	5	4.870
	7	6.819
500 (2)	3	2.635
	5	4.391
	7	6.147
1000 (3)	3	2.184
	5	3.639
	7	5.095

(1) The maximum switching frequency value for R_{RT} = 511kΩ was used for the calculation.
(2) The maximum switching frequency value for R_{RT} = 90.9kΩ was used for the calculation.
(3) The maximum switching frequency value for R_{RT} = 37.4kΩ was used for the calculation.
(4) The typical value for the t_{OFFx_MIN} = 216ns was used for the calculation

8.3.4 Enable and EN_SEQ

8.3.4.1 ENx and External UVLO

The ENx pins provide an electrical on/off control for each CHx (or V_{OUTx}). The ENx pins are connected to the non-inverting input of a comparator with hysteresis (106mV typ.). When the enable pin is low [$V_{ENx} < V_{ENx\_FALLING\ (MIN)}$], the device enters in shutdown mode and does not regulate the output voltage (V_{OUTx}) for the selected channel (x). To turn on a given channel the enable pin needs to be forced to a logic high [$V_{ENx} > V_{ENx\_RISING\ (MAX)}$]. Each ENx pin is independent and controls only the specified CHx (or V_{OUTx}).

If desired, the user can adjust the individual turn-on voltages for each channel by connecting a resistive divider between VIN and GND to feed into the ENx pin as presented on Figure 8-2. The resistors can be appropriately sized to turn on the device when a desired preset input voltage is reached.

Note

The user can program the rising voltage UVLO, the falling voltage is dictated by the comparator hysteresis. The selected rising voltage UVLO needs to be greater than the maximum V_{UVLOR_VIN} specification of 2.83V.

To program an external UVLO for the desired channel (CHx), follow these steps:

1. Select the desired rising voltage UVLO ($V_{UVLO\_CHx\_TARGET}$)
2. Select the top resistor value for the resistive voltage divider (R_{ENx_TOP}).
   - A good starting value is 10kΩ. Greater values can be used on the application to minimize power consumption. However this comes at the expense of greater susceptibility to noise, also the error associated with the ENx leakage (I_{ENx_LKG}) becomes more noticeable
3. Calculate the bottom resistor for the resistive voltage divider (R_{ENx_BOT}) using Equation 8.
4. Select the closest value to minimize error.
5. Calculate the nominal rising and falling UVLO for the desired channel using Equation 9 and Equation 10

$$R_{ENx\_BOT\_CALCULATED} = \left(\frac{V_{ENx\_RISING}}{V_{UVLO\_CHx\_TARGET} - V_{ENx\_RISING}}\right) \times R_{ENx\_TOP} \quad (8)$$

$$V_{UVLO\_CHx\_RISING} = \left(1 + \frac{R_{ENx\_TOP}}{R_{ENx\_BOT}}\right) \times V_{ENx\_RISING} \quad (9)$$

$$V_{UVLO\_CHx\_FALLING} = \left(1 + \frac{R_{ENx\_TOP}}{R_{ENx\_BOT}}\right) \times V_{ENx\_FALLING} \quad (10)$$

where:

- $R_{ENx\_BOT\_CALCULATED}$ is the calculated bottom resistor to set the external UVLO at $V_{UVLO\_CHx\_TARGET}$.
- $V_{UVLO\_CHx\_RISING}$ is the nominal externally programmed rising input voltage UVLO.
- V_{ENx_RISING} = 0.606V (typ.)
- $V_{UVLO\_CHx\_FALLING}$ is the nominal externally programmed falling input voltage UVLO.
- $V_{ENx\_FALLING}$ = 0.5V (typ.)
- R_{ENx_TOP} is the selected top resistor value connected from VIN to ENx
- R_{ENx_BOT} is the selected bottom resistor value connected from ENx to GND

Alternatively, the ENx pin can be driven directly from a microcontroller or FPGA. The low voltage threshold of the enable pin aids in support of 1.1V, 1.8V, 2.5V, and 3.3V logic levels.

If needed, a small capacitor can be placed in parallel with ENx and GND as shown in Figure 8-2. This capacitor can be used to:

- Minimize Noise in the ENx voltage.
- Filter fast transients that otherwise can turn on/off the channel.
- Delay the turn-on of the channel (CHx).

If desired, the designer can use Equation 11 to calculate the necessary capacitor to delay the turn-on of a given channel (x).

$$C_{EN\_DELAY}\left(F\right) = \frac{t_{DELAY}(s)}{R_{TH}\left(\Omega\right) \times \ln\left(-\frac{V_{TH}(V)}{V_{ENx\_RISING} - V_{TH}(V)}\right)} \quad (11)$$

where:

- t_{DELAY} is the desired delay time in seconds.
- R_{TH} is the Thévenin equivalent resistance. In this case the parallel between R_{ENx_TOP} and R_{ENx_BOT} in ohms (Ω).
  - $$R_{TH}\left(\Omega\right) = \frac{R_{ENx\_TOP}(\Omega) \times R_{ENx\_BOT}(\Omega)}{R_{ENx\_TOP}(\Omega) + R_{ENx\_BOT}(\Omega)} \quad (12)$$
- V_{TH} is the Thévenin equivalent voltage. In this case the voltage at V_{ENx} during steady state operation in volts (V).
  - $$V_{TH}\left(V\right) = \left(\frac{R_{ENx\_BOT}(\Omega)}{R_{ENx\_TOP}(\Omega) + R_{ENx\_BOT}(\Omega)}\right) \times VIN\left(V\right) \quad (13)$$
- V_{ENx_RISING} is the rising ENx threshold to enable the device.

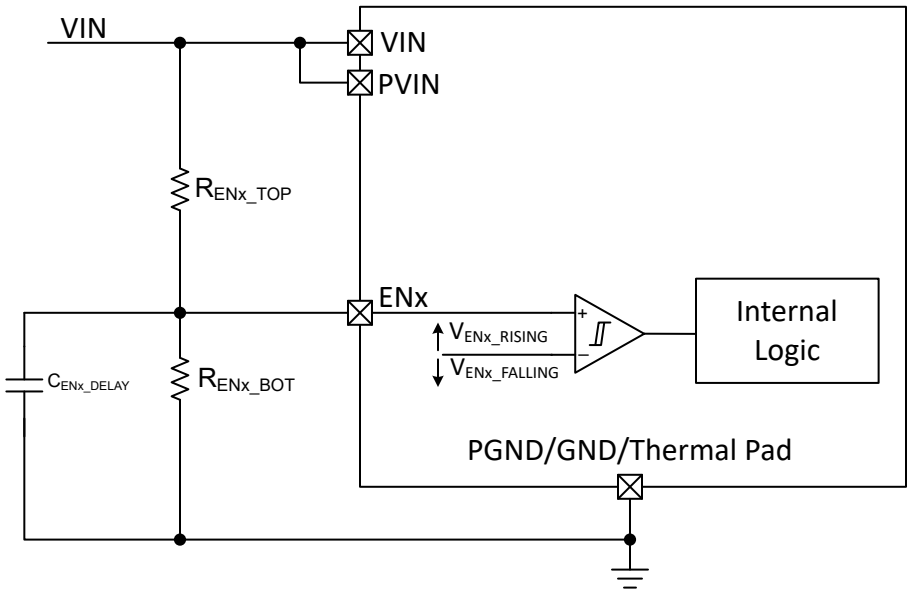


Figure 8-2. External UVLO using ENx with Resistive Divider

8.3.4.2 Sequence UP/DOWN (EN_SEQ)

In multichannel regulator systems it is often needed to sequence up and reverse sequence down the channels. The TPS7H4104 includes a sequence up (from CH1 to CH4) and reverse sequence down (CH4 to CH1) with fixed turn on/off thresholds for ease of use. *The sequence up and down is only valid when the used channels are operated independently*. This means the channels cannot be interleaved for proper sequence up and down.

Note

The TPS7H4102 does not offer the sequence up/down feature.

The on threshold is typically 87.4% of V_{REFx} (524mV in VSNSx), while the off threshold is typically 15.4%of V_{REFx} (92.28mV in VSNSx).

Note

The turn on/off voltages are referred as percentage (or ratio) of V_{REFx}, however V_{OUTx} is a scaled up version of V_{REFX} when the feedback loop is closed. For this reason it is equivalent to refer the ratios as a percent of V_{OUTx}.

A typical sequence up/down when all channels (ENx=logic high) is shown in Figure 8-3. During sequence up/down, channels with ENx logic low are skipped. As the internal sequence up/down logic uses the logical voltage level at ENx to determine if the channel is used during the sequencing, it is important to have a stable logic value on these pins before sending the logical sequence command to the EN_SEQ pin. The logic levels for EN_SEQ are a function of the input voltage (VIN) as:

- $V_{EN\_SEQ\_RISING}$ (V) >80% x VIN (V)
- $V_{EN\_SEQ\_FALLING}$ (V) < 17% x VIN (V)
- Open = No Sequencing
  - In this scenario the CHx turn on/off , follows the individual ENx logic levels.

The logical truth table for SEQ_EN is shown in Table 8-3.

Note

The V_{EN_SEQ} rise time and fall time must be greater or equal to 100ns for proper operation. When EN_SEQ is not used (EN_SEQ = OPEN) and SYNC is externally driven, at least 100pF between EN_SEQ and GND is required. Internally the EN_SEQ is biased with a resistive divider of two 200kΩ (typ.) in series. This impedance along with the capacitance creates a delay, that may impact the system start-up time. Refer Figure 8-4 for more details. The delay due to this capacitor can be calculated using: Equation 14

The sequencer logic is not synchronized to local faults. Faults can be classify as:

1. Local: faults or signals that affect only an specific channel (x), such as:
   - ENx
   - over-current
   - over-voltage
   - under-voltage
2. Global: faults that affect all channels simultaneously, such as:
   - Thermal shutdown
   - PVIN UVLO
   - VIN UVLO

When a local fault is detected in a given channel (x), the channel reacts accordingly without affecting any other channels. For example in a scenario where, after a complete sequence up, a hard-short (or overcurrent event) is detected in channel # 1, V_{OUT1} drops out of regulation; once the short is removed the voltage is regulated back accordingly. This behavior is not coupled to any other channels.

During a global fault all channels are disabled and the switch nodes are put into a high impedance mode. Once the fault is cleared and assuming EN_SEQ and all desired ENx are in a logical high state, the device starts the sequence up.

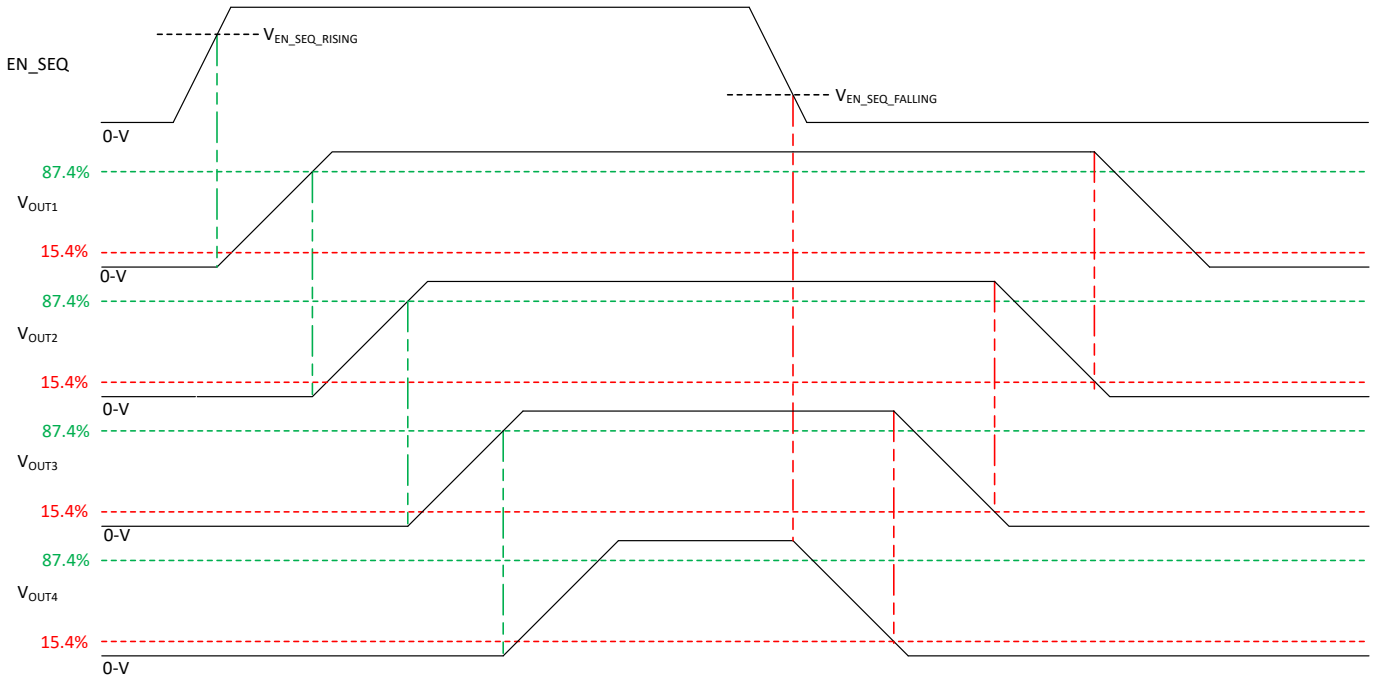


Figure 8-3. Sequence UP/DOWN

A. In this plot is assumed all ENx are logic high ($V_{ENx} > V_{ENx\_RISING(MAX)}$) before sending the EN_SEQ logic command.

Table 8-3. EN_SEQ Truth Table

CASE #	EN_SEQ (1)	EN1 (2)	EN2 (2)	EN3 (2)	EN4 (2)	SEQUENCE UP ORDER	SEQUENCE DOWN ORDER
1	OPEN (3)	Local	Local	Local	Local	None	None
2	↑↓ (4) (5)	0	0	1	1	3→4	4→3
3	↑↓ (4) (5)	0	1	0	1	2→4	4→2
4	↑↓ (4) (5)	0	1	1	0	2→3	3→2
5	↑↓ (4) (5)	0	1	1	1	2→3→4	4→3→2
6	↑↓ (4) (5)	1	0	0	1	1→4	4→1
7	↑↓ (4) (5)	1	0	1	0	1→3	3→1
8	↑↓ (4) (5)	1	0	1	1	1→3→4	4→3→1
9	↑↓ (4) (5)	1	1	0	0	1→2	2→1
10	↑↓ (4) (5)	1	1	0	1	1→2→4	4→2→1
11	↑↓ (4) (5)	1	1	1	0	1→2→3	3→2→1
12	↑↓ (4) (5)	1	1	1	1	1→2→3→4	4→3→2→1

(1) 0 = $V_{EN\_SEQ} < V_{EN\_SEQ\_FALLING(MIN)}$; 1 = $V_{EN\_SEQ} > V_{EN\_SEQ\_RISING(MAX)}$
(2) 0 = $V_{ENx} < V_{ENx\_FALLING(MIN)}$; 1 = $V_{ENx} > V_{ENx\_RISING(MAX)}$
(3) When EN_SEQ is high impedance, all channels turn on/off accordingly to the local ENx logical input voltage.
(4) Is recommended to have stable logic value in ENx before sending the logical sequence command in the EN_SEQ pin, for proper operation.
(5) The rise and fall time for V_{SEQ_EN} are specified as ≥ 100ns.

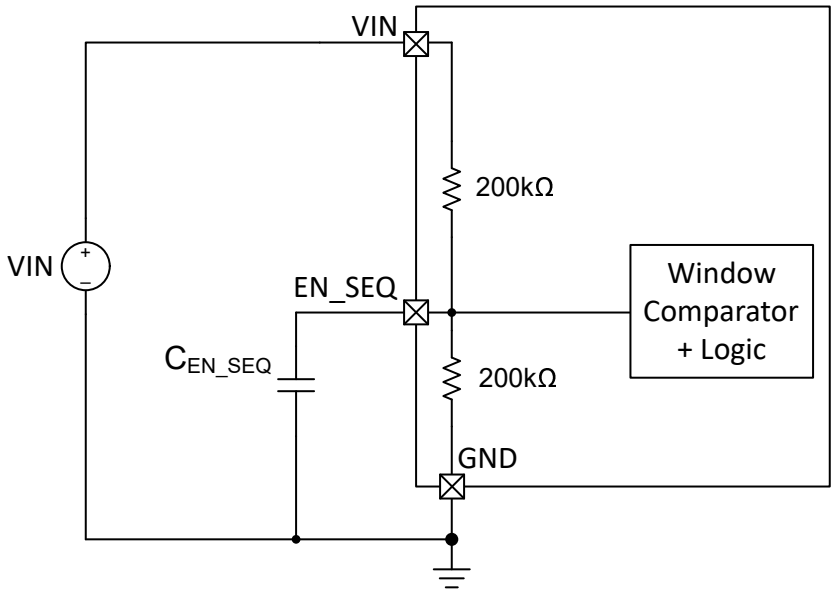


Figure 8-4. Internal Nominal Impedance on EN_SEQ

$$t_{DELAY}\,(s) \approx 100k\Omega \times C_{EN\_SEQ}(F) \times 1.61 \quad (14)$$

8.3.5 Power Good (PWRGDx)

The PWRGDx pin is an open-drain output that is asserted when the output voltage (V_{OUTx}) reaches an appropriate range. This is achieved by comparing the voltage at the VSNSx pin with the internal reference voltage (V_{REFx}). The PWRGDx pins are externally pulled-up through a resistor to a voltage source with the desired logic level (typically V_{OUTx}). The maximum voltage the PWRGDx pins can be pulled-up to is 7V. Select the pull-up resistor value to keep the maximum current sink by PWRGDx to under the recommended operating condition current maximum of 2mA. Generally a pull-up resistor of 10kΩ is sufficient. Using a larger value resistor minimizes power dissipation but can allow switching noise to couple into the PWRGDx signal due a "weaker" pull-up.

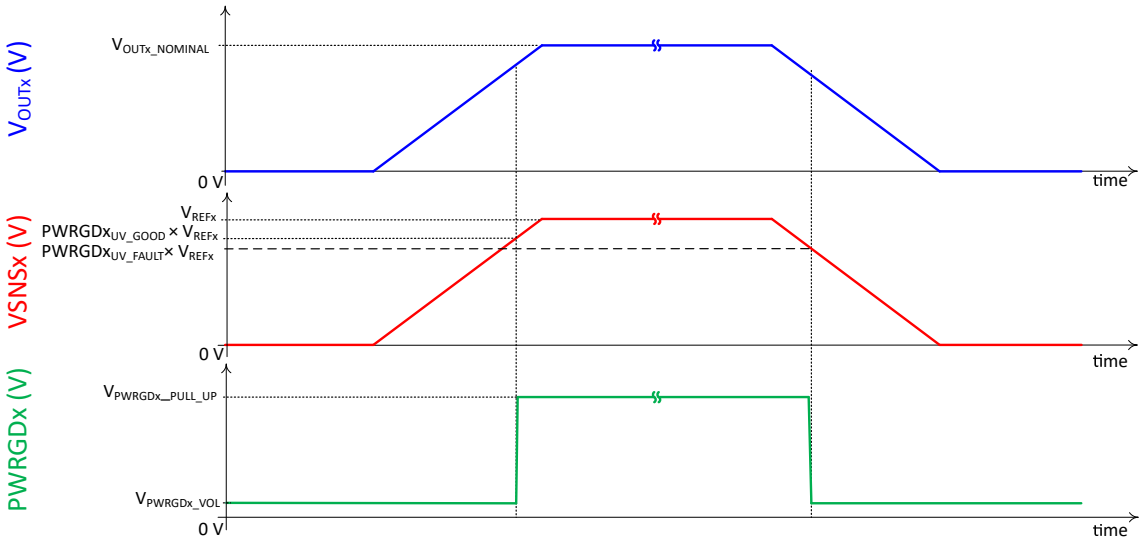
The PWRGDx signals logical states are:

1. Asserted (high impedance or logic high): *when* the V_{OUTx} voltage in percent of final (nominal) value is:
   - Between 92% to 96% during a rising voltage (from an under-voltage or power-up condition).
   - Between 104% to 108% during a falling voltage (from an over-voltage condition).
2. Deasserted (low impedance or logic low) *when* the V_{OUTx} voltage in percent of final (nominal) value is:
   - Between 89% to 92% during a falling voltage (or an under-voltage condition).
   - Between 107% to 111% during a rising voltage (or over-voltage condition).

The responses of PWRGDx to UV_GOOD and UV_FAULT are shown in Figure 8-5, while the OV_FAULT and OV_GOOD is presented on Figure 8-6. The PWRGDx is in a defined state when the VIN input voltage is greater than 1V, but has reduced current sinking capability (See Figure 8-7). PWRGD achieves full current sinking capability when VIN reaches 3V. For more details on the VIN_{MIN_PWRGDx} refer to *POWER GOOD* section in Section 6.5.

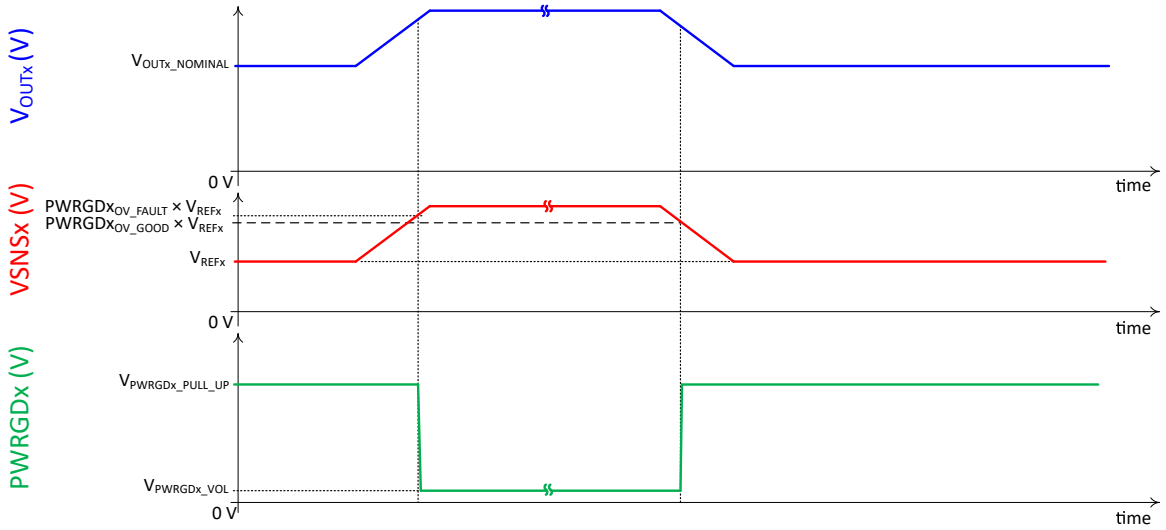
In addition to the description of PWRGDx above, PWRGDx is deasserted (forced low) during other conditions that cause regulation to stop such as:

- VIN UVLO.
- PVIN UVLO
- The device is in thermal shutdown.
- The device ENx pin is logic low (or disabled).
- The COMPx pin reaches the $COMPx_{CLAMP}$ threshold voltage (1.9V typical).
  - $COMPx_{CLAMP}$ force a re-start of V_{OUTx}



A. In this plot is assumed that VIN is in a valid range between 3V to 7V, and a valid rising edge (↑) voltage is provided in the ENx.

Figure 8-5. PWRGDx Undervoltage (UV) Thresholds



A. In this plot is assumed that VIN is in a valid range between 3V to 7V.

Figure 8-6. PWRGDx Overvoltage (OV) Thresholds

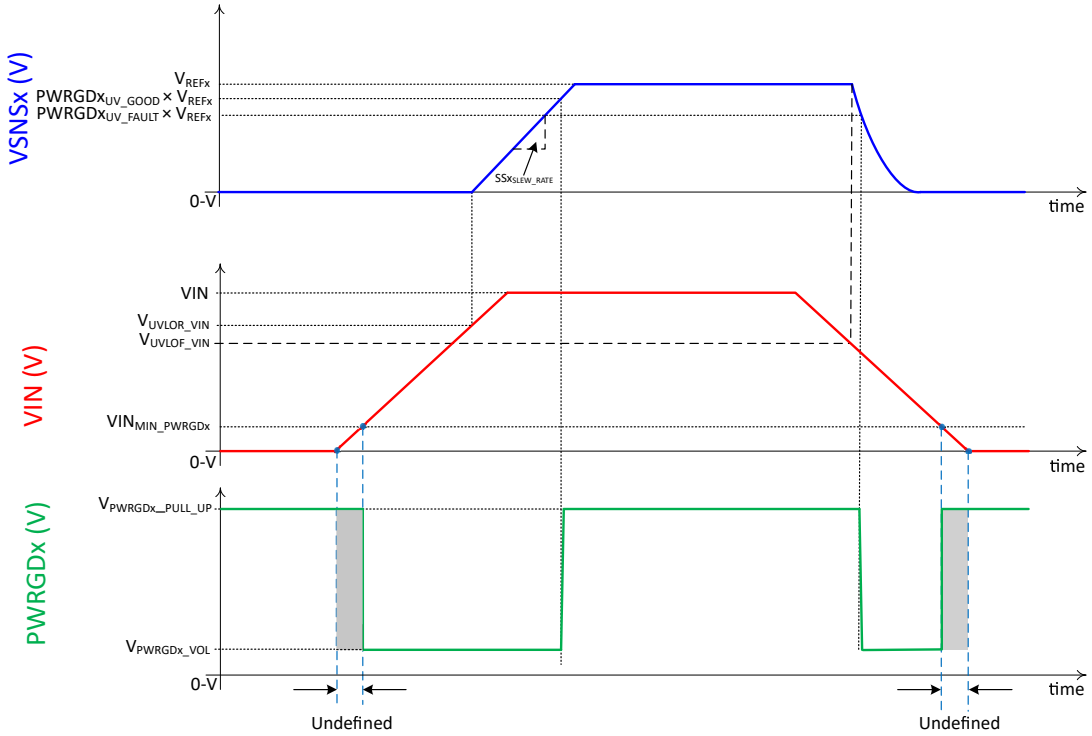


Figure 8-7. PWRGDx in Valid States after VIN > VIN_{MIN_PWRGDx}

8.3.6 Adjustable Switching Frequency, Synchronization (SYNC) and Relative Phase Shift

There are two clocking mode options available on the TPS7H410x:

1. Internal clock
2. External clock

The RT and SYNC conditions for both modes is described on Table 8-4.

Table 8-4. Clock Modes

MODE	CLOCK	INPUT CONFIGURATION FOR CLOCK
	SYNC INPUT	RT
Internal clock	No Clock (or High Impedance)	Resistor from RT to GND
External clock	Clock with frequency as 4 times the f_{SW} (f_{SYNC}= 4 x f_{SW})	

Note

If the RT resistor is not connected the device will stop switching.

8.3.6.1 Internal Clock Mode

In internal clock mode (also called internal oscillator mode), the RT resistor is connected between the RT pin and GND to configure the switching frequency, f_{SW}, of the device. The switching frequency is adjustable from 100kHz to 1MHz depending on the RT resistor value, which can be calculated using Equation 15. Figure 8-8 shows the relationship curve between the RT resistor value and the configurable switching frequency range.

$$\mathrm{RT}\ (\mathrm{k\Omega}) = 54{,}462\left(\frac{1}{f_{SW}(\mathrm{kHz})}\right) - 17 \tag{15}$$

where:

- RT is in kΩ
- f_{SW} in kHz

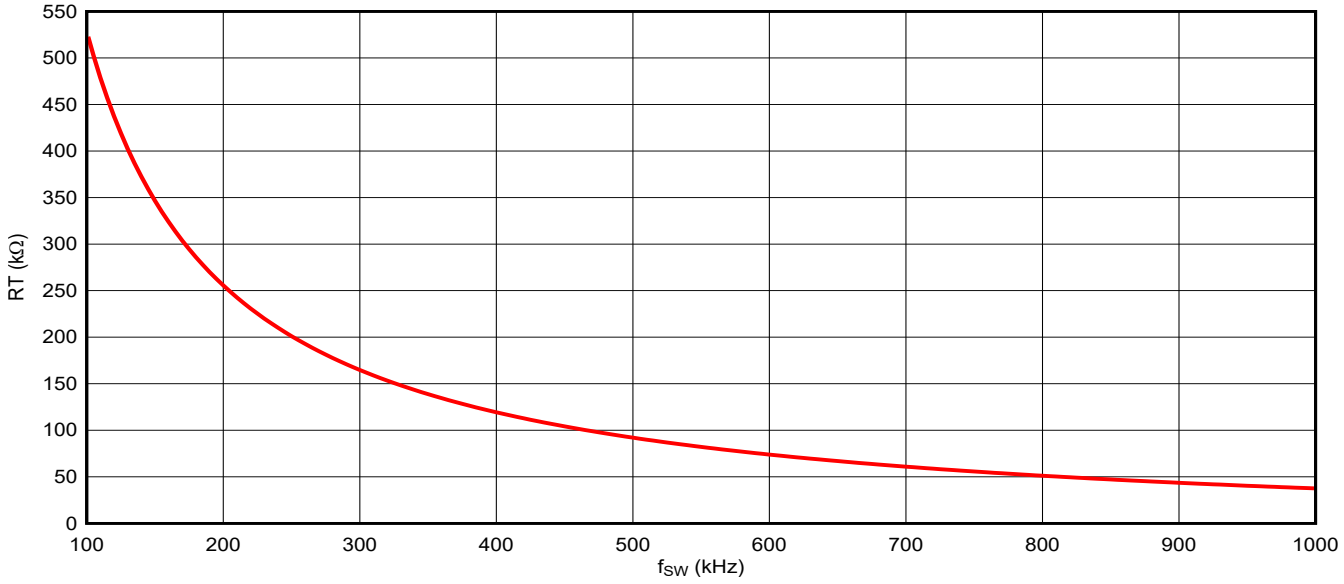


Figure 8-8. Nominal RT vs Switching Frequency

8.3.6.2 External Clock Mode and Switchover

In external clock mode (also called external oscillator mode), a resistor is connected between the RT pin and GND corresponding to the desired switching frequency, the resistor can be calculated using Equation 15. The SYNC input requires a toggling (CLK) signal with a duty cycle between 40% and 60% and a frequency equal to 4 times the programmed switching frequency by RT (f_{SYNC} = 4 x f_{SW}).

The TPS7H410x has an internal clock detector; the device transitions to external clock after the clock is detected for $t_{CLK\_I\_E}$ (typically 1 clock cycles of the internal oscillator). In the event of a loss of the SYNC clock the device transitions to the internal clock after the $t_{CLK\_E\_I}$ (typically 2 clock cycles of the external oscillator). This can be observed on Figure 8-9 and Figure 8-10. The minimum high level voltage of the SYNC clock is a function of the input VIN voltage as described on the V_{SYNC_VIH} parameter on the *SWITCHING FREQUENCY AND SYNCHRONIZATION* section in Section 6.5. For the low level voltage of the external clock any voltage ≤ 0.8V is appropriately interpreted. The external clock can be provided by an oscillator, FPGA, or other device.

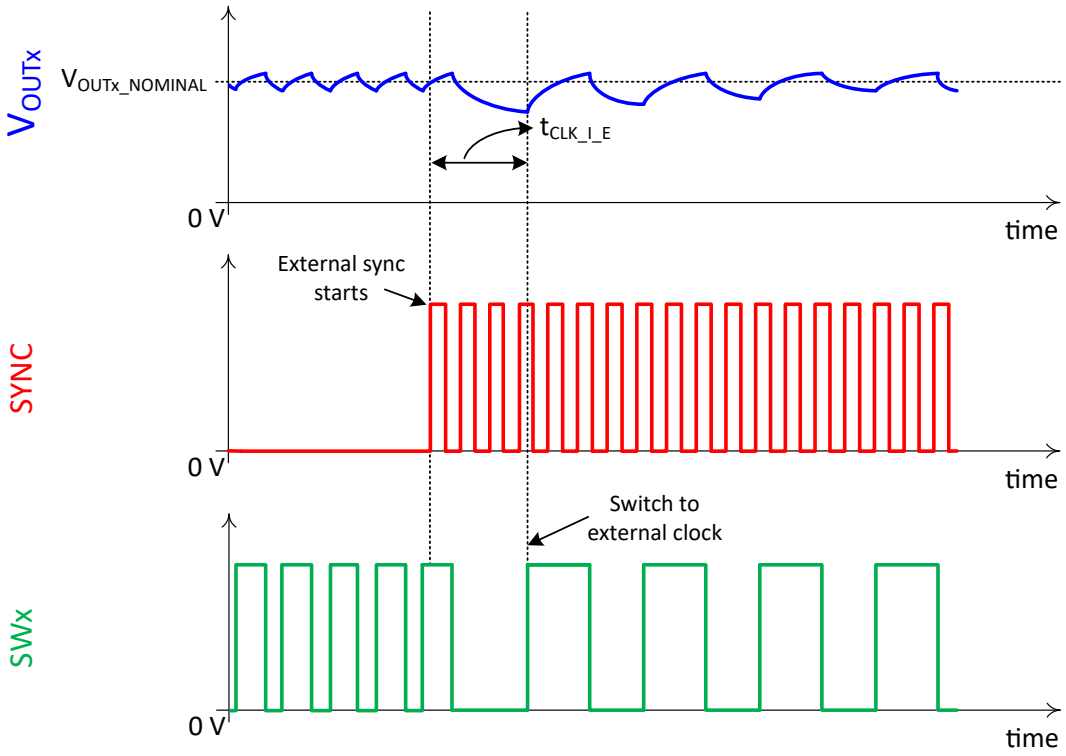


Figure 8-9. Internal to External Clock Transition

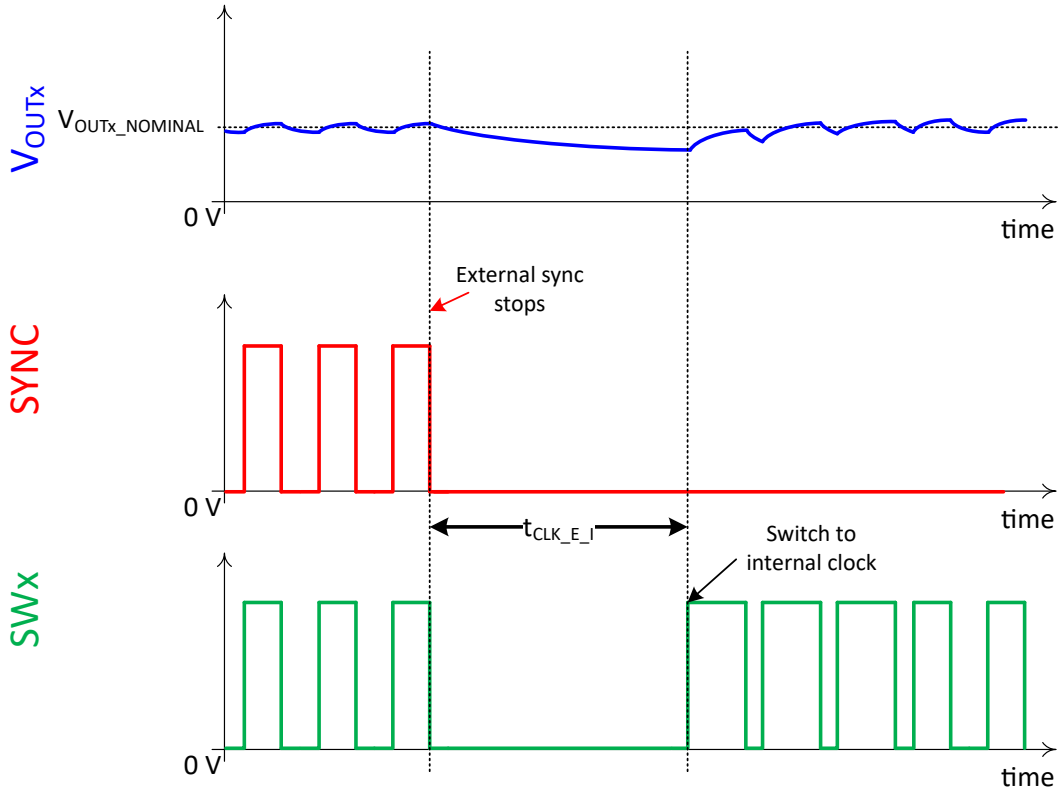


Figure 8-10. External to Internal Clock Transition

8.3.6.3 Relative Phase Shift

The TPS7H410x creates internally a relative phase shift of 90° for each channel (or SWx). This facilitates the interleaving of all four phases to create a single 12A channel. The top (SW1 and SW4) and bottom (SW2 and SW3) channels have a relative 180° phase shift to facilitate the interleaving of those channels for dual 6A channels. Another advantage of having the SWx 90° out-of-phase is a reduced input capacitance (or rms input current) for a given total load current ($\sum I_{OUTx}$).

The phase shift for each channels is:

1. Channel # 1: at a relative phase shift (Φ) of 0°.
2. Channel # 2: at a relative phase shift (Φ) of 90°.
3. Channel # 3: at a relative phase shift (Φ) of 270°.
4. Channel # 4: at a relative phase shift (Φ) of 180°.

The phase shift for each channel is also presented on Pin Configuration and Functions.

8.3.7 Turn-On Behavior

8.3.7.1 Pulse Skipping During Start-up

The device enters into a pulse-skipping mode (hysteretic mode) during start-up in the event that VSNSx is greater than the voltage at the SS_TRx pin (VSNSx > V_{SS_TRx}). During this period, the high-side switch remains off and the low-side switch remains on until VSNSx again falls below the voltage at SS_TR (VSNSx < V_{SS_TRx})

This is because a lower output voltage is needed than that supported by the minimum on time (t_{ONx_MIN}). Thus, instantaneous output pulses can be higher or lower than the desired voltage. This behavior is evident when operating at high frequency and high VIN. For more details refer to SLVA866.

When the minimum on-pulse is greater than the minimum controllable on-time, the pulse-skipping behavior is generally not observed at startup.

8.3.7.2 Soft-Start (SS_TRx)

The device uses the the V_{SS_TRx} as the tracking reference, during start-up. A C_{SS_TRx} capacitor on the SS_TRx pin to GND implements a soft-start time, by providing a "slow" ramp tracking reference. Equation 16 shows the equation for the nominal soft-start time, $t_{SS\_TRx\_NOMINAL}$. This is the time for V_{OUTx} to reach the programmed voltage. The voltage reference (V_{REFx}) is 599.48mV (typ. at 25 °C) and the soft-start charge current (I_{SS_TRx}) is typically 2.28µA. When calculating the soft-start time t_{SS_TRx}, take into account the variation of the parameters C_{SS_TRx}, V_{REFx} and I_{SS_TRx} as these can cause $t_{SS\_TRx\_NOMINAL}$ to deviate from the nominal value in the actual implementation. The error (or deviation) from the nominal can be calculated using Equation 17. The range of the soft start time can be calculated using Equation 18.

$$t_{SS\_TRx\_NOMINAL}\left(ms\right) = \frac{V_{REFx}(V) \times C_{SS\_TRx}(nF)}{I_{SS\_TRx}(\mu A)} \tag{16}$$

$$t_{SS\_TRx\_ERROR}\left(ms\right) = \pm \sqrt{\frac{C_{SS\_TRx}{}^{2}(nF) \times V_{REFx}{}^{2}(V) \times \left(C_{SS\_TRx\_TOL}{}^{2} + I_{SS\_TRx\_ACC}{}^{2} + V_{REFx\_ACC}{}^{2}\right)}{I_{SS\_TRx}(\mu A)}} \tag{17}$$

$$t_{SS\_TRx}(ms) = t_{SS\_TRx\_NOMINAL}(ms) \pm t_{SS\_TRx\_ERROR}(ms) \tag{18}$$

where:

- $C_{SS\_TRx\_TOL}$ is the C_{SS_TRx} capacitor tolerance in numeric value. For example a 10% tolerance capacitor is 0.1.
- $I_{SS\_TRx\_Acc}$ is the soft start current accuracy, for more details refer to *SOFT START AND TRACKING* in Section 6.5
- V_{REFx_Acc} is the reference accuracy. Use 0.01 as the reference is 1% accurate.

During start-up when the output capacitor bank is discharged, a large in-rush current is required to quickly charge the bank. If this current is not controlled below the sourcing current limit, non-linearities can be observed due to the protection feature of the device. To select the soft-start capacitor for a given output capacitor the designer can use Equation 19 and Equation 20.

$$t_{SS\_TRx\_NOMINAL}\left(s\right) = \frac{C_{OUTx}(F)}{4.2A - I_{OUTx}(A)} \times V_{OUTx}\,(V) \tag{19}$$

Where:

- C_{OUTx} is the output capacitor in Farads (F).
- 4.39A is the minimum value from the sourcing current limits in this case is the minimum from the $I_{OC\_LS\_SOURCINGx}$.
- I_{OUTx} is the maximum expected load for a given channel in Amps (A). The maximum possible load (or upper bound) for a single channel is 3A.
- V_{OUTx} is the nominal output voltage in Volts (V)

$$C_{SS\_TRx\_NOMINAL}\left(nF\right) = \frac{t_{SS\_TRx\_NOMINAL}(ms) \times I_{SS\_TRx}\left(\mu A\right)}{V_{REFx}(V)} \quad (20)$$

Where:

- $t_{SS\_TRx\_NOMINAL}$ is the nominal soft-start time in milliseconds (ms).
- I_{SS_TRx} (2.28µA) is the nominal soft-start current in micro-amps (µA).
  - For more details on the I_{SS_TRx} refer to *SOFT START AND TRACKING* section in Section 6.5.
  - If desired to minimize the soft-start capacitor error across temperature we can re-center the current as:

$$I_{SS\_TRx} = \frac{I_{SS\_TRx(MIN)} + I_{SS\_TRx(MAX)}}{2} = 2.115\mu A \quad (21)$$

- I_{OUTx} is the maximum expected load for a given channel in Amps (A). The maximum possible load (or upper bound) for a single channel is 3A.
- V_{OUTx} is the nominal output voltage in Volts (V)

When any of the following four scenarios occur the SS_TRx pin is discharged through the internal $R_{SS\_TRx\_DISCHARGE}$ pull-down resistor (typically 364Ω):

- The input UVLO is triggered (VIN < V_{UVLOF_VIN}).
- The ENx pin voltage is a logic low (V_{ENx} < $V_{ENx\_FALLING}$).
- The CHx is turn off by the internal EN_SEQ logic during sequence down.
- The COMPx pin reaches the $COMPx_{CLAMP}$ threshold.
- A thermal shutdown event occurs.

When the SS_TR pin is discharged, the device cannot restart again until the pin has discharged to below $SS\_TRx_{START\_UP}$ (typically 22mV) in order to provide proper soft-start behavior

.

8.3.7.3 Safe Start-up Into Pre-biased Outputs

The device prevents the low-side MOSFET from continuously discharging a pre-biased output voltage. This is achieved by making sure the device always starts switching by turning on the high side (PMOS) in conjunction with a pulse-skipping (hysteresis) mode control during start-up.

8.3.7.4 Tracking and Sequencing (SS_TRx)

In addition to the internal sequence up/down (using EN_SEQ), typical sequence-up methodologies as described below can be implemented using the SS_TRx, ENx, and PWRGDx pins.

Note

The sequencing methodologies described below offer upwards control, however the system configuration does not offer reverse sequence down, needed in many applications. For sequential up and reverse sequence down use the EN_SEQ input as described on the Sequence UP/DOWN (EN_SEQ) section. For a more comprehensive sequence control the designers can use the TPS7H3014, a 3V to 14V space-grade sequencer.

The sequential method is shown in Figure 8-11. In this case channel # 1 and #2 of TPS7H4104 are used. As with any methodology discussed here, the figure can be expanded to any CHx (or from another point of load converter), however for simplicity the figure shows only 2 channels (in this case CH1 and CH2). The PWRGD1 pin of the first channel is coupled to the EN2 pin of the second channel, which enables the second power supply after the primary supply reaches regulation (typically 94% during a rising V_{OUTx} voltage) . If a further delay is desired between sequencing of the first and second channel an optional C_{PWRGD1} capacitor can be included on PWRGD1 as well. This causes an RC delay based on the value of the power good pull-up resistor and the capacitor utilized.

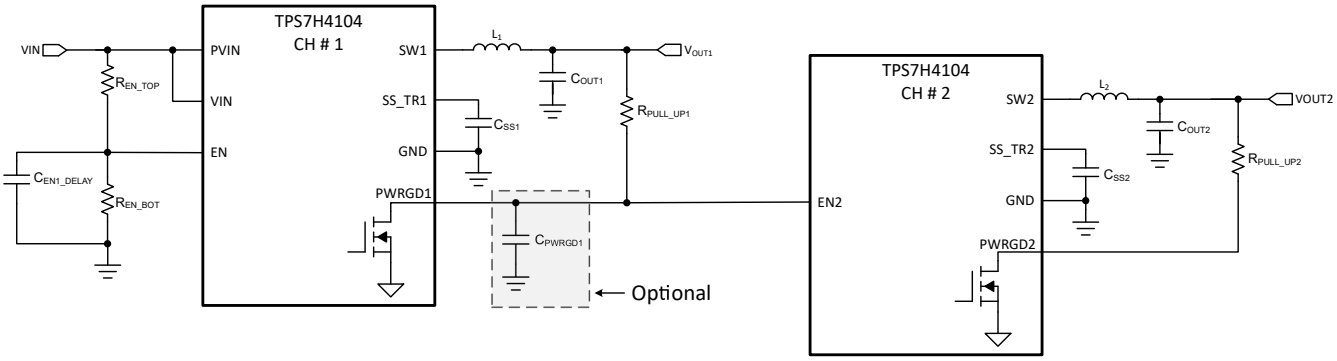


Figure 8-11. Sequential Start-Up Sequence

Figure 8-12 shows the method implementing ratiometric sequencing by connecting the SS_TR1 and SS_TR2 pins of two channels together (in this case channels # 1 and 2). The regulator outputs (V_{OUT1} and V_{OUT2}) ramp up and reach regulation at the same time.

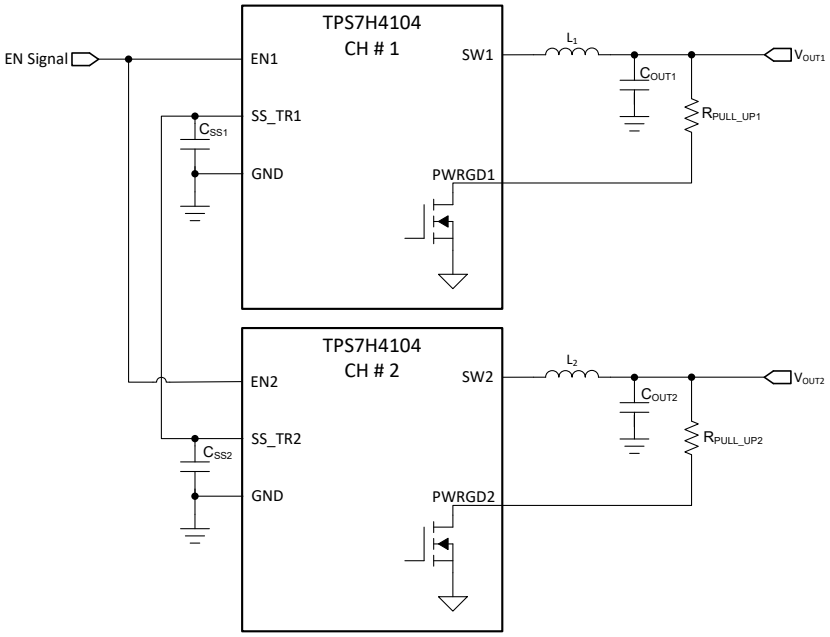


Figure 8-12. Ratiometric Start-Up Sequence

Ratiometric and simultaneous power-supply sequencing can be implemented by connecting the resistor network of R_1 and R_2 (shown in Figure Ratiometric and Simultaneous Start-Up Sequence) to the output of the power supply that needs to be tracked or another voltage reference source. Using Equation 22 and Equation 23 , the tracking resistors can be calculated to initiate the V_{OUT2} slightly before, after, or at the same time as V_{OUT1}. Equation 24 is the voltage difference between V_{OUT1} and V_{OUT2}.

To design a ratiometric start-up in which the V_{OUT2} voltage is slightly greater than the V_{OUT1} voltage when V_{OUT2} reaches regulation, use a negative number in Equation 22 and Equation 23 for ΔV. Equation 24 results in a positive number for applications where the V_{OUT2} is slightly lower than V_{OUT1} when V_{OUT2} regulation is achieved.

The ΔV variable is 0 V for simultaneous sequencing. To minimize the effect of the inherent SS_TRx to VSNSx offset ($SS\_TRx_{START\_UP}$ = 22mV typ.) in the soft-start circuit and the offset created by the pullup current source (I_{SS_TRx} = 2.28µA typ.) and tracking resistors, the $SS\_TRx_{START\_UP}$ and I_{SS_TRx} are included as variables in the equations.

To provide proper operation of the device, the calculated R_1 value from Equation 22 must be greater than the value calculated in Equation 25.

$$R_1 = \frac{V_{OUT2} + \Delta V}{V_{REFx}} \times \frac{SS\_TRx_{START\_UP}}{I_{SS\_TRx}} \quad (22)$$

$$R_2 = \frac{V_{REFx} \times R_1}{V_{OUT2} + \Delta V - V_{REFx}} \quad (23)$$

$$\Delta V = V_{OUT1} - V_{OUT2} \quad (24)$$

$$R_1 > (2800 \times V_{OUT1}) - (180 \times \Delta V) \quad (25)$$

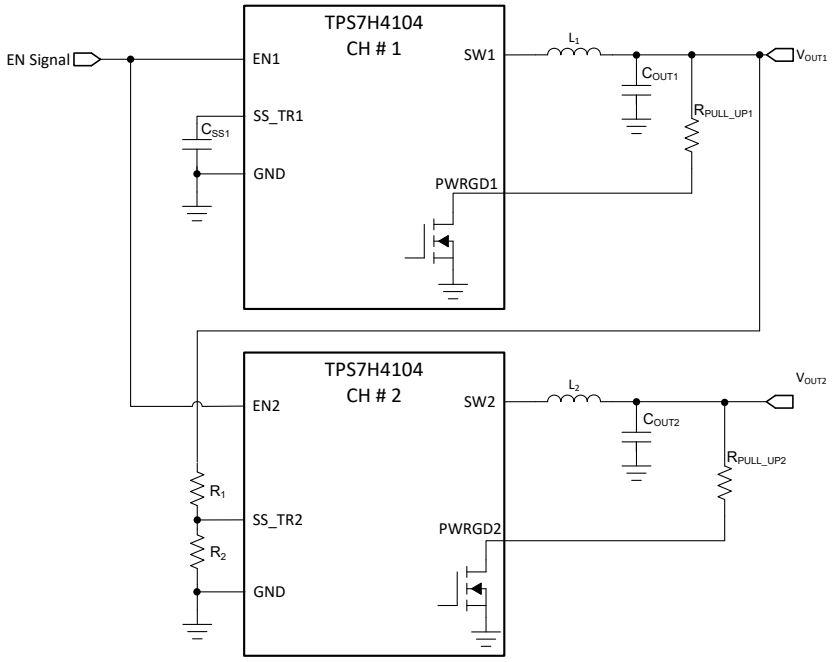


Figure 8-13. Ratiometric and Simultaneous Start-Up Sequence

8.3.8 Protection Modes

The following protection modes are detailed in the following sections:

- Overcurrent Protection: Section 8.3.8.1
  - High-Side Overcurrent Protection: High-Side Cycle by Cycle Overcurrent Protection (I_{OC_HSx})
  - Low-Side Overcurrent Sourcing and Sinking Protection: Low-Side Overcurrent Sourcing and Sinking Protection
- Output Overvoltage Protection (OVP): Section 8.3.8.2
- Thermal Shutdown: Section 8.3.8.3

8.3.8.1 Overcurrent Protection

The TPS7H410x device employs multiple overcurrent protection mechanisms. The device is primarily protected from overcurrent conditions by means of the following:

1. High-side cycle by cycle current limit (I_{OC_HSx}) .
2. Low-side sourcing current limit ($I_{OC\_LS\_SOURCINGx}$)
3. $COMPx_{CLAMP}$ shutdown.
4. Low-side sinking current limit.

These current protection mechanisms are detailed in the subsequent sections.

8.3.8.1.1 High-Side Cycle by Cycle Overcurrent Protection (I_{OC_HSx})

The device implements current mode control, which uses the COMPx pin voltage to control the turn-off of the high-side MOSFET and the turn-on of the low-side MOSFET on a cycle-by-cycle basis. Each cycle, the switch current and the current reference generated by the COMPx pin voltage are compared. When the peak switch current intersects the programmed high side current, I_{OC_HSx}, the high-side switch is immediately turned off (although the high side is on for at least the minimum on time, t_{ONx_MIN}).

I_{OC_HSx} is implemented utilizing the COMPx voltage. As the device approaches I_{OC_HSx}, COMPx increases which causes the gm_{PSx} of the device to approach zero. Therefore, at high enough values of COMPx, the output current is essentially clamped to the internal limit. This functionality is shown in the simplified waveforms of Figure 8-14.

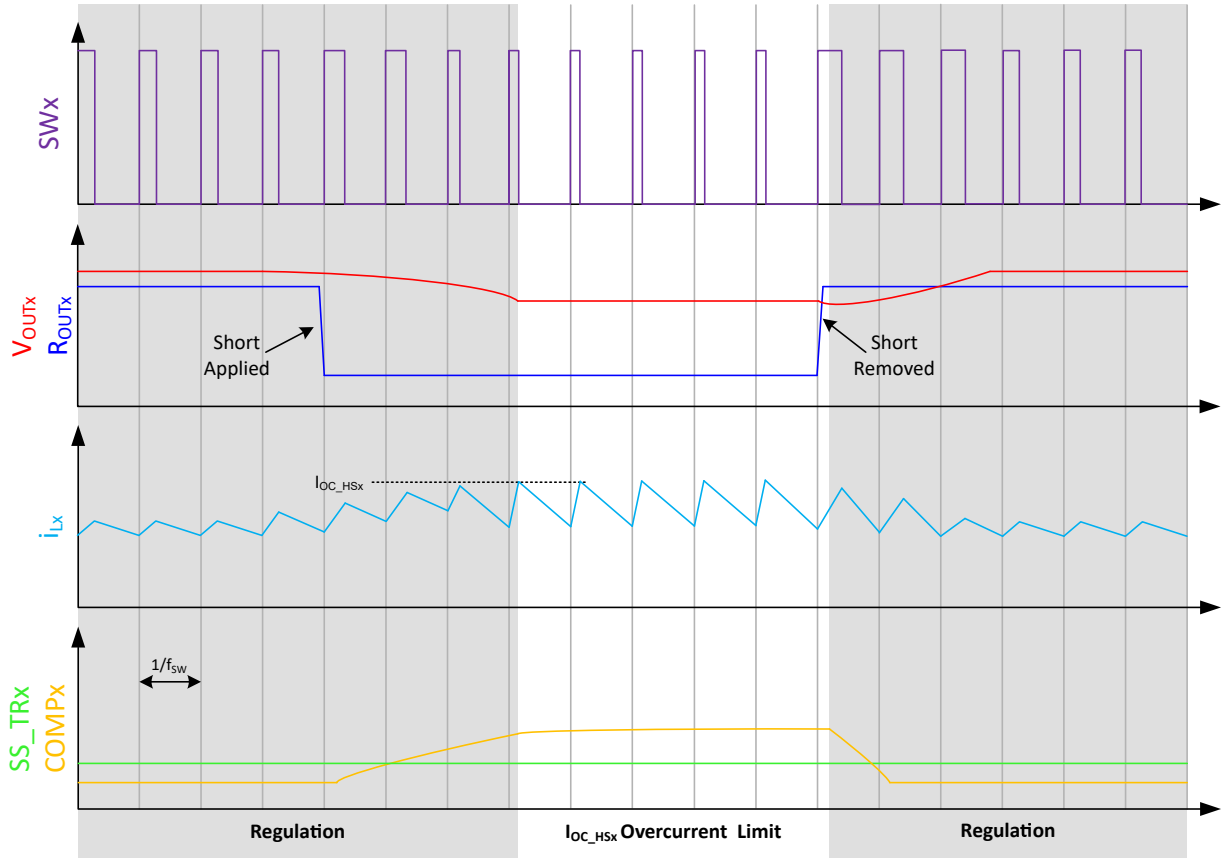


Figure 8-14. High-Side Cycle by Cycle Overcurrent Protection (I_{OC_HSx})

8.3.8.1.2 Low-Side Sourcing Overcurrent Protection ($I_{OC\_LS\_SOURCINGx}$)

Sometimes, the I_{OC_HSx} current limit is not sufficient to protect the device. For example, a short circuit can be so aggressive that even if the high side is only on for the minimum on time (t_{ONx_MIN}) the current can continue to rise. To mitigate this risk, the TPS7H410x implements a secondary overcurrent protection in the form of low-side sourcing current limit ($I_{OC\_LS\_SOURCINGx}$). The $I_{OC\_LS\_SOURCINGx}$ current limit is reached when the current through the low side MOSFET meets or exceeds $I_{OC\_LS\_SOURCINGx}$. To prevent sustained current increase, the high-side is prevented from turn-on until the current trough the low-side FET falls below the $I_{OC\_LS\_SOURCINGx}$ threshold. The simplified waveforms of this operation are shown in Figure 8-15.

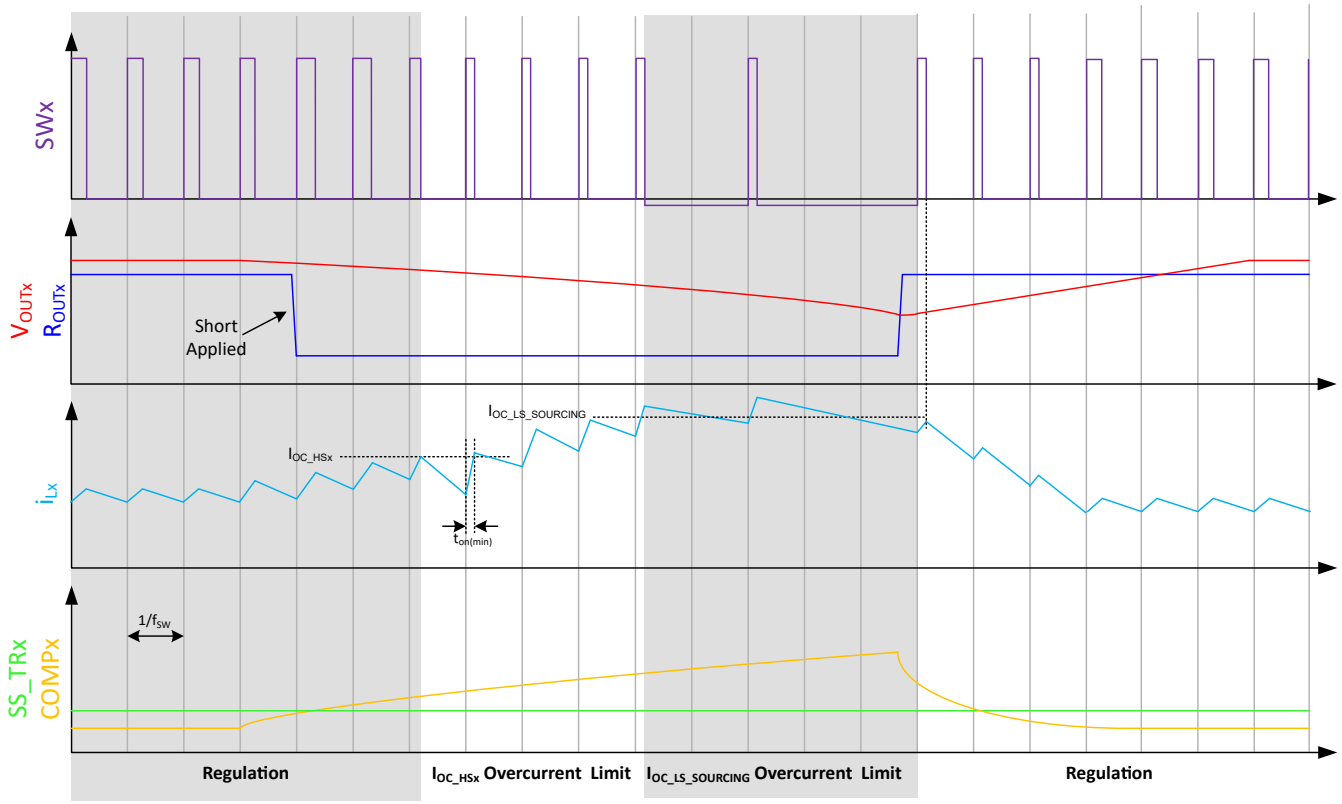


Figure 8-15. Low-Side Sourcing Overcurrent Protection ($I_{OC\_LS\_SOURCINGx}$)

8.3.8.1.3 COMPx Clamp Shutdown ($COMPx_{CLAMP}$)

Since the voltage on the COMPx pin is proportional to the device output current, clamping the COMPx voltage achieves another method to protect the device from overcurrent events. Specifically, if COMPx rises above $COMPx_{CLAMP}$ (typically 1.9V), the part is shutdown. This feature is a complement to the I_{OC_HSx} and $I_{OC\_LS\_SOURCINGx}$ current limits. Since the slew rate of COMPx is limited by the overall loop bandwidth and by the drive strength of the error amplifier, the time for COMPx to reach $COMPx_{CLAMP}$ during a fault depends on the loop compensation and specific type of fault. During most faults, I_{OC_HSx} is reached before COMPx reaches $COMPx_{CLAMP}$. $I_{OC\_LS\_SOURCINGx}$ is often reached before COMPx reaches $COMPx_{CLAMP}$; however depending on the fault type, COMPx can reach $COMPx_{CLAMP}$ and disable the part before $I_{OC\_LS\_SOURCINGx}$ is reached. Consequently, $COMPx_{CLAMP}$ can be thought of as a type of fail-safe. After COMPx reaches $COMPx_{CLAMP}$, the device stops switching and begins discharging the SS_TRx pin through a pull-down resistance, $R_{SS\_TRx\_DISCHARGE}$ (typically 364Ω). The part does not attempt a restart until SS_TRx has discharged to $SS\_TRx_{START\_UP}$ startup (typically 22mV). This provides a cool down period for the TPS7H410x. Note that this discharge time is directly dependent upon the value of the soft start capacitor, C_{SS_TRx}. An example of the COMP shutdown functionality is shown in the simplified waveforms of Figure 8-16.

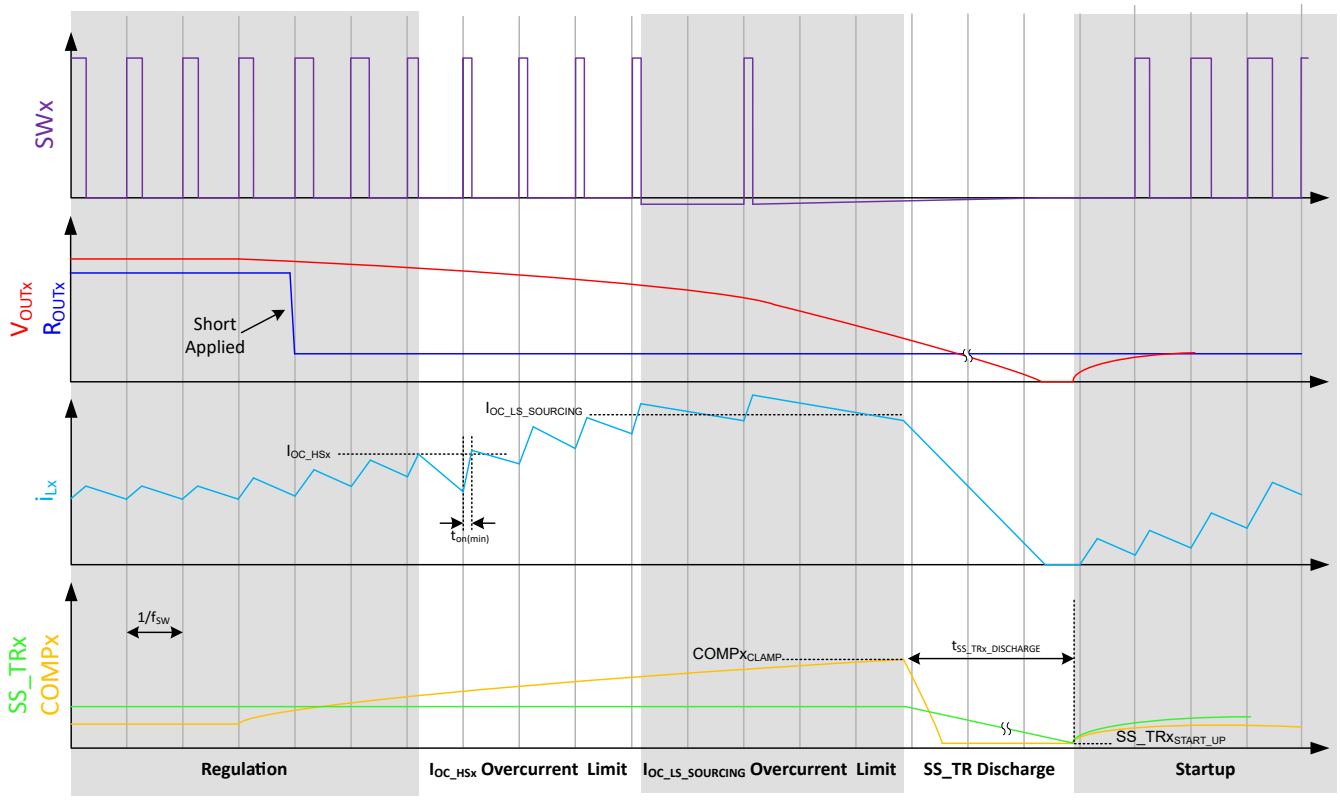


Figure 8-16. COMPx Clamp Shutdown ($COMPx_{CLAMP}$)

Additionally, COMPx can reach $COMPx_{CLAMP}$ if an aggressive load step is applied to the output load and a high loop bandwidth is utilized. This is because in this situation, COMPx can slew higher faster than the load can respond. This can be avoided through a compensation network that is appropriately designed for the worse case load step.

8.3.8.1.4 Low-Side Overcurrent Sourcing and Sinking Protection

The low-side MOSFET can sink current from the load (such as during light load operation). In certain situations (such as a high current load being suddenly removed or VOUT being raised above the set point), the low-side sink current can become excessive. Therefore, low-side overcurrent sinking protection is provided. If the low-side sinking current limit is exceeded, the low-side MOSFET is turned off immediately for the rest of that clock cycle. In this scenario, both MOSFETs are off until the start of the next cycle. When the low-side MOSFET turns off, the switch node voltage increases and forward biases the high-side MOSFET parallel body diode (the high-side MOSFET is still off at this stage).

8.3.8.2 Output Overvoltage Protection (OVP)

The device incorporates an output overvoltage protection (OVP) circuit to minimize output voltage overshoot. The OVP circuit engages when VSNSx ≥ ($PWRGDx_{OV\_FAULT\%}$ × V_{REFx}). Typically, this means the OVP circuitry engages when V_{OUTx} rises above 109% of the nominal value. When OVP is active, the high-side FET stays off and the low-side FET stays on to quickly discharge V_{OUTx}.

An example that can cause an overvoltage condition is when the power supply output is overloaded for a sustained period of time. Therefore, the error amplifier compares the actual output voltage to the internal reference voltage. If the VSNSx pin voltage is lower than the internal reference voltage for a considerable time, the output of the error amplifier demands maximum output current. After the condition is removed, the regulator output rises and the error amplifier output transitions to the steady-state voltage. In some applications with small output capacitance, the power supply output voltage can respond faster than the error amplifier. This leads to the possibility of an output overshoot. The OVP feature minimizes this overshoot.

If the VSNSx pin voltage is greater than the OVP threshold, the high-side MOSFET is turned off, preventing current from flowing to the output and minimizing output overshoot. When the VSNSx voltage drops lower than the OVP threshold, the high-side MOSFET is allowed to turn on at the next clock cycle.

8.3.8.3 Thermal Shutdown

The internal thermal shutdown circuitry forces the device to stop switching if the junction temperature exceeds 163°C (typical). The device re-initiates the power-up sequence when the junction temperature drops below 134°C (typical). The low thermal shutdown voltage and large hysteresis aims to keep the device as cool as possible during this fault condition.

8.3.9 Error Amplifier and Loop Response

Figure 8-17 shows a simplified model for the device control loop. The model can be utilized to aid in determining the frequency response and transient response of the buck regulator system. The simplified model is composed of an operational transconductance error amplifier (OTA), the power stage, external feedback, and external compensation. The effects of slope compensation are not shown in this model. More information on the error amplifier and power stage are shown in the subsequent sections (Section 8.3.10.1 and Section 8.3.10.2 respectively).

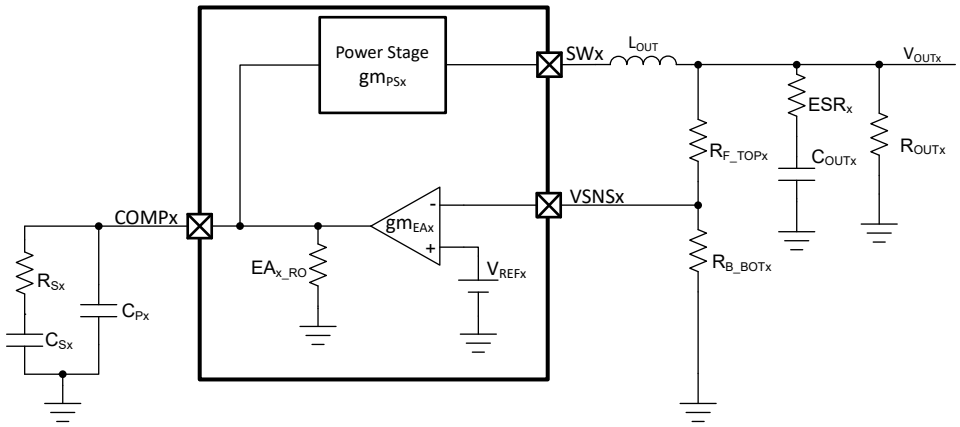


Figure 8-17. Simplified Small Signal Model For Loop Response

8.3.9.1 Error Amplifier

The TPS7H410x device utilizes a transconductance error amplifier. The error amplifier compares the VSNSx voltage to the internal V_{REFx} voltage reference. The transconductance of the error amplifier is 1,672µS (typ). The frequency compensation network is connected between the COMPx pin and ground. The error amplifier DC gain is typically 16,000 V/V (or 84dB).The error amplifier output resistance is 9.57MΩ (typ).

8.3.9.2 Power Stage Transconductance

The power stage transconductance of the TPS7H410x (gm_{PSx}) is 8.35S (or A/V), typically. For more details refer to the *ERROR AMPLIFIER* section in Section 6.5. The gm_{PSx} have a proportionally inverse relationship with the load current. This means that the gm_{PSx} decrements as the load current increments. This can be observed on Figure 8-18.

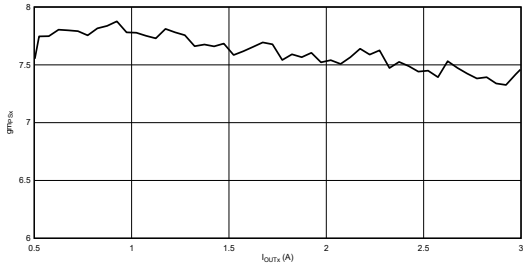


Figure 8-18. gm_{PSx} vs I_{OUTx} at PVIN = VIN = 5V and T_A = 25℃

8.3.9.3 Slope Compensation

The desired slope compensation, SCx, can be configured with a resistor from the RSCx pin to GND. The TPS7H410x device adds a compensating ramp to the switch current signal for all duty cycles. Various typical values of RSCx and the resulting slope compensation are shown in the *SLOPE COMPENSATION* section in the Section 6.5. Equation 26 is provided to approximate the value of RSCx needed to achieve a desired slope compensation (SCx).

$$\mathrm{RSCx\ (k\Omega)} = -20245 \cdot \frac{1}{\mathrm{f_{SW}(kHz)}} + 428\frac{1}{\mathrm{SCx}\left(\frac{\mathrm{A}}{\mu\mathrm{s}}\right)} - 51.1 \quad (26)$$

where:

- RSCx is the suggested value of the resistance in kΩ to achieve the desired slope compensation (SCx) in A/µs.
- f_{SW} is the switching frequency in kHz.
- SCx is the desired slope compensation (absolute value) in A/µs. (note that the *SLOPE COMPENSATION* in Section 6.5 gives this value as a negative unit)

A commonly suggested value for slope compensation is defined as the output voltage divided by the inductor value as presented on Equation 27.

$$\mathrm{SC_{IDEAL}} = \frac{\mathrm{V_{OUTx}}}{\mathrm{L_x}} \quad (27)$$

8.3.9.4 Frequency Compensation

External frequency compensation is required for the TPS7H410x. There are several industry techniques used to compensate DC-DC regulators. For the TPS7H410x, type 2A compensation is most often recommended though other approaches are acceptable. See Section 9.2.2.9 in the application section for a specific example.

8.4 Device Functional Modes

The device uses fixed frequency, peak current mode control. As a synchronous buck converter, the device normally operates in continuous current mode under all load conditions. The output voltage is divided down through external resistors and VSNSx is compared to an internal voltage reference by an error amplifier, which drives the COMPx pin. An internal oscillator initiates the turn on of the high-side power switch. The error amplifier output is converted into a current reference, which is compared to the high-side power switch current. When the power switch current reaches the current reference generated by the COMPx voltage level, the high-side power switch is turned off and the low-side power switch is turned on.

9 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

9.1 Application Information

The TPS7H410x is a radiation hardened synchronous buck converter. The device is utilized to convert a higher DC input voltage to a lower DC output voltage at a maximum of 3A/channel. The device can be used over an input voltage range of 3V to 7V.

9.2 Typical Application

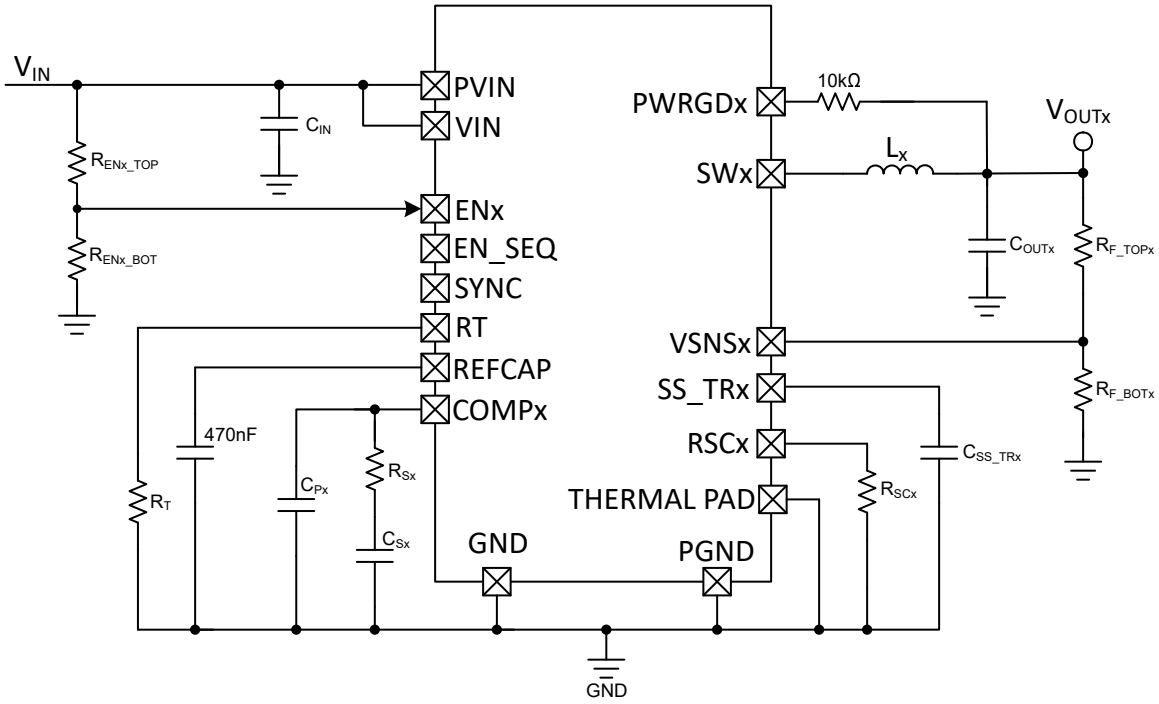


Figure 9-1. Typical Application Schematic

9.2.1 Design Requirements

Table 9-1. Design Parameters

DESIGN PARAMETER	EXAMPLE VALUE
Input voltage	5V ±10%
Nominal output voltage for channel # 1 (V_{OUT1})	0.8V
Nominal output voltage for channel # 2 (V_{OUT2})	1.2V
Nominal output voltage for channel # 3 (V_{OUT3})	1.5V
Nominal output voltage for channel # 4 (V_{OUT4})	1.8V
Maximum output current (per channel)	3A
Transient response for a full-load (3A) load step	$\Delta V_{OUTx} \leq$ 3.5%
Output voltage ripple	≤0.8% of V_{OUTx}
Start input voltage (rising V_{IN})	3V
Switching frequency (f_{SW})	500kHz

Note

Calculated values shown in this section are rounded up to 3 decimal points.

9.2.2 Detailed Design Procedure

9.2.2.1 Operating Frequency

The first step is to decide on a switching frequency for the regulator. There is a trade off between higher and lower switching frequencies. Higher switching frequencies can produce a smaller size using lower valued inductors and smaller output capacitors compared to a power supply that switches at a lower frequency. However, the higher switching frequency causes extra switching losses, which hurt the converter efficiency and thermal performance. In this design, a switching frequency of 500kHz is selected. Using Equation 15, an RT resistor of 92.42kΩ is calculated. The selected component for this example is 90.9kΩ.

9.2.2.2 Output Inductor Selection

To calculate the value of the output inductor, use Equation 28. K_{Lx} is a coefficient that represents the amount of inductor ripple current relative to the maximum output current, I_{OUTx} as shown in Equation 29. Since the output capacitors must have a ripple current rating greater than or equal to the inductor ripple current, choosing a high inductor ripple current impacts output capacitors selection. In general, the inductor ripple value is at the discretion of the designer depending on specific system needs. Typical values for K_{Lx} range from 10% to 50%. For low output currents, the value of $K_{L\ x}$ can be increased to minimize excessive switch (SWx) jitter and to reduce the value of the output inductor.

$$L \geq \left(\frac{V_{IN\_MAX} - V_{OUTx}}{I_{OUTx} \times K_{Lx}}\right) \times \left(\frac{V_{OUTx}}{V_{IN\_MAX} \times f_{SW}}\right) \quad (28)$$

$$K_{Lx} = \frac{\Delta i_{Lx}}{I_{OUTx}} \quad (29)$$

For this design example, use K_{Lx} = 40% and V_{IN_MAX} = 5.5V (5V + 10%). Once the inductor value is known (or selected) the actual ripple current (Δi_{Lx}), RMS and peak current can be calculated, using Equation 30, Equation 31 and Equation 32, respectively. The inductor design details are presented in Table 9-2.

$$\Delta i_{Lx} = \left(\frac{V_{IN\_MAX} - V_{OUTx}}{Lx}\right) \times \left(\frac{V_{OUTx}}{V_{IN\_MAX} \times f_{SW}}\right) \quad (30)$$

$$i_{L\_RMSx} = \sqrt{I_{OUTx}{}^2 + \frac{1}{12} \times \left(\frac{V_{OUTx} \times (V_{IN\_MAX} - V_{OUTx})}{V_{IN\_MAx} \times Lx \times f_{SW}}\right)^2} \quad (31)$$

$$i_{L\_PEAK} = I_{OUTx} + \frac{\Delta i_{Lx}}{2} \quad (32)$$

Table 9-2. Inductor Design Calculations

V_{OUTx} (V)	CALCULATED INDUCTOR VALUE (µH)	SELECTED INDUCTOR VALUE (µH)	INDUCTOR RIPPLE CURRENT (A)	INDUCTOR RMS CURRENT (A)	INDUCTOR PEAK CURRENT (A)
0.8	1.14	1.8	0.76	3.01	3.38
1.2	1.56	1.8	1.04	3.02	3.52
1.5	1.82	1.8	1.21	3.02	3.61
1.8	2.02	2.2	1.10	3.02	3.55

The current flowing through the inductor is the inductor ripple current plus the output current. During power up, faults, or transient load conditions, the inductor current can increase above the previously calculated peak inductor current level. In transient conditions, the inductor current can increase up to the switch current limit of the device. For this reason, the most conservative approach is to specify an inductor with a saturation current rating equal to or greater than the maximum switch current limit, rather than the peak inductor current.

For the TPS7H410x the maximum value for the current limit is dominated by the $I_{OC\_LS\_SOURCINGx}$ at 7.6A. The selected inductor model, saturation current, and the RMS are shown in Table 9-2.

Table 9-3. Selected Inductor Details

INDUCTOR VALUE (µH)	INDUCTOR PART NUMBER	INDUCTOR I_{SAT} RATING (A)	INDUCTOR I_{RMS} RATING (A)
1.8	XGL6030-182MEC	9.4	9.5
2.2	XGL6030-222MEC	8.7	8.5

9.2.2.3 Output Capacitor Selection

There are several considerations in determining the value of the output capacitor. The selection of the output capacitor is driven by:

1. The desired output voltage ripple, driven by the natural switching action of the power stage.
2. The allowable voltage deviation due to a large, abrupt change in load current (load step).

The output capacitance needs to be selected based on the more stringent of these two criteria (refer to Equation 33).When selecting the capacitors, care can be taken to select capacitors with a sufficient voltage rating, temperature rating, and consideration of any effective capacitance changes due to DC bias effects. Of importance is the note that the value of the output capacitor directly influences the modulator pole of the converter frequency response, as described in Section 9.2.2.9.

$$C_{OUTx}(F) \geq \max\left(C_{OUTx\_LOAD\_STEP}(F), C_{OUTx\_RIPPLE}(F)\right) \quad (33)$$

The first criteria to consider is the desired response to a load step. This generally occurs when the regulator is temporarily not able to supply sufficient output current during a large, fast increase in the current needs of the load. This can occur during a transition from no load to full load due to dynamic loads such as processors. The output capacitor must be sized to supply the extra current to the load until the control loop responds to the load change. Equation 34 shows the minimum output capacitance, from the electrical point of view, necessary to accomplish this. This is a first order approximation and does not take into condideration the ESR and ESL of the ourput capacitor. For ceramic capacitors, the ESR is usually small enough to ignore in this calculation. However, for space applications and large capacitance values, tantalum capacitors are typically used, which have a certain ESR value to take into consideration.

$$C_{OUTx\_LOAD\_STEP}(F) = \frac{2 \times \Delta I_{OUTx}(A)}{f_{SW}(Hz) \times \Delta V_{OUTx\_LOAD\_STEP}(V)} \quad (34)$$

Where:

- ΔI_{OUTx} is the worst case change in load current (load step) in the application in Amps (A). In this case we are designing for a full-load step of 3A/phase.
- f_{SW} is the switching frequency of the converter in Hertz. In this case the selected switching frequency is 500kHz.
- $\Delta V_{OUTx\_LOAD\_STEP}$ is the allowed change in the output voltage due to the load step. In this case the target is to stay below a 3.5% change in the nominal output voltage.

The next criteria is to calculate the required capacitance to meet the output voltage ripple requirements using Equation 35. In this design, the maximum desired output voltage ripple is less than 0.8% of V_{OUTx}.

$$C_{OUTx\_RIPPLE}(F) = \frac{\Delta i_{Lx}(A)}{8 \times f_{SW}(Hz) \times \Delta V_{OUTx\_RIPPLE}(V)} \quad (35)$$

Where:

1. Δi_{Lx} is the ripple current in Amps (A). Refer to Table 9-3 for the values for each channel.
2. f_{SW} is the switching frequency of the converter in Hertz. In this case the selected switching frequency is 500kHz.
3. ΔV_{OUTx_RIPPLE} is the target output voltage ripple due to the switching nature of the converter. In this design the target is to be less than 0.8% of the nominal output voltage.

Finally, the ESR of the capacitor must be considered when meeting the output voltage ripple. The upper bound for the ESR can be calculated using Equation 36. The results for each channel are shown in Output Capacitor Design Calculations.

$$ESRx \leq \frac{\Delta V_{OUTx\_RIPPLE}(V)}{\Delta i_{Lx}(A)} \quad (36)$$

Table 9-4. Output Capacitor Design Calculations

V_{OUTx} (V)	$C_{OUTx\_LOAD\_STEP}$ (µF)	C_{OUTx_RIPPLE} (µF)	MAXIMUM ESR (mΩ)
0.8	428.57	29.67	8.43
1.2	285.71	27.15	9.21
1.5	228.57	25.25	9.90
1.8	190.48	19.11	13.08

Additional capacitance deratings for aging, temperature, and DC bias should be factored in, which increases the minimum required output capacitance value. Capacitors generally have limits to the amount of ripple current capacitors can handle without failing or producing excess heat. The selected bank of output capacitors must handle the ripple current calculated using Equation 30. For the selected inductor and nominal output voltage the ripple current for each case is shown on Table 9-2.

For this specific design, taking into consideration all of the above requirements, a 470µF T55 Tantalum capacitors is selected for each channel. The selected capacitor have a max ESR of 7mΩ, and a maximum RMS current rating of 5.66A. Additionally, a 0.1µF ceramic capacitor is added in parallel for high frequency filtering. This results in a total capacitance of 470.1µF. Using Equation 37 we can calculate the expected ripple voltage at each channel, the results are shown in Table 9-5

$$\Delta V_{OUTx\_RIPPLE} = \frac{\Delta i_{Lx}(A)}{8 \times f_{SW}(Hz) \times C_{OUTx}(F)} + [ESR(\Omega) \times \Delta i_{Lx}(A)] \quad (37)$$

Table 9-5. Expected Output Voltage Ripple

V_{OUTx} (V)	ΔV_{OUTx_RIPPLE} (mV)	ΔV_{OUTx_RIPPLE} in % of V_{OUTx}
0.8	5.72	0.72
1.2	7.85	0.65
1.5	9.13	0.61
1.8	8.29	0.46

9.2.2.4 Input Capacitor Selection

The input supply to the TPS7H410x must be well regulated with sufficient capacitor bypassing for proper electrical performance. While a minimum ceramic capacitor of at least 4.7µF effective capacitance near the PVIN and VIN inputs is required, additional bulk capacitance is generally required to handle the high input currents. Similar to the output capacitor selection, when selecting the input capacitors, take care to select capacitors with a sufficient voltage rating, temperature rating, and consideration of any effective capacitance changes due to DC bias effects. The capacitor must also have a ripple current rating greater than the maximum input current ripple as calculated using Equation 38.

$$i_{CIN\_RMSx}\left(A\right) = I_{OUTx}\left(A\right) \times \sqrt{\left(\frac{V_{OUTx}(V) \times \left[V_{IN\_MIN}(V) - V_{OUTx}(V)\right]}{V_{IN\_MIN}(V)^2}\right)} \tag{38}$$

The minimum input capacitance can then be calculated by using Equation 39 and selecting a maximum desired input ripple voltage, ΔV_{IN_RIPPLE}. For this design an input ripple voltage of ≤ 0.1% of the minimum VIN (4.5V) voltage is selected (ΔV_{IN_RIPPLE} = 4.5mV) .

$$C_{INx}(F) \geq \frac{0.25 \times I_{OUTx}(A)}{\Delta V_{IN\_RIPPLE}(V) \times f_{SW}(Hz)} \tag{39}$$

The input capacitor design calculations are shown in Table 9-6.

Table 9-6. Input Capacitor Design Calculations

V_{OUTx} (V)	i_{CIN_RMSx} (A)	LOWER BOUND FOR C_{INx} (µF)
0.8	1.15	333.33
1.2	1.33	
1.5	1.41	
1.8	1.47	

Note, however, that Equation 39 does not include the effects of ESR on the input ripple voltage. Therefore, additional capacitance is utilized. Specifically, 330µF Tantalum capacitors are used along with a 22µF and a 0.1µF ceramic capacitors are selected for a total input capacitance of 352.1µF. This is the selected input capacitor for each phase (or channel). Each set of capacitor is placed near the PVIN pins of each phase.

9.2.2.5 Soft-Start Capacitor Selection

The soft-start capacitor C_{SS_TRx}, determines the amount of time for the output voltage to reach nominal programmed value during power up. This is useful if a load requires a controlled voltage slew rate. This is also used if the output capacitance is large (as is typical with space grade buck converters), which requires a large amount of current to quickly charge the capacitor to the output voltage level. The large currents necessary to charge the capacitor can make the TPS7H410x reach the current limit, draw excessive current from the input power supply, or cause the input voltage rail to sag. Limiting the output voltage slew rate solves these problems. The soft-start capacitor value can be calculated using Equation 19 and Equation 20. The calculated value are shown in Table 9-7, along with the selected values. The center across temperature and voltage was used for V_{REFx} and I_{SS_TRx} for the calculations as: Equation 2, Equation 21, respectively.

Table 9-7. Soft-Start Capacitor Design Calculations

V_{OUTx} (V)	$t_{SS\_TRx\_NOMINAL}$ (ms)	$C_{SS\_TRx\_NOMINAL}$ (nF)	$C_{SS\_TRx\_SELECTED}$ (nF)
0.8	0.31	1.11	1.2
1.2	0.47	1.66	1.8
1.5	0.59	2.08	2.2
1.8	0.71	2.5	2.7

9.2.2.6 Undervoltage Lockout (UVLO) Set Point

An external resistor divider from VIN to GND is used to enable the TPS7H410x when a desired preset input voltage is reached. In effect, this acts as an adjustable UVLO. First, 3V is selected as the desired turn-on voltage ($V_{UVLO\_CHx\_TARGET}$). Next, R_{ENx_TOP} of 10kΩ is selected as a reasonable trade-off between a large enough resistor to minimize power dissipation, but low enough to prevent excessive noise coupling to a high impedance node. Equation 8 is then used to calculate an R_{ENx_BOT} of 2.53kΩ. The selected value is 2.61kΩ. Using Equation 9 and Equation 10 we can calculate the actual rising and falling UVLO, respectively. The $V_{UVLO\_CHx\_RISING}$ is calculated as, 2.93V and the $V_{UVLO\_CHx\_FALLING}$ as 2.42V.

9.2.2.7 Output Voltage Feedback Resistor Selection

The resistor divider network R_{FB_TOPx} and R_{FB_BOTx} is used to set the output voltage. For this design, 10kΩ was selected for R_{FB_TOPx}. Additionally, a 20Ω resistor was placed in series with R_{FB_TOPx} to aid in measuring the control loop. Using the combined value of 10.02kΩ and using Equation 1 the bottom resistors are calculated. The real (or selected) resistors were chosen, using the closest value to the calculation (using 0.1% tolerance). To minimize the error due to the reference voltage (V_{REFx}), the center across temperature, rather than the typical value is used for the calculations as presented on Equation 2.

Using the real (or selected) values the expected nominal and error are calculated using Equation 3 and Equation 4. The results are presented on Table 9-8.

Table 9-8. Feedback Resistors and Expected V_{OUTx} with Error

VOUTx (V)	CALCULATED R_{FB_BOTx} (kΩ)	SELECTED R_{FB_BOTx} (kΩ)	V_{OUTx} REAL (V)	V_{OUTx} ERROR (mV)
0.8	29.57	29.4	0.802	8.02
1.2	9.94	9.88	1.204	12.07
1.5	6.63	6.57	1.509	15.15
1.8	4.98	4.93	1.812	18.2

Lifetime drift data can similarly be added. Group C data can be used to aid in this calculation. For this example, assume the lifetime drift is minimal compared to the other sources of error and is therefore not added.

9.2.2.8 Slope Compensation Requirements

While one can chose different values of slope compensation for different applications, a commonly suggested value for slope compensation is defined as the output voltage divided by the inductor size as shown in Equation 27. Once the slope compensation is calculated the necessary RSC resistor can be calculated using Equation 26.

Table 9-9. Slope Compensation Design Calculations

VOUTx (V)	SC_{IDEAL} (A/µs)	RSC CALCULATED (kΩ)	RSC SELECTED (kΩ)
0.8	0.44	871.41	499
1.2	0.67	550.41	360
1.5	0.83	422.01	294
1.8	0.82	431.52	294

In this specific application example, there is more slope compensation than suggested which provided additional margin and quality of testing different configurations, hence the discrepancy between calculated and selected RSC resistors

9.2.2.9 Compensation Component Selection

The control loop of the TPS7H410x is described in Section 8.3.9. The component selection for compensating this device is as shown below. Other industry standard approaches for compensating a peak current mode control buck regulator are also acceptable.

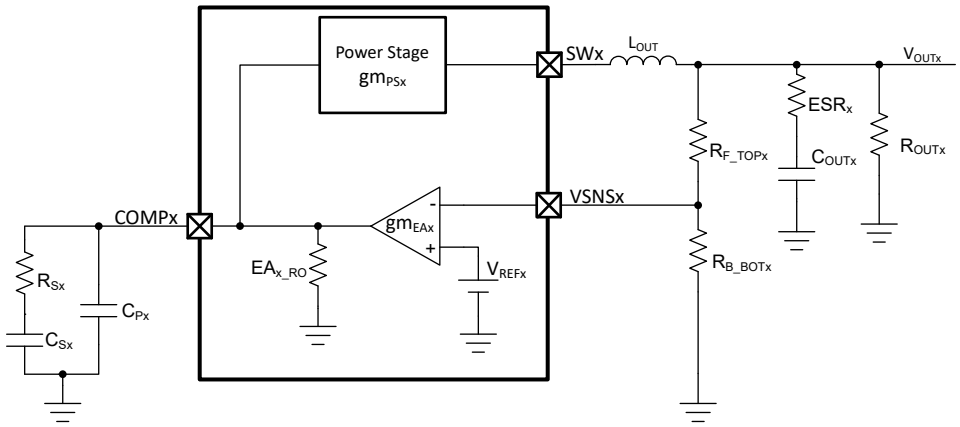


Figure 9-2. Type II Compensation with Simplified Loop

1. Determine the desired (or target) crossover frequency, f_{COx_TARGET}. A good starting method is to set the crossover frequency between 10% (1/10) and 20% (1/5) of the switching frequency. This generally provides a good transient response and make sure that the modulator poles do not degrade the phase margin. For this design, 25kHz was the selected target crossover frequency.
2. Determine the required gain from the compensated error amplifier using Equation 40:

$$A_{VMx} = \frac{2\pi \times f_{COx\_TARGET} \times C_{OUTx}}{gm_{PSx}} \quad (40)$$

   where gm_{PSx} is the power stage transconductance. (8.35S typ at 25°C)
3. R_{Sx} can be determined by Equation 41:

$$R_{Sx} = \frac{A_{VM}}{gm_{EAx}} \times \frac{V_{OUTx}}{V_{REFx}} \quad (41)$$

   where gm_{EAx} is the transconductance of the error amplifier (1672µS typical at 25°C) and V_{REF} is the reference voltage (0.597.5V as shown onEquation 2).
4. Calculate the power stage dominant pole determined by Equation 42:

$$f_{P\_PSx} = \frac{I_{OUTx}}{2\pi \times C_{OUTx} \times V_{OUTx}} \quad (42)$$

5. Place a compensation zero at the dominant pole by selecting C_{Sx} as determined by Equation 43:

$$C_{Sx} = \frac{1}{2\pi \times f_{P\_PSx} \times R_{Sx}} \quad (43)$$

6. Calculate the ESR zero from the output capacitor bank by Equation 44:

$$f_{Z\_ESRx} = \frac{1}{2\pi \times ESRx \times C_{OUTx}} \quad (44)$$

7. C_{Px} is used to cancel the zero from the equivalent series resistance (ESR) of the output capacitor C_{OUT}. It is calculated using Equation 45:

$$C_{Px} = \frac{1}{R_{Sx} \times 2\pi \times f_{Z\_ESRx}} \quad (45)$$

Note that if the ESR zero is higher than half the switching frequency, use half the switching frequency instead of the ESR zero in Equation 45.

Table 9-10. Compensation Components Calculation

V_{OUTx} (V)	A_{VMx} (V/V)	R_{Sx} (kΩ)	f_{P_PSx}(kHz)	C_{SX} (nF)	f_{Z_ESRx} (kHz)	C_{Sx} (pF)
0.8	8.84	7.08	1.27	17.7	48.37	464.67
1.2		10.62	0.85			309.78
1.5		13.28	0.68			247.83
1.8		15.93	0.56			206.52

Table 9-11. Selected Compensation Components

V_{OUTx} (V)	R_{Sx} (kΩ)	C_{Sx}(nF)	C_{Px} (pF)
0.8	6.98	18	470
1.2	10.5		330
1.5	13.3		220
1.8	16.2		220

Note that the components selected using these equations are often only starting values in a design. Optimizations can be made after lab testing to further improve the frequency response and provide a closer match to the desired crossover frequency.

9.2.3 Application Curves

The evaluation module for the TPS7H4104 was used to capture the shown waveforms below. The testing conditions were:

- VIN = PVIN = 5V
- Switching frequency (f_{SW}) = 500kHz
- V_{OUT1} = 0.8V, V_{OUT2} = 1.2V, V_{OUT3} = 1.5V and V_{OUT4} = 1.8V
- I_{OUTx}=3A

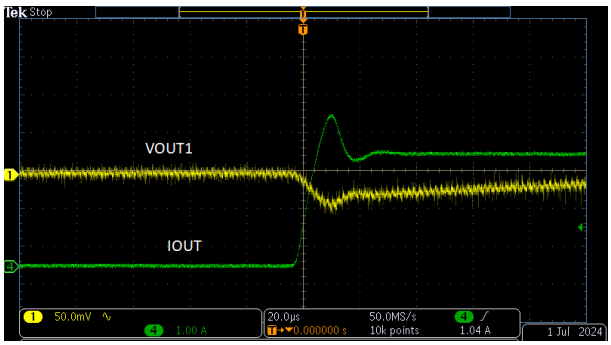


Figure 9-3. Rising Full Load Step in V_{OUT1}

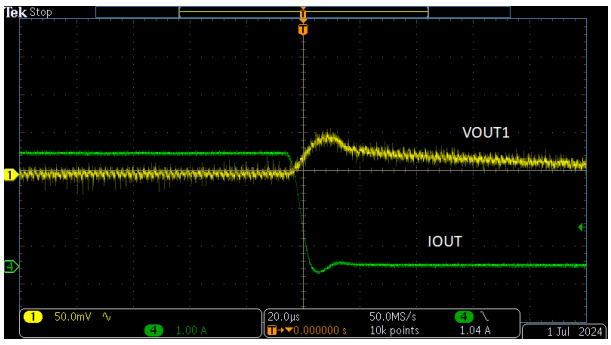


Figure 9-4. Falling Full Load Step in V_{OUT1}

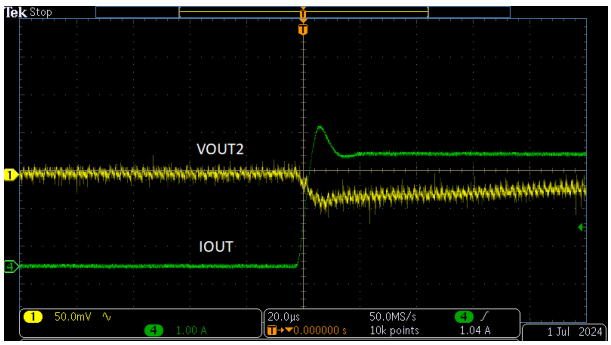


Figure 9-5. Rising Full Load Step in V_{OUT2}

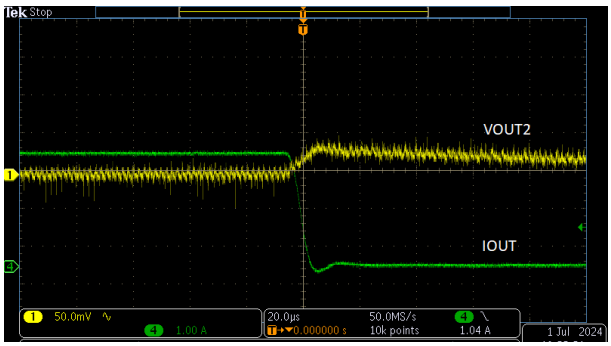


Figure 9-6. Falling Full Load Step in V_{OUT2}

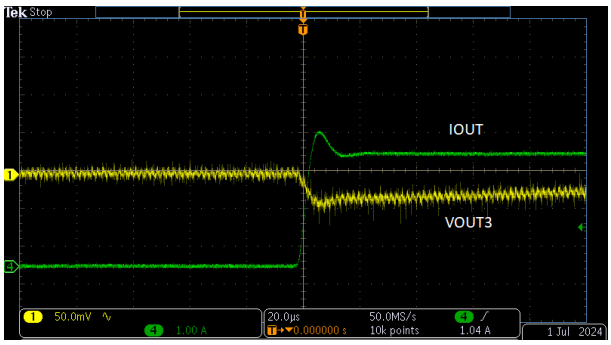


Figure 9-7. Rising Full Load Step in V_{OUT3}

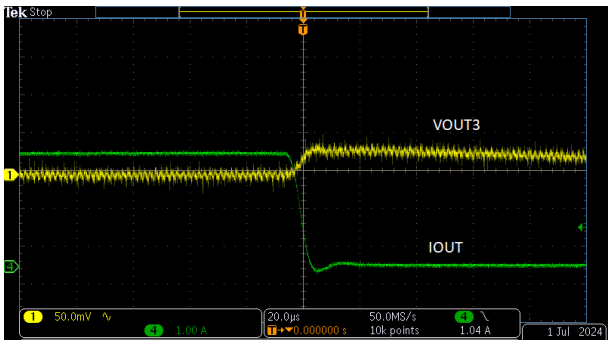


Figure 9-8. Falling Full Load Step in V_{OUT3}

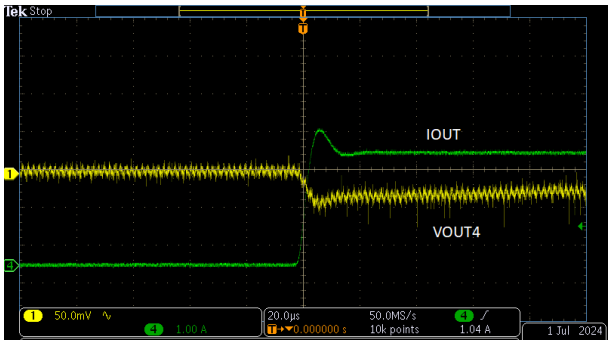


Figure 9-9. Rising Full Load Step in V_{OUT4}

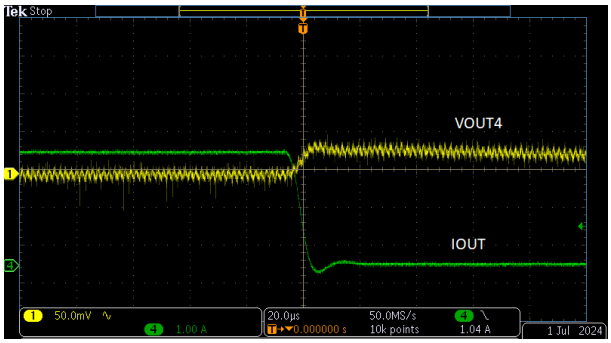
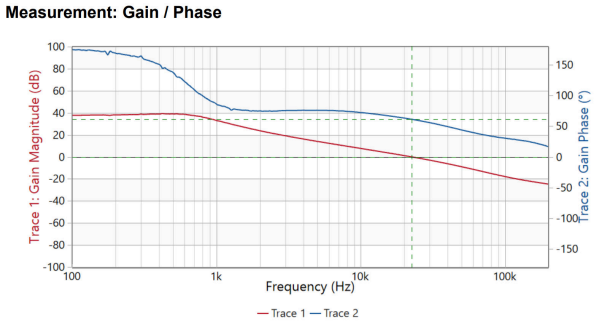
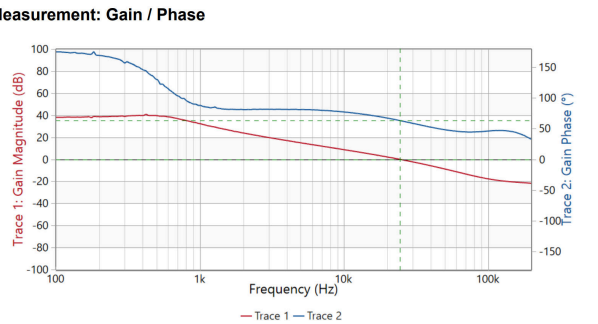


Figure 9-10. Falling Full Load Step in V_{OUT4}



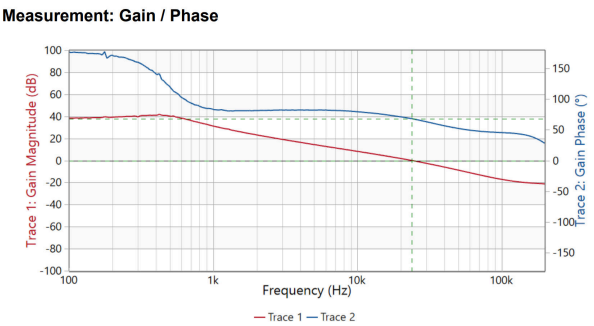
Crossover frequency measured to be 22.5kHz with 61.4 degrees of phase margin.

Figure 9-11. Complete Loop Bode Plot for V_{OUT1}



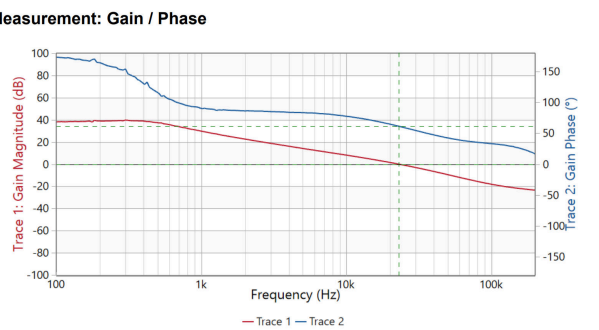
Crossover frequency measured to be 24.5kHz with 63.3 degrees of phase margin.

Figure 9-12. Complete Loop Bode Plot for V_{OUT2}



Crossover frequency measured to be 23.9kHz with 68.2 degrees of phase margin.

Figure 9-13. Complete Loop Bode Plot for V_{OUT3}



Crossover frequency measured to be 23kHz with 61.4 degrees of phase margin.

Figure 9-14. Complete Loop Bode Plot for V_{OUT4}

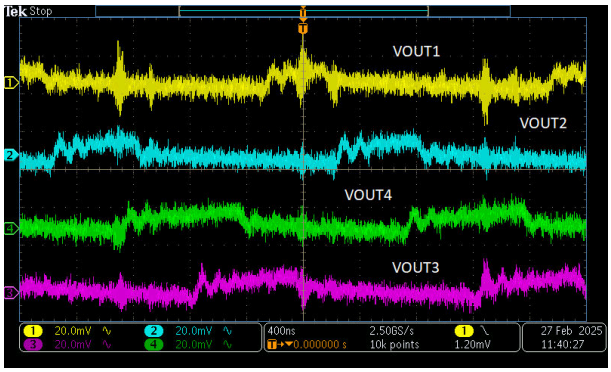


Figure 9-15. Output Voltage Ripple for V_{OUTx}

9.3 Parallel Operation

The TPS7H410x can be configured in parallel configuration to deliver maximum output currents of 12A with the TPS7H4104 model or 6A with the TPS7H4102 model. The phase shift by channel and device is shown on Table 9-12. The top (CH1 and CH4) and bottom (CH2 and CH3) channels have a relative phase shift of 180 degrees for easier paralleling of the channels.

The paralleling connection for channel 1 and channel 4 are shown on Figure 9-16, the assumption here is two channels are connected in parallel to supply up to 6A. However the connections can be extended to more than 2 phases in parallel. The current through each of the n paralleled devices is nominally 1/N, where N is the number of paralleled phases.

In parallel mode, the current mismatch due to error amplifier gm_{EAx} differences are minimized since the output of the error amplifiers (COMPx) are all electrically connected together. Therefore, the current mismatch is dominated by the mismatch of the individual power stage gm_{PSx} values. This parameter is specified in the Electrical Characteristics table across temperature, voltage, and TID.

Table 9-12. Relative Phase Shift by Channel for the TPS7H410x

DEVICE	CHANNEL NO.	RELATIVE PHASE SHIFT (°)
TPS7H4104	1	0
	2	90
	3	270
	4	180
TPS7H4102	1	0
	4	180

There are two approaches to compensate the TPS7H410x when in parallel mode:

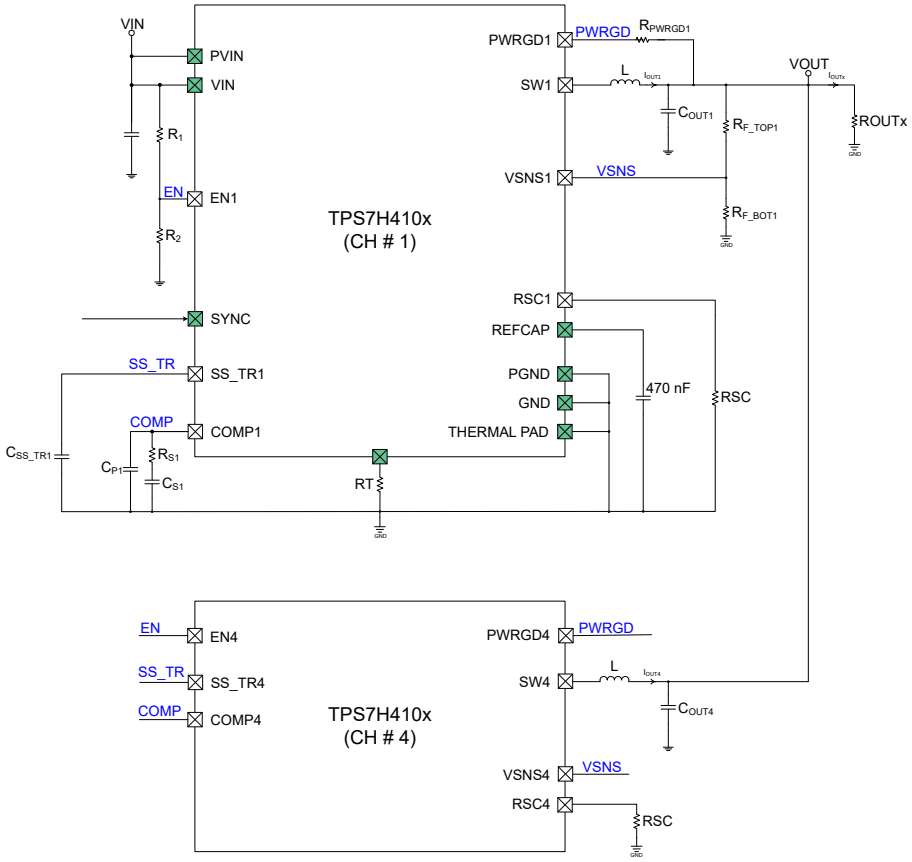
1. Compensate the complete system, using the total output capacitance C_{OUTx} and load current (I_{OUTx}). Using Figure 9-16 as reference, $C_{OUTx} = C_{OUT1} + C_{OUT2}$ and $I_{OUTx} = I_{OUT1} + I_{OUT2}$. Use the same procedure as presented on Section 9.2.2.9, with the exception of using Equation 46 to calculate the R_{Sx} calculation.
2. Compensate each channel individually by following the steps in Section 9.2.2.9. In this case the C_{OUTx} and I_{OUTx} needs to be scaled by 1/N, and there is no change to the R_{Sx} equation. The disadvantage of this approach is increased component count, but the advantage is that it may reduce the noise that gets injected into the COMP pin due to the physically close compensation components near each device.

$$R_{Sx\_PARALLEL} = \frac{1}{N^2} \times \frac{A_{VMx}}{gm_{EAx}} \times \frac{V_{OUTx}}{V_{REFx}} \quad (46)$$

In addition to the changes in the compensation procedure, the soft-start capacitance needs to be adjusted as now the soft-start current is: $I_{SS\_TRx\_PARALLEL} = I_{SS\_TRX}$ x N. Use this value to calculate the soft-start capacitance in Equation 16.

Note

The slope compensation resistor for each phase must be the same value and be present for each phase.



The green pins are settings that apply to all channels of the TPS7H410x, SYNC is an optional input.

Figure 9-16. Parallel Configuration Showing Channels 1 and 4 on a Single TPS7H410x Device

The procedure to parallel N phases of the TPS7H410x is:

- Only a single feedback network is utilized to configure the output voltage by tying all VSNS nodes together.
- Only a single soft-start capacitor is required with all SSx pins connected (or shorted) together.
  - The soft-start current is incremented by the number of phases (N).
- An single resistive divider is used to set the external UVLO with all ENx pins connected together.
- Connect all PWRGD pins together and use a single pull-up resistor to have a wired-OR power good signal.
- Connect all COMPx pins together and compensate the loop accordingly as discussed above.

9.3.1 Input and Output Capacitance Reduction

One of the benefits of paralleling multiple phases is the reduction in input and output capacitance for steady-state requirements, when compared to a single phase and same total load.

Note

The equations under discussion in this section are valid when the phase shift between phases equals 360/N degrees (where N is the number of phases). This applies when specific channels are operated in parallel, such as channels 1 and 4, channels 2 and 3, or all channels 1 through 4. It is also improtant to keep in mind this reduction is valid at steady-state conditions, often times the input and output capacitance values are dominated by the characteristics of the load transient.

9.3.1.1 Output Capacitance Reduction

When phases operate concurrently, they charge and discharge the output capacitance at different times based on their active status. This results in the total current (the sum of all phase currents) having a smaller peak-to-peak value. Since the AC component of this total current is what gets absorbed by the output capacitance (C_{OUTx}), the smaller ripple current directly leads to lower output voltage ripple. For a visual representation of this effect, refer to the Figure 9-17.

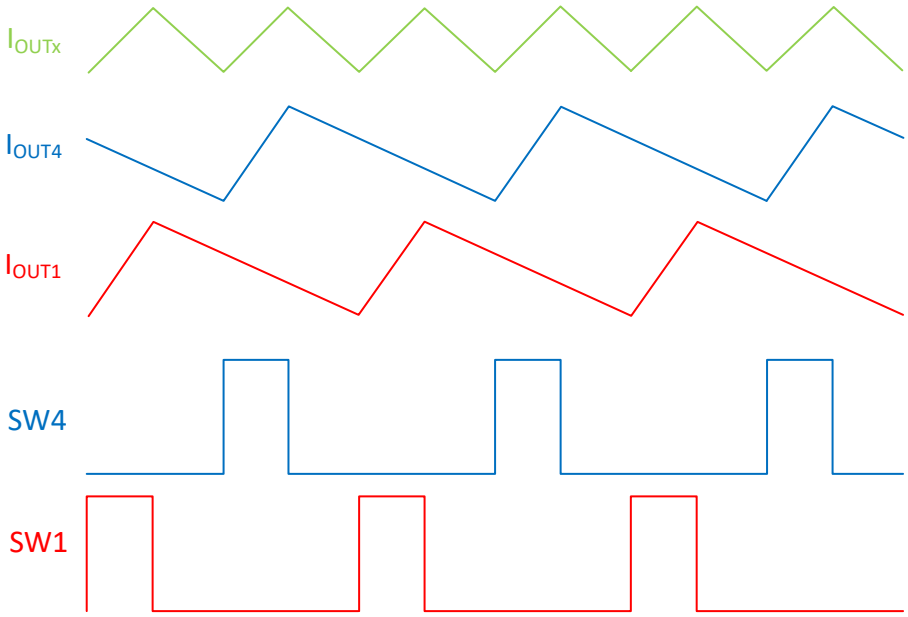


Figure 9-17. Inductor Ripple Currents for SW1 and SW4 in Parallel

The reduced ripple output current factor can be calculated using Equation 47. This factor can be seen in Figure 9-18 for 2 and 4 channels (or phases) in parallel. This factor is applied to Equation 30 to calculate the I_{OUTx} ripple current.

$$\Delta i_{L\_PARALLEL\_FACTOR} = \frac{N}{D \times (1-D)} \times \left(D - \frac{m}{N}\right) \times \left(\frac{1+m}{N} - D\right) \quad (47)$$

where:

- D is the duty cycle in numerical value (0 to 1).
- N is the number of parallel phases.
- m=floor (N × D)

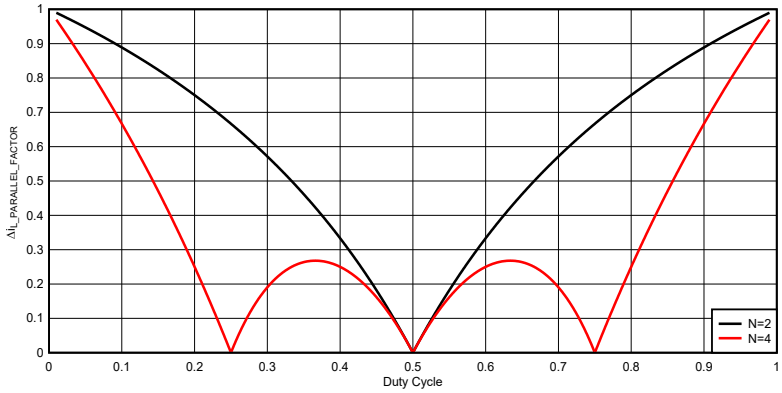


Figure 9-18. $\Delta i_{L\_PARALLEL\_FACTOR}$ vs Duty Cycle

9.3.1.2 Input Capacitance Reduction

In a multiphase system, the input RMS current is lower compared to a single-phase system with the same total load (I_{OUTx}). This reduction allows for smaller input capacitance while meeting the same input ripple specifications. An additional benefit is reduced self-heating due to the lower current through the equivalent series resistance (ESR) of the capacitors. Figure 9-19 shows the simplified input current waveforms for CH1 and CH4 in parallel when compared to a single phase (in dashed-line). The input current RMS reduction can be calculated using Equation 48. This factor is applied to the single phase RMS current as calculated per Equation 38. Figure 9-20 shows the $i_{CIN\_RMS\_PARALLEL\_FACTOR}$ vs duty cycle.

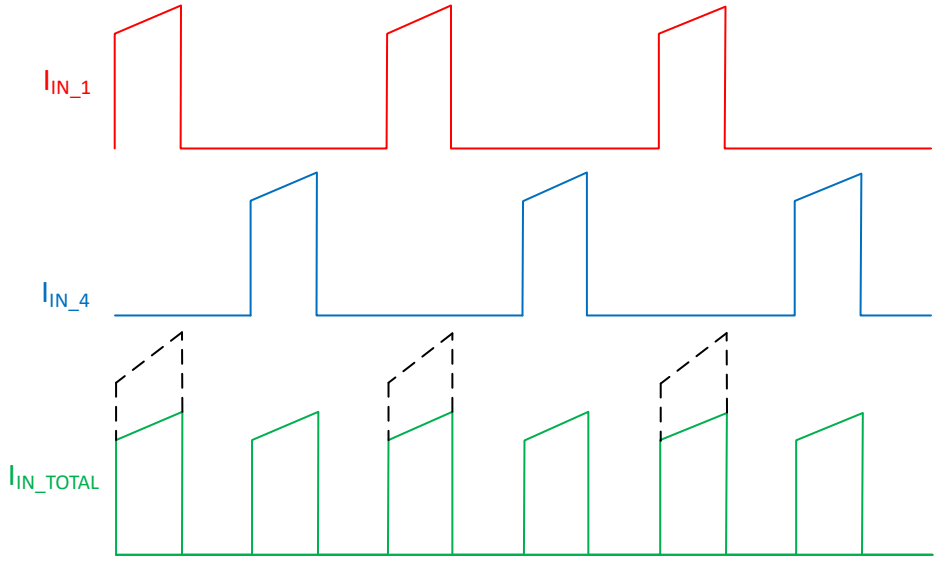


Figure 9-19. Input Current Waveform for SW1 and SW4 in Parallel

$$i_{CIN\_RMS\_PARALLEL\_FACTOR} = \sqrt{\left(D - \frac{m}{N}\right) \times \left(\frac{1+m}{N} - D\right)} \quad (48)$$

Where:

- D is the duty cycle in numerical value (0 to 1).
- N is the number of parallel phases.
- m=floor (N × D)

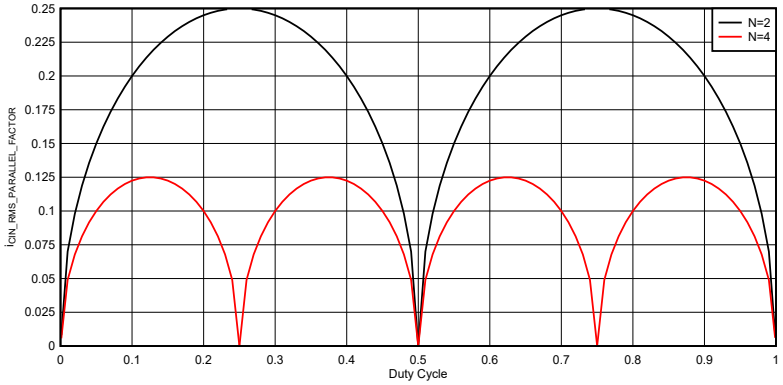


Figure 9-20. $i_{CIN\_RMS\_PARALLEL\_FACTOR}$ vs Duty Cycle

9.4 Termination Guidelines for Unused Channels

When not all channels are used (or needed) in the application, the recommendation is to terminate the unused channel pins as described below to avoid floating nodes:

1. ENx ≥ 10kΩ pull-down to GND.
2. COMPx is internally pull down to GND when $V_{ENx} \leq V_{EN\_FALLING}$ (or ENx = low)
   - If a external pull-down is desired connect a resistor ≥ 10kΩ.
3. RSCx ≥ 10kΩ pull-down to GND.
4. SS_TRx is internally pull-down to GND via a 364Ω (typ).
5. VSNSx ≥ 10kΩ pull-down to GND.
6. SWx ≥ 10kΩ pull-down to GND.
7. PWRGDx ≥ 10kΩ pull-down to GND.

9.5 Power Supply Recommendations

The TPS7H410x is designed to operate from an input voltage supply range between 3V and 7V. This supply voltage must be well regulated. Power supplies must be well bypassed for proper electrical performance. This includes a minimum of one 4.7µF (after derating) from PVIN to GND (one across each pair of PVIN pin, next to each SWx), and one 1µF from VIN to GND ceramic capacitors, type X7R or better. PVIN and VIN must be the same voltage, and users are recommended to externally connect PVIN and VIN. Additional local ceramic bypass capacitance can be required in systems with small input ripple specifications, as well as additional bulk capacitance if the TPS7H410x device is located more than a few inches away from the device's input power supply. Bypass capacitors are recommended to be placed as close as possible to the input pins, and have a low impedance path to GND. Larger values of bypass capacitance at the output improve the response to radiation induced transients.

9.6 Layout

9.6.1 Layout Guidelines

- Layout is a critical portion of good power supply design. See Section 9.6.2 for a PCB layout example.
- Users are recommended to include a large topside area filled with ground. This top layer ground area can be connected to the internal ground layers using vias at the input bypass capacitor, the output filter capacitor, and directly under the TPS7H410x device to provide a thermal path from the exposed thermal pad to ground. The topside ground area together with the internal ground plane must provide adequate heat dissipating area.
- Users are recommended that the thermal pad under the TPS7H410x is tied to GND on internal ground layers utilizing vias. The thermal pad does not need to directly connect to ground on the top layer to provide noise isolation between the thermal pad ground and the topside PGND, which can be noisy.
- There are several signal paths that conduct fast changing currents or voltages that can interact with stray inductance or parasitic capacitance to generate noise or degrade the power supply's performance. To help eliminate these problems, the PVIN pin can be bypassed to ground with a low ESR ceramic bypass capacitor with an X7R dielectric.
- Take care minimize the loop area formed by the bypass capacitor connections, the PVIN pins, and the ground connections.
- The VIN pin must also be bypassed to ground using a low ESR ceramic capacitor with an X7R dielectric. Make sure to connect this capacitor to the quieter analog ground trace (if utilized) rather than the power ground trace of the PVIN bypass capacitor.
- Since the SW connection is the switching node, the output inductor can be located close to the SW pins and the PCB conductor area minimized to prevent excessive capacitive coupling.
- The output filter capacitor ground can use the same power ground as the PVIN input bypass capacitor. Try to minimize this conductor length while maintaining adequate width.
- Keep the feedback trace away from inductor EMI and other noise sources. Run the feedback trace as far from the inductor, switch (SW) node, and noisy power traces as possible. Avoid routing this trace directly under the output inductor if possible. If not possible, make sure that the trace is routed on another layer with a ground layer separating the trace and inductor.
- Keep the resistive divider used to generate the VSNSx voltage as close to the device pin as possible to reduce noise pickup.
- The RT and COMP pins are sensitive to noise, so components around these pins can be located as close as possible to the IC and routed with minimal trace lengths.
- Make all of the power (high current) traces as short, direct, and thick as possible.
- Users can possibly obtain acceptable performance with alternate PCB layouts.

9.6.2 Layout Example

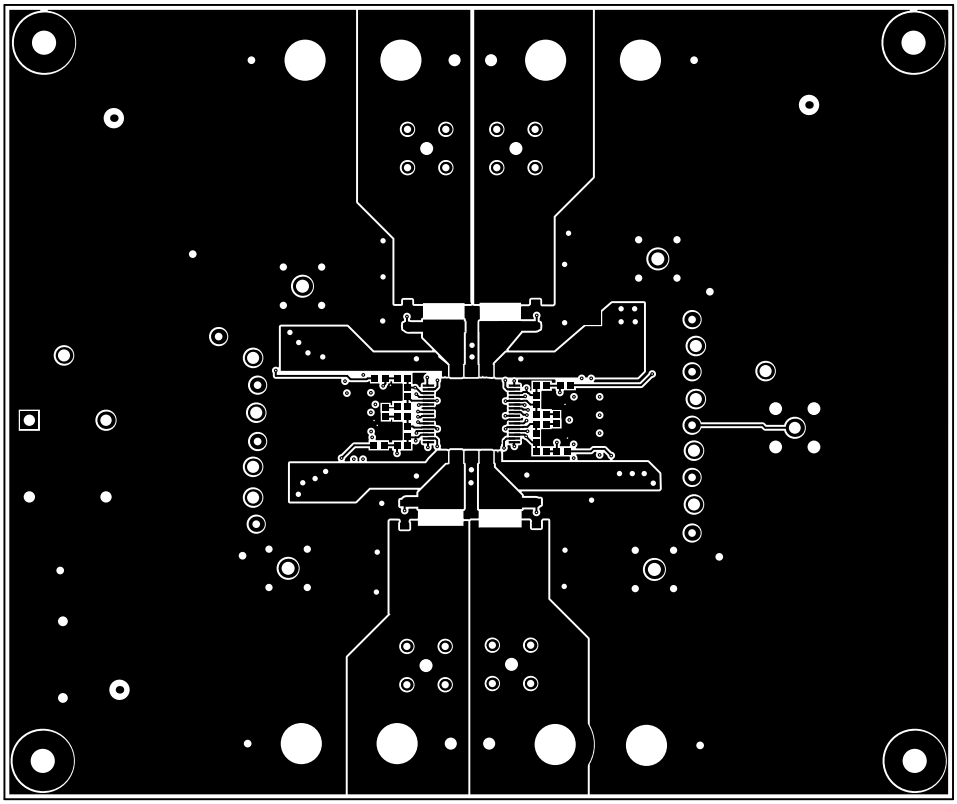


Figure 9-21. PCB Layout Example-Top Layer

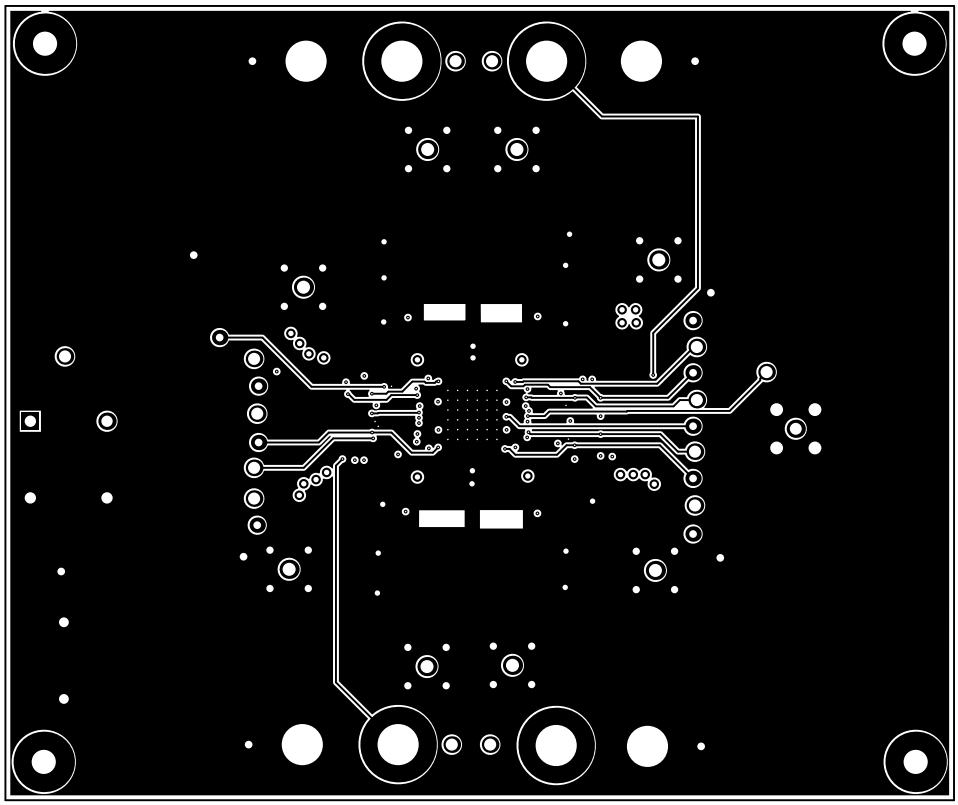


Figure 9-22. PCB Layout Example-Internal Layer 1

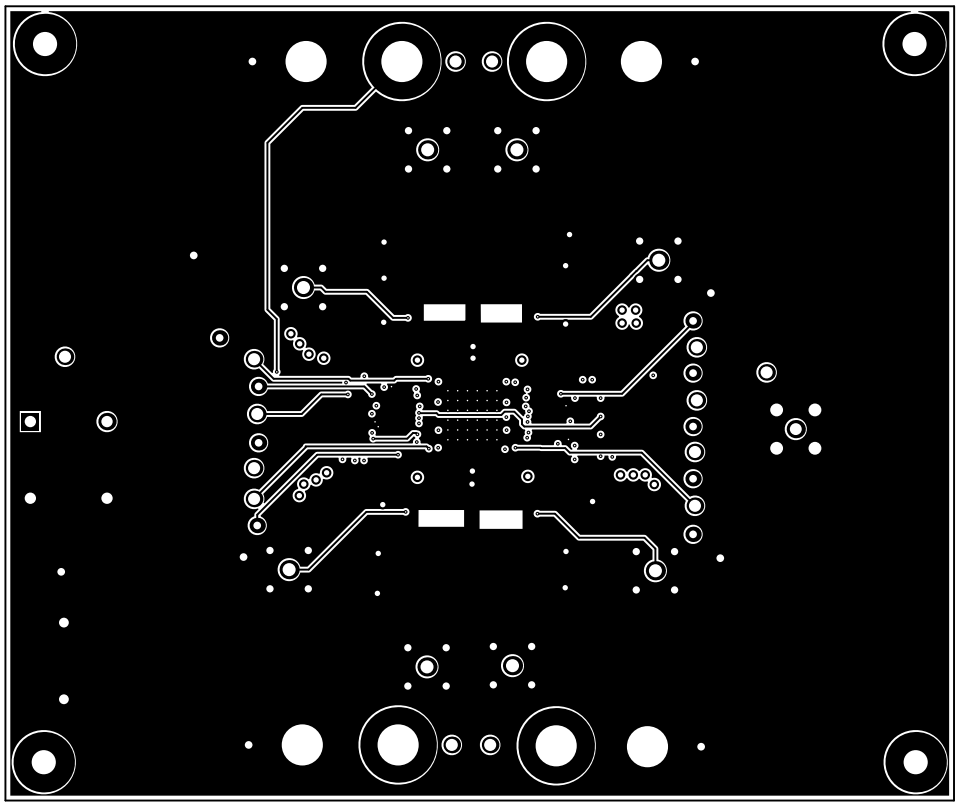


Figure 9-23. PCB Layout Example-Internal Layer 2

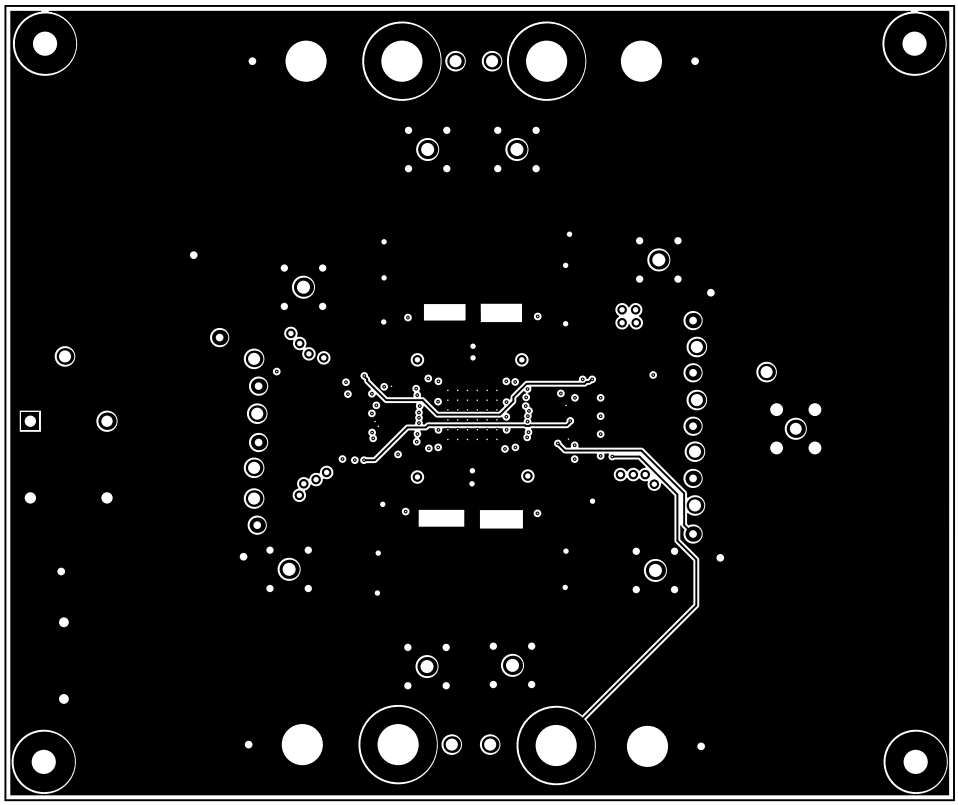


Figure 9-24. PCB Layout Example-Internal Layer 3

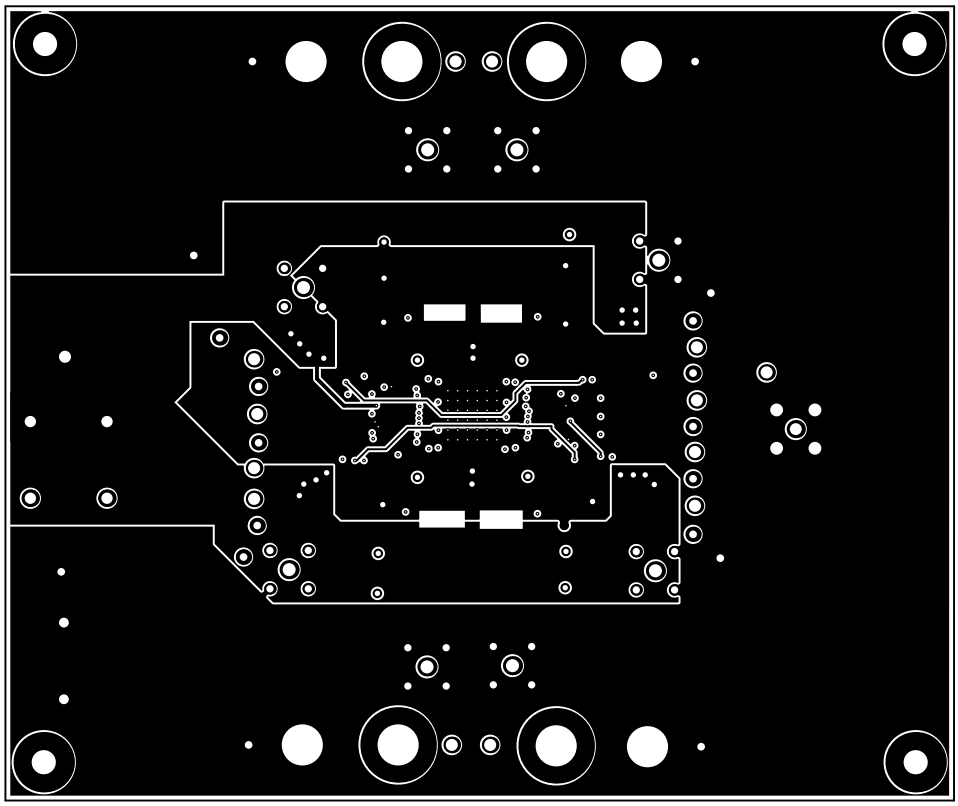


Figure 9-25. PCB Layout Example-Internal Layer 4

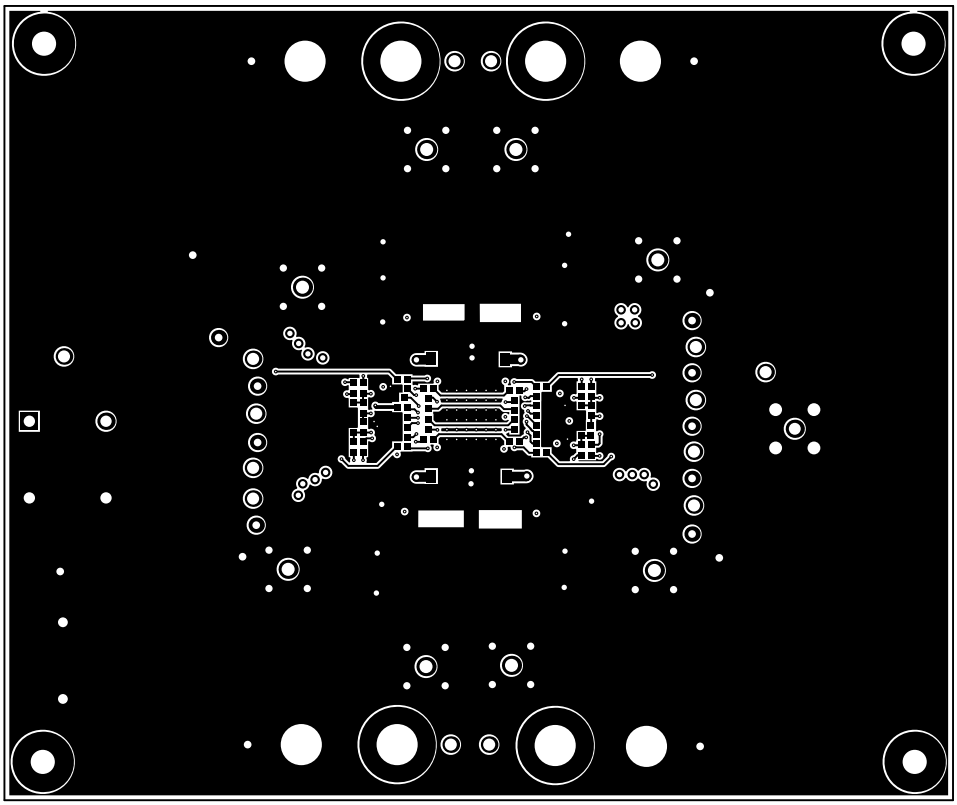


Figure 9-26. PCB Layout Example-Bottom Layer

10 Device and Documentation Support

10.1 Documentation Support

10.1.1 Related Documentation

- Texas Instruments, *TPS7H4104 Evaluation Module (EVM)* user's guide
- Texas Instruments, *TPS7H4102 Evaluation Module (EVM)* user's guide
- Texas Instruments, *TPS7H4104-SEP Total Ioninzing Dose (TID) Report*
- Texas Instruments, *TPS7H4102-SEP Total Ioninzing Dose (TID) Report*
- Texas Instruments, *TPS7H4104-SEP and TPS7H4104-SP QMLP Neutron Displacement Damage (NDD) Characterization Report*
- Texas Instruments, *TPS7H4102-SEP and TPS7H4102-SP QMLP Neutron Displacement Damage (NDD) Characterization Report*
- Texas Instruments, *TPS7H4104-SEP Single-Event-Effects (SEE) Report*
- Texas Instruments, *TPS7H4102-SEP Single-Event-Effects (SEE) Report*
- Vendor Item Drawing

10.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

10.3 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

10.4 Trademarks

TI E2E™ is a trademark of Texas Instruments.
All trademarks are the property of their respective owners.

10.5 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

10.6 Glossary

TI Glossary	This glossary lists and explains terms, acronyms, and definitions.

11 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision B (September 2025) to Revision C (November 2025)	Page
• Changed TPS7H410x-SEP from Advanced Information to Production Data	1
• Added *Output Inductor Selection* as a guideline to minimize jitter at small currents using bigger K_{Lx} factor	56
• Added the *Parallel Operation* section	66

Changes from Revision A (August 2025) to Revision B (September 2025)	Page
• Added TPS7H4102MPAPTSEP part to Device Information table	1
• Fixed calculation on Table 9-10	61

Changes from Revision * (March 2025) to Revision A (August 2025)	Page
• Updated input ripple current equation in *Input Capacitor Selection* section	59
• Added the *Termination Guidelines for Unused Channels* section	70
• Added *Documentation Support* to the *Device and Documentation Support* section	76

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
PTPS7H4104PAPTSEP.A	Active	Preproduction	HTQFP (PAP) | 64	250 | SMALL T&R	-	Call TI	Call TI	-55 to 125	
TPS7H4102MPAPTSEP	Active	Production	HTQFP (PAP) | 64	250 | SMALL T&R	Yes	NIPDAU	Level-3-260C-168 HR	-55 to 125	TPS7H4102M PAPSEP
TPS7H4104MPAPTSEP	Active	Production	HTQFP (PAP) | 64	250 | SMALL T&R	Yes	NIPDAU	Level-3-260C-168 HR	-55 to 125	TPS7H4104M PAPSEP
V62/25661-01XE	Active	Production	HTQFP (PAP) | 64	250 | SMALL T&R	-	NIPDAU	Level-3-260C-168 HR	-55 to 125	TPS7H4104M PAPSEP
V62/25661-02XE	Active	Production	HTQFP (PAP) | 64	250 | SMALL T&R	-	NIPDAU	Level-3-260C-168 HR	-55 to 125	TPS7H4102M PAPSEP

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

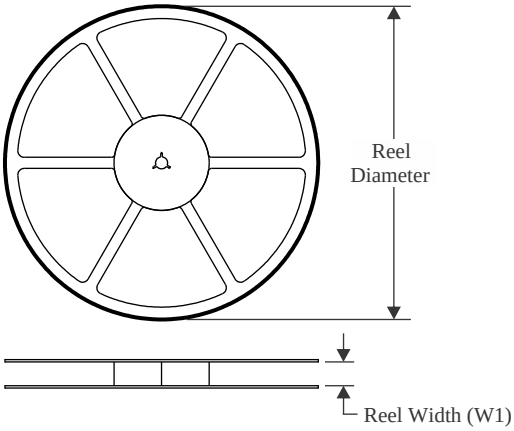
(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

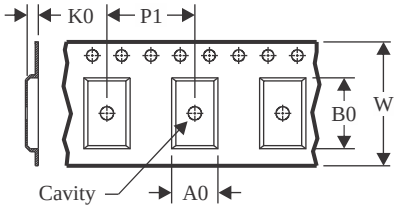
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

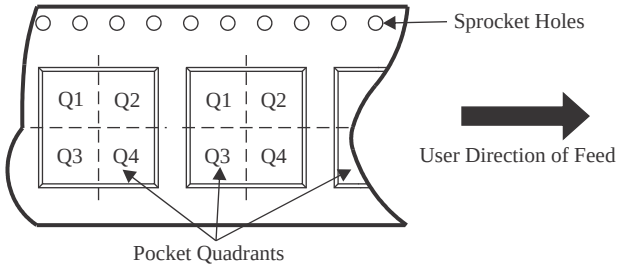


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

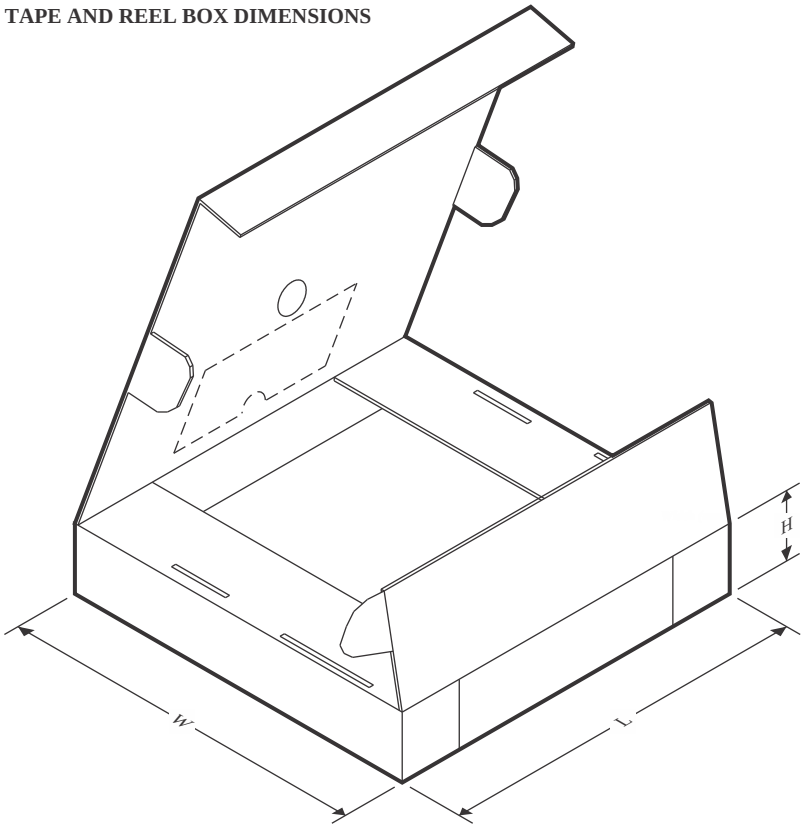
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS7H4102MPAPTSEP	HTQFP	PAP	64	250	330.0	24.4	13.0	13.0	1.5	16.0	24.0	Q2
TPS7H4104MPAPTSEP	HTQFP	PAP	64	250	330.0	24.4	13.0	13.0	1.5	16.0	24.0	Q2

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS7H4102MPAPTSEP	HTQFP	PAP	64	250	367.0	367.0	55.0
TPS7H4104MPAPTSEP	HTQFP	PAP	64	250	367.0	367.0	55.0

GENERIC PACKAGE VIEW

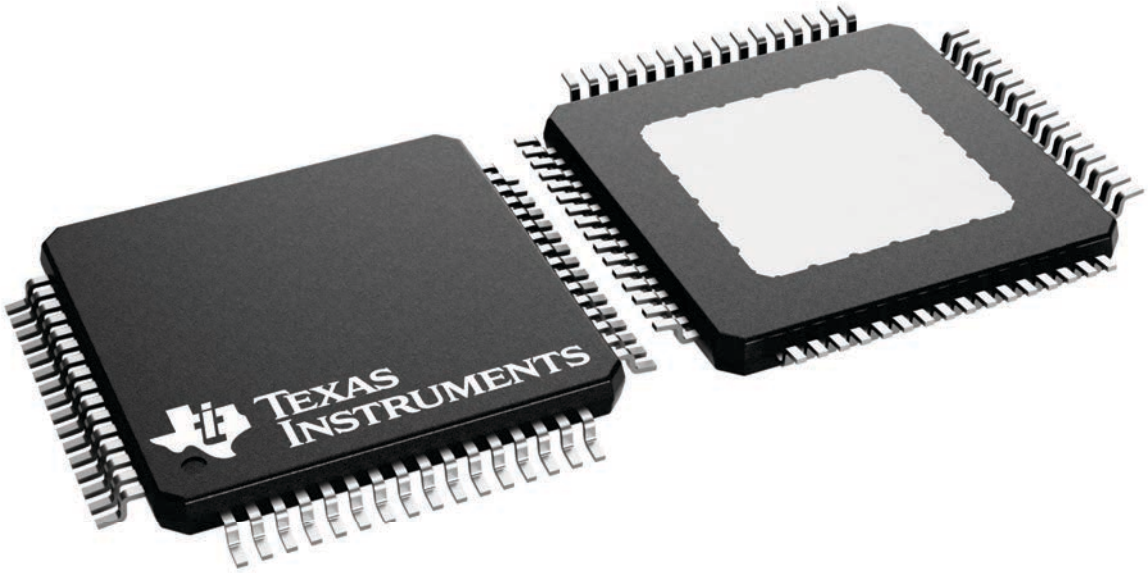
PAP 64

HTQFP - 1.2 mm max height

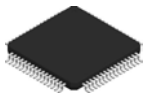
10 x 10, 0.5 mm pitch

QUAD FLATPACK

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



4226442/A

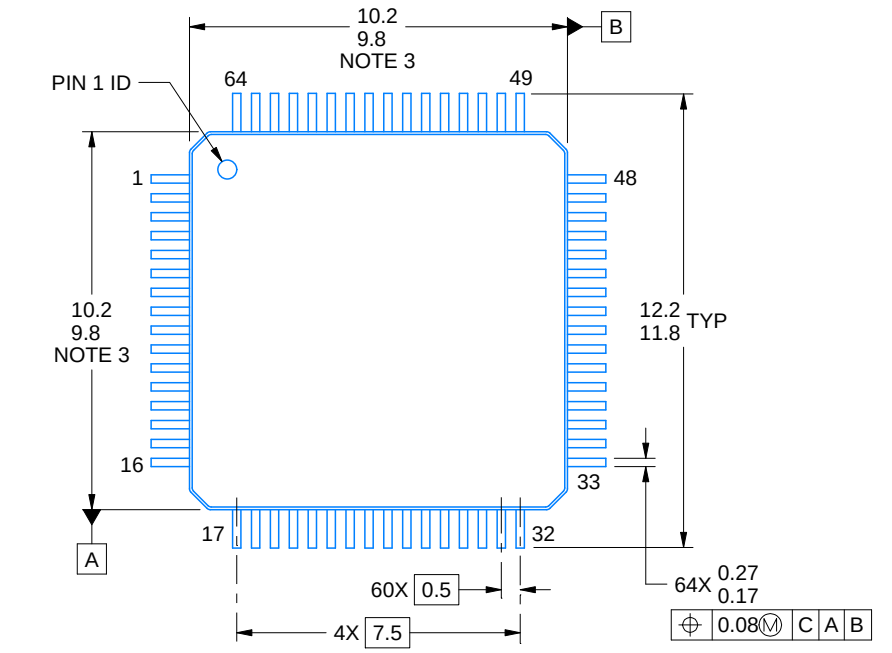


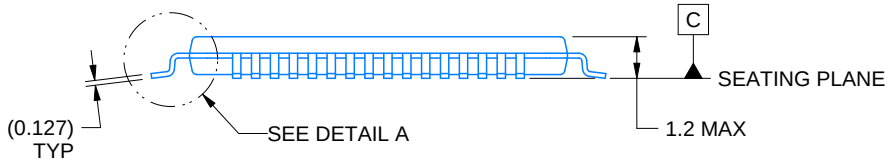
PACKAGE OUTLINE

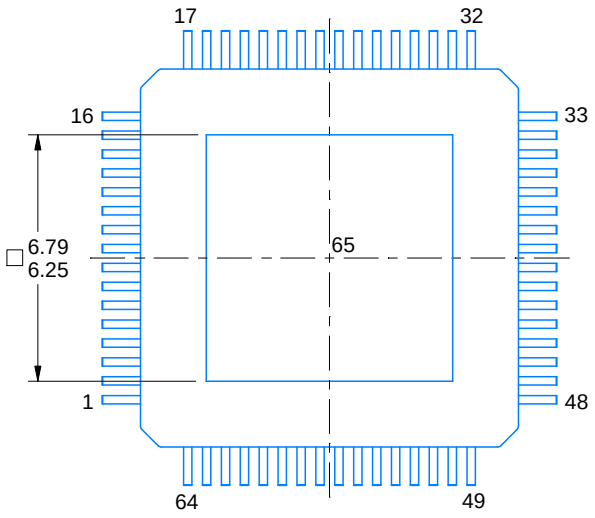
PAP0064R

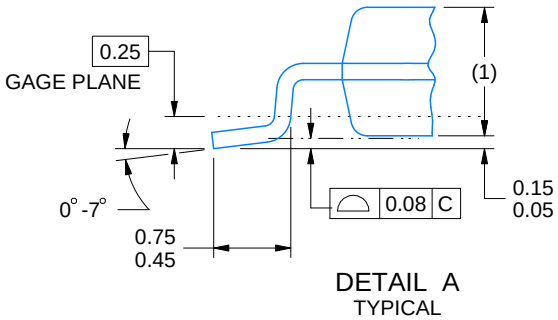
PowerPAD™ TQFP - 1.2 mm max height

PLASTIC QUAD FLATPACK







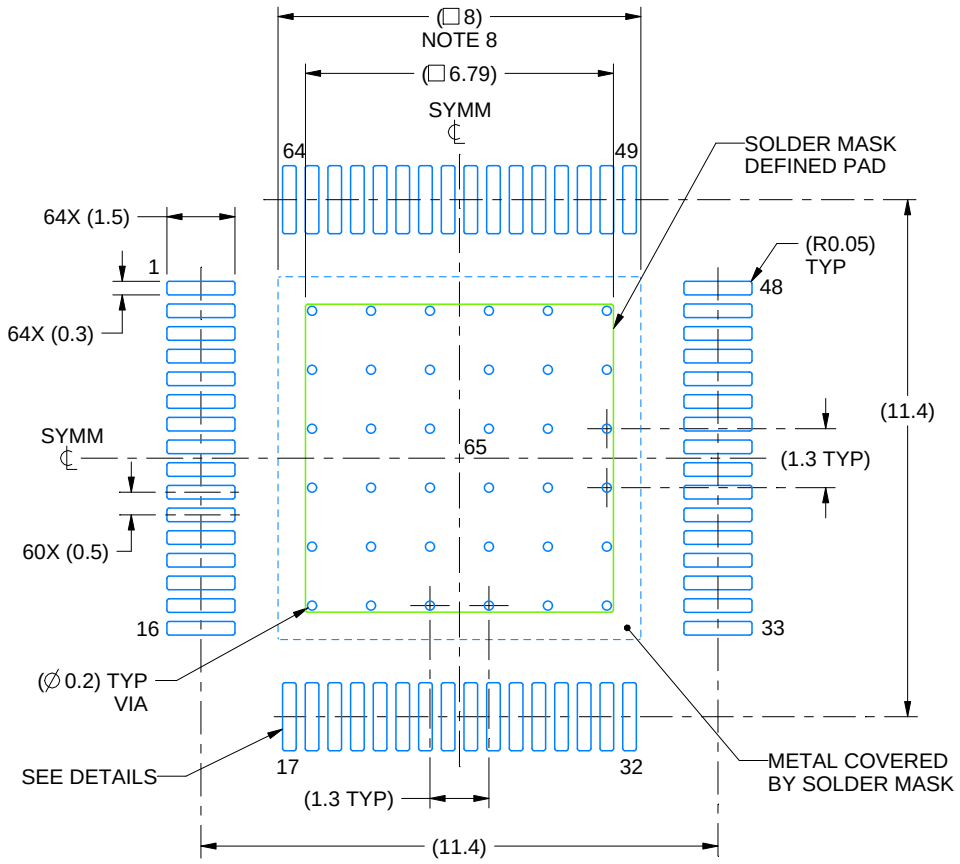


4230159/B 08/2024

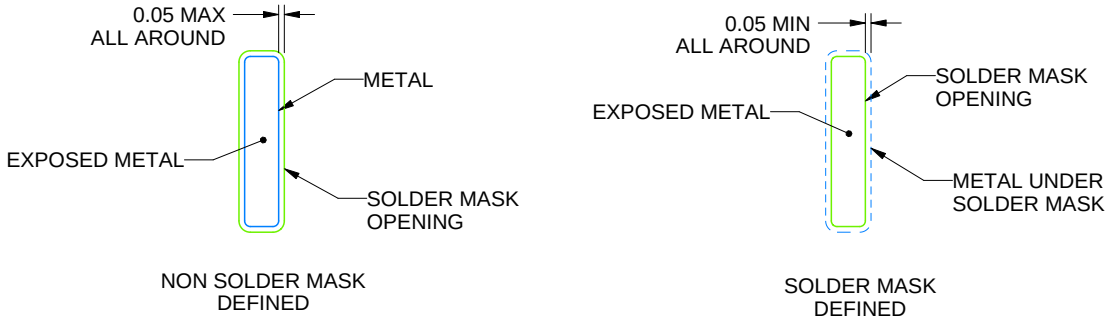
PowerPAD is a trademark of Texas Instruments.

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs.
4. Strap features may not be present.
5. Reference JEDEC registration MS-026.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:6X



SOLDER MASK DETAILS

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NOTES: (continued)

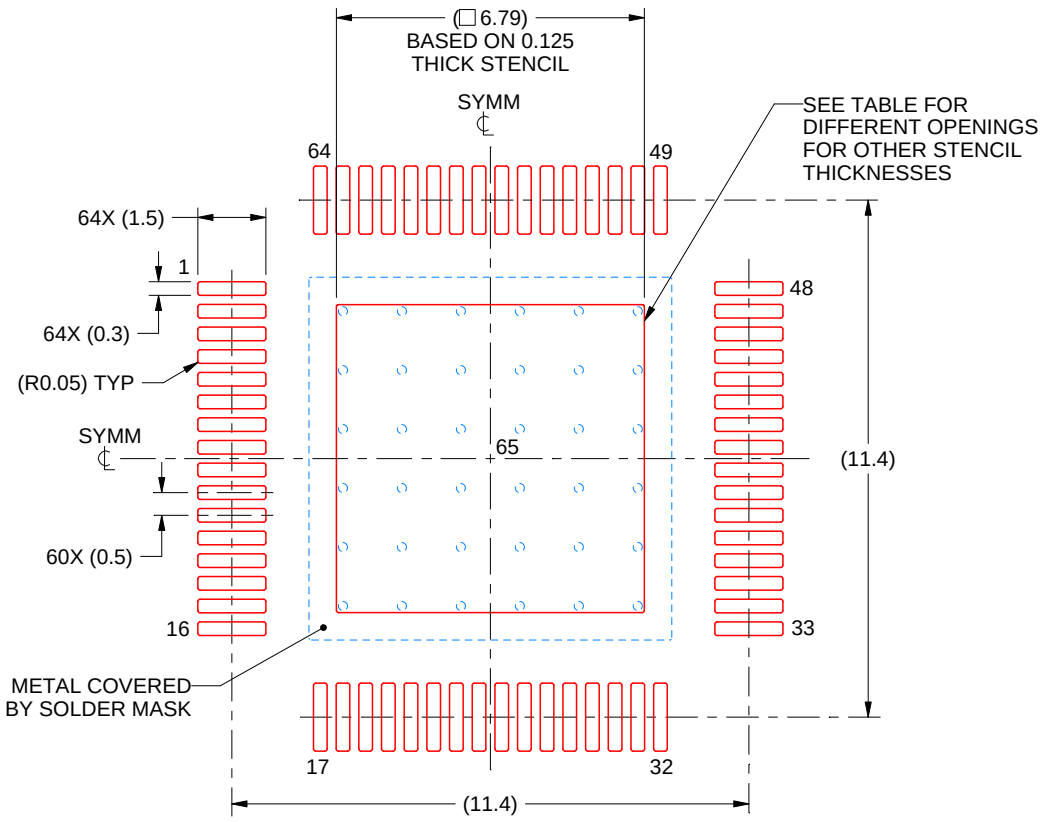
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. This package is designed to be soldered to a thermal pad on the board. See technical brief, Powerpad thermally enhanced package, Texas Instruments Literature No. SLMA002 (www.ti.com/lit/slma002) and SLMA004 (www.ti.com/lit/slma004).
9. Vias are optional depending on application, refer to device data sheet. It is recommended that vias under paste be filled, plugged or tented.
10. Size of metal pad may vary due to creepage requirement.

EXAMPLE STENCIL DESIGN

PAP0064R

PowerPAD™ TQFP - 1.2 mm max height

PLASTIC QUAD FLATPACK



SOLDER PASTE EXAMPLE
EXPOSED PAD
100% PRINTED SOLDER COVERAGE BY AREA
SCALE:6X

STENCIL THICKNESS	SOLDER STENCIL OPENING
0.1	7.59 X 7.59
0.125	6.79 X 6.79 (SHOWN)
0.15	6.20 X 6.20
0.175	5.74 X 5.74

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NOTES: (continued)

11. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
12. Board assembly site may have different recommendations for stencil design.

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