TPS92543-Q1 65V Automotive Synchronous BOOST Controller, 2A Synchronous CC BUCK and Bypass FET Controllers

1 Features

- AEC-Q100 qualified for automotive applications
  - Grade 1: –40°C to 125°C ambient operating temperature
  - Device HBM classification level H1C
  - Device CDM classification level C5
- Functional Safety-Capable
  - Documentation available to aid functional safety system design
- 4.5V to 65V wide input voltage range
- Synchronous Buck with integrated switches
  - Up to 2A continuous output current with 4% accuracy
- Synchronous BOOST controller
  - Programmable output voltage up to 65V
- Six floating gate drivers for shunt-FET dimming
  - Programmable width and phase setting
  - Programmable PWM frequency
- BOOST and BUCK spread-spectrum for EMI mitigation
- BUCK switch thermal protection
- UART serial communication
  - Internal oscillator for system clock
  - LMM compatible
- Internal EEPROM
  - Default settings
  - Customer calibration data

2 Applications

- Automotive headlight and adaptive LED driving module

3 Description

The TPS92543 device contains a synchronous BOOST controller and a monolithic synchronous buck LED driver with a wide 4.5V to 65V operating BUCK input voltage range. The TPS92543 includes two sub-strings of three series connected floating bypass FET controllers.

The synchronous BOOST controller implements a peak current-mode controller to operate in constant voltage mode. The Boost can be programmed to operate as dual-phase together with another TPS92543. The output voltage can be programmed using a programmable 8-bit DAC.

The monolithic synchronous BUCK implements an adaptive on-time average current mode control and is designed to be compatible with shunt FET dimming techniques and LED matrix manager-based dynamic beam headlamps. The adaptive on-time control provides near constant switching frequency that can be set between 100kHz and 1.0MHz. Inductor current sensing and closed-loop feedback enable better than ±4% accuracy over wide input voltage, output voltage and ambient temperature range.

The TPS92543 incorporates two sub-strings of three series connected floating bypass FET controllers to perform LED shunt FET dimming. Each controller can perform FET dimming with segment voltages of up to 55V. The device includes programmable registers for phase shift and pulse width of each individual segment.

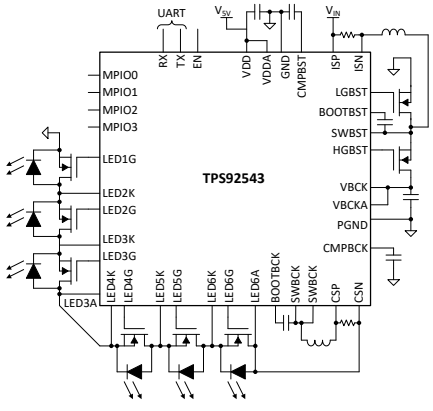
The TPS92543 includes an internal oscillator. The UART serial interface is compatible with TPS9266x, and TPS9254x devices. The internal EEPROM can store system defaults as well as calibration and lighting module data. The four configurable MPIOs can be configured as digital inputs or outputs, or ADC input for use with system temperature compensation, LED binning and coding.

The TPS92543-Q1 is available in a 7.0mm × 7.0mm thermally-enhanced 48-pin HTQFP package with top-exposed pad.

Device Information

PART NUMBER(1)	PACKAGE	PACKAGE SIZE (NOM)(2)
TPS92543-Q1	PKD, PHP (HTQFP, 48)	7.0mm × 7.0mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.
(2) The package size (length x width) is a nominal value and includes pins, where applicable



Simplified Schematic

Table of Contents

4 Pin Configuration and Functions

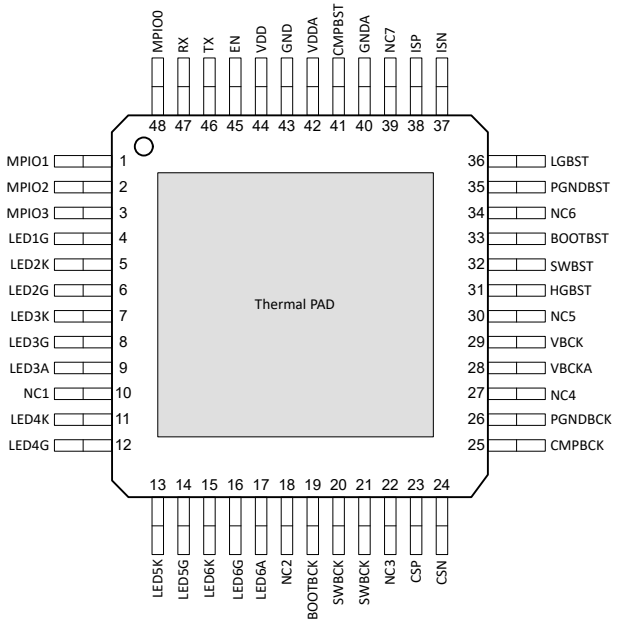


Figure 4-1. PKD Package 48-Pin HTQFP (Top-Exposed PAD) Top View

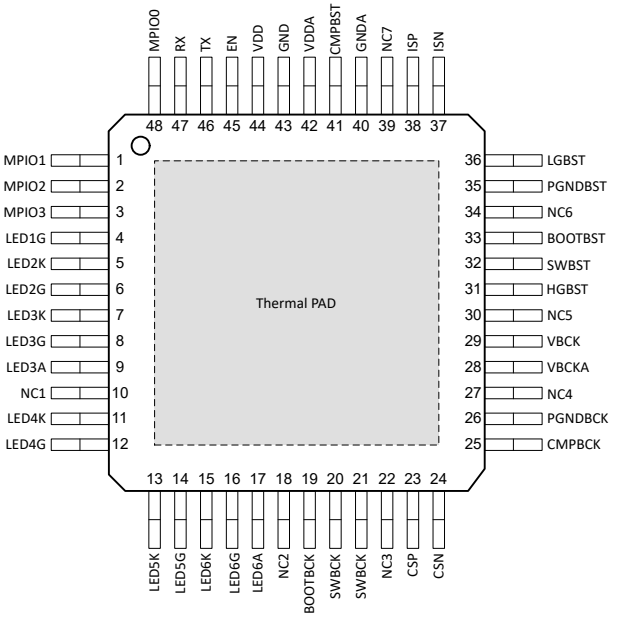


Figure 4-2. PHP Package 48-Pin HTQFP (Bottom Exposed PAD) Top View

Table 4-1. Pin Functions

PIN		I/O	DESCRIPTION
NAME	NO. PKD/PHP		
BOOTBCK	19	P	Supply input for BUCK high-side MOSFET gate drive circuit. Connect a ceramic capacitor between BOOTBCK and SWBCK pins. An internal diode is connected between VDD and BOOTBCK.
BOOTBST	33	P	Supply input for BOOST high-side MOSFET gate drive circuit. Connect a ceramic capacitor between BOOTBST and SWBST pins. An internal diode is connected between VDD and BOOTBST.
CMPBCK	25	I/O	Output of BUCK internal transconductance error amplifier. Connect an integral compensation network to maintain stability.
CMPBST	41	I/O	Output of BOOST internal transconductance error amplifier. Connect a proportional-integral compensation network to maintain stability.
CSN	24	I	Negative input (–) of internal rail-to-rail transconductance error amplifier. Connect directly to the negative node of the LED current sense resistor, R_{CS}.
CSP	23	I	Positive input (+) of internal rail-to-rail transconductance error amplifier. Connect directly to the positive node of the LED current sense resistor, R_{CS}.
EN	45	I	Hardware enable. Pull this pin low to enter shutdown.
GND	43	G	Signal and analog ground. Return for the internal voltage reference and analog circuits. Connect to circuit ground to complete return path.
GNDA	40		
HGBST	31	I/O	BOOST high side gate driver output.
ISN	37	O	Negative input (–) of BOOST current sense amplifier. Connect directly to the current sense resistor, R_{IS}.
ISP	38	I	Positive input (+) of BOOST current sense amplifier. Connect directly to the current sense resistor, R_{IS}.
LGBST	36	I/O	BOOST low side gate driver output.

Table 4-1. Pin Functions (continued)

PIN		I/O	DESCRIPTION
NAME	NO.		
	PKD/PHP		
LED1G	4	I/O	Gate driver output for external shunt FET controller. Connect to the gate of the external FET
LED2G	6	I/O	
LED3G	8	I/O	
LED4G	12	I/O	
LED5G	14	I/O	
LED6G	16	I/O	
LED3A	9	I/O	Connect to anode of the LED3 (top of the sub-string 2)
LED6A	17	I/O	Connect to anode of the LED6 (top of the sub-string 1)
LED2K	5	I/O	Connect to cathode of the LED2
LED3K	7	I/O	Connect to cathode of the LED3
LED4K	11	I/O	Connect to cathode of the LED4
LED5K	13	I/O	Connect to cathode of the LED5
LED6K	15	I/O	Connect to cathode of the LED6
MPIO0	48	I/O	Multi-purpose IO. The pin can be configured as an ADC input, digital input, or digital output. MPIO0 is used to enter CTM.
MPIO1	1	I/O	Multi-purpose IO. The pin can be configured as an ADC input, digital input, or digital output
MPIO2	2	I/O	
MPIO3	3	I/O	
NC1, NC2, NC3, NC4, NC5, NC6, NC7	10, 18, 22, 27, 30, 34, 39	NC	Do not connect. Can be connected to ground.
PGNDBCK	26	G	Ground return for BUCK low-side MOSFET
PGNDBST	35	G	Ground return for BOOST high-side gate driver
RX	47	I	UART receive data input. Connect to RX of CAN transceiver.
SWBCK	20, 21	P	Switching output of the BUCK regulator. Internally connected to both power MOSFETs. Connect to the power inductor.
SWBST	32	P	Switch node of the BOOST controller.
TX	46	O	UART transmit data output. Connect to TX of CAN transceiver.
VBCK	29	P	Power input and connections to BUCK high-side MOSFET drain node. Connect to the BOOST output voltage and bypass capacitors C_{IN}. The path from the VBCK pin to high frequency bypass C_{IN} and PGND must be as short as possible.
VBCKA	28	P	Power to internal analog block of BUCK regulator. Connect to VBCK pin and high frequency bypass capacitor.
VDD	44	P	Digital input supply voltage. Locally decouple to GND using a 2.2µF to 4.7µF ceramic capacitor located close to the device.
VDDA	42	P	Analog input supply voltage. Locally decouple to GND using a 100nF to 1µF ceramic capacitor located close to the device.

5 Device and Documentation Support

5.1 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

5.2 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

5.3 Trademarks

TI E2E™ is a trademark of Texas Instruments.
All trademarks are the property of their respective owners.

5.4 Glossary

TI Glossary	This glossary lists and explains terms, acronyms, and definitions.

6 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision * (November 2024) to Revision A (August 2025)	Page
• Added PHP package	1

7 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

7.1 Package Option Addendum

Packaging Information

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish(4)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking(5) (6)
TPS92543QPKDRQ1	ACTIVE	HTQFP	PKD	48	1000	Green (RoHS and no Sb/Br)	NIPDAU	LEVEL3-260C-168 HR	-40 to 125	TPS92543
TPS92543QPHPRQ1	ACTIVE	HTQFP	PHP	48	1000	Green (RoHS and no Sb/Br)	NIPDAU	LEVEL3-260C-168 HR	-40 to 125	TPS92543Q

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PRE_PROD Unannounced device, not in production, not available for mass market, nor on the web, samples not available.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

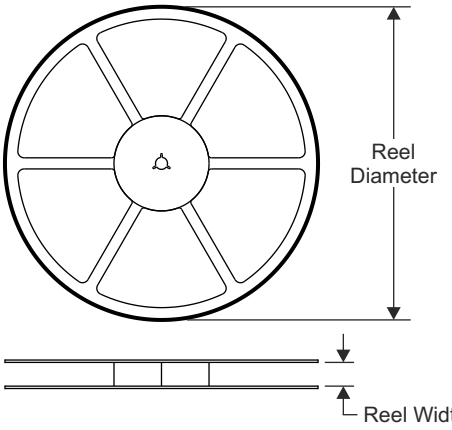
(4) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

(5) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device

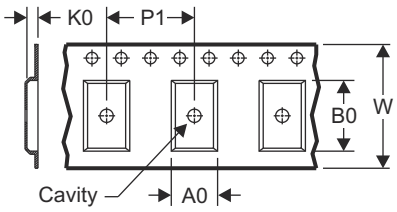
(6) Multiple Device markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

7.2 Tape and Reel Information

REEL DIMENSIONS

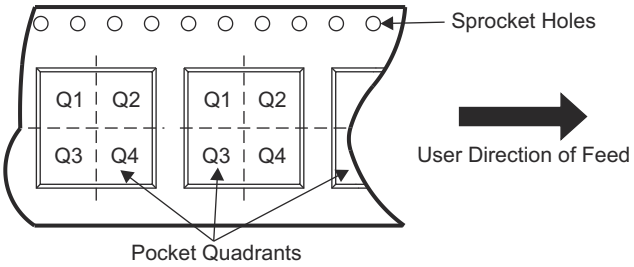


TAPE DIMENSIONS



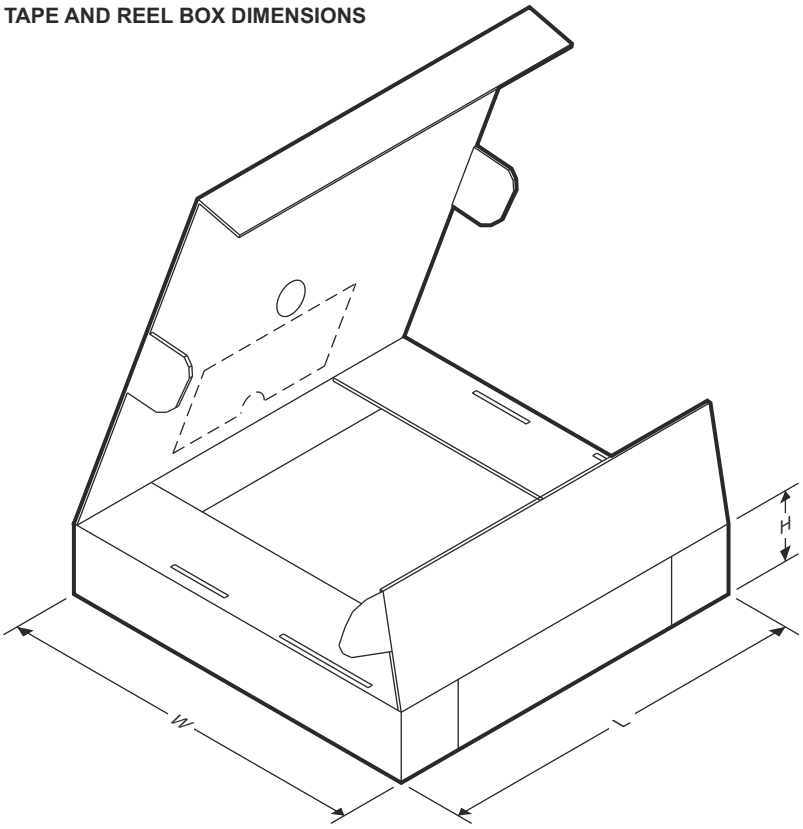
A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS92543QPKDRQ1	HTQFP	PKD	48	1000	330	16.4	9.6	9.6	1.5	12	16	Q2
TPS92543QPHPRQ1	HTQFP	PHP	48	1000	330	16.4	9.6	9.6	1.5	12	16	Q2

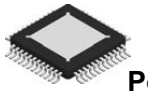
TAPE AND REEL BOX DIMENSIONS



Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS92543QPKDRQ1	HTQFP	PKD	48	1000	336.6	336.6	31.8
TPS92543QPHPRQ1	HTQFP	PHP	48	1000	336.6	336.6	31.8

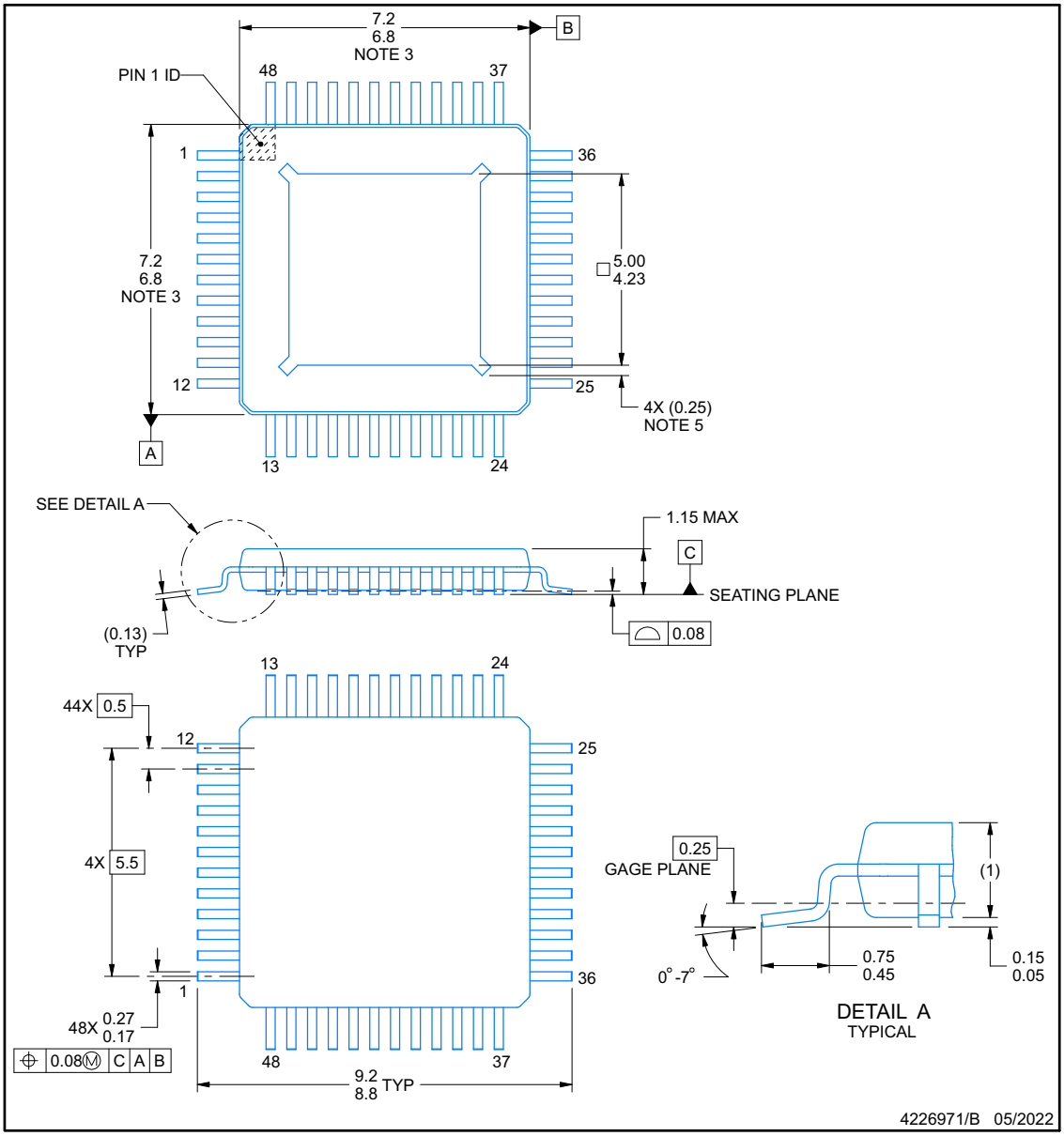
PACKAGE OUTLINE

PKD0048A



PowerPAD™ HTQFP - 1.15 mm max height

PLASTIC QUAD FLATPACK



PowerPAD is a trademark of Texas Instruments.

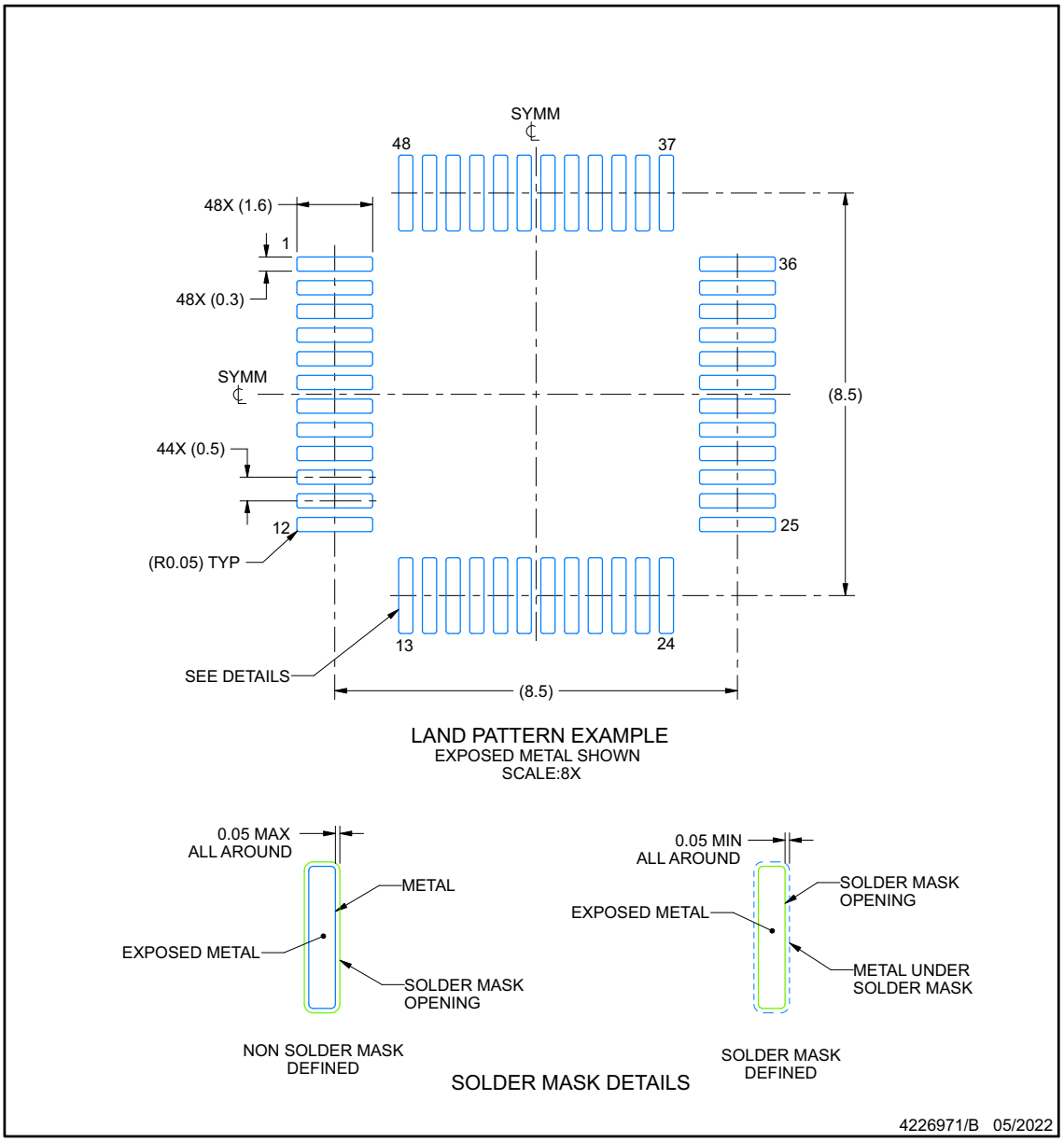
NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. Reference JEDEC registration MS-026.
5. Feature may not be present.

EXAMPLE BOARD LAYOUT

PKD0048A — **PowerPAD ™HTQFP - 1.15 mm max height**

PLASTIC QUAD FLATPACK



NOTES: (continued)

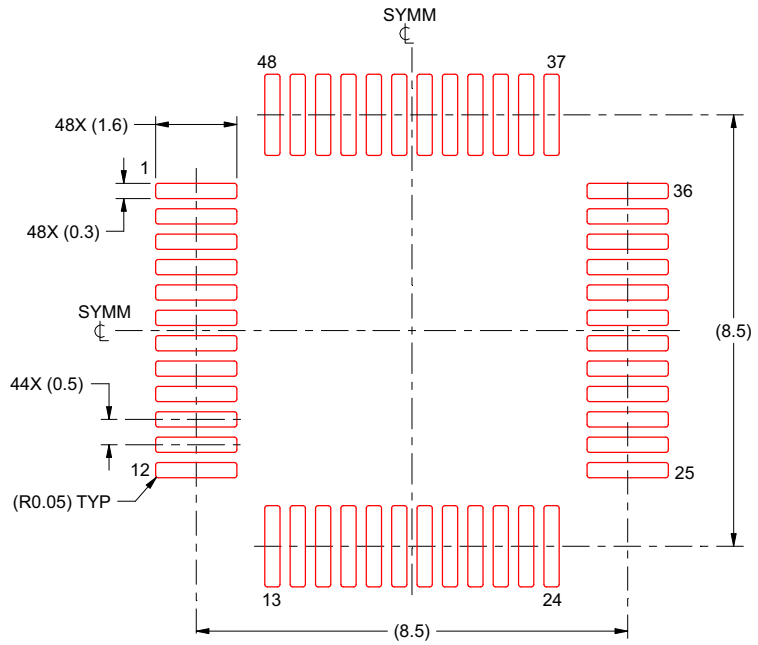
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. This package is designed to be soldered to a thermal pad on the board. See technical brief, Powerpad thermally enhanced package, Texas Instruments Literature No. SLMA002 (www.ti.com/lit/slma002) and SLMA004 (www.ti.com/lit/slma004).
9. Vias are optional depending on application, refer to device data sheet. It is recommended that vias under paste be filled, plugged or tented.
10. Size of metal pad may vary due to creepage requirement.

EXAMPLE STENCIL DESIGN

PKD0048A

PowerPAD ™HTQFP - 1.15 mm max height

PLASTIC QUAD FLATPACK



SOLDER PASTE EXAMPLE
SCALE:8X

4226971/B 05/2022

NOTES: (continued)

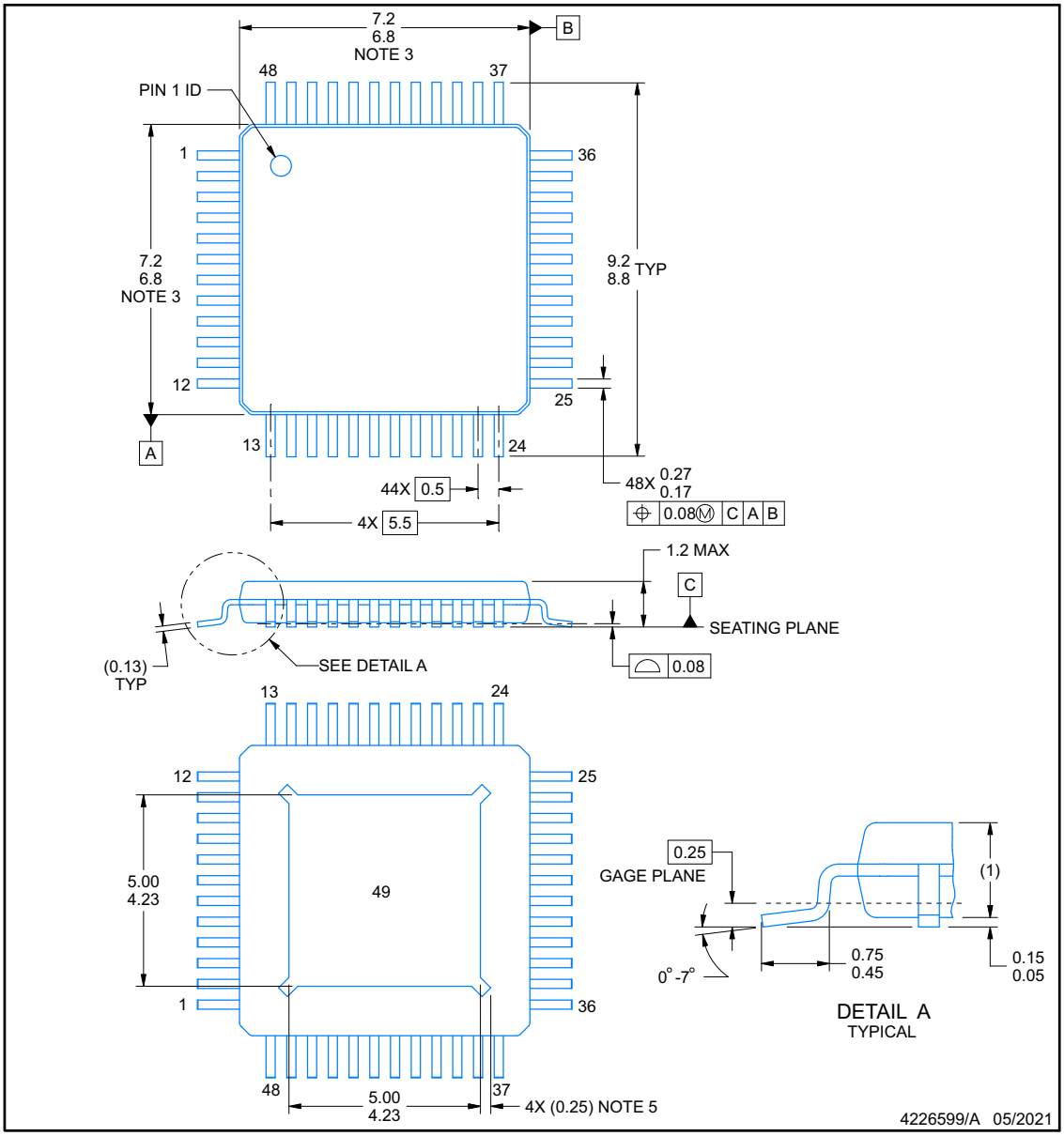
11. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
12. Board assembly site may have different recommendations for stencil design.

PACKAGE OUTLINE

PHP0048L

PowerPAD™ HTQFP - 1.2 mm max height

PLASTIC QUAD FLATPACK



PowerPAD is a trademark of Texas Instruments.

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2. This drawing is subject to change without notice.
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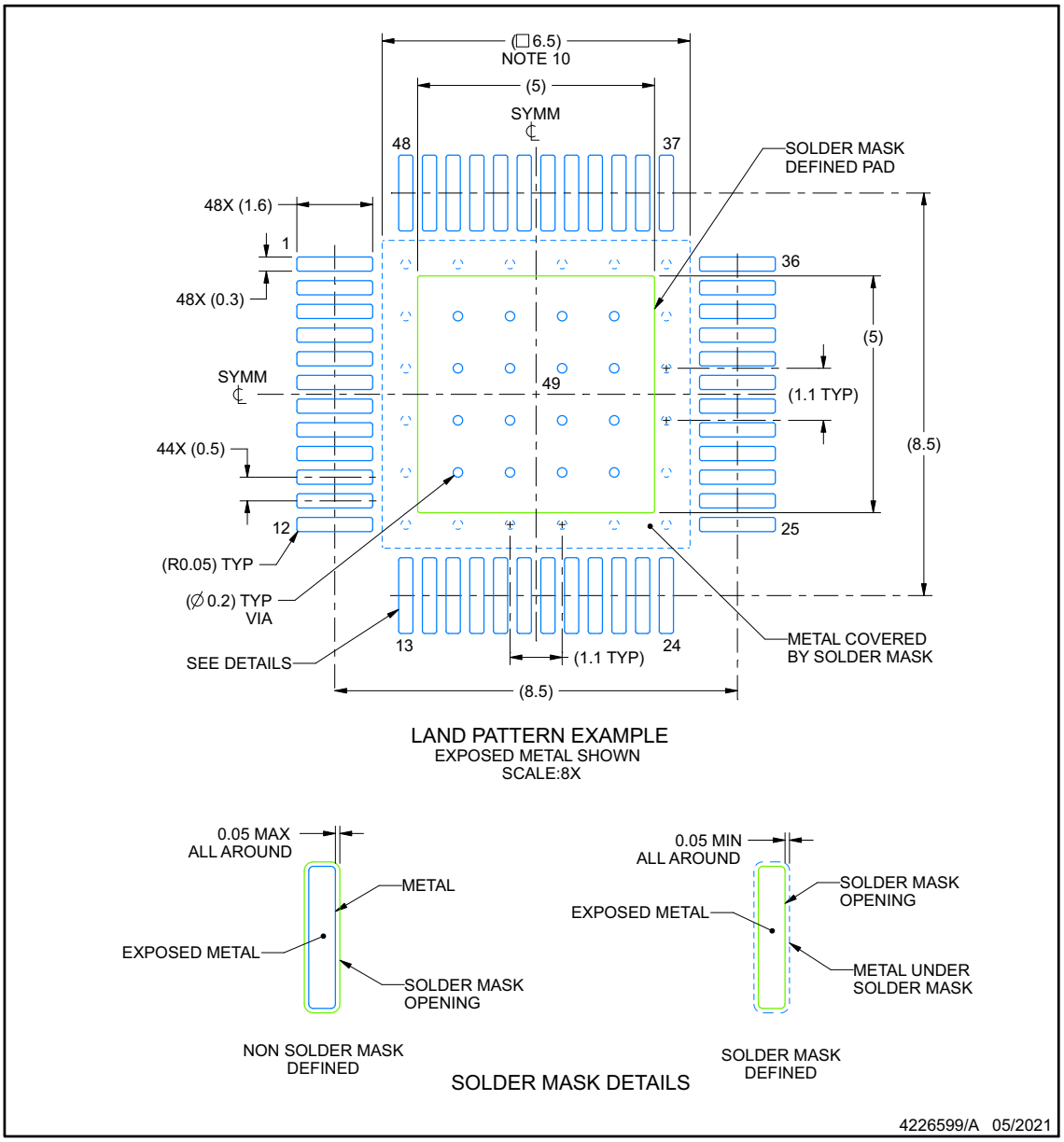
4. Reference JEDEC registration MS-026.
5. Feature may not be present.

EXAMPLE BOARD LAYOUT

PHP0048L

PowerPAD™ HTQFP - 1.2 mm max height

PLASTIC QUAD FLATPACK



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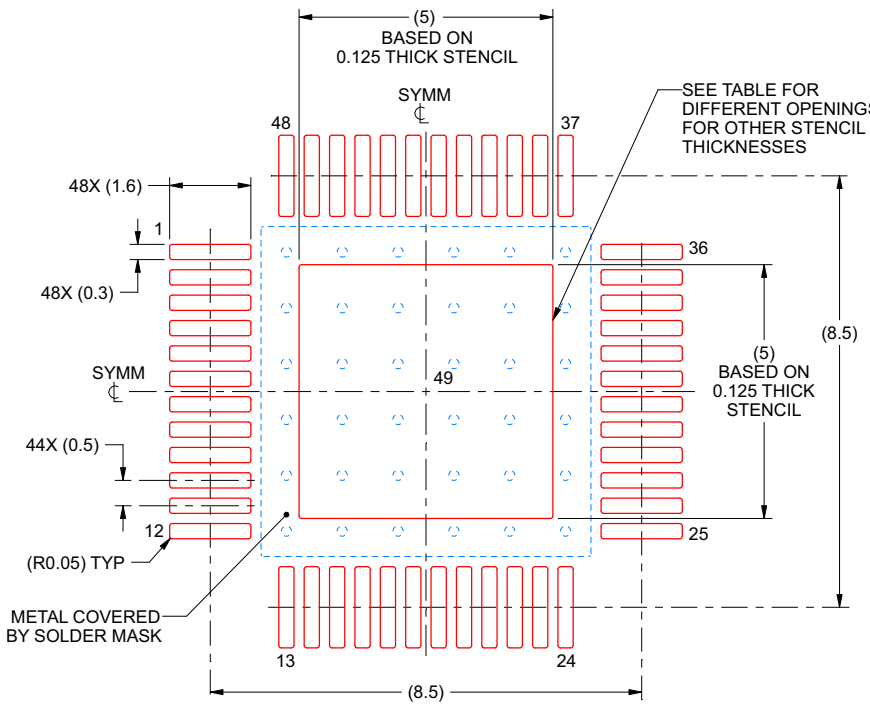
EXAMPLE STENCIL DESIGN

PHP0048L — **PowerPAD™ HTQFP - 1.2 mm max height**

PLASTIC QUAD FLATPACK



SOLDER PASTE EXAMPLE
EXPOSED PAD
100% PRINTED SOLDER COVERAGE BY AREA
SCALE:8X

STENCIL THICKNESS	SOLDER STENCIL OPENING
0.1	5.59 X 5.59
0.125	5.00 X 5.00 (SHOWN)
0.150	4.56 X 4.56
0.175	4.23 X 4.23

4226599/A 05/2021

NOTES: (continued)

11. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
12. Board assembly site may have different recommendations for stencil design.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TPS92543QPHPRQ1	Active	Production	HTQFP (PHP) | 48	1000 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 125	TPS92543Q
TPS92543QPKDRQ1	Active	Production	HTQFP (PKD) | 48	1000 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 125	TPS92543
TPS92543QPKDRQ1.A	Active	Production	HTQFP (PKD) | 48	1000 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 125	TPS92543

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

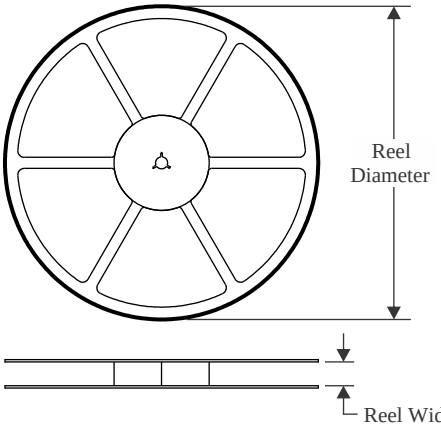
(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

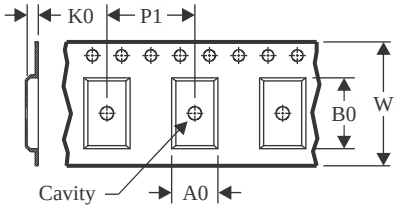
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

TAPE AND REEL INFORMATION

REEL DIMENSIONS



TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
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W	Overall width of the carrier tape
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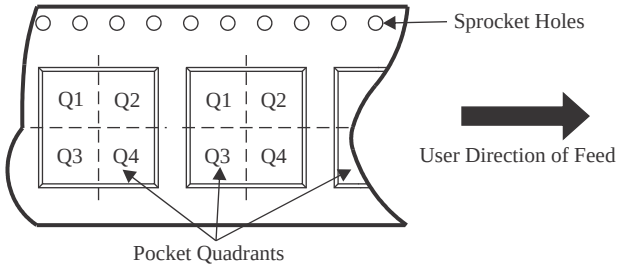
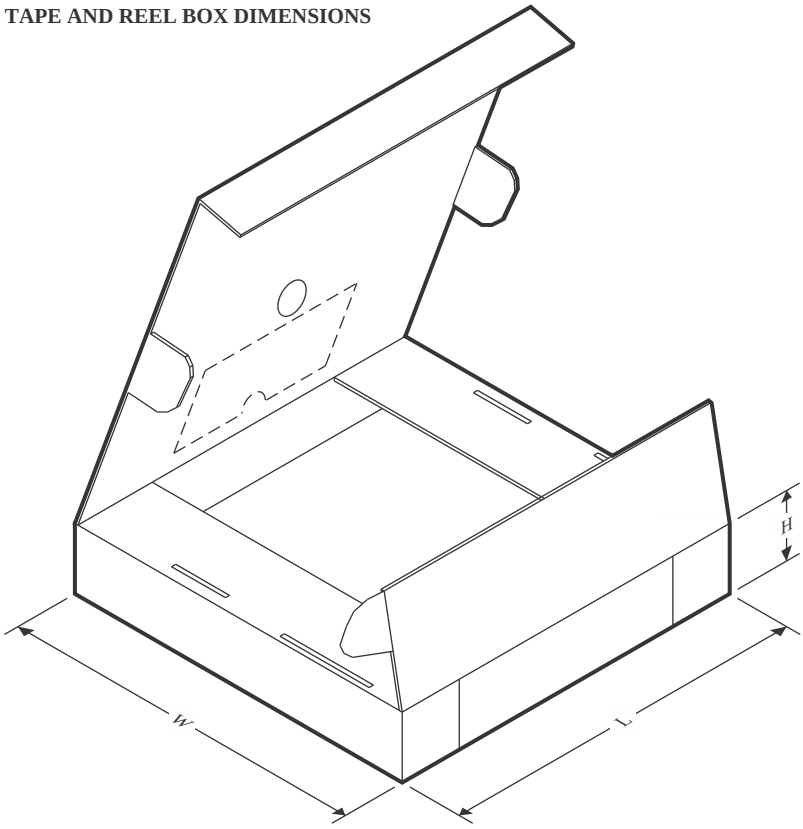
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS92543QPHPRQ1	HTQFP	PHP	48	1000	330.0	16.4	9.6	9.6	1.5	12.0	16.0	Q2
TPS92543QPKDRQ1	HTQFP	PKD	48	1000	330.0	16.4	9.6	9.6	1.5	12.0	16.0	Q2

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS92543QPHPRQ1	HTQFP	PHP	48	1000	336.6	336.6	31.8
TPS92543QPKDRQ1	HTQFP	PKD	48	1000	336.6	336.6	31.8

GENERIC PACKAGE VIEW

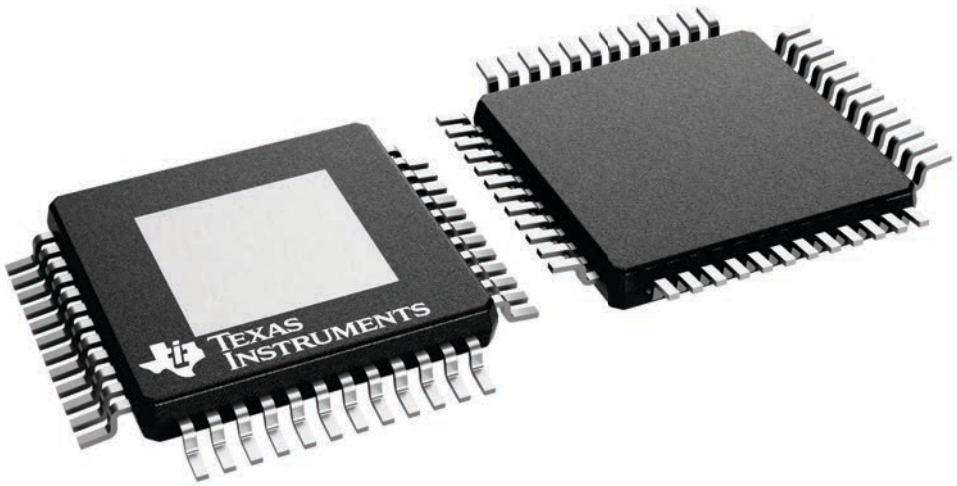
PKD 48

PowerPAD™ HTQFP - 1.15 mm max height

7 x 7, 0.5 mm pitch

PLASTIC QUAD FLATPACK

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



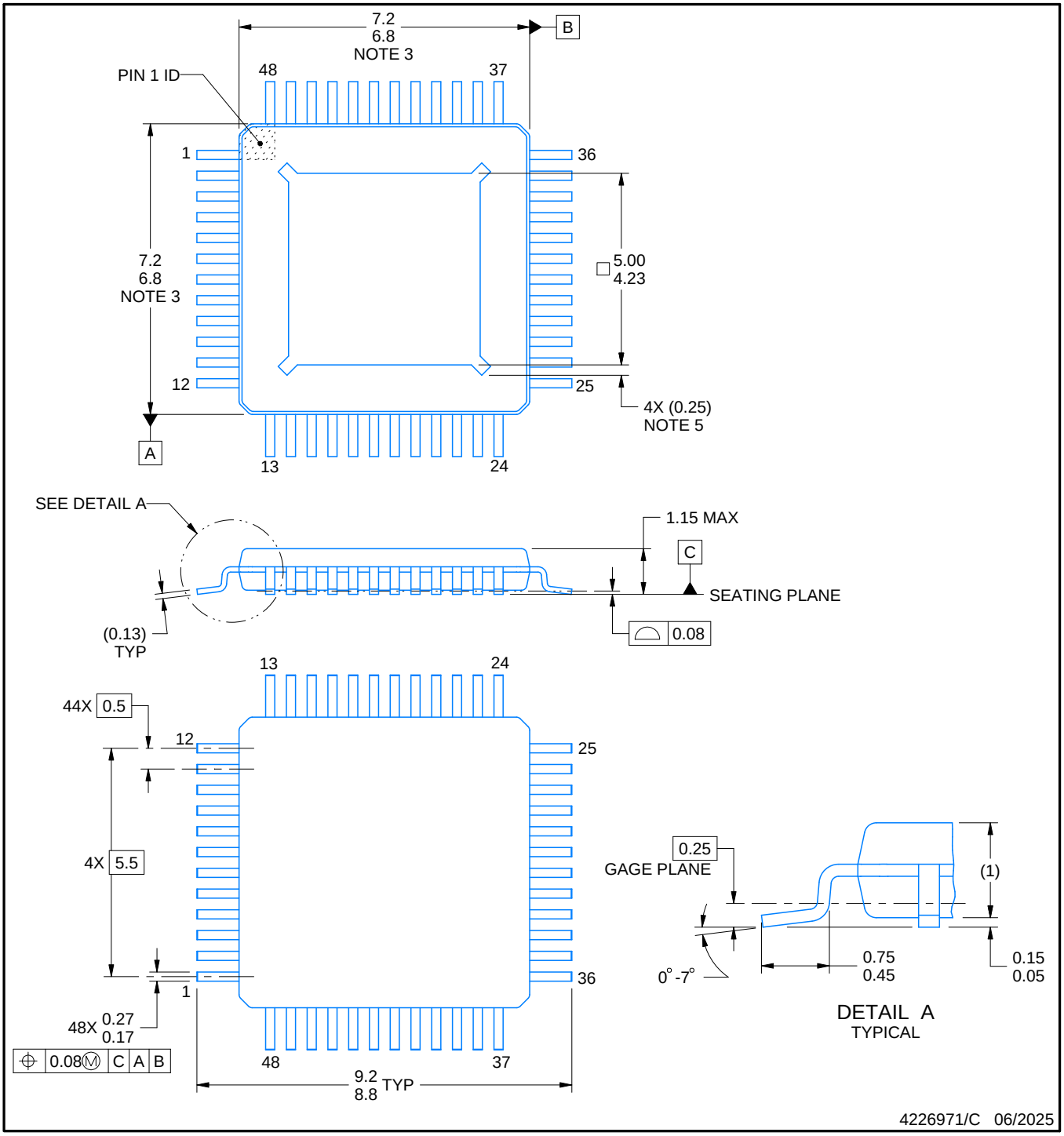
4231748/A

PACKAGE OUTLINE

PKD0048A

PowerPAD ™HTQFP - 1.15 mm max height

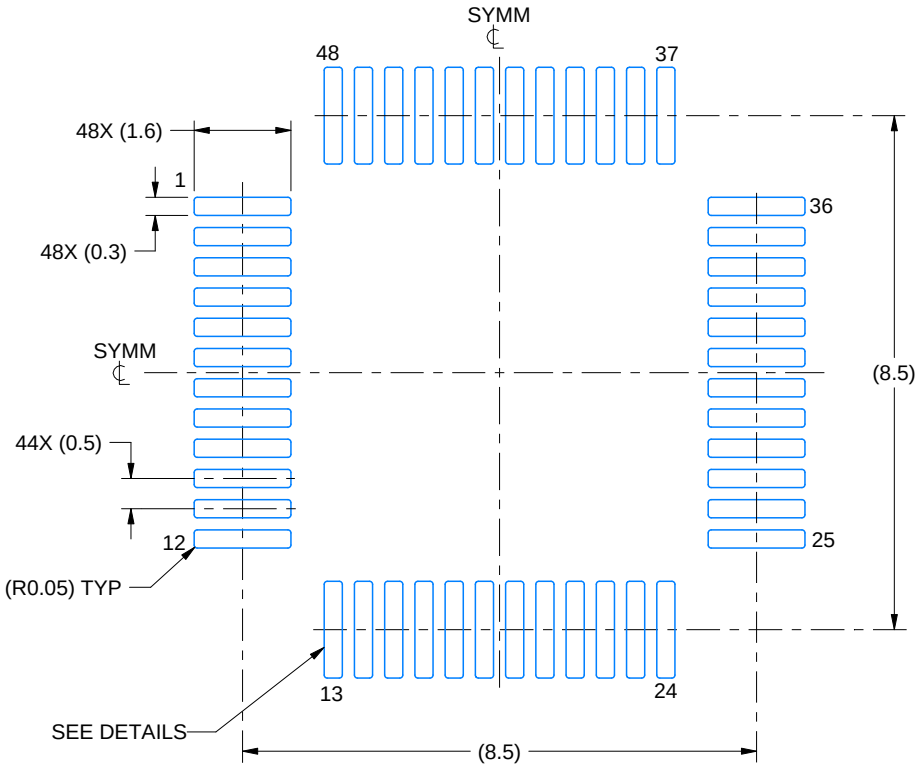
PLASTIC QUAD FLATPACK



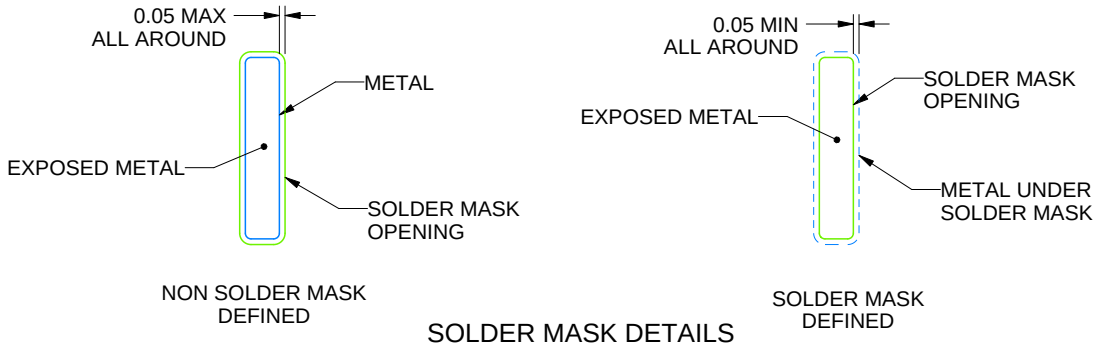
PowerPAD is a trademark of Texas Instruments.

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. Reference JEDEC registration MS-026.
5. Feature may not be present.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X

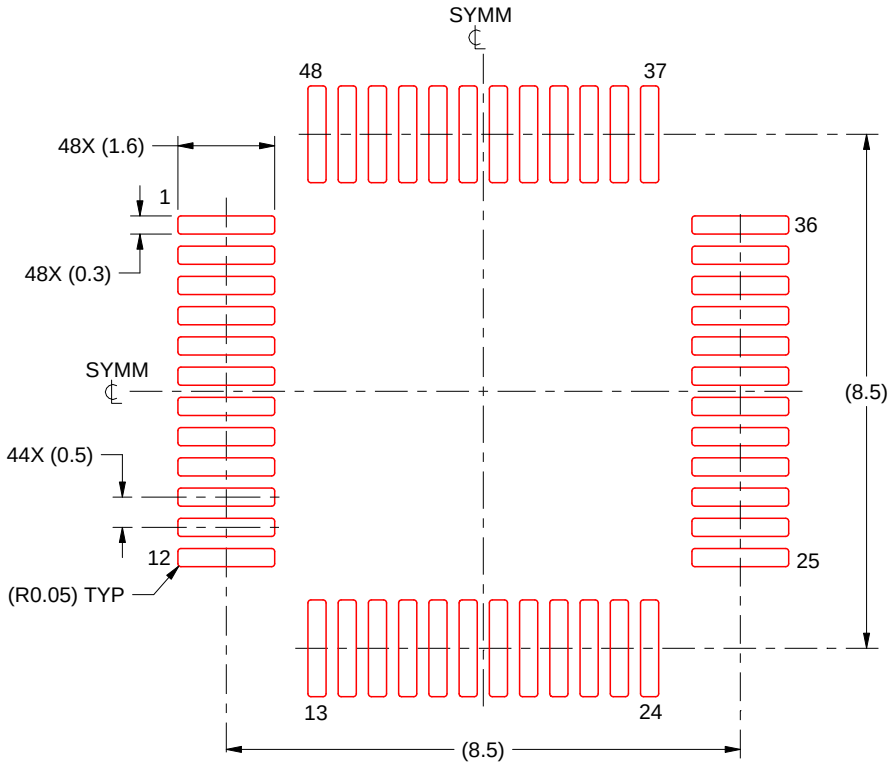


SOLDER MASK DETAILS

4226971/C 06/2025

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. This package is designed to be soldered to a thermal pad on the board. See technical brief, Powerpad thermally enhanced package, Texas Instruments Literature No. SLMA002 (www.ti.com/lit/slma002) and SLMA004 (www.ti.com/lit/slma004).
9. Vias are optional depending on application, refer to device data sheet. It is recommended that vias under paste be filled, plugged or tented.
10. Size of metal pad may vary due to creepage requirement.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:8X

4226971/C 06/2025

NOTES: (continued)

11. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
12. Board assembly site may have different recommendations for stencil design.

GENERIC PACKAGE VIEW

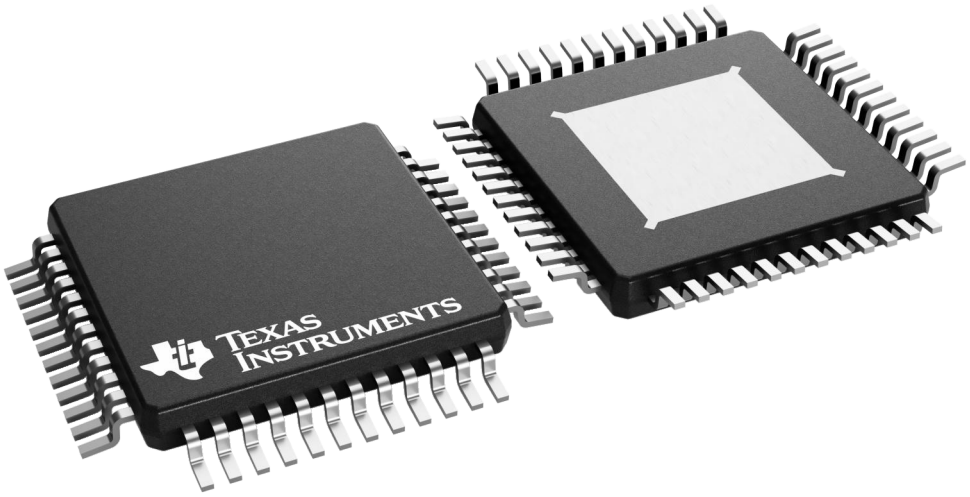
PHP 48

TQFP - 1.2 mm max height

7 x 7, 0.5 mm pitch

QUAD FLATPACK

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



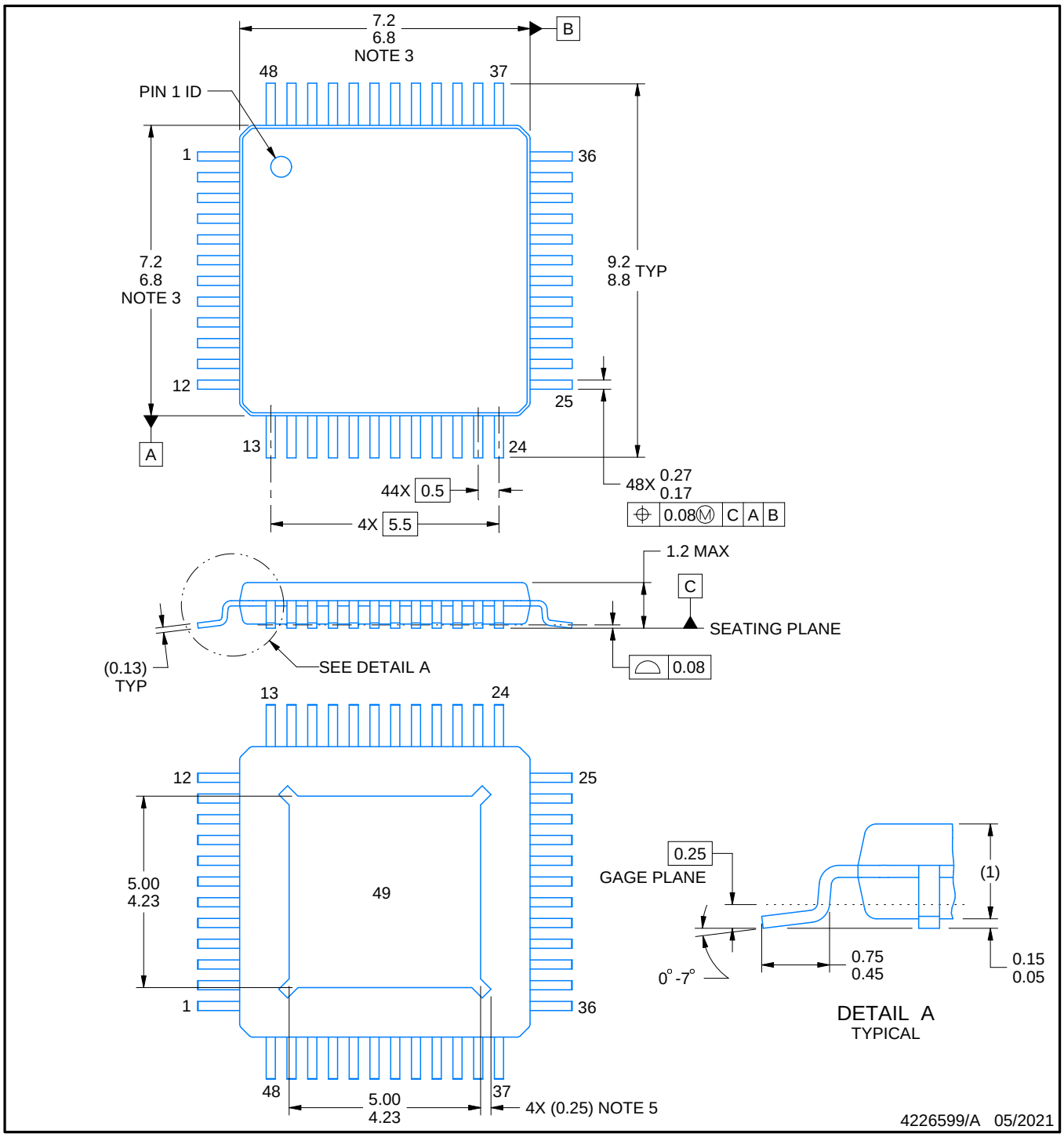
4226443/A

PACKAGE OUTLINE

PHP0048L

PowerPAD™ HTQFP - 1.2 mm max height

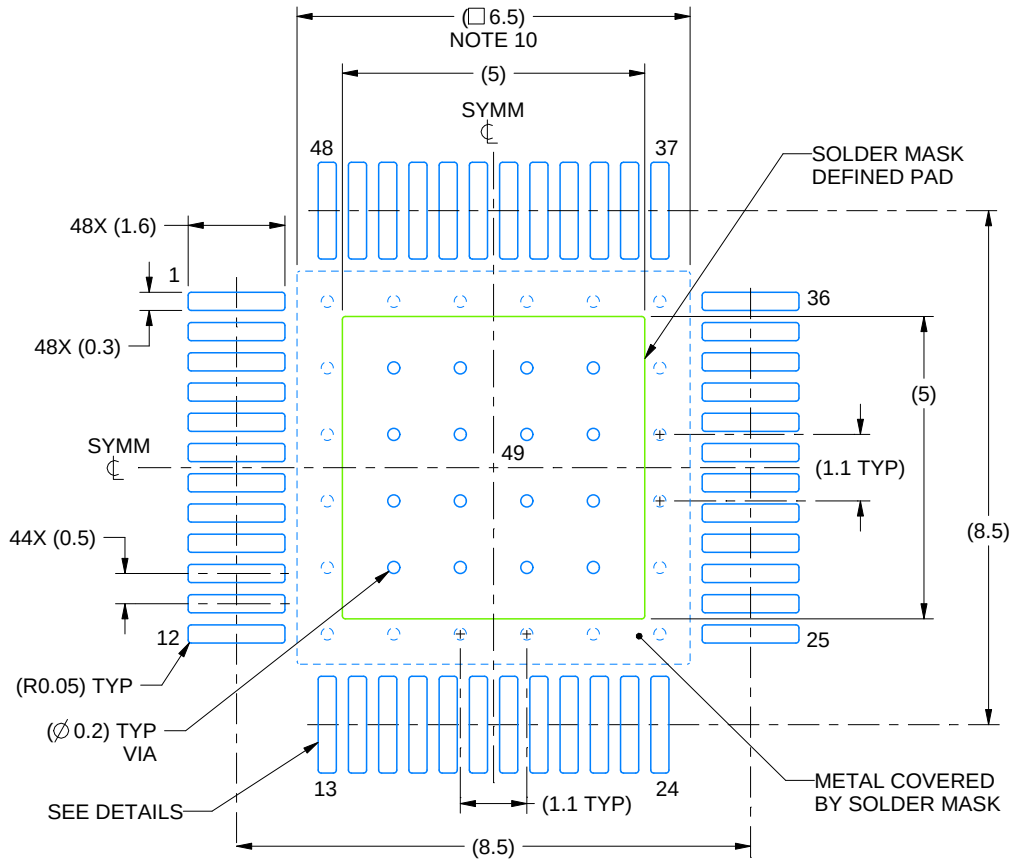
PLASTIC QUAD FLATPACK



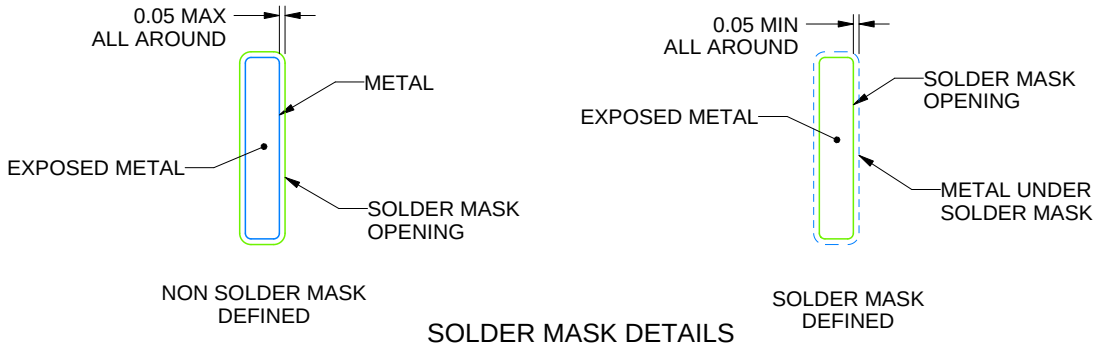
PowerPAD is a trademark of Texas Instruments.

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. Reference JEDEC registration MS-026.
5. Feature may not be present.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X



SOLDER MASK DETAILS

4226599/A 05/2021

NOTES: (continued)

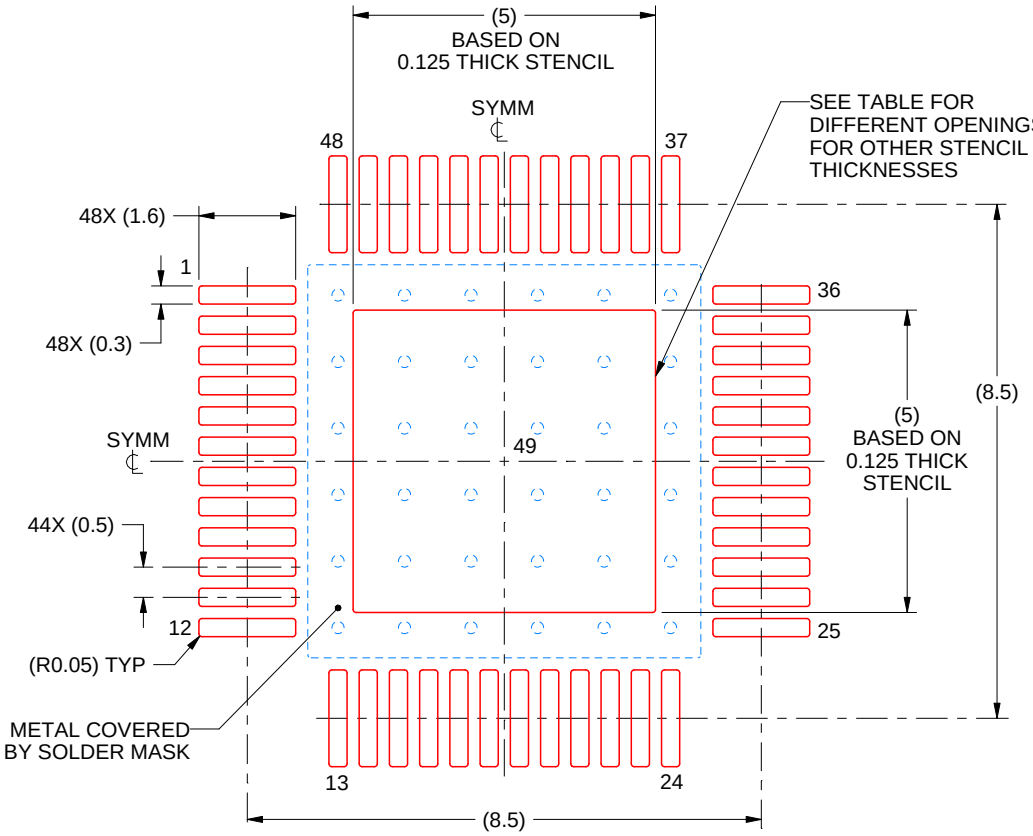
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. This package is designed to be soldered to a thermal pad on the board. See technical brief, Powerpad thermally enhanced package, Texas Instruments Literature No. SLMA002 (www.ti.com/lit/slma002) and SLMA004 (www.ti.com/lit/slma004).
9. Vias are optional depending on application, refer to device data sheet. It is recommended that vias under paste be filled, plugged or tented.
10. Size of metal pad may vary due to creepage requirement.

EXAMPLE STENCIL DESIGN

PHP0048L

PowerPAD™ HTQFP - 1.2 mm max height

PLASTIC QUAD FLATPACK



SOLDER PASTE EXAMPLE
EXPOSED PAD
100% PRINTED SOLDER COVERAGE BY AREA
SCALE:8X

STENCIL THICKNESS	SOLDER STENCIL OPENING
0.1	5.59 X 5.59
0.125	5.00 X 5.00 (SHOWN)
0.150	4.56 X 4.56
0.175	4.23 X 4.23

4226599/A 05/2021

NOTES: (continued)

11. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
12. Board assembly site may have different recommendations for stencil design.

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Last updated 10/2025