TRF1218 Near-DC to 25GHz Single-Ended to Differential RF Amplifier

1 Features

- Fixed 16dB gain
- 3dB bandwidth: 25GHz
- Gain flatness:
  - +1.2dB (20GHz)
  - –1dB (23GHz)
- Imbalance (10MHz to 20GHz):
  - Gain: ±0.2dB
  - Phase: +3º
- HD2 (8GHz, P_O = 3dBm): –62dBc
- HD3 (6GHz, P_O = 3dBm): –50dBc
- OIP2: 67dBm (2GHz), 62dBm (8GHz)
- OIP3: 31dBm (4GHz), 22.8dBm (16GHz)
- OP1dB: 12.6dBm (4GHz), 13.1dBm (16GHz)
- NF: 10dB (4GHz), 13.2dB (16GHz)
- 50Ω single-ended input impedance
- 50Ω differential output impedance
- Power-down feature
- 5V single-supply operation
- Active current: 190mA

2 Applications

- RF sampling or GSPS ADC driver
- Aerospace and defense
- Electronic Warfare
- Radar seeker front end
- Phased array radar
- Software Defined Radios
- Test and measurement
- High-speed digitizers
- Vector signal transceiver (VST)
- Wireless Communications Test

3 Description

The TRF1218 is a very high performance, single-ended to differential radio frequency (RF) amplifier optimized for wide signal bandwidth applications. The device is excellent for ac-coupled uses that require a single-ended to differential conversion such as driving an RF sampling analog-to-digital converter (ADC). The device combines the functionality of a wide-band gain block and wide-band passive balun in a single 2mm × 2mm package. The on-chip matching components simplify printed circuit board (PCB) implementation and enables high performance over the full operating bandwidth. The device is fabricated in Texas Instruments' advanced complementary BiCMOS process and is available in a space-saving WQFN-FCRLF package.

The TRF1218 operates on a single-rail supply and consumes about 190mA of active current. A power-down feature via a single pin is also available for simplified power savings.

Package Information

PART NUMBER	PACKAGE(1)	PACKAGE SIZE(2)
TRF1218	RPV (WQFN-FCRLF, 12)	2mm × 2mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.
(2) The package size (length × width) is a nominal value and includes pins, where applicable.

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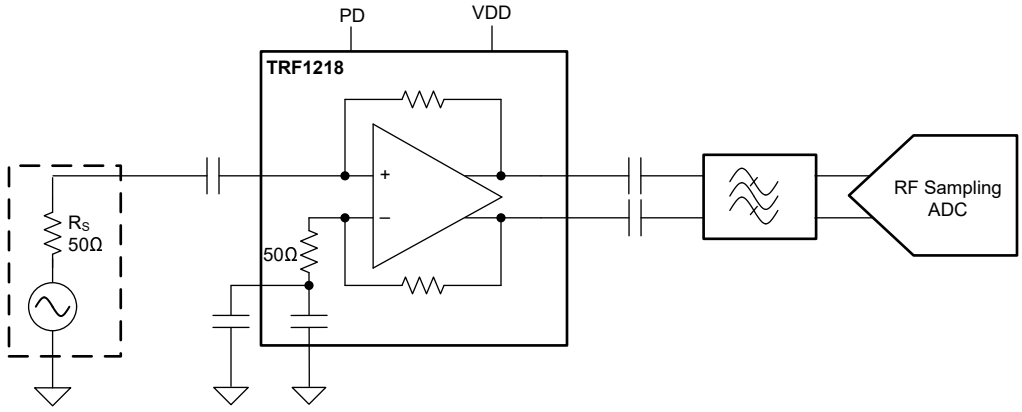

TRF1218 Driving an RF Sampling ADC

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4 Pin Configuration and Functions

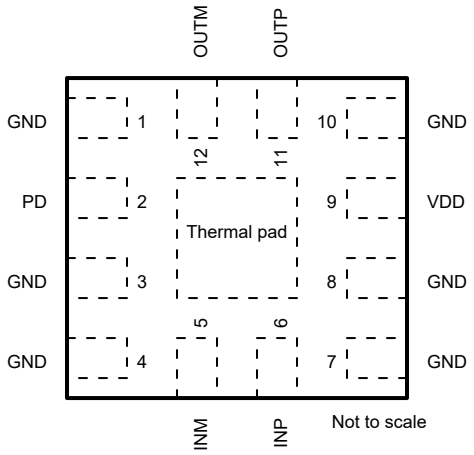

**Figure 4-1. RPV Package,
12-Pin WQFN-FCRLF
(Top View)**

Table 4-1. Pin Functions

PIN		TYPE	DESCRIPTION
NAME	NO.		
GND	1, 3, 4, 7, 8, 10	Ground	Ground
INM	5	Input	External ac coupling capacitor on negative input. Typical value 100nF.
INP	6	Input	Single ended input
OUTM	12	Output	Differential signal output, negative
OUTP	11	Output	Differential signal output, positive
PD	2	Input	Power-down signal. Supports 1.8V and 3.3V Logic. 0 = Chip enabled 1 = Power down
VDD	9	Power	5V supply
Thermal pad	Pad	—	Thermal pad. Connect to ground on board.

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5 Specifications

5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
V_{DD}	Supply voltage	–0.3	5.5	V
P_{INP}	INP input pin power		TBD	dBm
V_{INM}	INM input pin voltage	–0.3	3.3(2)	V
V_{PD}	Power-down pin voltage	–0.3	3.45(2)	V
T_J	Junction temperature		150	ºC
T_{stg}	Storage temperature	–40	150	ºC

(1) Operation outside the *Absolute Maximum Ratings* may cause permanent device damage. *Absolute Maximum Ratings* do not imply functional operation of the device at these or any other conditions beyond those listed under *Recommended Operating Conditions*. If used outside the *Recommended Operating Conditions* but within the *Absolute Maximum Ratings*, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.
(2) When V_{DD} = 0V, maximum value is 0.3V.

5.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins(1)	±1000	V
		Charged device model (CDM), per ANSI/ESDA/JEDEC JS-002, all pins(2)	±250	

(1) JEDEC document JEP155 states that 500V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250V CDM allows safe manufacturing with a standard ESD control process.

5.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
V_{DD}	Supply voltage	4.75	5	5.25	V
T_A	Ambient free-air temperature	–40	25		°C
T_J	Junction temperature			125	°C

5.4 Thermal Information

THERMAL METRIC(1)		TRF1218 RPV (WQFN-FCRLF) 12 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	66.7	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	35.3	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	31.1	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	0.6	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	31.1	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	10.7	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

5.5 Electrical Characteristics

at T_A = 25°C, V_{DD} = 5V, 50Ω single-ended input, and 50Ω differential output (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
AC PERFORMANCE							
SSBW	Small-signal 3dB bandwidth	V_O = 0.1V_{PP}			25		GHz
LSBW	Large-signal 3dB bandwidth	V_O = 1V_{PP}			25		GHz
1dB BW	1dB bandwidth	V_O = 1V_{PP}			23.5		GHz
Sds21	Power gain	f = 0.5GHz			16.3		dB
		f = 2GHz			16.1		
		f = 4GHz			16		
		f = 8GHz			15.9		
		f = 10GHz			15.7		
		f = 12GHz			15.6		
		f = 14GHz			15.9		
		f = 16GHz			16.6		
		f = 18GHz			17.3		
		f = 20GHz			17.5		
Sss11	Single-ended input return loss	f = 10MHz to 20GHz			–15		dB
Sdd22	Differential output return loss	f = 10MHz to 20GHz			–10		dB
Ssd12	Reverse isolation	f = 10MHz to 20GHz			-45		dB
Imb_{GAIN}	Gain imbalance	f = 10MHz to 20GHz			0.2		dB
Imb_{PHASE}	Phase imbalance	f = 10MHz to 20GHz			3		°
CMRR	Common-mode rejection ratio[1]	f = 10MHz to 12GHz			–35		dB
		f = 12GHz to 20GHz			–30		
HD2	Second-order harmonic distortion	P_O = 3dBm	f = 0.5GHz		–68.5		dBc
			f = 2GHz		–70		
			f = 6GHz		–53.5		
			f = 8GHz		–62		
HD3	Third-order harmonic distortion	P_O = 3dBm	f = 0.5GHz		–68.3		dBc
			f = 2GHz		–60.3		
			f = 4GHz		–56		
			f = 6GHz		–50		
OIP2	Output second-order intercept point	P_O = 0dBm per tone, 10MHz spacing	f = 0.5GHz		64.5		dBm
			f = 2GHz		64.8		
			f = 6GHz		49.9		
			f = 8GHz		60.4		
		P_O = –4dBm per tone, 10MHz spacing	f = 0.5GHz		66		
			f = 2GHz		67		
			f = 6GHz		52		
			f = 8GHz		62		
IMD2	Second-order intermodulation distortion	P_O = –4dBm per tone, 10MHz spacing	f = 0.5GHz		–70		dBc
			f = 2GHz		–71		
			f = 6GHz		–56		
			f = 8GHz		–66		

ADVANCE INFORMATION

5.5 Electrical Characteristics (continued)

at T_A = 25°C, V_{DD} = 5V, 50Ω single-ended input, and 50Ω differential output (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
OIP3	Output third-order intercept point	P_O = 0dBm per tone, 10MHz spacing	f = 0.5GHz		36		dBm
			f = 2GHz		32.4		
			f = 4GHz		30.9		
			f = 8GHz		28.7		
			f = 10GHz		27.3		
			f = 12GHz		25.5		
			f = 14GHz		23.9		
			f = 16GHz		22		
			f = 18GHz		21		
		P_O = –4dBm per tone, 10MHz spacing	f = 0.5GHz		34.5		
			f = 2GHz		32		
			f = 4GHz		31		
			f = 8GHz		29		
			f = 10GHz		27.8		
			f = 12GHz		26.4		
			f = 14GHz		24.5		
			f = 16GHz		22.8		
			f = 18GHz		22		
IMD3	Third-order intermodulation distortion	P_O = –4dBm per tone, 10MHz spacing	f = 0.5GHz		–77		dBc
			f = 2GHz		–72		
			f = 4GHz		–70		
			f = 8GHz		–66		
			f = 10GHz		–64		
			f = 12GHz		–61		
			f = 14GHz		–57		
			f = 16GHz		–54		
			f = 18GHz		–52		
OP1dB	Output 1dB compression point	f = 0.5GHz			11.8		dBm
		f = 2GHz			11.8		
		f = 4GHz			12.6		
		f = 8GHz			13.1		
		f = 10GHz			12.6		
		f = 12GHz			12.9		
		f = 14GHz			13.4		
		f = 16GHz			13.1		
		f = 18GHz			13.8		

ADVANCE INFORMATION

5.5 Electrical Characteristics (continued)

at T_A = 25°C, V_{DD} = 5V, 50Ω single-ended input, and 50Ω differential output (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
NF	Noise Figure	f = 0.5GHz		9.3		dB
		f = 2GHz		9.3		
		f = 4GHz		10		
		f = 8GHz		11		
		f = 10GHz		12		
		f = 12GHz		12.5		
		f = 14GHz		12.8		
		f = 16GHz		13.2		
		f = 18GHz		13.5		
IMPEDANCE						
Z_{O-DIFF}	Differential output impedance	f = dc (internal to the device)		26.5		Ω
R_{INM}	Internal INM resistance	Internal INM resistance		50		Ω
C_{INM}	Internal INM capacitance	Internal INM capacitance		12.5		pF
TRANSIENT						
t_{REC}	Overdrive recovery time	Using a –0.5V_P input pulse of 2ns duration		TBD		ns
POWER SUPPLY						
I_{QA}	Active current	Current on V_{DD} pin, PD = 0		190		mA
I_{QPD}	Power-down quiescent current	Current on V_{DD} pin, PD = 1		20		mA
ENABLE						
V_{PDHIGH}	PD pin logic high		1.45			V
V_{PDLOW}	PD pin logic low				0.8	V
I_{PDBIAS}	PD bias current (current on PD pin)	PD = high (1.8V logic)		40	100	µA
		PD = high (3.3V logic)		200	250	
C_{PD}	PD pin capacitance			2		pF
t_{ON}	Turn-on time	50% V_{PD} to 90% RF		TBD		ns
t_{OFF}	Turn-off time	50% V_{PD} to 10% RF		TBD		ns

(1) Calculated using the formula (S21 – S31) / (S21 + S31). Port-1: INP, Port-2: OUTP, Port-3: OUTM.

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6 Device and Documentation Support

6.1 Device Support

6.1.1 Third-Party Products Disclaimer

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6.2 Documentation Support

6.2.1 Related Documentation

For related documentation, see the following:

- Texas Instruments, *TRF1218EVM* user's guide

6.3 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

6.4 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

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6.5 Trademarks

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6.6 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

6.7 Glossary

TI Glossary	This glossary lists and explains terms, acronyms, and definitions.

7 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

DATE	REVISION	NOTES
June 2026	*	Initial Advance Information Release

8 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

8.1 Package Option Addendum

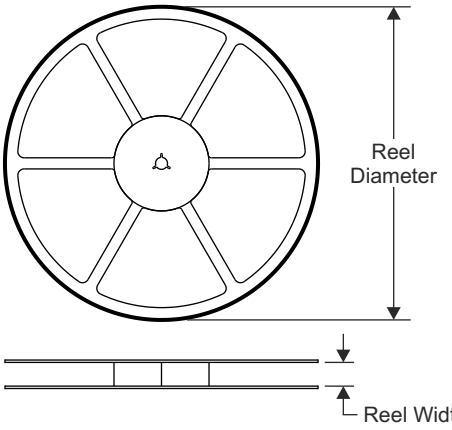
Packaging Information

Orderable part number	Status(1)	Material type(2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/Ball material(4)	MSL rating/Peak reflow(5)	Op temp (°C)	Part marking(6)
PTRF1218RPVR	Preview	Preproduction	WQFN-HR (RPV) | 12	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 105	1218

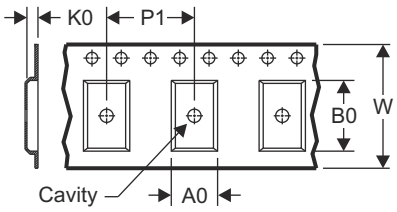
(1) **Status:** For more details on status, see our product life cycle.
(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.
(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.
(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.
(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.
(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

8.2 Tape and Reel Information

REEL DIMENSIONS

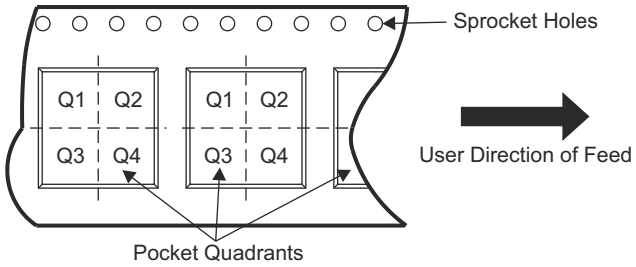


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
PTRF1218RPVR	WQFN-HR	RPV	12	3000	180.0	8.4	2.3	2.3	1.15	4.0	8.0	Q2

ADVANCE INFORMATION

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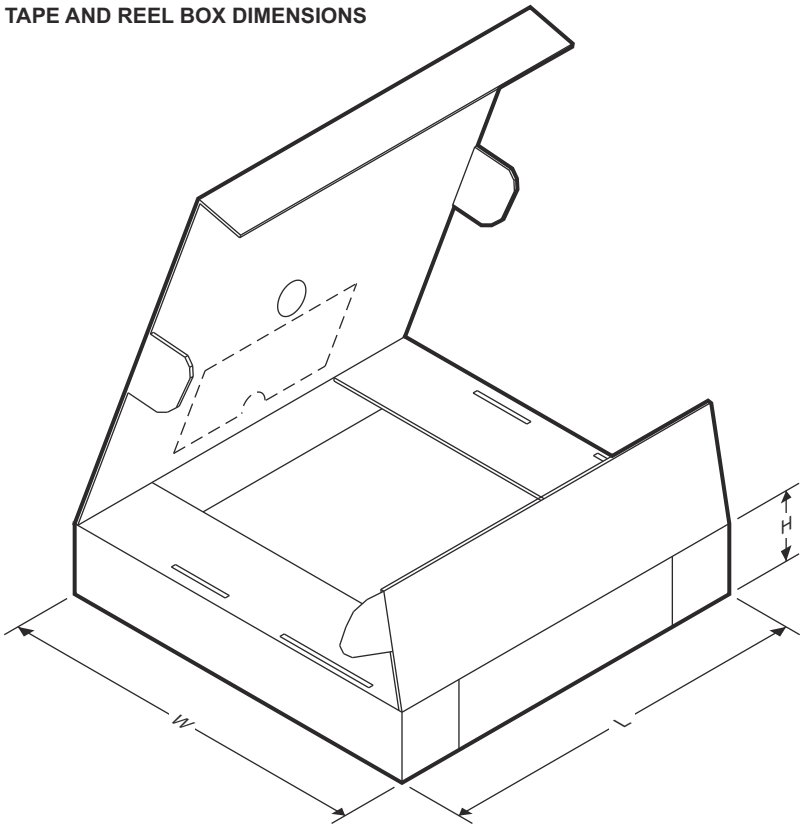
TAPE AND REEL BOX DIMENSIONS



Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
PTRF1218RPVR	WQFN-HR	RPV	12	3000	210.0	185.0	35.0

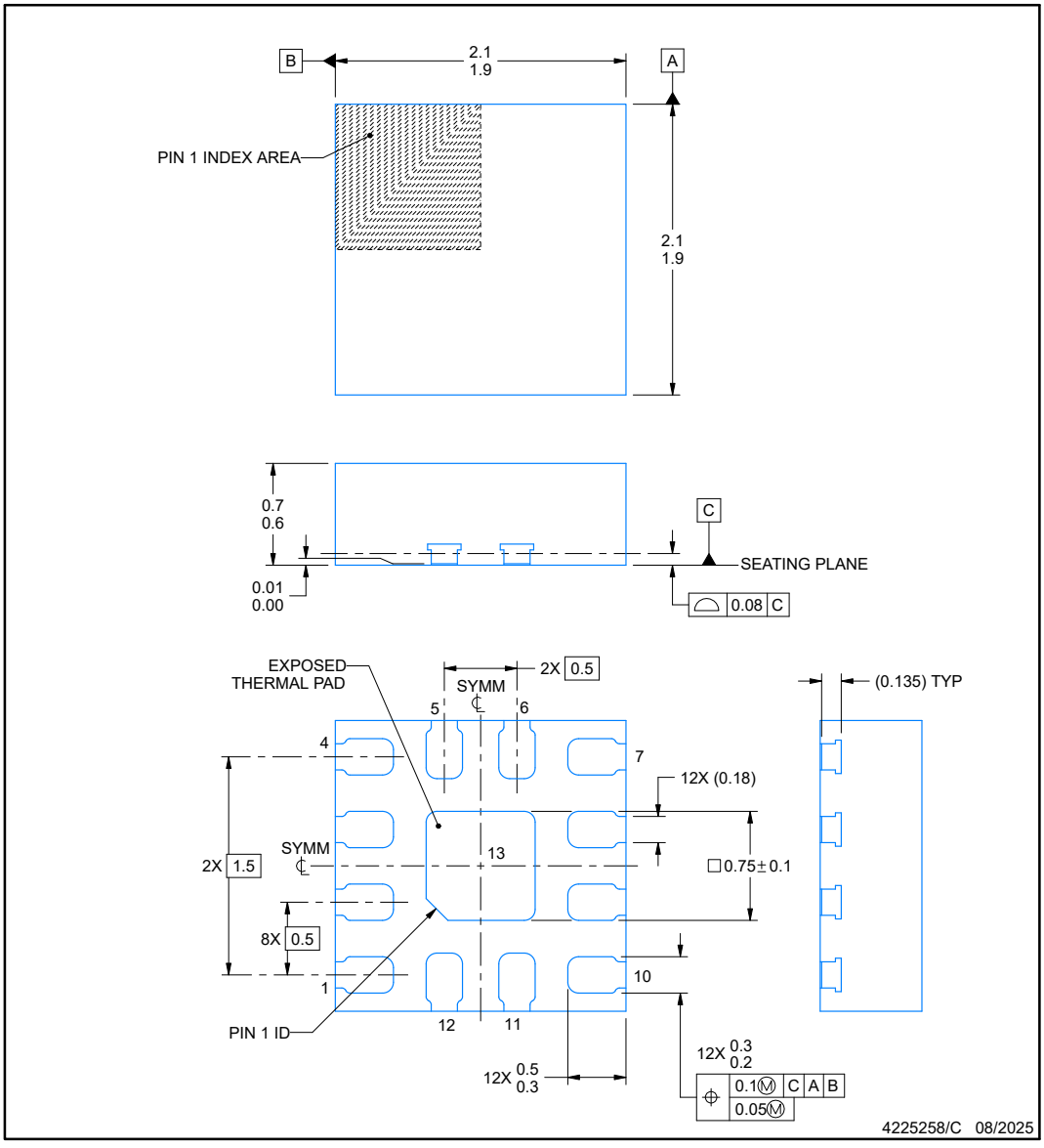
8.3 Mechanical Data

RPV0012A

PACKAGE OUTLINE

WQFN-FCRLF - 0.7 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



NOTES:

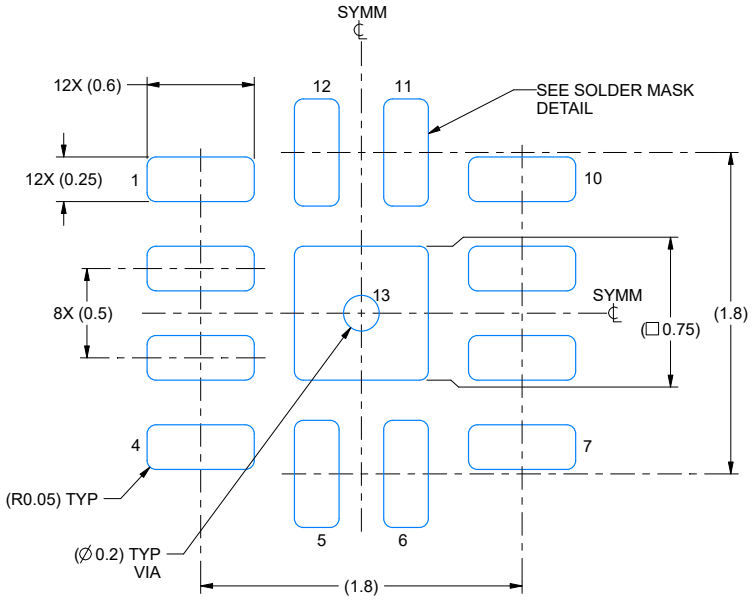
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.

ADVANCE INFORMATION

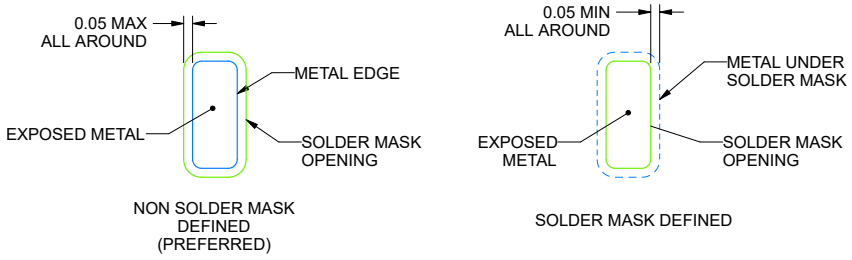
EXAMPLE BOARD LAYOUT

RPV0012A — **WQFN-FCRLF - 0.7 mm max height**

PLASTIC QUAD FLATPACK - NO LEAD



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 30X



SOLDER MASK DETAILS

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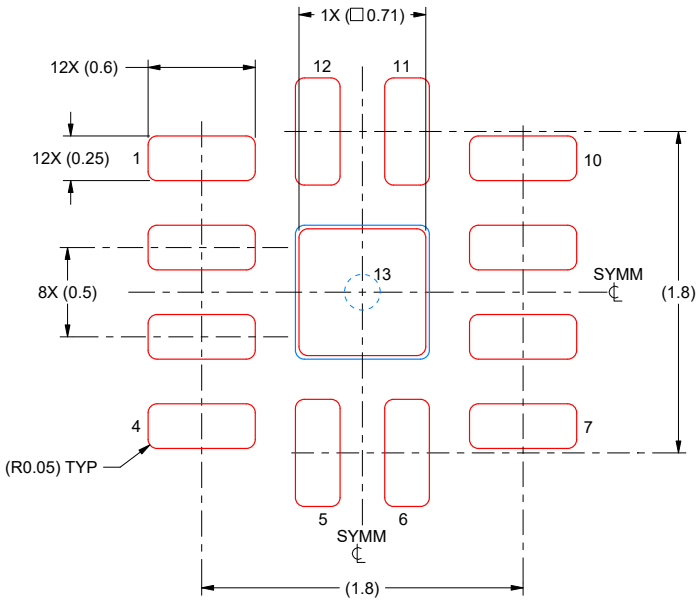
NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.

EXAMPLE STENCIL DESIGN

RPV0012A — **WQFN-FCRLF - 0.7 mm max height**

PLASTIC QUAD FLATPACK - NO LEAD



SOLDER PASTE EXAMPLE
BASED ON 0.125 MM THICK STENCIL
SCALE: 30X

EXPOSED PAD 13
90% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE

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NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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