TRF2001P 820-1054MHz ISM Band Multiprotocol and Wi-SUN RF FEM

1 Features

- 820MHz to 1054MHz RF front end module
- Transmit (TX):
  - Saturated output power (P_{SAT}): 27.5dBm (3.3V)
  - PA gain: 24dB
  - PAE: 42.2% at 27dBm
  - HD2 / HD3: –56dBc / –70dBc
- Receive (RX) LNA:
  - Gain: 16dB
  - Noise figure (NF): 1.3dB
  - IP1dB: –6.7dBm
- ANT to RX_FLT insertion loss: 1.5dB
- Integrated 50Ω RF match
- Integrated linear-in-dB power detector
- Supply voltage: 3.1V to 4.25V
- Total supply current at 3.3V:
  - 360mA (TX P_O = 27dBm)
  - 65mA (TX, no RF)
  - 10.3mA (RX only)
- Low sleep mode current: 0.05µA
- Operating ambient temperature range: –40°C to 85°C

2 Applications

- 820MHz to 1054MHz wireless systems
- IEEE 802.15.4 systems
- Smart grid and smart meters:
  - Electricity meters
  - Water meters
  - Gas meters
  - Heat meters
- Smart data concentrators & collectors
- Energy infrastructure wireless communications
- Wireless building automation systems
- Wireless field transmitters & sensors
- Wireless EV charging stations

3 Description

The TRF2001P is a high-performance RF front-end module (FEM) for low-power wireless applications in sub-1GHz industrial, scientific, and medical (ISM) bands operating over an 820MHz to 1054MHz frequency range. The TRF2001P requires minimal external BOM and includes functions such as a range-extender power amplifier (PA) and a low noise amplifier (LNA), transmit-receive antenna switch, antenna port low pass filter, and a linear-in-dB RF power detector, for a cost-effective design in a space-saving 4.5mm × 4.5mm QFN-28 package.

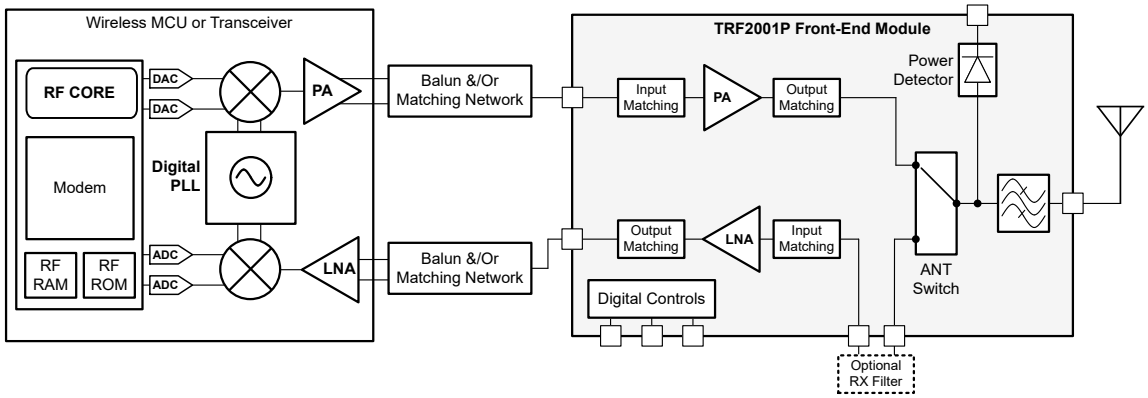
The TRF2001P increases the link budget and allows range extension in wireless systems by providing high output power with the integrated PA, beyond the capabilities of a WMCU or transceiver, and improves the receiver sensitivity with a low noise figure LNA. The integrated power detector can be used for system calibration or to monitor the power being delivered to the antenna. The device features fully matched, 50Ω RF interfaces for ease of use and design flexibility.

The TRF2001P is operational over a wide, 3.1V to 4.25V supply range, with digital controls that are compatible with 1.6V to 3.3V CMOS logic levels.

Device Information

PART NUMBER	PACKAGE(1)	PACKAGE SIZE(2)
TRF2001P	VBA (WQFN-FCRLF, 28) with NiPdAu finish	4.5mm × 4.5mm × 0.7mm

(1) For more information, see Section 10.
(2) The package size (length × width × height) is a nominal value and includes pins.



TRF2001P Typical Configuration with Wireless MCU (WMCU) or Transceiver

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4 Pin Configuration and Functions

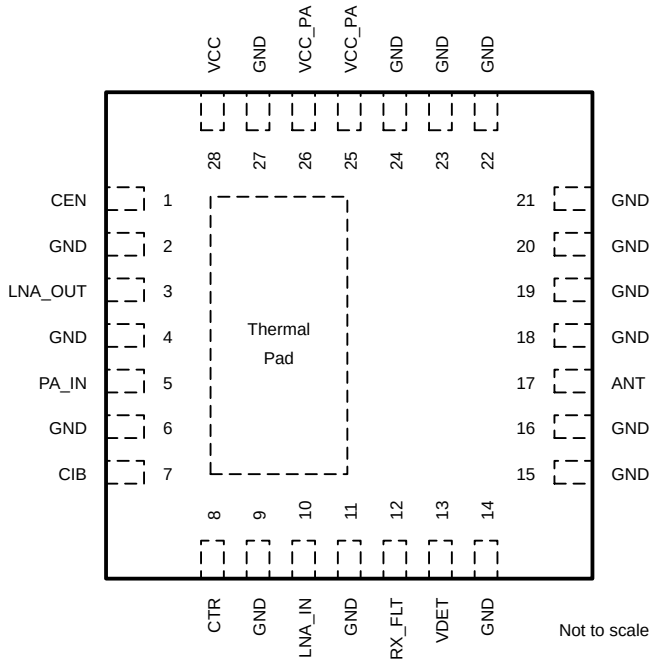


Figure 4-1. VBA Package, 28-Pin WQFN-FCRLF (Top View)

Table 4-1. Pin Functions

PIN		TYPE[1]	DESCRIPTION
NAME	NO.		
ANT	17	I/O	Antenna port.
CEN	1	D	Chip enable digital control logic.
CIB	7	D	Internal bias digital control logic.
CTR	8	D	Transmit and receive path select digital control logic.
GND	2, 4, 6, 9, 11, 14, 15, 16, 18, 19, 20, 21, 22, 23, 24, 27	–	RF ground.
LNA_IN	10	I	LNA input. Short to RX_FLT if a receive filter is not required.
PA_IN	5	I	PA input.
RX_FLT	12	O	Receive signal from ANT pin. Typically RX filter connected between RX_FLT and LNA_IN.
LNA_OUT	3	O	LNA output.
VCC	28	P	LNA and digital control logic supply voltage.
VCC_PA	25, 26	P	PA supply voltage.
VDET	13	O	Power detector voltage output.
Thermal Pad	Pad	–	Thermal pad and serves as ground reference. Connect to heat-dissipating ground plane on the board.

(1) I = analog input, O = analog output, D = digital control logic, P = power,

5 Specifications

5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

			MIN	MAX	UNIT
V_{CC_PA}	PA supply voltage	No RF		4.5	V
V_{CC}	VCC pin supply voltage	No RF		4.5	V
	Input RF level	ANT, RX mode		10	dBm
		LNA_IN		10	
		PA_IN		16	
	Digital control logic pins		−0.5	3.6	V
VSWR	ANT voltage standing wave ratio			10:1	-
T_J	Maximum junction temperature		–40	125	°C
T_{stg}	Storage temperature		–55	150	°C

(1) Operation outside the Absolute Maximum Ratings may cause permanent device damage. Absolute Maximum Ratings do not imply functional operation of the device at these or any other conditions beyond those listed under Recommended Operating Conditions. If used outside the Recommended Operating Conditions but within the Absolute Maximum Ratings, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.

5.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins(1)	±2000	V
		Charged device model (CDM), per JEDEC specification JS-002, all pins(2)	±1000	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

5.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
V_{CC_PA}	PA supply voltage	3.1	3.3	4.25	V
V_{CC}	VCC pin supply voltage	3.1	3.3	4.25	V
T_A	Ambient operating air temperature	–40	25	85	°C

5.4 Thermal Information

THERMAL METRIC(1)		TRF2001P VBA (WQFN-FCRLF) 28 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	34.0	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	15.5	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	9.6	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	0.1	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	9.5	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	5.5	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

5.5 Electrical Characteristics

at T_A = 25°C, V_{CC_PA} = 3.3V, V_{CC} = 3.3V, f = 915MHz, RX_FLT shorted to LNA_IN, RF transmit specification from PA_IN to ANT pin, RF receive specifications from ANT to LNA_OUT pin, 50Ω source and load at input and output RF pins respectively, measured on EVM and de-embedded up to the device pins (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
RF TRANSMIT							
	Frequency range			820		1054	MHz
	Transmit small signal gain	P_{IN} = –25dBm	f = 867MHz		25		dB
			f = 902MHz to 928MHz		24		
P_{SAT}	Saturated output power	f = 867MHz			27.2		dBm
		f = 902MHz			27.5		
		f = 915MHz, 928MHz			27.4		
		V_{CC_PA} = 3.6V, V_{CC} = 3.6V	f = 867MHz		28.1		
			f = 902MHz		28.4		
			f = 915MHz, 928MHz		28.3		
OP1dB	Output 1-dB compression point	f = 867MHz			25.4		dBm
		f = 902MHz			26.2		
		f = 915MHz			26.0		
		f = 928MHz			25.2		
		V_{CC_PA} = 3.6V, V_{CC} = 3.6V	f = 867MHz		25.7		
			f = 902MHz		26.4		
			f = 915MHz		26.6		
			f = 928MHz		26.4		
PAE	Power added efficiency	P_O = 27dBm	f = 867MHz		43.2%		
			f = 902MHz		42.2%		
			f = 915MHz		42.0%		
			f = 928MHz		41.7%		
	Harmonic distortion[1]	f = 867MHz, P_O = 27dBm	2nd harmonic		−59.5		dBc
			3rd harmonic		−67.5		
		f = 928MHz, P_O = 27dBm	2nd harmonic		−56.0		
			3rd harmonic		−72.0		
	Input return loss at PA_IN	P_{IN} = –27dBm			14.5		dB
	Maximum input power at PA_IN	f = 867MHz	VSWR = 1:1		15		dBm
			VSWR = 2:1		15		
			VSWR = 4:1		6		
		f = 928MHz	VSWR = 1:1		15		
			VSWR = 2:1		10		
			VSWR = 4:1		5.5		
	Survivability	CW, P_O into 50Ω load, VSWR = 10:1, without permanent damage			27		dBm
POWER DETECTOR							
	Power detector power range	Power at ANT pin, f = 820MHz to 1054MHz		5		P_{SAT}	dBm
V_{DET}	Power detector voltage range			0		1.8	V

at T_A = 25°C, V_{CC_PA} = 3.3V, V_{CC} = 3.3V, f = 915MHz, RX_FLT shorted to LNA_IN, RF transmit specification from PA_IN to ANT pin, RF receive specifications from ANT to LNA_OUT pin, 50Ω source and load at input and output RF pins respectively, measured on EVM and de-embedded up to the device pins (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
RF RECEIVE							
	Frequency range			820		1054	MHz
	Receive small signal gain	P_{IN} = –27dBm, f = 867MHz to 928MHz			16		dB
NF	Noise figure	f = 867MHz			3.0		dB
		f = 915MHz			3.2		
		LNA_IN to LNA_OUT, f = 867MHz to 928MHz			1.3		
	ANT to RX_FLT insertion loss	P_{IN} = –27dBm			1.5		dB
IIP3	Input 3rd order compression point	P_{IN} = –27dBm	f = 867MHz		–5.2		dBm
			f = 902MHz to 928MHz		–6.0		
IP1dB	Input 1dB compression point	f = 867MHz			−7.6		dBm
		f = 902MHz to 928MHz			−6.7		
	Input return loss at ANT	P_{IN} = –27dBm	f = 867MHz		16		dB
			f = 915MHz		12		dB
	Output return loss at LNA_OUT	P_{IN} = –27dBm	f = 867MHz		18		dB
			f = 915MHz		16		dB

at T_A = 25°C, V_{CC_PA} = 3.3V, V_{CC} = 3.3V, f = 915MHz, RX_FLT shorted to LNA_IN, RF transmit specification from PA_IN to ANT pin, RF receive specifications from ANT to LNA_OUT pin, 50Ω source and load at input and output RF pins respectively, measured on EVM and de-embedded up to the device pins (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
DC SPECIFICATIONS							
I_{CC_PA}	VCC_PA supply current	TX mode	P_O = 27dBm		318		mA
			P_O = 24dBm		228		
			No RF		58		
		RX mode, P_{IN} = –27dBm			0.3		
I_{CC}	VCC supply current	TX mode	P_O = 27dBm		42		mA
			P_O = 24dBm		20		
			No RF		7		
		RX mode, P_{IN} = –27dBm			10		
	Powerdown supply current(2)	No RF			0.05	1	µA
DIGITAL CONTROL LOGIC SPECIFICATIONS							
V_{IH}	High voltage threshold	With respect to GND	High (logic 1)	1.6	3.3	3.45	V
V_{IL}	Low voltage threshold		Low (logic 0)		0	0.5	V
I_{IH}	Pin-high input current	Pin voltage = 3.3V				1	µA
I_{IL}	Pin-low input current	Pin voltage = 0V				1	µA

(1) No external filter on ANT pin. Refer to Figure 5-4 for higher order harmonic performance.
(2) Sum of currents into the VCC_PA and VCC pins.

5.6 Timing Requirements

		MIN	NOM	MAX	UNIT
RF TRANSMIT					
t_{ON}	Turn-on time: time for RF output power at ANT to reach 90% of final value from 50% of CTR edge		1.4		µs
t_{OFF}	Turn-off time: time for RF output power at ANT to reach 10% of final value from 50% of CTR edge		0.4		µs
RF RECEIVE					
t_{ON}	Turn-on time: time for RF output power at LNA_OUT to reach 90% of final value from 50% of CTR edge		0.7		µs
t_{OFF}	Turn-off time: time for RF output power at LNA_OUT to reach 10% of final value from 50% of CTR edge		0.1		µs

5.7 Digital Mode Control Logic

Device Pin Configuration			Description
CEN	CIB	CTR	
1	0	0	Not supported
1	1	0	RX path enabled (RF receive), TX PA powered down
1	0	1	Not supported
1	1	1	TX path enabled (RF transmit)
0	X(1)	X(1)	Device in powered down state
0	0	0	Guaranteed powered down supply current state

(1) Pin logic is ignored

5.8 Typical Characteristics - Transmit

at T_A = 25°C, V_{CC_PA} = V_{CC} = 3.3V, input = PA_IN, output = ANT, RX_FLT shorted to LNA_IN, 50Ω source and load at input and output RF pins respectively, and de-embedded up to the device pins, frequency and ambient temperatures shown (unless otherwise noted)

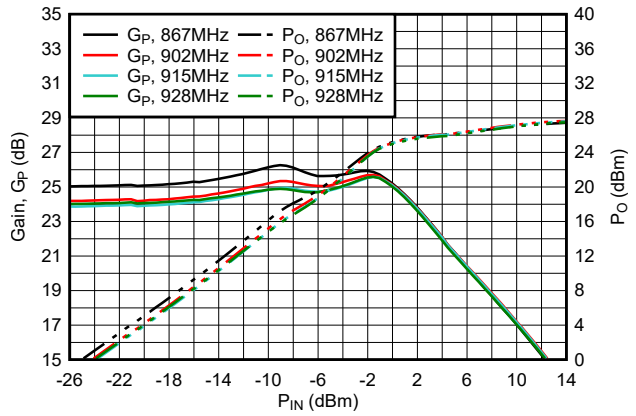


Figure 5-1. Gain and P_O vs P_{IN} Across Frequency

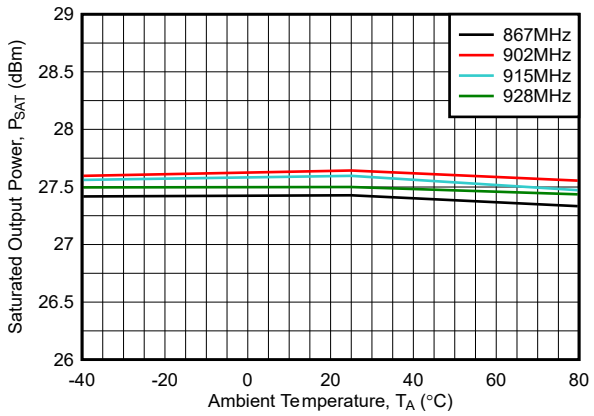


Figure 5-2. P_{SAT} vs Temperature Across Frequency

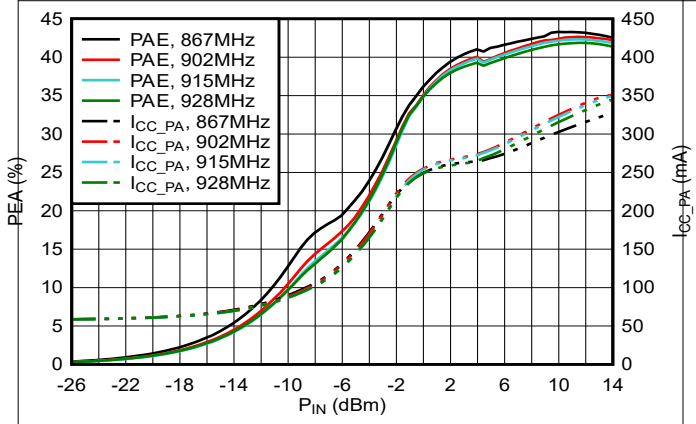
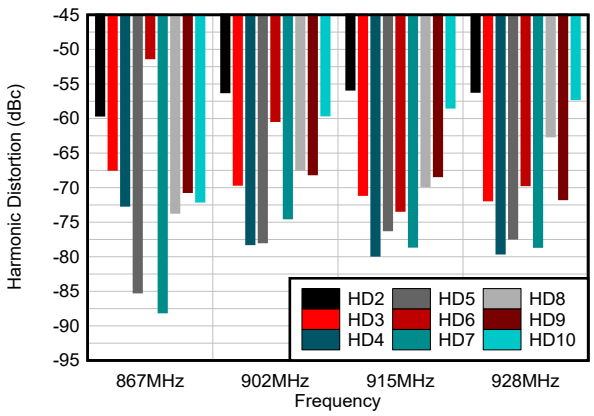
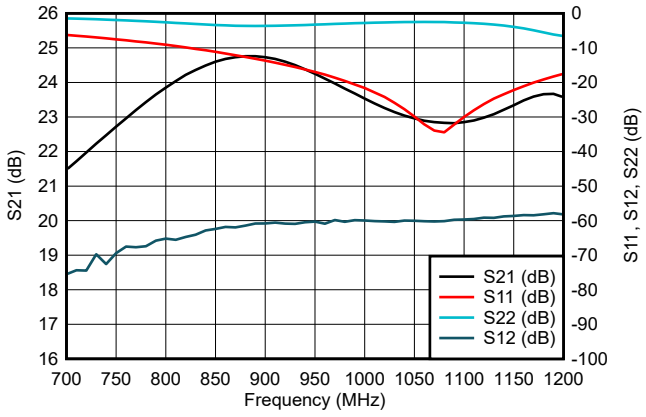


Figure 5-3. PAE and Supply Current vs P_{IN} Across Frequency



P_O = 27dBm

Figure 5-4. Harmonic Distortion Across Frequency



P_{IN} = –27dBm

Figure 5-5. Small-Signal S-Parameters

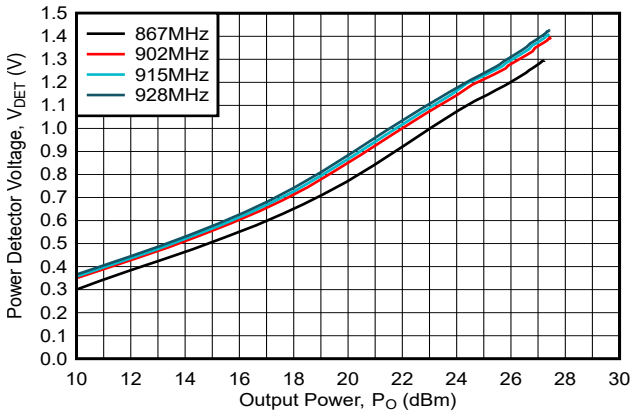
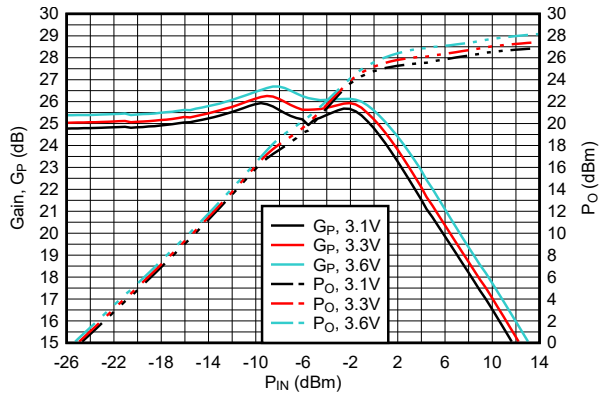


Figure 5-6. V_{DET} vs P_O Across Frequency

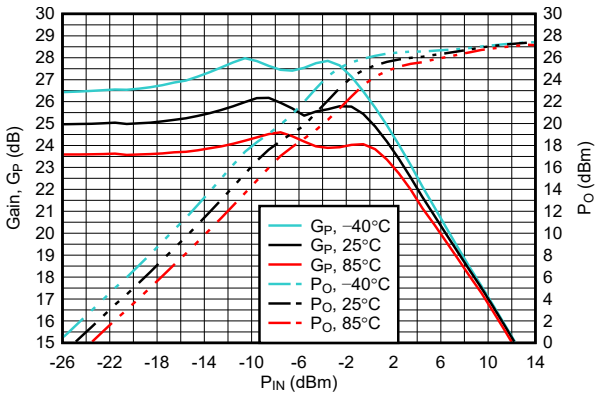
5.8 Typical Characteristics - Transmit (continued)

at T_A = 25°C, V_{CC_PA} = V_{CC} = 3.3V, input = PA_IN, output = ANT, RX_FLT shorted to LNA_IN, 50Ω source and load at input and output RF pins respectively, and de-embedded up to the device pins, frequency and ambient temperatures shown (unless otherwise noted)



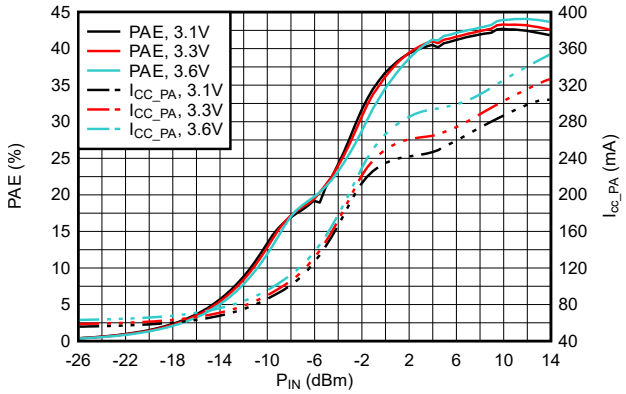
f = 867MHz, V_{CC_PA} as shown, V_{CC} = V_{CC_PA}

Figure 5-7. Gain and P_O vs P_{IN} Across Supply Voltage



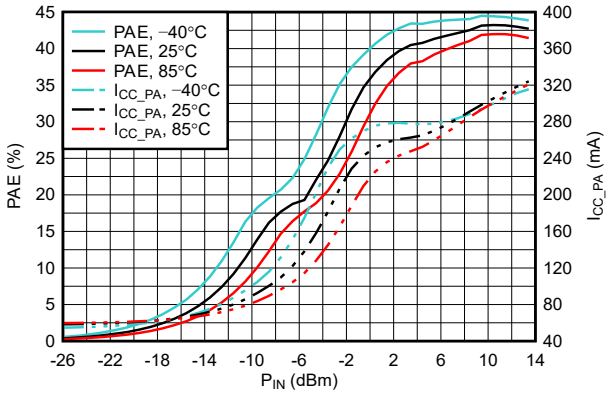
f = 867MHz

Figure 5-8. Gain and P_O vs P_{IN} Across Temperature



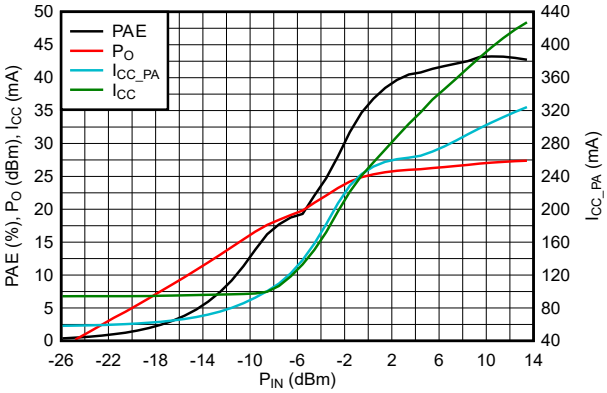
f = 867MHz, V_{CC} = V_{CC_PA}

Figure 5-9. PAE and Supply Current vs P_{IN} Across Supply Voltage



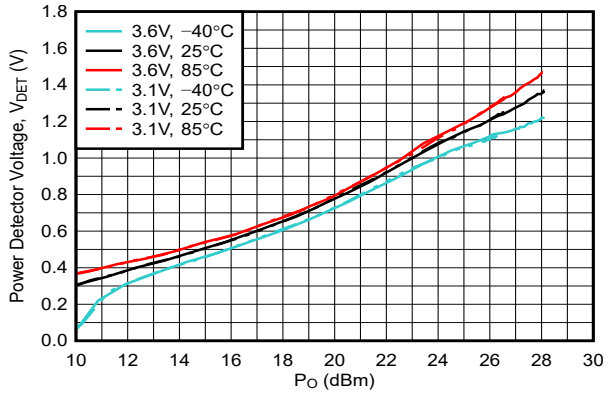
f = 867MHz

Figure 5-10. PAE and Supply Current vs P_{IN} Across Temperature



f = 867MHz

Figure 5-11. PAE, P_O, and Supply Current vs P_{IN}

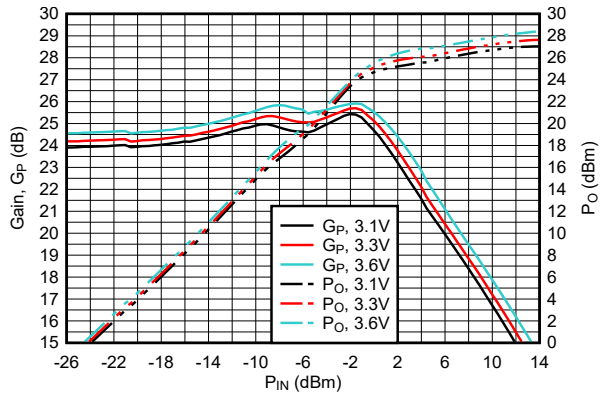


f = 867MHz, V_{CC_PA} as shown, V_{CC} = V_{CC_PA}

Figure 5-12. V_{DET} vs P_O Across Supply Voltage and Temperature

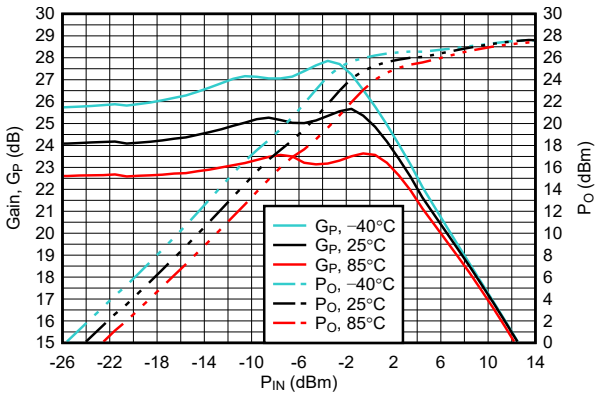
5.8 Typical Characteristics - Transmit (continued)

at T_A = 25°C, V_{CC_PA} = V_{CC} = 3.3V, input = PA_IN, output = ANT, RX_FLT shorted to LNA_IN, 50Ω source and load at input and output RF pins respectively, and de-embedded up to the device pins, frequency and ambient temperatures shown (unless otherwise noted)



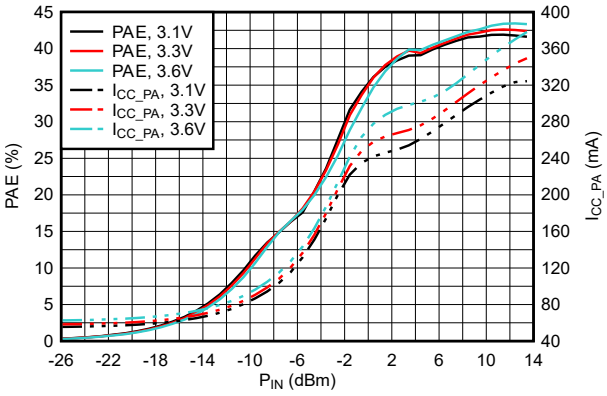
f = 902MHz, V_{CC_PA} as shown, V_{CC} = V_{CC_PA}

Figure 5-13. Gain and P_O vs P_{IN} Across Supply Voltage



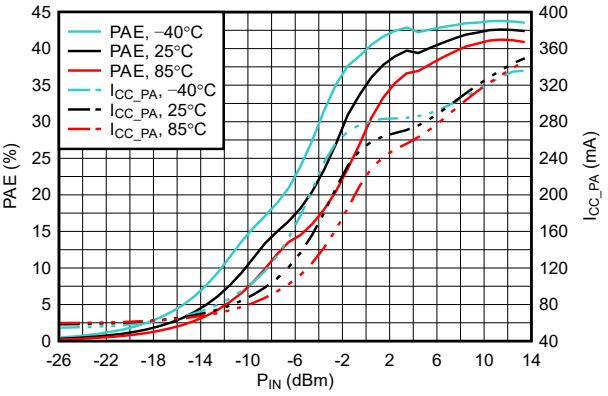
f = 902MHz

Figure 5-14. Gain and P_O vs P_{IN} Across Temperature



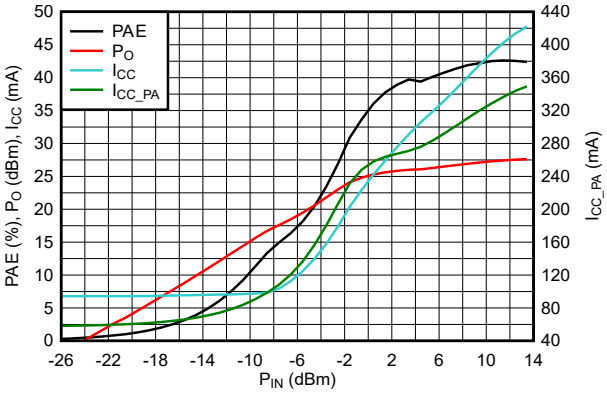
f = 902MHz, V_{CC} = V_{CC_PA}

Figure 5-15. PAE and Supply Current vs P_{IN} Across Supply Voltage



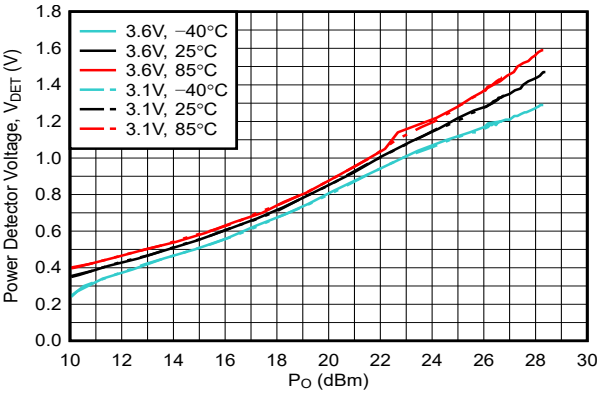
f = 902MHz

Figure 5-16. PAE and Supply Current vs P_{IN} Across Temperature



f = 902MHz

Figure 5-17. PAE, P_O, and Supply Current vs P_{IN}

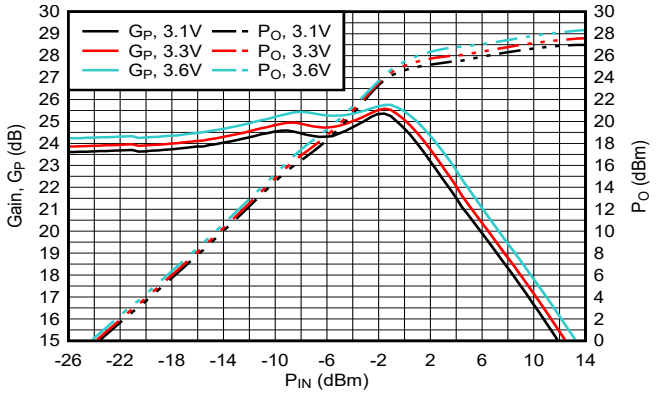


f = 902MHz, V_{CC_PA} as shown, V_{CC} = V_{CC_PA}

Figure 5-18. V_{DET} vs P_O Across Supply Voltage and Temperature

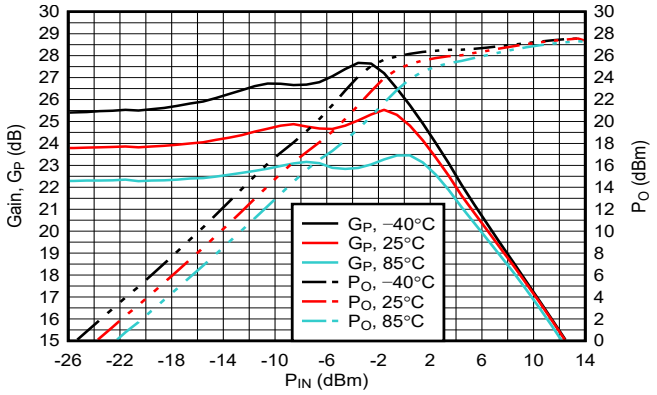
5.8 Typical Characteristics - Transmit (continued)

at T_A = 25°C, V_{CC_PA} = V_{CC} = 3.3V, input = PA_IN, output = ANT, RX_FLT shorted to LNA_IN, 50Ω source and load at input and output RF pins respectively, and de-embedded up to the device pins, frequency and ambient temperatures shown (unless otherwise noted)



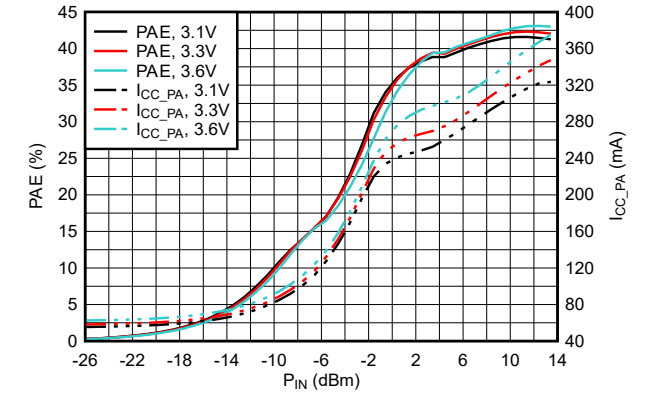
f = 915MHz, V_{CC_PA} as shown, V_{CC} = V_{CC_PA}

Figure 5-19. Gain and P_O vs P_{IN} Across Supply Voltage



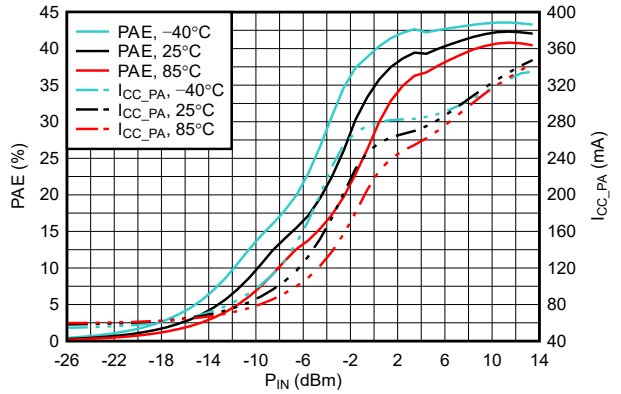
f = 915MHz

Figure 5-20. Gain and P_O vs P_{IN} Across Temperature



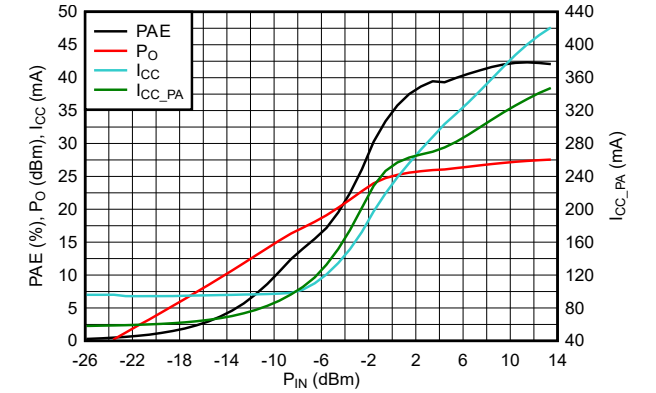
f = 915MHz, V_{CC} = V_{CC_PA}

Figure 5-21. PAE and Supply Current vs P_{IN} Across Supply Voltage



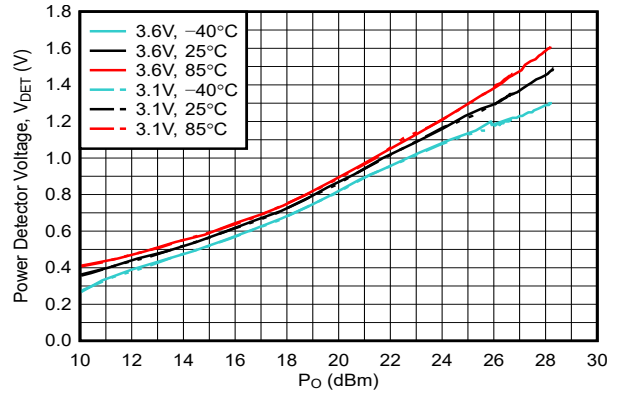
f = 915MHz

Figure 5-22. PAE and Supply Current vs P_{IN} Across Temperature



f = 915MHz

Figure 5-23. PAE, P_O, and Supply Current vs P_{IN}

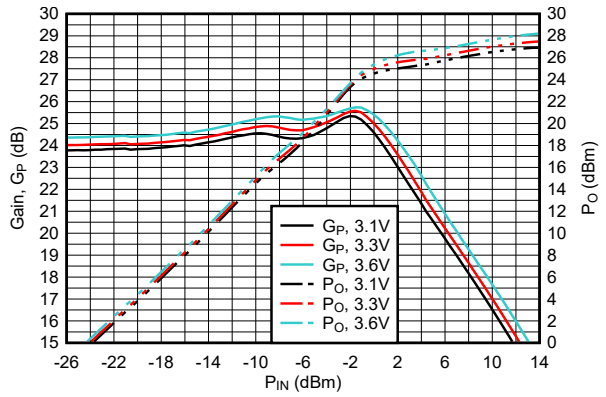


f = 915MHz, V_{CC_PA} as shown, V_{CC} = V_{CC_PA}

Figure 5-24. V_{DET} vs P_O Across Supply Voltage and Temperature

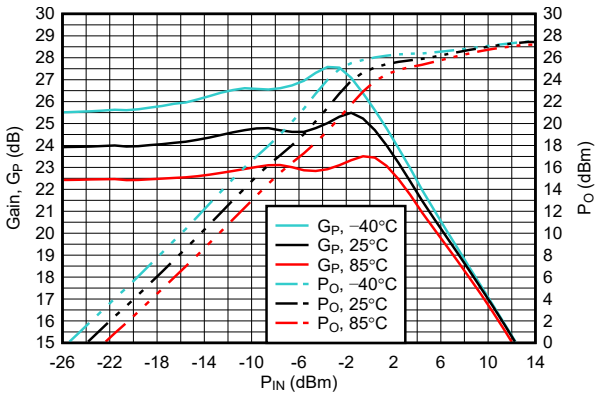
5.8 Typical Characteristics - Transmit (continued)

at T_A = 25°C, V_{CC_PA} = V_{CC} = 3.3V, input = PA_IN, output = ANT, RX_FLT shorted to LNA_IN, 50Ω source and load at input and output RF pins respectively, and de-embedded up to the device pins, frequency and ambient temperatures shown (unless otherwise noted)



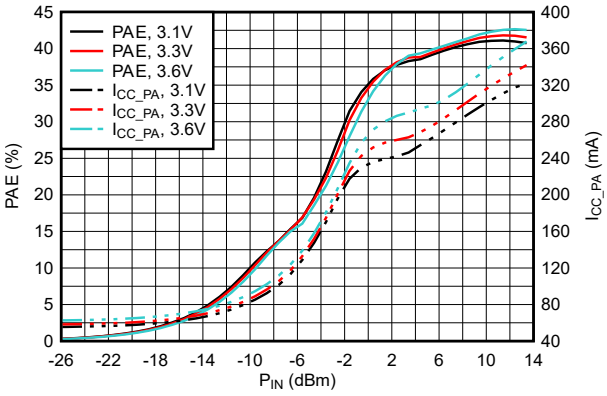
f = 928MHz, V_{CC_PA} as shown, V_{CC} = V_{CC_PA}

Figure 5-25. Gain and P_O vs P_{IN} Across Supply Voltage



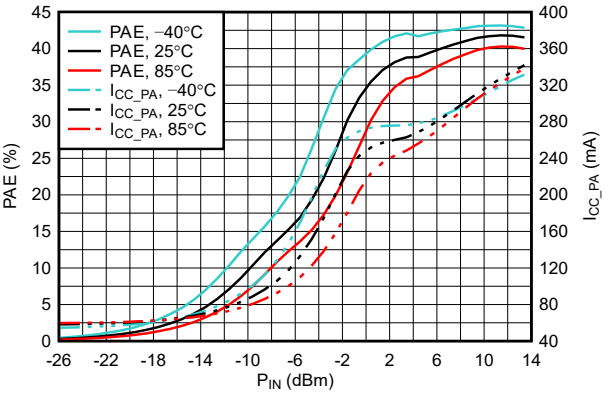
f = 928MHz

Figure 5-26. Gain and P_O vs P_{IN} Across Temperature



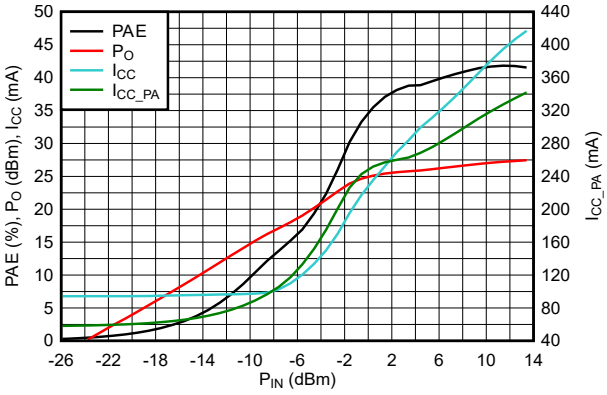
f = 928MHz, V_{CC} = V_{CC_PA}

Figure 5-27. PAE and Supply Current vs P_{IN} Across Supply Voltage



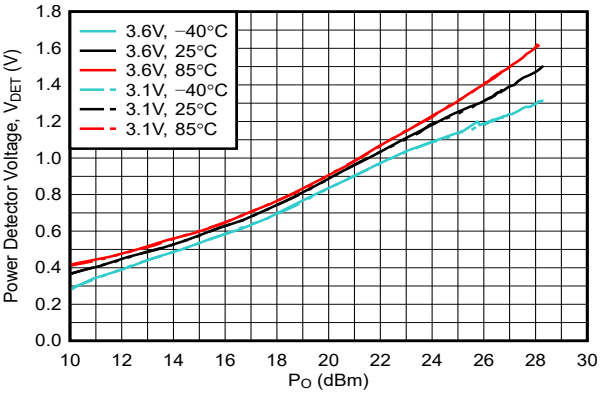
f = 928MHz

Figure 5-28. PAE and Supply Current vs P_{IN} Across Temperature



f = 928MHz

Figure 5-29. PAE, P_O, and Supply Current vs P_{IN}

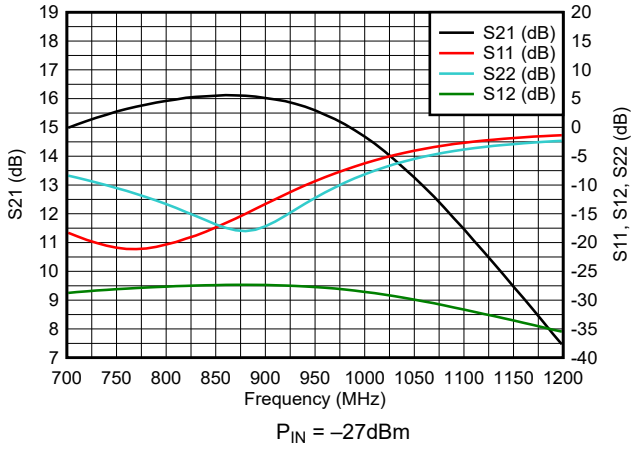


f = 928MHz, V_{CC_PA} as shown, V_{CC} = V_{CC_PA}

Figure 5-30. V_{DET} vs P_O Across Supply Voltage and Temperature

5.9 Typical Characteristics - Receive

at T_A = 25°C, V_{CC_PA} = V_{CC} = 3.3V, input = ANT, output = LNA_OUT, RX_FLT shorted to LNA_IN, 50Ω source and load at input and output RF pins respectively, and de-embedded up to the device pins, frequency and ambient temperatures shown (unless otherwise noted)



P_{IN} = –27dBm

Figure 5-31. Small-Signal S-Parameters

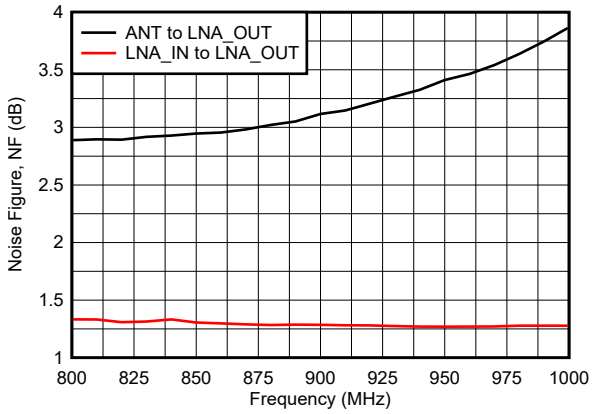


Figure 5-32. Noise Figure

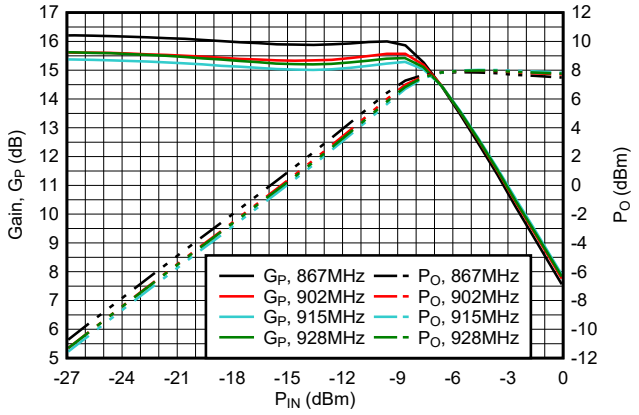
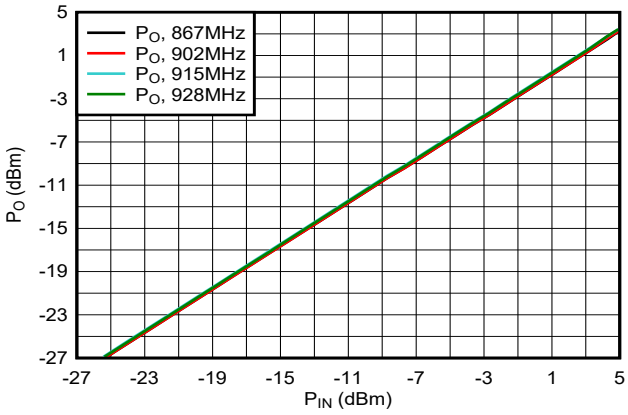
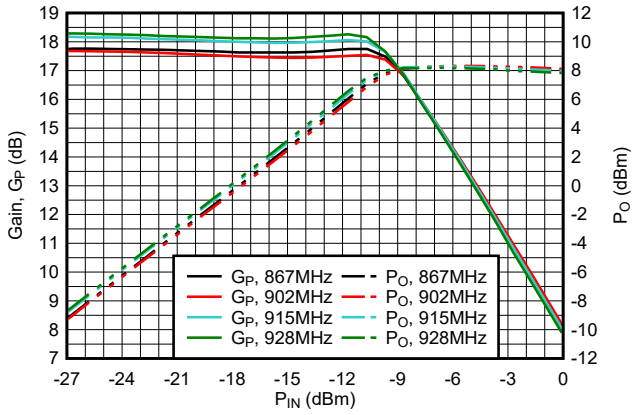


Figure 5-33. Gain and P_O vs P_{IN} Across Frequency



Input = ANT, output = RX_FLT

Figure 5-34. P_O vs P_{IN} Across Frequency



Input = LNA_IN, output = LNA_OUT

Figure 5-35. Gain and P_O vs P_{IN} Across Frequency

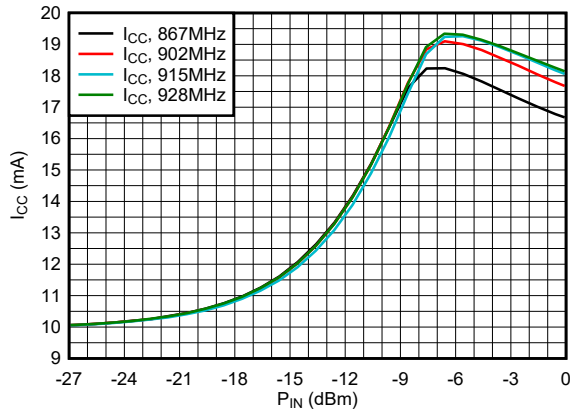


Figure 5-36. Supply Current vs P_{IN}

5.9 Typical Characteristics - Receive (continued)

at T_A = 25°C, V_{CC_PA} = V_{CC} = 3.3V, input = ANT, output = LNA_OUT, RX_FLT shorted to LNA_IN, 50Ω source and load at input and output RF pins respectively, and de-embedded up to the device pins, frequency and ambient temperatures shown (unless otherwise noted)

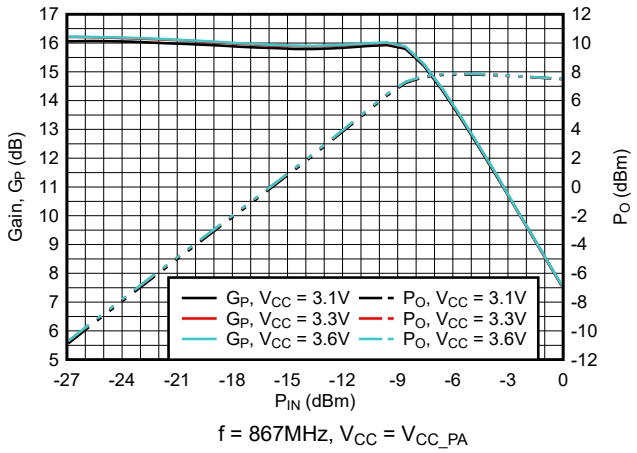


Figure 5-37. Gain and P_O vs P_{IN} Across Supply Voltage

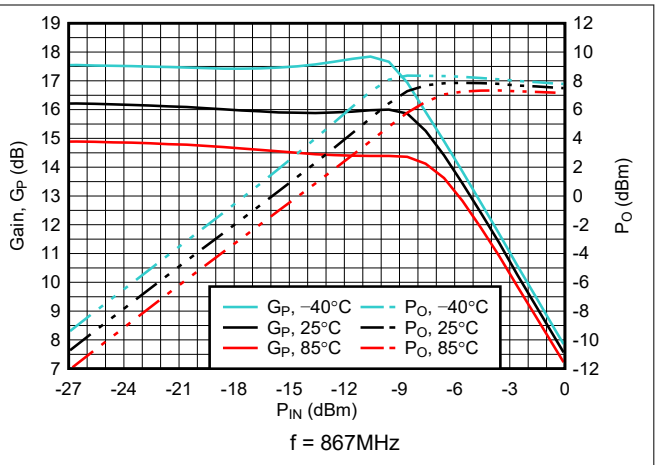


Figure 5-38. Gain and P_O vs P_{IN} Across Temperature

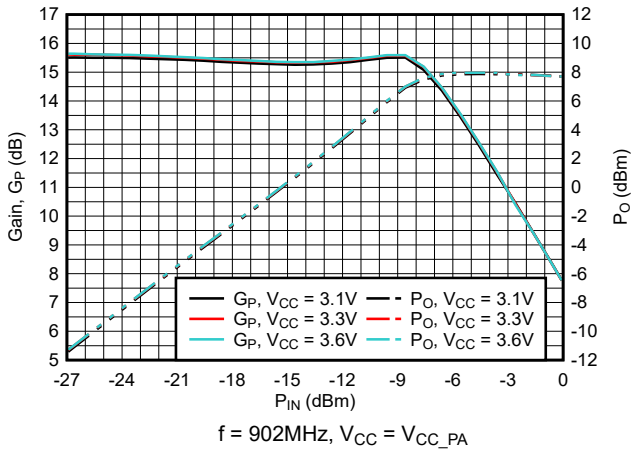


Figure 5-39. Gain and P_O vs P_{IN} Across Supply Voltage

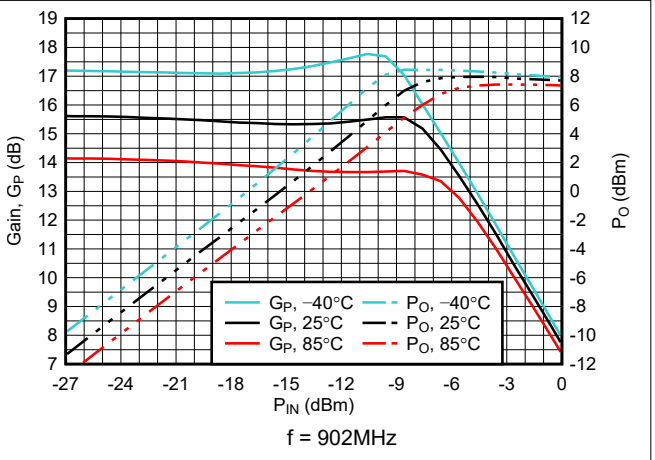


Figure 5-40. Gain and P_O vs P_{IN} Across Temperature

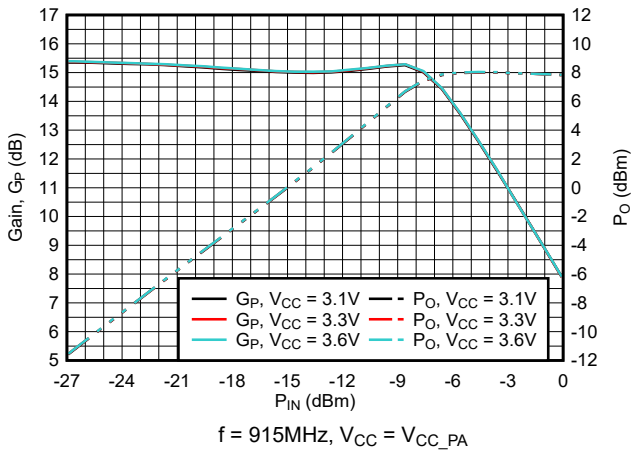


Figure 5-41. Gain and P_O vs P_{IN} Across Supply Voltage

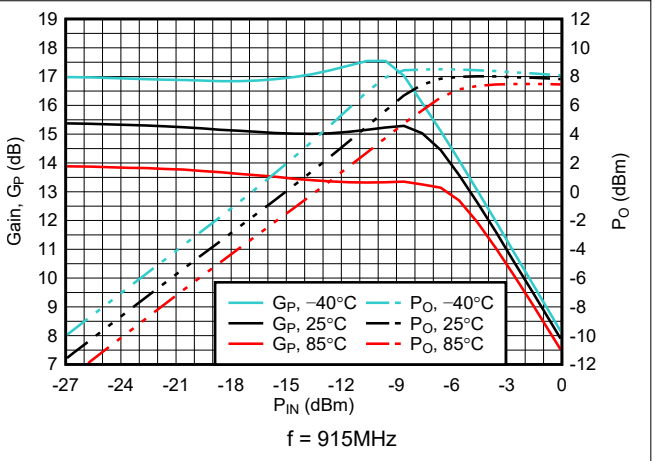
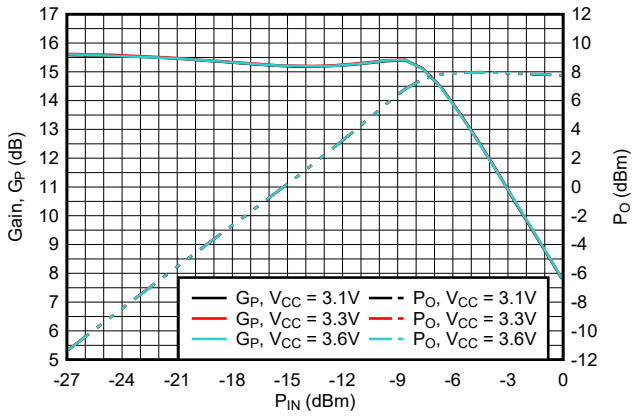


Figure 5-42. Gain and P_O vs P_{IN} Across Temperature

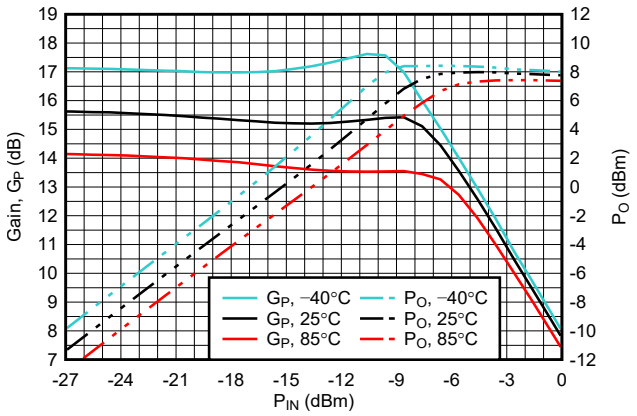
5.9 Typical Characteristics - Receive (continued)

at T_A = 25°C, V_{CC_PA} = V_{CC} = 3.3V, input = ANT, output = LNA_OUT, RX_FLT shorted to LNA_IN, 50Ω source and load at input and output RF pins respectively, and de-embedded up to the device pins, frequency and ambient temperatures shown (unless otherwise noted)



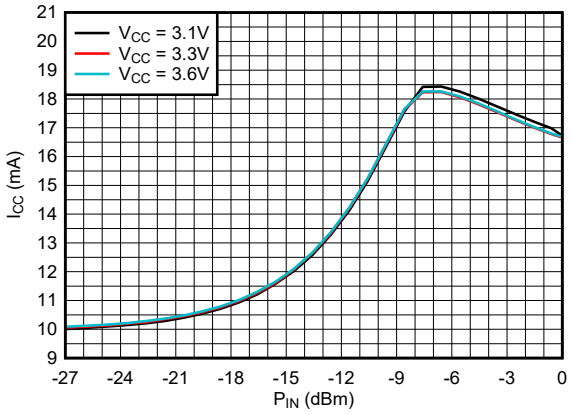
f = 928MHz, V_{CC} = V_{CC_PA}

Figure 5-43. Gain and P_O vs P_{IN} Across Supply Voltage



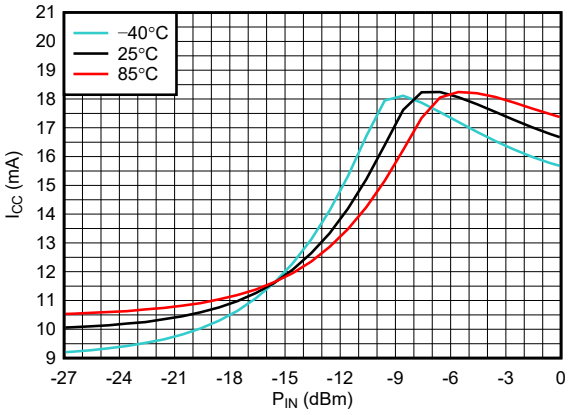
f = 928MHz

Figure 5-44. Gain and P_O vs P_{IN} Across Temperature



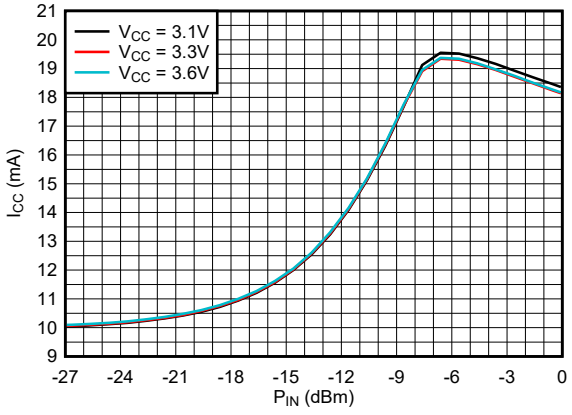
f = 867MHz, V_{CC} = V_{CC_PA}

Figure 5-45. Supply Current vs P_{IN} Across Supply Voltage



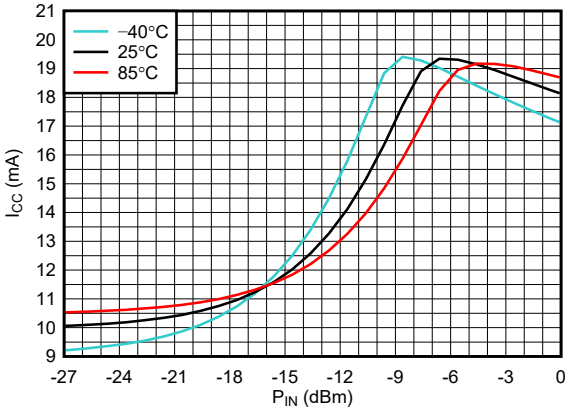
f = 867MHz

Figure 5-46. Supply Current vs P_{IN} Across Temperature



f = 928MHz, V_{CC} = V_{CC_PA}

Figure 5-47. Supply Current vs P_{IN} Across Supply Voltage



f = 928MHz

Figure 5-48. Supply Current vs P_{IN} Across Temperature

6 Detailed Description

6.1 Overview

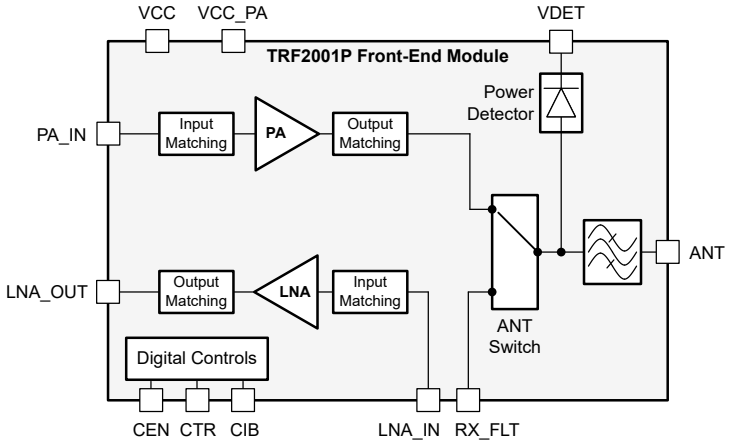
The TRF2001P is a high-performance RF front-end module (FEM) designed to be paired with wireless microcontroller (MCU) and system-on-chip (SoC) ICs for applications primarily supporting various sub-1GHz ISM bands. The device improves the link budget by increasing the system's TX power well beyond the capabilities of the wireless MCUs and SoCs with the integrated PA and improving the RX sensitivity with the integrated LNA.

A key limitation of most wireless SoCs designed for the sub-1GHz ISM band is that the transmit (TX) output power is typically limited to about 16dBm, with very few supporting up to 22dBm. When these SoCs are used at TX powers greater than 10dBm, the spurious-free dynamic range (SFDR) often deteriorates. The increased spurious levels require additional filtering and metal shielding in many cases, to comply with regulatory requirements such as those set by the FCC and ETSI standards. The TRF2001P allows the SoCs to operate at lower output power levels by providing additional RF gain and high TX output power capability that exceed 27dBm, thus reducing the SoC's spurious levels, and often eliminating the need for additional filtering and shielding.

With integrated, fully matched 50Ω RF interfaces, the TRF2001P simplifies interface design to the antenna and the wireless SoCs. The digital control logic pins (CEN, CTR, and CIB) of the device are used to configure the device in TX, RX, or device powered down mode, and are compatible with CMOS levels of 1.6V to 3.3V.

The TRF2001P operates over a wide single supply voltage range of 3.1V to 4.25V and achieves 27.5dBm P_{SAT} on 3.3V supply. The device is available in a space-saving 4.5mm × 4.5mm, 28-pin, WQFN-FCRLF package.

6.2 Functional Block Diagram



6.3 Feature Description

Besides the PA, LNA, and the ANT switch, the TRF2001P integrates additional functions such as a harmonic rejection filter and a power detector in a small 4.5mm × 4.5mm package.

The integrated harmonic rejection filter either eliminates the need for an external filter to the antenna or notably relaxes the rejection requirements of the external filter if the system requires one. The TRF2001P inherently achieves second order harmonic rejection below –55dBc at P_O = 27dBm without any external filtering. The integrated power detector provides analog voltage output corresponding to the output power as shown in Figure 5-6 and has a very stable response across temperature and supply voltage.

6.4 Device Functional Modes

The TRF2001P three functional modes: Transmit (TX), Receive (RX), and power down mode. The operating mode of the device is set using the digital control pins, CEN, CTR, and CIB as shown in Section 5.7. In the TX mode the PA path is enabled by connecting the ANT switch to the PA output path. In the RX mode, the ANT switch connects to the RX_FLT pin. Connect an optional RX filter between RX_FLT and LNA_IN pins to reject out-of-band signals or short the RX_FLT pin to LNA_IN pin to engage the LNA in the receive path.

7 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

7.1 Application Information

The TRF2001P is a FEM typically used with wireless SoCs to extend the communication range beyond what the SoCs are natively capable of, and to provide an improved link budget. The primary application of the TRF2001P is in the ISM band frequency range of 860MHz to 928MHz but the TX and RX performance holds well beyond this frequency range to support communication systems in an extended frequency range of 820MHz to 1054MHz.

7.2 Typical Application

7.2.1 TRF2001P as Range Extender

Figure 7-1 shows a typical application of the TRF2001P when used as a range extender, paired with wireless MCUs or SoCs.

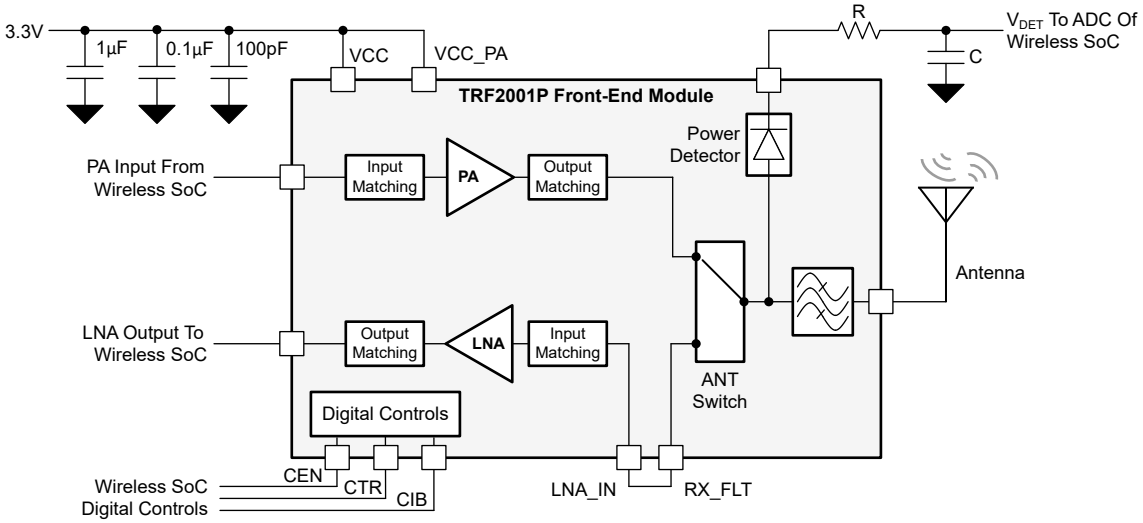


Figure 7-1. TRF2001P as Range Extender Paired with Wireless SoC

7.2.1.1 Design Requirements

Use TRF2001P to extend the communication range and the TX output power in a sub-1GHz system using a wireless SoC. The design parameters in Table 7-1 are for a 50Ω matched system.

Table 7-1. Design Parameters

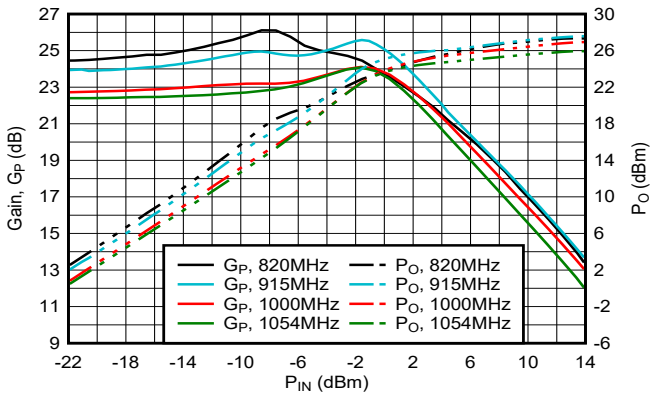
DESIGN PARAMETER		VALUE
f ≤ 1000MHz	TX P_{SAT}	≥ 27dBm
	RX small-signal gain	≥ 14dB
f = 1054MHz	TX P_{SAT}	≥ 26dBm
	RX small-signal gain	≥ 12dB

7.2.1.2 Detailed Design Procedure

The TRF2001P has integrated 50Ω matching elements and as shown in Figure 7-1, does not require any external matching components to achieve the design goals.

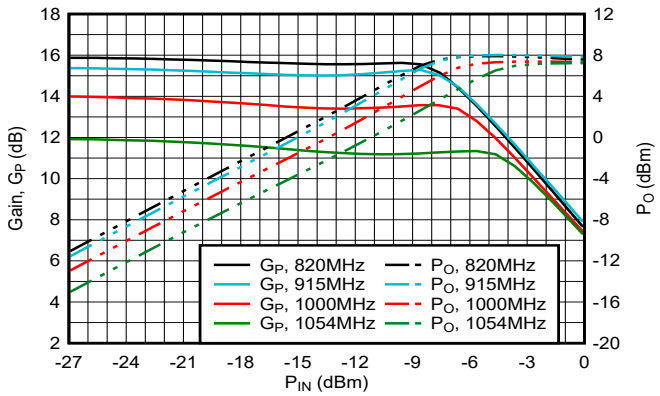
7.2.1.3 Application Curves

Figure 7-2 and Figure 7-3 show the TX and RX performance, respectively, for the TRF2001P configuration as shown in Figure 7-1.



V_{CC_PA} = V_{CC} = 3.3V, input = PA_IN, output = ANT, T_A = 25°C

Figure 7-2. Transmit Performance



V_{CC_PA} = V_{CC} = 3.3V, input = ANT, output = LNA_OUT, T_A = 25°C

Figure 7-3. Receive Performance

7.3 Power Supply Recommendations

The TRF2001P operates on a 3.1V to 4.25V single-supply voltage. Isolate the supply voltage through decoupling capacitors placed close to the device. Select capacitors with self-resonant frequency greater than the application frequency. When multiple capacitors are used in parallel to create a broadband decoupling network, place the capacitor with the higher self-resonant frequency closer to the device. Use a ferrite bead in series with the supply source if there is a need to isolate undesired high frequencies in the system. Choose a ferrite bead that provides high impedance at the lowest undesired frequency and beyond.

7.4 Layout

7.4.1 Layout Guidelines

Figure 7-4 shows example layout for TRF2001P. Only the top signal layer (layer 1) and second ground layer (layer 2) are shown. Use a multilayer board to maintain signal integrity and power integrity.

- Route the RF signals as grounded coplanar waveguide (GCPW) traces.
- Maintain that the ground planes on the top and any internal layers are well stitched with vias, and the second layer of the PCB has a continuous ground layer without any cutouts in the vicinity of the device.
- Avoid routing clocks and digital control lines near RF signal lines.
- Do not route RF or DC signal lines over noisy power planes.
- Place supply decoupling caps close to the device.
- Use small-footprint, passive components wherever possible.

See the *TRF2001P Evaluation Module user's guide* for more details on board layout and design. The TRF2001P can be evaluated using the *TRF2001P Evaluation Module*.

7.4.1.1 Thermal Considerations

The TRF2001P is packaged in a WQFN-FCRLF package that has excellent thermal properties. Connect the thermal pad underneath the device to the thermally dissipative ground plane on the board. For good thermal design, use thermal vias to connect the thermal pad plane on the top layer of the PCB to the ground planes in the inner layers.

7.4.2 Layout Example

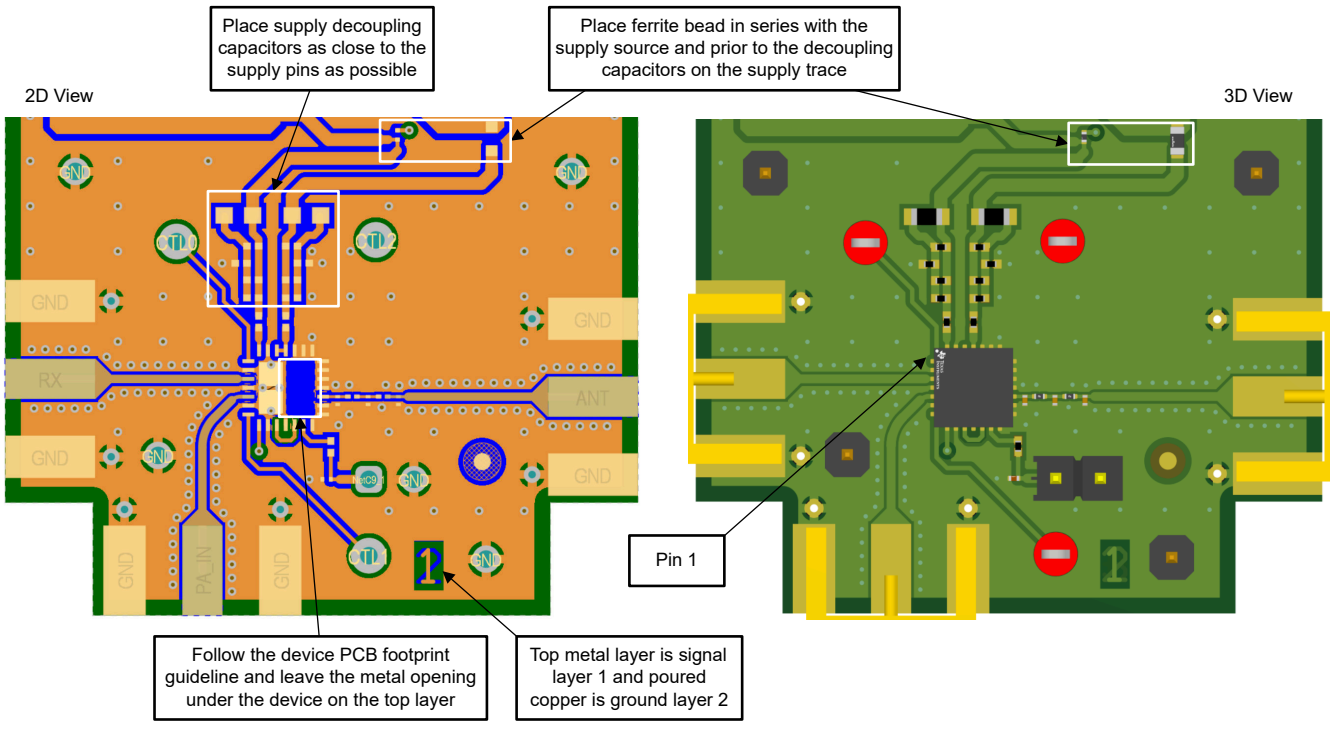


Figure 7-4. Layout Example

8 Device and Documentation Support

8.1 Documentation Support

8.1.1 Related Documentation

For related documentation, see the following:

- Texas Instruments, *TRF2001P Evaluation Module user's guide*

8.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

8.3 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

8.4 Trademarks

TI E2E™ is a trademark of Texas Instruments.
All trademarks are the property of their respective owners.

8.5 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

8.6 Glossary

TI Glossary	This glossary lists and explains terms, acronyms, and definitions.

9 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

DATE	REVISION	NOTES
December 2025	*	Draft only

10 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TRF2001PVBAR	Active	Production	WQFN-FCRLF (VBA) | 28	3000 | LARGE T&R	-	NIPDAU	Level-2-260C-1 YEAR	-	(T201A21, T201PA21)

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

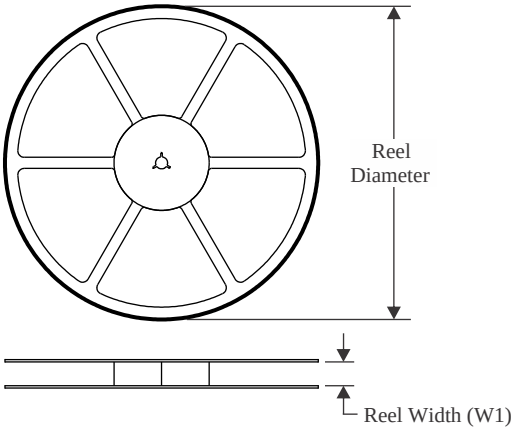
(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

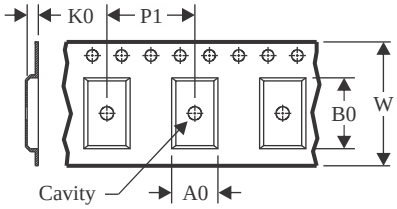
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

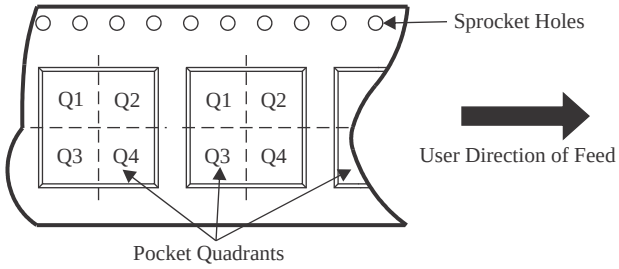


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

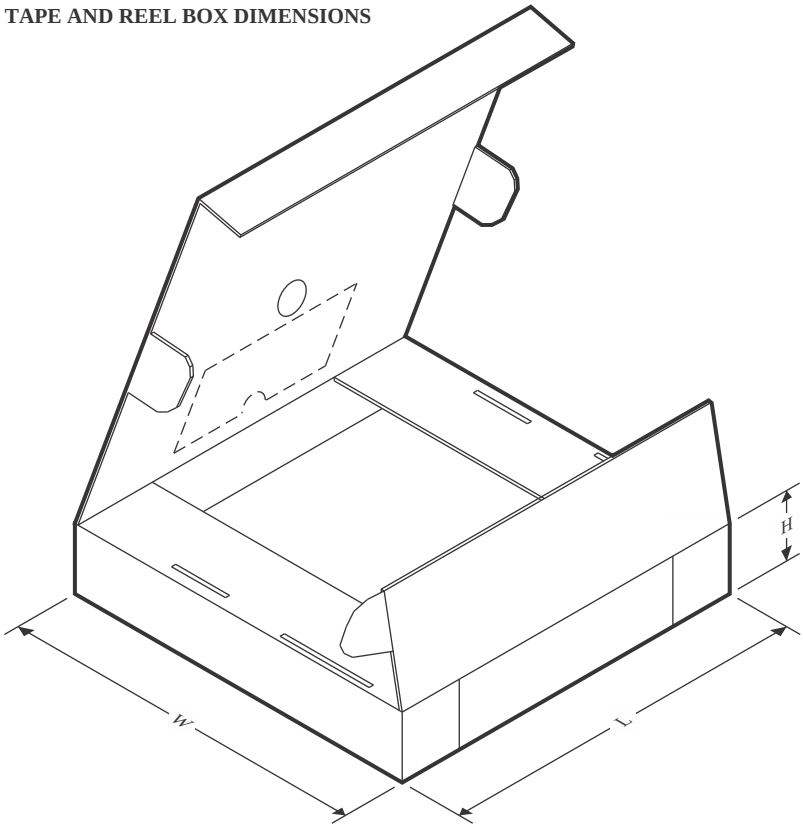
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TRF2001PVBAR	WQFN-FCRLF	VBA	28	3000	330.0	12.4	4.75	4.75	1.6	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

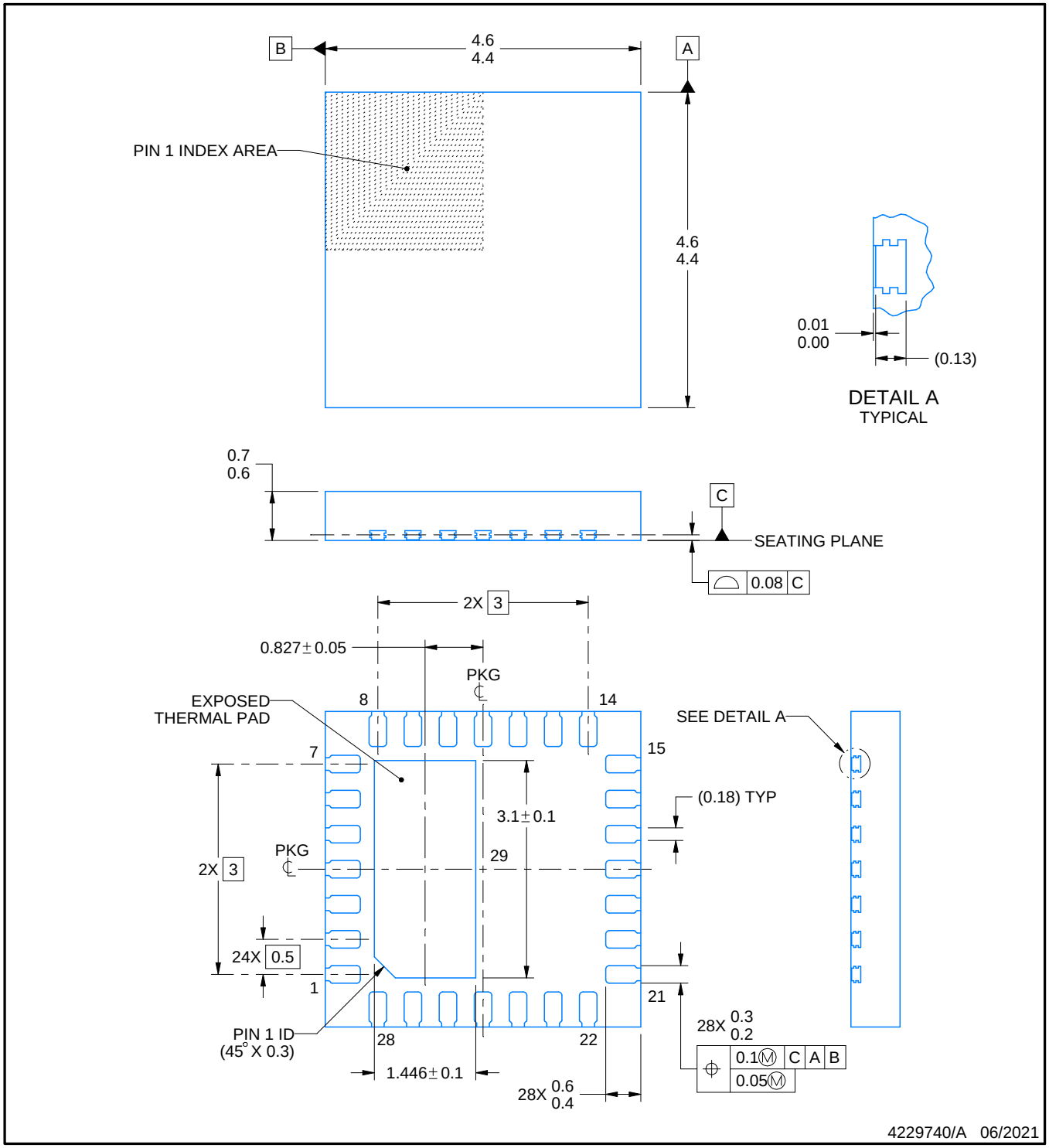
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TRF2001PVBAR	WQFN-FCRLF	VBA	28	3000	336.6	336.6	31.8

PACKAGE OUTLINE

VBA0028A

WQFN-FCRLF - 0.7 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



NOTES:

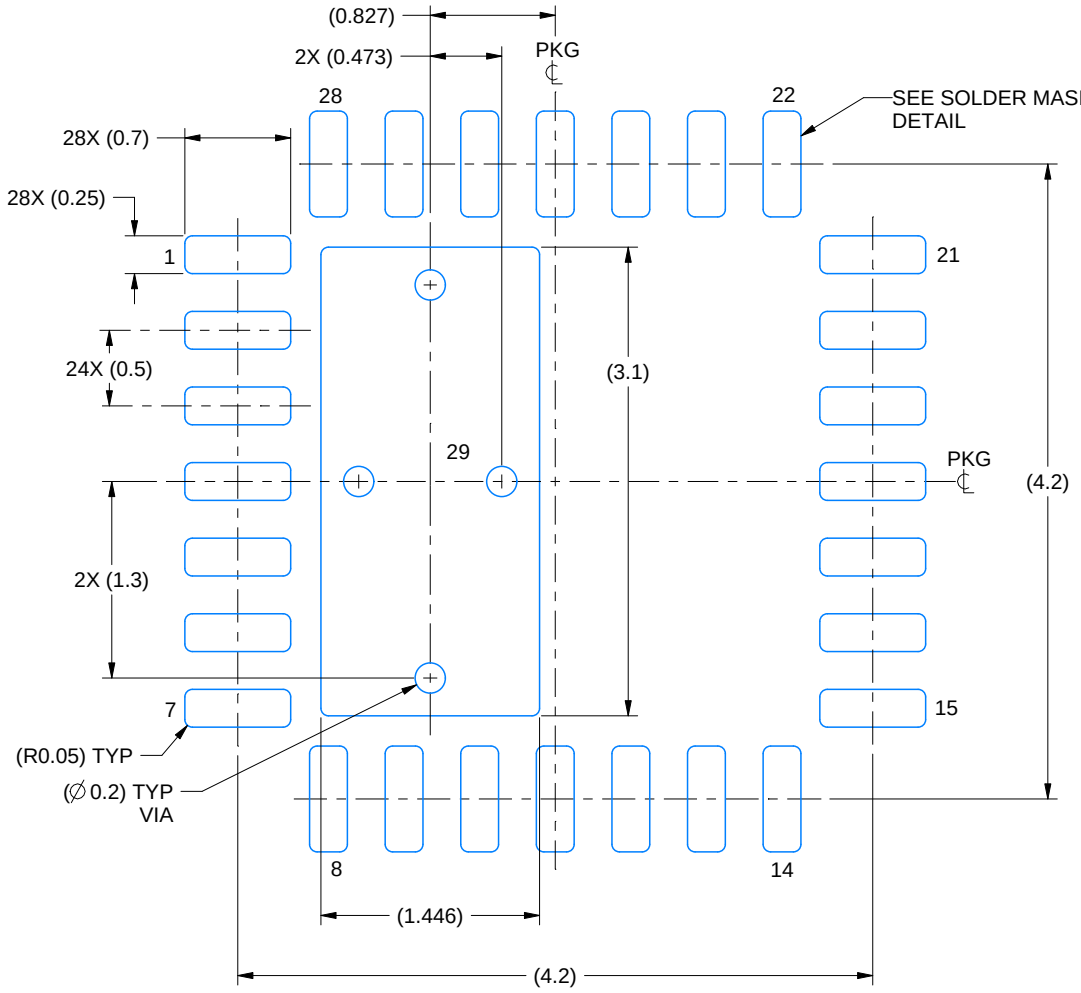
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.

EXAMPLE BOARD LAYOUT

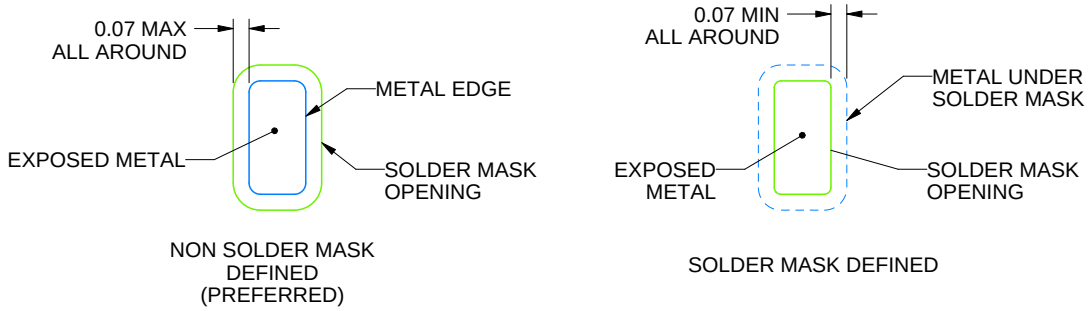
VBA0028A

WQFN-FCRLF - 0.7 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 20X



SOLDER MASK DETAILS

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NOTES: (continued)

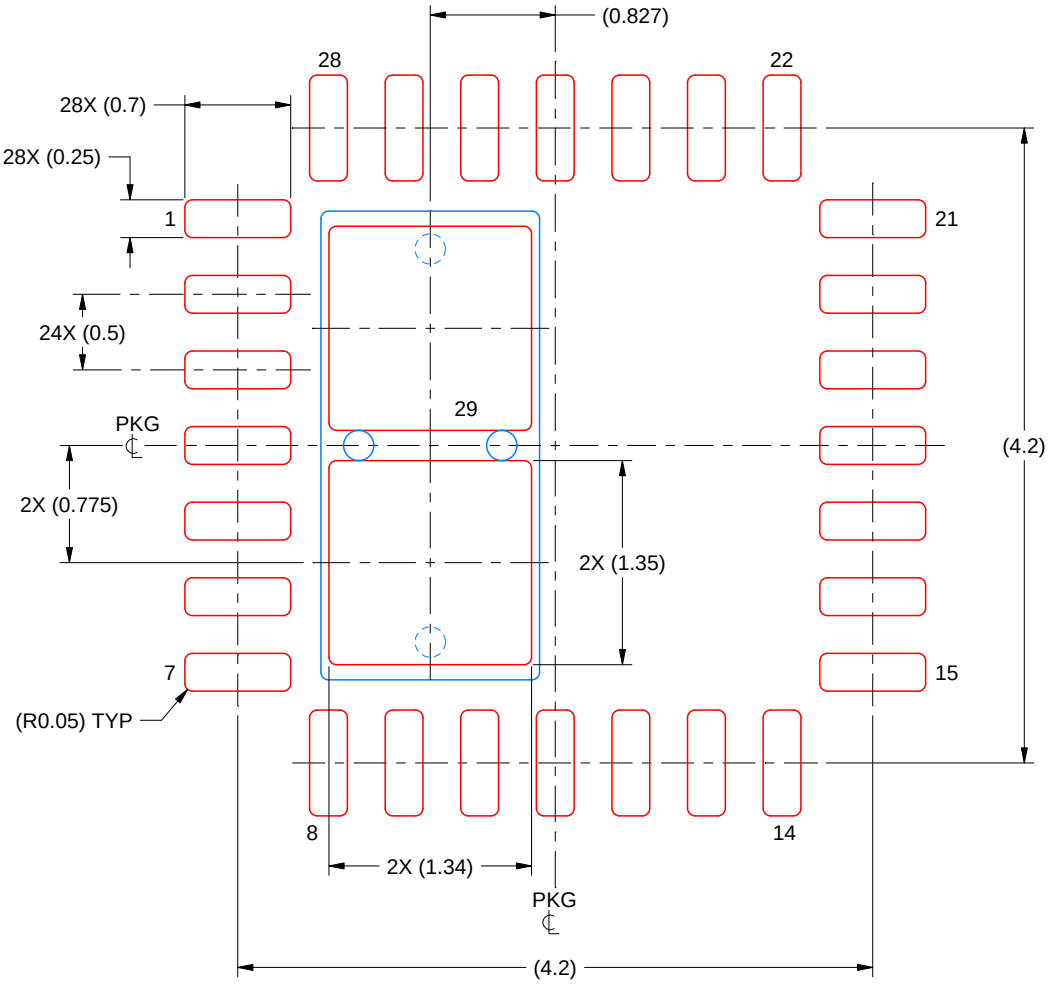
4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.

EXAMPLE STENCIL DESIGN

VBA0028A

WQFN-FCRLF - 0.7 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



SOLDER PASTE EXAMPLE
BASED ON 0.125 MM THICK STENCIL
SCALE: 20X

EXPOSED PAD 29
35% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE

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NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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