

2 X 2 Crosspoint Switch for Audio Applications

Check for Samples: TS3A26746E

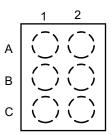
FEATURES

- Ultra Low R_{ON} for GND Switch (80-mΩ typical)
- R_{ON} for MIC Switch <10-Ω
- 3.0V to 3.6V V+ Operation
- Control Input is 1.8-V Logic Compatible
- 6-bump, 0.5mm pitch CSP Package (1.45mm × 0.95mm × 0.5mm)
- Latch-Up Performance Exceeds 100 mA Per JESD 78, Class II
- ESD Performance Tested Per JESD 22
 - 2000-V Human-Body Model (A114-B, Class II)
 - 500-V Charged-Device Model (C101)
- ESD Performance (SLEEVE, RING2)
 - ±8-kV Contact Discharge (IEC 61000-4-2)

APPLICATIONS

- Cellular phones
- PDAs
- Portable Instrumentation
- Digital Still Cameras
- Portable Navigation Devices

PINOUT



DESCRIPTION

The TS3A26746E is a 2 × 2 cross-point switch that is used to interchange the Ground and MIC connections on a headphone connector. The Ground switch has an ultra low R_{ON} of <0.1 Ω to minimize voltage drop across it, preventing undesired increases in headphone ground reference voltage. The switch state is controlled via the SEL input. When SEL=High, GND is connected to RING2 and MIC is connected to SLEEVE. When SEL=Low, GND is connected to SLEEVE and MIC is connected to RING2. An internal 100k pull-up resistor on the SEL input sets the default state of the switch.



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.





These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

TYPICAL APPLICATION BLOCK DIAGRAM

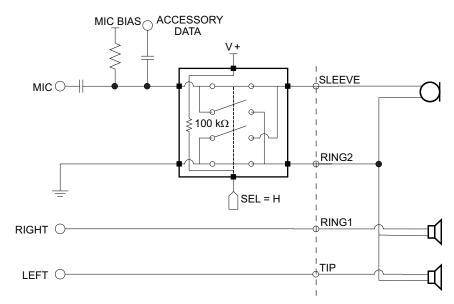


Figure 1. Standard Headphone Configuration (SEL=H)

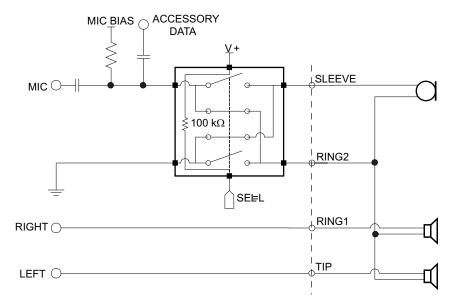
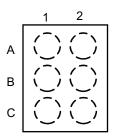


Figure 2. Alternate Headphone Configuration (SEL=L)



PINOUT



TERMINAL ASSIGNMENTS

	1	2
Α	SEL	V+
В	MIC	SLEEVE
С	GND	RING2

PIN FUNCTIONS

BALL#	PIN		DESCRIPTION
DALL#	NAME	TYPE	DESCRIPTION
A1 SEL Input		Input	Control Input
A2	A2 V+ Power		Supply Voltage
B1	B1 MIC I/O		MIC
B2	B2 SLEEV I/O		Sleeve Connection on Headphone Jack
C1 GND Ground		Ground	Ground
C2 RING2 I/O		I/O	2 nd Ring Connection on Headphone Jack

Table 1. FUNCTION TABLE

SEL	MIC to SLEEVE, GND to RING2	MIC to RING2, GND to SLEEVE
L	OFF	ON
Н	ON	OFF

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ABSOLUTE MAXIMUM RATINGS(1)(2)

over operating free-air temperature range (unless otherwise noted)

			MIN	MAX	UNIT
V ₊	Supply voltage range (3)		-0.3	4.0	V
V _{MIC} V _{SLEEVE} V _{RING2}	Analog voltage range ⁽³⁾		-0.3	4.0	V
I _K	Analog port diode current	V _{MIC} , V _{SLEEVE} , V _{RING2} < 0 V	-50		mA
VI	Digital input voltage rang	е	-0.3	4.0	V
I _{IK}	Digital input clamp current (3)	V _I < 0 V	-50		mA
I ₊	Continuous current throu	gh V ₊		100	mA
I _{GND}	Continuous current throu	gh GND	-100		mA
θ_{JA}	Package thermal impedance ⁽⁴⁾	YZP package		102	°C/W
T _{stg}	Storage temperature ran	ge	-65	150	°C

- (1) Stresses above these ratings may cause permanent damage. Exposure to absolute maximum conditions for extended periods may degrade device reliability. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those specified is not implied.
- (2) The algebraic convention, whereby the most negative value is a minimum and the most positive value is a maximum.
- (3) All voltages are with respect to ground, unless otherwise specified.
- (4) The package thermal impedance is calculated in accordance with JESD 51-7.

ELECTRICAL CHARACTERISTICS FOR 3.3 V SUPPLY⁽¹⁾

 $V_{+} = 3 \text{ V to } 3.6 \text{ V}, T_{A} = -40^{\circ}\text{C to } 85^{\circ}\text{C (unless otherwise noted)}$

PARAMETER		TEST CONDITIONS	TA	V_{+}	MIN	TYP	MAX	UNIT	
MIC SWITCH									
$\begin{matrix} V_{MIC}, V_{SLEEVE}, \\ V_{RING2} \end{matrix}$	Analog signal range					0		V+	V
r	ON-state	0 ≤ V _{SLEEVE} or V _{RING2} ≤ V ₊ , I _{MIC} = −32	Switch	25°C	3 V		5	8	Ω
r _{on}	resistance	mA	ON	Full				10	\$2
	ON-state	$0 \le V_{SLEEVE}$ or $V_{RING2} \le V_+$, $I_{MIC} = -32$	Switch	25°C	3 V		1	2.3	
r _{on(flat)}	resistance flatness	mA	ON	Full				2.5	Ω
I _{SLEEVE(OFF)} ,	SLEEVE, RING2	V _{SLEEVE} or V _{RING2} = 1 V, V _{MIC} = 3 V, or	Switch	25°C		-0.5	0.05	0.5	
I _{RING2(OFF)}	OFF leakage current	V _{SLEEVE} or V _{RING2} = 3 V, V _{MIC} = 1 V		Full	3.6 V	-2		2	μA
1	MIC OFF leakage V_{SLEEVE} or $V_{RING2} = 3 \text{ V}$, $V_{MIC} = 1 \text{ V}$, or V_{SLEEVE} or $V_{RING2} = 1 \text{ V}$, $V_{MIC} = 3 \text{ V}$		Switch	25°C	3.6 V	-1	0.1	1	
IMIC(OFF)			OFF	OFF Full		-2		2	μA
I _{SLEEVE(ON)} ,	SLEEVE, RING2	V _{SLEEVE} or V _{RING2} = 1 V, V _{MIC} = Open, or	Switch	25°C		-2	0.5	2	
I _{RING2(ON)}	ON leakage current	V _{SLEEVE} or V _{RING2} = 3 V, V _{MIC} = Open	ON	Full	3.6 V	-2		2	μA
1	MIC ON leakage	V _{SLEEVE} or V _{RING2} = Open V, V _{MIC} = 1 V,	Switch	25°C	261/	-2	0.5	2	
I _{MIC(ON)}	current	or V_{SLEEVE} or V_{RING2} = Open, V_{MIC} = 3 V ON		Full 3.6 V		-2		2	μA
GND SWITCH				·					
	ON-state	I _{SLEEVE} or I _{RING2} = +32 mA, V _{GND} = 0 V,	Switch	25°C	3 V		0.08	0.09	Ω
r _{on}	resistance	$I_{GND} = -32 \text{ mA}$	ON	Full	3 V			0.11	122
I _{SLEEVE(OFF)} ,		// or // - 2\/ and // 0.\/	Switch	25°C	3.6 V	-0.5	0.05	0.5	
I _{RING2(OFF)}	SLEEVE, RING2	V_{SLEEVE} or $V_{RING2} = 3V$ and $V_{GND} = 0 V$	OFF	Full	3.0 V	-1		1	μA
I _{SLEEVE(PWROFF}	OFF leakage	OFF leakage current V_{SLEEVE} or $V_{RING2} = 0$ to 3.6 V and V_{GND} $= 0$ V		25°C		-1	0.5	1	
), I _{RING2(PWROFF))}	Ouron			Full	0 V	-10		10	μA

(1) The algebraic convention, whereby the most negative value is a minimum and the most positive value is a maximum

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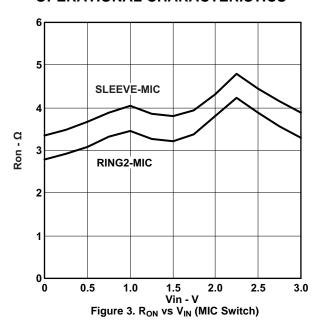
ELECTRICAL CHARACTERISTICS FOR 3.3 V SUPPLY⁽¹⁾ (continued)

 $V_{+} = 3 \text{ V}$ to 3.6 V, $T_{A} = -40^{\circ}\text{C}$ to 85°C (unless otherwise noted)

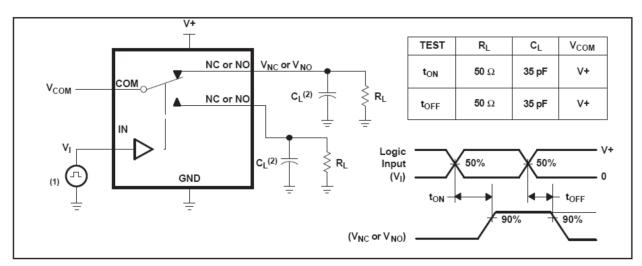
PARAMETER		TEST CONDITION	TA	V_{+}	MIN	TYP	MAX	UNIT	
DIGITAL C	ONTROL INPUTS (SEL)							
V _{IH}	Input logic high			Full	3.6 V	1.2		3.6	V
V _{IL}	Input logic low		Full	3.6 V	0		0.4	V	
L	Input logic high	$V_1 = V_+$			3.6 V	-1	0.05	1	μA
I _{IH}	leakage current	VI = V+		Full		-2		2	μΑ
I _{IL}	Input logic low leakage current	V _I = 0 V		25°C Full	3.6 V	-38	-36	-34	μA
	leakage current					-4 5		-30	
DYNAMIC		T		1 1					
		V D 50.0	C ₁ = 35	25°C	3.3 V		150	200	
t _{ON}	Turn-on time	$V_{MIC} = V_+, R_L = 50 \Omega$	C _L = 35 pF	Full	3 V to 3.6 V			250	ns
			C - 25	25°C	3.3 V		5	10	
t _{OFF}	Turn-off time	$V_{MIC} = V_{+}, R_{L} = 50 \Omega$ C_{L} pF		Full	3 V to 3.6 V			15	ns
	Duranta haɗa wa		25°C		3.3 V	70		330	ns
t _{BBM}	Break-before- make time	$V_{MIC} = V_{+}$	Full		3 V to 3.6 V			330	
C _{MIC}	MIC capacitance	SEL=High	25°C		3.3 V		100	140	pF
		SEL=Low	25°C		3.3 V		100	140	pF
0	SLEEVE / RING2	SEL=High	25°C		3.3 V		100	140	pF
C _{SLEEVE}	capacitance	SEL=Low	25°C		3.3 V		100	140	pF
C _I	Digital input capacitance	V _I = V ₊ or 0 V	25°C		3.3 V		4.0		pF
THD	Total harmonic distortion	$R_L = 1k \Omega$, $V = 30 \text{ mVPP}$	f = 20 Hz to 20 kHz	25°C	3.3 V		0.01%		
SUPPLY			•						
V+	Power Supply Voltage					3.0	3.3	3.6	V
		V _I = V ₊			3.6 V		0.01	1	
	Positive supply							5	μΑ
I ₊	current						40	41	
		$V_1 = U V$	$V_I = 0 V$					50	μA



OPERATIONAL CHARACTERISTICS



PARAMETER MEASRUMENT INFORMATION

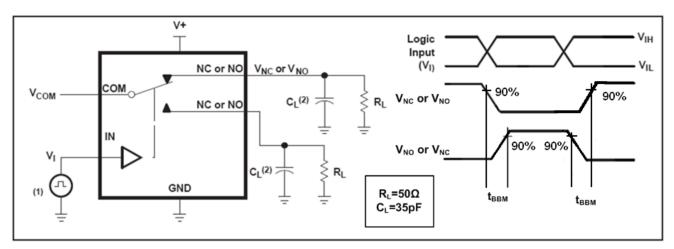


- A. All input pulses are supplied by generators having the following characteristics: PRR \leq 10 MHz, $Z_O = 50 \Omega$, $t_r < 5 \text{ ns}$, $t_r < 5 \text{ ns}$.
- B. C_L includes probe and jig capacitance.

Figure 4. Turn-On (t_{ON}) and Turn-Off Time (t_{OFF})



PARAMETER MEASRUMENT INFORMATION (continued)



- C_L includes probe and jig capacitance.
- B. All input pulses are supplied by generators having the following characteristics: PRR \leq 10 MHz, Z_O = 50 Ω , t_r \leq 5 ns.

Figure 5. Break-Before-Make Time (t_{BBM})



REVISION HISTORY

Changes from Revision B (November 2011) to Revision C Replaced 1 page preview with full document.				
•	Replaced 1 page preview with full document.			

www.ti.com 11-Nov-2025

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type	Package Pins	Package qty Carrier	RoHS (3)	Lead finish/ Ball material	MSL rating/ Peak reflow	Op temp (°C)	Part marking (6)
TS3A26746EYZPR	Active	Production	DSBGA (YZP) 6	3000 LARGE T&R	Yes	SNAGCU	Level-1-260C-UNLIM	-40 to 85	7N
TS3A26746EYZPR.B	Active	Production	DSBGA (YZP) 6	3000 LARGE T&R	Yes	SNAGCU	Level-1-260C-UNLIM	-40 to 85	7N

⁽¹⁾ Status: For more details on status, see our product life cycle.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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⁽²⁾ Material type: When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

⁽³⁾ RoHS values: Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

⁽⁴⁾ Lead finish/Ball material: Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

⁽⁵⁾ MSL rating/Peak reflow: The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

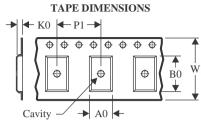
⁽⁶⁾ Part marking: There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

PACKAGE MATERIALS INFORMATION

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TAPE AND REEL INFORMATION





A0	Dimension designed to accommodate the component width
В0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE

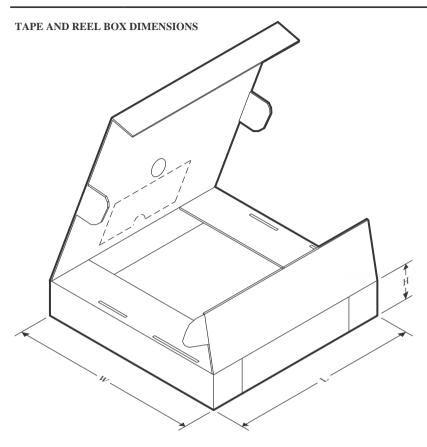


*All dimensions are nominal

Device	Package Type	Package Drawing		SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TS3A26746EYZPR	DSBGA	YZP	6	3000	180.0	8.4	1.02	1.52	0.63	4.0	8.0	Q1

PACKAGE MATERIALS INFORMATION

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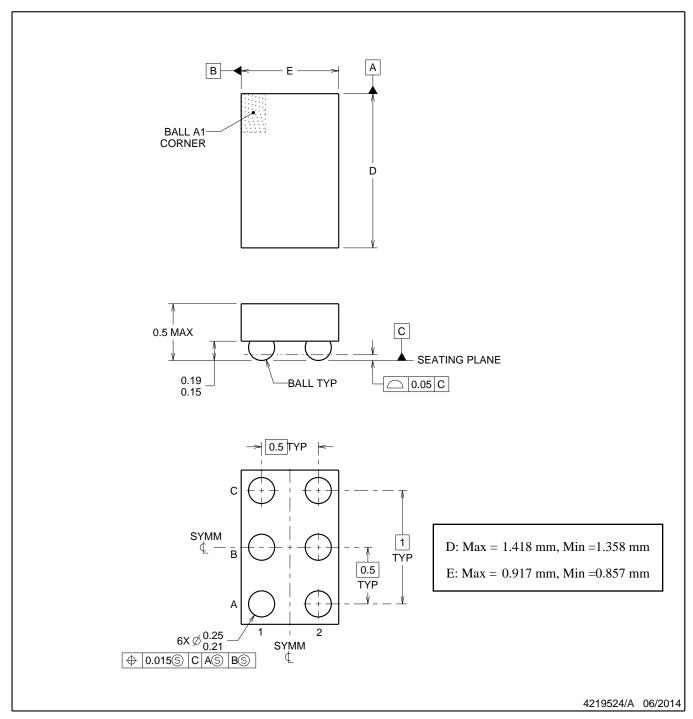


*All dimensions are nominal

	Device	Device Package Type		Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
ı	TS3A26746EYZPR	DSBGA	YZP	6	3000	182.0	182.0	20.0



DIE SIZE BALL GRID ARRAY



NOTES:

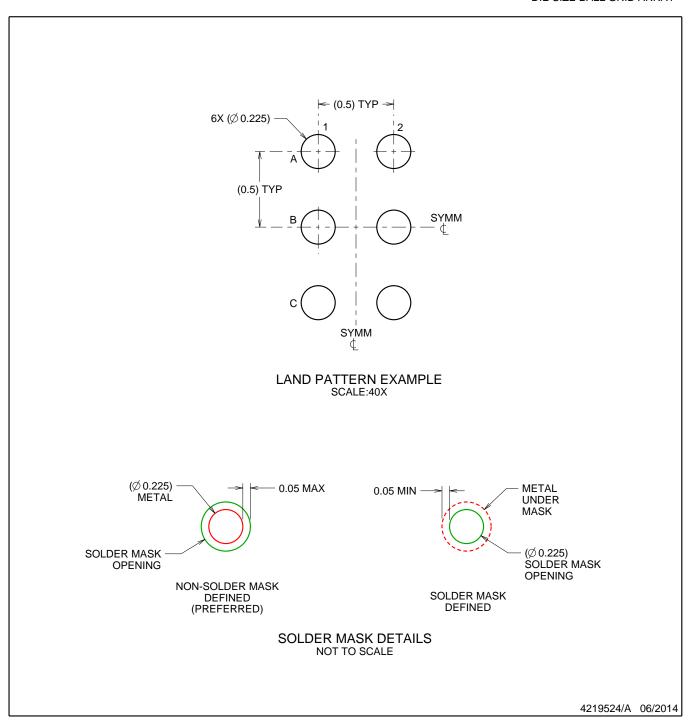
NanoFree Is a trademark of Texas Instruments.

- 1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.

 2. This drawing is subject to change without notice.
- 3. NanoFree[™] package configuration.



DIE SIZE BALL GRID ARRAY

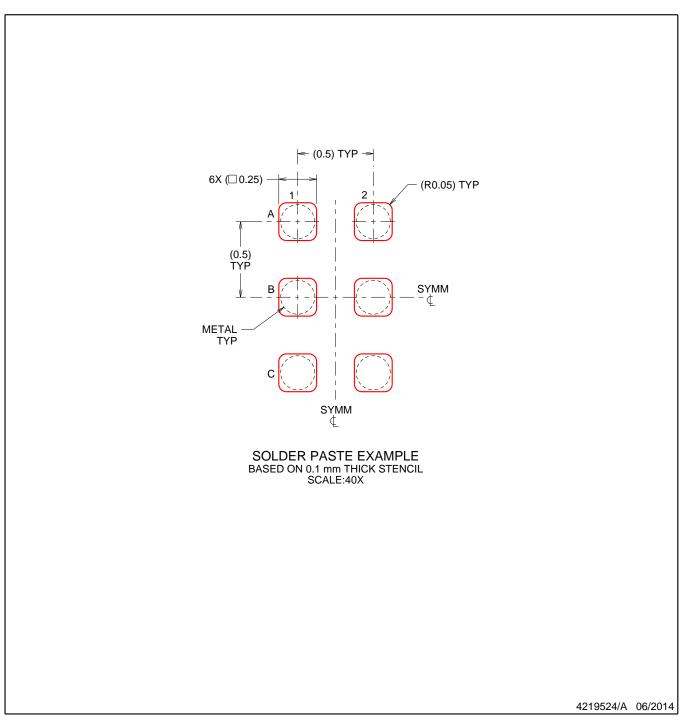


NOTES: (continued)

Final dimensions may vary due to manufacturing tolerance considerations and also routing constraints.
 For more information, see Texas Instruments literature number SBVA017 (www.ti.com/lit/sbva017).



DIE SIZE BALL GRID ARRAY



NOTES: (continued)

5. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release.



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Last updated 10/2025