TS5A3167 0.9Ω 1-channel 1:1 SPST Analog Switch

1 Features

- Isolation in powered-off mode, V_{cc} = 0
- Low on-state resistance (0.9Ω)
- Control inputs are 5.5V tolerant
- Low charge injection
- Low total harmonic distortion (THD)
- 1.65V to 5.5V single-supply operation
- Latch-up performance exceeds 100mA per JESD 78, Class II
- ESD performance tested per JESD 22
  - 2000V Human-Body Model (A114-B, Class II)
  - 1000V Charged-Device Model (C101)

2 Applications

- Cell phones
- PDAs
- Portable instrumentation
- Audio and video signal routing
- Low-voltage data-acquisition systems
- Communication circuits
- Modems
- Hard drives
- Computer peripherals
- Wireless terminals and peripherals
- Microphone switching
- Notebook docking

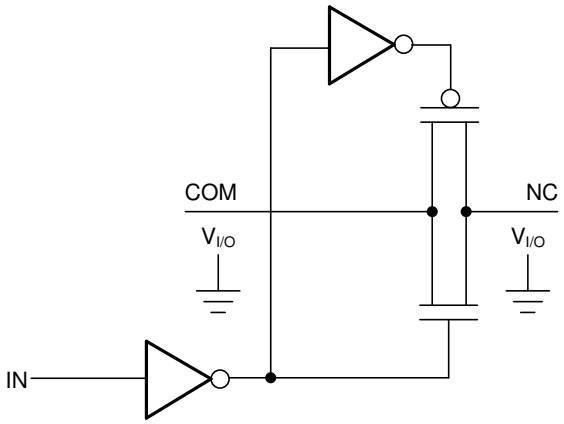
3 Description

The TS5A3167 is a bidirectional, single-channel, single-pole single-throw (SPST) analog switch that is designed to operate from 1.65V to 5.5V. The TS5A3167 device offers a low ON-state resistance. The device has excellent total harmonic distortion (THD) performance and consumes very low power. These features make this device correct for portable audio applications.

Package Information

PART NUMBER	PACKAGE(1)	PACKAGE SIZE(2)
TS5A3167	DBV (SOT-23, 5)	2.90mm x 1.60mm
	DCK (SOT-SC70, 5)	2.00mm x 1.25mm
	YZP (DSBGA, 5)	1.50mm x 0.90mm

(1) For all available packages, see Section Mechanical, Packaging, and Orderable Information.
(2) The package size (length × width) is a nominal value and includes pins, where applicable.



Simple Schematic

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4 Pin Configuration and Functions

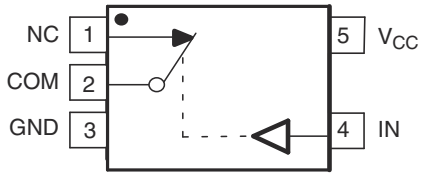


Figure 4-1. DBV or DCK Package 5- Pin (SOT-23 or SC70) Top View

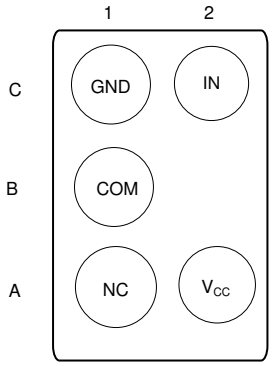


Figure 4-2. YZP Package 5-Pin (DSBGA) Bottom View

PIN		DESCRIPTION
NAME	NO.	
NC	1	Normally Closed
COM	2	Common
GND	3	Ground
IN	4	Digital control pin, COM connected to NC when logic low
V_{CC}	5	Power Supply
NC	A1	Normally Closed
COM	B1	Common
GND	C1	Ground
V_{CC}	A2	Power Supply
IN	C2	Digital control pin, COM connected to NC when logic low

5 Specifications

5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1) (2)

			MIN	MAX	UNIT
Supply voltage range(3)		V_{CC}	–0.5	6.5	V
Analog voltage range(3) (4) (5)		V_{NC} V_{COM}	–0.5	V_{CC} + 0.5	V
Analog port diode current	V_{NC}, V_{COM} < 0	I_K	–50		mA
On-state switch current	V_{NC}, V_{COM} = 0 to V_{CC}	I_{NC} I_{COM}	–200	200	mA
On-state peak switch current(6)			–400	400	
Digital input voltage range(3) (4)		V_I	–0.5	6.5	V
Digital clamp current	V_I < 0	I_{IK}	–50		mA
Continuous current through V_{CC}		I_{CC}		100	mA
Continuous current through GND		I_{GND}	–100		mA
Storage temperature range		T_{stg}	–65	150	°C

(1) Operation outside the *Absolute Maximum Ratings* may cause permanent device damage. *Absolute Maximum Ratings* do not imply functional operation of the device at these or any other conditions beyond those listed under *Recommended Operating Conditions*. If used outside the *Recommended Operating Conditions* but within the *Absolute Maximum Ratings*, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.
(2) The algebraic convention, whereby the most negative value is a minimum and the most positive value is a maximum.
(3) All voltages are with respect to ground, unless otherwise specified.
(4) The input and output voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
(5) This value is limited to 5.5V maximum.
(6) Pulse at 1ms duration < 10% duty cycle.

5.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±2000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101(2)	±1000	

(1) JEDEC document JEP155 states that 500V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250V CDM allows safe manufacturing with a standard ESD control process.

5.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
V_{CC}	Supply voltage range	1.65	5.5	V
V_{NC} V_{COM}	Analog voltage range	0	V_{CC}	V
V_I	Digital input voltage range	0	V_{CC}	V

5.4 Thermal Information

THERMAL METRIC(1)		TS5A3167			UNIT
		DBV (SOT-23)	DCK (SOT-23)	YZP (DSBGA)	
		5 PINS	5 PINS	5 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	230.3	268.0	146.2	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	111.9	171.8	1.4	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	69.5	64.5	39.3	°C/W
ψ_{JT}	Junction-to-top characterization parameter	33.0	40.5	0.7	°C/W

THERMAL METRIC(1)		TS5A3167			UNIT
		DBV (SOT-23)	DCK (SOT-23)	YZP (DSBGA)	
		5 PINS	5 PINS	5 PINS	
ψ_{JB}	Junction-to-board characterization parameter	69.0	62.9	39.8	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	N/A	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application note.

5.5 Electrical Characteristics for 5V Supply

V_{CC} = 4.5V to 5.5V, T_A = –40°C to 85°C (unless otherwise noted)(1)

PARAMETER		TEST CONDITIONS		T_A	V_{CC}	MIN	TYP	MAX	UNIT
ANALOG SWITCH									
r_{peak}	Peak ON resistance	0 ≤ V_{NC} ≤ V_{CC}, I_{COM} = –100mA	Switch ON, See Figure 6-1	25°C	4.5V		0.8	1.1	Ω
				Full				1.2	
r_{on}	ON-state resistance	V_{NC} = 2.5V, I_{COM} = –100mA	Switch ON, See Figure 6-1	25°C	4.5V		0.75	0.9	Ω
				Full				1	
$r_{on(flat)}$	ON-state resistance flatness	0 ≤ V_{NC} ≤ V_{CC}, I_{COM} = –100mA	Switch ON, See Figure 6-1	25°C	4.5V		0.2		Ω
		V_{NC} = 1V, 1.5V, 2.5V, I_{COM} = –100mA		25°C			0.15	0.25	
				Full				0.25	
$I_{NC(OFF)}$ $I_{NC(PWROFF)}$	NC OFF leakage current	V_{NC} = 1V, V_{COM} = 4.5V, or V_{NC} = 4.5V, V_{COM} = 1V,	Switch OFF, See Figure 6-2	25°C	5.5V	0	4	20	nA
				Full		–150		150	
		V_{NC} = 0 to 5.5V, V_{COM} = 5.5V to 0		25°C	0V	–10	0.2	10	µA
				Full		–50		50	
$I_{COM(OFF)}$ $I_{COM(PWROFF)}$	COM OFF leakage current	V_{COM} = 1V, V_{NC} = 4.5V, or V_{COM} = 4.5V, V_{NC} = 1V	Switch OFF, See Figure 6-2	25°C	5.5V	0	4	20	nA
				Full		–150		150	
		V_{COM} = 5.5V to 0, V_{NC} = 0 to 5.5V		25°C	0V	–10	0.2	10	µA
				Full		–50		50	
$I_{NC(ON)}$	NC ON leakage current	V_{NC} = 1V, V_{COM} = Open, or V_{NC} = 4.5V, V_{COM} = Open	Switch ON, See Figure 6-3	25°C	5.5V	–5	0.4	5	nA
				Full		–50		50	
$I_{COM(ON)}$	COM ON leakage current	V_{COM} = 1V, V_{NC} = Open, or V_{COM} = 4.5V, V_{NC} = Open	Switch ON, See Figure 6-3	25°C	5.5V	–5	0.4	5	nA
				Full		–20		20	
DIGITAL CONTROL INPUTS (IN)									
V_{IH}	Input logic high			Full		2.4		5.5	V
V_{IL}	Input logic low			Full		0		0.8	V
I_{IH}, I_{IL}	Input leakage current	V_I = 5.5V or 0		25°C	5.5V	–2	0.3	2	nA
				Full		–20		20	
DYNAMIC									
t_{ON}	Turn-on time	V_{COM} = V_{CC}, R_L = 50Ω	C_L = 35pF, See Figure 6-5	25°C	5V	1	4.5	7.5	ns
				Full	4.5V to 5.5V	1		9	

V_{CC} = 4.5V to 5.5V, T_A = –40°C to 85°C (unless otherwise noted)(1)

PARAMETER		TEST CONDITIONS		T_A	V_{CC}	MIN	TYP	MAX	UNIT
t_{OFF}	Turn-off time	V_{COM} = V_{CC}, R_L = 50Ω	C_L = 35pF, See Figure 6-5	25°C	5V	4.5	8	11	ns
				Full	4.5V to 5.5V	3.5		13	
Q_C	Charge injection	V_{GEN} = 0, R_{GEN} = 0	C_L = 1nF, See Figure 6-8	25°C	5V		6		pC
$C_{NC(OFF)}$	NC OFF capacitance	V_{NC} = V_{CC} or GND	Switch OFF, See Figure 6-4	25°C	5V		19		pF
$C_{COM(OFF)}$	COM OFF capacitance	V_{COM} = V_{CC} or GND	Switch OFF, See Figure 6-4	25°C	5V		18		pF
$C_{NC(ON)}$	NC ON capacitance	V_{NC} = V_{CC} or GND	Switch ON, See Figure 6-4	25°C	5V		35.5		pF
$C_{COM(ON)}$	COM ON capacitance	V_{COM} = V_{CC} or GND	Switch ON, See Figure 6-4	25°C	5V		35.5		pF
C_I	Digital input capacitance	V_I = V_{CC} or GND	See Figure 6-4	25°C	5V		2		pF
BW	Bandwidth	R_L = 50Ω	Switch ON, See Figure 6-6	25°C	5V		150		MHz
O_{ISO}	OFF isolation	R_L = 50Ω, f = 1MHz	Switch OFF, See Figure 6-7	25°C	5V		–62		dB
THD	Total harmonic distortion	R_L = 600Ω, C_L = 50pF	f = 20Hz to 20kHz, See Figure 6-9	25°C	5V		0.005 %		
SUPPLY									
I_{CC}	Positive supply current	V_I = V_{CC} or GND	Switch ON or OFF	25°C	5.5V		0.01	0.1	μA
				Full				1	

(1) The algebraic convention, whereby the most negative value is a minimum and the most positive value is a maximum.

5.6 Electrical Characteristics for 3.3V Supply

V_{CC} = 3V to 3.6V, T_A = –40°C to 85°C (unless otherwise noted)(1)

PARAMETER		TEST CONDITIONS		T_A	V_{CC}	MIN	TYP	MAX	UNIT
ANALOG SWITCH									
r_{peak}	Peak ON resistance	0 ≤ V_{NC} ≤ V_{CC}, I_{COM} = –100mA	Switch ON, See Figure 6-1	25°C	3V		1.3	1.6	Ω
				Full				1.8	
r_{on}	ON-state resistance	V_{NC} = 2V, I_{COM} = –100mA	Switch ON, See Figure 6-1	25°C	3V		1.1	1.5	Ω
				Full				1.7	
$r_{on(flat)}$	ON-state resistance flatness	0 ≤ V_{NC} ≤ V_{CC}, I_{COM} = –100mA	Switch ON, See Figure 6-1	25°C	3V		0.3		Ω
		V_{NC} = 2V, 0.8V, I_{COM} = –100mA		25°C			0.15	0.25	
				Full				0.25	
$I_{NC(OFF)}$	NC OFF leakage current	V_{NC} = 1V, V_{COM} = 3V, or V_{NC} = 3V, V_{COM} = 1V	Switch OFF, See Figure 6-2	25°C	3.6V	–5	0.5	5	nA
				Full		–50		50	
$I_{NC(PWROFF)}$		V_{NC} = 0 to 3.6V, V_{COM} = 3.6V to 0		25°C	0V	–5	0.1	5	μA
				Full		–25		25	
$I_{COM(OFF)}$	COM OFF leakage current	V_{COM} = 1V, V_{NC} = 3V, or V_{COM} = 3V, V_{NC} = 1V	Switch OFF, See Figure 6-2	25°C	3.6V	–5	0.5	5	nA
				Full		–50		50	
$I_{COM(PWROFF)}$		V_{COM} = 3.6V to 0, V_{NC} = 0 to 3.6V		25°C	0V	–5	0.1	5	μA
				Full		–25		25	

V_{CC} = 3V to 3.6V, T_A = –40°C to 85°C (unless otherwise noted)(1)

PARAMETER		TEST CONDITIONS		T_A	V_{CC}	MIN	TYP	MAX	UNIT
$I_{NC(ON)}$	NC ON leakage current	V_{NC} = 1V, V_{COM} = Open, or V_{NC} = 3V, V_{COM} = Open	Switch ON, See Figure 6-3	25°C	3.6V	–2	0.3	2	nA
				Full		–20		20	
$I_{COM(ON)}$	COM ON leakage current	V_{COM} = 1V, V_{NC} = Open, or V_{COM} = 3V, V_{NC} = Open	Switch ON, See Figure 6-3	25°C	3.6V	–2	0.3	2	nA
				Full		–20		20	
DIGITAL CONTROL INPUTS (IN)									
V_{IH}	Input logic high			Full		2		5.5	V
V_{IL}	Input logic low			Full		0		0.8	V
I_{IH}, I_{IL}	Input leakage current	V_I = 5.5V or 0		25°C	3.6V	–2	0.3	2	nA
				Full		–20		20	
DYNAMIC									
t_{ON}	Turn-on time	V_{COM} = V_{CC}, R_L = 50Ω	C_L = 35pF, See Figure 6-5	25°C	3.3V	1.5	5	9.5	ns
				Full	3V to 3.6V	1.0		10	
t_{OFF}	Turn-off time	V_{COM} = V_{CC}, R_L = 50Ω	C_L = 35pF, See Figure 6-5	25°C	3.3V	4.5	8.5	11	ns
				Full	3V to 3.6V	3		12.5	
Q_C	Charge injection	V_{GEN} = 0, R_{GEN} = 0	C_L = 1nF, See Figure 6-8	25°C	3.3V		6		pC
$C_{NC(OFF)}$	NC OFF capacitance	V_{NC} = V_{CC} or GND	Switch OFF, See Figure 6-4	25°C	3.3V		19.5		pF
$C_{COM(OFF)}$	COM OFF capacitance	V_{COM} = V_{CC} or GND	Switch OFF, See Figure 6-4	25°C	3.3V		18.5		pF
$C_{NC(ON)}$	NC ON capacitance	V_{NC} = V_{CC} or GND	Switch ON, See Figure 6-4	25°C	3.3V		36		pF
$C_{COM(ON)}$	COM ON capacitance	V_{COM} = V_{CC} or GND	Switch ON, See Figure 6-4	25°C	3.3V		36		pF
C_I	Digital input capacitance	V_I = V_{CC} or GND	See Figure 6-4	25°C	3.3V		2		pF
BW	Bandwidth	R_L = 50Ω	Switch ON, See Figure 6-6	25°C	3.3V		150		MHz
O_{ISO}	OFF isolation	R_L = 50Ω, f = 1MHz	Switch OFF, See Figure 6-7	25°C	3.3V		–62		dB
THD	Total harmonic distortion	R_L = 600Ω, C_L = 50pF	f = 20Hz to 20kHz, See Figure 6-9	25°C	3.3V		0.01%		
SUPPLY									
I_{CC}	Positive supply current	V_I = V_{CC} or GND	Switch ON or OFF	25°C	3.6V		0.001	0.05	µA
				Full				0.3	

(1) The algebraic convention, whereby the most negative value is a minimum and the most positive value is a maximum.

5.7 Electrical Characteristics for 2.5V Supply

V_{CC} = 2.3V to 2.7V, T_A = –40°C to 85°C (unless otherwise noted)(1)

PARAMETER		TEST CONDITIONS		T_A	V_{CC}	MIN	TYP	MAX	UNIT
ANALOG SWITCH									
r_{peak}	Peak ON resistance	0 ≤ V_{NC} ≤ V_{CC}, I_{COM} = –100mA	Switch ON, See Figure 6-1	25°C	2.3V		1.8	2.4	Ω
				Full				2.6	
r_{on}	ON-state resistance	V_{NC} = 2V, I_{COM} = –100mA	Switch ON, See Figure 6-1	25°C	2.3V		1.2	2.1	Ω
				Full				2.4	

V_{CC} = 2.3V to 2.7V, T_A = –40°C to 85°C (unless otherwise noted)(1)

PARAMETER		TEST CONDITIONS		T_A	V_{CC}	MIN	TYP	MAX	UNIT
$r_{on(flat)}$	ON-state resistance flatness	0 ≤ V_{NC} ≤ V_{CC}, I_{COM} = –100mA	Switch ON, See Figure 6-1	25°C	2.3V		0.7		Ω
		V_{NC} = 2V, 0.8V, I_{COM} = –100mA		25°C			0.4	0.6	
				Full				0.6	
$I_{NC(OFF)}$	NC OFF leakage current	V_{NC} = 1V, V_{COM} = 3V, or V_{NC} = 3V, V_{COM} = 1V	Switch OFF, See Figure 6-2	25°C	2.7V	–5	0.3	5	nA
				Full		–50		50	
$I_{NC(PWROFF)}$		V_{NC} = 0 to 3.6V, V_{COM} = 3.6V to 0		25°C	0V	–2	0.05	2	µA
				Full		–15		15	
$I_{COM(OFF)}$	COM OFF leakage current	V_{COM} = 1V, V_{NC} = 3V, or V_{COM} = 3V, V_{NC} = 1V	Switch OFF, See Figure 6-2	25°C	2.7V	–5	0.3	5	nA
				Full		–50		50	
$I_{COM(PWROFF)}$		V_{COM} = 3.6V to 0, V_{NC} = 0 to 3.6V		25°C	0V	–2	0.05	2	µA
				Full		–15		15	
$I_{NC(ON)}$	NC ON leakage current	V_{NC} = 1V, V_{COM} = Open, or V_{NC} = 3V, V_{COM} = Open	Switch ON, See Figure 6-3	25°C	2.7V	–2	0.3	2	nA
				Full		–20		20	
$I_{COM(ON)}$	COM ON leakage current	V_{COM} = 1V, V_{NC} = Open, or V_{COM} = 3V, V_{NC} = Open	Switch ON, See Figure 6-3	25°C	2.7V	–2	0.3	2	nA
				Full		–20		20	
DIGITAL CONTROL INPUTS (IN)									
V_{IH}	Input logic high			Full		1.8		5.5	V
V_{IL}	Input logic low			Full		0		0.6	V
I_{IH}, I_{IL}	Input leakage current	V_I = 5.5V or 0		25°C	2.7V	–2	0.3	2	nA
				Full		–20		20	
DYNAMIC									
t_{ON}	Turn-on time	V_{COM} = V_{CC}, R_L = 50Ω	C_L = 35pF, See Figure 6-5	25°C	2.5V	2	6	10	ns
				Full	2.3V to 2.7V	1		12	
t_{OFF}	Turn-off time	V_{COM} = V_{CC}, R_L = 50Ω	C_L = 35pF, See Figure 6-5	25°C	2.5V	4.5	8	10.5	ns
				Full	2.3V to 2.7V	3		15	
Q_C	Charge injection	V_{GEN} = 0, R_{GEN} = 0	C_L = 1nF, See Figure 6-8	25°C	2.5V		4		pC
$C_{NC(OFF)}$	NC OFF capacitance	V_{NC} = V_{CC} or GND	Switch OFF, See Figure 6-4	25°C	2.5V		19.5		pF
$C_{COM(OFF)}$	COM OFF capacitance	V_{COM} = V_{CC} or GND	Switch OFF, See Figure 6-4	25°C	2.5V		18.5		pF
$C_{NC(ON)}$	NC ON capacitance	V_{NC} = V_{CC} or GND	Switch ON, See Figure 6-4	25°C	2.5V		36.5		pF
$C_{COM(ON)}$	COM ON capacitance	V_{COM} = V_{CC} or GND	Switch ON, See Figure 6-4	25°C	2.5V		36.5		pF
C_I	Digital input capacitance	V_I = V_{CC} or GND	See Figure 6-4	25°C	2.5V		2		pF
BW	Bandwidth	R_L = 50Ω	Switch ON, See Figure 6-6	25°C	2.5V		150		MHz
O_{ISO}	OFF isolation	R_L = 50Ω, f = 1MHz	Switch OFF, See Figure 6-7	25°C	2.5V		–62		dB

V_{CC} = 2.3V to 2.7V, T_A = –40°C to 85°C (unless otherwise noted)(1)

PARAMETER		TEST CONDITIONS		T_A	V_{CC}	MIN	TYP	MAX	UNIT
THD	Total harmonic distortion	R_L = 600Ω, C_L = 50pF	f = 20Hz to 20kHz, See Figure 6-9	25°C	2.5V		0.02%		
SUPPLY									
I_{CC}	Positive supply current	V_I = V_{CC} or GND	Switch ON or OFF	25°C	2.7V		0.001	0.02	μA
				Full				0.25	

(1) The algebraic convention, whereby the most negative value is a minimum and the most positive value is a maximum.

5.8 Electrical Characteristics for 1.8V Supply

V_{CC} = 1.65V to 1.95V, T_A = –40°C to 85°C (unless otherwise noted)(1)

PARAMETER		TEST CONDITIONS		T_A	V_{CC}	MIN	TYP	MAX	UNIT
ANALOG SWITCH									
r_{peak}	Peak ON resistance	0 ≤ V_{NC} ≤ V_{CC}, I_{COM} = –100mA	Switch ON, See Figure 6-1	25°C	1.65V		4.2	25	Ω
				Full				30	
r_{on}	ON-state resistance	V_{NC} = 2V, I_{COM} = –100mA	Switch ON, See Figure 6-1	25°C	1.65V		1.6	3.9	Ω
				Full				4.0	
$r_{on(flat)}$	ON-state resistance flatness	0 ≤ V_{NC} ≤ V_{CC}, I_{COM} = –100mA	Switch ON, See Figure 6-1	25°C	1.65V		2.8		Ω
		V_{NC} = 2V, 0.8V, I_{COM} = –100mA		25°C			4.1	22	
				Full				27	
$I_{NC(OFF)}$	NC OFF leakage current	V_{NC} = 1V, V_{COM} = 3V, or V_{NC} = 3V, V_{COM} = 1V	Switch OFF, See Figure 6-2	25°C	1.95V	–5		5	nA
				Full		–50		50	
$I_{NC(PWROFF)}$		V_{NC} = 0 to 3.6V, V_{COM} = 3.6V to 0		25°C	0V	–2		2	μA
				Full		–10		10	
$I_{COM(OFF)}$	COM OFF leakage current	V_{COM} = 1V, V_{NC} = 3V, or V_{COM} = 3V, V_{NC} = 1V	Switch OFF, See Figure 6-2	25°C	1.95V	–5		5	nA
				Full		–50		50	
$I_{COM(PWROFF)}$		V_{COM} = 0 to 3.6V, V_{NC} = 3.6V to 0		25°C	0V	–2		2	μA
				Full		–10		10	
$I_{NC(ON)}$	NC ON leakage current	V_{NC} = 1V, V_{COM} = Open, or V_{NC} = 3V, V_{COM} = Open	Switch ON, See Figure 6-3	25°C	1.95V	–2		2	nA
				Full		–20		20	
$I_{COM(ON)}$	COM ON leakage current	V_{COM} = 1V, V_{NC} = Open, or V_{COM} = 3V, V_{NC} = Open	Switch ON, See Figure 6-3	25°C	1.95V	–2		2	nA
				Full		–20		20	
DIGITAL CONTROL INPUTS (IN)									
V_{IH}	Input logic high			Full		1.5		5.5	V
V_{IL}	Input logic low			Full		0		0.6	V
I_{IH}, I_{IL}	Input leakage current	V_I = 5.5V or 0		25°C	1.95V	–2	0.3	2	nA
				Full		–20		20	
DYNAMIC									
t_{ON}	Turn-on time	V_{COM} = V_{CC}, R_L = 50Ω	C_L = 35pF, See Figure 6-5	25°C	1.8V	3	9	18	ns
				Full	1.65V to 1.95V	1		20	

V_{CC} = 1.65V to 1.95V, T_A = –40°C to 85°C (unless otherwise noted)(1)

PARAMETER		TEST CONDITIONS		T_A	V_{CC}	MIN	TYP	MAX	UNIT
t_{OFF}	Turn-off time	V_{COM} = V_{CC}, R_L = 50Ω	C_L = 35pF, See Figure 6-5	25°C	1.8V	5	10	15.5	ns
				Full	1.65V to 1.95V	4		18.5	
Q_C	Charge injection	V_{GEN} = 0, R_{GEN} = 0	C_L = 1nF, See Figure 6-8	25°C	1.8V		2		pC
$C_{NC(OFF)}$	NC OFF capacitance	V_{NC} = V_{CC} or GND	Switch OFF, See Figure 6-4	25°C	1.8V		19.5		pF
$C_{COM(OFF)}$	COM OFF capacitance	V_{COM} = V_{CC} or GND	Switch OFF, See Figure 6-4	25°C	1.8V		18.5		pF
$C_{NC(ON)}$	NC ON capacitance	V_{NC} = V_{CC} or GND	Switch ON, See Figure 6-4	25°C	1.8V		36.5		pF
$C_{COM(ON)}$	COM ON capacitance	V_{COM} = V_{CC} or GND	Switch ON, See Figure 6-4	25°C	1.8V		36.5		pF
C_I	Digital input capacitance	V_I = V_{CC} or GND	See Figure 6-4	25°C	1.8V		2		pF
BW	Bandwidth	R_L = 50Ω	Switch ON, See Figure 6-6	25°C	1.8V		150		MHz
O_{ISO}	OFF isolation	R_L = 50Ω, f = 1MHz	Switch OFF, See Figure 6-7	25°C	1.8V		–62		dB
THD	Total harmonic distortion	R_L = 600Ω, C_L = 50pF	f = 20Hz to 20kHz, See Figure 6-9	25°C	1.8V		0.055 %		
SUPPLY									
I_{CC}	Positive supply current	V_I = V_{CC} or GND	Switch ON or OFF	25°C	1.95V		0.001	0.01	μA
				Full				0.15	

(1) The algebraic convention, whereby the most negative value is a minimum and the most positive value is a maximum.

5.9 Typical Characteristics

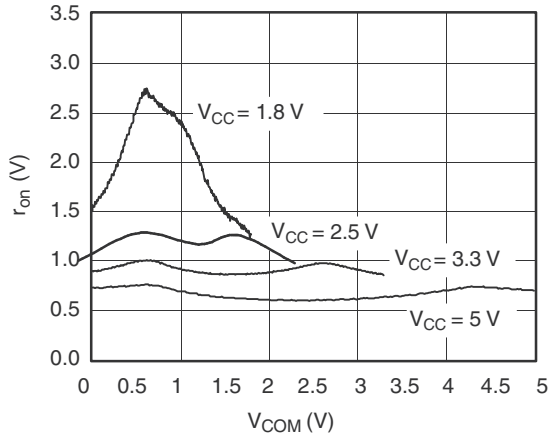


Figure 5-1. r_{on} vs V_{COM}

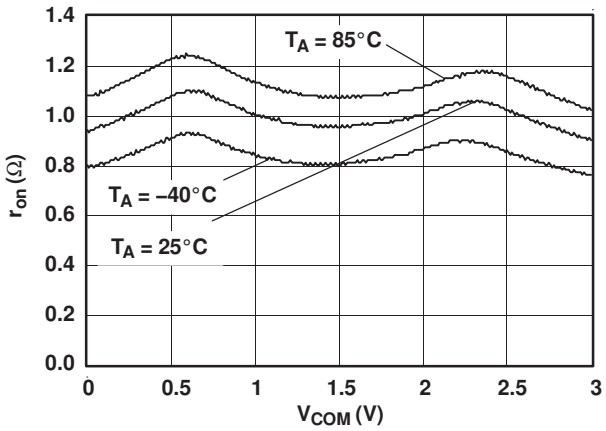


Figure 5-2. r_{on} vs V_{COM} (V_{CC} = 3V)

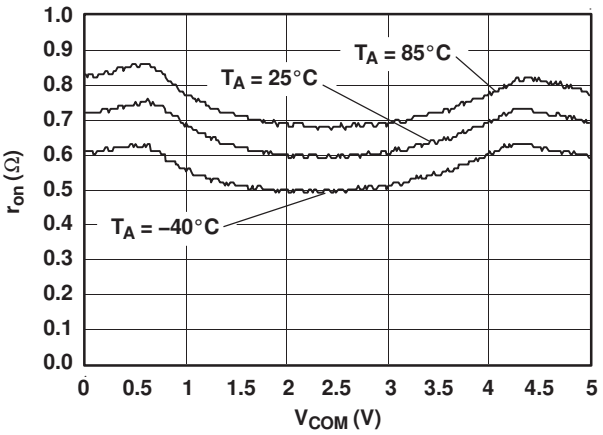


Figure 5-3. r_{on} vs V_{COM} (V_{CC} = 5V)

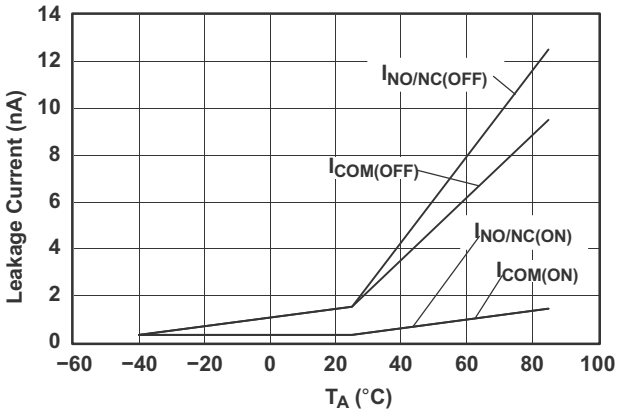


Figure 5-4. Leakage Current vs Temperature (V_{CC} = 5.5V)

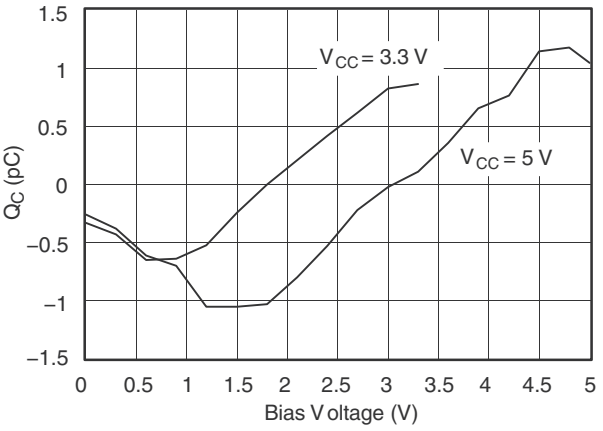


Figure 5-5. Charge Injection (Q_C) vs V_{COM}

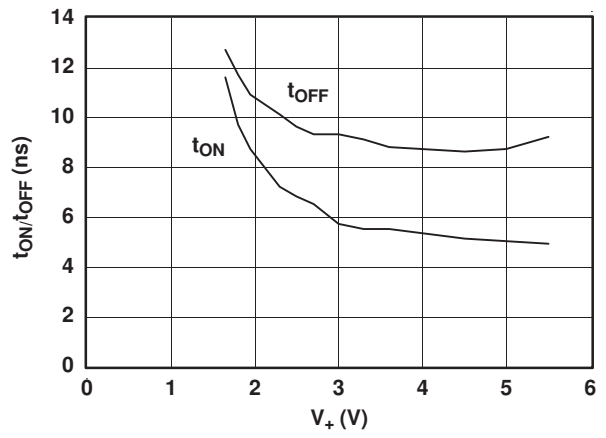


Figure 5-6. t_{ON} and t_{OFF} vs Supply Voltage

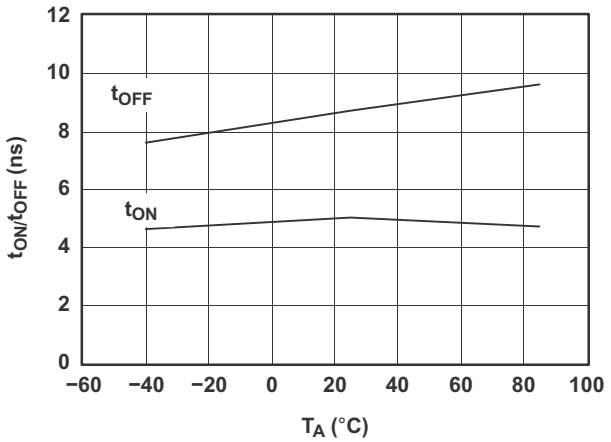


Figure 5-7. t_{ON} and t_{OFF} vs Temperature (V_{CC} = 5V)

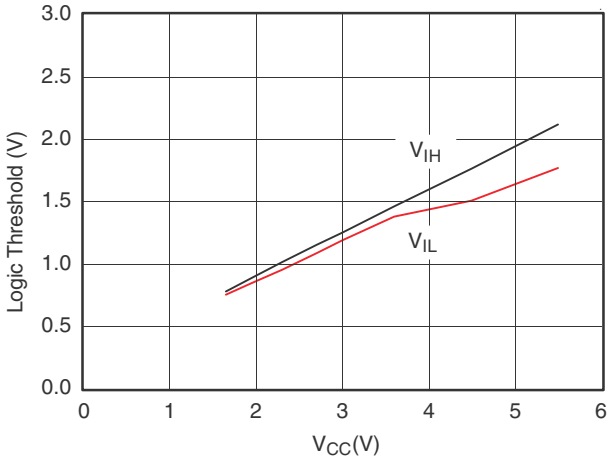


Figure 5-8. Logic Threshold vs V_{CC}

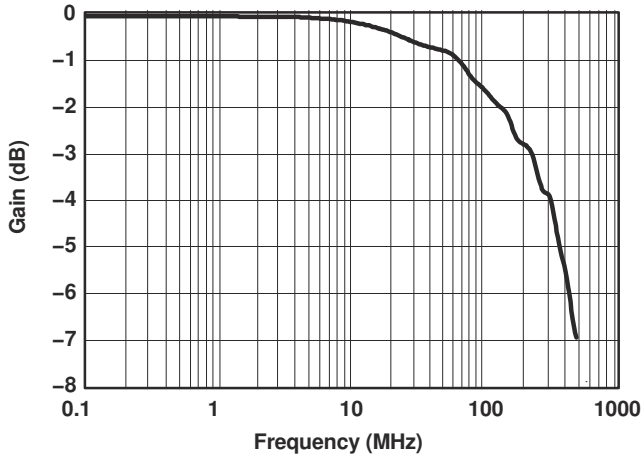


Figure 5-9. Gain vs Frequency (V_{CC} = 5V)

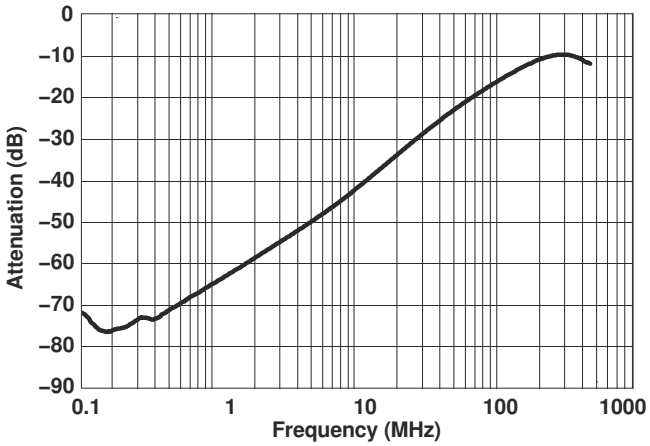


Figure 5-10. OFF Isolation vs Frequency (V_{CC} = 5V)

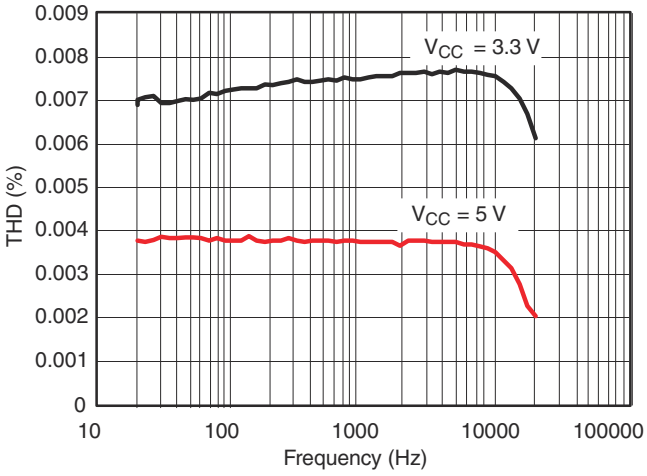


Figure 5-11. Total Harmonic Distortion vs Frequency (V_{CC} = 5V)

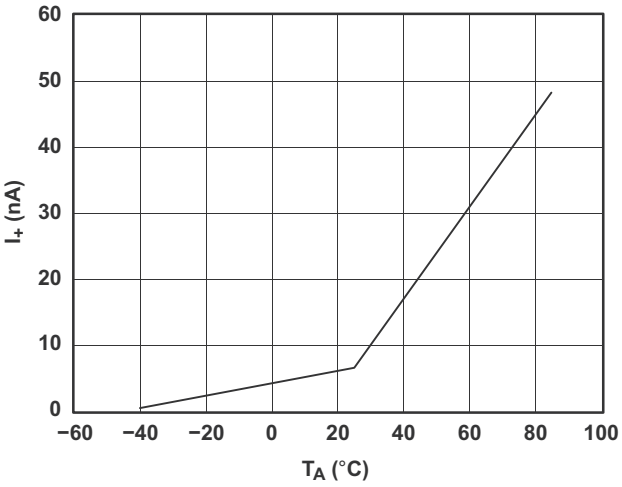


Figure 5-12. Power-Supply Current vs Temperature (V_{CC} = 5V)

6 Parameter Measurement Information

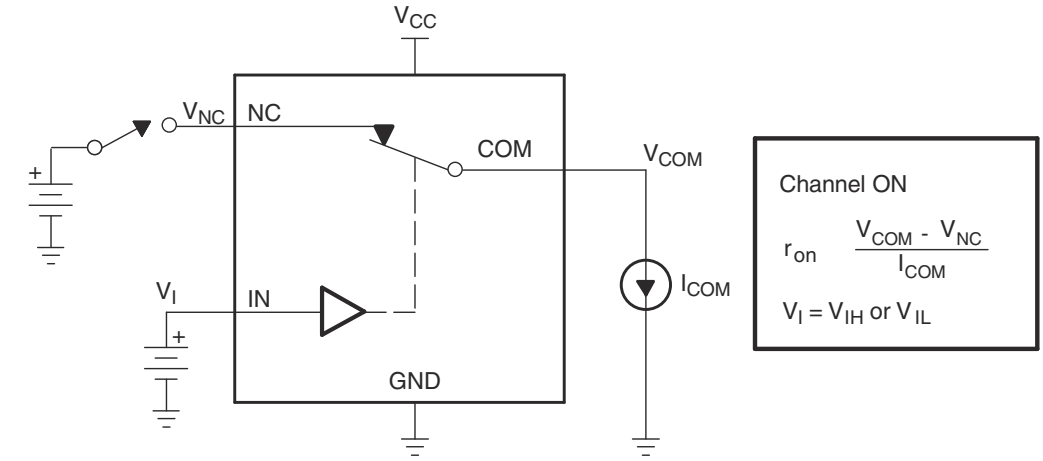


Figure 6-1. ON-State Resistance (r_{on})

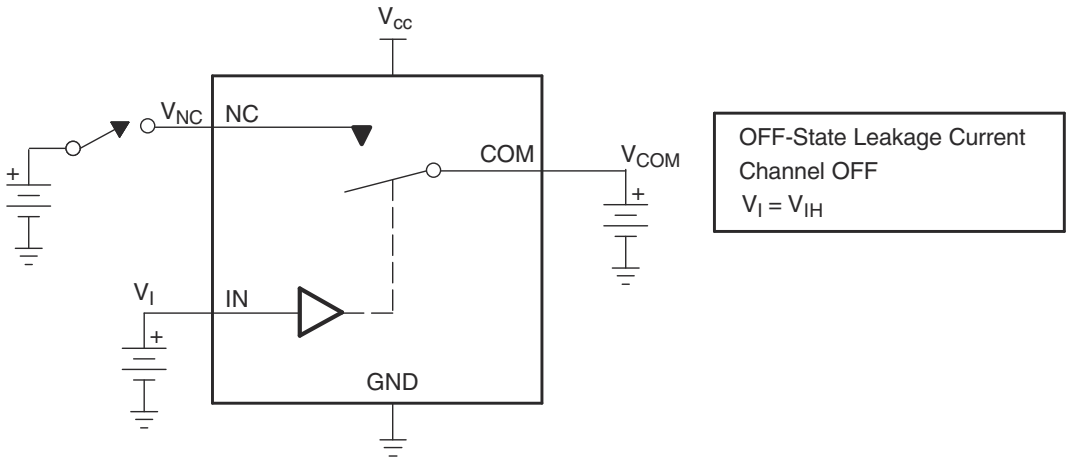


Figure 6-2. OFF-State Leakage Current ($I_{COM(OFF)}$, $I_{NC(OFF)}$, $I_{COM(PWROFF)}$, $I_{NC(PWROFF)}$)

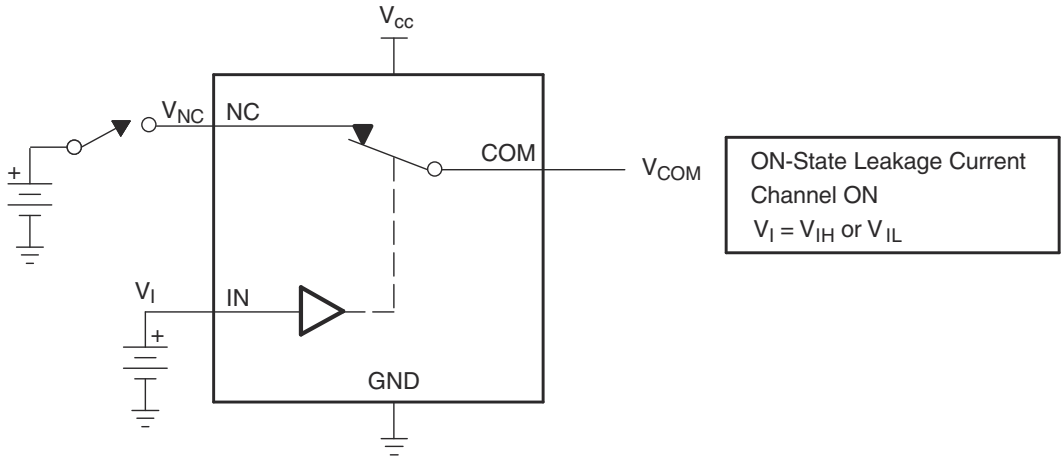


Figure 6-3. ON-State Leakage Current ($I_{COM(ON)}$, $I_{NC(ON)}$)

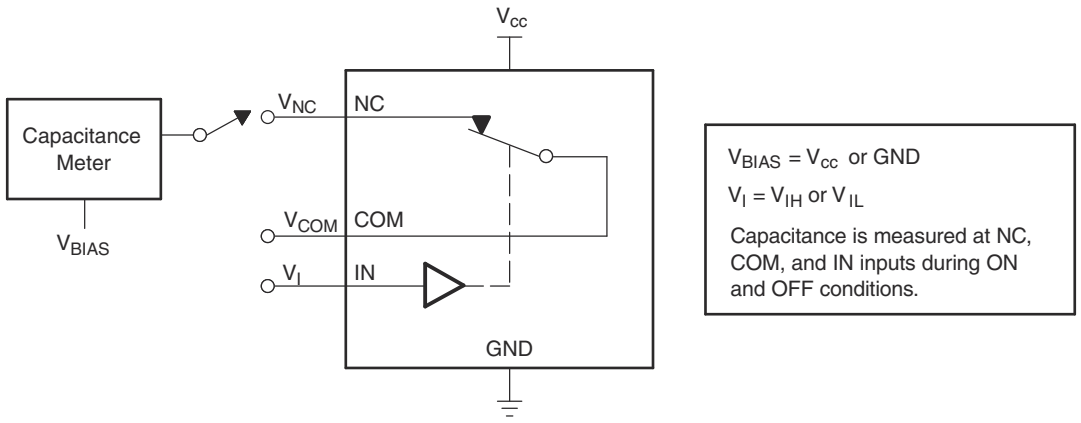
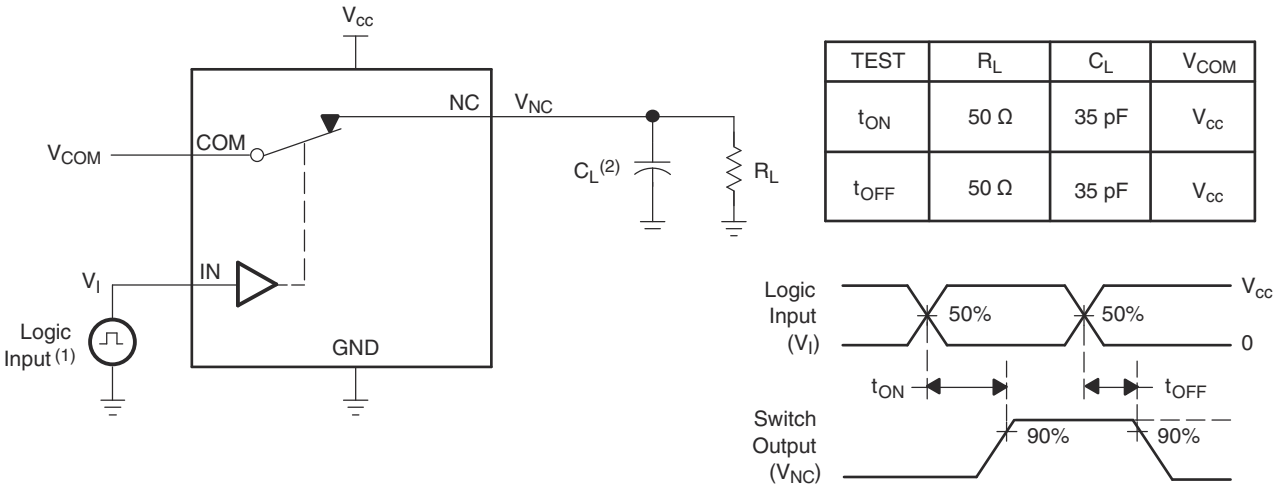


Figure 6-4. Capacitance (C_I, $C_{COM(OFF)}$, $C_{COM(ON)}$, $C_{NC(OFF)}$, $C_{NC(ON)}$)



A. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10MHz, Z_O = 50Ω, t_r < 5ns, t_f < 5ns.
B. C_L includes probe and jig capacitance.

Figure 6-5. Turn-On (t_{ON}) and Turn-Off Time (t_{OFF})

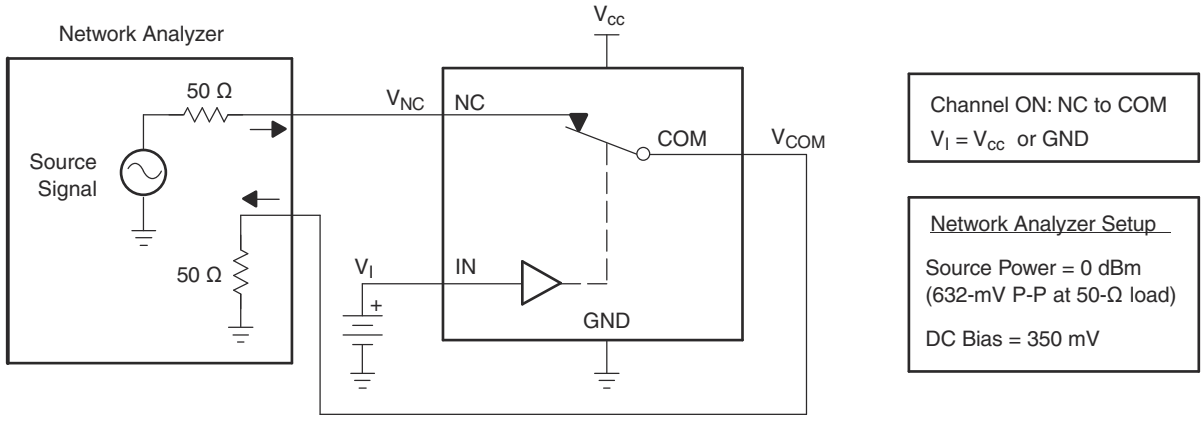


Figure 6-6. Bandwidth (BW)

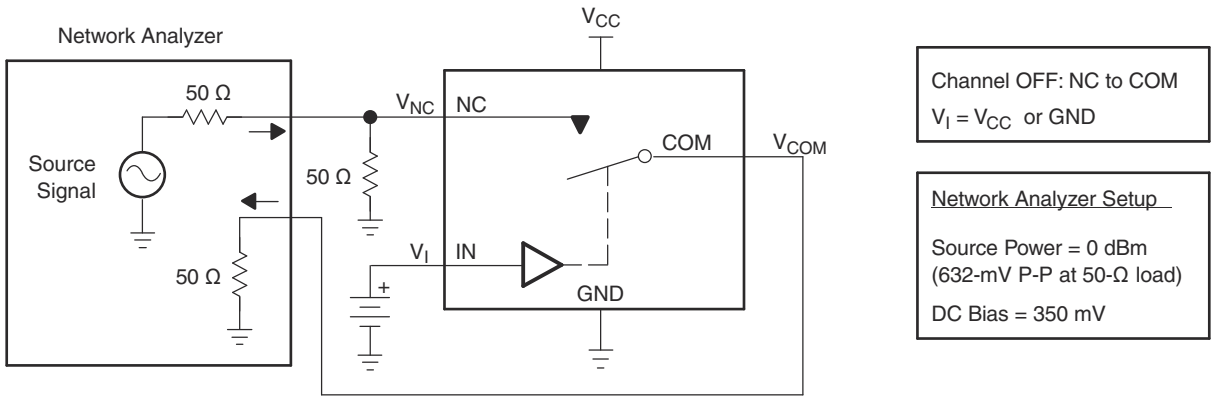
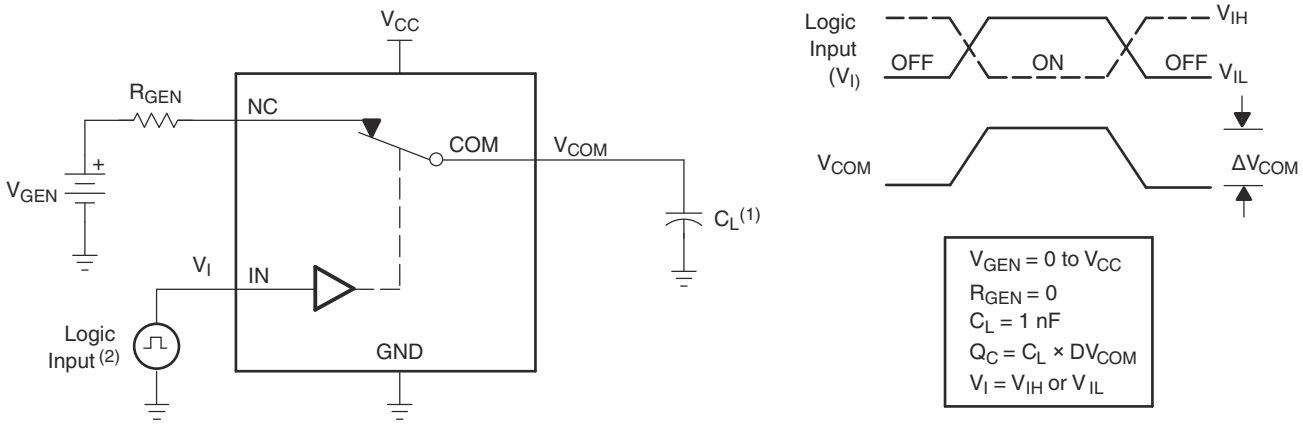


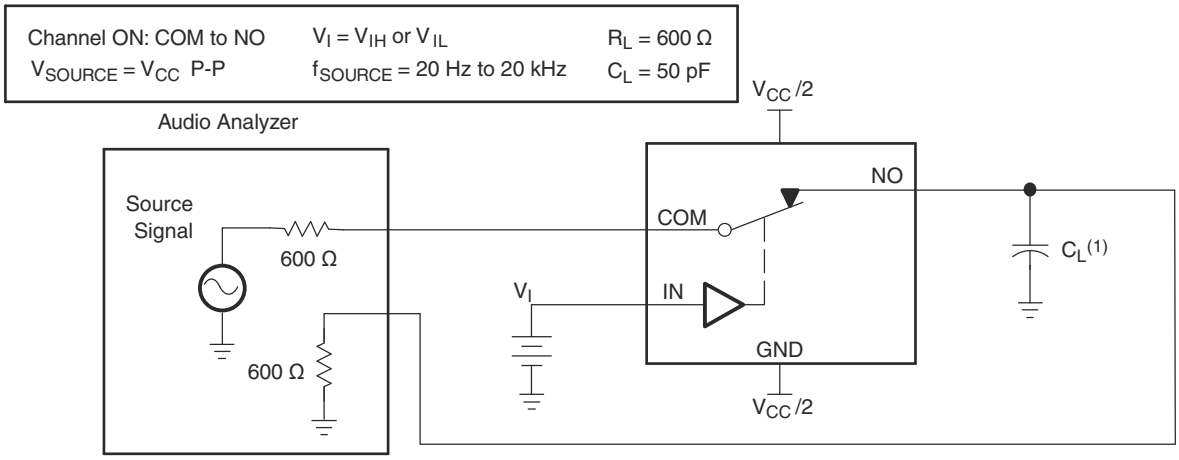
Figure 6-7. OFF Isolation (O_{ISO})



A. C_L includes probe and jig capacitance.

B. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10MHz, Z_O = 50Ω, t_r < 5ns, t_f < 5ns.

Figure 6-8. Charge Injection (Q_C)



A. C_L includes probe and jig capacitance.

Figure 6-9. Total Harmonic Distortion (THD)

Table 6-1. Parameter Description

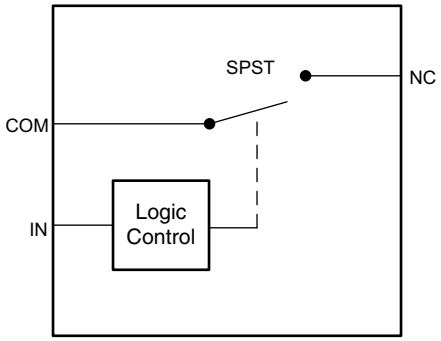
SYMBOL	DESCRIPTION
V_{COM}	Voltage at COM
V_{NC}	Voltage at NC
r_{on}	Resistance between COM and NC ports when the channel is ON
r_{peak}	Peak on-state resistance over a specified voltage range
$r_{on(flat)}$	Difference between the maximum and minimum value of r_{on} in a channel over the specified range of conditions
$I_{NC(OFF)}$	Leakage current measured at the NC port, with the corresponding channel (NC to COM) in the OFF state under worst-case input and output conditions
$I_{NC(PWROFF)}$	Leakage current measured at the NC port during the power-down condition, V_{CC} = 0
$I_{COM(OFF)}$	Leakage current measured at the COM port, with the corresponding channel (COM to NC) in the OFF state under worst-case input and output conditions
$I_{COM(PWROFF)}$	Leakage current measured at the COM port during the power-down condition, V_{CC} = 0
$I_{NC(ON)}$	Leakage current measured at the NC port, with the corresponding channel (NC to COM) in the ON state and the output (COM) open
$I_{COM(ON)}$	Leakage current measured at the COM port, with the corresponding channel (COM to NC) in the ON state and the output (NC) open
V_{IH}	Minimum input voltage for logic high for the control input (IN)
V_{IL}	Maximum input voltage for logic low for the control input (IN)
V_I	Voltage at the control input (IN)
I_{IH}, I_{IL}	Leakage current measured at the control input (IN)
t_{ON}	Turn-on time for the switch. This parameter is measured under the specified range of conditions and by the propagation delay between the digital control (IN) signal and analog output (COM or NC) signal when the switch is turning ON.
t_{OFF}	Turn-off time for the switch. This parameter is measured under the specified range of conditions and by the propagation delay between the digital control (IN) signal and analog output (COM or NC) signal when the switch is turning OFF.
Q_C	Charge injection is a measurement of unwanted signal coupling from the control (IN) input to the analog (NC or COM) output. This is measured in coulombs (C) and measured by the total charge induced due to switching of the control input. Charge injection, $Q_C = C_L \times \Delta V_{COM}$, C_L is the load capacitance, and ΔV_{COM} is the change in analog output voltage.
$C_{NC(OFF)}$	Capacitance at the NC port when the corresponding channel (NC to COM) is OFF
$C_{COM(OFF)}$	Capacitance at the COM port when the corresponding channel (COM to NC) is OFF
$C_{NC(ON)}$	Capacitance at the NC port when the corresponding channel (NC to COM) is ON
$C_{COM(ON)}$	Capacitance at the COM port when the corresponding channel (COM to NC) is ON
C_I	Capacitance of control input (IN)
O_{ISO}	OFF isolation of the switch is a measurement of OFF-state switch impedance. This is measured in dB in a specific frequency, with the corresponding channel (NC to COM) in the OFF state.
BW	Bandwidth of the switch. This is the frequency in which the gain of an ON channel is –3dB below the DC gain.
THD	Total harmonic distortion describes the signal distortion caused by the analog switch. This is defined as the ratio of root mean square (RMS) value of the second, third, and higher harmonic to the absolute magnitude of the fundamental harmonic.
I_{CC}	Static power-supply current with the control (IN) pin at V_{CC} or GND

7 Detailed Description

7.1 Overview

The TS5A3167 is a bidirectional, single-channel, single-pole single-throw (SPST) analog switch that is designed to operate from 1.65V to 5.5V. This device provides a signal switching solution while maintaining excellent signal integrity, which makes the TS5A3367 appropriate for a wide range of applications in various markets including personal electronics, portable instrumentation, and test and measurement equipment. The device maintains the signal integrity by its low ON-state resistance, excellent ON-state resistance matching, and total harmonic distortion (THD) performance. The device consumes very low power and provides isolation when VCC = 0.

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 Isolation in Powered-Off Mode, V_{CC} = 0

When power is not supplied to the V_{CC} pin, V_{CC} = 0, the signal paths NC and COM are high impedance. This is specified in the electrical characteristics table under the COM and NC OFF leakage current when V_{CC} = 0. Because the device is high impedance when it is not powered, other signals are connectable without interference of the TS5A3167.

7.4 Device Functional Modes

Placing a logic low signal on the IN pin of the device turns on the switch and provides a low impedance path from NC to COM.

Table 7-1. Functions

IN	NC TO COM, COM TO NC
L	ON
H	OFF

8 Application and Implementation

8.1 Application Information Disclaimer

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

8.2 Application Information

The TS5A3167 switch is bidirectional, so the NC and COM pins can be used as either inputs or outputs. This switch is typically used when there is one signal path that requires isolation at certain times.

8.3 Typical Application

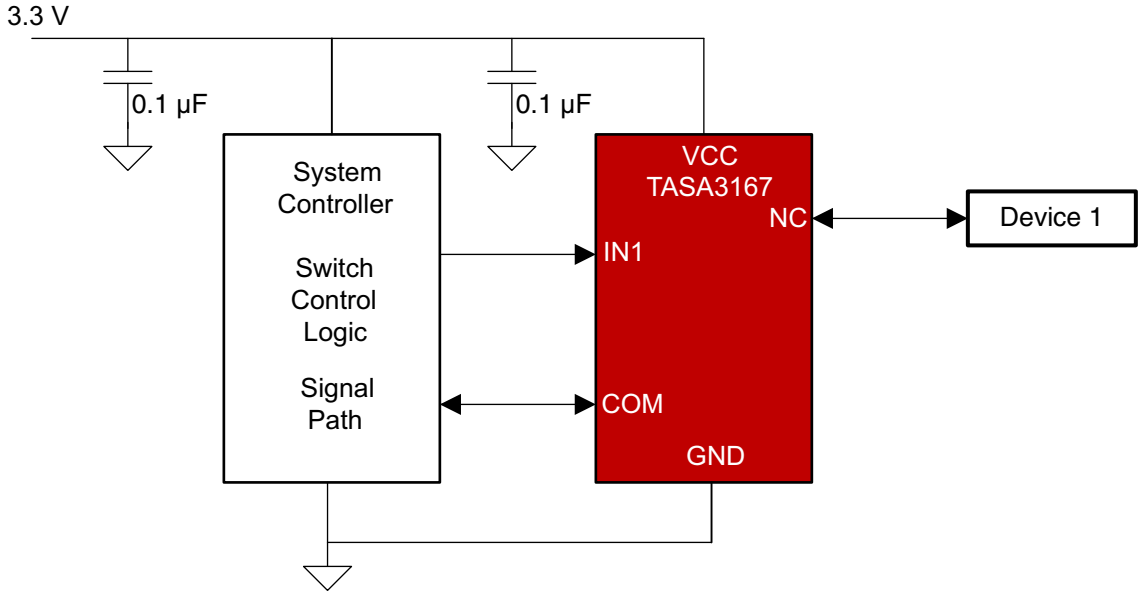


Figure 8-1. Typical Application

8.3.1 Design Requirements

The TS5A3167 device can be properly operated without any external components.

Unused pin may be left floating or connected to ground.

TI recommends pulling up the digital control pin (IN) to V_{CC} or pulling down to GND to avoid undesired switch positions that could result from the floating pin. A floating digital pin could cause excess current consumption refer to *Implications of Slow or Floating CMOS Inputs*.

8.3.2 Detailed Design Procedure

Select the appropriate supply voltage to cover the entire voltage swing of the signal passing through the switch because the TS5A3167 input and output signal swing through NC and COM are dependent on the supply voltage V_{CC}. For example, if the desired signal level to pass through the switch is 5V, V_{CC} must be greater than or equal to 5V. V_{CC} = 3.3V is not valid for passing a 5V signal since the analog signal voltage cannot exceed the supply.

8.3.3 Application Curves

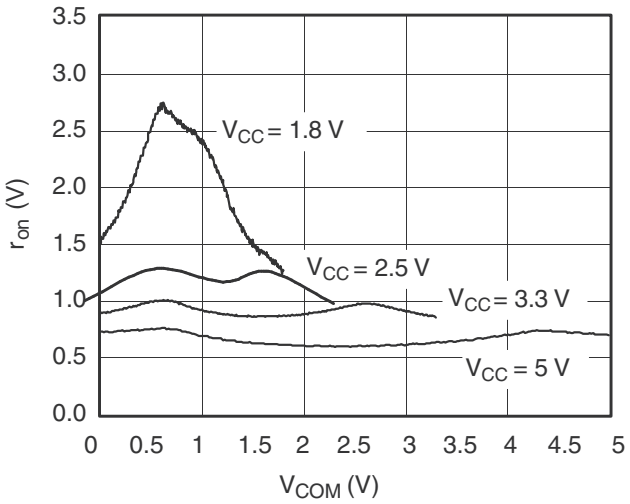


Figure 8-2. r_{on} vs V_{COM}

Power Supply Recommendations

TI recommends proper power-supply sequencing for all CMOS devices. Do not exceed the absolute maximum ratings, because stresses beyond the listed ratings can cause permanent damage to the device. It is recommended that V_{CC} is powered on first, followed by NC or COM but not required because of the Isolation in Powered-Off Mode, V_{CC} = 0 feature.

Although it is not required, power-supply bypassing improves noise margin and prevents switching noise propagation from the V_{CC} supply to other components. A 0.1µF capacitor, connected from V_{CC} to GND, is adequate for most applications.

8.4 Layout

8.4.1 Layout Guidelines

TI recommends following common printed-circuit board layout guidelines to ensure reliability of the device.

- Use bypass capacitors on power supplies
- Use short trace lengths to avoid excessive loading

8.4.2 Layout Example

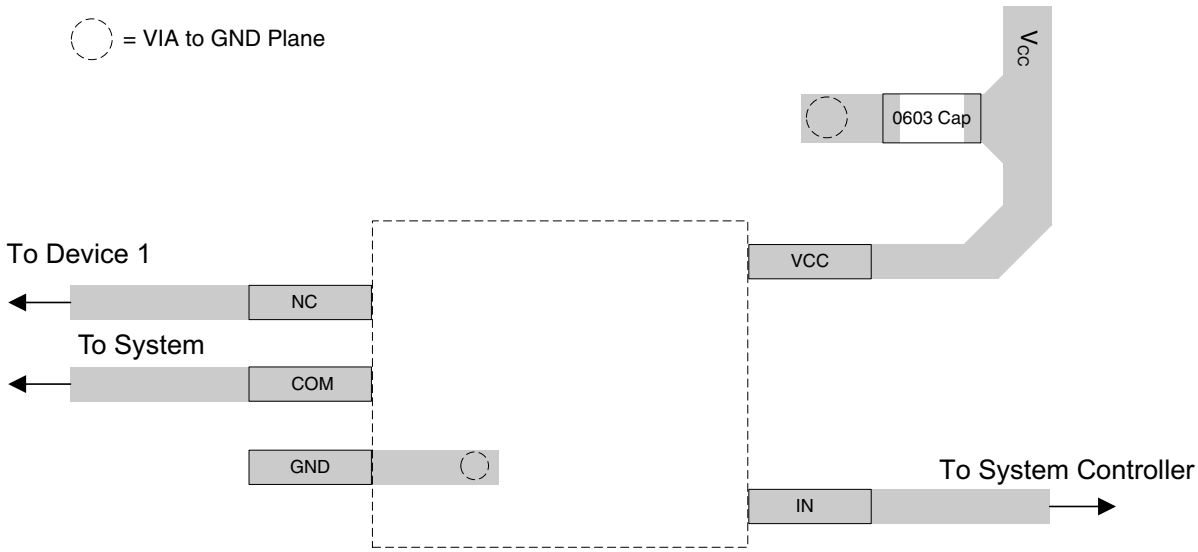


Figure 8-3. Example Layout

9 Device and Documentation Support

9.1 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

9.2 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

9.3 Trademarks

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10 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision C (August 2018) to Revision D (June 2025)	Page
• Updated the numbering format for tables, figures, and cross-references throughout the document	1
• Moved *Parameter Description* table from Section 9 to Section 6	13

Changes from Revision B (March 2017) to Revision C (August 2018)	Page
• Changed the DSBGA Body Size From: 1.50 mm x 9.00 mm To: 1.50 mm x 0.90 mm in the *Device Information* table	1
• Changed the YZP package pinout view From: Top View To: Bottom View	3

Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TS5A3167DBVR	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	NIPDAU | SN	Level-1-260C-UNLIM	-40 to 85	(JATF, JATR) (JATH, JATP)
TS5A3167DBVR.B	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 85	(JATF, JATR) (JATH, JATP)
TS5A3167DCKR	Active	Production	SC70 (DCK) | 5	3000 | LARGE T&R	Yes	NIPDAU | SN	Level-1-260C-UNLIM	-40 to 85	(JG5, JGF, JGR) (JGH, JGP, JGS)
TS5A3167DCKR.B	Active	Production	SC70 (DCK) | 5	3000 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 85	(JG5, JGF, JGR) (JGH, JGP, JGS)
TS5A3167DCKRG4	Active	Production	SC70 (DCK) | 5	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	(JG5, JGF, JGR) (JGH, JGP, JGS)
TS5A3167DCKRG4.B	Active	Production	SC70 (DCK) | 5	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	(JG5, JGF, JGR) (JGH, JGP, JGS)
TS5A3167YZPR	Active	Production	DSBGA (YZP) | 5	3000 | LARGE T&R	Yes	SNAGCU	Level-1-260C-UNLIM	-40 to 85	JGN
TS5A3167YZPR.B	Active	Production	DSBGA (YZP) | 5	3000 | LARGE T&R	Yes	SNAGCU	Level-1-260C-UNLIM	-40 to 85	JGN

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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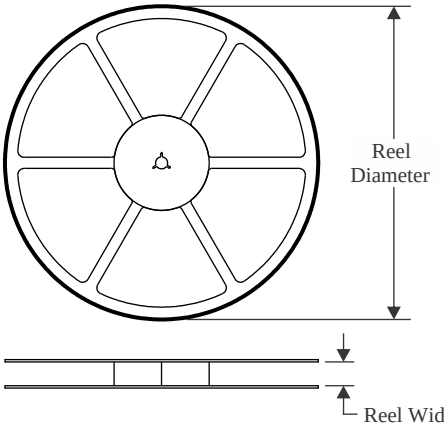
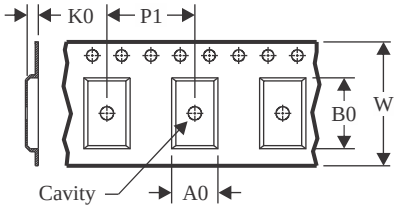
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

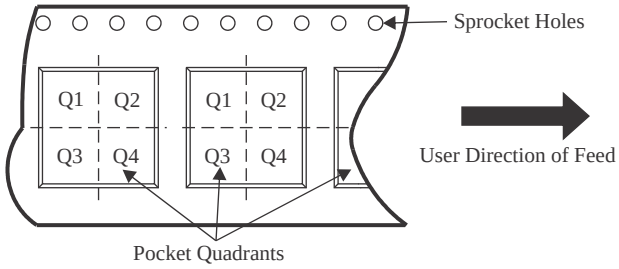


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

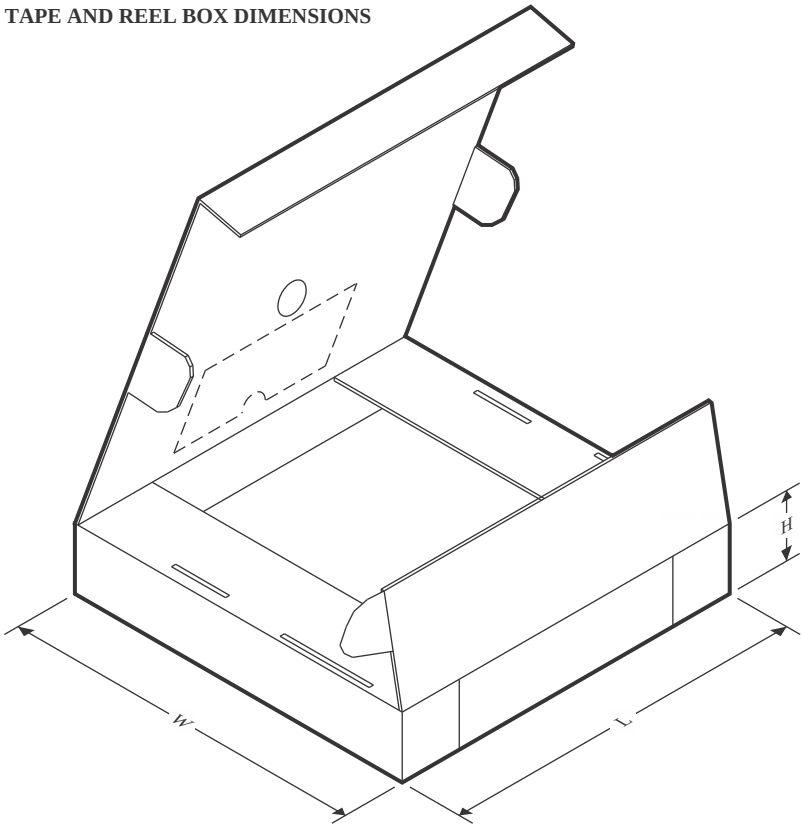
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TS5A3167DBVR	SOT-23	DBV	5	3000	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3
TS5A3167DCKR	SC70	DCK	5	3000	180.0	8.4	2.47	2.3	1.25	4.0	8.0	Q3
TS5A3167DCKR	SC70	DCK	5	3000	180.0	8.4	2.3	2.5	1.2	4.0	8.0	Q3
TS5A3167DCKR	SC70	DCK	5	3000	178.0	8.4	2.25	2.45	1.2	4.0	8.0	Q3
TS5A3167DCKRG4	SC70	DCK	5	3000	180.0	8.4	2.47	2.3	1.25	4.0	8.0	Q3
TS5A3167YZPR	DSBGA	YZP	5	3000	178.0	9.2	1.02	1.52	0.63	4.0	8.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

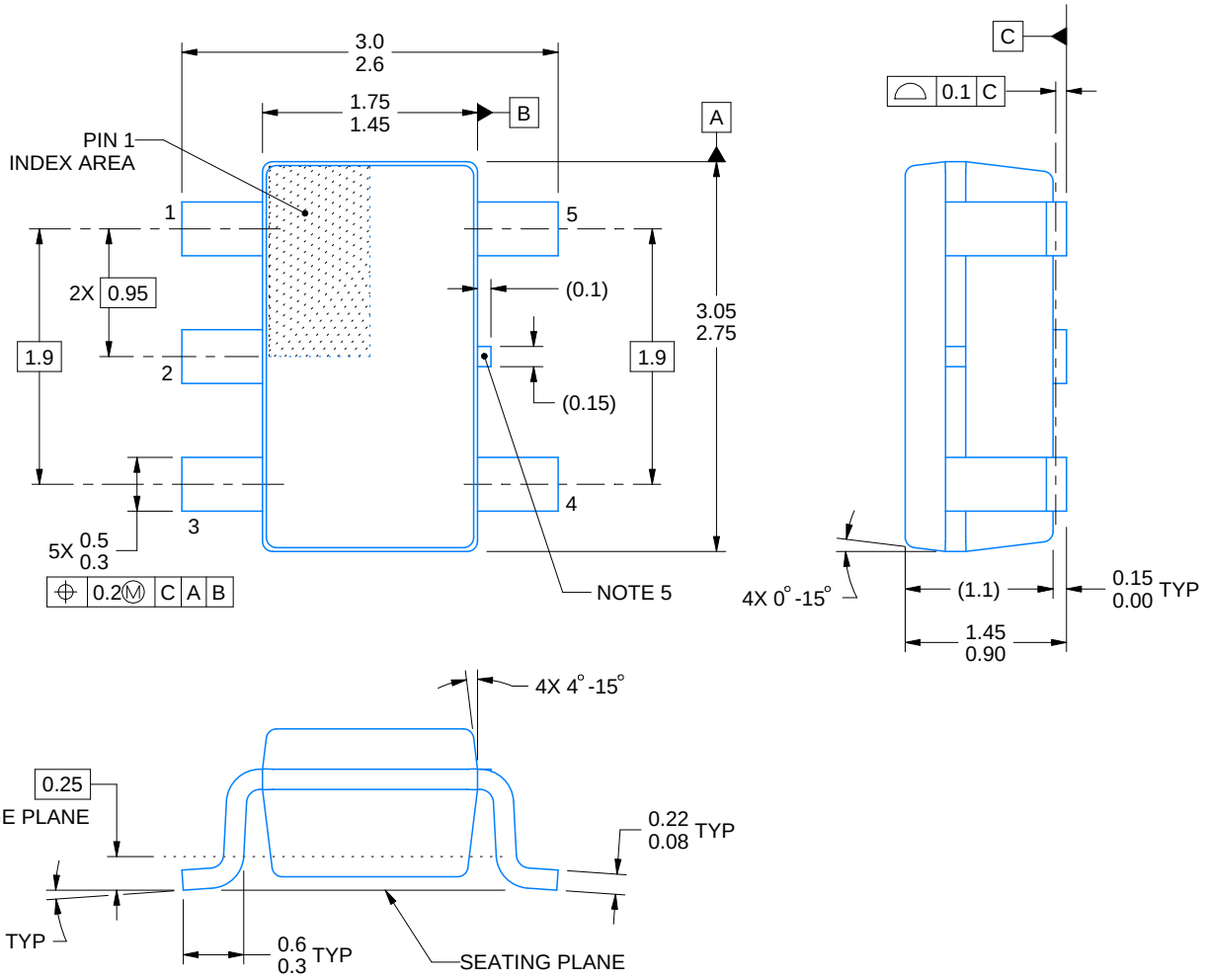
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TS5A3167DBVR	SOT-23	DBV	5	3000	180.0	180.0	18.0
TS5A3167DCKR	SC70	DCK	5	3000	202.0	201.0	28.0
TS5A3167DCKR	SC70	DCK	5	3000	210.0	185.0	35.0
TS5A3167DCKR	SC70	DCK	5	3000	208.0	191.0	35.0
TS5A3167DCKRG4	SC70	DCK	5	3000	202.0	201.0	28.0
TS5A3167YZPR	DSBGA	YZP	5	3000	220.0	220.0	35.0

PACKAGE OUTLINE

DBV0005A

SOT-23 - 1.45 mm max height

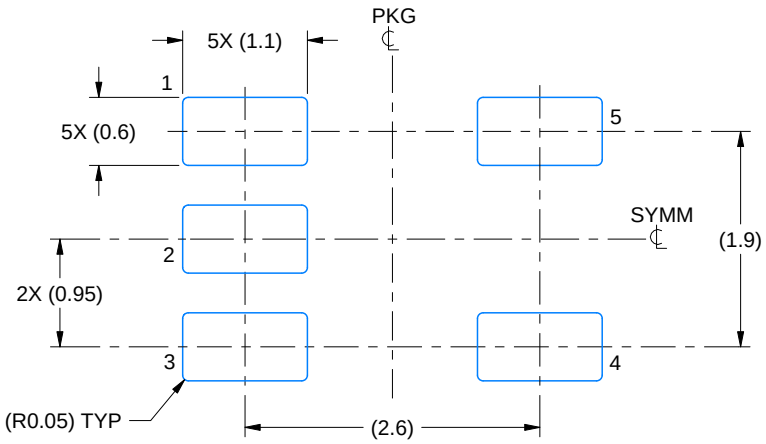
SMALL OUTLINE TRANSISTOR



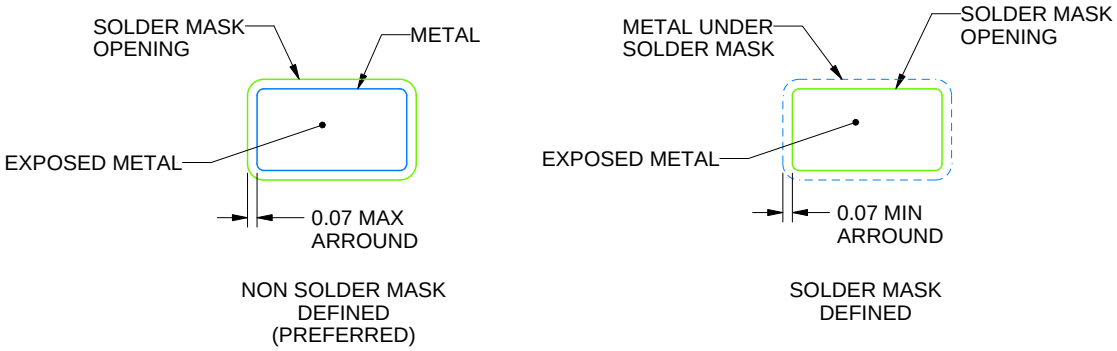
4214839/K 08/2024

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Refernce JEDEC MO-178.
4. Body dimensions do not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.25 mm per side.
5. Support pin may differ or may not be present.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X

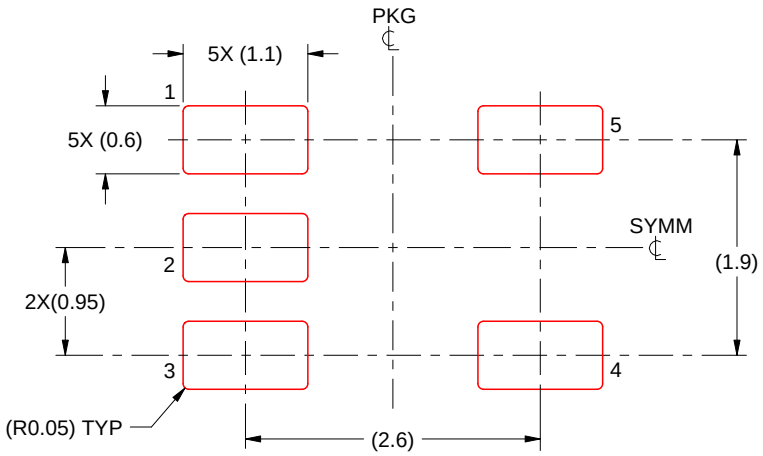


SOLDER MASK DETAILS

4214839/K 08/2024

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:15X

4214839/K 08/2024

NOTES: (continued)

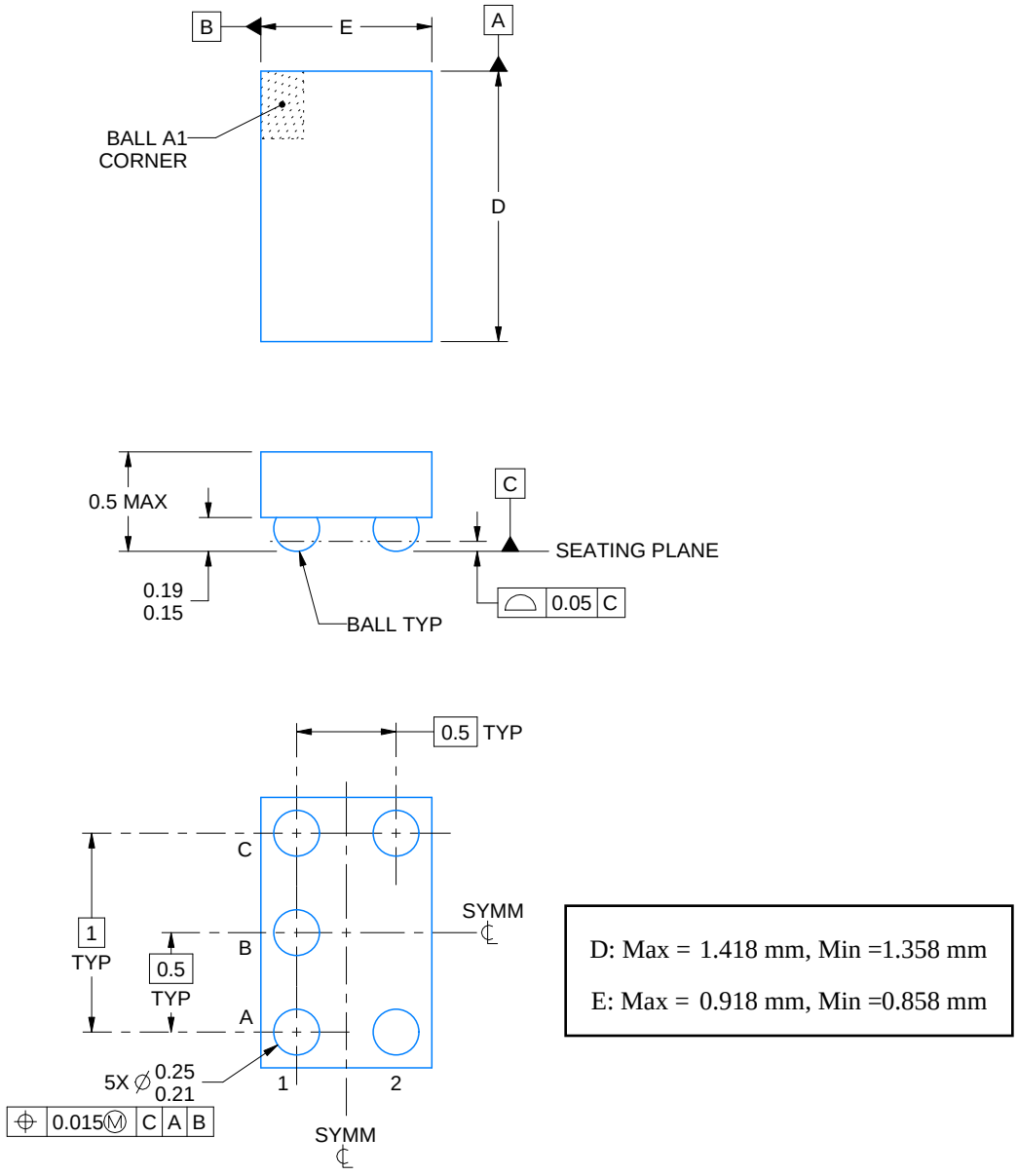
8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

PACKAGE OUTLINE

YZP0005

DSBGA - 0.5 mm max height

DIE SIZE BALL GRID ARRAY



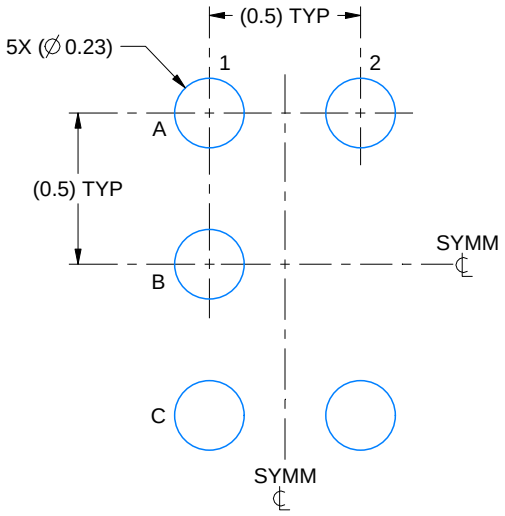
D: Max = 1.418 mm, Min =1.358 mm

E: Max = 0.918 mm, Min =0.858 mm

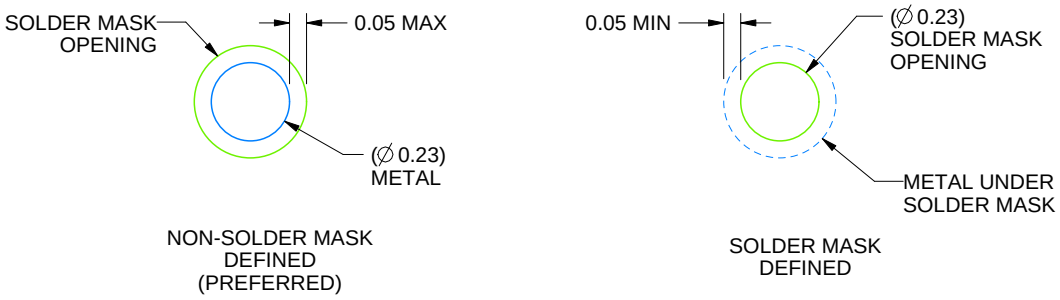
4219492/A 05/2017

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.



LAND PATTERN EXAMPLE
SCALE:40X

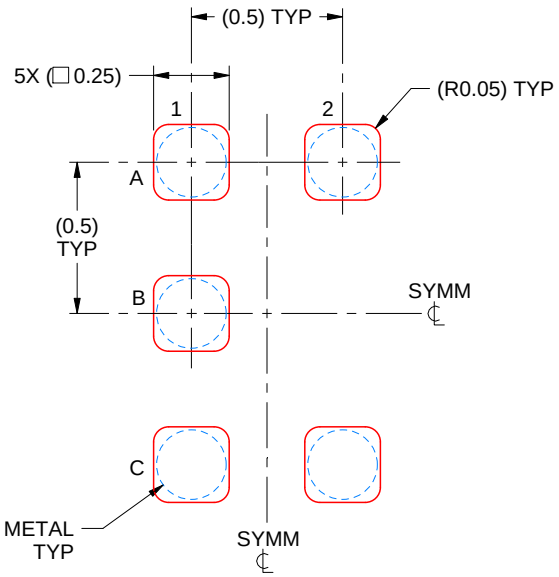


SOLDER MASK DETAILS
NOT TO SCALE

4219492/A 05/2017

NOTES: (continued)

3. Final dimensions may vary due to manufacturing tolerance considerations and also routing constraints. For more information, see Texas Instruments literature number SNVA009 (www.ti.com/lit/snva009).



SOLDER PASTE EXAMPLE
BASED ON 0.1 mm THICK STENCIL
SCALE:40X

4219492/A 05/2017

NOTES: (continued)

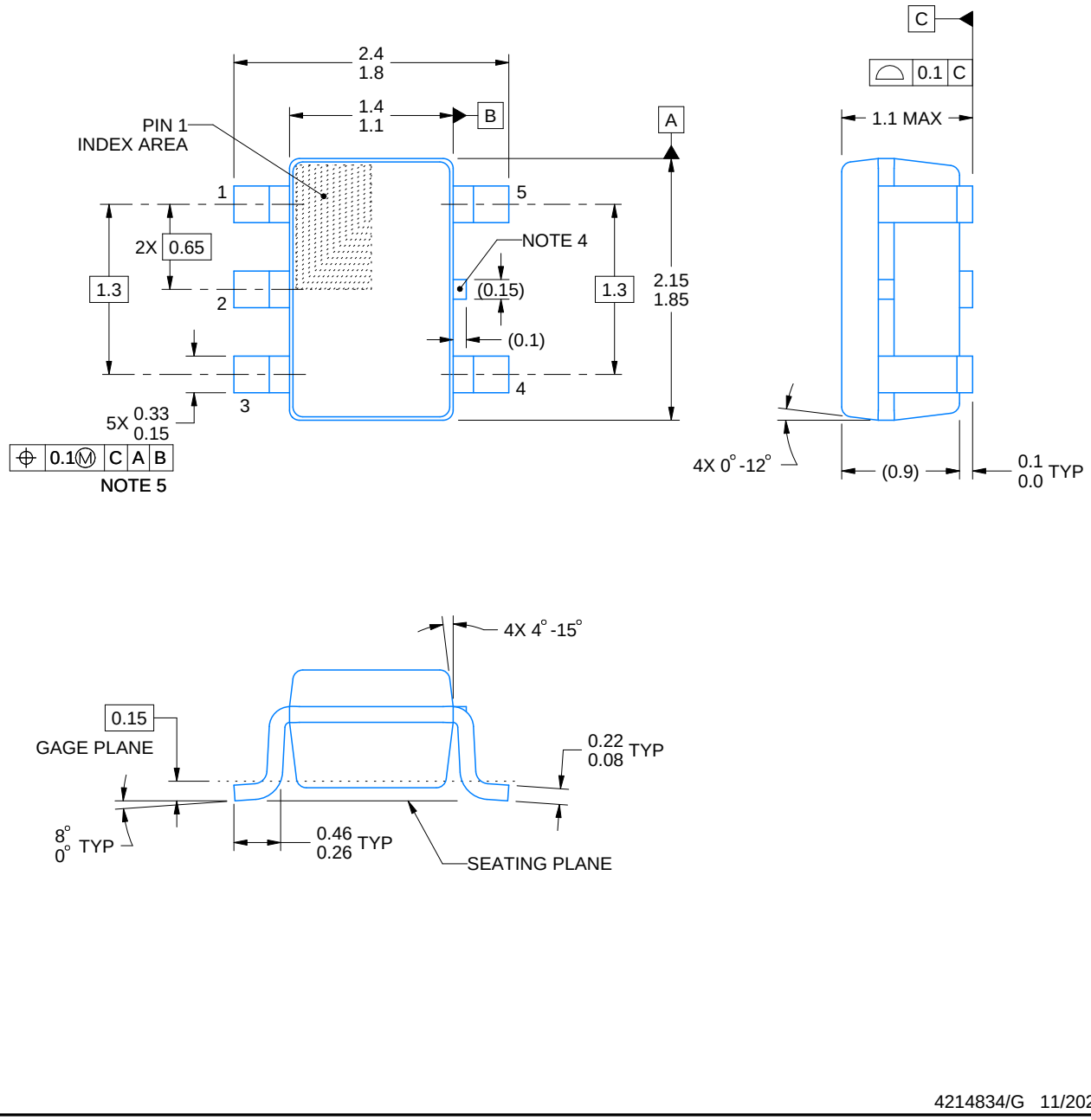
4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release.

PACKAGE OUTLINE

DCK0005A

SOT - 1.1 max height

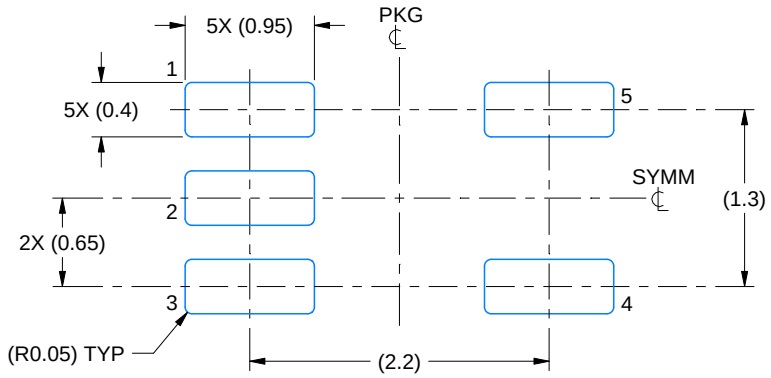
SMALL OUTLINE TRANSISTOR



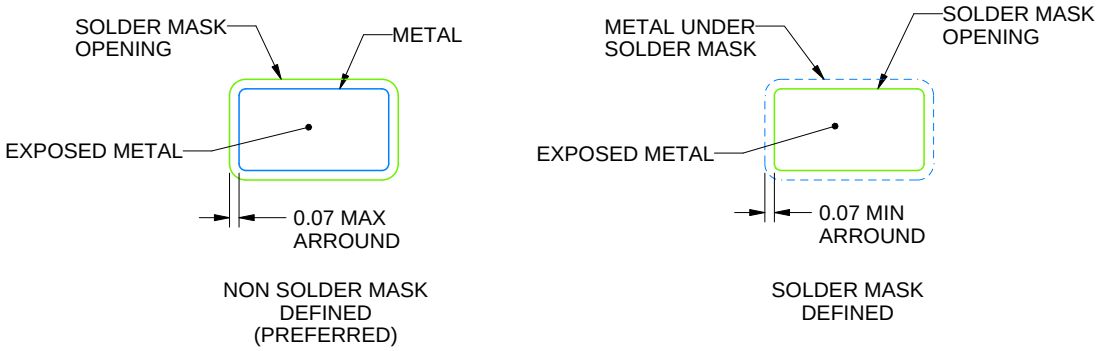
4214834/G 11/2024

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Refernce JEDEC MO-203.
4. Support pin may differ or may not be present.
5. Lead width does not comply with JEDEC.
6. Body dimensions do not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.25mm per side



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:18X

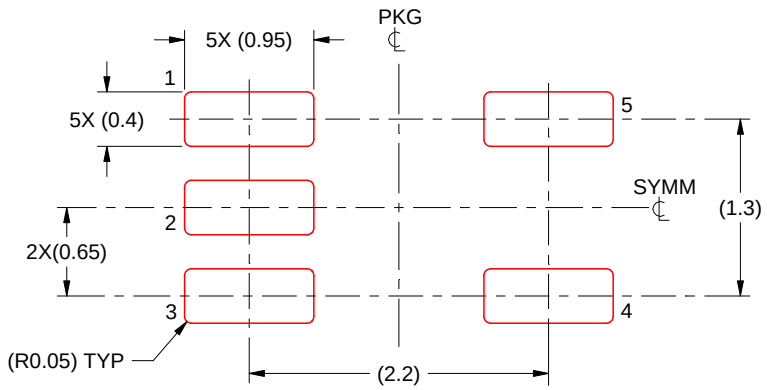


SOLDER MASK DETAILS

4214834/G 11/2024

NOTES: (continued)

7. Publication IPC-7351 may have alternate designs.
8. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 THICK STENCIL
SCALE:18X

4214834/G 11/2024

NOTES: (continued)

9. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
10. Board assembly site may have different recommendations for stencil design.

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Last updated 10/2025