

## Single 5- $\Omega$ SP3T Analog Switch 5-V/3.3-V 3:1 Multiplexer/Demultiplexer

### 1 Features

- Specified Break-Before-Make Switching
- Low ON-State Resistance
- High Bandwidth
- Control Inputs Are 5.5-V Tolerant
- Low Charge Injection
- Excellent ON-State Resistance Matching
- Low Total Harmonic Distortion (THD)
- 1.65-V to 5.5-V Single-Supply Operation
- Latch-Up Performance Exceeds 100 mA Per JESD 78, Class II
- ESD Performance Tested Per JESD 22
  - 2000-V Human-Body Model (A114-B, Class II)
  - 1000-V Charged-Device Model (C101)

### 2 Applications

- Cell Phones
- PDAs
- Portable Instrumentation

### 3 Description

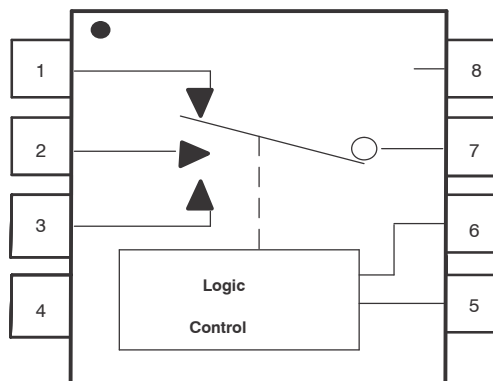
The TS5A3357 is a high-performance, 1-channel 3:1 analog switch that is designed to operate from 1.65 V to 5.5 V. The device offers a low ON-state resistance and low input/output capacitance and, thus, causes a low signal distortion. The break-before-make feature allows transferring of a signal from one port to another, with a minimal signal distortion. This device also offers a low charge injection which makes this device suitable for high-performance audio and data acquisition systems.

#### Device Information<sup>(1)</sup>

PART NUMBER	PACKAGE	BODY SIZE (NOM)
TS5A3357	VSSOP (8)	2.3 mm x 2 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

#### Logic Diagram



## Table of Contents

<b>1 Features</b> .....	<b>1</b>	9.2 Functional Block Diagram .....	20
<b>2 Applications</b> .....	<b>1</b>	9.3 Feature Description .....	20
<b>3 Description</b> .....	<b>1</b>	9.4 Device Functional Modes .....	20
<b>4 Revision History</b> .....	<b>2</b>	<b>10 Application and Implementation</b> .....	<b>21</b>
<b>5 Device Comparison Table</b> .....	<b>3</b>	10.1 Application Information .....	21
<b>6 Pin Configuration and Functions</b> .....	<b>4</b>	10.2 Typical Application .....	21
<b>7 Specifications</b> .....	<b>5</b>	<b>11 Power Supply Recommendations</b> .....	<b>22</b>
7.1 Absolute Maximum Ratings .....	5	<b>12 Layout</b> .....	<b>23</b>
7.2 ESD Ratings .....	5	12.1 Layout Guidelines .....	23
7.3 Recommended Operating Conditions .....	5	12.2 Layout Example .....	23
7.4 Thermal Information .....	5	<b>13 Device and Documentation Support</b> .....	<b>24</b>
7.5 Electrical Characteristics for 5-V Supply .....	6	13.1 Device Support .....	24
7.6 Electrical Characteristics for 3.3-V Supply .....	8	13.2 Documentation Support .....	24
7.7 Electrical Characteristics for 2.5-V Supply .....	10	13.3 Receiving Notification of Documentation Updates .....	24
7.8 Electrical Characteristics for 1.8-V Supply .....	12	13.4 Community Resources .....	24
7.9 Typical Characteristics .....	14	13.5 Trademarks .....	24
<b>8 Parameter Measurement Information</b> .....	<b>16</b>	13.6 Electrostatic Discharge Caution .....	24
<b>9 Detailed Description</b> .....	<b>20</b>	13.7 Glossary .....	24
9.1 Overview .....	20	<b>14 Mechanical, Packaging, and Orderable Information</b> .....	<b>24</b>

## 4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision A (December 2007) to Revision B	Page
<ul style="list-style-type: none"> <li>Added <i>Device Information</i> table, <i>ESD Ratings</i> table, <i>Recommended Operating Conditions</i> table, <i>Feature Description</i> section, <i>Device Functional Modes</i>, <i>Application and Implementation</i> section, <i>Power Supply Recommendations</i> section, <i>Layout</i> section, <i>Device and Documentation Support</i> section, and <i>Mechanical, Packaging, and Orderable Information</i> section .....</li> </ul>	<b>1</b>

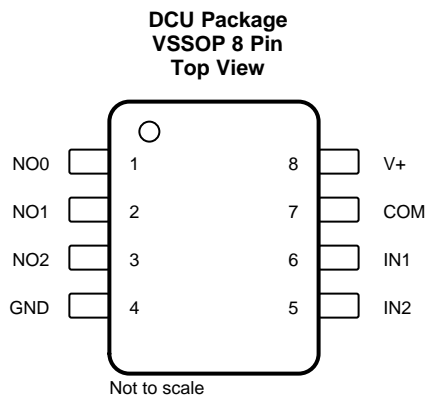
## 5 Device Comparison Table

**Table 1. Summary of Characteristics<sup>(1)</sup>**

Configuration	Triple 3:1 Multiplexer/ Demultiplexer (1 × SP3T)
Number of channels	1
ON-state resistance ( $r_{on}$ )	5 $\Omega$
ON-state resistance match ( $\Delta r_{on}$ )	0.1 $\Omega$
ON-state resistance flatness ( $r_{on(flat)}$ )	6.5 $\Omega$
Turn-on/turn-off time ( $t_{ON}/t_{OFF}$ )	6.5 ns/3.7 ns
Break-before-make time ( $t_{BBM}$ )	0.5 ns
Charge injection ( $Q_C$ )	3.4 pC
Bandwidth (BW)	334 MHz
OFF isolation ( $O_{ISO}$ )	–82 dB at 10 MHz
Crosstalk ( $X_{TALK}$ )	–62 dB at 10 MHz
Total harmonic distortion (THD)	0.05%
Leakage current ( $I_{COM(OFF)}$ )	$\pm 1 \mu A$

(1)  $V_+ = 5 V$ ,  $T_A = 25^\circ C$

## 6 Pin Configuration and Functions



### Pin Functions

PIN		DESCRIPTION
NAME	NO.	
NO0	1	Normally open
NO1	2	Normally open
NO2	3	Normally open
GND	4	Digital ground
IN2	5	Digital control to connect COM to NO
IN1	6	Digital control to connect COM to NO
COM	7	Common
V+	8	Power supply

## 7 Specifications

### 7.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)<sup>(1)</sup>

		MIN	MAX	UNIT
V <sub>+</sub>	Supply voltage range <sup>(2)</sup>	-0.5	6.5	V
V <sub>NO</sub> V <sub>COM</sub>	Analog voltage range <sup>(2) (3) (4)</sup>	-0.5	V <sub>+</sub> + 0.5	V
I <sub>K</sub>	Analog port diode current	V <sub>NO</sub> , V <sub>COM</sub> < 0 or V <sub>NO</sub> , V <sub>COM</sub> > V <sub>+</sub>		mA
I <sub>NO</sub> I <sub>COM</sub>	On-state switch current	V <sub>NO</sub> , V <sub>COM</sub> = 0 to V <sub>+</sub>		mA
V <sub>I</sub>	Digital input voltage range <sup>(2) (3)</sup>	-0.5	6.5	V
I <sub>IK</sub>	Digital input clamp current	V <sub>I</sub> < 0		mA
I <sub>+</sub>	Continuous current through V <sub>+</sub>		100	mA
I <sub>GND</sub>	Continuous current through GND	-100	100	mA
T <sub>stg</sub>	Storage temperature range	-65	150	°C

- (1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) All voltages are with respect to ground, unless otherwise specified.
- (3) The input and output voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
- (4) This value is limited to 5.5 V maximum.

### 7.2 ESD Ratings

		VALUE	UNIT
V <sub>(ESD)</sub>	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 <sup>(1)</sup>	±2000
		Charged-device model (CDM), per JEDEC specification JESD22-C101 <sup>(2)</sup>	±1000

- (1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
- (2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

### 7.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
V <sub>+</sub>	Supply voltage range	1.65	5.5	V
V <sub>NO</sub> V <sub>COM</sub>	Analog voltage range	0	V <sub>+</sub>	
V <sub>I</sub>	Digital input voltage range	0	5.5	

### 7.4 Thermal Information

THERMAL METRIC <sup>(1)</sup>		TS5A3357	UNIT
		DCU (VSSOP)	
		8 PINS	
R <sub>θJA</sub>	Junction-to-ambient thermal resistance	206.5	°C/W
R <sub>θJC(top)</sub>	Junction-to-case (top) thermal resistance	78.7	°C/W
R <sub>θJB</sub>	Junction-to-board thermal resistance	85.3	°C/W
ψ <sub>JT</sub>	Junction-to-top characterization parameter	7.3	°C/W
ψ <sub>JB</sub>	Junction-to-board characterization parameter	84.8	°C/W
R <sub>θJC(bot)</sub>	Junction-to-case (bottom) thermal resistance	n/a	°C/W

- (1) For more information about traditional and new thermal metrics, see the [Semiconductor and IC Package Thermal Metrics](#) application report.

## 7.5 Electrical Characteristics for 5-V Supply<sup>(1)</sup>

$V_+ = 4.5\text{ V to }5.5\text{ V}$ ,  $T_A = -40^\circ\text{C to }85^\circ\text{C}$  (unless otherwise noted)

PARAMETER	SYMBOL	TEST CONDITIONS	$T_A$	$V_+$	MIN	TYP	MAX	UNIT	
<b>Analog Switch</b>									
Peak ON resistance	$r_{\text{peak}}$	$0 \leq V_{\text{NO}} \leq V_+$ , $I_{\text{COM}} = -30\text{ mA}$ , Switch ON, See <a href="#">Figure 13</a>	Full	4.5 V			15	$\Omega$	
ON-state resistance	$r_{\text{on}}$	$V_{\text{NO}} = 0$ , $I_{\text{COM}} = 30\text{ mA}$	25°C	4.5 V			5	7	$\Omega$
			Full				7		
		$V_{\text{NO}} = 2.4\text{ V}$ , $I_{\text{COM}} = -30\text{ mA}$	25°C				6	12	
			Full				12		
$V_{\text{NO}} = 4.5\text{ V}$ , $I_{\text{COM}} = -30\text{ mA}$	25°C	7	15						
	Full	15							
ON-state resistance match between channels	$\Delta r_{\text{on}}$	$V_{\text{NO}} = 3.15\text{ V}$ , $I_{\text{COM}} = -30\text{ mA}$ , Switch ON, See <a href="#">Figure 13</a>	25°C	4.5 V		0.1		$\Omega$	
ON-state resistance flatness	$r_{\text{on(Flat)}}$	$0 \leq V_{\text{NO}} \leq V_+$ , $I_{\text{COM}} = -30\text{ mA}$ , Switch ON, See <a href="#">Figure 13</a>	25°C	5 V		6.5		$\Omega$	
NO OFF leakage current	$I_{\text{NO(OFF)}}$	$V_{\text{NO}} = 0\text{ to }V_+$ , $V_{\text{COM}} = V_+\text{ to }0$ , Switch OFF, See <a href="#">Figure 14</a>	25°C	5.5 V			-0.1	0.1	$\mu\text{A}$
			Full				-1	1	
COM OFF leakage current	$I_{\text{COM(OFF)}}$	$V_{\text{COM}} = 0\text{ to }V_+$ , $V_{\text{NO}} = V_+\text{ to }0$ , Switch OFF, See <a href="#">Figure 14</a>	25°C	0			-0.1	0.1	$\mu\text{A}$
			Full				-1	1	
NO ON leakage current	$I_{\text{NO(ON)}}$	$V_{\text{NO}} = 0\text{ to }V_+$ , $V_{\text{COM}} = \text{Open}$ , Switch ON, See <a href="#">Figure 14</a>	25°C	5.5 V			-0.1	0.1	$\mu\text{A}$
			Full				-1	1	
COM ON leakage current	$I_{\text{COM(ON)}}$	$V_{\text{NO}} = \text{Open}$ , $V_{\text{COM}} = 0\text{ to }V_+$ , Switch ON, See <a href="#">Figure 14</a>	25°C	5.5 V			-0.1	0.1	$\mu\text{A}$
			Full				-1	1	
<b>Digital Control Inputs (IN1, IN2)<sup>(2)</sup></b>									
Input logic high	$V_{\text{IH}}$		Full			$V_+ \times 0.7$	5.5	V	
Input logic low	$V_{\text{IL}}$		Full		0		$V_+ \times 0.3$	V	
Input leakage current	$I_{\text{IH}}, I_{\text{IL}}$	$V_{\text{I}} = 5.5\text{ V or }0$	25°C	5.5 V			0.1	$\mu\text{A}$	
			Full				1		

(1) The algebraic convention, whereby the most negative value is a minimum and the most positive value is a maximum

(2) All unused digital inputs of the device must be held at  $V_+$  or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

**Electrical Characteristics for 5-V Supply<sup>(1)</sup> (continued)**
 $V_+ = 4.5\text{ V to }5.5\text{ V}$ ,  $T_A = -40^\circ\text{C to }85^\circ\text{C}$  (unless otherwise noted)

PARAMETER	SYMBOL	TEST CONDITIONS	$T_A$	$V_+$	MIN	TYP	MAX	UNIT
<b>Dynamic</b>								
Turn-on time	$t_{ON}$	$V_{NO} = V_+$ or GND, $R_L = 500\ \Omega$ , See <a href="#">Figure 16</a>	25°C	5 V	1.5		6.5	ns
			Full	4.5 V to 5.5 V	1.5		7	
Turn-off time	$t_{OFF}$	$V_{NO} = V_+$ or GND, $R_L = 500\ \Omega$ , See <a href="#">Figure 16</a>	25°C	5 V	0.8		3.7	ns
			Full	4.5 V to 5.5 V	0.8		7	
Break-before-make time	$t_{BBM}$	$V_{NO} = V_+$ , $R_L = 50\ \Omega$ , See <a href="#">Figure 17</a>	25°C	5 V	0.5			ns
			Full	4.5 V to 5.5 V	0.5			
Charge injection	$Q_C$	$V_{GEN} = 0$ , $C_L = 0.1\text{ nF}$ , See <a href="#">Figure 21</a>	25°C	5 V		3.4		pC
NO OFF capacitance	$C_{NO(OFF)}$	$V_{NO} = V_+$ or GND, Switch OFF, See <a href="#">Figure 15</a>	25°C	5 V		4.5		pF
COM OFF capacitance	$C_{COM(OFF)}$	$V_{NO} = V_+$ or GND, Switch OFF, See <a href="#">Figure 15</a>	25°C	5 V		10.5		pF
NO ON capacitance	$C_{NO(ON)}$	$V_{NO} = V_+$ or GND, Switch ON, See <a href="#">Figure 15</a>	25°C	5 V		17		pF
COM ON capacitance	$C_{COM(ON)}$	$V_{COM} = V_+$ or GND, Switch ON, See <a href="#">Figure 15</a>	25°C	5 V		17		pF
Digital input capacitance	$C_I$	$V_I = V_+$ or GND, See <a href="#">Figure 15</a>	25°C	5 V		3		pF
Bandwidth	BW	$R_L = 50\ \Omega$ , Switch ON, See <a href="#">Figure 18</a>	25°C	4.5 V to 5.5 V		334		MHz
OFF isolation	$O_{ISO}$	$R_L = 50\ \Omega$ , $f = 10\text{ MHz}$ , Switch OFF, See <a href="#">Figure 19</a>	25°C	4.5 V to 5.5 V		-82		dB
Crosstalk	$X_{TALK}$	$R_L = 50\ \Omega$ , $f = 10\text{ MHz}$ , Switch ON, See <a href="#">Figure 20</a>	25°C	4.5 V to 5.5 V		-62		dB
<b>Supply</b>								
Positive supply current	$I_+$	$V_I = V_+$ or GND, Switch ON or OFF	25°C	5.5 V			1	$\mu\text{A}$
			Full				10	

## 7.6 Electrical Characteristics for 3.3-V Supply<sup>(1)</sup>

$V_+ = 3\text{ V to }3.6\text{ V}$ ,  $T_A = -40^\circ\text{C to }85^\circ\text{C}$  (unless otherwise noted)

PARAMETER	SYMBOL	TEST CONDITIONS	$T_A$	$V_+$	MIN	TYP	MAX	UNIT
<b>Analog Switch</b>								
Peak ON resistance	$r_{\text{peak}}$	$0 \leq V_{\text{NO}} \leq V_+$ , $I_{\text{COM}} = -24\text{ mA}$ , Switch ON, See <a href="#">Figure 13</a>	Full	3 V			25	$\Omega$
ON-state resistance	$r_{\text{on}}$	$V_{\text{NO}} = 0\text{ V}$ , $I_{\text{COM}} = 24\text{ mA}$ Switch ON, See <a href="#">Figure 13</a>	25°C	3 V			6.5	9
			Full				9	
			25°C				9	20
			Full				20	
ON-state resistance match between channels	$\Delta r_{\text{on}}$	$V_{\text{NO}} = 2.1\text{ V}$ , $I_{\text{COM}} = -24\text{ mA}$ , Switch ON, See <a href="#">Figure 13</a>	25°C	3 V		0.1	$\Omega$	
ON-state resistance flatness	$r_{\text{on(Flat)}}$	$0 \leq V_{\text{NO}} \leq V_+$ , $I_{\text{COM}} = -24\text{ mA}$ , Switch ON, See <a href="#">Figure 13</a>	25°C	3.3 V		13.5	$\Omega$	
NO OFF leakage current	$I_{\text{NO(OFF)}}$	$V_{\text{NO}} = 0\text{ to }V_+$ , $V_{\text{COM}} = V_+\text{ to }0$ , Switch OFF, See <a href="#">Figure 14</a>	25°C	3.6 V			-0.1	0.1
			Full				-1	1
COM OFF leakage current	$I_{\text{COM(OFF)}}$	$V_{\text{COM}} = 0\text{ to }V_+$ , $V_{\text{NO}} = V_+\text{ to }0$ , Switch OFF, See <a href="#">Figure 14</a>	25°C	3.6 V			-0.1	0.1
			Full				-1	1
NO ON leakage current	$I_{\text{NO(ON)}}$	$V_{\text{NO}} = 0\text{ to }V_+$ , $V_{\text{COM}} = V_+\text{ to }0$ , Switch ON, See <a href="#">Figure 14</a>	25°C	3.6 V			-0.1	0.1
			Full				-1	1
COM ON leakage current	$I_{\text{COM(ON)}}$	$V_{\text{NO}} = \text{Open}$ , $V_{\text{COM}} = 0\text{ to }V_+$ , Switch ON, See <a href="#">Figure 14</a>	25°C	3.6 V			-0.1	0.1
			Full				-1	1
<b>Digital Control Inputs (IN1, IN2)<sup>(2)</sup></b>								
Input logic high	$V_{\text{IH}}$		Full		$V_+ \times 0.7$		5.5	V
Input logic low	$V_{\text{IL}}$		Full		0		$V_+ \times 0.3$	V
Input leakage current	$I_{\text{IH}}, I_{\text{IL}}$	$V_{\text{I}} = 5.5\text{ V or }0$	25°C	3.6 V			-1	0.1
			Full				1	

(1) The algebraic convention, whereby the most negative value is a minimum and the most positive value is a maximum

(2) All unused digital inputs of the device must be held at  $V_+$  or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.



**Electrical Characteristics for 3.3-V Supply<sup>(1)</sup> (continued)**
 $V_+ = 3\text{ V to }3.6\text{ V}$ ,  $T_A = -40^\circ\text{C to }85^\circ\text{C}$  (unless otherwise noted)

PARAMETER	SYMBOL	TEST CONDITIONS	$T_A$	$V_+$	MIN	TYP	MAX	UNIT
<b>Dynamic</b>								
Turn-on time	$t_{ON}$	$V_{NO} = V_+$ or GND, $R_L = 500\ \Omega$ ,	$C_L = 50\ \text{pF}$ , See <a href="#">Figure 16</a>	25°C	3.3 V	2	9.5	ns
				Full	3 V to 3.6 V	2	11	
Turn-off time	$t_{OFF}$	$V_{NO} = V_+$ or GND, $R_L = 500\ \Omega$ ,	$C_L = 50\ \text{pF}$ , See <a href="#">Figure 16</a>	25°C	3.3 V	1.3	5.1	ns
				Full	3 V to 3.6 V	1.5	5.5	
Break-before-make time	$t_{BBM}$	$V_{NO} = V_+$ , $R_L = 50\ \Omega$ ,	$C_L = 50\ \text{pF}$ , See <a href="#">Figure 17</a>	25°C	3.3 V	0.5		ns
				Full	3 V to 3.6 V	0.5		
Charge injection	$Q_C$	$V_{GEN} = 0$ , $C_L = 0.1\ \text{nF}$ ,	25°C	3.3 V		1.75		pC
NO OFF capacitance	$C_{NO(OFF)}$	$V_{NO} = V_+$ or GND, Switch OFF,	25°C	3.3 V		4.5		pF
COM OFF capacitance	$C_{COM(OFF)}$	$V_{NO} = V_+$ or GND, Switch OFF,	25°C	3.3 V		10.5		pF
NO ON capacitance	$C_{NO(ON)}$	$V_{NO} = V_+$ or GND, Switch ON,	25°C	3.3 V		17		pF
COM ON capacitance	$C_{COM(ON)}$	$V_{COM} = V_+$ or GND, Switch ON,	25°C	3.3 V		17		pF
Digital input capacitance	$C_I$	$V_I = V_+$ or GND,	25°C	3.3 V		3		pF
Bandwidth	BW	$R_L = 50\ \Omega$ , Switch ON,	25°C	3 V to 3.6 V		327		MHz
OFF isolation	$O_{ISO}$	$R_L = 50\ \Omega$ , $f = 10\ \text{MHz}$ ,	25°C	3 V to 3.6 V		-82		dB
Crosstalk	$X_{TALK}$	$R_L = 50\ \Omega$ , $f = 10\ \text{MHz}$ ,	25°C	3 V to 3.6 V		-62		dB
<b>Supply</b>								
Positive supply current	$I_+$	$V_I = V_+$ or GND, Switch ON or OFF	25°C	3.6 V			1	$\mu\text{A}$
			Full				10	

## 7.7 Electrical Characteristics for 2.5-V Supply<sup>(1)</sup>

$V_+ = 2.3 \text{ V to } 2.7 \text{ V}$ ,  $T_A = -40^\circ\text{C to } 85^\circ\text{C}$  (unless otherwise noted)

PARAMETER	SYMBOL	TEST CONDITIONS		$T_A$	$V_+$	MIN	TYP	MAX	UNIT
<b>Analog Switch</b>									
Analog signal range	$V_{COM}, V_{NO}$					0		$V_+$	V
Peak ON resistance	$r_{peak}$	$0 \leq V_{NO} \leq V_+$ , $I_{COM} = -8 \text{ mA}$	Switch ON, See Figure 13	Full	2.3 V			50	$\Omega$
ON-state resistance	$r_{on}$	$V_{NO} = 0 \text{ V}$ , $I_{COM} = 8 \text{ mA}$	Switch ON, See Figure 13	25°C	2.3 V	8		12	$\Omega$
				Full				12	
		25°C		11		30			
		Full				30			
ON-state resistance match between channels	$\Delta r_{on}$	$V_{NO} = 1.8 \text{ V}$ , $I_{COM} = -8 \text{ mA}$	Switch ON, See Figure 13	25°C	2.3 V	0.3		$\Omega$	
ON-state resistance flatness	$r_{on(Flat)}$	$0 \leq V_{NO} \leq V_+$ , $I_{COM} = -8 \text{ mA}$	Switch ON, See Figure 13	25°C	2.5 V	39		$\Omega$	
NO OFF leakage current	$I_{NO(OFF)}$	$V_{NO} = 0 \text{ to } V_+$ , $V_{COM} = V_+ \text{ to } 0$	Switch OFF, See Figure 14	25°C	2.7 V	-0.1		0.1	$\mu\text{A}$
				Full		-1		1	
COM OFF leakage current	$I_{COM(OFF)}$	$V_{COM} = 0 \text{ to } V_+$ , $V_{NO} = V_+ \text{ to } 0$	Switch OFF, See Figure 14	25°C	2.7 V	-0.1		0.1	$\mu\text{A}$
				Full		-1		1	
NO ON leakage current	$I_{NO(ON)}$	$V_{NO} = 0 \text{ to } V_+$ , $V_{COM} = V_+ \text{ to } 0$	Switch ON, See Figure 14	25°C	2.7 V	-0.1		0.1	$\mu\text{A}$
				Full		-1		1	
COM ON leakage current	$I_{COM(ON)}$	$V_{NO} = \text{Open}$ , $V_{COM} = 0 \text{ to } V_+$	Switch ON, See Figure 14	25°C	2.7 V	-0.1		0.1	$\mu\text{A}$
				Full		-1		1	
<b>Digital Control Inputs (IN1, IN2)<sup>(2)</sup></b>									
Input logic high	$V_{IH}$			Full		$V_+ \times 0.75$		5.5	V
Input logic low	$V_{IL}$			Full		0	$V_+ \times 0.25$		V
Input leakage current	$I_{IH}, I_{IL}$	$V_I = 5.5 \text{ V or } 0$		25°C	2.7 V			0.1	$\mu\text{A}$
				Full				1	

(1) The algebraic convention, whereby the most negative value is a minimum and the most positive value is a maximum

(2) All unused digital inputs of the device must be held at  $V_+$  or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

**Electrical Characteristics for 2.5-V Supply<sup>(1)</sup> (continued)**
 $V_+ = 2.3\text{ V to }2.7\text{ V}$ ,  $T_A = -40^\circ\text{C to }85^\circ\text{C}$  (unless otherwise noted)

PARAMETER	SYMBOL	TEST CONDITIONS	$T_A$	$V_+$	MIN	TYP	MAX	UNIT
<b>Dynamic</b>								
Turn-on time	$t_{ON}$	$V_{NO} = V_+$ or GND, $R_L = 500\ \Omega$ ,	$C_L = 50\text{ pF}$ , See <a href="#">Figure 16</a>	25°C	2.5 V	3	15	ns
				Full	2.3 V to 2.7 V	3	16.5	
Turn-off time	$t_{OFF}$	$V_{NO} = V_+$ or GND, $R_L = 500\ \Omega$ ,	$C_L = 50\text{ pF}$ , See <a href="#">Figure 16</a>	25°C	2.5 V	2	7.2	ns
				Full	2.3 V to 2.7 V	2	7.8	
Break-before-make time	$t_{BBM}$	$V_{NO} = V_+$ , $R_L = 50\ \Omega$ ,	$C_L = 50\text{ pF}$ , See <a href="#">Figure 17</a>	25°C	2.5 V	0.5		ns
				Full	2.3 V to 2.7 V	0.5		
Charge injection	$Q_C$	$V_{GEN} = 0$ , $C_L = 0.1\text{ nF}$ ,	See <a href="#">Figure 21</a>	25°C	2.5 V	1.15		pC
NO OFF capacitance	$C_{NO(OFF)}$	$V_{NO} = V_+$ or GND, Switch OFF,	See <a href="#">Figure 15</a>	25°C	2.5 V	4.5		pF
COM OFF capacitance	$C_{COM(OFF)}$	$V_{NO} = V_+$ or GND, Switch OFF,	See <a href="#">Figure 15</a>	25°C	2.5 V	10.5		pF
NO ON capacitance	$C_{NO(ON)}$	$V_{NO} = V_+$ or GND, Switch ON,	See <a href="#">Figure 15</a>	25°C	2.5 V	17		pF
COM ON capacitance	$C_{COM(ON)}$	$V_{COM} = V_+$ or GND, Switch ON,	See <a href="#">Figure 15</a>	25°C	2.5 V	17		pF
Digital input capacitance	$C_I$	$V_I = V_+$ or GND,	See <a href="#">Figure 15</a>	25°C	2.5 V	3		pF
Bandwidth	BW	$R_L = 50\ \Omega$ , Switch ON,	See <a href="#">Figure 18</a>	25°C	2.3 V to 2.7 V	320		MHz
OFF isolation	$O_{ISO}$	$R_L = 50\ \Omega$ , $f = 10\text{ MHz}$ ,	Switch OFF, See <a href="#">Figure 19</a>	25°C	2.3 V to 2.7 V	-81		dB
Crosstalk	$X_{TALK}$	$R_L = 50\ \Omega$ , $f = 10\text{ MHz}$ ,	Switch ON, See <a href="#">Figure 20</a>	25°C	2.3 V to 2.7 V	-61		dB
<b>Supply</b>								
Positive supply current	$I_+$	$V_I = V_+$ or GND,	Switch ON or OFF	25°C	2.7 V		1	$\mu\text{A}$
				Full			10	

### 7.8 Electrical Characteristics for 1.8-V Supply<sup>(1)</sup>

$V_+ = 1.65\text{ V to }1.95\text{ V}$ ,  $T_A = -40^\circ\text{C to }85^\circ\text{C}$  (unless otherwise noted)

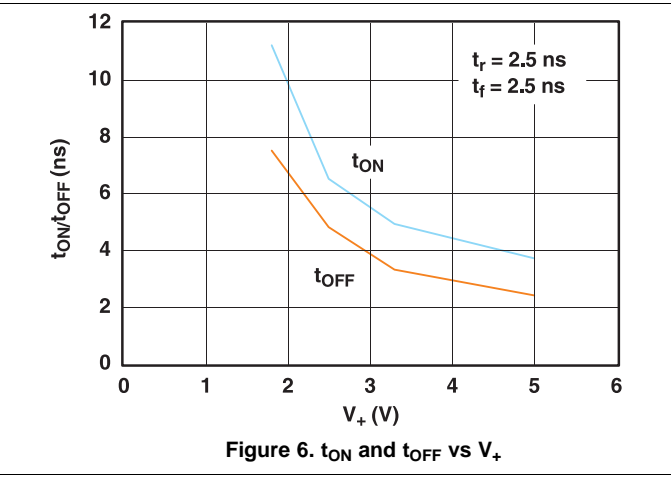
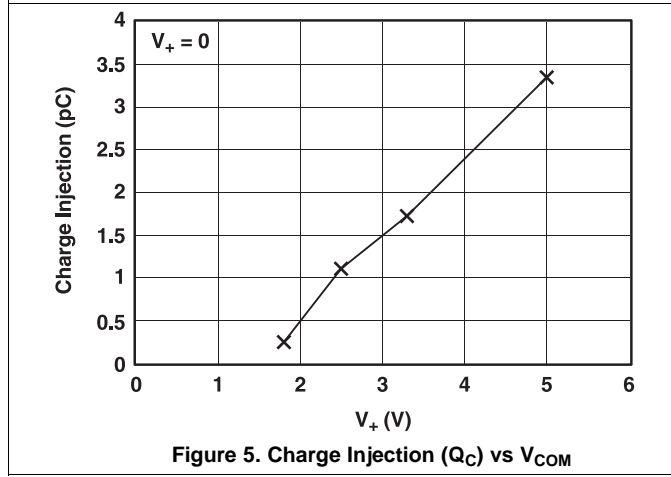
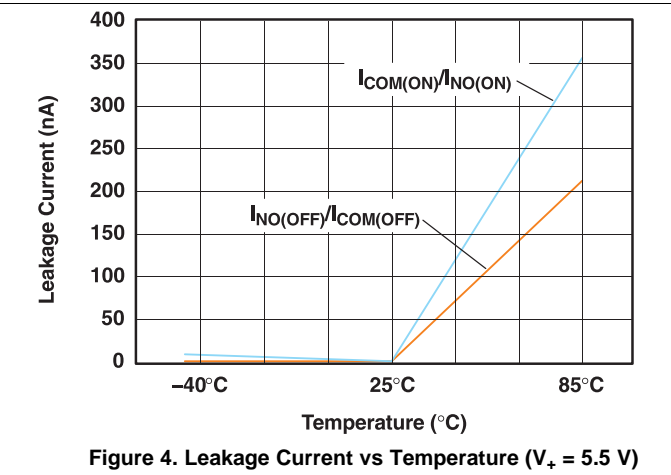
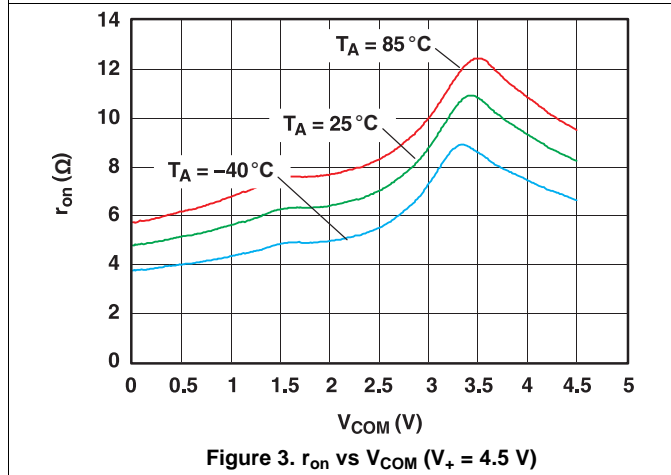
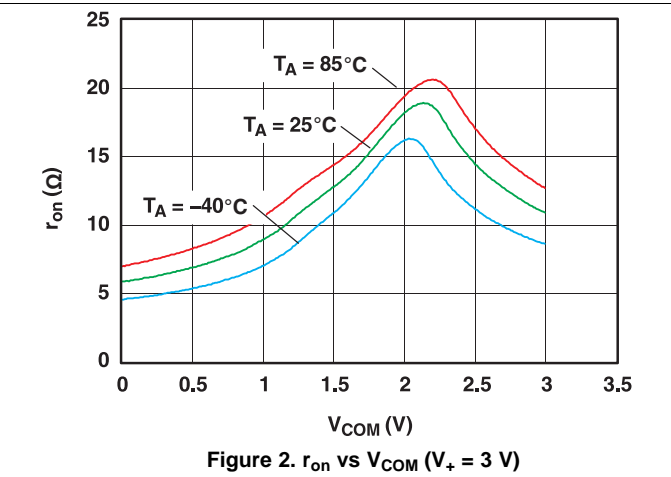
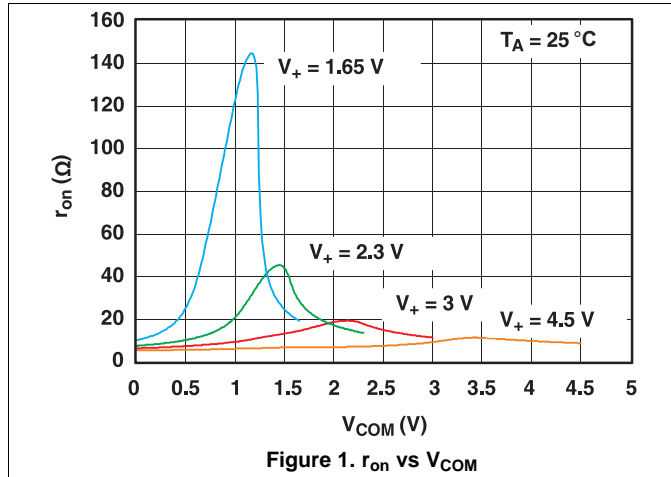
PARAMETER	SYMBOL	TEST CONDITIONS	$T_A$	$V_+$	MIN	TYP	MAX	UNIT	
<b>Analog Switch</b>									
Analog signal range	$V_{COM}, V_{NO}$				0		$V_+$	V	
Peak ON resistance	$r_{peak}$	$0 \leq V_{NO} \leq V_+$ , $I_{COM} = -4\text{ mA}$ , Switch ON, See <a href="#">Figure 13</a>	Full	1.65 V			150	$\Omega$	
ON-state resistance	$r_{on}$	$V_{NO} = 0\text{ V}$ , $I_{COM} = 4\text{ mA}$	25°C	1.65 V			10	$\Omega$	
			Full				20		
		25°C	17				50		
		Full	50						
ON-state resistance match between channels	$\Delta r_{on}$	$V_{NO} = 1.15\text{ V}$ , $I_{COM} = -4\text{ mA}$ , Switch ON, See <a href="#">Figure 13</a>	25°C	1.65 V		0.3		$\Omega$	
ON-state resistance flatness	$r_{on(Flat)}$	$0 \leq V_{NO} \leq V_+$ , $I_{COM} = -4\text{ mA}$ , Switch ON, See <a href="#">Figure 13</a>	25°C	1.8 V		140		$\Omega$	
NO OFF leakage current	$I_{NO(OFF)}$	$V_{NO} = 0\text{ to }V_+$ , $V_{COM} = V_+\text{ to }0$ , Switch OFF, See <a href="#">Figure 14</a>	25°C	1.95 V			-0.1	0.1	$\mu\text{A}$
			Full				-1	1	
COM OFF leakage current	$I_{COM(OFF)}$	$V_{COM} = 0\text{ to }V_+$ , $V_{NO} = V_+\text{ to }0$ , Switch OFF, See <a href="#">Figure 14</a>	25°C	1.95 V			-0.1	0.1	$\mu\text{A}$
			Full				-1	1	
NO ON leakage current	$I_{NO(ON)}$	$V_{NO} = 0\text{ to }V_+$ , $V_{COM} = V_+\text{ to }0$ , Switch ON, See <a href="#">Figure 14</a>	25°C	1.95 V			-0.1	0.1	$\mu\text{A}$
			Full				-1	1	
COM ON leakage current	$I_{COM(ON)}$	$V_{NO} = \text{Open}$ , $V_{COM} = 0\text{ to }V_+$ , Switch ON, See <a href="#">Figure 14</a>	25°C	1.95 V			-0.1	0.1	$\mu\text{A}$
			Full				-1	1	
<b>Digital Control Inputs (IN1, IN2)<sup>(2)</sup></b>									
Input logic high	$V_{IH}$		Full		$V_+ \times 0.75$		5.5	V	
Input logic low	$V_{IL}$		Full		0		$V_+ \times 0.25$	V	
Input leakage current	$I_{IH}, I_{IL}$	$V_I = 5.5\text{ V or }0$	25°C	1.95 V			0.1	$\mu\text{A}$	
			Full				1		

- (1) The algebraic convention, whereby the most negative value is a minimum and the most positive value is a maximum
- (2) All unused digital inputs of the device must be held at  $V_+$  or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

**Electrical Characteristics for 1.8-V Supply<sup>(1)</sup> (continued)**
 $V_+ = 1.65\text{ V to }1.95\text{ V}$ ,  $T_A = -40^\circ\text{C to }85^\circ\text{C}$  (unless otherwise noted)

PARAMETER	SYMBOL	TEST CONDITIONS	$T_A$	$V_+$	MIN	TYP	MAX	UNIT
<b>Dynamic</b>								
Turn-on time	$t_{ON}$	$V_{NO} = V_+$ or GND, $R_L = 500\ \Omega$ , $C_L = 50\text{ pF}$ , See <a href="#">Figure 16</a>	25°C	1.8 V	5		32	ns
			Full	1.65 V to 1.95 V	5		34	
Turn-off time	$t_{OFF}$	$V_{NO} = V_+$ or GND, $R_L = 500\ \Omega$ , $C_L = 50\text{ pF}$ , See <a href="#">Figure 16</a>	25°C	1.8 V	3		14	ns
			Full	1.65 V to 1.95 V	3		14.5	
Break-before-make time	$t_{BBM}$	$V_{NO} = V_+$ , $R_L = 50\ \Omega$ , $C_L = 50\text{ pF}$ , See <a href="#">Figure 17</a>	25°C	1.8 V	0.5			ns
			Full	1.65 V to 1.95 V	0.5			
Charge injection	$Q_C$	$V_{GEN} = 0$ , $C_L = 0.1\text{ nF}$ , See <a href="#">Figure 21</a>	25°C	1.8 V		0.3		pC
NO OFF capacitance	$C_{NO(OFF)}$	$V_{NO} = V_+$ or GND, Switch OFF, See <a href="#">Figure 15</a>	25°C	1.8 V		4.5		pF
COM OFF capacitance	$C_{COM(OFF)}$	$V_{NO} = V_+$ or GND, Switch OFF, See <a href="#">Figure 15</a>	25°C	1.8 V		10.5		pF
NO ON capacitance	$C_{NO(ON)}$	$V_{NO} = V_+$ or GND, Switch ON, See <a href="#">Figure 15</a>	25°C	1.8 V		17		pF
COM ON capacitance	$C_{COM(ON)}$	$V_{COM} = V_+$ or GND, Switch ON, See <a href="#">Figure 15</a>	25°C	1.8 V		17		pF
Digital input capacitance	$C_I$	$V_I = V_+$ or GND, See <a href="#">Figure 15</a>	25°C	1.8 V		3		pF
Bandwidth	BW	$R_L = 50\ \Omega$ , Switch ON, See <a href="#">Figure 18</a>	25°C	1.65 V to 1.95 V		341		MHz
OFF isolation	$O_{ISO}$	$R_L = 50\ \Omega$ , $f = 10\text{ MHz}$ , Switch OFF, See <a href="#">Figure 19</a>	25°C	1.65 V to 1.95 V		-81		dB
Crosstalk	$X_{TALK}$	$R_L = 50\ \Omega$ , $f = 10\text{ MHz}$ , Switch ON, See <a href="#">Figure 20</a>	25°C	1.65 V to 1.95 V		-61		dB
<b>Supply</b>								
Positive supply current	$I_+$	$V_I = V_+$ or GND, Switch ON or OFF	25°C	1.95 V			1	$\mu\text{A}$
			Full				10	

## 7.9 Typical Characteristics



Typical Characteristics (continued)

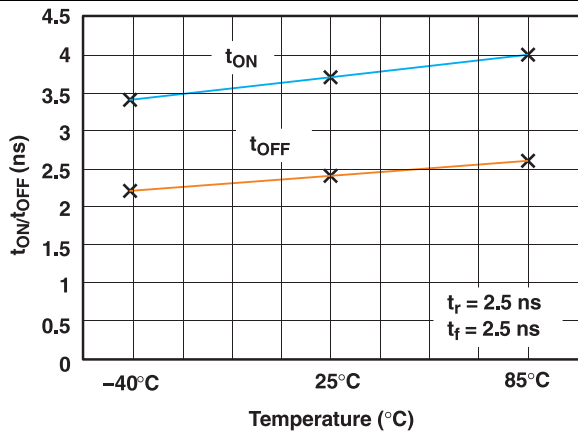


Figure 7. t<sub>ON</sub> and t<sub>OFF</sub> vs Temperature (V<sub>+</sub> = 5 V)

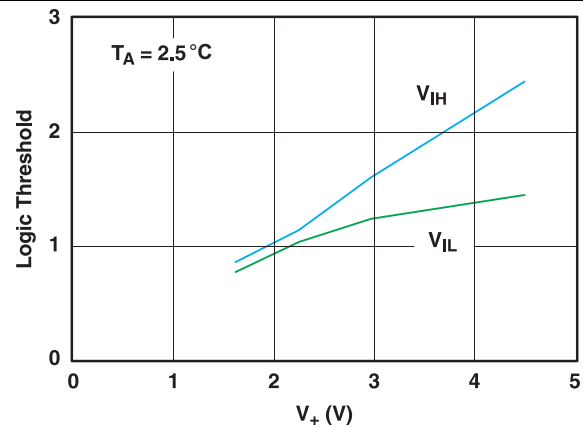


Figure 8. Logic-Level Threshold vs V<sub>+</sub>

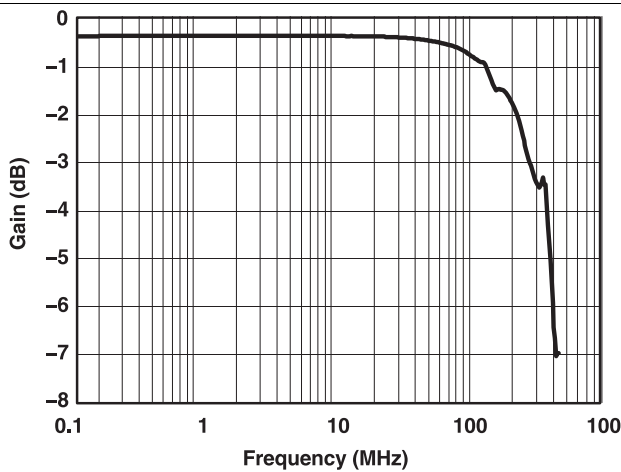


Figure 9. Frequency Response (V<sub>+</sub> = 3 V)

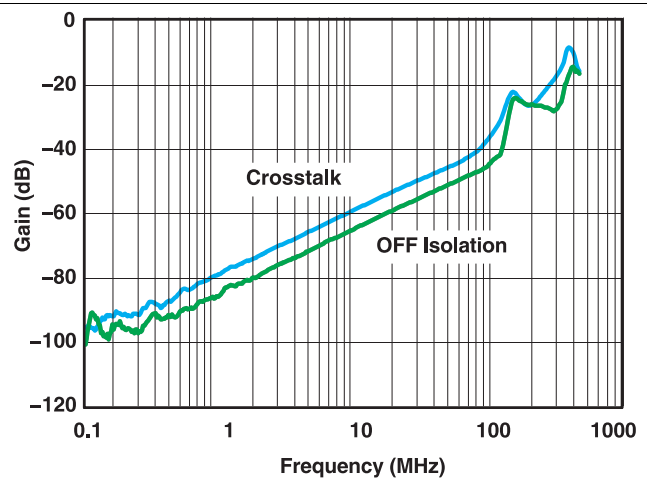


Figure 10. OFF Isolation and Crosstalk vs Frequency (V<sub>+</sub> = 3 V)

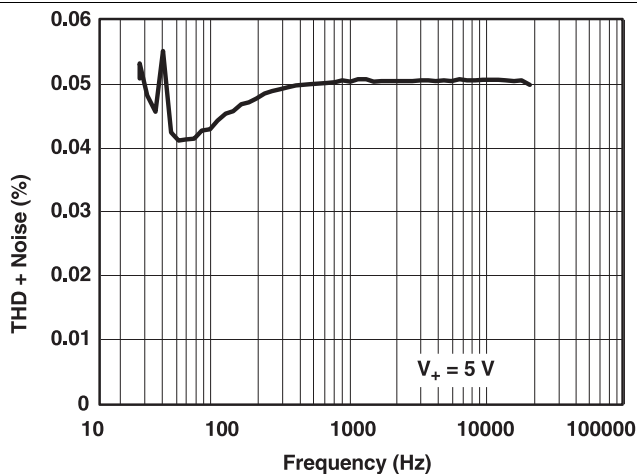


Figure 11. Total Harmonic Distortion vs Frequency (V<sub>+</sub> = 5 V)

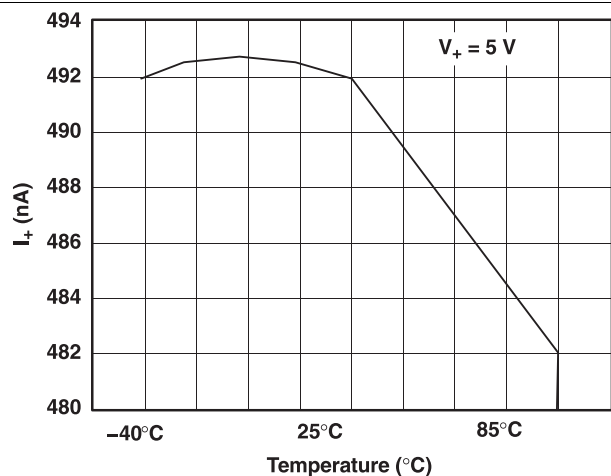


Figure 12. Power-Supply Current vs Temperature (V<sub>+</sub> = 5 V)

## 8 Parameter Measurement Information

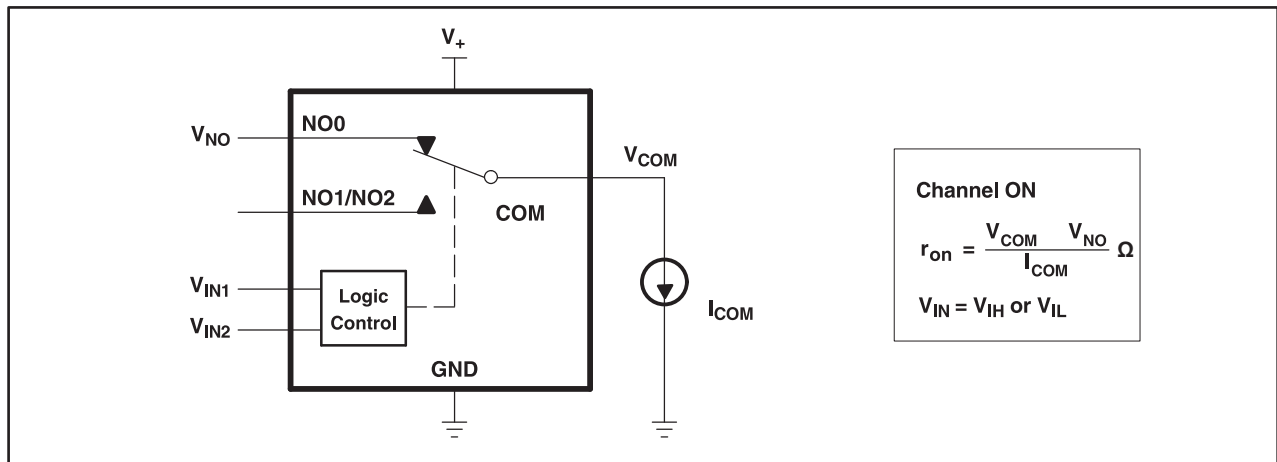


Figure 13. ON-State Resistance ( $r_{on}$ )

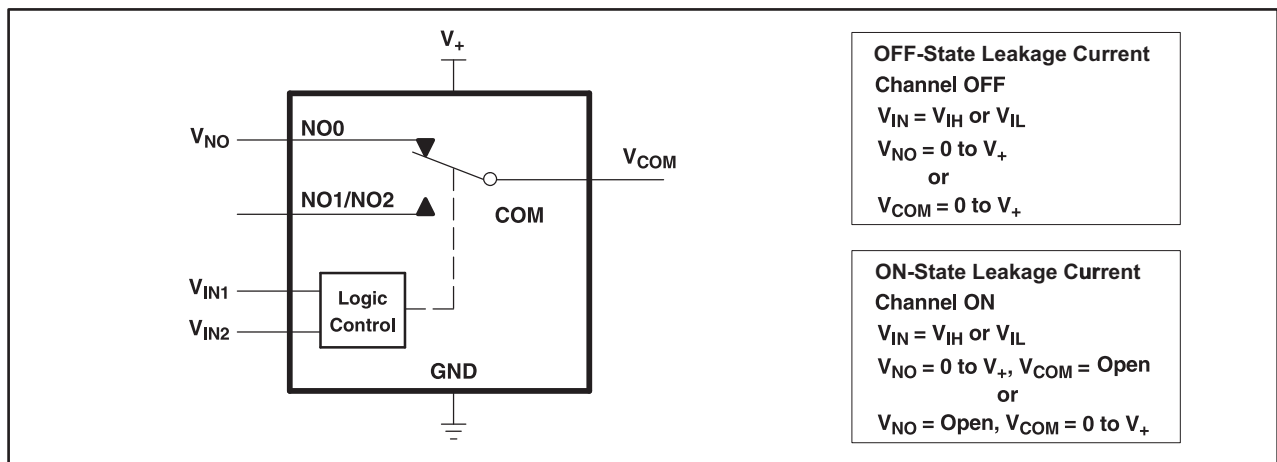


Figure 14. ON- and OFF-State Leakage Current ( $I_{COM(ON)}$ ,  $I_{COM(OFF)}$ ,  $I_{NO(ON)}$ ,  $I_{NO(OFF)}$ )

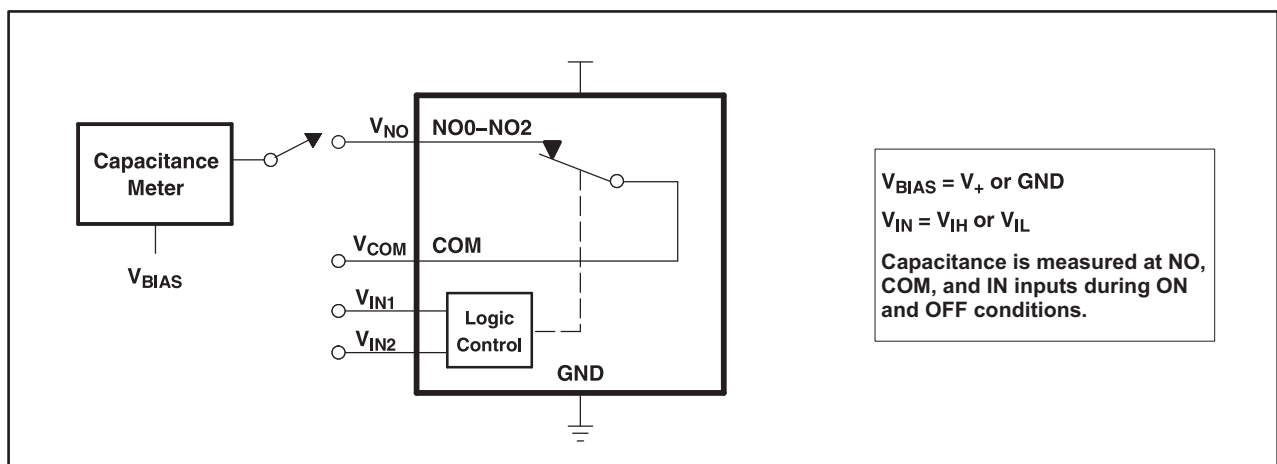
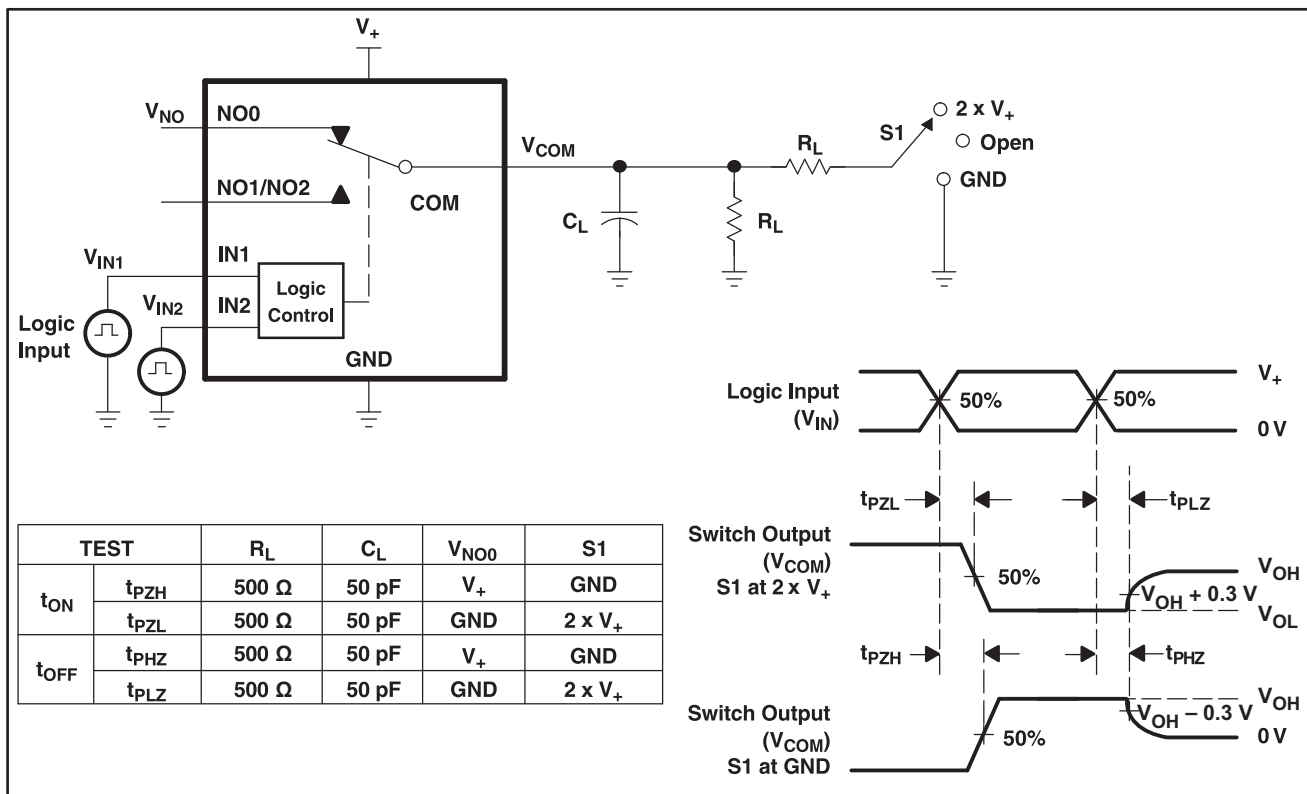


Figure 15. Capacitance ( $C_I$ ,  $C_{COM(ON)}$ ,  $C_{NO(OFF)}$ ,  $C_{COM(OFF)}$ ,  $C_{NO(ON)}$ )

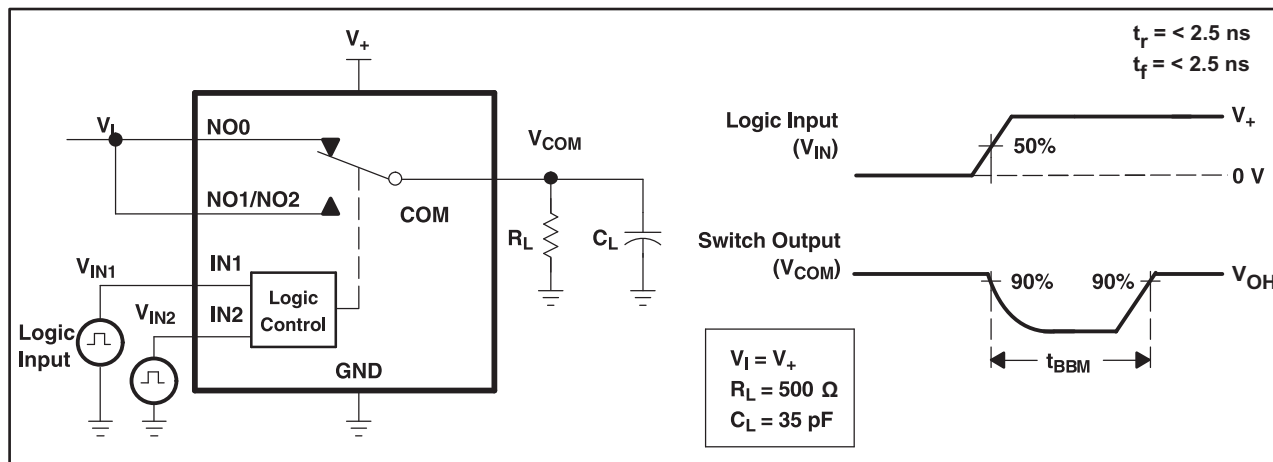


Parameter Measurement Information (continued)



- A. All input pulses are supplied by generators having the following characteristics: PRR  $\leq$  10 MHz,  $Z_O = 50 \Omega$ ,  $t_r < 5$  ns,  $t_f < 5$  ns.
- B.  $C_L$  includes probe and jig capacitance.

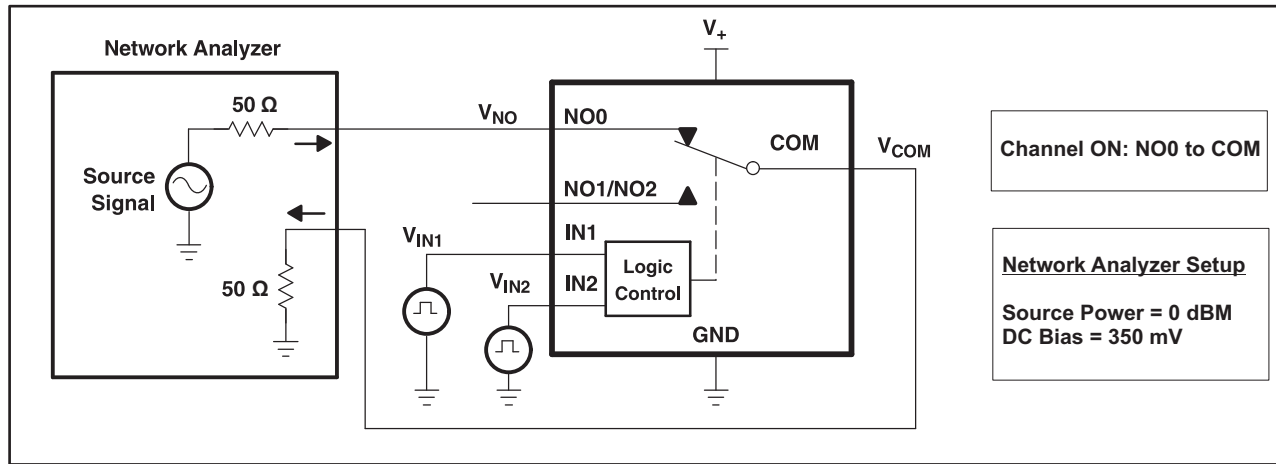
Figure 16. Turn-On ( $t_{ON}$ ) and Turn-Off Time ( $t_{OFF}$ )



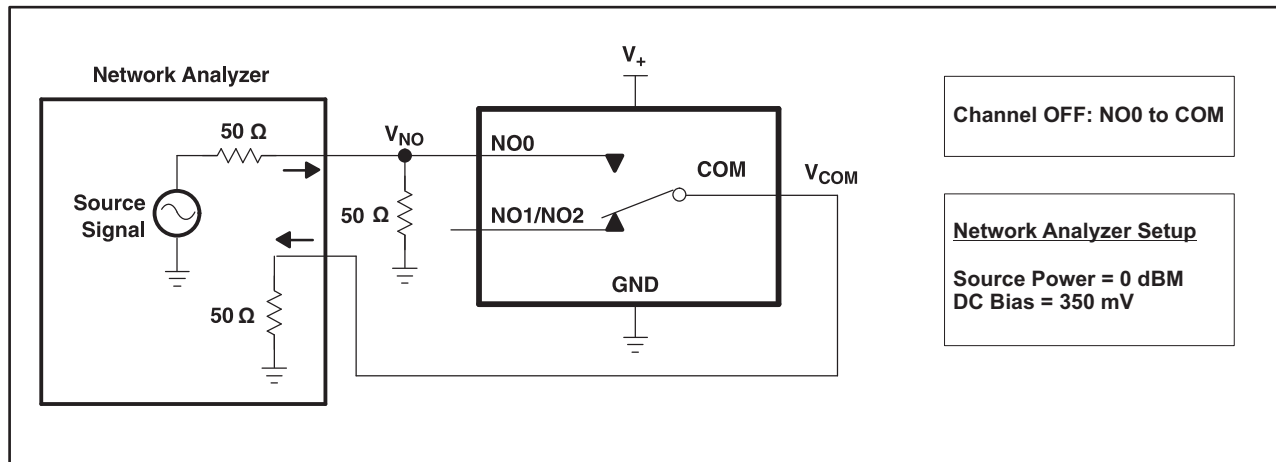
- A. All input pulses are supplied by generators having the following characteristics: PRR  $\leq$  10 MHz,  $Z_O = 50 \Omega$ ,  $t_r < 5$  ns,  $t_f < 5$  ns.
- B.  $C_L$  includes probe and jig capacitance.

Figure 17. Break-Before-Make Time ( $t_{BBM}$ )

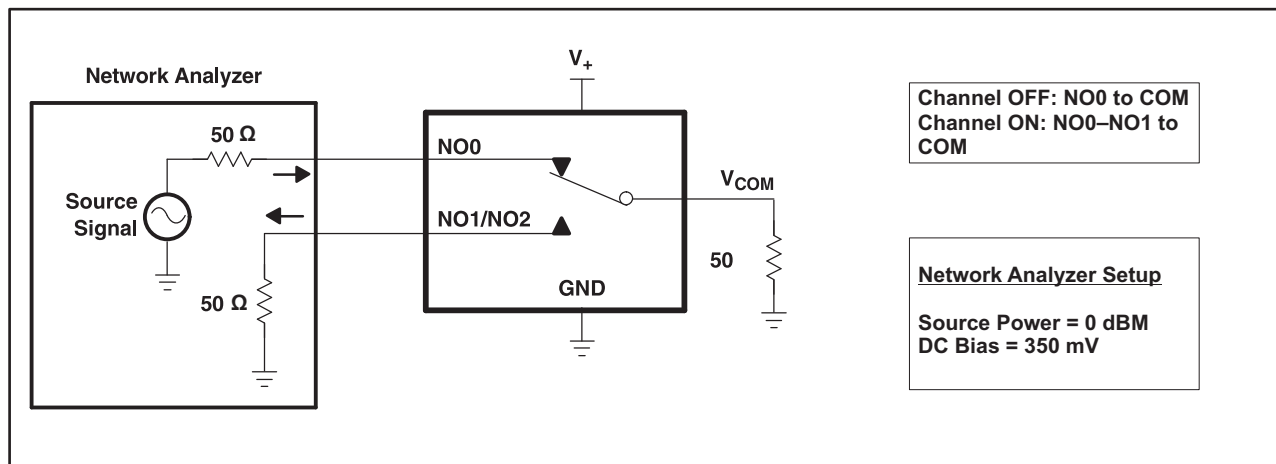
**Parameter Measurement Information (continued)**



**Figure 18. Bandwidth (BW)**

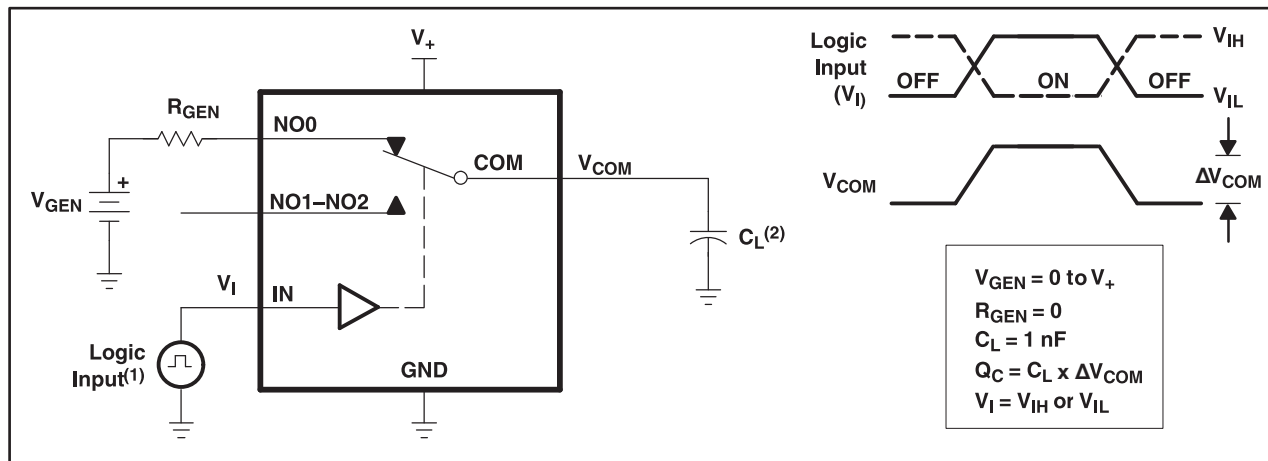


**Figure 19. OFF Isolation ( $O_{ISO}$ )**



**Figure 20. Crosstalk ( $X_{TALK}$ )**

Parameter Measurement Information (continued)



- A. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z<sub>O</sub> = 50 Ω, t<sub>r</sub> < 5 ns, t<sub>f</sub> < 5 ns.
- B. C<sub>L</sub> includes probe and jig capacitance.

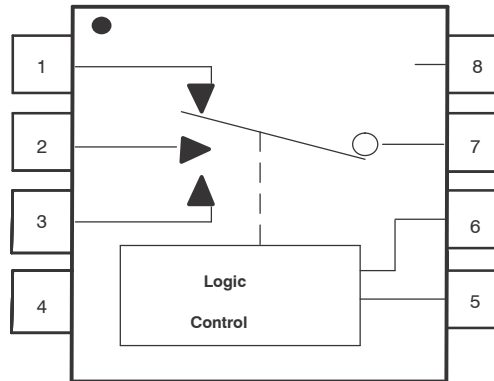
Figure 21. Charge Injection (Q<sub>C</sub>)

## 9 Detailed Description

### 9.1 Overview

The TS5A3357 is a bidirectional, single-channel, 3:1 analog switch that is designed to operate from 1.65 V to 5.5 V. This device provides a signal switching solution while maintaining excellent signal integrity, which makes the TS5A3357 suitable for a wide range of applications in various markets including personal electronics, portable instrumentation, and test and measurement equipment. The device maintains the signal integrity by its low ON-state resistance, excellent ON-state resistance matching, and total harmonic distortion (THD) performance. To prevent signal distortion during the transferring of a signal from one channel to another, the TS5A3357 device also has a specified break-before-make feature.

### 9.2 Functional Block Diagram



### 9.3 Feature Description

Break-before-make

Break-before-make is a safety feature that prevents two inputs from connecting when the TS5A3357 is switching. The TS5A3357 COM pin first breaks from the on-state switch before making the connection with the next on-state switch. The time delay between the break and the make is known as a break-before-make delay  $t_{BBM}$ .

### 9.4 Device Functional Modes

The digital control pins IN1 and IN2 determine the state of the connection between the COM and NO pins based on the truth table below.

Table 2. Function Table

IN1	IN2	COM TO NO0	COM TO NO1	COM TO NO2
L	L	OFF	OFF	OFF
H	L	ON	OFF	OFF
L	H	OFF	ON	OFF
H	H	OFF	OFF	ON

## 10 Application and Implementation

### NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

### 10.1 Application Information

#### 10.2 Typical Application

The TS5A3357 switch is bidirectional, so the NO and COM pins can be used as either inputs or outputs. This switch is typically used when there is only one signal path that needs to be able to communicate to 3 different signal paths.

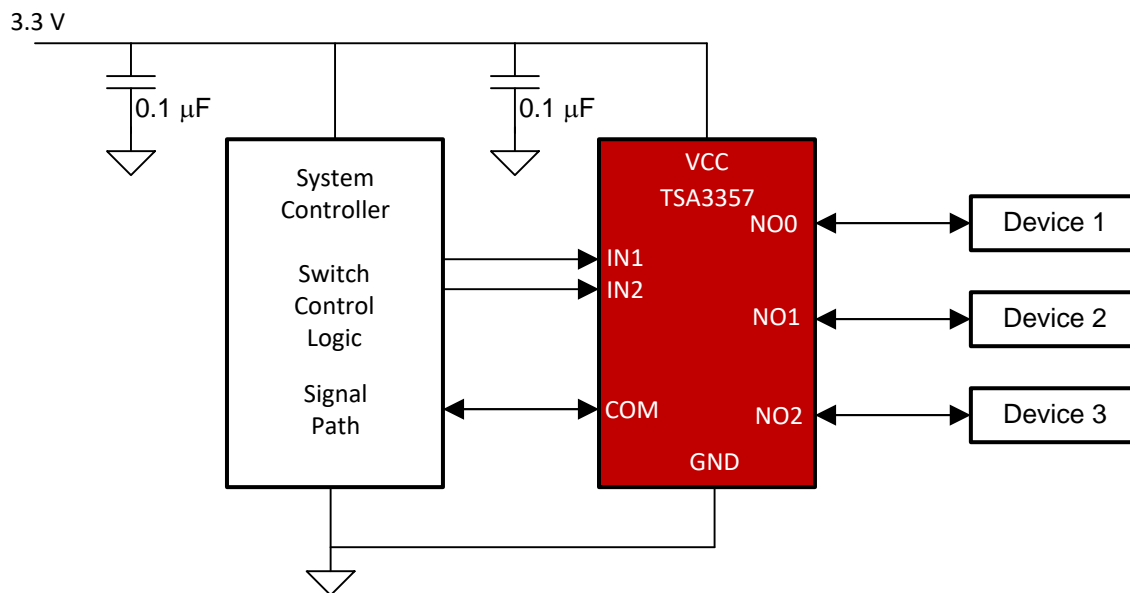


Figure 22. Typical Application Schematic

#### 10.2.1 Design Requirements

The TS5A3357 device can be properly operated without any external components. However, TI recommends connecting unused pins to ground through a 50-Ω resistor to prevent signal reflections back into the device. TI also recommends pulling up the digital control pins (IN1 and IN2) to VCC or pulling down to GND to avoid undesired switch positions that could result from the floating pin.

#### 10.2.2 Detailed Design Procedure

Select the appropriate supply voltage to cover the entire voltage swing of the signal passing through the switch because the TS5A3357 input and output signal swing through NO and COM are dependent on the supply voltage  $V_+$ . For example, if the desired signal level to pass through the switch is 5 V, VCC must be greater than or equal to 5 V.  $V_+ = 3.3$  V would not be valid for passing a 5-V signal since the Analog signal voltage cannot exceed the supply.

## Typical Application (continued)

### 10.2.3 Application Curves

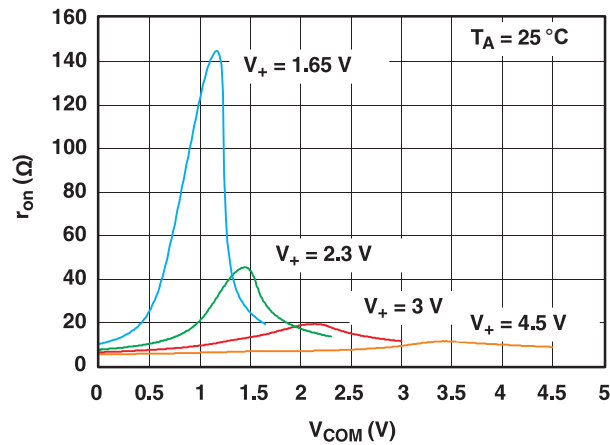


Figure 23.  $r_{on}$  vs  $V_{COM}$

## 11 Power Supply Recommendations

TI recommends proper power-supply sequencing for all CMOS devices. Do not exceed the absolute maximum ratings, because stresses beyond the listed ratings can cause permanent damage to the device. Always sequence  $V_+$  on first, followed by NO or COM. Although it is not required, power-supply bypassing improves noise margin and prevents switching noise propagation from the  $V_+$  supply to other components. A 0.1- $\mu$ F capacitor, connected from VCC to GND, is adequate for most applications.

## 12 Layout

### 12.1 Layout Guidelines

TI recommends following common printed-circuit board layout guidelines to ensure reliability of the device. Bypass capacitors should be used on power supplies. Short trace lengths should be used to avoid excessive loading.

### 12.2 Layout Example

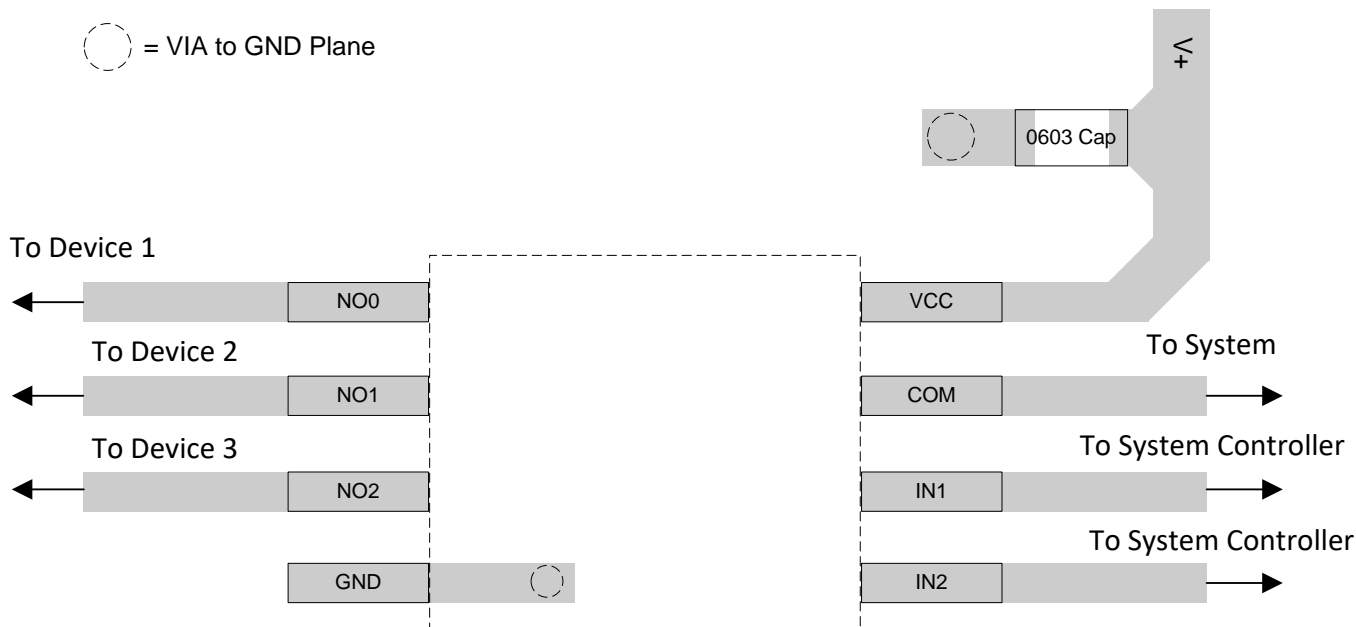


Figure 24. Example Layout

## 13 Device and Documentation Support

### 13.1 Device Support

### 13.2 Documentation Support

### 13.3 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

### 13.4 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's [Terms of Use](#).

**TI E2E™ Online Community** *TI's Engineer-to-Engineer (E2E) Community*. Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

**Design Support** *TI's Design Support* Quickly find helpful E2E forums along with design support tools and contact information for technical support.

### 13.5 Trademarks

E2E is a trademark of Texas Instruments.

### 13.6 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

### 13.7 Glossary

[SLYZ022](#) — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

## 14 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.



**PACKAGING INFORMATION**

Orderable part number	Status (1)	Material type (2)	Package   Pins	Package qty   Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
<a href="#">TS5A3357DCUR</a>	Active	Production	VSSOP (DCU)   8	3000   LARGE T&R	Yes	NIPDAU   SN	Level-1-260C-UNLIM	-40 to 85	(JA9Q, JA9R)
TS5A3357DCUR.B	Active	Production	VSSOP (DCU)   8	3000   LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 85	(JA9Q, JA9R)
<a href="#">TS5A3357DCURG4</a>	Active	Production	VSSOP (DCU)   8	3000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	JA9R
TS5A3357DCURG4.B	Active	Production	VSSOP (DCU)   8	3000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	JA9R

(1) **Status:** For more details on status, see our [product life cycle](#).

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

**Important Information and Disclaimer:** The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

**OTHER QUALIFIED VERSIONS OF TS5A3357 :**

- Automotive : [TS5A3357-Q1](#)

NOTE: Qualified Version Definitions:

- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects

**TAPE AND REEL INFORMATION**

**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TS5A3357DCUR	VSSOP	DCU	8	3000	178.0	9.0	2.25	3.35	1.05	4.0	8.0	Q3
TS5A3357DCURG4	VSSOP	DCU	8	3000	180.0	8.4	2.25	3.35	1.05	4.0	8.0	Q3

**TAPE AND REEL BOX DIMENSIONS**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TS5A3357DCUR	VSSOP	DCU	8	3000	180.0	180.0	18.0
TS5A3357DCURG4	VSSOP	DCU	8	3000	202.0	201.0	28.0



# EXAMPLE BOARD LAYOUT

DCU0008A

VSSOP - 0.9 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE  
EXPOSED METAL SHOWN  
SCALE: 25X



4225266/A 09/2014

NOTES: (continued)

- 5. Publication IPC-7351 may have alternate designs.
- 6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

# EXAMPLE STENCIL DESIGN

DCU0008A

VSSOP - 0.9 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE  
BASED ON 0.125 mm THICK STENCIL  
SCALE: 25X

4225266/A 09/2014

NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

## IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATASHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES "AS IS" AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, regulatory or other requirements.

These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you fully indemnify TI and its representatives against any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI's products are provided subject to [TI's Terms of Sale](#), [TI's General Quality Guidelines](#), or other applicable terms available either on [ti.com](http://ti.com) or provided in conjunction with such TI products. TI's provision of these resources does not expand or otherwise alter TI's applicable warranties or warranty disclaimers for TI products. Unless TI explicitly designates a product as custom or customer-specified, TI products are standard, catalog, general purpose devices.

TI objects to and rejects any additional or different terms you may propose.

Copyright © 2026, Texas Instruments Incorporated

Last updated 10/2025