TSD5402-Q1 8W High-Efficiency Automotive Sensor Driver Amplifier with Integrated Protections and I2C Diagnostics

1 Features

- AEC-Q100 Qualified for automotive applications
  - Temperature grade 1: –40°C to 125°C, T_A
- Mono BTL Digital power amplifier
- 8W Output power at 10% THD+N into 4Ω
- 4.5V to 18V Operating range
- 83% Efficiency into 4Ω
- Differential analog input
- Power Guard protection (adjustable voltage limiter)
- 75dB Power-supply rejection ratio (PSRR)
- Load diagnostic functions:
  - Open and shorted output load
  - Output-to-power and output-to-ground shorts
- Protection and monitoring functions:
  - Short-circuit protection
  - 40V Load dump protection per ISO-7637-2
  - Output DC Level detection
  - Overtemperature protection
  - Overvoltage and Undervoltage protection
- Thermally enhanced 16-Pin HTSSOP (PWP) package with PowerPAD™ package (pad down)
- Designed for automotive EMC requirements
- ISO9000: 2002 TS16949 certified
- 40V Load dump protection in standby
- Non-blocking I^2C in standby

2 Applications

- Resolver-based automotive and industrial applications
- HEV/EV inverter & motor control
- Electric power steering (EPS)
- Rearview mirror module
- Automotive eMirrors
- Servo drive power stage module
- Flight control system

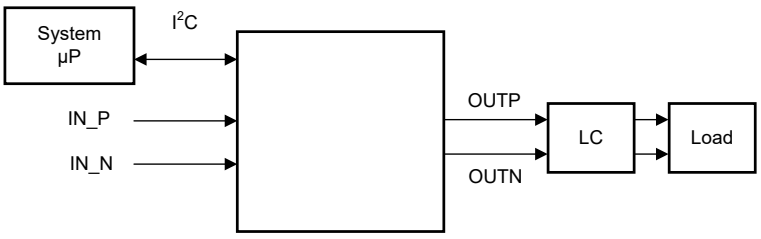
3 Description

The TSD5402-Q1 is a class-D sensor driving amplifier, ideal for use in automotive and industrial applications, including, but not limited to: resolver-based motor control, braking systems, electric power steering, servos, and flight control surfaces. The wide operating voltage range and excellent efficiency make the device ideal for applications that require design flexibility. The integrated load-dump protection reduces external voltage clamp cost and size, and the onboard load diagnostics report the status of the load through I^2C. The integrated shorted load and open load diagnostics allows systems to avoid external implementations.

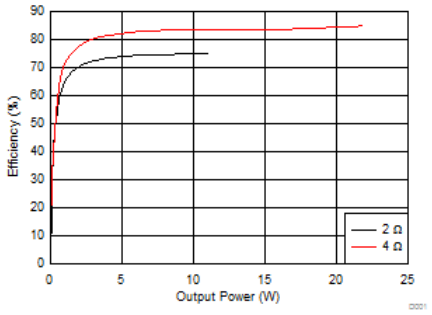
Device Information

PART NUMBER	PACKAGE(1)	PACKAGE SIZE(2)
TSD5402-Q1	HTSSOP (16)	5.0mm × 6.4mm

(1) For all available packages, see the orderable addendum at the end of the datasheet.
(2) The package size (length × width) is a nominal value and includes pins, where applicable.



Simplified Block Diagram



Output Power Efficiency

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4 Pin Configuration and Functions

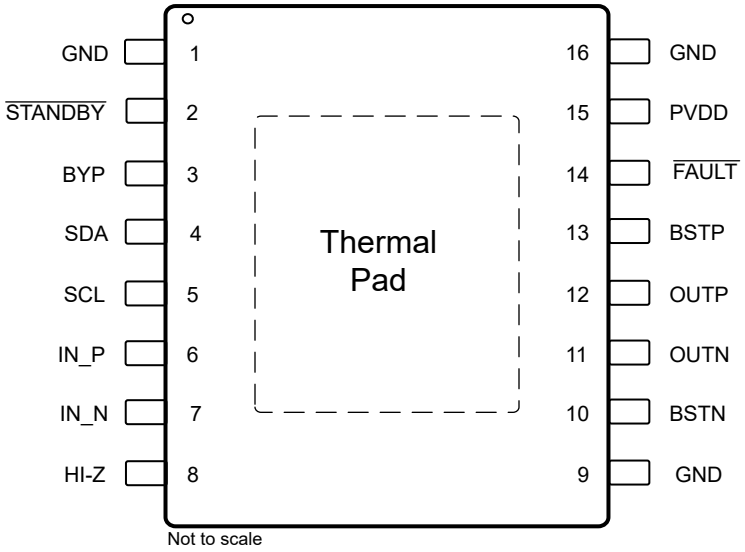


Figure 4-1. PWP Package, 16-Pin, TSSOP With Exposed Thermal Pad (Top View)

Table 4-1. Pin Functions

PIN		TYPE[1]	DESCRIPTION
NAME	NO.		
BSTN	10	AI	Bootstrap for negative-output high-side FET
BSTP	13	AI	Bootstrap for positive-output high-side FET
BYP	3	PBY	Voltage-regulator bypass-capacitor pin
$\overline{\text{FAULT}}$	14	DO	Active-low open-drain output used to report faults
GND	1, 9, 16	GND	Ground
IN_N	7	AI	Inverting analog input
IN_P	6	AI	Non-inverting analog input
HI-Z	8	DI	Stops output switching in DRIVE mode, active-high (no internal pullup or pulldown)
OUTN	11	PO	Output (–)
OUTP	12	PO	Output (+)
PVDD	15	PWR	Power supply
SCL	5	DI	I^2C clock
SDA	4	DI/DO	I^2C data
$\overline{\text{STANDBY}}$	2	DI	Active-low STANDBY pin (no internal pullup or pulldown)
Thermal pad	—	—	Must be soldered to ground

(1) DI = digital input, DO = digital output, AI = analog input, PWR = power supply, PBY = power bypass, PO = power output, GND = ground

5 Specifications

5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted) (1)

			MIN	MAX	UNIT
Input voltage	DC supply voltage range, $V_{(PVDD)}$	Relative to GND	–0.3	30	V
	Pulsed supply voltage range, $V_{(PVDD\_MAX)}$	t ≤ 400 ms exposure	–1	40	
	Supply voltage ramp rate, $\Delta V_{(PVDD\_RAMP)}$			15	V/ms
	For SCL, SDA, and $\overline{\text{STANDBY}}$, $\overline{\text{FAULT}}$ pins	Relative to GND	–0.3	5	V
	For IN_N, IN_P, and HI-Z pins	Relative to GND	–0.3	6.5	
	BYP	Relative to GND	–0.3	7	
	BSTN, BSTP	Relative to BYP	–0.3	30	
	BSTN, BSTP	Relative to GND	–0.3	36.3	
	OUTN, OUTP	Relative to GND	–0.3	30	
Current	DC current on PVDD, GND and OUTx pins, $I_{(PVDD)}$, I_O			±4	A
	Maximum current, on all input pins, $I_{(IN\_MAX)}$ (2)			±1	mA
	Maximum sink current for open-drain pin, $I_{(IN\_ODMAX)}$			7	
Storage temperature, T_{stg}			–55	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

(2) See the section for information on analog input voltage and ac coupling.

5.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per AEC Q100-002(1) HBM ESD Classification Level H2	±3500	V
		Charged-device model (CDM), per AEC Q100-011 CDM ESD Classification Level C5	±1000	

(1) AEC Q100-002 indicates that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

5.3 Recommended Operating Conditions

			MIN	NOM	MAX	UNIT
$V_{(PVDD\_OP)}$	Supply voltage range relative to GND. Includes ac transients, requires proper decoupling.(3)	4-Ω ±20% load (or higher)	4.5	14.4	18	V
		2-Ω ±20% load	5	14.4	18	
$V_{(PVDD\_RIPPLE)}$	Maximum ripple on PVDD	$V_{(PVDD)}$ < 8 V			1	V_{pp}
$V_{(HI-Z)}$	HI-Z pin voltage range relative to GND		-0.3	3.3	5.5	V
$V_{(AIN)}$ (1)	Analog input-signal level	AC-coupled input voltage	0		0.25–1(2)	Vrms
$V_{(IH\_STANDBY)}$	HI-Z and $\overline{\text{STANDBY}}$ pins input voltage for logic-level high		2			V
$V_{(IL\_STANDBY)}$	HI-Z and $\overline{\text{STANDBY}}$ pins input voltage for logic-level low				0.7	V
$V_{(IH\_SCL)}$	SCL pin input voltage for logic-level high	$R_{(PU\_I2C)}$ = 4.7-kΩ pullup, supply voltage = 3.3 V or 5 V	2.1			V
$V_{(IH\_SDA)}$	SDA pin input voltage for logic-level high	$R_{(PU\_I2C)}$ = 4.7-kΩ pullup, supply voltage = 3.3 V or 5 V	2.1			V
$V_{(IL\_SCL)}$	SCL pin input voltage for logic-level low	$R_{(PU\_I2C)}$ = 4.7-kΩ pullup, supply voltage = 3.3 V or 5 V			1.1	V
$V_{(IL\_SDA)}$	SDA pin input voltage for logic-level low	$R_{(PU\_I2C)}$ = 4.7-kΩ pullup, supply voltage = 3.3 V or 5 V			1.1	V
T_A	Ambient temperature		–40		125	°C

			MIN	NOM	MAX	UNIT
$R_{(L)}$	Nominal load impedance	When using low-impedance loads, do not exceed overcurrent limit.	2	4	60	Ω
$V_{(PU)}$	Pullup voltage supply (for open-drain logic outputs)	$V_{(PU)}$ must be less than ($V_{(PVDD)}$ - 1V) during normal operation.	3	3.3	5.5	V
$R_{(PU\_EXT)}$	External pullup resistor on open-drain logic outputs	Resistor connected between open-drain logic output and $V_{(PU)}$ supply.	10		50	kΩ
$R_{(PU\_I2C)}$	I^2C pullup resistance on SDA and SCL pins		1	4.7	10	kΩ
$C_{(PVDD)}$	External capacitor on the PVDD pin, typical value ± 20%(3)			10		µF
$C_{(BYP)}$	External capacitor on the BYP pin, typical value ± 10%			1		µF
$C_{(OUT)}$	External capacitance to GND on OUT_X pins				4	µF
$C_{(IN)}$	External capacitance to analog input pin in series with input signal			1		µF
$C_{(BSTN)}$, $C_{(BSTP)}$	External boostrap capacitor, typical value ± 20%			220		nF

(1) Signal input for full unclipped output with gains of 36dB, 32dB, 26dB, and 20dB
(2) Maximum recommended input voltage is determined by the gain setting.
(3) See the section.

5.4 Thermal Information

THERMAL METRIC(1)		TSD5402 PWP (HTSSOP) 16 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	39.4	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	24.9	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	20	°C/W
ψ_{JT}	Junction-to-top characterization parameter	0.6	°C/W
ψ_{JB}	Junction-to-board characterization parameter	19.8	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	2	°C/W

(1) For more information about traditional and new thermal metrics, see the application report.

5.5 Electrical Characteristics

T_C = 25°C, PVDD = 14.4 V, R_L = 4 Ω, $P_{(O)}$ = 1 W/ch, AES17 filter, default I^2C settings (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
OPERATING CURRENT					
PVDD idle current	In DRIVE mode, no signal present		16		mA
PVDD standby current	STANDBY mode, HI-Z= 0 V		5	20	µA
OUTPUT POWER					
Output power per channel	4 Ω, THD+N ≤ 1%, 1 kHz, T_C = 75°C		6		W
	4 Ω, THD+N = 10%, 1 kHz, T_C = 75°C		8		
Power efficiency	4 Ω, $P_{(O)}$ = 8 W (10% THD)		83%		
OUTPUT PERFORMANCE					
Noise voltage at output	G = 20 dB, zero input, and A-weighting		65		µV
Common-mode rejection ratio	f = 1 kHz, 100 mVrms referenced to GND, G = 20 dB		63		dB
Power-supply rejection ratio	PVDD = 14.4 Vdc + 1 Vrms, f = 1 kHz		75		
Total harmonic distortion + noise	$P_{(O)}$ = 1 W, f = 1 kHz		0.05%		

T_C = 25°C, PVDD = 14.4 V, R_L = 4 Ω, $P_{(O)}$ = 1 W/ch, AES17 filter, default I^2C settings (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Switching frequency	Switching frequency selectable for AM interference avoidance		400		kHz
			500		
Internal common-mode input bias voltage	Internal bias applied to IN_N, IN_P pins		3		V
Voltage gain (V_O / V_{IN})	Source impedance = 0 Ω, register 0x03 bits 7–6 = 00	19	20	21	dB
	Source impedance = 0 Ω, register 0x03 bits 7–6 = 01	25	26	27	
	Source impedance = 0 Ω, register 0x03 bits 7–6 = 10	31	32	33	
	Source impedance = 0 Ω, register 0x03 bits 7–6 = 11	35	36	37	
PWM OUTPUT STAGE					
FET drain-to-source resistance	T_J = 25°C		180		mΩ
Output offset voltage	Zero input signal, G = 20 dB			±25	mV
PVDD OVERVOLTAGE (OV) PROTECTION					
PVDD overvoltage-shutdown set		19.5	21	22.5	V
PVDD overvoltage-shutdown hysteresis			0.6		V
PVDD UNDERVOLTAGE (UV) PROTECTION					
PVDD undervoltage-shutdown set		3.6	4	4.4	V
PVDD undervoltage-shutdown hysteresis			0.25		V
BYP					
BYP pin voltage		6.4	6.9	7.4	V
POWER-ON RESET (POR)					
PVDD voltage for POR				4.1	V
PVDD recovery hysteresis voltage for POR			0.3		V
OVERTEMPERATURE (OT) PROTECTION					
Junction temperature for overtemperature shutdown		155	170		°C
Junction temperature overtemperature shutdown hystersis			15		°C
OVERCURRENT (OC) SHUTDOWN PROTECTION					
Maximum current (peak output current)			2.4		A
$\overline{\text{STANDBY}}$ PIN					
$\overline{\text{STANDBY}}$ pin current			0.1	0.2	µA
DC DETECT					
DC detect threshold			2.9		V
DC detect step response time				700	ms
FAULT REPORT					
$\overline{\text{FAULT}}$ pin output voltage for logic-level high (open-drain logic output)	External 47-kΩ pullup resistor to 3.3 V	2.4			V
$\overline{\text{FAULT}}$ pin output voltage for logic-level low (open-drain logic output)	External 47-kΩ pullup resistor to 3.3 V			0.5	V
LOAD DIAGNOSTICS					
Resistance to detect a short from OUT pin(s) to PVDD or ground				200	Ω
Open-circuit detection threshold	Including load wires	70	95	120	Ω
Short-circuit detection threshold	Including load wires	0.9	1.2	1.5	Ω
I^2C					

T_C = 25°C, PVDD = 14.4 V, R_L = 4 Ω, $P_{(O)}$ = 1 W/ch, AES17 filter, default I^2C settings (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
SDA pin output voltage for logic-level high	$R_{(PU\_I2C)}$ = 4.7-kΩ pullup, supply voltage = 3.3 V or 5 V	2.4			V
SDA pin output voltage for logic-level low	3-mA sink current			0.4	V
Capacitance for SCL and SDA pins				10	pF
Capacitance for SDA pin	STANDBY mode		30		pF

5.6 Timing Requirements for I2C Interface Signals

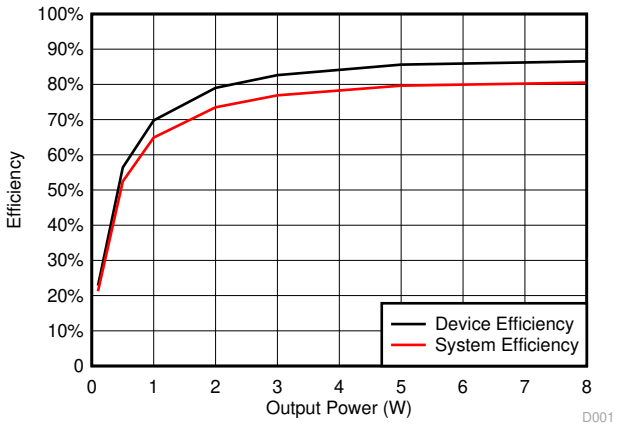
over recommended operating conditions (unless otherwise noted)

		MIN	NOM	MAX	UNIT
$f_{(SCL)}$	SCL clock frequency			400	kHz
t_r	Rise time for both SDA and SCL signals			300	ns
t_f	Fall time for both SDA and SCL signals			300	ns
$t_{w(H)}$	SCL pulse duration, high	0.6			µs
$t_{w(L)}$	SCL pulse duration, low	1.3			µs
$t_{su(2)}$	Setup time for START condition	0.6			µs
$t_{h(2)}$	START condition hold time before generation of first clock pulse	0.6			µs
$t_{su(1)}$	Data setup time	100			ns
$t_{h(1)}$	Data hold time	0(1)			ns
$t_{su(3)}$	Setup time for STOP condition	0.6			µs
$C_{(B)}$	Load capacitance for each bus line			400	pF

(1) A device must internally provide a hold time of at least 300ns for the SDA signal to bridge the undefined region of the falling edge of SCL.

5.7 Typical Characteristics

T_C = 25°C, PVDD = 14.4 V, R_L = 4 Ω, $P_{(O)}$ = 1 W per channel, AES17 filter, 1-kHz input, default I^2C settings (unless otherwise noted)



$f_{(SW)}$ = 400 kHz T_A = 25°C $V_{(PVDD)}$ = 14.4 V

Figure 5-1. Efficiency vs Output Power

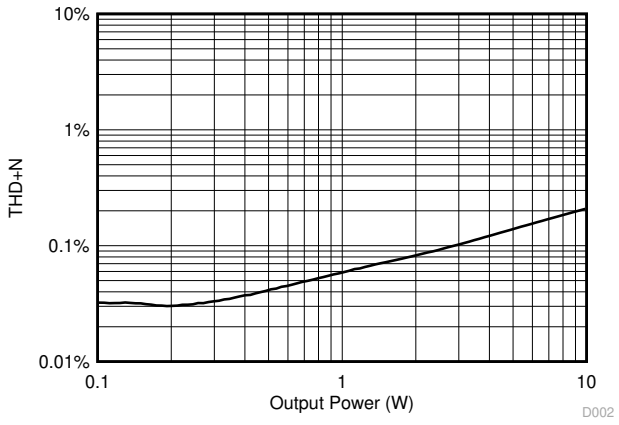


Figure 5-2. THD+N vs Output Power

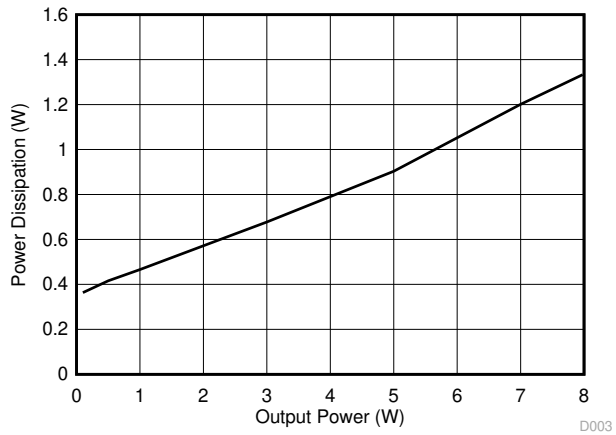


Figure 5-3. Power Dissipation vs Output Power

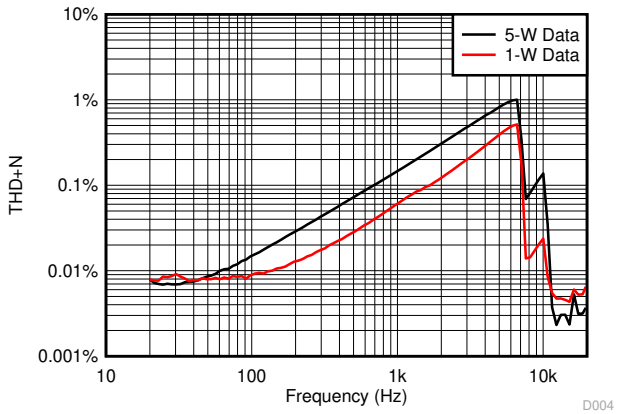


Figure 5-4. THD+N vs Frequency

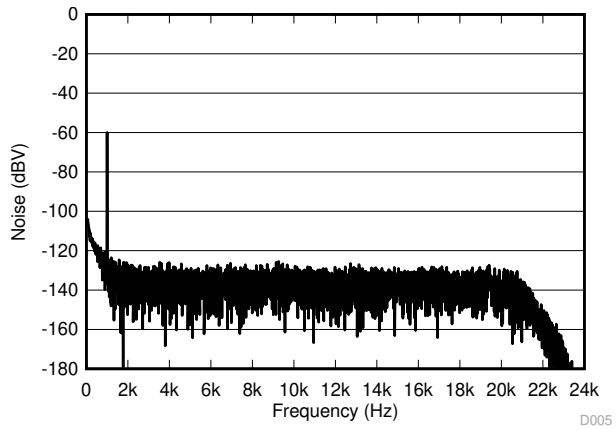


Figure 5-5. Noise FFT With –60-dB Output

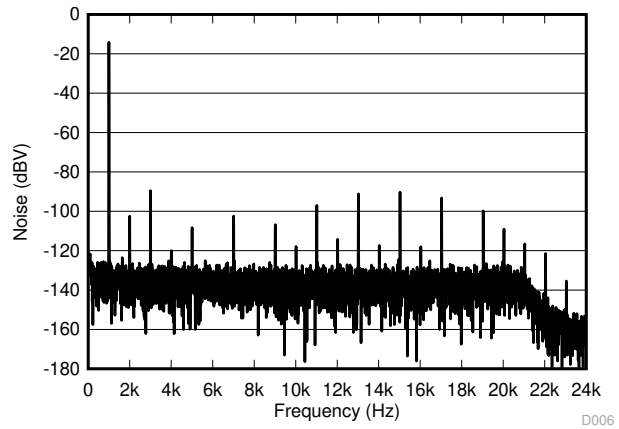


Figure 5-6. Noise FFT With 1-W Output

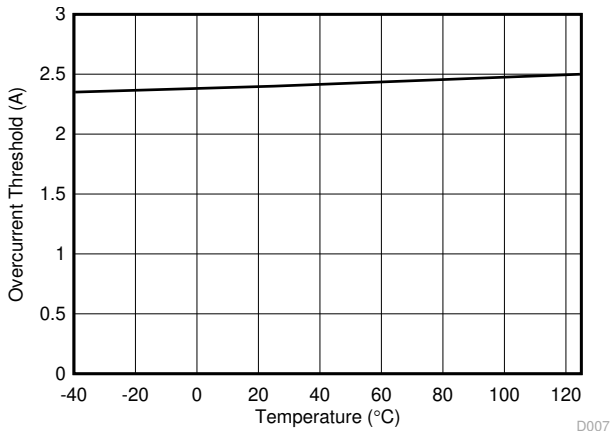


Figure 5-7. Overcurrent Threshold vs Temperature

6 Detailed Description

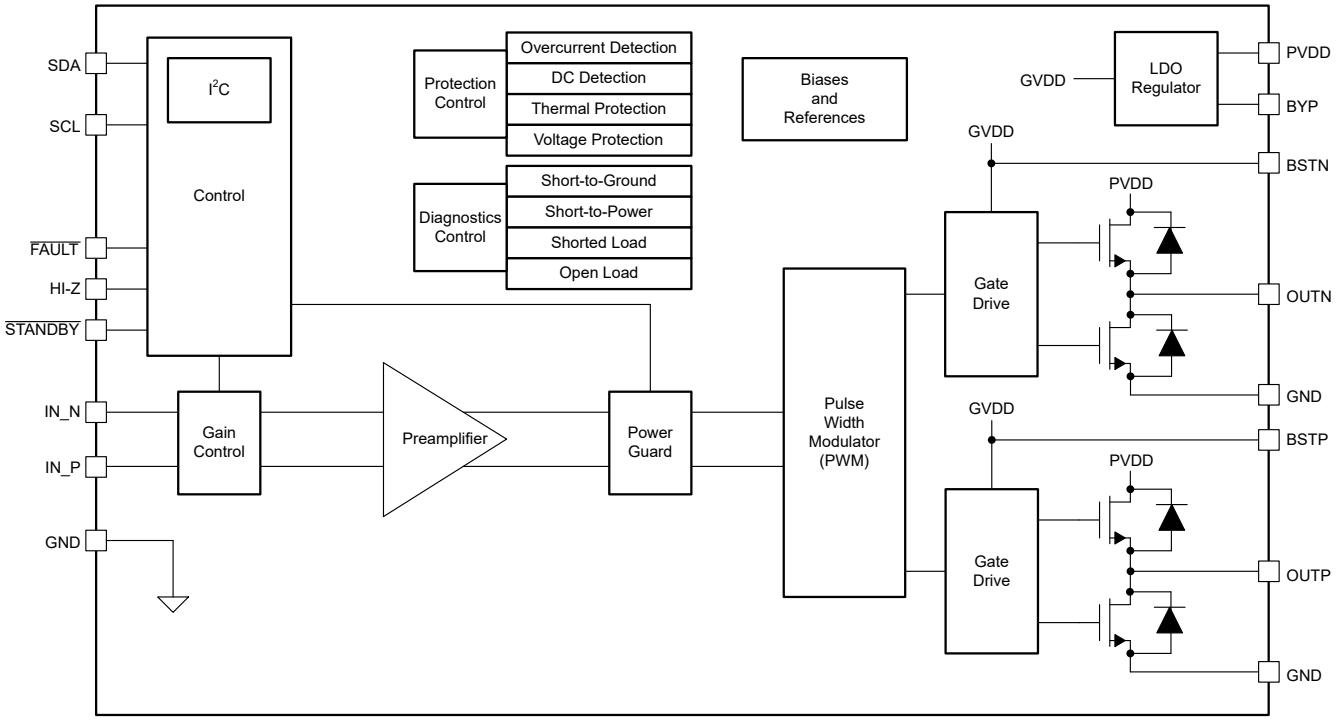
6.1 Overview

The TSD5402-Q1 is an analog-input class-D sensor driving amplifier for use in an automotive/industrial environment. The design uses an ultra-efficient class-D technology developed by Texas Instruments with additional features specific to the automotive industry. The class-D technology allows for reduced power consumption, reduced heat, and reduced peak currents in the electrical system. The device functions as a highly-integrated sensor-driver with smaller size and higher efficiency than traditional class-AB solutions.

The TSD5402-Q1 device has seven core design blocks:

- PWM
- Gate drive
- Power FETs
- Diagnostics
- Protection
- Power supply
- I^2C serial communication bus

6.2 Functional Block Diagram



6.3 Feature Description

6.3.1 Analog Input and Preamplifier

The differential input stage of the amplifier cancels common-mode noise that appears on the inputs. For a differential source, connect the positive lead to IN_P and the negative lead to IN_N. The inputs must be ac-coupled to minimize the output dc-offset and ensure correct ramping of the output voltages. For good transient performance, the impedance seen at each of the two differential inputs should be the same.

The gain setting impacts the analog input impedance of the amplifier. See Input Impedance and Gain for typical values.

Table 6-1. Input Impedance and Gain

Gain	Input Impedance
20dB	60kΩ ± 20%
26dB	30kΩ ± 20%
32dB	15kΩ ± 20%
36dB	9kΩ ± 20%

6.3.2 Pulse-Width Modulator (PWM)

The PWM converts the analog signal from the preamplifier into a switched signal of varying duty cycle. This is the critical stage that defines the class-D architecture. In the TSD5402-Q1, the modulator is an advanced design with high bandwidth, low noise, low distortion, and excellent stability.

The pulse-width modulation scheme allows increased efficiency at low power. Each output is switching from 0 V to PVDD. The OUTP and OUTN pins are in phase with each other with no input so that there is little or no current in the load. The duty cycle of OUTP is greater than 50% and the duty cycle OUTN is less than 50% for positive output voltages. The duty cycle of OUTN is greater than 50% and the duty cycle of OUTP is less than 50% for negative output voltages. The voltage across the load is at 0 V through most of the switching period, reducing power loss.

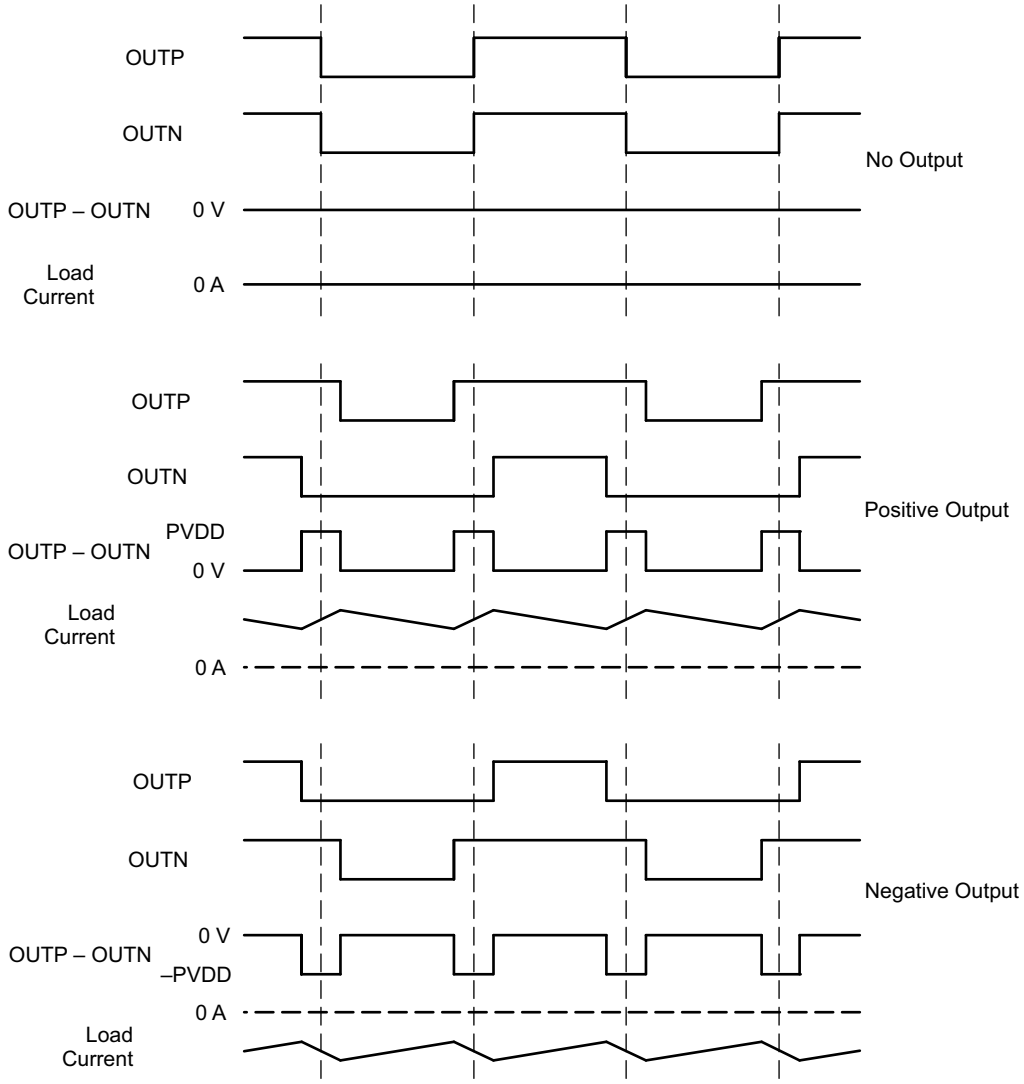


Figure 6-1. BD Mode Modulation

6.3.3 Gate Drive

The gate driver accepts the low-voltage PWM signal and level-shifts the signal to drive a high-current, full-bridge, power FET stage. The device uses proprietary techniques to optimize EMI performance.

6.3.4 Power FETs

The BTL output comprises four matched N-channel FETs for high efficiency and maximum power transfer to the load. By design, the FETs withstand large voltage transients during a load-dump event.

6.3.5 Load Diagnostics

The device incorporates load diagnostic circuitry designed for detecting and determining the status of output connections. The device supports the following diagnostics:

- Short to GND
- Short to PVDD
- Short across load
- Open load

The device reports the presence of any of the short or open conditions to the system via I^2C register read.

6.3.5.1 Load Diagnostics Sequence

The load diagnostic function runs on de-assertion of STANDBY or when the device is in a fault state (dc detect, overcurrent, overvoltage, undervoltage, and overtemperature). During this test, the outputs are in a Hi-Z state. The device determines whether the output is a short to GND, short to PVDD, open load, or shorted load. The load diagnostic biases the output, which therefore requires limiting the capacitance value for proper functioning; see the *Recommended Operating Conditions*. The load diagnostic test takes approximately 229 ms to run. Note that the *check* phase repeats up to five times if a fault is present or a large capacitor to GND is present on the output. On detection of an open load, the output still operates. On detection of any other fault condition, the output goes into a Hi-Z state, and the device checks the load continuously until removal of the fault condition. After detection of a normal output condition, the signal output starts. The load diagnostics run after every other overvoltage (OV) event. The load diagnostic for open load only has I^2C reporting. All other faults have I^2C and $\overline{\text{FAULT}}$ pin assertion.

The device performs load diagnostic tests as shown in Figure 6-2.

Figure 6-3 illustrates how the diagnostics determine the load based on output conditions.

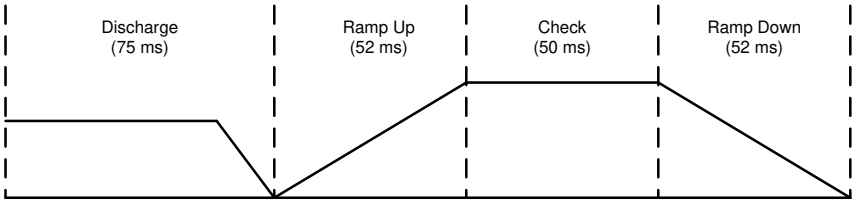


Figure 6-2. Load Diagnostics Sequence of Events

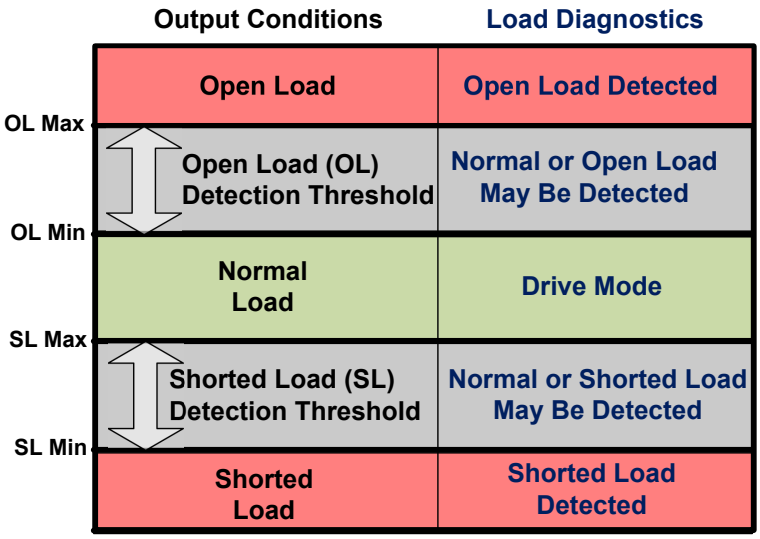


Figure 6-3. Load Diagnostic Reporting Thresholds

6.3.5.2 Faults During Load Diagnostics

If the device detects a fault (such as overtemperature, overvoltage, or undervoltage) during the load diagnostics test, the device exits the load diagnostics, which can result in a pop or click on the output.

6.3.6 Protection and Monitoring

- **Overcurrent Shutdown (OCSD)**—The overcurrent shutdown forces the output into Hi-Z. The device asserts the $\overline{\text{FAULT}}$ pin and updates the I^2C register.
- **DC Detect**—This circuit checks for a dc offset continuously during normal operation at the output of the amplifier. If a dc offset occurs, the device asserts the $\overline{\text{FAULT}}$ pin and updates the I^2C register. Note that the dc detection threshold follows PVDD changes.
- **Overtemperature Shutdown (OTSD)**—The device shuts down when the die junction temperature reaches the overtemperature threshold. The device asserts the $\overline{\text{FAULT}}$ pin asserts and updates I^2C register. Recovery is automatic when the temperature returns to a safe level.
- **Undervoltage (UV)**—The undervoltage (UV) protection detects low voltages on PVDD. In the event of an undervoltage condition, the device asserts the $\overline{\text{FAULT}}$ pin and resets the I^2C register.
- **Power-On Reset (POR)**—Power-on reset (POR) occurs when PVDD drops below the POR threshold. A POR event causes the I^2C bus to go into a high-impedance state. After recovery from the POR event, the device restarts automatically with default I^2C register settings.
- **Overvoltage (OV) and Load Dump**—OV protection detects high voltages on PVDD. If PVDD reaches the overvoltage threshold, the device asserts the $\overline{\text{FAULT}}$ pin and updates the I^2C register. The device can withstand 40-V load-dump voltage spikes. The device supports load-dump in both standby and active modes.
- **Power Guard**—This protection circuitry limits the output voltage to the value selected in I^2C register 0x03. This value determines both the positive and negative limits. The user can use the Power Guard feature to improve battery life or protect the load from exceeding its excursion limits.
- **Adjacent-Pin Shorts**—The device design is such that shorts between adjacent pins do not cause damage.

6.3.7 I^2C Serial Communication Bus

The device communicates with the system processor via the I^2C serial communication bus as an I^2C target-only device. The processor can poll the device via I^2C to determine the operating status. All reports of fault conditions and detections are via I^2C. The system can also set numerous features and operating conditions via I^2C. The I^2C interface is active approximately 1 ms after the $\overline{\text{STANDBY}}$ pin is high.

The I^2C interface controls the following device features:

- Changing gain setting to 20dB, 26dB, 32dB, or 36dB.
- Controlling peak voltage value of Power Guard protection circuitry

- Reporting load diagnostic results
- Changing of switching frequency for AM radio avoidance

6.3.7.1 I²C Bus Protocol

The device has a bidirectional serial control interface that is compatible with the Inter IC (I²C) bus protocol and supports 400kbps data transfer rates for random and sequential write and read operations. This is a target-only device that does not support a multicontroller bus environment or wait-state insertion. The controller device uses the I²C control interface to program the registers of the device and to read device status.

The I²C bus employs two signals, SDA (data) and SCL (clock), to communicate between integrated circuits in a system. Data transfer on the bus is serial, one bit at a time. The transfer of address and data is in byte (8-bit) format with the most-significant bit (MSB) transferred first. In addition, the receiving device acknowledges each byte transferred on the bus with an acknowledge bit. Each transfer operation begins with the controller device driving a start condition on the bus and ends with the controller device driving a stop condition on the bus. The bus uses transitions on the data pin (SDA) while the clock is HIGH to indicate start and stop conditions. A HIGH-to-LOW transition on SDA indicates a start, and a LOW-to-HIGH transition indicates a stop. Normal data bit transitions must occur within the low time of the clock period. Figure 6-4 shows these conditions. The controller generates the 7-bit target address and the read/write (R/ $\overline{W}$) bit to open communication with another device and then waits for an acknowledge condition. The device holds SDA LOW during the acknowledge clock period to indicate an acknowledgment. When this occurs, the controller transmits the next byte of the sequence. The address for each device is a unique 7-bit target address plus a R/ $\overline{W}$ bit (1 byte). All compatible devices share the same signals via a bidirectional bus using a wired-AND connection. The SDA and SCL signals require the use of an external pullup resistor to set the HIGH level for the bus. There is no limit on the number of bytes that the communicating devices can transmit between start and stop conditions. After transfer of the last word, the controller generates a stop condition to release the bus.

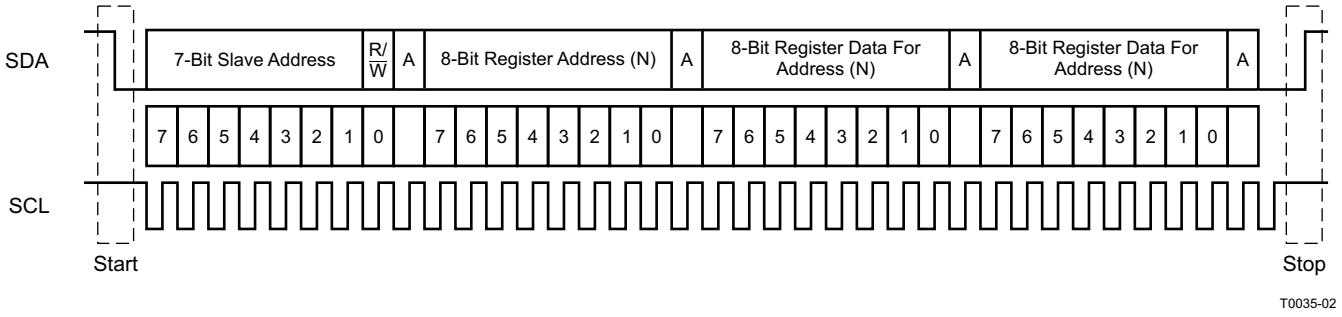


Figure 6-4. Typical I²C Sequence

To communicate with the device, the I²C controller uses addresses shown in Figure 6-4. Transmission of read and write data can be by single-byte or multiple-byte data transfers.

6.3.7.2 Random Write

As shown in Figure 6-5, a single-byte data-write transfer begins with the controller device transmitting a start condition followed by the I²C device address and the read/write bit. The read/write bit determines the direction of the data transfer. For a write data transfer, the read/write bit is a 0. After receiving the correct I²C device address and the read/write bit, the device responds with an acknowledge bit. Next, the controller transmits the address byte corresponding to the internal memory address being accessed. After receiving the address byte, the device again responds with an acknowledge bit. Next, the controller device transmits the data byte for writing to the memory address being accessed. After receiving the data byte, the device again responds with an acknowledge bit. Finally, the controller device transmits a stop condition to complete the single-byte data-write transfer.

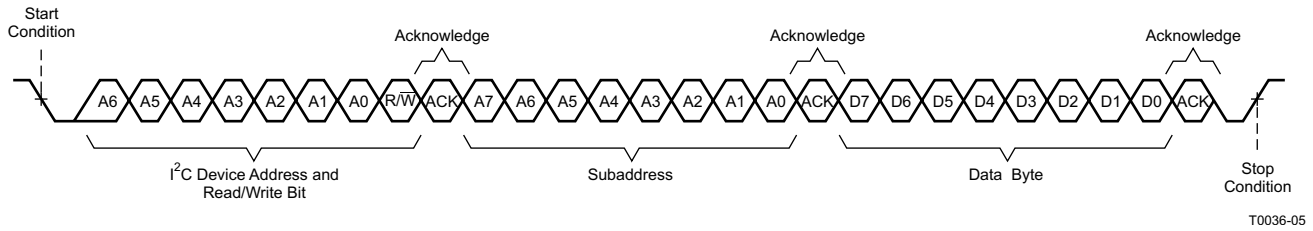


Figure 6-5. Random Write Transfer

6.3.7.3 Random Read

As shown in Figure 6-6, a single-byte data-read transfer begins with the controller device transmitting a start condition followed by the I^2C device address and the read/write bit. For the data-read transfer, the controller device performs both a write and a following read. Initially, the controller device performs a write to transfer the address byte of the internal memory address to be read. As a result, the read/write bit is a 0. After receiving the address and the read/write bit, the device responds with an acknowledge bit. In addition, after sending the internal memory address byte, the controller device transmits another start condition followed by the device address and the read/write bit again. This time, the read/write bit is a 1, indicating a read transfer. After receiving the address and the read/write bit, the device again responds with an acknowledge bit. Next, the device transmits the data byte from the memory address being read. After receiving the data byte, the controller device transmits a not-acknowledge followed by a stop condition to complete the single-byte data-read transfer.

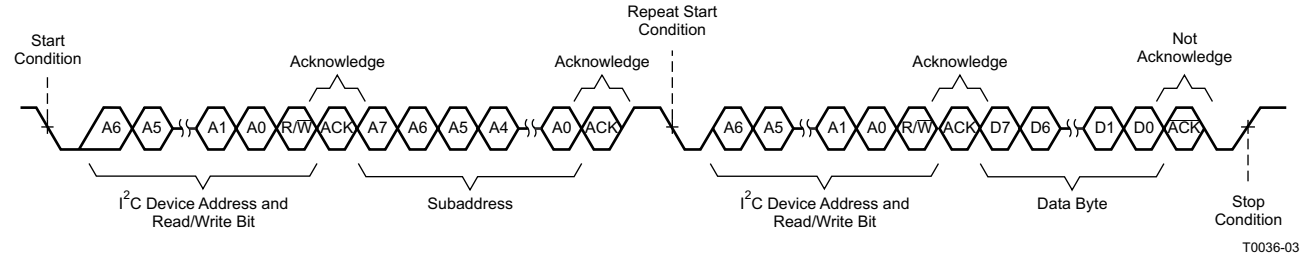


Figure 6-6. Random Read Transfer

6.3.7.4 Sequential Read

A sequential data-read transfer is identical to a single-byte data-read transfer except that the TSD5402-Q1 transmits multiple data bytes to the controller device as shown in Figure 6-7. Except for the last data byte, the controller device responds with an acknowledge bit after receiving each data byte and automatically increments the I^2C subaddress by one. After receiving the last data byte, the controller device transmits a not-acknowledge followed by a stop condition to complete the transfer.

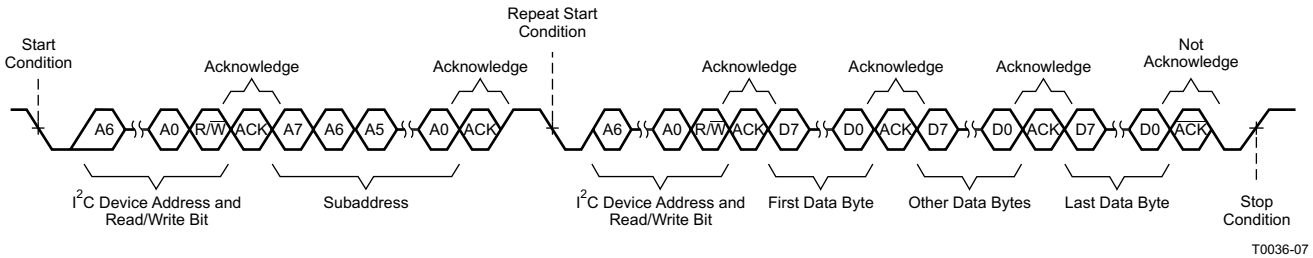


Figure 6-7. Sequential Read Transfer

6.4 Device Functional Modes

6.4.1 Hardware Control Pins

Three discrete hardware pins are available for real-time control and indication of device status.

1. **$\overline{\text{FAULT}}$** pin: This active-low open-drain output pin indicates the presence of a fault condition which requires the device to go into the Hi-Z mode. On assertion of this pin, the device has protected itself and the system from potential damage. The system can read the exact nature of the fault via I^2C with the exception of PVDD undervoltage faults below POR, in which case the I^2C bus is no longer operational.
2. **$\overline{\text{STANDBY}}$** pin: Assertion of this active-low pin sends the device into a complete shutdown, limiting the current draw. Load-dump protection is supported. I^2C is inactive and non-blocking (does not pull I^2C bus low) and the device registers are reset.
3. **HI-Z** pin: On assertion of this active-high pin, the device is in Hi-Z mode. The output pins stop switching and no signal passes from the input to the output. To place the device back into drive mode, deassert this pin. The HI-Z pin should be asserted low when the device is in $\overline{\text{STANDBY}}$.

6.4.2 EMI Considerations

Automotive-level EMI performance depends on both careful integrated-circuit design and good system-level design. Controlling sources of electromagnetic interference (EMI) was a major consideration in all aspects of the design.

The design has minimal parasitic inductances due to the short leads on the package, which dramatically reduces the EMI that results from current passing from the die to the system PCB. The design incorporates circuitry that optimizes output transitions that cause EMI.

6.4.3 Operating Modes and Faults

The following tables list operating modes and faults.

Table 6-2. Operating Modes

STATE NAME	OUTPUT	OSCILLATOR	I^2C (1)
STANDBY	HI-Z, floating	Stopped	Inactive, Registers Reset, Non-blocking
Load diagnostic	DC biased	Active	Active
HI-Z (Hi-Z) / Fault	Hi-Z, floating	Active	Active
DRIVE	Switching with output signal	Active	Active

(1) See SLOA264 for I2C applications.

Table 6-3. Faults and Actions

FAULT EVENT	FAULT EVENT CATEGORY	MONITORING MODES	REPORTING METHOD	ACTION TYPE	ACTION RESULT	CLEARING	STANDBY
POR	Voltage fault	HI-Z (Hi-Z), Drive	Not applicable	Hard stop (no ramp)	Standby	Self-clearing	Disabled
UV			I^2C + $\overline{\text{FAULT}}$ pin		Hi-Z		
OV and Load dump(1)							Protected, No Reporting
OTSD	Thermal fault	HI-Z (Hi-Z), Drive	I^2C + $\overline{\text{FAULT}}$ pin				Disabled
OC fault	Output channel fault	Drive					
DC detect							
Load diagnostic - short	Diagnostic	Hi-Z		None	Hi-Z, re-run diagnostics		
Load diagnostic - open			I^2C		None	Clears on next diagnostic cycle	

(1) Tested in accordance with ISO7637-1

7 Register Maps

Table 7-1. I²C Address

DESCRIPTION	FIXED ADDRESS							READ/WRITE BIT	I²C ADDRESS
	MSB	6	5	4	3	2	1	LSB	
I²C write	1	1	0	1	1	0	0	0	0xD8
I²C read	1	1	0	1	1	0	0	1	0xD9

7.1 I²C Address Register Definitions

Table 7-2. I²C Address Register Definitions

ADDRESS	R/ $\overline{W}$	REGISTER DESCRIPTION
0x01	R	Latched fault register
0x02	R	Status and load diagnostics register
0x03	R/ $\overline{W}$	Control register

Table 7-3. Fault Register (0x01)

D7	D6	D5	D4	D3	D2	D1	D0	FUNCTION
0	0	0	0	0	0	0	0	No protection-created faults, default value
–	–	–	–	–	–	–	1	Reserved
–	–	–	–	–	–	1	–	Reserved
–	–	–	–	–	1	–	–	A load-diagnostics fault has occurred.
–	–	–	–	1	–	–	–	Overcurrent shutdown has occurred.
–	–	–	1	–	–	–	–	PVDD undervoltage has occurred.
–	–	1	–	–	–	–	–	PVDD overvoltage has occurred.
–	1	–	–	–	–	–	–	DC offset protection has occurred.
1	–	–	–	–	–	–	–	Overtemperature shutdown has occurred.

Table 7-4. Status and Load Diagnostic Register (0x02)

D7	D6	D5	D4	D3	D2	D1	D0	FUNCTION
0	0	0	0	0	0	0	0	No load-diagnostic-created faults, default value
–	–	–	–	–	–	–	1	Output short to PVDD is present.
–	–	–	–	–	–	1	–	Output short to ground is present.
–	–	–	–	–	1	–	–	Open load is present.
–	–	–	–	1	–	–	–	Shorted load is present.
–	–	–	1	–	–	–	–	In a fault condition
–	–	1	–	–	–	–	–	Performing load diagnostics
–	1	–	–	–	–	–	–	In Hi-Z mode
1	–	–	–	–	–	–	–	In drive mode

Table 7-5. Control Register (0x03)

D7	D6	D5	D4	D3	D2	D1	D0	FUNCTION
0	1	1	1	1	0	0	0	26dB gain, switching frequency set to 400kHz , Power Guard protection circuitry disabled
–	–	–	–	–	–	–	1	Switching frequency set to 500khz
–	–	–	–	–	1	1	-	Reserved
–	–	1	1	0	–	–	–	Power Guard protection circuitry set to 14V peak output
–	–	1	0	1	–	–	–	Power Guard protection circuitry set to 11.8V peak output
–	–	1	0	0	–	–	–	Power Guard protection circuitry set to 9.8V peak output
–	–	0	1	1	–	–	–	Power Guard protection circuitry set to 8.4V peak output
–	–	0	1	0	–	–	–	Power Guard protection circuitry set to 7V peak output
–	–	0	0	1	–	–	–	Power Guard protection circuitry set to 5.9V peak output
–	–	0	0	0	–	–	–	Power Guard protection circuitry set to 5V peak output
0	0	–	–	–	–	–	–	Gain set to 20dB
1	0	–	–	–	–	–	–	Gain set to 32dB
1	1	–	–	–	–	–	–	Gain set to 36dB

8 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

8.1 Application Information

The device is a high-efficiency sensor driving class-D amplifier. Typical use of the device is to amplify a signal input to drive a sensor. The intent of its use is for a bridge-tied load (BTL) application, not for support of single-ended configuration. This section presents how to use the device in the application, including what external components are necessary and how to connect unused pins.

8.2 Typical Application

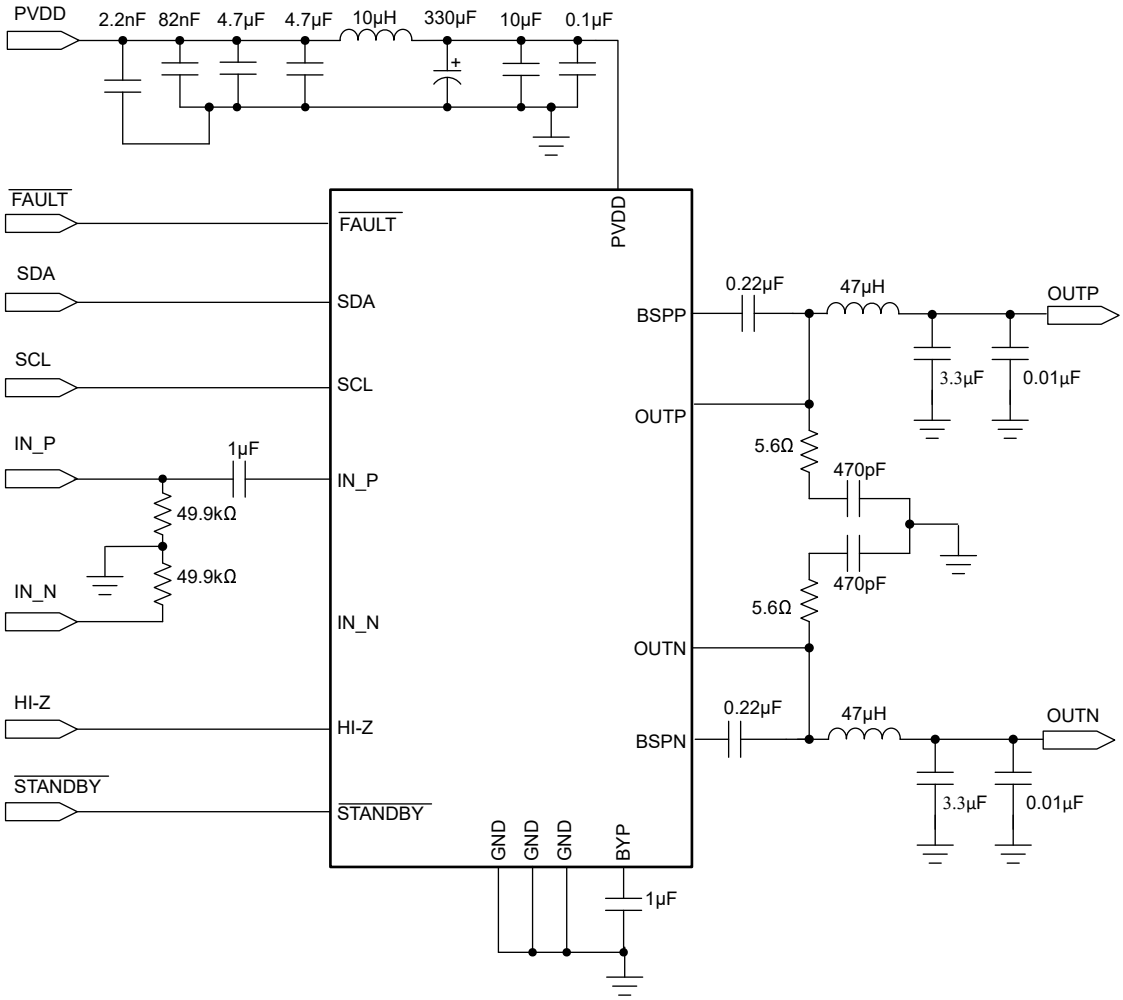


Figure 8-1. TSD5402-Q1 Typical Application Schematic

8.2.1 Design Requirements

Use the following for the design requirements:

Power supplies

- The device requires only a single power supply compliant with the recommended operation range. The device is designed to work with either a vehicle battery or regulated power supply such as from a backup battery.

Communication

- The device communicates with the system controller with both discrete hardware control pins and with I^2C. The device is an I^2C target and thus requires a controller. If a controller I^2C-compliant device is not present in the system, the device can still be used, but only with the default settings. Diagnostic information is limited to the discrete reporting $\overline{\text{FAULT}}$ pin.

External components

- Table 8-1 lists the components required for the device.

Table 8-1. Supporting Components

EVM DESIGNATOR	QUANITY	VALUE	SIZE	DESCRIPTION	USE IN APPLICATION
C7	1	10 µF ± 10%	1206	X7R ceramic capacitor, 25-V	Power supply
C8	1	330 µF ± 20%	10 mm	Low-ESR aluminum capacitor, 25-V	Power supply
C9, C16, C20	3	1 µF ± 10%	0805	X7R ceramic capacitor, 25-V	Analog signal input filter, bypass
C10, C14	2	0.22 µF ± 10%	0603	X7R ceramic capacitor, 25-V	Bootstrap capacitors
C11, C17	2	3.3 µF ± 10%	0805	X7R ceramic capacitor, 25-V	Amplifier output filtering
C13, C15	2	470 pF ± 10%	0603	X7R ceramic capacitor, 250-V	Amplifier output snubbers
C6	1	0.1 µF ± 10%	0603	X7R ceramic capacitor, 25-V	Power supply
C2	1	2200 pF ± 10%	0603	X7R ceramic capacitor, 50-V	Power supply
C3	1	0.082 µF ± 10%	0603	X7R ceramic capacitor, 25-V	Power supply
C4, C5	2	4.7 µF ± 10%	1206	X7R ceramic capacitor, 25-V	Power supply
C12, C18	2	0.01 µF ± 10%	0603	X7R ceramic capacitor, 25-V	Output EMI filtering
L1	1	10 µH ± 20%	13.5 mm ×13.5 mm	Shielded ferrite inductor	Power supply
L2	1	47 µH ± 20%	8 mm × 8 mm	Coupled inductor	Amplifier output filtering
R5, R6	2	49.9 kΩ ± 1%	0805	Resistors, 0.125-W	Analog signal input filter
R4, R7	2	5.6 Ω ± 5%	0805	Resistors, 0.125-W	Output snubbers

8.2.1.1 Amplifier Output Filtering

Output FETs drive the amplifier outputs in an H-bridge configuration. These transistors are either fully off or on. The result is a square-wave output signal with a duty cycle that is proportional to the amplitude of the input signal. The amplifier outputs require a low-pass filter to filter out the PWM modulation carrier frequency. People frequently call this filter the L-C filter, due to the presence of an inductive element L and a capacitive element C to make up the 2-pole low-pass filter. The L-C filter attenuates the carrier frequency, reducing electromagnetic emissions and smoothing the current waveform which the load draws from the power supply. See *Class-D LC Filter Design* for a detailed description on proper component selection and design of an L-C filter based upon the desired load and response.

8.2.1.2 Amplifier Output Snubbers

A snubber is an RC network placed at the output of the amplifier to dampen ringing or overshoot on the PWM output waveform. Overshoot and ringing can have negative impacts including: potential EMI sources and overvoltage stress of the output FETs or board components. For more information on the use and design of output snubbers, see *Class-D Output Snubber Design Guide*.

8.2.1.3 Bootstrap Capacitors

The output stage uses dual NMOS transistors; therefore, the circuit requires bootstrap capacitors for the high side of each output to turn on correctly. The required capacitor connection is from BSTN to OUTN and from BSTP to OUTP as shown in Figure 8-1.

8.2.1.4 Analog Signal Input Filter

The circuit requires an input capacitor to allow biasing of the amplifier put to the proper dc level. The input capacitor and the input impedance of the amplifier form a high-pass filter with a –3-dB corner frequency determined by the equation: $f = 1 / (2\pi R_{(i)} C_{(i)})$, where $R_{(i)}$ is the input impedance of the device based on the gain setting and $C_{(i)}$ is the input capacitor value. Table 8-2 lists largest recommended input capacitor values. Use a capacitor which matches the application requirement for the lowest frequency but does not exceed the values listed.

Table 8-2. Recommended Input AC-Coupling Capacitors

GAIN (dB)	TYPICAL INPUT IMPEDANCE (kΩ)	INPUT CAPACITANCE (µF)	HIGH-PASS FILTER (Hz)
20	60	1	2.7
		1.5	1.8
26	30	1	5.3
		3.3	1.6
32	15	5.6	2.3
36	9	10	1.8

8.2.2 Detailed Design Procedure

Use the following steps for the design procedure:

- Step 1: Hardware Schematic Design: Using the Figure 8-1 as a guide, integrate the hardware into the system schematic.
- Step 2: Following the layout guidelines recommended in the *Section 8.4.1* section, integrate the device and its supporting components into the system PCB file.
- Step 3: Thermal Design: The device has an exposed thermal pad which requires proper soldering. For more information, see *Semiconductor and IC Package Thermal Metrics* and *PowerPAD Thermally Enhanced Package*.
- Step 4: Develop software: The EVM User's Guide has detailed instructions for how to set up the device, interpret diagnostic information, and so forth. For information about control registers, see the *Section 7* section.

For questions and support, go to the E2E forums.

8.2.2.1 Unused Pin Connections

Even if unused, always connect pins to a fixed rail; do not leave them floating. Floating input pins represent an ESD risk, therefore the user must adhere to the following guidance for each pin.

8.2.2.1.1 HI-Z Pin

If the HI-Z pin is unused in the application, connect it to GND through a high-impedance resistor.

8.2.2.1.2 $\overline{\text{STANDBY}}$ Pin

If the $\overline{\text{STANDBY}}$ pin is unused in the application, connect it to a low-voltage rail such as 3.3V or 5V through a high-impedance resistor.

8.2.2.1.3 I²C Pins (SDA and SCL)

If there is no microcontroller in the system, use of the device without I²C communication is possible. In this situation, connect the SDA and SCL pins to 3.3V.

8.2.2.1.4 Terminating Unused Outputs

If the $\overline{\text{FAULT}}$ pin does not report to a system microcontroller in the application, connect it to GND.

8.2.2.1.5 Using a Single-Ended Signal Input

When using a single-ended signal source, ac-ground the negative input through a capacitor equal in value to the input capacitor on the positive input, and apply the signal source to the positive input. For best performance, the ac ground should be at the signal source instead of at the device input if possible.

8.2.3 Application Curves

See the *Typical Characteristcs* section for application performance plots.

Table 8-3. Table of Graphs

GRAPH	FIGURE NO.
Efficiency vs Output Power	Figure 5-1
THD+N vs Output Power	Figure 5-2
Power Dissipation vs Output Power	Figure 5-3
THD+N vs Frequency	Figure 5-4
Noise FFT With –60dB Output	Figure 5-5
Noise FFT With 1-W Output	Figure 5-6
Overcurrent Threshold vs Temperature	Figure 5-7

8.3 Power Supply Recommendations

A car battery that can have a large voltage range most commonly provides power for the device. PVDD, a filtered battery voltage, is the supply for the output FETs and the low-side FET gate driver. Good power-supply decoupling is necessary, especially at low voltage and temperature levels. To meet the PVDD specifications in the *Electrical Characteristics* section, TI uses 10µF and 0.1µF ceramic capacitors near the PVDD pin along with a larger bulk 330µF electrolytic decoupling capacitor.

An internal linear regulator, which powers the analog circuitry, provides the voltage on the BYP pin. This supply requires an external bypass ceramic capacitor at the BYP pin.

8.4 Layout

8.4.1 Layout Guidelines

The EVM layout optimizes for thermal dissipation and EMC performance. The TSD5402-Q1 device has a thermal pad down, and good thermal conduction and dissipation require adequate copper area. Layout also affects EMC performance. TSD5402Q1EVM illustrations form the basis for the layout discussions.

8.4.2 Layout Examples

8.4.2.1 Top Layer

The red boxes around number 1 are the copper ground on the top layer. Soldered directly to the thermal pad, the ground is the first significant thermal dissipation required. There are vias that go to the other layers for further thermal relief, but vias have high thermal resistance. TI recommends that use of the top layer be mostly for thermal dissipation. A further recommendation is short routes from output pins to the second-order LC filter for EMC suppression. The number 2 arrow indicates these short routes for better ECM results. A short route from the PVDD pin to the LC filter from the battery or power source, as indicated by the number 3 arrow, also improves EMC suppression. Route on an outside layer for added current capability. The red box around number 4 indicates the ground plane that is common to both OUTP and OUTN. Place the capacitors of the LC filter in the common ground plane to help with common-mode noise and short ground loops

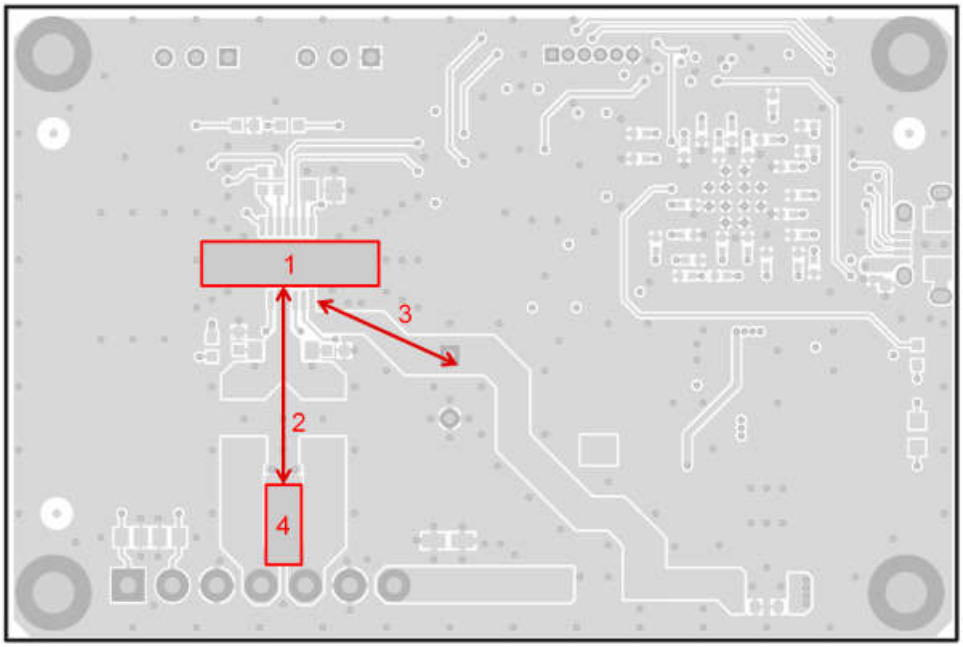


Figure 8-2. Top layer

8.4.2.2 Second Layer – Signal Layer

Pour a full ground plane on an inner layer to keep current loops small to reduce EMI.

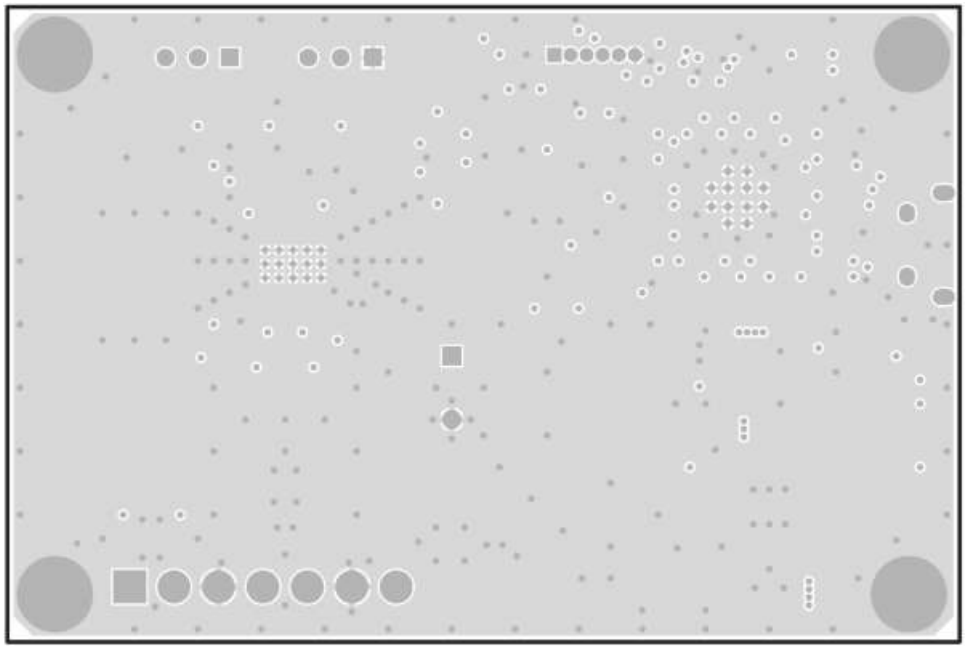


Figure 8-3. Signal Layer

8.4.2.3 Third Layer – Power Layer

There is no requirement for a power plane, but TI recommends a wide single wide trace to keep the switching noise to a minimum and provide enough current to the device. The wide trace provides a low-impedance path from the power source. Suppression of switching noise (ripple voltage) on both the positive and return (ground) paths requires a low impedance.

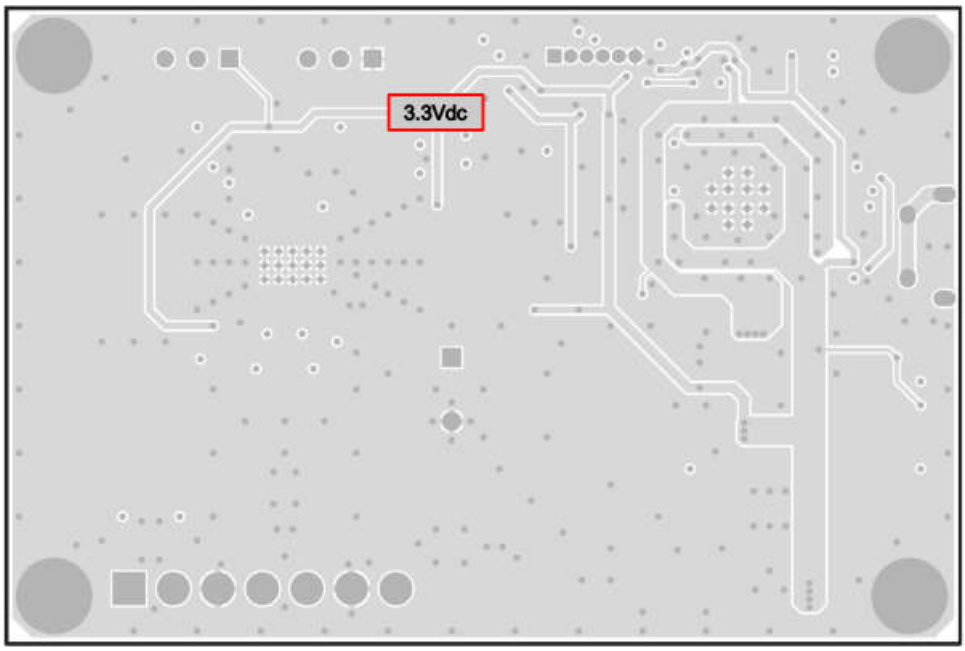


Figure 8-4. Power Layer

8.4.2.4 Bottom Layer – Ground Layer

The device has an exposed thermal pad on the bottom side for improved thermal performance. Conducting heat from the thermal pad to other layers requires thermal vias. Because the bottom layer is the secondary heat exchange surface to ambient, the thermal vias area must have low thermal resistance.

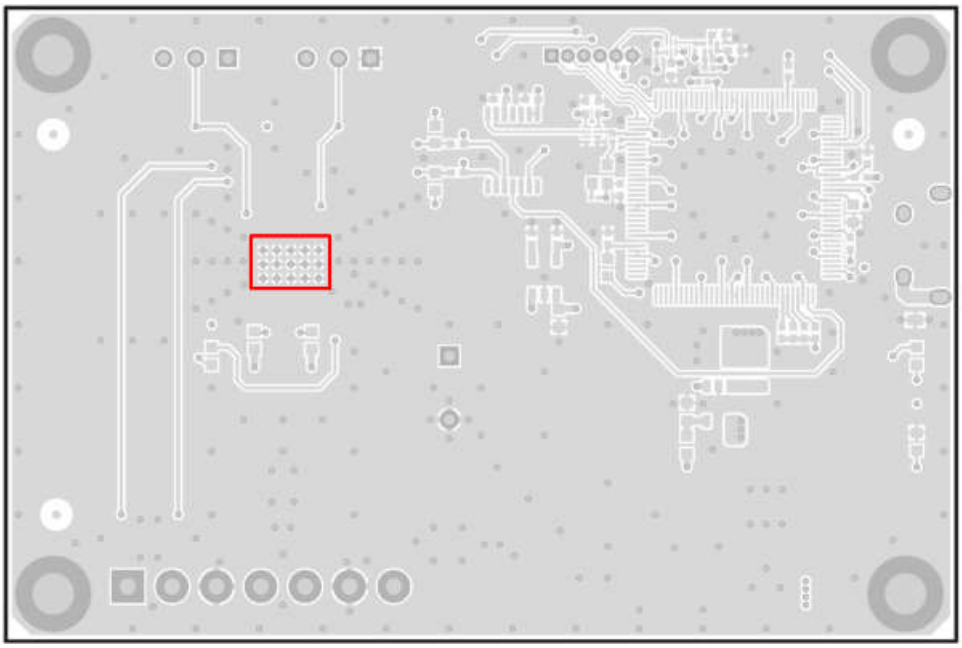


Figure 8-5. Bottom Layer

9 Device and Documentation Support

9.1 Device Support

9.1.1 Third-Party Products Disclaimer

TI'S PUBLICATION OF INFORMATION REGARDING THIRD-PARTY PRODUCTS OR SERVICES DOES NOT CONSTITUTE AN ENDORSEMENT REGARDING THE SUITABILITY OF SUCH PRODUCTS OR SERVICES OR A WARRANTY, REPRESENTATION OR ENDORSEMENT OF SUCH PRODUCTS OR SERVICES, EITHER ALONE OR IN COMBINATION WITH ANY TI PRODUCT OR SERVICE.

9.2 Documentation Support

9.2.1 Related Documentation

For related documentation see the following:

- *Class-D LC Filter Design* (SLOA119)
- *Class-D Output Snubber Design Guide* (SLOA201)
- *PowerPAD Thermally Enhanced Package* (SLMA002)

9.3 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

9.4 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

9.5 Trademarks

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9.6 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

9.7 Glossary

TI Glossary	This glossary lists and explains terms, acronyms, and definitions.

10 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision * (September 2024) to Revision A (January 2025)	Page
• Changed data-sheet status from *Advanced Information* to *Production Data*	1

11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical packaging and orderable information. This information is the most-current data available for the designated devices. This data is subject to change without notice and without revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

11.1 Package Option Addendum

11.1.1 Packaging Information

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish(4)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking(5) (6)
TSD5402QPWPRQ1	PREVIEW	HTSSOP	PWP	16	2000	TBD	NIPDAU	Level-3-260C-168 HR	-40 to 125	TSD5402

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PRE_PROD Unannounced device, not in production, not available for mass market, nor on the web, samples not available.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

(5) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device

(6) Multiple Device markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

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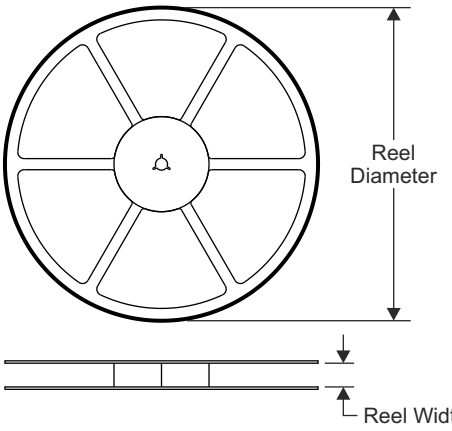
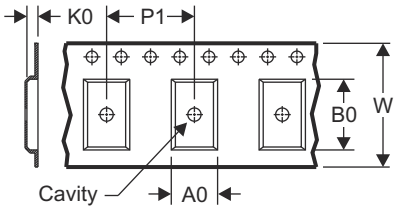
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

11.1.2 Tape and Reel Information

REEL DIMENSIONS

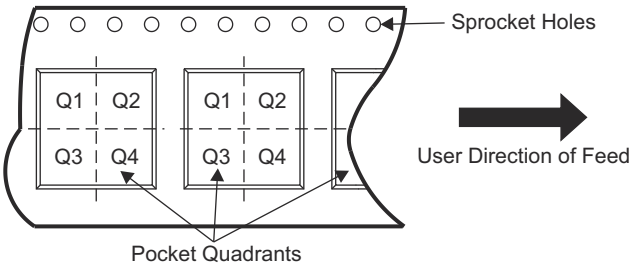


TAPE DIMENSIONS



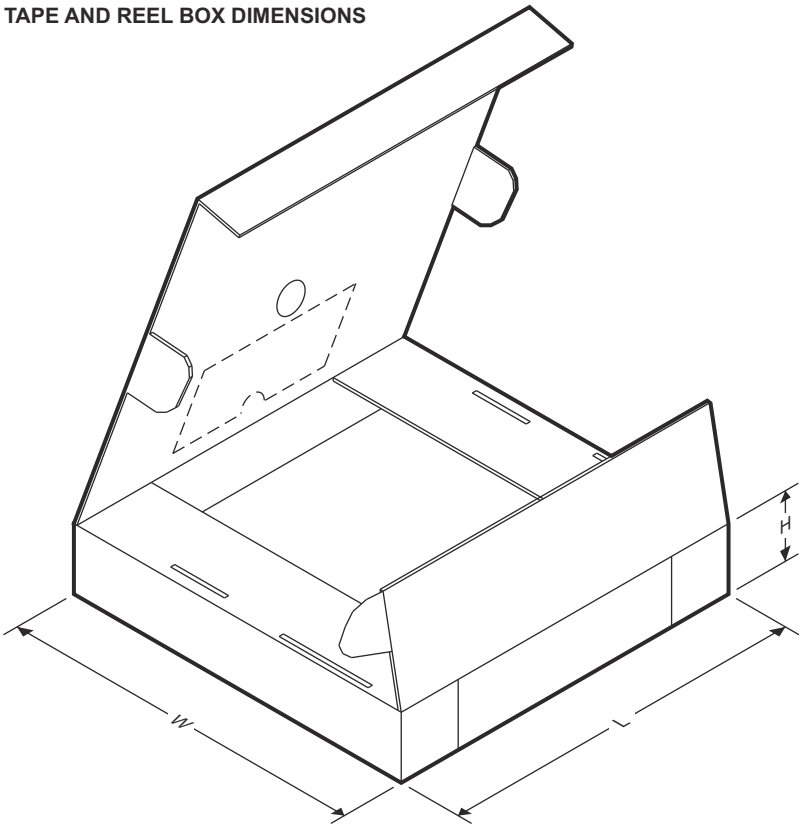
A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TSD5402QPWPRQ1	HTSSOP	PWP	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1

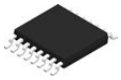
TAPE AND REEL BOX DIMENSIONS



Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TSD54021QPWPRQ1	HTSSOP	PWP	16	2000	350.0	350.0	43.0

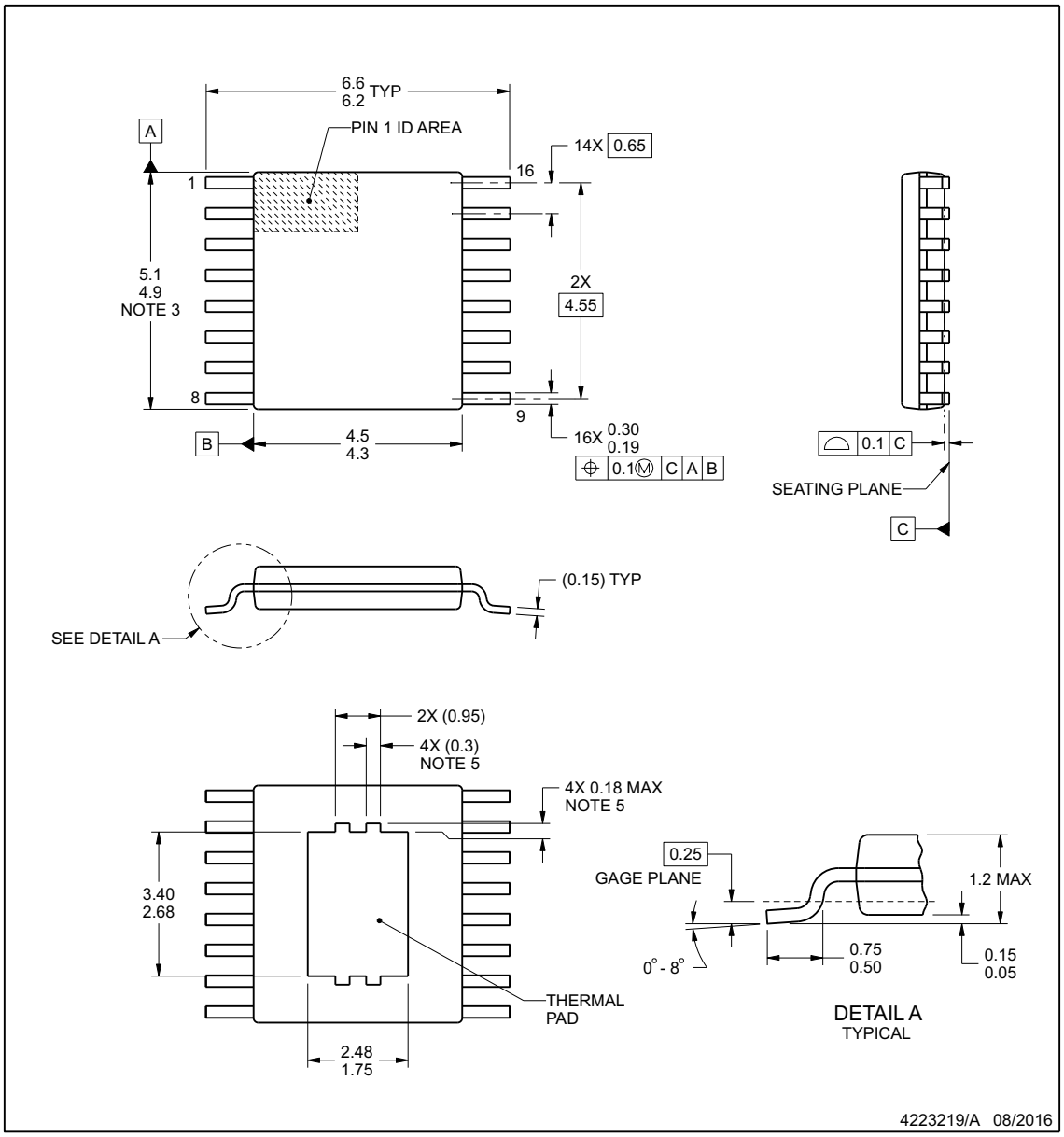
PACKAGE OUTLINE

PWP0016D



PowerPAD™ TSSOP - 1.2 mm max height

PLASTIC SMALL OUTLINE



PowerPAD is a trademark of Texas Instruments.

NOTES:

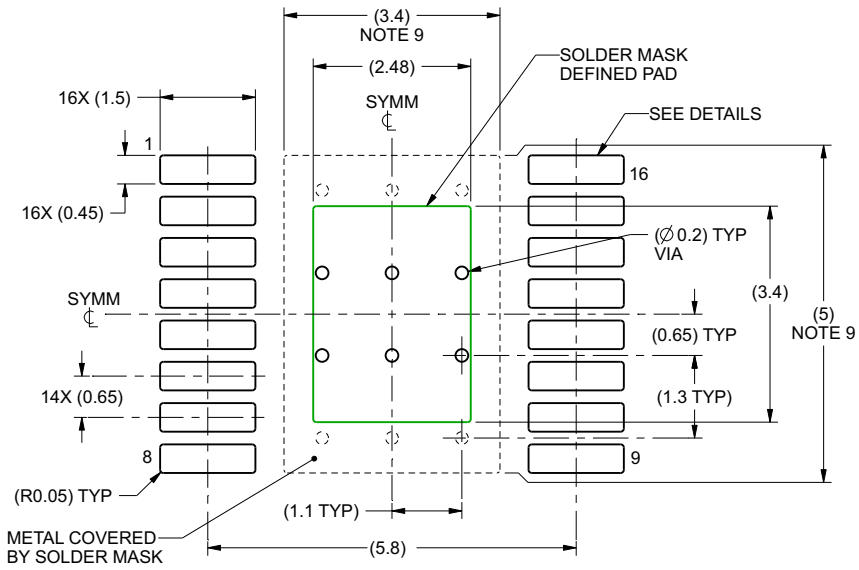
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. Reference JEDEC registration MO-153.
5. Features may differ and may not be present.

EXAMPLE BOARD LAYOUT

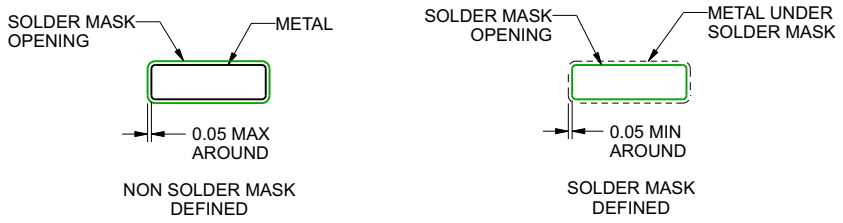
PWP0016D

PowerPAD™ TSSOP - 1.2 mm max height

PLASTIC SMALL OUTLINE



LAND PATTERN EXAMPLE
SCALE:10X



SOLDER MASK DETAILS
NOT TO SCALE

4223219/A 08/2016

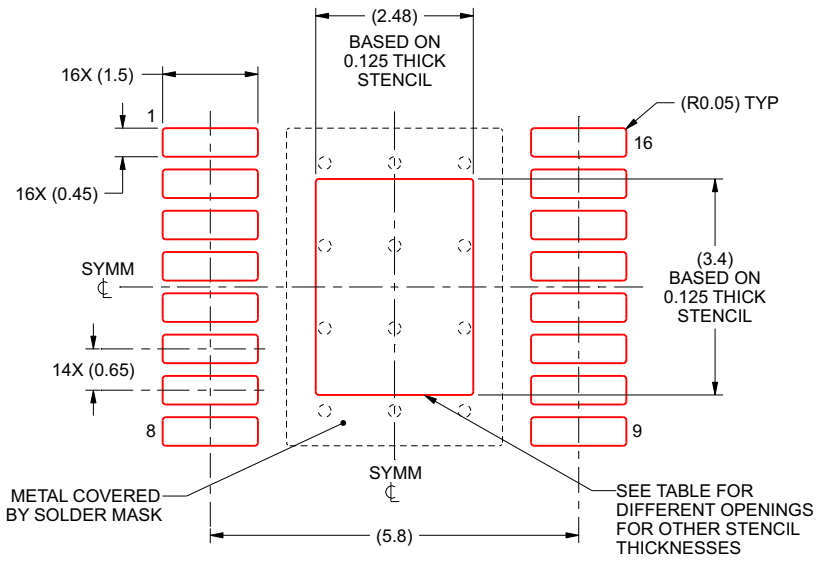
NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature numbers SLMA002 (www.ti.com/lit/slma002) and SLMA004 (www.ti.com/lit/slma004).
9. Size of metal pad may vary due to creepage requirement.

EXAMPLE STENCIL DESIGN

PWP0016D — **PowerPAD™ TSSOP - 1.2 mm max height**

PLASTIC SMALL OUTLINE



SOLDER PASTE EXAMPLE
EXPOSED PAD
100% PRINTED SOLDER COVERAGE BY AREA
SCALE:10X

STENCIL THICKNESS	SOLDER STENCIL OPENING
0.1	2.77 X 3.8
0.125	2.48 X 3.4 (SHOWN)
0.15	2.26 X 3.1
0.175	2.1 X 2.87

4223219/A 08/2016

NOTES: (continued)

10. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
11. Board assembly site may have different recommendations for stencil design.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TSD5402QPWPRQ1	Active	Production	HTSSOP (PWP) | 16	2000 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 125	TSD5402
TSD5402QPWPRQ1.A	Active	Production	HTSSOP (PWP) | 16	2000 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 125	TSD5402

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

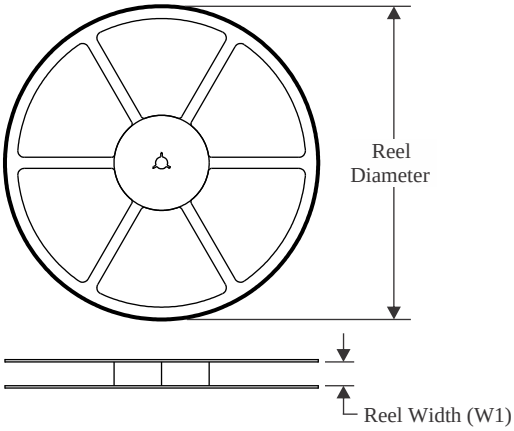
(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

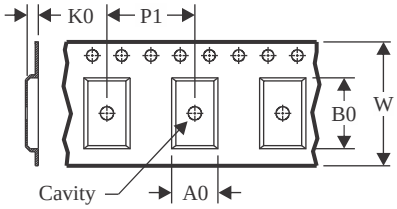
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

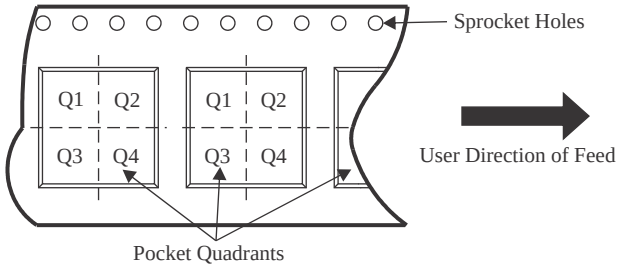


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

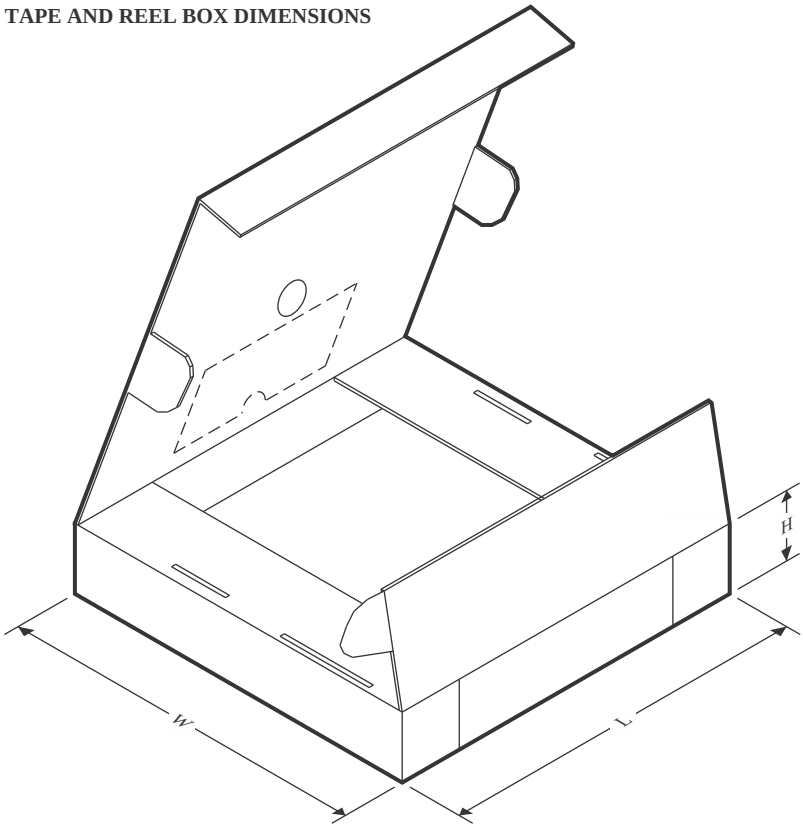
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TSD5402QPWPRQ1	HTSSOP	PWP	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS

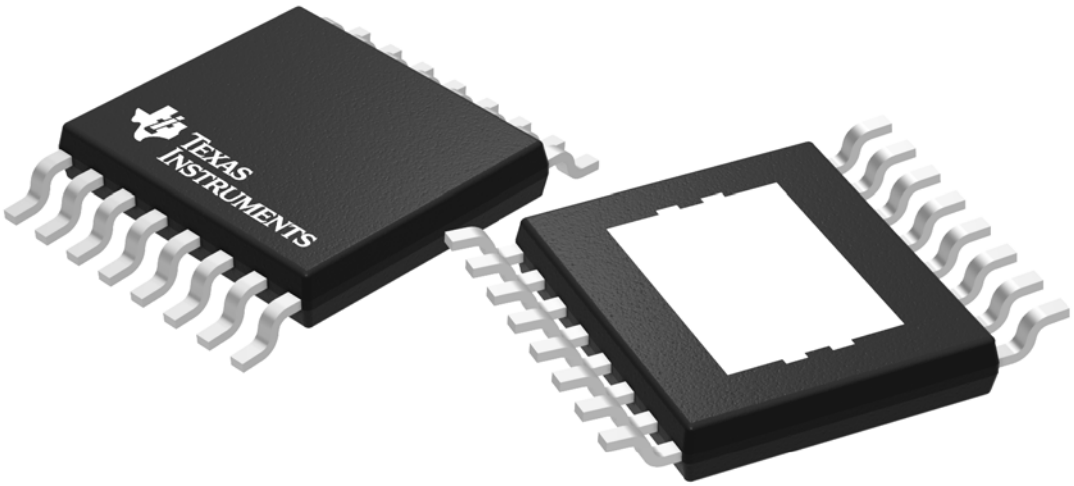


*All dimensions are nominal

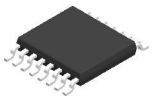
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TSD5402QPWPRQ1	HTSSOP	PWP	16	2000	353.0	353.0	32.0

PWP 16 PowerPAD™ TSSOP - 1.2 mm max height

PLASTIC SMALL OUTLINE



Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

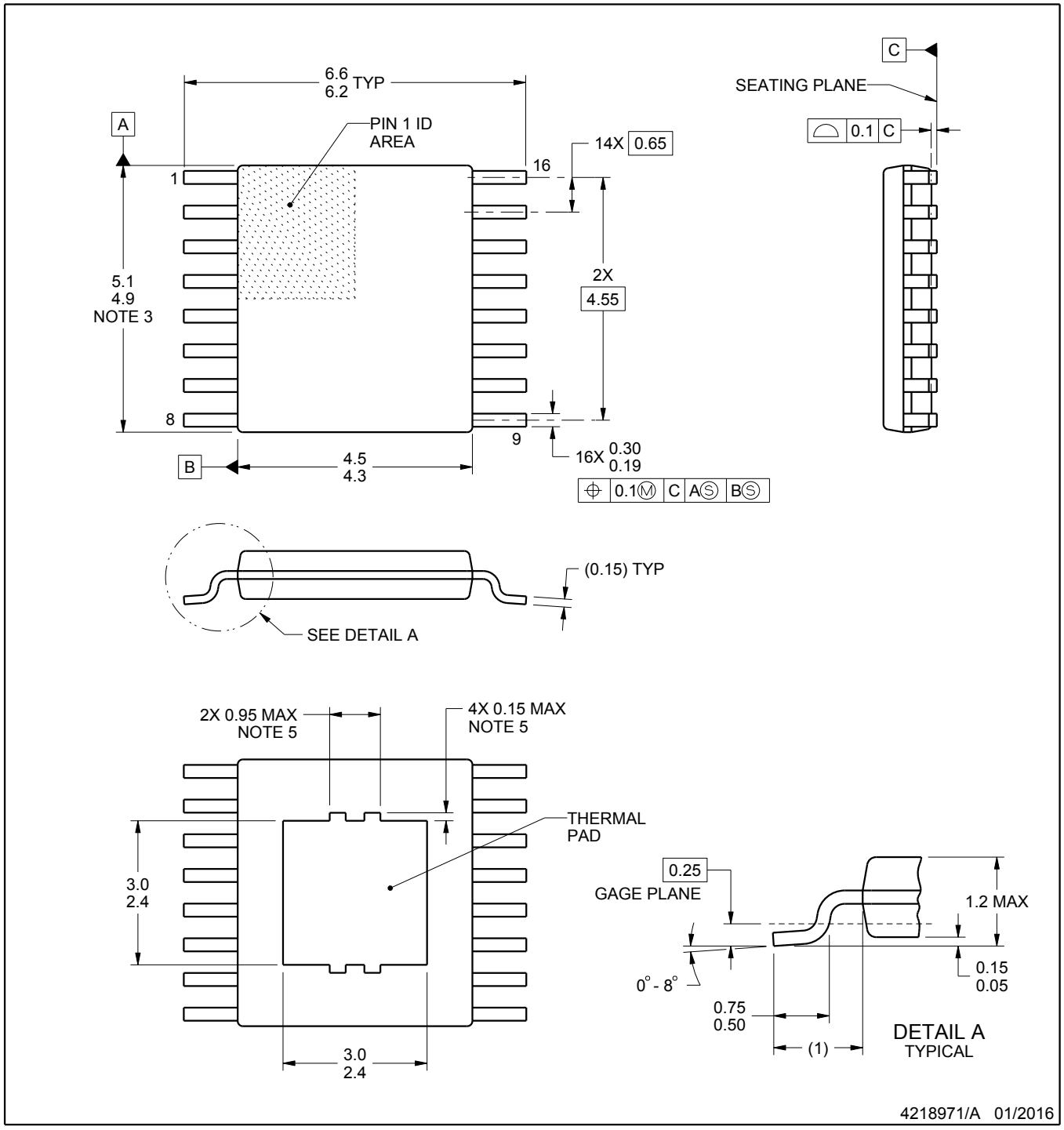


PACKAGE OUTLINE

PWP0016B

PowerPAD™ TSSOP - 1.2 mm max height

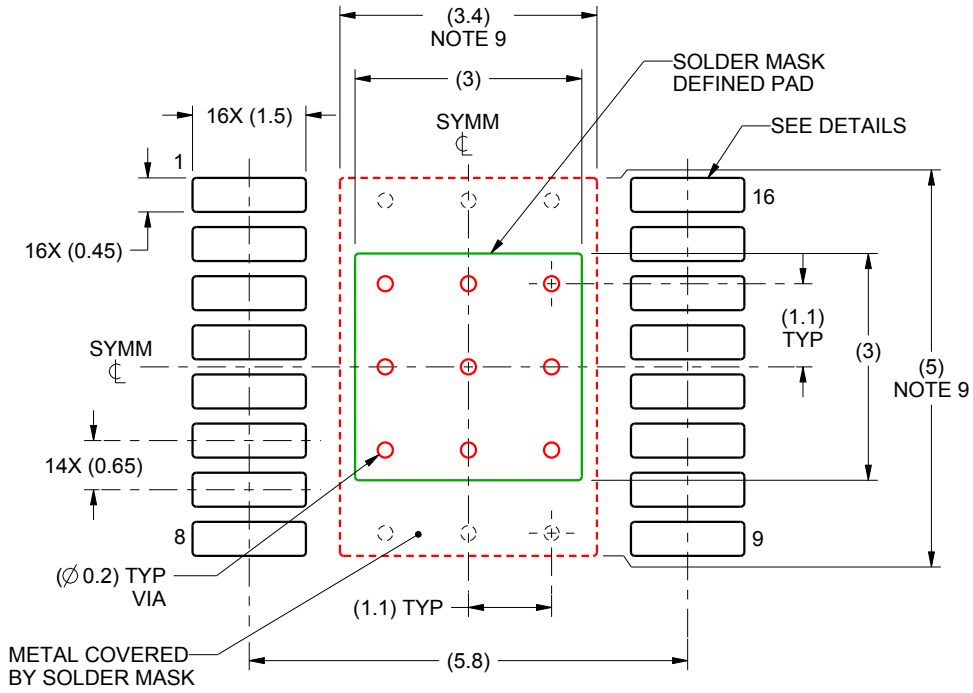
PLASTIC SMALL OUTLINE



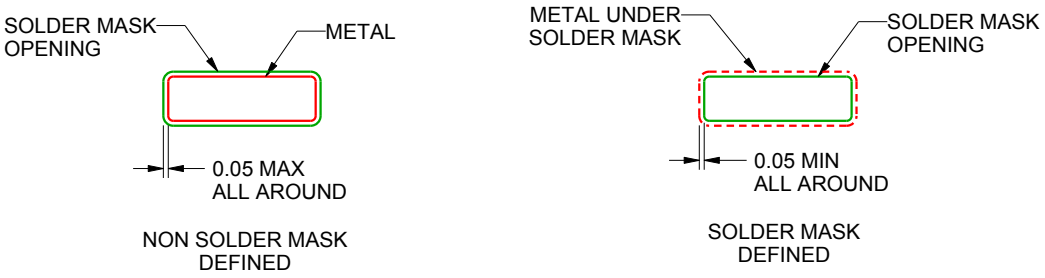
PowerPAD is a trademark of Texas Instruments.

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. Reference JEDEC registration MO-153.
5. Features may not be present.



LAND PATTERN EXAMPLE
SCALE:10X

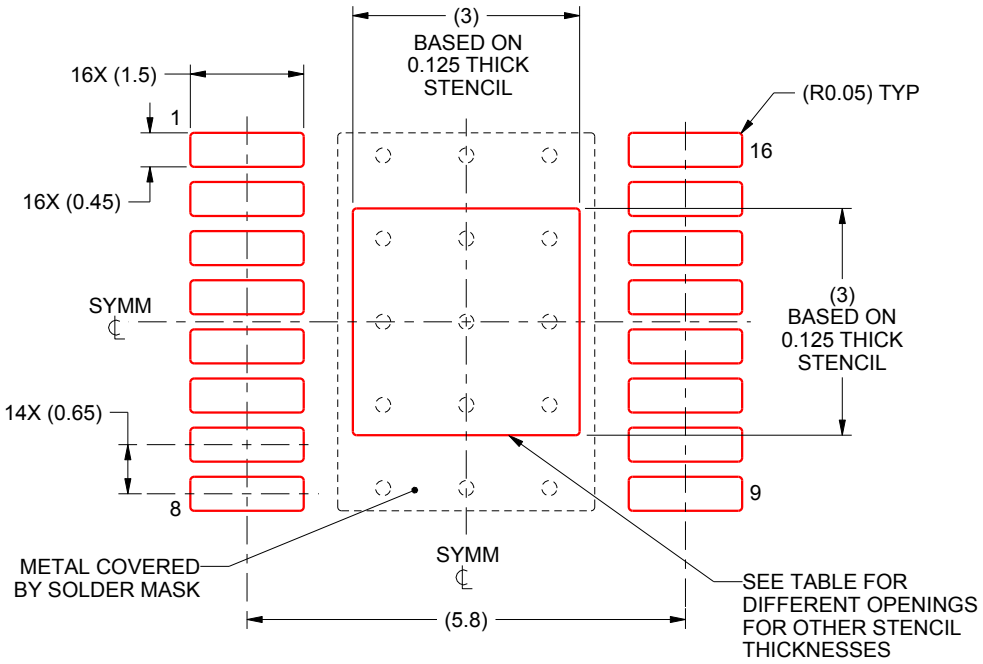


SOLDER MASK DETAILS
PADS 1-16

4218971/A 01/2016

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature numbers SLMA002 (www.ti.com/lit/slma002) and SLMA004 (www.ti.com/lit/slma004).
9. Size of metal pad may vary due to creepage requirement.



SOLDER PASTE EXAMPLE
EXPOSED PAD
100% PRINTED SOLDER COVERAGE BY AREA
SCALE:10X

STENCIL THICKNESS	SOLDER STENCIL OPENING
0.1	3.35 X 3.35
0.125	3 X 3 (SHOWN)
0.15	2.74 X 2.74
0.175	2.54 X 2.54

4218971/A 01/2016

NOTES: (continued)

10. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
11. Board assembly site may have different recommendations for stencil design.

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Last updated 10/2025