# TVS2210 22V Flat-Clamp Surge Protection Device

## 1 Features

- Protection against ±1kV, 42Ω IEC 61000-4-5 surge test for industrial signal lines
- Maximum clamping voltage of 28V at 25A of 8/20µs surge current
- Robust surge protection:
  - IEC 61000-4-5 (8/20µs): 25A
- Integrated IEC 61000-4-2 ESD protection
- Tiny 1.0mm x 0.6mm footprint

## 2 Applications

- Mobile Phones
- Tablets
- PC & Notebooks
- USB Type-C™ $V_{bus}$

## 3 Description

The TVS2210 robustly shunts up to 25A of IEC 61000-4-5 fault current to protect systems from high power transients or lightning strikes. The device offers a solution to the common industrial signal line EMC requirement to survive up to ±1kV IEC 61000-4-5 open circuit voltage coupled through a 42Ω impedance.

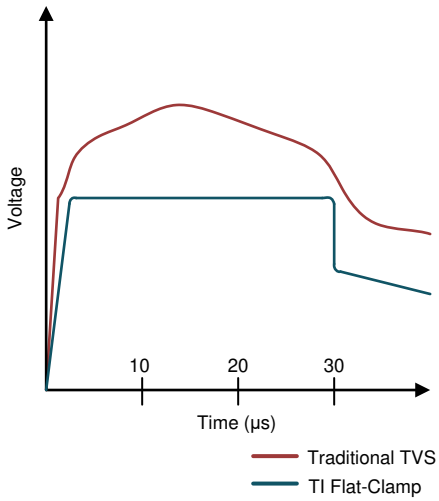
The TVS2210 uses a unique feedback mechanism for precise flat clamping during a fault, allowing system exposure below 30V. The tight voltage regulation allows designers to confidently select system components with a lower voltage tolerance, lowering system costs and complexity without sacrificing robustness.

In addition, the TVS2210 is available in a small, non-encapsulated 1.0mm × 0.6mm footprint which is designed for space constrained applications. The extremely low device leakage and capacitance causes a minimal effect on the protected line.

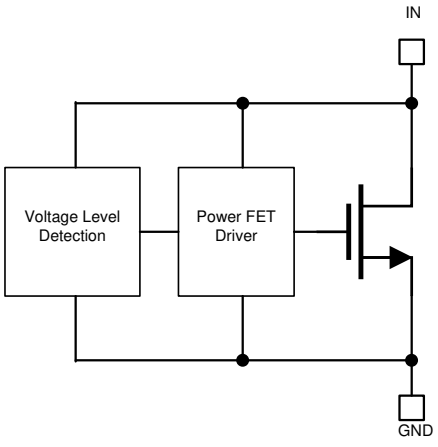
**Package Information**

| PART NUMBER | PACKAGE (1) | PACKAGE SIZE (2) |
|---|---|---|
| TVS2210 | (0402, 2), YMZ | 1.0mm × 0.6mm |

(1) For all available packages, see the orderable addendum at the end of the data sheet.
(2) The package size (length × width) is a nominal value and includes pins, where applicable.




**Voltage Clamp Response to 8µs to 20µs Surge Event**




**Functional Block Diagram**

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# 4 Pin Configuration and Functions

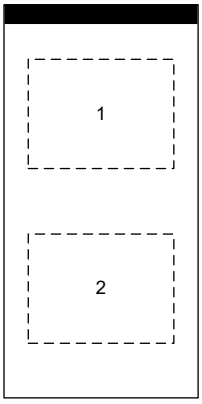


**Figure 4-1. YMZ Package, 2-Pin 0402 (Bottom View)**

**Pin Functions**

| PIN | | TYPE | DESCRIPTION |
|---|---|---|---|
| NAME | NO. | | |
| IN | 1 | IO | ESD and surge protected channel |
| GND | 2 | GND | Ground |

# 5 Specifications

## 5.1 Absolute Maximum Ratings

$T_A$ = 27°C (unless otherwise noted)(1)

| | | MIN | MAX | UNIT |
|---|---|---|---|---|
| Maximum Surge | IEC 61000-4-5 Current (8/20 µs) | | 25 | A |
| | IEC 61000-4-5 Power (8/20 µs) | | 700 | W |
| $T_A$ | Ambient Operating Temperature | -40 | 125 | °C |
| $T_{stg}$ | Storage Temperature | -65 | 150 | °C |

(1) Stresses beyond those listed under *Absolute Maximum Rating* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Condition*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

## 5.2 ESD Ratings - JEDEC

| | | | VALUE | UNIT |
|---|---|---|---|---|
| $V_{(ESD)}$ | Electrostatic discharge | Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins(1) | ±2000 | V |
| | | Charged device model (CDM), per JEDEC specification JESD22-C101, all pins(2) | ±500 | |

(1) JEDEC document JEP155 states that 500V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250V CDM allows safe manufacturing with a standard ESD control process.

## 5.3 ESD Ratings - IEC

| | | | VALUE | UNIT |
|---|---|---|---|---|
| $V_{(ESD)}$ | Electrostatic discharge | IEC 61000-4-2 contact discharge | ±8 | kV |

## 5.4 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

| PARAMETER | | MIN | NOM | MAX | UNIT |
|---|---|---|---|---|---|
| $V_{RWM}$ | Reverse Stand-off Voltage | | | 22 | V |

## 5.5 Thermal Information

| THERMAL METRIC(1) | | TVS2210 YMZ (0402) 2 PINS | UNIT |
|---|---|---|---|
| $R_{\theta JA}$ | Junction-to-ambient thermal resistance | 242.6 | °C/W |
| $R_{\theta JC(top)}$ | Junction-to-case (top) thermal resistance | 1.9 | °C/W |
| $R_{\theta JB}$ | Junction-to-board thermal resistance | 63.7 | °C/W |
| $\Psi_{JT}$ | Junction-to-top characterization parameter | 1.2 | °C/W |
| $\Psi_{JB}$ | Junction-to-board characterization parameter | 63.6 | °C/W |
| $R_{\theta JC(bot)}$ | Junction-to-case (bottom) thermal resistance | N/A | °C/W |

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application note.

## 5.6 Electrical Characteristics

over operating free-air temperature range (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| $V_{RWM}$ | Reverse Stand-off Voltage | | | | 22 | V |
| $I_{LEAK}$ | Leakage Current | Measured at $V_{IN} = V_{RWM}$ $T_A$ = 25°C | | 6 | 70 | nA |
| | | Measured at $V_{IN} = V_{RWM}$ $T_A$ = 85°C | | 25 | 500 | nA |
| $V_{BR}$ | Break-down Voltage | $I_{IN}$ = 1mA from IO to GND | 24.6 | 25.9 | 27.6 | V |
| $V_F$ | Forward Voltage | $I_{IN}$ = 1mA from GND to IO | 0.25 | 0.5 | 0.65 | V |
| $V_{CLAMP}$ | Clamp Voltage | 1A IEC 61000-4-5 Surge (8/20µs) from IO to GND, $V_{IN}$ = 0V before surge, 25°C | | 27.2 | 27.7 | V |
| $V_{CLAMP}$ | Clamp Voltage | 25A IEC 61000-4-5 Surge (8/20µs) from IO to GND, $V_{IN}$ = 0V before surge, 25°C | | 27.6 | 28 | V |
| $R_{DYN}$ | 8/20µs surge dynamic resistance | Calculated from $V_{CLAMP}$ at .5*$I_{pp}$ and $I_{pp}$ surge current levels, 25°C | | 30 | | mΩ |
| $C_{IN}$ | Input pin capacitance | $V_{IN} = V_{RWM}$, f = 1MHz, IO to GND | | 59 | | pF |

## 5.7 Typical Characteristics

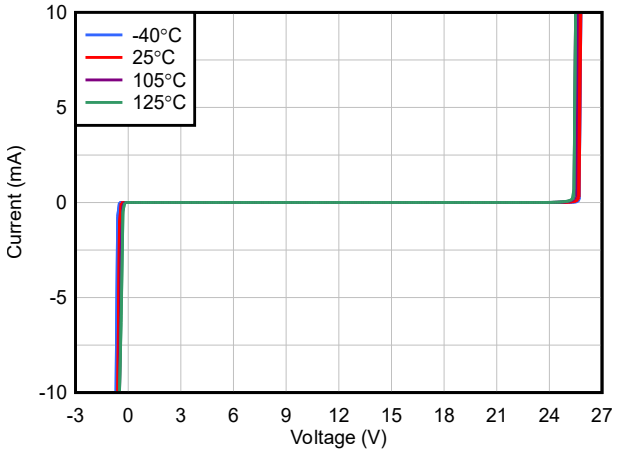


**Figure 5-1. IV Across Temperature**

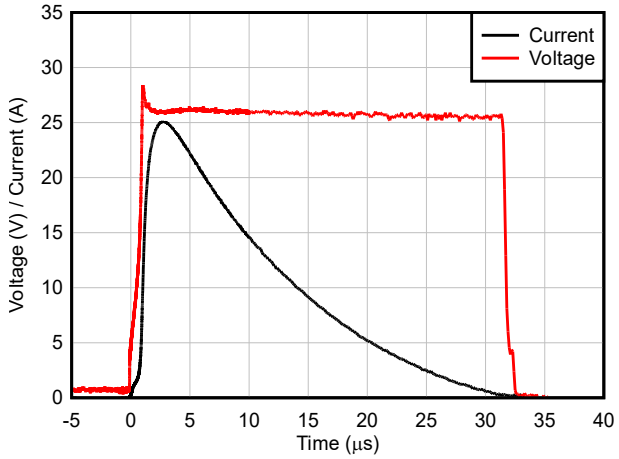


**Figure 5-2. Surge Response at 25A**

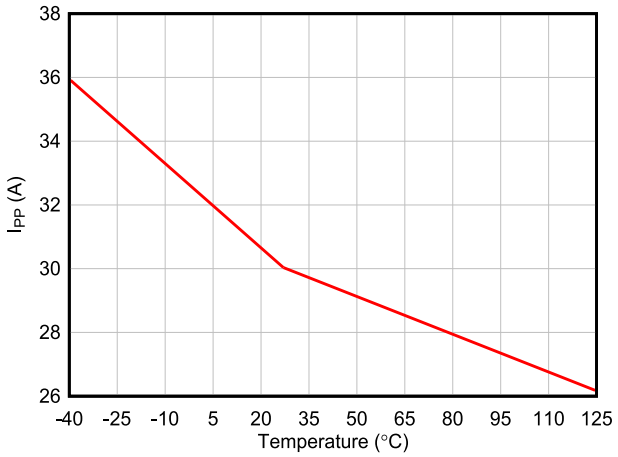


**Figure 5-3. Maximum Surge Current (8/20µs) vs Temperature**

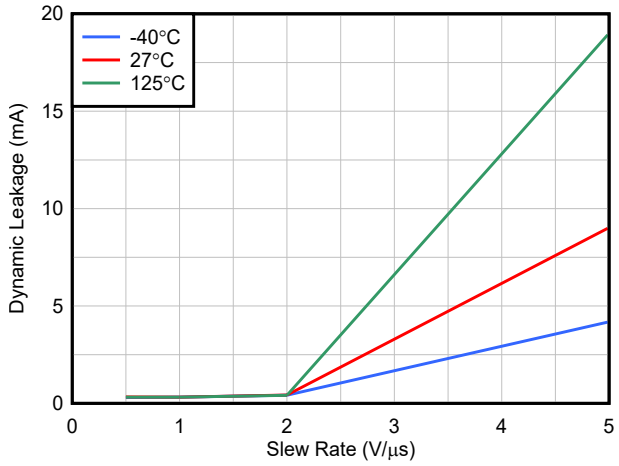


**Figure 5-4. Maximum Leakage vs Signal Slew Rate Across Temperature**

# 6 Application and Implementation

**Note**

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

## 6.1 Power Supply Recommendations

The TVS2210 is a clamping device so there is no need to power it. To ensure the device functions properly, do not violate the recommended $V_{IN}$ voltage range (0V to 22V).

## 6.2 Layout

### *6.2.1 Layout Guidelines*

The optimum placement is close to the connector. EMI during an ESD event can couple from the trace being struck to other nearby unprotected traces, resulting in early system failures. The PCB designer must minimize the possibility of EMI coupling by keeping any unprotected traces away from the protected traces which are between the TVS and the connector.

Route the protected traces straight. Eliminate any sharp corners on the protected traces between the TVS2210 and the connector by using rounded corners with the largest radii possible. Electric fields tend to build up on corners, increasing EMI coupling.

### *6.2.2 Layout Example*

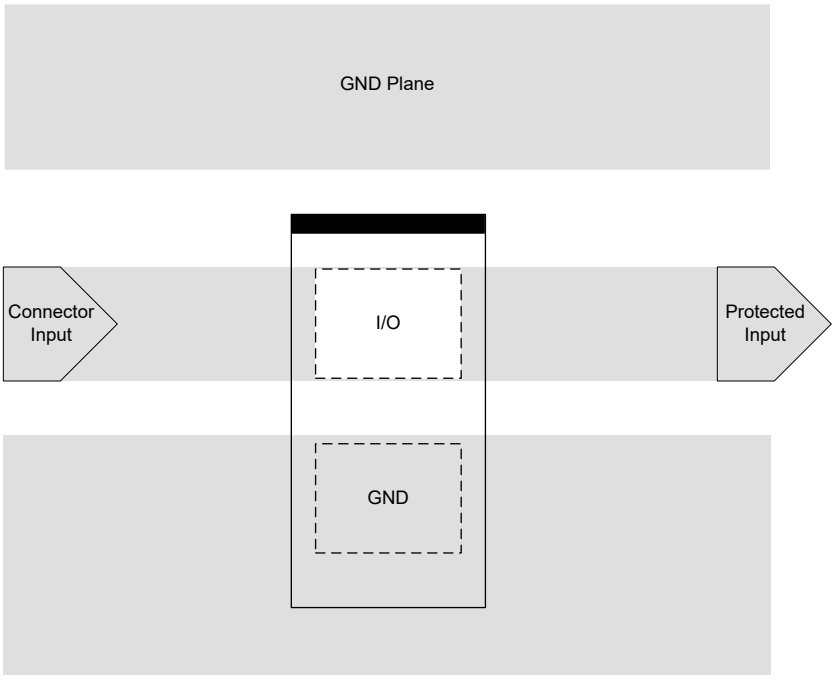


**Figure 6-1. TVS2210 Layout**

# 7 Device and Documentation Support

## 7.1 Documentation Support

### *7.1.1 Related Documentation*

For related documentation, see the following:

- Texas Instruments, *Flat-Clamp surge protection technology for efficient system protection*
- Texas Instruments, *TI's IEC 61000-4-x Testing Application Note*.
- Texas Instruments, *TVS3300 Configurations Characterization*

## 7.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

## 7.3 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

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## 7.4 Trademarks

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## 7.5 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

## 7.6 Glossary

| | |
|---|---|
| TI Glossary | This glossary lists and explains terms, acronyms, and definitions. |

# 8 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

| DATE | REVISION | NOTES |
|---|---|---|
| December 2025 | * | Initial Release |

# 9 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

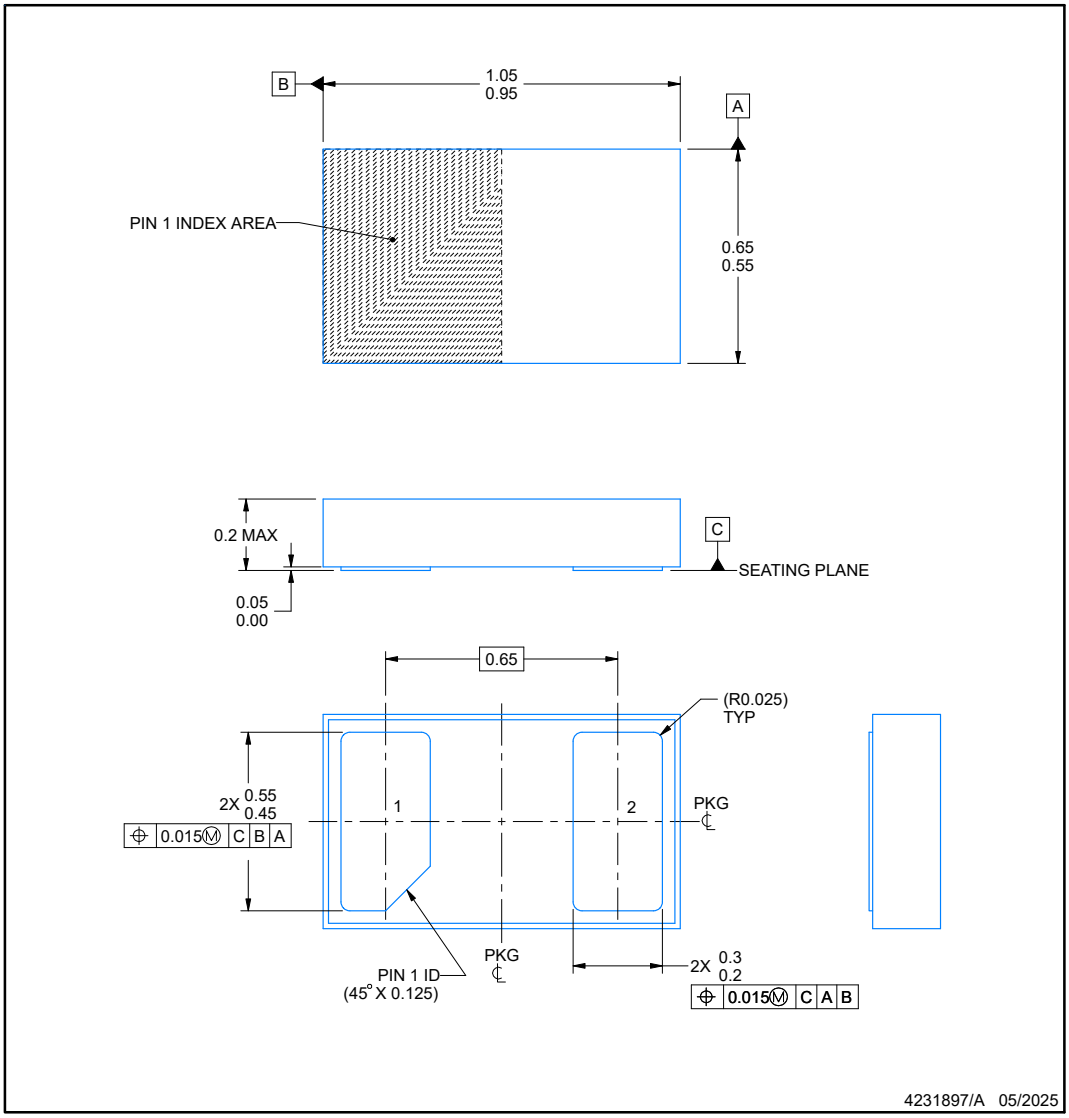
## 9.1 Mechanical Data

**YNZ0002A**

**PACKAGE OUTLINE**

**PicoStar™ - 0.2 mm max height**

PicoStar™




PicoStar is a trademark of Texas Instruments.

NOTES:

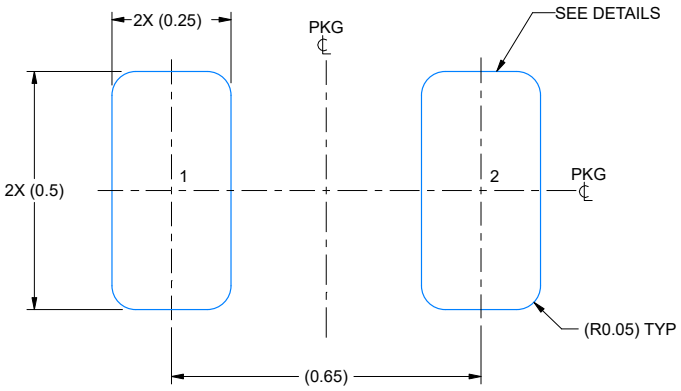
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M
2. This drawing is subject to change without notice.
3. This package is a Pb-free bump design. Bump finish may vary. To determine the exact finish, refer to the device datasheet or contact a local TI representative.

## EXAMPLE BOARD LAYOUT

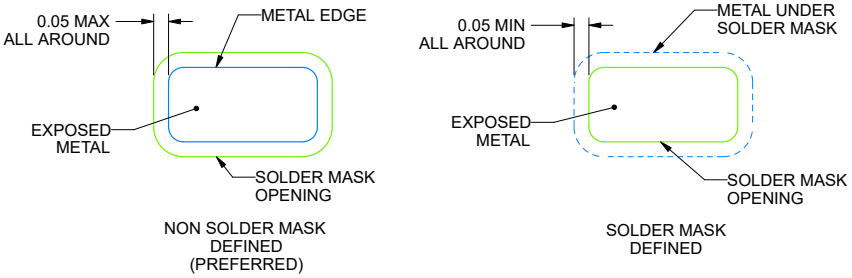
### YNZ0002A

**PicoStar ™ - 0.2 mm max height**

PicoStar ™




LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:80X




SOLDER MASK DETAILS

4231897/A 05/2025

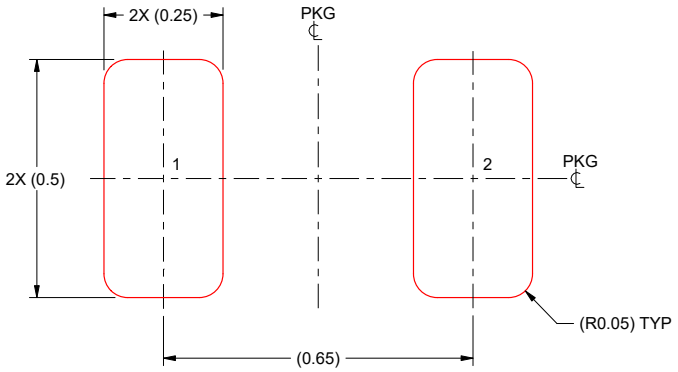
NOTES: (continued)

4. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).

## EXAMPLE STENCIL DESIGN

**YNZ0002A** **PicoStar ™ - 0.2 mm max height**

PicoStar ™




SOLDER PASTE EXAMPLE
BASED ON 0.1 mm THICK STENCIL
SCALE:80X

4231897/A 05/2025

NOTES: (continued)

5. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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