TXG404x-Q1 4-Bit, ±40V Ground-Level Translator

1 Features

- Supports DC ground shifts up to ±40V
- AC Noise Rejection up to 130V_{PP} at 1MHz and CMTI of 1kV/µs
- Low Prop Delay (8.5ns max) and Ch-Ch Skew (2ns max)
- 100Mbps data rate
- Low power consumption (0.7mA per channel at 1Mbps, 1.8V)
- Fully configurable dual-rail design allows each port to operate from 1.71V to 5.5V
- 4, 2, 1 channel devices with multiple configurations will be available
- Two device variants:
  - TXG4041: 3 forward, 1 reverse
  - TXG4042: 2 forward, 2 reverse
- Supports V_{CC} disconnect feature (I/Os are forced into high-Z)
- Schmitt-trigger inputs allows for slow and noisy signals
- Inputs with integrated static pull-down resistors prevent channels from floating
- Operating temperature from –40°C to +125°C
- Latch-up performance exceeds 100mA per JESD 78, class II
- ESD protection exceeds JESD 22
  - 2000V human-body model
  - 500V charged-device model
- Package option: RUC (X2QFN-14)

2 Applications

- Electric Power Steering
- Vehicle Control Unit
- Automotive Display
- Head Unit and Digital Cockpit
- Test and Measurement
- Factory Automation
- Appliances

3 Description

The TXG404x-Q1 is a 4-bit, fixed direction, non-galvanic based voltage and ground-level translator that can support both logic-level shifting between 1.71V to 5.5V and ground-level shifting up to ±40V. Compared to traditional level shifters, the TXG404x-Q1 family can solve the challenges of voltage translation across different ground levels. The Simplified Block Diagram shows a common use case where there is a DC shift between GNDA to GNDB due to parasitic resistance or capacitance.

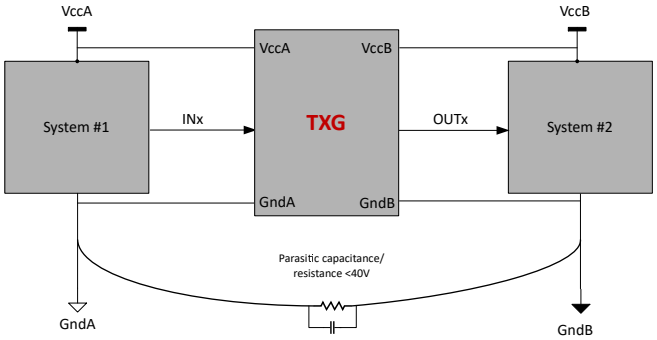
V_{CCA} is referenced to GNDA and V_{CCB} is referenced to GNDB. Ax pins are referenced to V_{CCA} logic levels while Bx pins are referenced to V_{CCB} logic levels. Both A port and B port can accept voltages from 1.71V to 5.5V. This device includes two enable pins that can place the respective outputs in a high-impedance state when the OE pin is connected to GND or left floating. In the event of input power or signal loss, the output is default low when OE is High (refer to Table 7-1). The max leakage between GNDA and GNDB is 2µA when V_{CC} to GND is shorted.

The TXG404x-Q1 device helps improve noise immunity and power sequencing across different ground domains while providing low power consumption, latency and channel-to-channel skew. It can supress noise levels at 130V_{PP} up to 1MHz (Figure 6-1). This device can support multiple interfaces such as SPI, UART, GPIO, and I2S.

Package Information

PART NUMBER	PACKAGE (1)	BODY SIZE (NOM)
TXG4041-Q1 TXG4042-Q1	RUC (X2QFN-14)	2.00mm × 2.00mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.



Simplified Block Diagram

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4 Pin Configuration and Functions

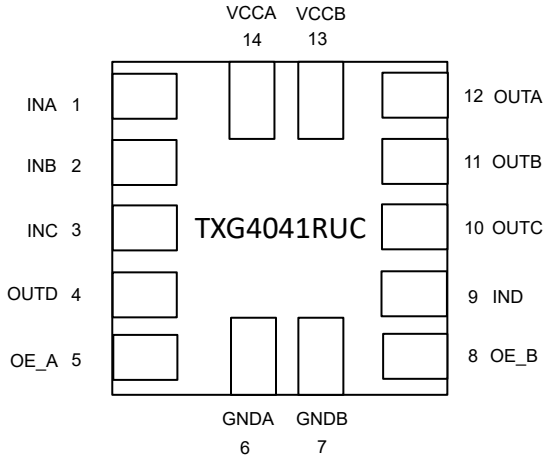

Figure 4-1. TXG4041RUC Package 14-Pin X2QFN Top View

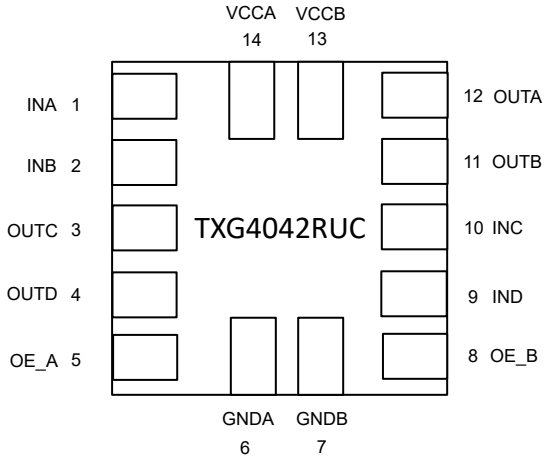

Figure 4-2. TXG4042RUC Package 14-Pin X2QFN Top View

Table 4-1. TXG404x RUC Pin Functions

PIN			I/O	DESCRIPTION
Name	TXG4041	TXG4042		
INA	1	1	I	Input Channel A
INB	2	2	I	Input Channel B
INC	3	10	I	Input Channel C
IND	9	9	I	Input Channel D
OUTA	12	12	O	Output Channel A
OUTB	11	11	O	Output Channel B
OUTC	10	3	O	Output Channel C
OUTD	4	4	O	Output Channel D
OE_A	5	5	I	Active-High Output Enable (A side). Pull to GND to place all outputs in high-impedance mode.
OE_B	8	8	I	Active-High Output Enable (B side). Pull to GND to place all outputs in high-impedance mode.
V_{CCA}	14	14	—	A side supply voltage. 1.71 V ≤ V_{CCA} ≤ 5.5 V
V_{CCB}	13	13	—	B side supply voltage. 1.71 V ≤ V_{CCB} ≤ 5.5 V
GNDA	6	6	—	Ground reference for V_{CCA}
GNDB	7	7	—	Ground reference for V_{CCB}

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5 Specifications

5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

			MIN	MAX	UNIT
V_{CCA} to V_{GNDA}	Supply voltage A to Ground voltage A		–0.5	6.5	V
V_{CCB} to V_{GNDB}	Supply voltage B to Ground voltage B		–0.5	6.5	V
V_{GNDA} to V_{GNDB}	Ground voltage B to Ground voltage A		-42	42	V
V_I	Input Voltage(2)	I/O Ports (A Port) to V_{GNDA}	–0.5	6.5	V
		I/O Ports (B Port) to V_{GNDB}	–0.5	6.5	
		OE	–0.5	6.5	V
V_O	Voltage applied to any output in the high-impedance or power-off state(2)	A Port to V_{GNDA}	–0.5	6.5	V
		B Port to V_{GNDB}	–0.5	6.5	
V_O	Voltage applied to any output in the high or low state(2) (3)	A Port to V_{GNDA}	–0.5	V_{CCA} + 0.5	V
		B Port to V_{GNDB}	–0.5	V_{CCB} + 0.5	
I_{IK}	Input clamp current	V_I < 0	–20		mA
I_{OK}	Output clamp current	V_O < 0	–20		mA
I_O	Continuous output current		–25	25	mA
	Continuous current through V_{CC} or GND		–100	100	mA
T_j	Junction Temperature			150	°C
T_{stg}	Storage temperature		–65	150	°C

(1) Stresses beyond those listed under *Section 5.1* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Section 5.3* Exposure beyond the limits listed in *Section 5.3* may affect device reliability.
(2) The input voltage and output negative-voltage ratings may be exceeded if the input and output current ratings are observed.
(3) The output positive-voltage rating may be exceeded up to 6.5V maximum if the output current rating is observed.

5.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001	±2500	V
		Charged device model (CDM), per ANSI/ESDA/JEDEC JS-002	±500	

5.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted) (1) (2) (3)

			MIN	TYP	MAX	UNIT
V_{CCA}	Supply voltage A - Relative to GNDA		1.71		5.5	V
V_{CCB}	Supply voltage B - Relative to GNDB		1.71		5.5	V
V_{GNDA} - V_{GNDB}	Voltage Between GNDA and GNDB		-40		40	V
I_{OH}	High-level output current	V_{CCO} = 1.71 V	-4.5			mA
		V_{CCO} = 2.3 V	-8			
		V_{CCO} = 3 V	-10			
		V_{CCO} = 4.5 V	-12			
I_{OL}	Low-level output current	V_{CCO} = 1.71V			4.5	mA
		V_{CCO} = 2.3 V			8	
		V_{CCO} = 3 V			10	
		V_{CCO} = 4.5 V			12	
V_I	Input voltage - Relative to GNDx		0		5.5	V
V_{IH}	High-level input voltage		0.7 x V_{CCI}			V
V_{IL}	High-level output voltage				0.3 x V_{CCI}	V
V_O	Output voltage - Relative to GNDx		0		V_{CCO}	V
T_A	Operating free-air temperature		–40		125	°C

(1) V_{CCI} is the V_{CC} associated with the input port.
(2) V_{CCO} is the V_{CC} associated with the output port.
(3) All control inputs and data I/Os of this device have weak pulldowns to ensure the line is not floating when undefined external to the device. The input leakage from these weak pulldowns is defined by the I_I specification indicated under Section 5.4.

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5.4 Electrical Characteristics

over operating free-air temperature range (unless otherwise noted)(1) (2)

PARAMETER		TEST CONDITIONS	V_{CCA}	V_{CCB}	Operating free-air temperature (T_A)			UNIT
					–40°C to 125°C			
					MIN	TYP	MAX	
V_{OH}	High-level output voltage (3)	I_{OH} = –4.5 mA	1.71 V	1.71 V	1.5			V
		I_{OH} = –8 mA	2.3 V	2.3 V	2.0			
		I_{OH} = –10 mA	3 V	3 V	2.7			
		I_{OH} = –12 mA	4.5 V	4.5 V	4.1			
V_{OL}	Low-level output voltage (4)	I_{OL} = 4.5 mA	1.71 V	1.71 V			0.16	V
		I_{OL} = 8 mA	2.3 V	2.3 V			0.27	
		I_{OL} = 10 mA	3 V	3 V			0.34	
		I_{OL} = 12 mA	4.5 V	4.5 V			0.41	
V_{T+}	Positive-going input-threshold voltage	Data Inputs (Ax, Bx) (Referenced to V_{CCI})	1.71 V	1.71 V			1.11	V
			2.3 V	2.3 V			1.40	
			3 V	3 V			1.73	
			4.5 V	4.5 V			2.45	
			5.5 V	5.5 V			3.0	
V_{T+}	Positive-going input-threshold voltage	OE (Referenced to V_{CCA} or V_{CCB})	1.71 V	1.71 V			1.10	V
			2.3 V	2.3 V			1.40	
			3 V	3 V			1.72	
			4.5 V	4.5 V			2.45	
			5.5 V	5.5 V			2.96	
V_{T-}	Negative-going input-threshold voltage	Data Inputs (Ax, Bx) (Referenced to V_{CCI})	1.71 V	1.71 V	0.56			V
			2.3 V	2.3 V	0.80			
			3 V	3 V	1.15			
			4.5 V	4.5 V	1.61			
			5.5 V	5.5 V	2.0			
V_{T-}	Negative-going input-threshold voltage	OE (Referenced to V_{CCA} or V_{CCB})	1.71 V	1.71 V	0.5		0.72	V
			2.3 V	2.3 V	0.80		0.87	
			3 V	3 V	1.1		1.23	
			4.5 V	4.5 V	1.7		1.96	
			5.5 V	5.5 V	2.2		2.43	
ΔV_T	Input-threshold hysteresis ($V_{T+} – V_{T-}$)	Data Inputs (Ax, Bx) (Referenced to V_{CCI})	1.71 V	1.71 V	0.3		0.50	V
			2.3 V	2.3 V	0.36		0.60	
			3 V	3 V	0.38		0.54	
			4.5 V	4.5 V	0.41		0.82	
			5.5 V	5.5 V	0.40		0.96	
ΔV_T	Input-threshold hysteresis ($V_{T+} – V_{T-}$)	OE (Referenced to V_{CCA} or V_{CCB})	1.71 V	1.71 V	0.29		0.45	V
			2.3 V	2.3 V	0.35		0.58	
			3 V	3 V	0.38		0.54	
			4.5 V	4.5 V	0.41		0.58	
			5.5 V	5.5 V	0.43		0.62	
I_I	Input leakage current	Data Inputs (Ax, Bx) V_I = V_{CCI} or GND	1.71V – 5.5V	1.71V – 5.5V	0.2		1.6	µA

over operating free-air temperature range (unless otherwise noted)(1) (2)

PARAMETER		TEST CONDITIONS	V_{CCA}	V_{CCB}	Operating free-air temperature (T_A) –40°C to 125°C			UNIT
					MIN	TYP	MAX	
I_{off}	Partial power down current	A Port or B Port V_I = 1.71 V - 5.5 V	0 V	0 V - 5.5 V	–5		5	µA
			0 V - 5.5 V	0 V	–5		5	µA
$I_{off-float}$	Floating supply Partial power down current	A Port or B Port V_I = GND	Floating(5)	0 V - 5.5 V	–2.5		2.5	µA
			0 V - 5.5 V	Floating(5)	–2.5		2.5	
I_O	Tri-state output Output current	A or B Port: V_I = V_{CCA} or V_{GNDA} OE = GND	1.71V – 5.5V	1.1V – 5.5V	–5		5	µA
C_i	Control Input Capacitance	V_I = 3.3 V or V_{GNDA}	3.3 V	3.3 V	1		2	pF
C_{io}	Data I/O Capacitance	OE = GND, V_O = 1.71V DC +1 MHz -16 dBm sine wave	3.3 V	3.3 V	1		3	pF
C_{GND}	Cap between grounds	All channels combined (V_{CC} both sides are powered on)					46	pF
C_{GND}	Cap between grounds	All channels combined (V_{CC} to GND shorted)					53	pF
Leakage	Current Leakage between GndA to GndB	All channels combined (V_{CC} both sides are powered on and inputs are all low)	1.71V – 5.5V	1.71V – 5.5V			2	µA
Leakage	Current Leakage between GndA to GndB	All channels combined (V_{CC} both sides are powered on and inputs are all high)	1.71V – 5.5V	1.71V – 5.5V			44	µA
Leakage	Current Leakage between GndA to GndB	All channels combined (V_{CC} to GND shorted)	1.71V – 5.5V	1.71V – 5.5V			2	µA
CMTI	Common Mode Transient Immunity	Input toggling at 100Mbps Ground shift up to 40V	1.71V – 5.5V	1.71V – 5.5V		1		kV/µs
I_{CCA}	V_{CCA} supply current	V_I = V_{CCI} or GND I_O = 0	1.71V – 5.5V	1.71V – 5.5V	546		1220	µA
			0 V	5.5 V	-3		13	
			5.5 V	0 V	509		1050	
		V_I = GND I_O = 0	5.5 V	Floating(5)	509		1050	
I_{CCB}	V_{CCB} supply current	V_I = V_{CCI} or GND I_O = 0	1.71V – 5.5V	1.71V – 5.5V	760		1836	µA
			0 V	5.5 V	654		1350	
			5.5 V	0 V	-3		36	
		V_I = GND I_O = 0	Floating(5)	5.5 V	656		1350	
I_{CCA} + I_{CCB}	Supply Current - Disable	EN = 0	1.8V	1.8V	1.9		3.1	mA
			2.5V	2.5V	1.9		3.1	
			3.3V	3.3V	2.0		3.1	
			5V	5V	2.1		3.3	

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over operating free-air temperature range (unless otherwise noted)(1) (2)

PARAMETER		TEST CONDITIONS	V_{CCA}	V_{CCB}	Operating free-air temperature (T_A) –40°C to 125°C			UNIT
					MIN	TYP	MAX	
I_{CCA} + I_{CCB}	Supply Current - DC Signal	$V_I = V_{CCI}$	1.8V	1.8V	1		2.65	mA
			2.5V	2.5V	1.3		2.7	
			3.3V	3.3V	1.3		2.8	
			5V	5V	1.4		3.1	
		V_I = GND	1.8V	1.8V	1.2		2.7	mA
			2.5V	2.5V	1.3		2.7	
			3.3V	3.3V	1.3		2.8	
			5V	5V	1.4		3.1	
I_{CCA} + I_{CCB}	Supply Current - AC Signal	All channels switching with square wave clock input; CL = 15 pF, 1Mbps	1.8V	1.8V	1.5		2.6	mA
			2.5V	2.5V	1.6		2.7	
			3.3V	3.3V	1.6		2.8	
			5V	5V	1.9		3.3	
		All channels switching with square wave clock input; CL = 15 pF, 50Mbps	1.8V	1.8V	9.2		12.1	mA
			2.5V	2.5V	10.8		14	
			3.3V	3.3V	12.4		16.2	
			5V	5V	17.6		20.6	
		All channels switching with square wave clock input; CL = 15 pF, 100Mbps	1.8V	1.8V	16.5		20.1	mA
			2.5V	2.5V	20.2		24.7	
			3.3V	3.3V	24.1		29	
			5V	5V	35		38	
V_{UVLO+}	Positive-Going Undervoltage Lockout Voltage	A Supply	1.71V – 5.5V				1548	mV
		B Supply		1.71V – 5.5V			1548	
V_{UVLO-}	Negative-Going Undervoltage Lockout Voltage	A Supply	1.71V – 5.5V		1492			mV
		B Supply		1.71V – 5.5V	1492			
V_{UVLO_Hys}	Undervoltage Lockout Hysteresis	A Supply	1.71V – 5.5V		35		132	mV
		B Supply		1.71V – 5.5V	35		132	

(1) V_{CCI} is the V_{CC} associated with the input port and referenced to GND_A
(2) V_{CCO} is the V_{CC} associated with the output port and referenced to GND_B
(3) Tested at $V_I = V_{T+(MAX)}$
(4) Tested at $V_I = V_{T-(MIN)}$
(5) Floating is defined as a node that is both not actively driven by an external device and has leakage not exeeding 10nA

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5.5 Switching Characteristics, V_{CCA} = 1.8 ± 0.15 V

PARAMETER		TEST CONDITIONS	FROM	TO	TEMPERATURE	B-Port Supply Voltage (V_{CCB})									UNIT
						1.8 ± 0.15 V			2.5 ± 0.2 V			3.3 ± 0.3 V			5.0 ± 0.5 V			
						MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
t_{pd}	Propagation delay	1Mbps all 4 channels toggling	A	B	-40°C to 85°C	3		7.4	3		7.5	3.1		7.5	3.1		7.9	ns
			A	B	-40°C to 125°C	3		7.8	3		7.8	3.1		7.9	3.1		8.4	
			B	A	-40°C to 85°C	3		7.4	2.8		5.8	2.8		5.2	2.8		4.9	
			B	A	-40°C to 125°C	3		7.8	2.8		6.1	2.8		5.5	2.8		5.2	
t_{dis}	Disable time		OE	A	-40°C to 85°C	17.6		40.9	12.6		28.2	14.7		27.4	10		18.8	ns
			OE	A	-40°C to 125°C	17.6		42	12.6		29.1	14.7		28	10		19.3	
			OE	B	-40°C to 85°C	16.1		35	16.1		35	16.1		35	16.1		35	
			OE	B	-40°C to 125°C	16.1		35.6	16.1		35.5	16.1		35.6	16.1		35.6	
t_{en}	Enable time		OE	A	-40°C to 85°C	7.5		26.5	5.5		15.3	4.5		11	3.8		7.9	ns
			OE	A	-40°C to 125°C	7.9		27.5	5.5		16.3	4.5		11.8	3.8		8.4	
			OE	B	-40°C to 85°C	5.4		18.1	5.4		18.1	5.4		18.1	5.4		18.1	
			OE	B	-40°C to 125°C	5.4		18.9	5.4		18.8	5.4		18.9	5.4		18.8	
PWD	Pulse width distortion	$\lvert t_{phl} - t_{plh} \rvert$	A	B	-40°C to 85°C			1.6			1.5			1.4			1.3	ns
			A	B	-40°C to 125°C			1.6			1.5			1.4			1.3	
			B	A	-40°C to 85°C			1.6			1.5			1.4			1.3	
			B	A	-40°C to 125°C			1.6			1.5			1.4			1.4	
t_r	Output signal rise time		A	B	-40°C to 85°C			1.1			1.2			1.5			1.8	ns
			A	B	-40°C to 125°C	0.6		1.3	0.5		1.5	0.5		1.6	0.6		1.9	
			B	A	-40°C to 85°C	0.5		0.9	0.5		1	0.5		0.9	0.5		0.9	
			B	A	-40°C to 125°C	0.5		1	0.5		1.1	0.5		1	0.5		1.1	
tf	Output signal fall time		A	B	-40°C to 85°C	0.5		1.3	0.5		1.6	0.5		1.6	0.6		1.9	ns
			A	B	-40°C to 125°C	0.5		1.6	0.5		1.8	0.5		1.9	0.6		2.2	
			B	A	-40°C to 85°C	0.5		1.1	0.5		1.1	0.5		1.1	0.5		1.1	
			B	A	-40°C to 125°C	0.5		1.4	0.5		1.5	0.5		1.4	0.5		1.4	
t_{DO}	Default output delay time from input power loss	Measured from the time V_{CC} goes below 1.49V			-40°C to 85°C	4.2		7.7	4.1		7.6	4.1		7.5	3.9		7.4	µs
					-40°C to 125°C	4.2		7.7	4.1		7.6	4.1		7.5	3.9		7.4	
t_{PU}	Time from ULVO to valid output data				-40°C to 85°C	21.2		54.2	21.2		54.1	21.2		54.1	21.2		54.1	µs
					-40°C to 125°C	20.8		54.2	20.8		54.1	20.8		54.1	20.8		54.1	

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5.6 Switching Characteristics, V_{CCA} = 2.5 ± 0.2 V

PARAMETER		TEST CONDITIONS	FROM	TO	TEMPERATURE	B-Port Supply Voltage (V_{CCB})									UNIT
						1.8 ± 0.15 V			2.5 ± 0.2 V			3.3 ± 0.3 V			5.0 ± 0.5 V			
						MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
t_{pd}	Propagation delay	1Mbps all 4 channels toggling	A	B	-40°C to 85°C	2.9		5.9	2.9		5.9	2.9		6	3		6.2	ns
			A	B	-40°C to 125°C	2.9		6.1	2.9		6.2	2.9		6.3	3		6.6	
			B	A	-40°C to 85°C	3		7.4	2.9		5.9	2.8		5.2	2.8		5	
			B	A	-40°C to 125°C	3		7.8	2.9		6.2	2.8		5.6	2.8		5.4	
t_{dis}	Disable time		OE	A	-40°C to 85°C	17.6		40.9	12.6		28.3	14.7		27.4	10.1		18.8	ns
			OE	A	-40°C to 125°C	17.6		41.9	12.6		29.1	14.7		28	10.1		19.3	
			OE	B	-40°C to 85°C	11.6		24.7	11.6		24.7	11.6		24.7	11.6		24.7	
			OE	B	-40°C to 125°C	11.6		25.2	11.6		25.2	11.6		25.2	11.6		25.2	
t_{en}	Enable time		OE	A	-40°C to 85°C	7.5		26.5	5.5		15.3	4.5		11	3.8		7.8	ns
			OE	A	-40°C to 125°C	7.9		27.5	5.5		16.3	4.5		11.8	3.8		8.4	
			OE	B	-40°C to 85°C	3.8		10.9	3.8		10.9	3.8		10.9	3.8		10.9	
			OE	B	-40°C to 125°C	3.8		11.6	3.8		11.6	3.8		11.6	3.8		11.6	
PWD	Pulse width distortion	$\lvert t_{phl} - t_{plh} \rvert$	A	B	-40°C to 85°C			0.9			0.8			0.8			0.7	ns
			A	B	-40°C to 125°C			0.9			0.8			0.8			0.7	
			B	A	-40°C to 85°C			0.9			0.8			0.8			0.7	
			B	A	-40°C to 125°C			0.9			0.8			0.8			0.7	
t_r	Output signal rise time		A	B	-40°C to 85°C	0.6		1.1	0.5		1.2	0.5		1.5	0.6		1.8	ns
			A	B	-40°C to 125°C	0.6		1.3	0.5		1.4	0.5		1.7	0.6		1.9	
			B	A	-40°C to 85°C	0.5		1	0.5		1	0.5		1	0.5		1	
			B	A	-40°C to 125°C	0.5		1.1	0.5		1.2	0.5		1.2	0.5		1.1	
tf	Output signal fall time		A	B	-40°C to 85°C	0.5		1.2	0.5		1.5	0.5		1.7	0.5		1.9	ns
			A	B	-40°C to 125°C	0.5		1.6	0.5		1.7	0.5		1.8	0.5		2.1	
			B	A	-40°C to 85°C	0.5		1.3	0.5		1.3	0.5		1.4	0.5		1.3	
			B	A	-40°C to 125°C	0.5		1.5	0.5		1.5	0.5		1.5	0.5		1.6	
t_{DO}	Default output delay time from input power loss	Measured from the time V_{CC} goes below 1.49V)			-40°C to 85°C	4.2		7.7	4.1		7.6	4.1		7.5	3.9		7.4	µs
					-40°C to 125°C	4.2		7.7	4.1		7.6	4.1		7.5	3.9		7.4	
t_{PU}	Time from ULVO to valid output data				-40°C to 85°C	26		61	26		61.1	26		61	26		61	µs
					-40°C to 125°C	25.6		61	25.6		61.1	25.6		61	25.6		61	

5.7 Switching Characteristics, V_{CCA} = 3.3 ± 0.3 V

PARAMETER		TEST CONDITIONS	FROM	TO	TEMPERATURE	B-Port Supply Voltage (V_{CCB})									UNIT
						1.8 ± 0.15 V			2.5 ± 0.2 V			3.3 ± 0.3 V			5.0 ± 0.5 V			
						MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
t_{pd}	Propagation delay	1Mbps all 4 channels toggling	A	B	-40°C to 85°C	2.9		5.2	2.9		5.3	2.8		5.4	3		5.7	ns
			A	B	-40°C to 125°C	2.9		5.5	2.9		5.6	2.8		5.8	3		6.1	
			B	A	-40°C to 85°C	3		7.5	2.9		5.9	2.8		5.3	2.8		5.1	
			B	A	-40°C to 125°C	3		7.9	2.9		6.3	2.8		5.7	2.8		5.5	
t_{dis}	Disable time		OE	A	-40°C to 85°C	17.6		40.9	12.6		28.2	14.7		27.4	10.1		18.8	ns
			OE	A	-40°C to 125°C	17.6		41.9	12.6		29	14.7		28	10.1		19.3	
			OE	B	-40°C to 85°C	13.9		25.3	13.8		25.3	13.8		25.3	13.8		25.3	
			OE	B	-40°C to 125°C	13.9		25.7	13.8		25.7	13.8		25.7	13.8		25.7	
t_{en}	Enable time		OE	A	-40°C to 85°C	7.5		26.5	5.5		15.3	4.5		11	3.8		7.8	ns
			OE	A	-40°C to 125°C	8		27.5	5.5		16.3	4.5		11.8	3.8		8.4	
			OE	B	-40°C to 85°C	3		8	3.1		8	3.1		8	3		8	
			OE	B	-40°C to 125°C	3		8.5	3.1		8.5	3.1		8.6	3		8.5	
PWD	Pulse width distortion	$\lvert t_{phl} - t_{plh} \rvert$	A	B	-40°C to 85°C			0.7			0.6			0.5			0.5	ns
			A	B	-40°C to 125°C			0.7			0.6			0.5			0.5	
			B	A	-40°C to 85°C			0.7			0.6			0.5			0.5	
			B	A	-40°C to 125°C			0.7			0.6			0.5			0.5	
t_r	output signal rise time		A	B	-40°C to 85°C	0.6		1.1	0.6		1.2	0.5		1.5	0.6		1.8	ns
			A	B	-40°C to 125°C	0.6		1.3	0.6		1.5	0.5		1.7	0.6		1.9	
			B	A	-40°C to 85°C	0.6		1.1	0.6		1.2	0.5		1.5	0.6		1.8	
			B	A	-40°C to 125°C	0.6		1.3	0.6		1.5	0.5		1.7	0.6		1.9	
tf	output signal fall time		A	B	-40°C to 85°C	0.5		1.2	0.5		1.6	0.5		1.6	0.6		1.9	ns
			A	B	-40°C to 125°C	0.5		1.7	0.5		1.7	0.5		1.8	0.6		2.1	
			B	A	-40°C to 85°C	0.5		1.4	0.5		1.5	0.5		1.4	0.5		1.5	
			B	A	-40°C to 125°C	0.5		1.7	0.5		1.7	0.5		1.7	0.5		1.6	
t_{DO}	Default output delay time from input power loss	Measured from the time V_{CC} goes below 1.49V			-40°C to 85°C	4.2		7.7	4.1		7.6	4.1		7.5	3.9		7.4	µs
					-40°C to 125°C	4.2		7.7	4.1		7.6	4.1		7.5	3.9		7.4	
t_{PU}	Time from ULVO to valid output data				-40°C to 85°C	26		61	26		61.1	26		61	26		61	µs
					-40°C to 125°C	25.6		61	25.6		61.1	25.6		61	25.6		61	

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5.8 Switching Characteristics, V_{CCA} = 5.0 ± 0.5 V

PARAMETER		TEST CONDITIONS	FROM	TO	TEMPERATURE	B-Port Supply Voltage (V_{CCB})												UNIT
						1.8 ± 0.15 V			2.5 ± 0.2 V			3.3 ± 0.3 V			5.0 ± 0.5 V			
						MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
t_{pd}	Propagation delay	1Mbps all 4 channels toggling	A	B	-40°C to 85°C	2.8		5	2.8		5	2.9		5.2	2.9		5.5	ns
			A	B	-40°C to 125°C	2.8		5.3	2.8		5.3	2.9		5.6	2.9		5.9	
			B	A	-40°C to 85°C	3.1		7.8	3		6.3	2.9		5.7	2.8		5.6	
			B	A	-40°C to 125°C	3.1		8.3	3		6.6	2.9		6.1	2.8		5.8	
t_{dis}	Disable time		OE	A	-40°C to 85°C	17.7		40.9	12.6		28.3	14.7		27.4	10.1		18.8	ns
			OE	A	-40°C to 125°C	17.7		41.9	12.6		29.1	14.7		28	10.1		19.4	
			OE	B	-40°C to 85°C	9.4		17.4	9.4		17.4	9.4		17.4	9.4		17.4	
			OE	B	-40°C to 125°C	9.4		17.7	9.4		17.7	9.4		17.7	9.4		17.7	
t_{en}	Enable time		OE	A	-40°C to 85°C	7.5		26.5	5.5		15.3	4.5		11	3.8		7.8	ns
			OE	A	-40°C to 125°C	8		27.5	5.5		16.3	4.5		11.8	3.8		8.4	
			OE	B	-40°C to 85°C	2.5		5.9	2.5		5.9	2.5		5.9	2.5		5.9	
			OE	B	-40°C to 125°C	2.5		6.3	2.5		6.3	2.5		6.3	2.5		6.3	
PWD	Pulse width distortion	$\lvert t_{phl} - t_{plh} \rvert$	A	B	-40°C to 85°C			0.5			0.4			0.3			0.3	ns
			A	B	-40°C to 125°C			0.5			0.4			0.3			0.3	
			B	A	-40°C to 85°C			0.5			0.4			0.3			0.3	
			B	A	-40°C to 125°C			0.5			0.4			0.3			0.3	
t_r	Output signal rise time		A	B	-40°C to 85°C	0.6		1.1	0.5		1.1	0.5		1.6	0.6		1.8	ns
			A	B	-40°C to 125°C	0.6		1.3	0.5		1.5	0.5		1.7	0.6		1.9	
			B	A	-40°C to 85°C	0.5		1.6	0.5		1.6	0.5		1.7	0.5		1.7	
			B	A	-40°C to 125°C	0.5		1.7	0.5		1.7	0.5		1.8	0.5		1.7	
tf	Output signal fall time		A	B	-40°C to 85°C	0.5		1.4	0.4		1.6	0.5		1.8	0.6		1.9	ns
			A	B	-40°C to 125°C	0.5		1.7	0.5		1.7	0.5		1.8	0.6		2.2	
			B	A	-40°C to 85°C	0.5		1.4	0.5		1.6	0.5		1.8	0.6		1.9	
			B	A	-40°C to 125°C	0.5		1.7	0.5		1.7	0.5		1.8	0.6		2.2	
t_{DO}	Default output delay time from input power loss	Measured from the time V_{CC} goes below 1.49V			-40°C to 85°C	4.2		7.7	4.1		7.6	4.1		7.5	3.9		7.4	µs
					-40°C to 125°C	4.2		7.7	4.1		7.6	4.1		7.5	3.9		7.4	
t_{PU}	Time from ULVO to valid output data				-40°C to 85°C	43.7		96.6	43.7		96.6	43.7		96.6	43.7		96.6	µs
					-40°C to 125°C	43.7		96.6	43.7		96.6	43.7		96.6	43.7		96.6	

5.9 Switching Characteristics: T_{sk}, T_{MAX}

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		V_{CCI}	V_{CCO}	Operating free-air temperature (T_A)			UNIT
						-40°C to 125°C			
						MIN	TYP	MAX	
T_{MAX}	Maximum Data Rate	50% Duty Cycle Input One channel switching 20% of pulse > 0.7*V_{CCO} 20% of pulse < 0.3*V_{CCO}	No Translation	1.65 V - 1.95 V	1.65 V - 1.95 V	100			Mbps
				2.3 V - 2.7 V	2.3 V - 2.7 V	100			Mbps
				3.0 V - 3.6 V	3.0 V - 3.6 V	100			Mbps
				4.5 V - 5.5 V	4.5 V - 5.5 V	100			Mbps
			Up Translation	1.65 V - 1.95 V	2.3 V - 2.7 V	100			Mbps
				1.65 V - 1.95 V	3.0 V - 3.6 V	100			Mbps
				1.65 V - 1.95 V	4.5 V - 5.5 V	100			Mbps
				2.3 V - 2.7 V	3.0 V - 3.6 V	100			Mbps
				2.3 V - 2.7 V	4.5 V - 5.5 V	100			Mbps
				3.0 V - 3.6 V	4.5 V - 5.5 V	100			Mbps
			Down Translation	2.3 V - 2.7 V	1.65 V - 1.95 V	100			Mbps
				3.0 V - 3.6 V	2.3 V - 2.7 V	100			Mbps
				3.0 V - 3.6 V	1.65 V - 1.95 V	100			Mbps
				4.5 V - 5.5 V	3.0 V - 3.6 V	100			Mbps
				4.5 V - 5.5 V	2.3 V - 2.7 V	100			Mbps
				4.5 V - 5.5 V	1.65 V - 1.95 V	100			Mbps

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over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		V_{CCI}	V_{CCO}	Operating free-air temperature (T_A)			UNIT
						-40°C to 125°C			
						MIN	TYP	MAX	
t_{sk}	Output skew	Timing skew between any switching outputs on the rising or falling edge (same direction channels)	No Translation	1.65 V - 1.95 V	1.65 V - 1.95 V			2	ns
				2.3 V - 2.7 V	2.3 V - 2.7 V			2	ns
				3.0 V - 3.6 V	3.0 V - 3.6 V			2	ns
				4.5 V - 5.5 V	4.5 V - 5.5 V			2	ns
			Up Translation	1.65 V - 1.95 V	2.3 V - 2.7 V			2	ns
				1.65 V - 1.95 V	3.0 V - 3.6 V			2	ns
				1.65 V - 1.95 V	4.5 V - 5.5 V			2	ns
				2.3 V - 2.7 V	3.0 V - 3.6 V			2	ns
				2.3 V - 2.7 V	4.5 V - 5.5 V			2	ns
				3.0 V - 3.6 V	4.5 V - 5.5 V			2	ns
			Down Translation	2.3 V - 2.7 V	1.65 V - 1.95 V			2	ns
				3.0 V - 3.6 V	2.3 V - 2.7 V			2	ns
				3.0 V - 3.6 V	1.65 V - 1.95 V			2	ns
				4.5 V - 5.5 V	3.0 V - 3.6 V			2	ns
				4.5 V - 5.5 V	2.3 V - 2.7 V			2	ns
				4.5 V - 5.5 V	1.65 V - 1.95 V			2	ns

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6 AC Noise Tolerance

TXG404x supports I/O voltage translation in environments with noisy grounds. The plot below illustrates the amount of noise that TXG404x can reject in terms of peak-to-peak voltage over frequency.

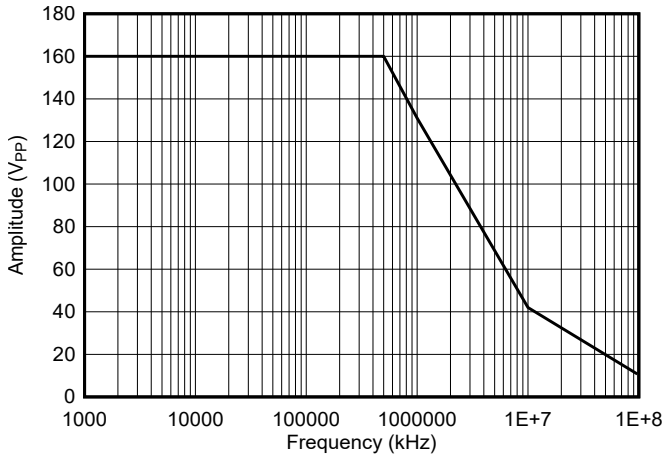

Figure 6-1. AC Noise Rejection Plot

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7 Detailed Description

7.1 Overview

The TXG404x-Q1 is a 4-bit translating transceiver that uses two individually configurable power-supply rails. The device is operational with V_{CCA} and V_{CCB} supplies as low as 1.71V and as high as 5.5V. The A port is designed to track V_{CCA}, and the B port is designed to track V_{CCB}. In addition to I/O level shifting, the device supports ground mismatch between two systems up to +/-40V.

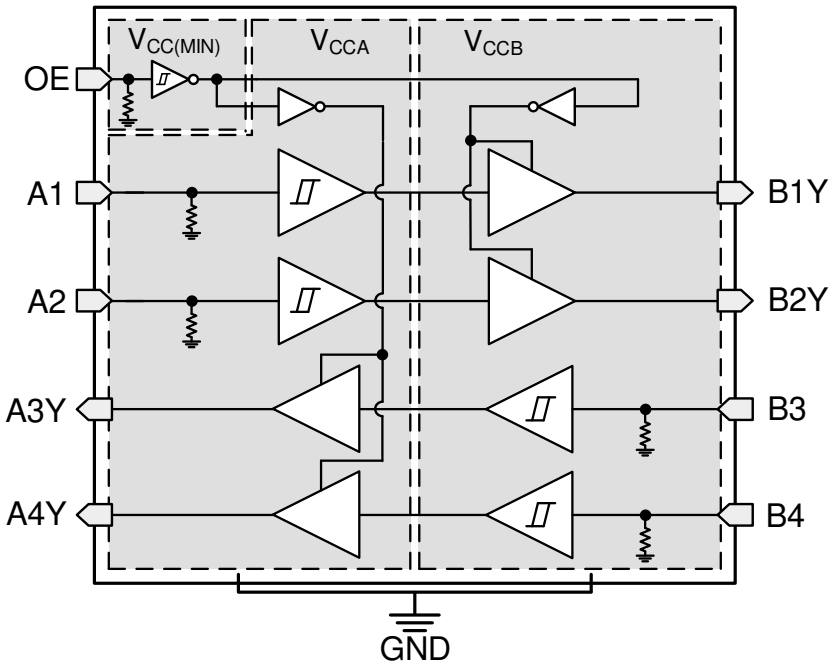
The TXG404x-Q1 device is designed for asynchronous communication between data buses, and transmits data with fixed direction from the A bus to the B bus on some channels and from the B bus to the A bus on the remaining channels. The output-enable input (OE) is used to disable the outputs so the buses are effectively isolated. The output-enable pin (OE) can be referenced to either V_{CCA} or V_{CCB}. The OE pin can be left floating or externally pulled down to ground to keep the level shifter outputs in a high-impedance state during power-up or power-down.

This device is fully specified for partial-power-down applications using the I_{off} current. The I_{off} protection circuitry ensures that no excessive current is drawn from or sourced into an input or output while the device is powered down.

The V_{CC} disconnect feature ensures that if V_{CC} is disconnected with the complementary supply within recommended operating conditions, outputs are disabled and set to the high-impedance state while the supply current is maintained. The $I_{off-float}$ circuitry ensures that no excessive current is drawn from or sourced into an input or output while the supply is floating.

Glitch-free power supply sequencing allows either supply rail to be powered on or off in any order while providing robust power sequencing performance.

7.2 Functional Block Diagram



7.3 Device Functional Modes

Table 7-1. Function Table

Power Supply (1)		Control Inputs	Port Status	
VCCI	VCCO	OE	Input	Output
PU	PU	H	H	H
PU	PU	H	L	L
PU	PU	L or Open	X	Hi-Z
PU	PU	H	Open	L
PD	PU	H	X	L
X	PU	L or Open	X	High-Z
X	PU	H	X	L
X	PD	X	X	Undetermined

(1) In the table above: PU = Powered Up; PD = Powered Down; X = Irrelevant; H = High Level; L = Low Level; Open = Floating

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8 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

8.1 Application Information

The TXG404x-Q1 device is used for level translation, enabling communication between devices or systems operating at different interface voltages and ground voltages. Figure 8-1 is an example of two systems that translate from 3.3V to 1.8V across an SPI interface while also experiencing a ground shift of 5V. The ground shift occurs due to the parasitic resistance of the cable used to connect the 48V battery ground and 12V battery ground to the chassis of the car. The TXG404x-Q1 device is ideal for use in applications where a push-pull driver is connected to the data inputs.

8.2 Typical Application

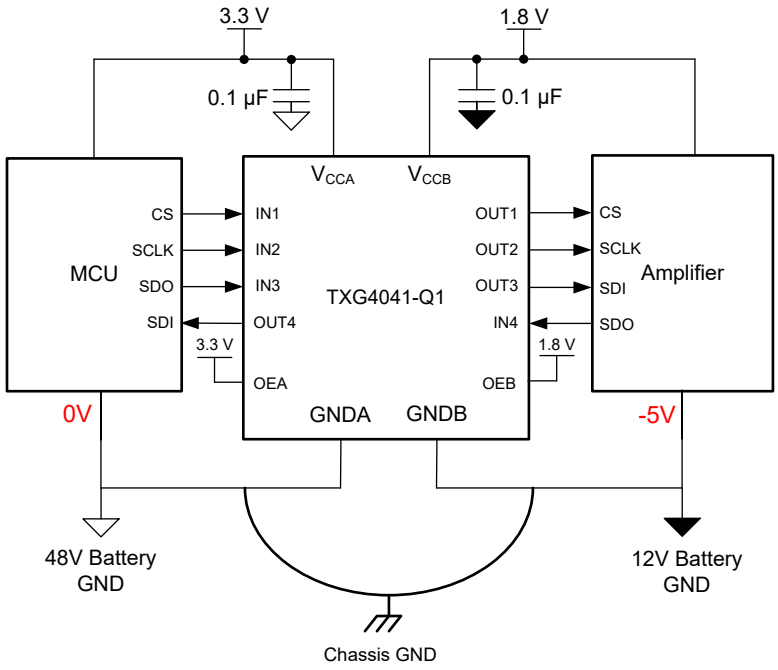

Figure 8-1. TXG404x SPI Interface Application in Automotive

8.2.1 Design Requirements

Use the parameters listed in Table 8-1 for this design example.

Table 8-1. Design Parameters

DESIGN PARAMETERS	EXAMPLE VALUES
Input voltage range	1.71V to 5.5V
Output voltage range	1.71V to 5.5V

8.2.2 Application Curve

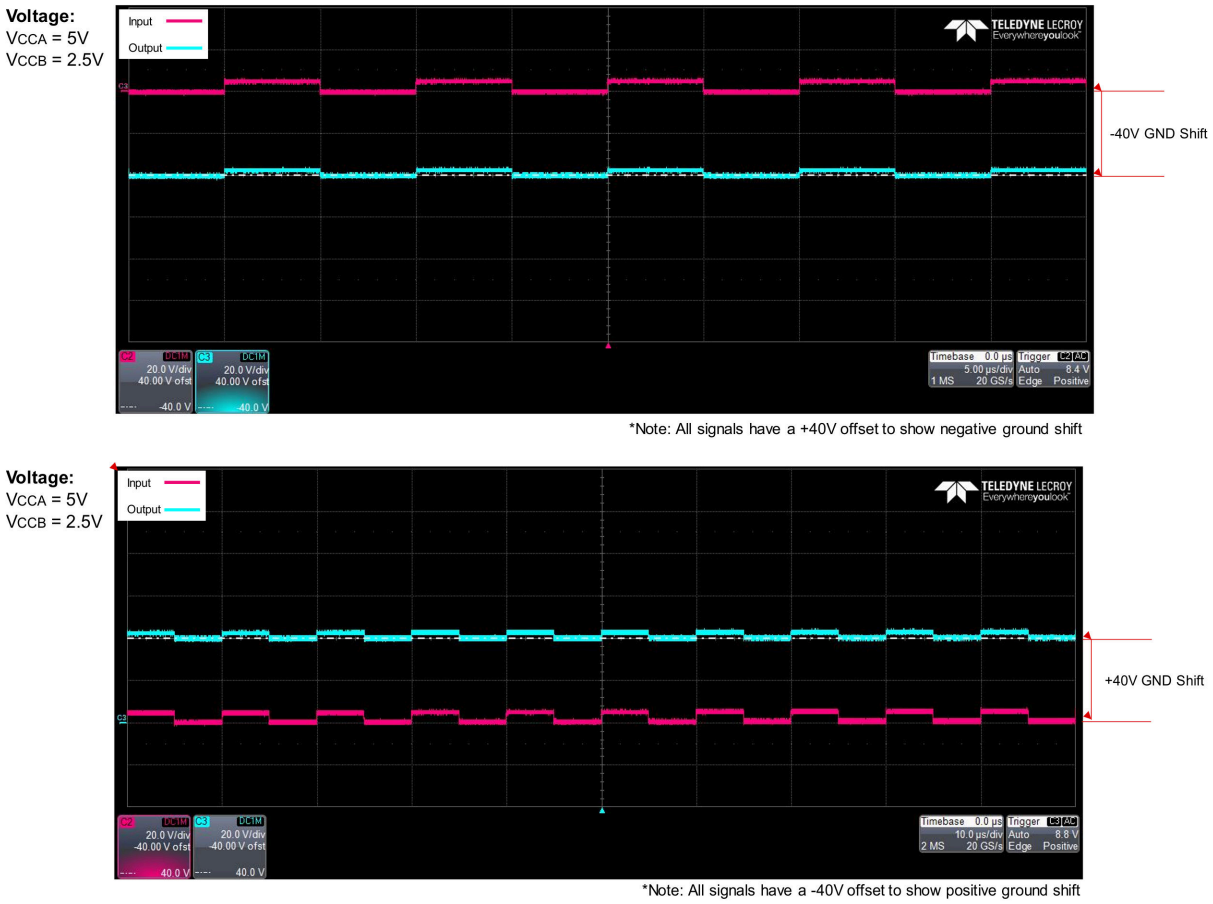

Figure 8-2. Waveform showing -40V (top) and +40V (bottom) Ground Shift with 2.25V to 5V I/O Translation

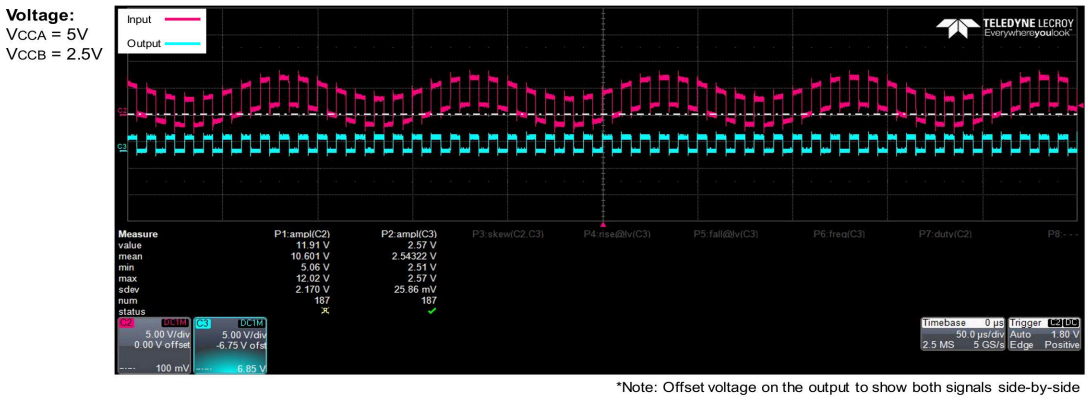

Figure 8-3. Waveform showing 5V to 2.5V I/O Translation with AC Ground Noise of 10kHz at $2V_{PP}$

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8.3 Power Supply Recommendations

Always apply a ground reference to the GND pins first. This device is designed for glitch free power sequencing without any supply sequencing requirements such as ramp order or ramp rate. Please make sure the difference between VCC and GND remains at 6.5V max at all times.

8.4 Layout

8.4.1 Layout Guidelines

To ensure reliability of the device, following common printed-circuit board layout guidelines are recommended:

- Use bypass capacitors on the power supply pins and place them as close to the device as possible. A 0.1µF capacitor is recommended, but transient performance can be improved by having 1µF and 0.1µF capacitors in parallel as bypass capacitors.
- The high drive capability of this device creates fast edges into light loads so routing and load conditions should be considered to prevent ringing.
- A 0.1µF capacitor can be added between GNDA and GNDB to improve performances of CMTI.

8.4.2 Layout Example

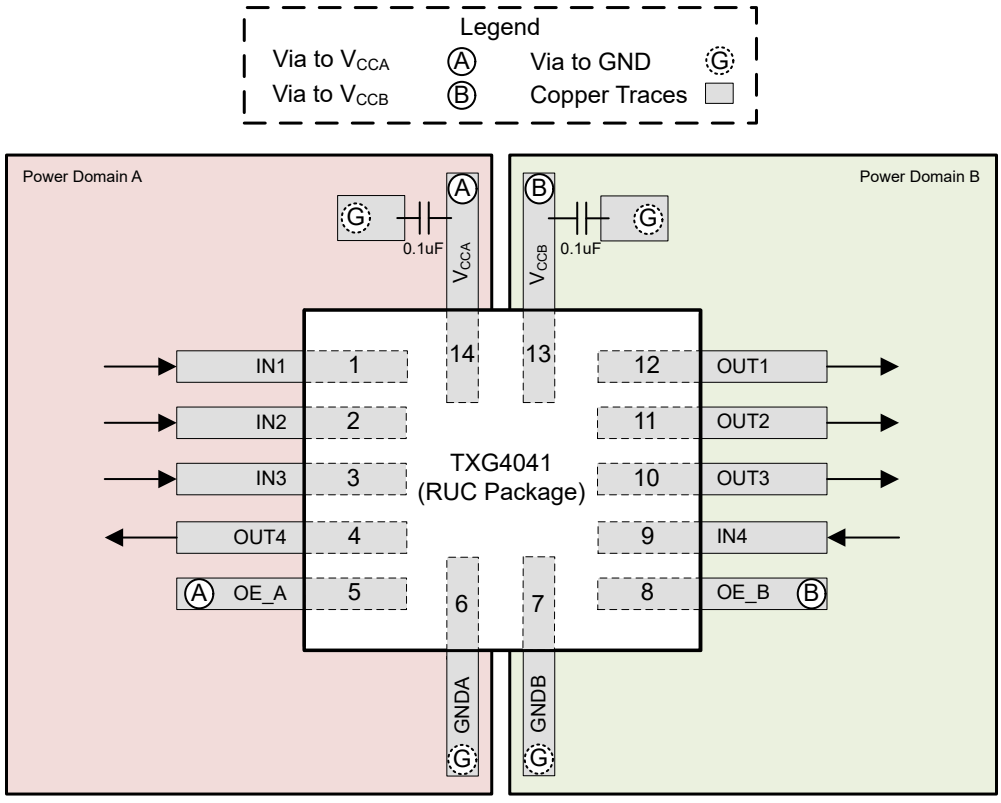

Figure 8-4. Layout Example

9 Device and Documentation Support

9.1 Documentation Support

9.1.1 Related Documentation

For related documentation, see the following:

- Texas Instruments, *Understanding Schmitt Triggers* application report
- Texas Instruments, *CMOS Power Consumption and C_{pd} Calculation* application report

9.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

9.3 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

9.4 Trademarks

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9.5 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

9.6 Glossary

TI Glossary	This glossary lists and explains terms, acronyms, and definitions.

10 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

DATE	REVISION	NOTES
February 2025	*	Initial APL Release

11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

ADVANCE INFORMATION

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
PTXG4041QRUCRQ1	ACTIVE	QFN	RUC	14	3000	TBD	Call TI	Call TI	-40 to 125		Samples
PTXG4042QRUCRQ1	ACTIVE	QFN	RUC	14	3000	TBD	Call TI	Call TI	-40 to 125		Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

GENERIC PACKAGE VIEW

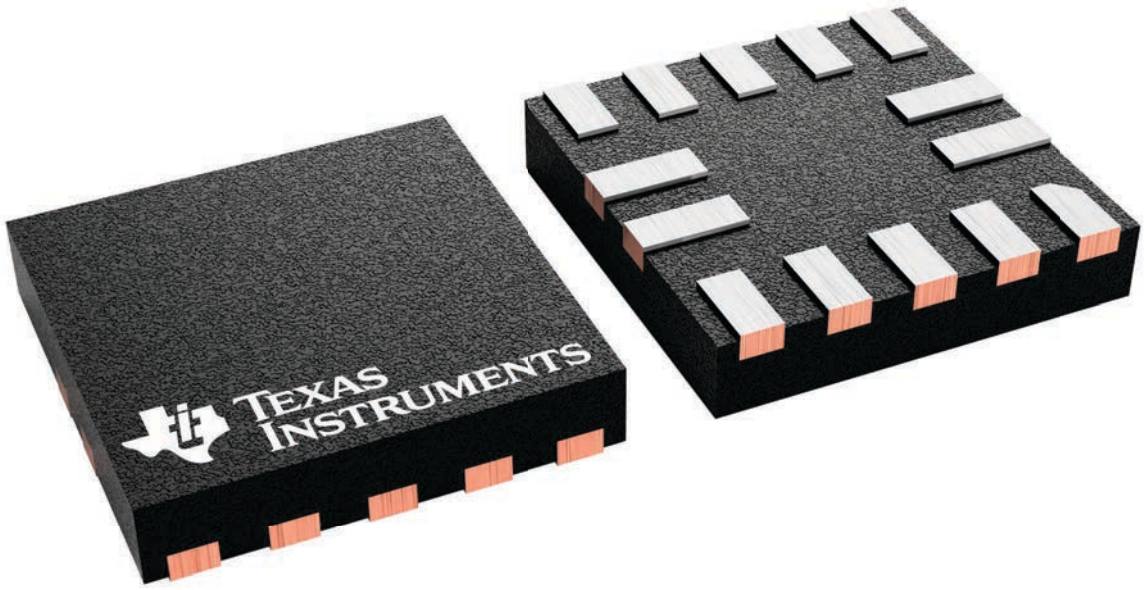
RUC 14

X2QFN - 0.4 mm max height

2 x 2, 0.4 mm pitch

PLASTIC QUAD FLATPACK - NO LEAD

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



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