UCC5350L-Q1 Single-Channel Isolated Gate Driver for SiC/IGBT and Automotive Applications

1 Features

- 5kV$_{RMS}$ single-channel isolated gate driver
- AEC-Q100 qualified for automotive applications
  - Temperature Grade 1
- Miller clamp, 12V UVLO
- ±10A typical peak current drive strength
- 3V to 15V input supply voltage
- Up to 30V driver supply voltage
- 100V/ns minimum CMTI
- Negative 5V handling capability on input pins
- 100ns (maximum) propagation delay and <25ns part-to-part skew
- 8-pin DWL (15.7mm creepage)
- Isolation barrier life > 40 Years
- Safety-related certifications planned:
  - UL 1577 Component Recognition program
  - DIN EN IEC 60747-17 (VDE 0884-17)
  - CQC - GB4943.1
- CMOS inputs
- Operating junction temperature: –40°C to +150°C

2 Applications

- On-board charger
- Traction inverter for EVs
- DC charging stations
- HVAC
- Heaters

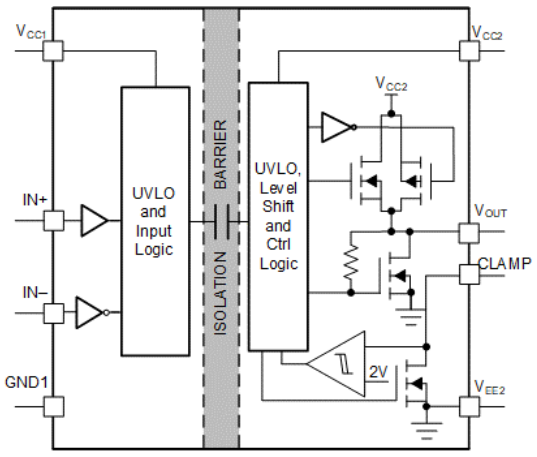
3 Description

The UCC5350L-Q1 is a single-channel, isolated gate driver with 10A source and 10A sink typical peak current designed to drive MOSFETs, IGBTs, and SiC MOSFETs. The UCC5350L-Q1 has the option for Miller clamp. The CLAMP pin is used to connect the transistor gate to an internal FET besides the output to prevent false turn-on caused by Miller current. The UCC5350L-Q1 is available in a 14mm wide body SOIC-8 (DWL) package and can support isolation voltage up to 5kV$_{RMS}$. The input side is isolated from the output side with SiO2 capacitive isolation technology with longer than 40 years isolation barrier lifetime. The UCC5350L-Q1 is a good fit for driving IGBTs or MOSFETs in applications such as high-voltage traction inverters and on-board chargers. Compared to an optocoupler, the device has lower part-to-part skew, lower propagation delay, higher operating temperature, and higher CMTI.

Device Information

PART VERSION	FEATURES	PACKAGE(1)	BODY SIZE (NOM)
UCC5350MCQDWL-Q1	Miller Clamp, 12V UVLO	DWL (SOIC-8)	14mm × 6.4mm

(1) For all available packages, see Section 13.



Functional Block Diagram

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4 Pin Configuration and Function

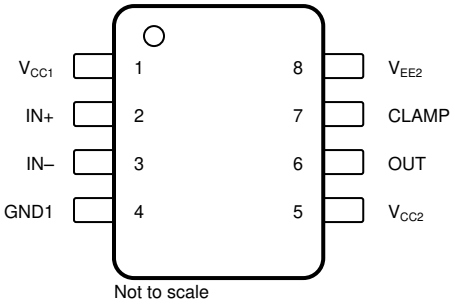


Figure 4-1. UCC5350L-Q1 8-Pin SOIC Top View

Table 4-1. Pin Functions

PIN		TYPE[1]	DESCRIPTION
NAME	UCC5350L-Q1		
V_{CC1}	1	P	Input supply voltage. Connect a locally decoupled capacitor to GND1. Use a low-ESR or ESL capacitor located as close to the device as possible.
V_{CC2}	5	P	Positive output supply rail. Connect a locally decoupled capacitor to V_{EE2}. Use a low-ESR or ESL capacitor located as close to the device as possible.
V_{EE2}	8	G	Ground pin. Connect to MOSFET source or IGBT emitter. Connect a locally decoupled capacitor from V_{CC2} to V_{EE2}. Use a low-ESR or ESL capacitor located as close to the device as possible.
GND1	4	G	Input ground. All signals on the input side are referenced to this ground.
IN+	2	I	Noninverting gate-drive voltage-control input. The IN+ pin has a CMOS input threshold. This pin is pulled low internally if left open. Use Table 7-4 to understand the input and output logic of these devices.
IN–	3	I	Inverting gate-drive voltage control input. The IN– pin has a CMOS input threshold. This pin is pulled high internally if left open. Use Table 7-4 to understand the input and output logic of these devices.
OUT	6	O	Gate-drive output
CLAMP	7	I	Active Miller-clamp input used to prevent false turn-on of the power switches

(1) P = Power, G = Ground, I = Input, O = Output

5 Specifications

5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
Input bias pin supply voltage	V_{CC1} - GND1	GND1–0.3	18	V
Driver bias supply	V_{CC2} - V_{EE2}	–0.3	35	V
Input pin voltage	IN+, IN-	GND1–5	V_{CC1}+0.3	V
Output signal voltage	Voltage on OUT	V_{EE2}–0.3	V_{CC2}+0.3	V
Clamp voltage	Voltage on CLMPE, reference to VEE	V_{EE2}–0.3	V_{CC2}+0.3	V
T_J	Junction temperature	–40	150	°C
T_{stg}	Storage temperature	–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Rating* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Condition*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

5.2 ESD Ratings (Automotive)

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per AEC Q100-002(1)	±4000	V
		Charged device model (CDM), per AEC Q100-011	±1500	

(1) AEC Q100-002 indicates that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

5.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

			MIN	MAX	UNIT
V_{CC1}	V_{CC1}-GND1		3	15	V
V_{CC2}	V_{CC2}-V_{EE2}		13.2	30	V
t_{PWM_MIN}	Minimum input pulse width (IN+ and IN-)		50		ns
T_J	Junction temperature		–40	150	°C

5.4 Thermal Information

THERMAL METRIC(1)		UCC5350L-Q1 DWL 8 Pins	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	87.1	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	47.4	V
$R_{\theta JB}$	Junction-to-board thermal resistance	41.2	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	33.9	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	39.7	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report.

5.5 Power Ratings

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
P_D	Maximum power dissipation on input and output	V_{CC1} = 15V, V_{CC2} = 15V, f = 1.9-MHz, 50% Duty Cycle, Square Wave, 2.2-nF load			1.04	W
P_{D1}	Maximum input power dissipation	V_{CC1} = 15V, V_{CC2} = 15V, f = 1.9-MHz, 50% Duty Cycle, Square Wave, 2.2-nF load			0.05	W
P_{D2}	Maximum output power dissipation	V_{CC1} = 15V, V_{CC2} = 15V, f = 1.9-MHz, 50% Duty Cycle, Square Wave, 2.2-nF load			0.99	W

5.6 Insulation Specifications

PARAMETER		TEST CONDITIONS	SPECIFICATION	UNIT
GENERAL				
CLR	External clearance(1)	Shortest terminal-to-terminal distance through air	> 14.7	mm
CPG	External Creepage(1)	Shortest terminal-to-terminal distance across the package surface	> 15.7	mm
DTI	Distance through the insulation	Minimum internal gap (internal clearance)	> 21	µm
CTI	Comparative tracking index	DIN EN 60112 (VDE 0303-11); IEC 60112	> 600	V
	Material Group	According to IEC 60664–1	I	
	Overvoltage Category per IEC 60664–1	Rated mains voltage ≤ 600 V_{RMS}	I-IV	
	Overvoltage Category per IEC 60664–1	Rated mains voltage ≤ 1000 V_{RMS}	I-III	
DIN EN IEC 60747-17 (VDE 0884-17)				
V_{IORM}	Maximum repetitive peak isolation voltage	AC voltage (bipolar)	2121	V_{PK}
V_{IOWM}	Maximum isolation working voltage	AC voltage (sine wave); time-dependent dielectric breakdown (TDDB) test; see Figure 1	1500	V_{RMS}
		DC voltage	2121	V_{DC}
V_{IOTM}	Maximum transient isolation voltage	V_{TEST} = V_{IOTM}, t = 60 s (qualification test) V_{TEST}= 1.2 × V_{IOTM}, t = 1 s (100% production test)	7000	V_{PK}
V_{IOSM}	Maximum surge isolation voltage(2)	Test method per IEC 60065, 1.2/50 µs waveform, V_{TEST} = 1.6 × V_{IOSM} (qualification)	8000	V_{PK}
q_{pd}	Apparent charge(3)	Method a: After I/O safety test subgroup 2/3, V_{ini} =V_{IOTM}, t_{ini} = 60 s; V_{pd}(m) = 1.2 × V_{IORM}, tm = 10 s	≤ 5	pC
		Method a: After environmental tests subgroup 1,V_{ini} = V_{IOTM}, t_{ini} = 60 s; $V_{pd(m)}$ = 1.6 × V_{IORM}, tm = 10 s	≤ 5	
		Method b1: At routine test (100% production) and preconditioning (type test), V_{ini} = V_{IOTM}, t_{ini} = 1 s; $V_{pd(m)}$ = 1.875 × V_{IORM} = x V_{PK}, t_m = 1 s	≤ 5	
C_{IO}	Barrier capacitance, input to output(4)	V_{IO} = 0.5 × sin (2πft), f = 1 MHz	~1.5	pF
R_{IO}	Insulation resistance, input to output(4)	V_{IO} = 500 V, T_A = 25°C	≥ 10^{12}	Ω
		V_{IO} = 500 V, 100°C ≤ T_A ≤ 125°C	≥ 10^{11}	
		V_{IO} = 500 V at T_S = 150°C	≥ 10^9	
	Pollution degree		2	
	Climatic category		40/125/21	
UL 1577				

5.6 Insulation Specifications (continued)

PARAMETER		TEST CONDITIONS	SPECIFICATION	UNIT
V_{ISO}	Withstand isolation voltage	$V_{TEST} = V_{ISO} = 5000\ V_{RMS}$, t = 60 s (qualification), $V_{TEST} = 1.2 \times V_{ISO} = 6000\ V_{RMS}$, t = 1 s (100% production)	5000	V_{RMS}

(1) Apply creepage and clearance requirements according to the specific equipment isolation standards of an application. Care must be taken to maintain the creepage and clearance distance of a board design to ensure that the mounting pads of the isolator on the printed circuit board (PCB) do not reduce this distance. Creepage and clearance on a PCB become equal in certain cases. Techniques such as inserting grooves and ribs on the PCB are used to help increase these specifications.
(2) Testing is carried out in air or oil to determine the intrinsic surge immunity of the isolation barrier.
(3) Apparent charge is electrical discharge caused by a partial discharge (pd).
(4) All pins on each side of the barrier tied together creating a two-pin device.

5.7 Safety-Related Certifications

VDE	UL	CQC
Plan to certify according to DIN EN IEC 60747-17 (VDE 0884-17)	Plan to certify under UL 1577Component Recognition Program	Plan to certify according to GB4943.1
Certificate Planned	Certificate Planned	Certificate Planned

5.8 Safety Limiting Values

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_S	Safety input, output, or supply current	R_{qJA} = 87.1°C/W, V_I = 15V, T_J = 150°C, T_A = 25°C			89.2	mA
		R_{qJA} = 87.1°C/W, V_I = 30V, T_J = 150°C, T_A = 25°C			44.6	
P_S	Safety input power	R_{qJA} = 87.1°C/W, T_J = 150°C, T_A = 25°C			0.05	W
P_S	Safety output power	R_{qJA} = 87.1°C/W, T_J = 150°C, T_A = 25°C			1.34	W
T_S	Maximum safety temperature(1)				150	°C

(1) The maximum safety temperature, T_S, has the same value as the maximum junction temperature, T_J, specified for the device. The I_S and P_S parameters represent the safety current and safety power respectively. The maximum limits of I_S and P_S should not be exceeded. These limits vary with the ambient temperature, T_A. The junction-to-air thermal resistance, R_{qJA}, in the Thermal Information table is that of a device installed on a high-K test board for leaded surface-mount packages. Use these equations to calculate the value for each parameter: $T_J = T_A + R_{qJA} \times P$, where P is the power dissipated in the device. $T_{J(max)} = T_S = T_A + R_{qJA} \times P_S$, where $T_{J(max)}$ is the maximum allowed junction temperature. $P_S = I_S \times V_I$, where VI is the maximum supply voltage.

5.9 Electrical Characteristics

VCC1 = 3.3 V or 5 V, 0.1-µF capacitor from VCC1 to GND1, VCC2= 15 V, 1-µF capacitor from VCC2 to VEE2, CL = 100-pF, TA = –40°C to +125°C, (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
SUPPLY CURRENTS						
I_{VCC1}	Input Supply Quiescent Current			1.67	2.4	mA
I_{VCC2}	Output Supply Quiescent Current			1.1	1.8	mA
VCC1 SUPPLY VOLTAGE UNDERVOLTAGE THRESHOLDS						
V_{VCC1_ON}	V_{CC1} UVLO Rising Threshold			2.6	2.8	V
V_{VCC1_OFF}	V_{CC1} UVLO Falling Threshold		2.4	2.5		
V_{VCC1_HYS}	V_{CC1} UVLO Threshold Hysteresis			0.1		
VCC2 SUPPLY VOLTAGE UNDERVOLTAGE THRESHOLDS AND DELAY						
V_{VCC2_ON}	V_{CC2} UVLO Rising Threshold			12	13	V
V_{VCC2_OFF}	V_{CC2} UVLO Falling Threshold		10.3	11		
V_{VCC2_HYS}	V_{CC2} UVLO Threshold Hysteresis			1		
LOGIC I/O						
$V_{IT+(IN)}$	Input High Threshold Voltage			$0.55*V_{CC1}$	$0.7*V_{CC1}$	V
$V_{IT-(IN)}$	Input Low Threshold Voltage		$0.3*V_{CC1}$	$0.45*V_{CC1}$		
$V_{hys\ (IN)}$	Input Threshold Hysteresis			$0.1*V_{CC1}$		
I_{IH}	INx Pin High Level Input Leakage Current	IN+ = V_{CC1}		40	240	µA
I_{IL}	INx Pin Low Level Input Leakage Current	IN- = GND1	-240	-40		µA
I_{IL}	IN- Pin Low Level Input Leakage Current	IN- = GND1 - 5V	-310	-80		µA
GATE DRIVER STAGE						
I_{OH}	Peak Output Source Current	IN+=high, IN-=low	5	10		A
I_{OL}	Peak Output Sink Current	IN+=low, IN-=high	5	10		A
V_{OH}	High Level Output Voltage (V_{CC2} - OUT)	I_{OUT} = -20mA	100	240		mV
V_{OL}	Low Level Output Voltage (OUT)	IN+ = low, IN- = high; I_{OUT} = 20mA	3	7		mV
SHORT CIRCUIT CLAMPING						
$V_{CLP-OUT}$	Clamping Voltage (V_{OUT} - V_{CC2})	IN+ = high, IN- = low, t_{CLAMP} = 10µs, I_{OUT} = 500mA		1	1.3	V
$V_{CLP-OUT}$	Clamping Voltage (V_{EE2} - V_{OUT})	IN+ = low, IN- = high, t_{CLAMP} = 10µs, I_{OUT} = -500mA		1.5		V
$V_{CLP-OUT}$	Clamping Voltage (V_{EE2} - V_{OUT})	IN+ = low, IN- = high, t_{CLAMP} = 10µs, I_{OUT} = -20mA		0.9	1	V
MILLER CLAMP						
V_{CLAMP}	Low-Level Clamp Voltage	I_{CLAMP} = 20mA		7	13	mV
I_{CLAMP}	Clamp Low-Level Current	V_{CLAMP} = V_{EE2} + 15V	5	10		A
$I_{CLAMP(L)}$	Clamp Low-Level Current For Low Output Voltage	V_{CLAMP} = V_{EE2} + 2V	5	10		A
$V_{CLAMP-TH}$	Clamp Threshold Voltage			2.1	2.3	V
ACTIVE PULL-DOWN						
V_{OUTSD}	Active Pulldown Votlage on OUT	I_{OUT} = 0.1 x $I_{OUT(typ)}$, V_{CC2} = open		1.8	2.5	V

5.10 Switching Characteristics

VCC1 = 3.3 V or 5 V, 0.1-µF capacitor from VCC1 to GND1, VCC2= 15 V, 1-µF capacitor from VCC2 to VEE2, CL = 100-pF, TJ = –40°C to +125°C

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_R	Output-Signal Rise Time	C_{LOAD}=1nF		10	26	ns
t_F	Output Fall Time	C_{LOAD}=1nF		10	22	ns
t_{PLH}	Propagation Delay – Low to High	C_{LOAD}=100pF		55	80	ns

5.10 Switching Characteristics (continued)

VCC1 = 3.3 V or 5 V, 0.1-µF capacitor from VCC1 to GND1, VCC2= 15 V, 1-µF capacitor from VCC2 to VEE2, CL = 100-pF, TJ = –40°C to +125°C

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PHL}	Propagation Delay – High to Low	C_{LOAD}=100pF		55	80	ns
t_{UVLO1_rec}	UVLO Recovery Delay of V_{CC1}			30		µs
t_{UVLO2_rec}	UVLO Recovery Delay of V_{CC2}			50		µs
t_{PWD}	Pulse Width Distortion	C_{LOAD}=100pF		1	20	ns
$t_{sk(pp)}$	Part-to-Part Skew	C_{LOAD}=100pF		1	25	ns
CMTI	Common-mode transient immunity	PWM is tied to GND or V_{CC1}, V_{CM} = 1200V	100	120		V/ns

5.11 Insulation Characteristics Curves

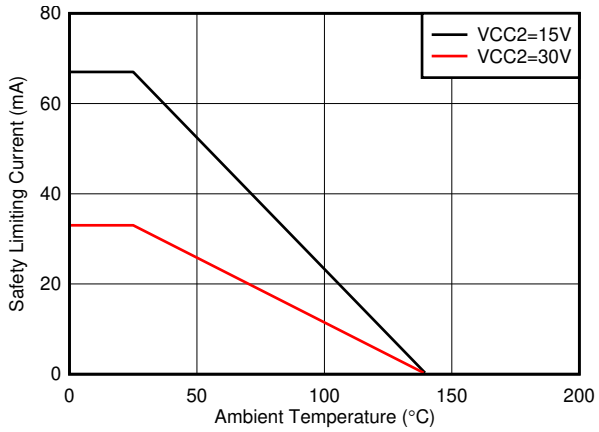


Figure 5-1. Thermal Derating Curve for Limiting Current per VDE

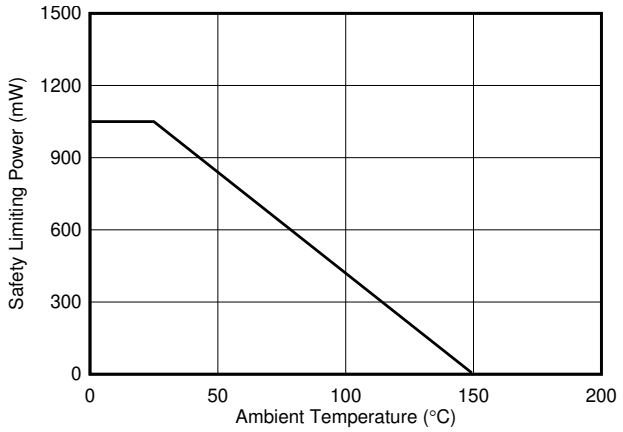


Figure 5-2. Thermal Derating Curve for Limiting Power per VDE

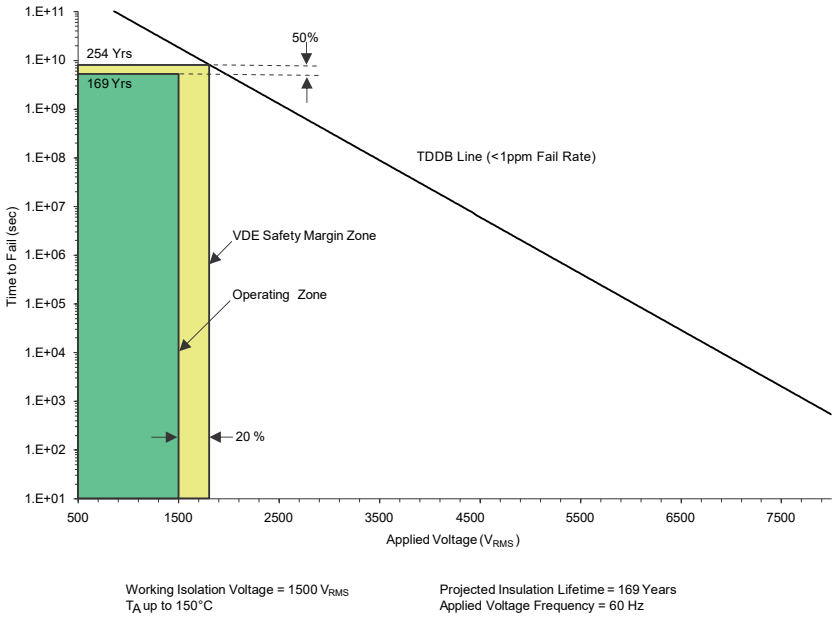
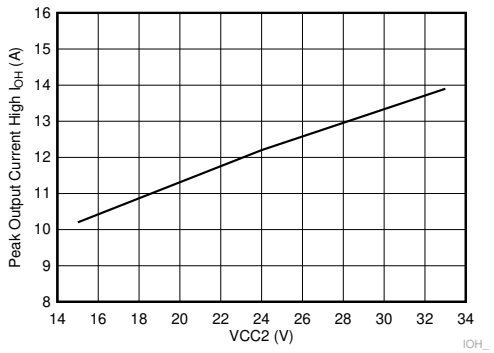


Figure 5-3. Insulation Lifetime Projection Data

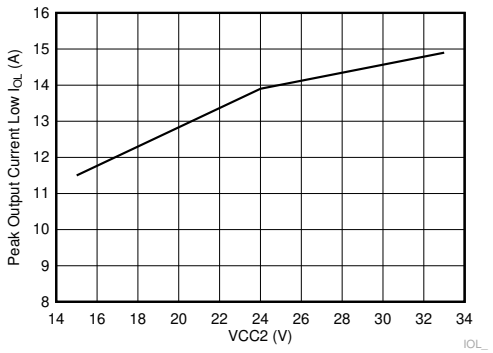
5.12 Typical Characteristics

V_{CC1} = 3.3 V or 5 V, 0.1-µF capacitor from V_{CC1} to GND1, V_{CC2}= 15 V, 1-µF capacitor from V_{CC2} to V_{EE2}, C_{LOAD} = 1 nF, T_J = –40°C to +125°C, (unless otherwise noted)



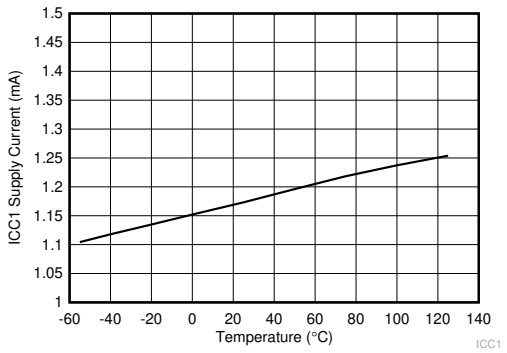
C_{LOAD} = 150 nF

Figure 5-4. Output-High Drive Current vs Output Voltage



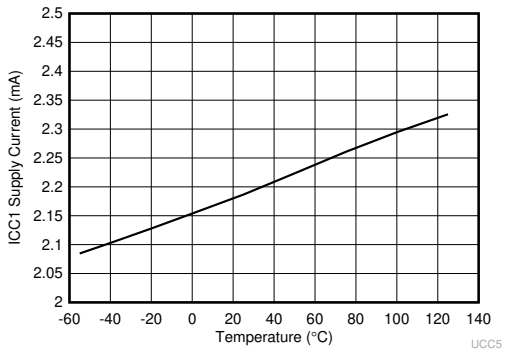
C_{LOAD} = 150 nF

Figure 5-5. Output-Low Drive Current vs Output Voltage



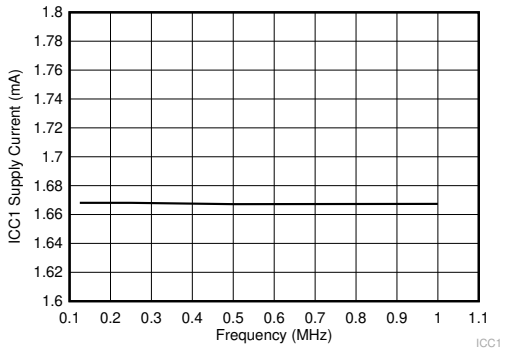
IN+ = L IN– = H

Figure 5-6. I_{CC1} Supply Current vs Temperature



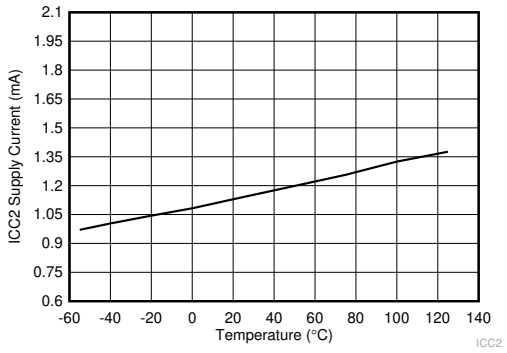
IN+ = H IN– = L

Figure 5-7. I_{CC1} Supply Current vs Temperature



Duty Cycle = 50% T = 25°C

Figure 5-8. I_{CC1} Supply Current vs Input Frequency

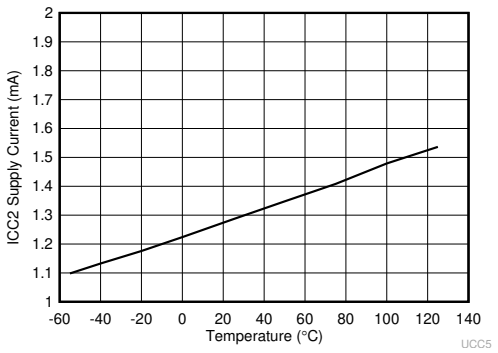


IN+ = L IN– = H

Figure 5-9. I_{CC2} Supply Current vs Temperature

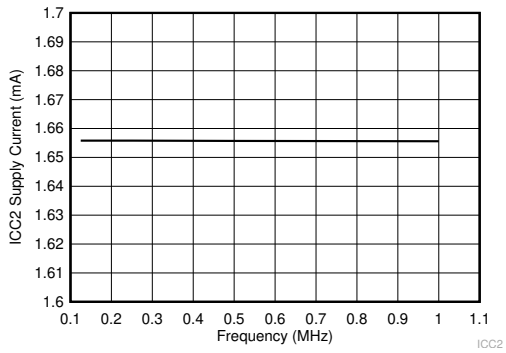
5.12 Typical Characteristics (continued)

V_{CC1} = 3.3 V or 5 V, 0.1-µF capacitor from V_{CC1} to GND1, V_{CC2}= 15 V, 1-µF capacitor from V_{CC2} to V_{EE2}, C_{LOAD} = 1 nF, T_J = –40°C to +125°C, (unless otherwise noted)



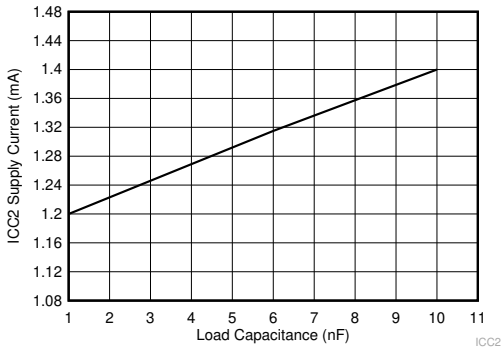
IN+ = H IN– = L

Figure 5-10. I_{CC2} Supply Current vs Temperature



Duty Cycle = 50% T = 25°C

Figure 5-11. I_{CC2} Supply Current vs Input Frequency



f_{SW} = 1 kHz

Figure 5-12. I_{CC2} Supply Current vs Load Capacitance

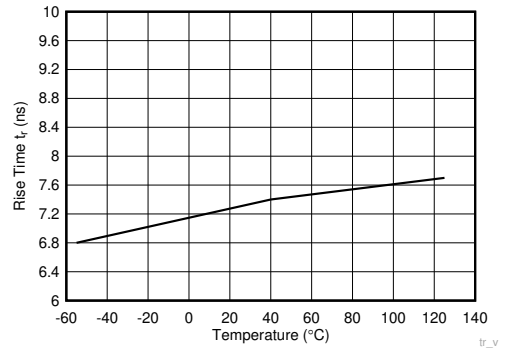


Figure 5-13. Rise Time vs Temperature

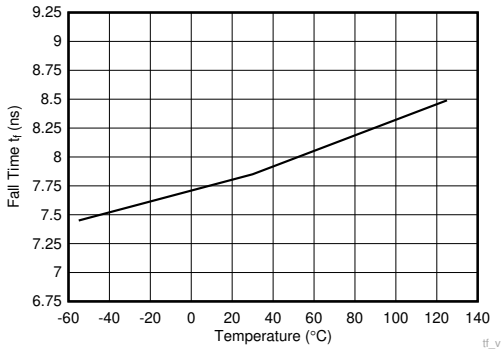


Figure 5-14. Fall Time vs Temperature

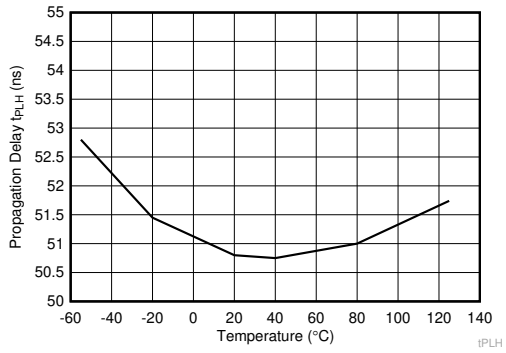


Figure 5-15. Propagation Delay t_{PLH} vs Temperature

5.12 Typical Characteristics (continued)

V_{CC1} = 3.3 V or 5 V, 0.1-µF capacitor from V_{CC1} to GND1, V_{CC2}= 15 V, 1-µF capacitor from V_{CC2} to V_{EE2}, C_{LOAD} = 1 nF, T_J = –40°C to +125°C, (unless otherwise noted)

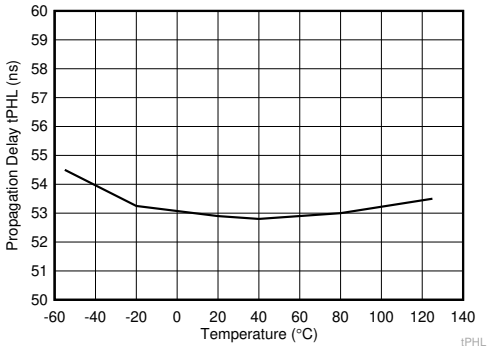
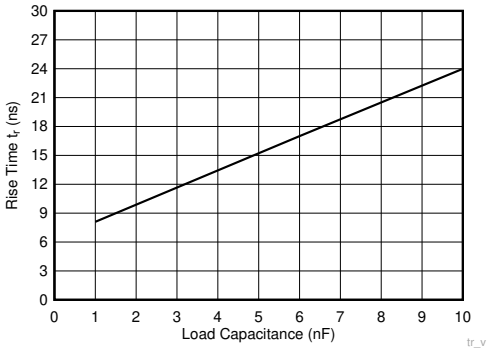
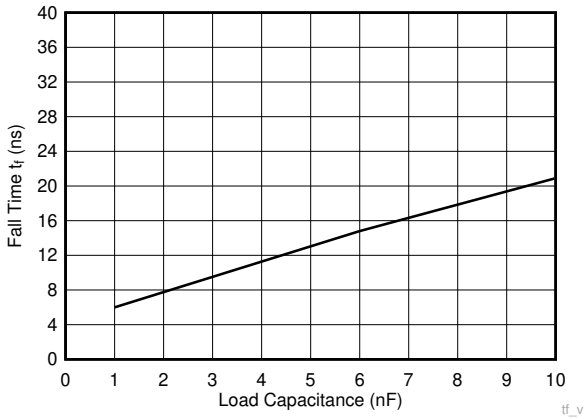


Figure 5-16. Propagation Delay t_{PHL} vs Temperature



f_{SW} = 1 kHz R_{GH} = 0 Ω R_{GL} = 0 Ω

Figure 5-17. Rise Time vs Load Capacitance



f_{SW} = 1 kHz R_{GH} = 0 Ω R_{GL} = 0 Ω

Figure 5-18. Fall Time vs Load Capacitance

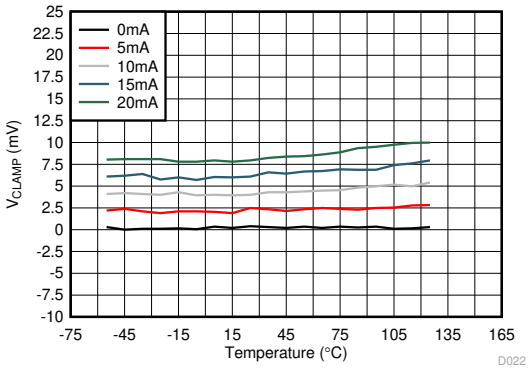


Figure 5-19. V_{CLAMP} vs Temperature

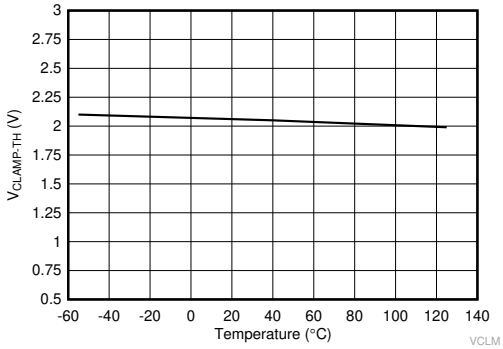


Figure 5-20. $V_{CLAMP-TH}$ vs Temperature

6 Parameter Measurement Information

6.1 Propagation Delay, Inverting, and Noninverting Configuration

Figure 6-1 shows the propagation delay for noninverting configurations. Figure 6-2 shows the propagation delay with the inverting configuration. These figures also demonstrate the method used to measure the rise (t_r) and fall (t_f) times.

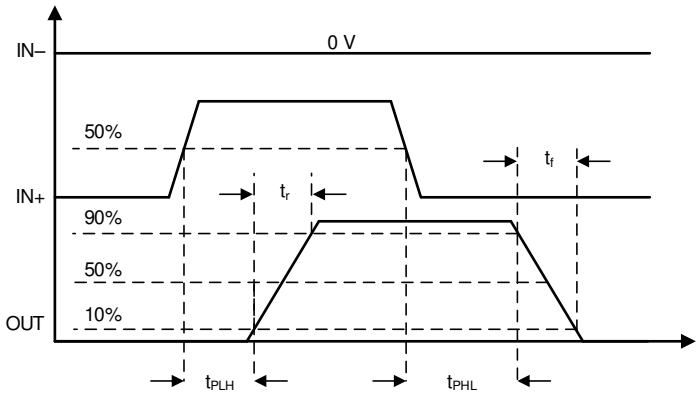


Figure 6-1. Propagation Delay, Noninverting Configuration

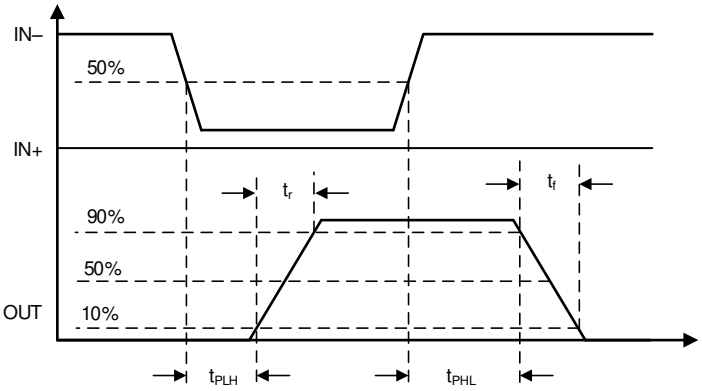


Figure 6-2. Propagation Delay, Inverting Configuration

6.1.1 CMTI Testing

Figure 6-3 is the simplified diagram of the CMTI testing configuration.

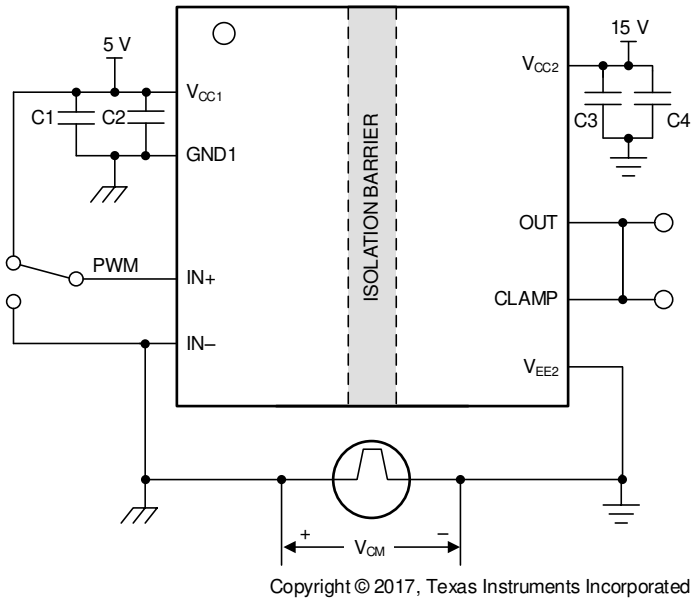


Figure 6-3. CMTI Test Circuit for Miller Clamp (UCC5350L-Q1)

7 Detailed Description

7.1 Overview

The isolation inside the UCC5350L-Q1 is implemented with high-voltage SiO_2-based capacitors. The signal across the isolation has an on-off keying (OOK) modulation scheme to transmit the digital data across a silicon dioxide based isolation barrier (see Figure 7-2). The transmitter sends a high-frequency carrier across the barrier to represent one digital state and sends no signal to represent the other digital state. The receiver demodulates the signal after advanced signal conditioning and produces the output through a buffer stage. The UCC5350L-Q1 incorporates advanced circuit techniques to maximize the CMTI performance and minimize the radiated emissions from the high frequency carrier and IO buffer switching. The conceptual block diagram of a digital capacitive isolator, Figure 7-1, shows a functional block diagram of a typical channel. Figure 7-2 shows a conceptual detail of how the OOK scheme works.

Figure 7-1 shows how the input signal passes through the capacitive isolation barrier through modulation (OOK) and signal conditioning.

7.2 Functional Block Diagram

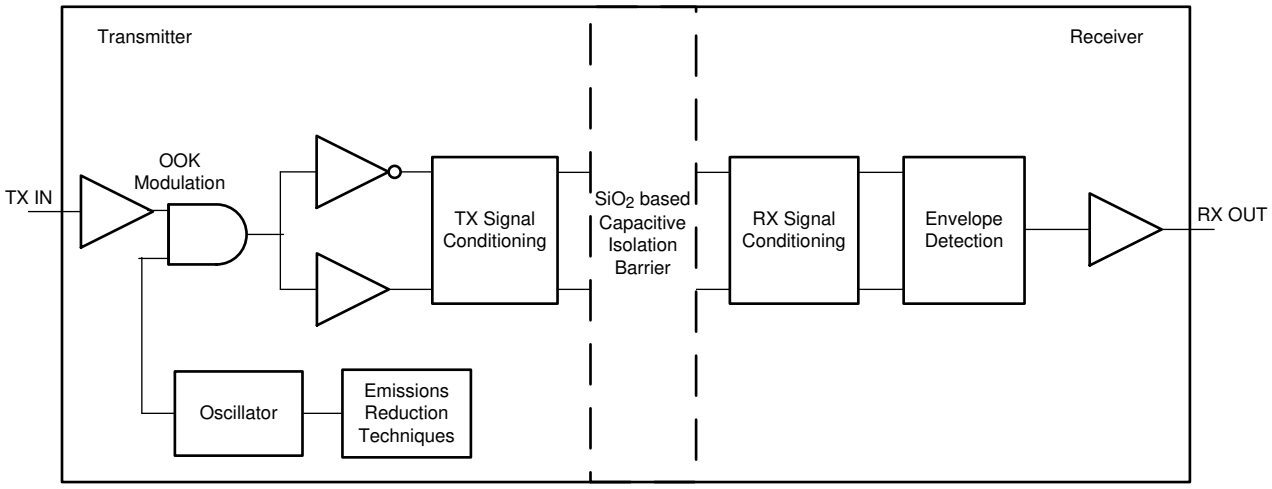


Figure 7-1. Conceptual Block Diagram of a Capacitive Data Channel

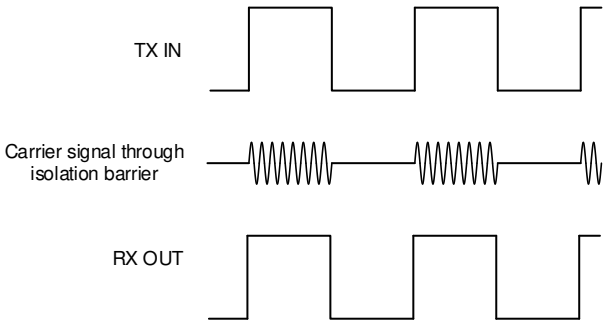


Figure 7-2. On-Off Keying (OOK) Based Modulation Scheme

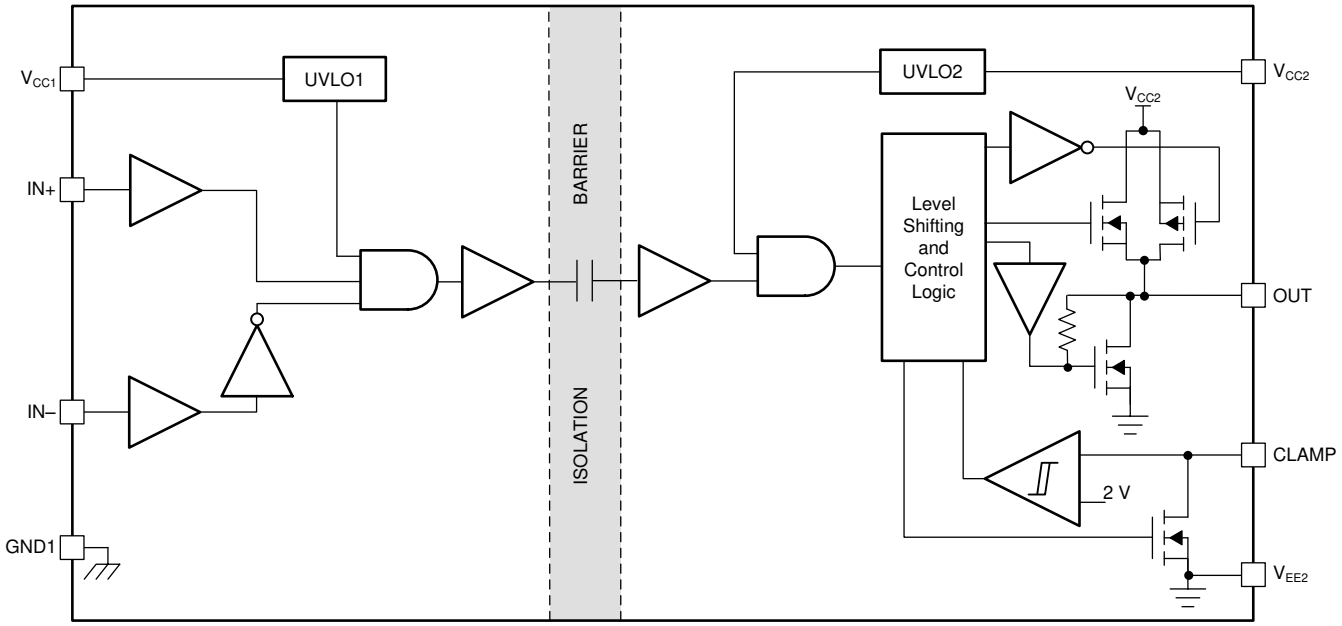


Figure 7-3. Functional Block Diagram

7.3 Feature Description

7.3.1 Power Supply

The V_{CC1} input power supply supports a wide voltage range from 3 V to 15 V and the V_{CC2} output supply supports a voltage range from 13.2 V to 30 V.

For operation with unipolar supply, the V_{CC2} supply is connected to 15 V with respect to VEE2 for IGBTs, and 20 V for SiC MOSFETs. The V_{EE2} supply is connected to 0 V. In this use case, the Miller clamp helps to prevent a false turn-on of the power switch without a negative voltage rail. The Miller clamping function is implemented by adding a low impedance path between the gate of the power device and the V_{EE2} supply. Miller current sinks through the clamp pin, which clamps the gate voltage to be lower than the turn-on threshold value for the gate.

7.3.2 Input Stage

The input pins (IN+ and IN–) are based on CMOS-compatible input-threshold logic that is completely isolated from the V_{CC2} supply voltage. The input pins are easy to drive with logic-level control signals (such as those from 3.3-V microcontrollers), because the UCC5350L-Q1 has a typical high threshold ($V_{IT+(IN)}$) of 0.55 × V_{CC1} and a typical low threshold of 0.45 × V_{CC1}. A wide hysteresis ($V_{hys(IN)}$) of 0.1 × V_{CC1} makes for good noise immunity and stable operation. If either of the inputs are left open, 128 kΩ of internal pull-down resistance forces the IN+ pin low and 128 kΩ of internal resistance pulls IN– high. However, TI still recommends grounding an input or tying to VCC1 if it is not being used for improved noise immunity.

Because the input side of the UCC5350L-Q1 is isolated from the output driver, the input signal amplitude can be larger or smaller than V_{CC2} provided that it does not exceed the recommended limit. This feature allows greater flexibility when integrating the gate-driver with control signal sources and allows the user to choose the most efficient V_{CC2} for any gate. However, the amplitude of any signal applied to IN+ or IN– must never be at a voltage higher than V_{CC1}.

7.3.3 Output Stage

The output stage of the UCC5350L-Q1 features a pull-up structure that delivers the highest peak-source current when it is most needed which is during the Miller plateau region of the power-switch turn-on transition (when the power-switch drain or collector voltage experiences dV/dt). The output stage pull-up structure features a P-channel MOSFET and an additional pull-up N-channel MOSFET in parallel. The function of the N-channel MOSFET is to provide a brief boost in the peak-sourcing current, which enables fast turn-on. Fast turn-on is accomplished by briefly turning on the N-channel MOSFET during a narrow instant when the output is changing

states from low to high. Table 7-1 lists the typical internal resistance values of the pull-up and pull-down structure.

Table 7-1. UCC5350L-Q1 On-Resistance

DEVICE OPTION	R_{NMOS}	R_{OH}	R_{OL}	R_{CLAMP}	UNIT
UCC5350L-Q1	1.54	12	0.26	0.26	Ω

The R_{OH} parameter is a DC measurement and is representative of the on-resistance of the P-channel device only. This parameter is only for the P-channel device, because the pull-up N-channel device is held in the OFF state in DC condition and is turned on only for a brief instant when the output is changing states from low to high. Therefore, the effective resistance of the UCC5350L-Q1 pull-up stage during this brief turn-on phase is much lower than what is represented by the R_{OH} parameter, which yields a faster turn-on. The turn-on-phase output resistance is the parallel combination R_{OH} || R_{NMOS}.

The pull-down structure in the UCC5350L-Q1 is simply composed of an N-channel MOSFET. For Miller Clamp, an additional FET is connected in parallel with the pull-down structure when the CLAMP and OUT pins are connected to the gate of the IGBT or MOSFET.The output is capable of delivering, or sinking, 5-A peak current pulses. The output voltage swing between V_{CC2} and V_{EE2} provides rail-to-rail operation.

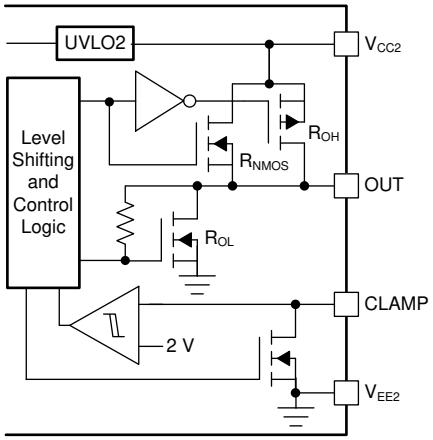


Figure 7-4. Output Stage

7.3.4 Protection Features

7.3.4.1 Undervoltage Lockout (UVLO)

UVLO functions are implemented for both the V_{CC1} and V_{CC2} supplies between the V_{CC1} and GND1, and V_{CC2} and V_{EE2} pins to prevent an underdriven condition on IGBTs and MOSFETs. When V_{CC} is lower than $V_{IT+\,(UVLO)}$ at device start-up or lower than $V_{IT-(UVLO)}$ after start-up, the voltage-supply UVLO feature holds the effected output low, regardless of the input pins (IN+ and IN–) as shown Table 7-2. The V_{CC} UVLO protection has a hysteresis feature ($V_{hys(UVLO)}$). This hysteresis prevents chatter when the power supply produces ground noise; this allows the device to permit small drops in bias voltage, which occurs when the device starts switching and operating current consumption increases suddenly. Figure 7-5 shows the UVLO functions.

Table 7-2. UCC5350L-Q1 V_{CC1} UVLO Logic

CONDITION	INPUTS		OUTPUT
	IN+	IN–	OUT
V_{CC1} – GND1 < $V_{IT+(UVLO1)}$ during device start-up	H	L	L
	L	H	L
	H	H	L
	L	L	L

Table 7-2. UCC5350L-Q1 V_{CC1} UVLO Logic (continued)

CONDITION	INPUTS		OUTPUT
	IN+	IN–	OUT
V_{CC1} – GND1 < $V_{IT–(UVLO1)}$ after device start-up	H	L	L
	L	H	L
	H	H	L
	L	L	L

Table 7-3. UCC5350L-Q1 V_{CC2} UVLO Logic

CONDITION	INPUTS		OUTPUT
	IN+	IN–	OUT
V_{CC2} – V_{EE2} < $V_{IT+(UVLO2)}$ during device start-up	H	L	L
	L	H	L
	H	H	L
	L	L	L
V_{CC2} – V_{EE2} < $V_{IT–(UVLO2)}$ after device start-up	H	L	L
	L	H	L
	H	H	L
	L	L	L

When V_{CC1} or V_{CC2} drops below the UVLO1 or UVLO2 threshold, a delay, t_{UVLO1_rec} or t_{UVLO2_rec}, occurs on the output when the supply voltage rises above $V_{IT+(UVLO)}$ or $V_{IT+(UVLO2)}$ again. Figure 7-5 shows this delay.

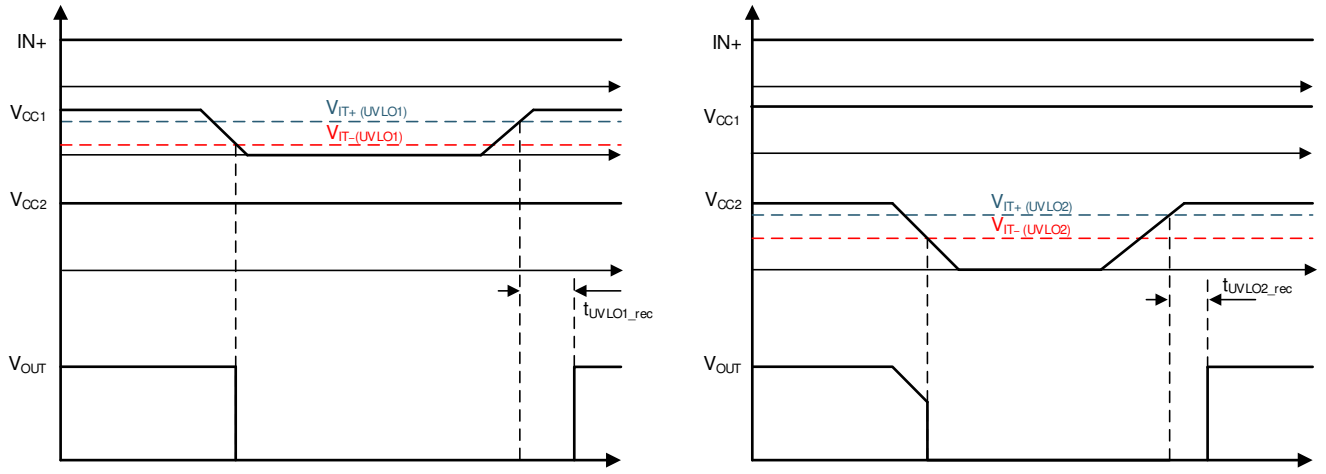


Figure 7-5. UVLO Functions

7.3.4.2 Active Pulldown

The active pull-down function is used to pull the IGBT or MOSFET gate to the low state when no power is connected to the V_{CC2} supply. This feature prevents false IGBT and MOSFET turn-on on the OUT and CLAMP pins by clamping the output to approximately 2 V.

When the output stages of the driver are in an unbiased or UVLO condition, the driver outputs are held low by an active clamp circuit that limits the voltage rise on the driver outputs. In this condition, the upper PMOS is resistively held off by a pull-up resistor while the lower NMOS gate is tied to the driver output through a 500-kΩ resistor. In this configuration, the output is effectively clamped to the threshold voltage of the lower NMOS device, which is approximately 1.5 V when no bias power is available.

7.3.4.3 Short-Circuit Clamping

The short-circuit clamping function is used to clamp voltages at the driver output and pull the active Miller clamp pins slightly higher than the V_{CC2} voltage during short-circuit conditions. The short-circuit clamping function helps protect the IGBT or MOSFET gate from overvoltage breakdown or degradation. The short-circuit clamping function is implemented by adding a diode connection between the dedicated pins and the V_{CC2} pin inside the driver. The internal diodes can conduct up to 500-mA current for a duration of 10 µs and a continuous current of 20 mA. Use external Schottky diodes to improve current conduction capability as needed.

7.3.4.4 Active Miller Clamp

The active Miller-clamp function helps to prevent a false turn-on of the power switches caused by Miller current in applications where a unipolar power supply is used. The active Miller-clamp function is implemented by adding a low impedance path between the power-switch gate terminal and ground (V_{EE2}) to sink the Miller current. With the Miller-clamp function, the power-switch gate voltage is clamped to less than 2 V during the off state. Figure 8-1 shows a typical application circuit of this function .

7.4 Device Functional Modes

Table 7-4 lists the functional modes for the UCC5350L-Q1 assuming V_{CC1} and V_{CC2} are in the recommended range.

Table 7-4. Function Table for UCC5350L-Q1

IN+	IN–	OUT
Low	X	Low
X	High	Low
High	Low	High

7.4.1 ESD Structure

Figure 7-6 shows the multiple diodes involved in the ESD protection components of the UCC5350L-Q1 device. This provides pictorial representation of the absolute maximum rating for the device.

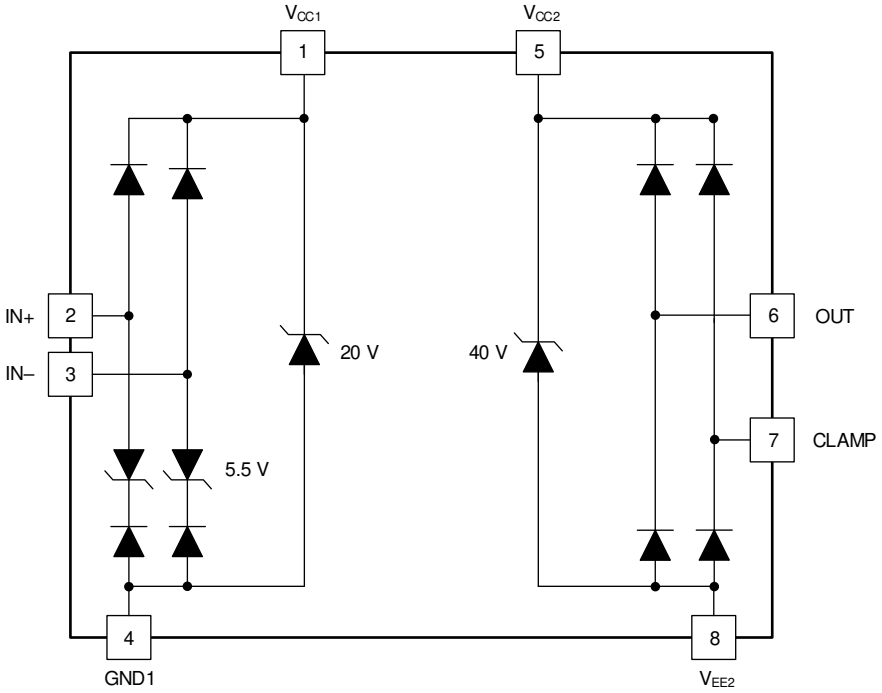


Figure 7-6. ESD Structure ' L' Version

8 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

8.1 Application Information

The UCC5350L-Q1 is a simple, isolated gate driver for power semiconductor devices, such as MOSFETs, IGBTs, or SiC MOSFETs. The family of devices is intended for use in applications such as motor control, solar inverters, switched-mode power supplies, and industrial inverters.

UCC5350L-Q1 features active Miller clamping, which can be used to prevent false turn-on of the power transistors induced by the Miller current. The device comes in an 8-pin DWL and has creepage of 15.7mm and clearance of 14.7mm , which is suitable for applications where basic or reinforced isolation is required. The UCC5350L-Q1 offers a 5-A minimum drive current.

8.2 Typical Application

The circuits in Figure 8-1 show a typical application for driving IGBTs.

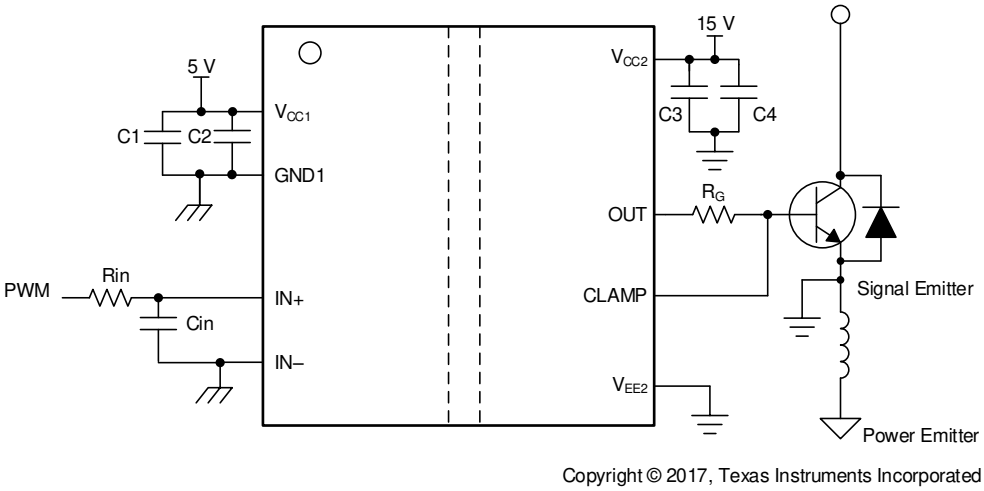


Figure 8-1. Typical Application Circuit for UCC5350L-Q1 to Drive IGBT

8.2.1 Design Requirements

Table 8-1. UCC5350L-Q1 Design Requirements

PARAMETER	VALUE	UNIT
V_{CC1}	3.3	V
$V_{CC2} – V_{EE2}$	18	V
IN+	3.3	V
IN–	GND1	-
Switching frequency	150	kHz
Gate Charge of Power Device	126	nC

8.2.2 Detailed Design Procedure

8.2.2.1 Designing IN+ and IN– Input Filter

TI recommends that users avoid shaping the signals to the gate driver in an attempt to slow down (or delay) the signal at the output. However, a small input filter, R_{IN}-C_{IN}, can be used to filter out the ringing introduced by nonideal layout or long PCB traces.

Such a filter should use an R_{IN} resistor with a value from 0 Ω to 100 Ω and a C_{IN} capacitor with a value from 10 pF to 1000 pF. In the example, the selected value for R_{IN} is 51 Ω and C_{IN} is 33 pF, with a corner frequency of approximately 100 MHz.

When selecting these components, pay attention to the trade-off between good noise immunity and propagation delay.

8.2.2.2 Gate-Driver Output Resistor

The external gate-driver resistors, $R_{G(ON)}$ and $R_{G(OFF)}$ are used to:

1. Limit ringing caused by parasitic inductances and capacitances
2. Limit ringing caused by high voltage or high current switching dv/dt, di/dt, and body-diode reverse recovery
3. Fine-tune gate drive strength, specifically peak sink and source current to optimize the switching loss
4. Reduce electromagnetic interference (EMI)

The output stage has a pull-up structure consisting of a P-channel MOSFET and an N-channel MOSFET in parallel. The combined typical peak source current is 10 A for UCC5350L-Q1. Use Equation 1 to estimate the peak source current. Recommend using at least 5Ω gate resistor for additional robustness for DWL package due to wide body adding additional inductance.

$$I_{OH} = \frac{V_{CC2} - V_{EE2}}{R_{NMOS}||R_{OH} + R_{GON} + R_{GFET\_Int}} \quad (1)$$

where

- R_{ON} is the external turn-on resistance, which is 2.2 Ω in this example.
- R_{GFET_Int} is the power transistor internal gate resistance, found in the power transistor data sheet. We will assume 1.8Ω for our example.
- I_{OH} is the typical peak source current which is the minimum value between 10 A, the gate-driver peak source current, and the calculated value based on the gate-drive loop resistance.

In this example, the peak source current is approximately 3.36 A as calculated in Equation 2.

$$I_{OH} = \frac{V_{CC2} - V_{EE2}}{R_{NMOS}||R_{OH} + R_{GON} + R_{GFET\_Int}} = \frac{18\,V}{1.54\Omega||12\Omega + 2.2\Omega + 1.8\Omega} \approx 3.36A \quad (2)$$

Similarly, use Equation 3 to calculate the peak sink current.

$$I_{OL} = \frac{V_{CC2} - V_{EE2}}{R_{OL} + R_{GOFF} + R_{GFET\_Int}} \quad (3)$$

where

- R_{OFF} is the external turn-off resistance, which is 2.2 Ω in this example.
- I_{OL} is the typical peak sink current which is the minimum value between 10 A, the gate-driver peak sink current, and the calculated value based on the gate-drive loop resistance.

In this example, the peak sink current is the minimum value between Equation 4 and 10 A.

$$I_{OL} = \frac{V_{CC2} - V_{EE2}}{R_{OL} + R_{GOFF} + R_{GFET\_Int}} = \frac{18\,V}{0.26\Omega + 2.2\Omega + 1.8\Omega} \approx 4.23A \quad (4)$$

Note

The estimated peak current is also influenced by PCB layout and load capacitance. Parasitic inductance in the gate-driver loop can slow down the peak gate-drive current and introduce overshoot and undershoot. Therefore, TI strongly recommends that the gate-driver loop should be minimized. Conversely, the peak source and sink current is dominated by loop parasitics when the load capacitance (C_{ISS}) of the power transistor is very small (typically less than 1 nF) because the rising and falling time is too small and close to the parasitic ringing period.

8.2.2.3 Estimate Gate-Driver Power Loss

The total loss, P_G, in the gate-driver subsystem includes the power losses (P_{GD}) of the UCC5350L-Q1 device and the power losses in the peripheral circuitry, such as the external gate-drive resistor.

The P_{GD} value is the key power loss which determines the thermal safety-related limits of the UCC5350L-Q1 device, and it can be estimated by calculating losses from several components.

The first component is the static power loss, P_{GDQ}, which includes quiescent power loss on the driver as well as driver self-power consumption when operating with a certain switching frequency. The P_{GDQ} parameter is measured on the bench with no load connected to the OUT pins at a given V_{CC1}, V_{CC2}, switching frequency, and ambient temperature. In this example, V_{CC1} is 3.3V and V_{CC2} is 18 V. The current on each power supply, with PWM switching from 0 V to 3.3 V at 150 kHz, is measured to be I_{CC1} = 1.67 mA and I_{CC2} = 1.11 mA. Therefore, use Equation 5 to calculate P_{GDQ}.

$$P_{GDQ} = V_{CC1} \times I_{VCC1} + (V_{CC2} - V_{EE2}) \times I_{CC2} \approx 23.31\text{mW} \tag{5}$$

The second component is the switching operation loss, P_{GDO}, with a given load capacitance which the driver charges and discharges the load during each switching cycle. Use Equation 6 to calculate the total dynamic loss from load switching, P_{GSW}.

$$P_{GSW} = (V_{CC2} - V_{EE2}) \times Q_G \times f_{SW} \tag{6}$$

where

- Q_G is the gate charge of the power transistor at V_{CC2}.

So, for this example application the total dynamic loss from load switching is approximately 340 mW as calculated in Equation 7.

$$P_{GSW} = 18\ \text{V} \times 126\ \text{nC} \times 150\ \text{kHz} = 340\ \text{mW} \tag{7}$$

Q_G represents the total gate charge of the power transistor and is subject to change with different testing conditions. The UCC5350L-Q1 gate-driver loss on the output stage, P_{GDO}, is part of P_{GSW}. P_{GDO} is equal to P_{GSW} if the external gate-driver resistance and power-transistor internal resistance are 0 Ω, and all the gate driver-loss will be dissipated inside the UCC5350L-Q1. If an external turn-on and turn-off resistance exists, the total loss is distributed between the gate driver pull-up/down resistance, external gate resistance, and power-transistor internal resistance. Importantly, the pull-up/down resistance is a linear and fixed resistance if the source/sink current is not saturated to 10 A, however, it will be non-linear if the source/sink current is saturated. The gate driver loss will be estimated in the case in which it is not saturated as given in Equation 8.

$$P_{GDO} = \frac{P_{GSW}}{2}\left(\frac{R_{OH}||R_{NMOS}}{R_{OH}||R_{NMOS} + R_{GON} + R_{GFET\_Int}} + \frac{R_{OL}}{R_{OL} + R_{GOFF} + R_{GFET\_Int}}\right) \tag{8}$$

In this design example, all the predicted source and sink currents are less than 10 A, therefore, use Equation 9 to estimate the gate-driver loss.

$$P_{GDO} = \frac{340\ mW}{2}\left(\frac{12\ \Omega \,||\, 1.54\ \Omega}{12\ \Omega \,||\, 1.54\ \Omega + 2.2\ \Omega + 1.8\ \Omega} + \frac{0.26\ \Omega}{0.26\ \Omega + 2.2\ \Omega + 1.8\ \Omega}\right) \approx 53.66\ mW \quad (9)$$

where

- $V_{OUTH/L(t)}$ is the gate-driver OUT pin voltage during the turnon and turnoff period. In cases where the output is saturated for some time, this value can be simplified as a constant-current source (10 A at turnon and turnoff) charging or discharging a load capacitor. Then, the $V_{OUTH/L(t)}$ waveform will be linear and the T_{R_Sys} and T_{F_Sys} can be easily predicted.

Use Equation 10 to calculate the total gate-driver loss dissipated in the UCC5350L-Q1 gate driver, P_{GD}.

$$P_{GD} = P_{GDQ} + P_{GDO} = 25.31 mW + 53.66 mW = 78.97 mW \quad (10)$$

8.2.2.4 Estimating Junction Temperature

Use the equation below to estimate the junction temperature (T_J) of the UCC5350L-Q1.

$$T_J = T_C + \Psi_{JT} \times P_{GD} \quad (11)$$

where

- T_C is the UCC5350L-Q1 case-top temperature measured with a thermocouple or some other instrument.
- Ψ_{JT} is the junction-to-top characterization parameter from the Thermal Information table.

Using the junction-to-top characterization parameter (Ψ_{JT}) instead of the junction-to-case thermal resistance ($R_{\theta JC}$) can greatly improve the accuracy of the junction temperature estimation. The majority of the thermal energy of most ICs is released into the PCB through the package leads, whereas only a small percentage of the total energy is released through the top of the case (where thermocouple measurements are usually conducted). The $R_{\theta JC}$ resistance can only be used effectively when most of the thermal energy is released through the case, such as with metal packages or when a heat sink is applied to an IC package. In all other cases, use of $R_{\theta JC}$ will inaccurately estimate the true junction temperature. The Ψ_{JT} parameter is experimentally derived by assuming that the dominant energy leaving through the top of the IC will be similar in both the testing environment and the application environment. As long as the recommended layout guidelines are observed, junction temperature estimations can be made accurately to within a few degrees Celsius.

8.2.2.5 Selecting V_{CC1} and V_{CC2} Capacitors

Bypass capacitors for the V_{CC1} and V_{CC2} supplies are essential for achieving reliable performance. TI recommends choosing low-ESR and low-ESL, surface-mount, multi-layer ceramic capacitors (MLCC) with sufficient voltage ratings, temperature coefficients, and capacitance tolerances.

Note

DC bias on some MLCCs will impact the actual capacitance value. For example, a 25-V, 1-µF X7R capacitor is measured to be only 500 nF when a DC bias of 15-V_{DC} is applied.

8.2.2.5.1 Selecting a V_{CC1} Capacitor

A bypass capacitor connected to the V_{CC1} pin supports the transient current required for the primary logic and the total current consumption, which is only a few milliamperes. Therefore, a 50-V MLCC with over 100 nF is recommended for this application. If the bias power-supply output is located a relatively long distance from the V_{CC1} pin, a tantalum or electrolytic capacitor with a value greater than 1 µF should be placed in parallel with the MLCC.

8.2.2.5.2 Selecting a V_{CC2} Capacitor

A 50-V, 10-µF MLCC and a 50-V, 0.22-µF MLCC are selected for the C_{VCC2} capacitor. If the bias power supply output is located a relatively long distance from the V_{CC2} pin, a tantalum or electrolytic capacitor with a value greater than 10 µF should be used in parallel with C_{VCC2}.

8.2.2.5.3 Application Circuits with Output Stage Negative Bias

When parasitic inductances are introduced by nonideal PCB layout and long package leads (such as TO-220 and TO-247 type packages), ringing in the gate-source drive voltage of the power transistor could occur during high di/dt and dv/dt switching. If the ringing is over the threshold voltage, unintended turn-on and shoot-through could occur. Applying a negative bias on the gate drive is a popular way to keep such ringing below the threshold. A few examples of implementing negative gate-drive bias follow.

Figure 8-2 shows another example which uses two supplies (or single-input, double-output power supply). The power supply across V_{CC2} and the emitter determines the positive drive output voltage and the power supply across V_{EE2} and the emitter determines the negative turn-off voltage. This solution requires more power supplies than the first example, however, it provides more flexibility when setting the positive and negative rail voltages.

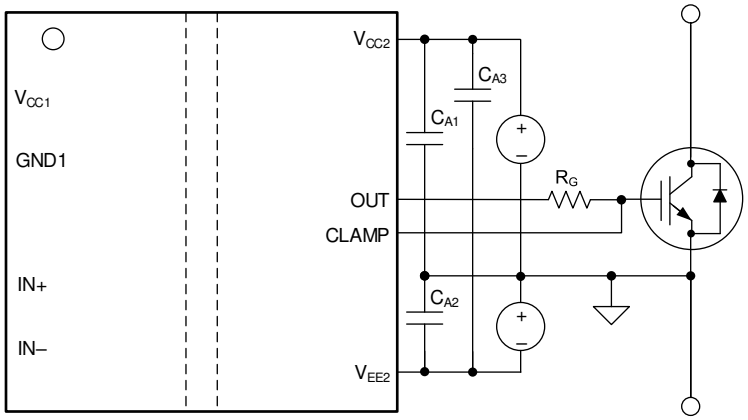
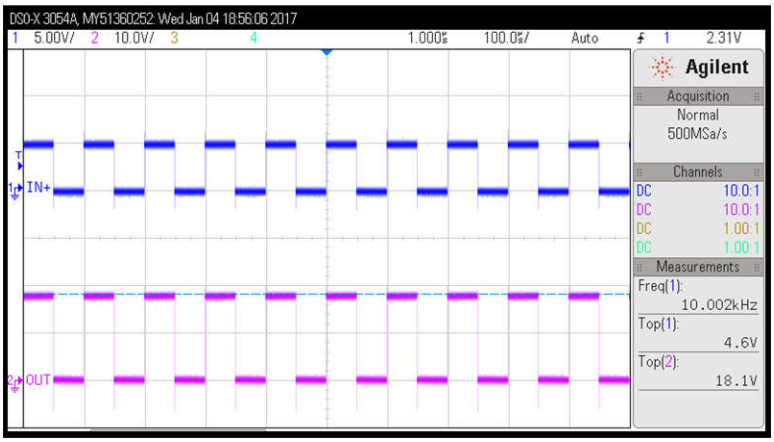


Figure 8-2. Negative Bias With Two Iso-Bias Power Supplies

8.2.3 Application Curve



V_{CC2} = 20 V V_{EE2} = GND f_{SW} = 10 kHz

Figure 8-3. PWM Input and Gate Voltage Waveform

9 Power Supply Recommendations

During the turn on and turn off switching transient, the peak source and sink current is provided by the VCC2 and VEE2 power supply. The large peak current is possible to drain the VCC2 and VEE2 voltage level and cause a voltage droop on the power supplies. To stabilize the power supply and ensure a reliable operation, a set of decoupling capacitors are recommended at the power supplies. Considering the device has ±10-A peak drive strength and can generate high dV/dt, a 10-µF bypass cap is recommended between VCC2 and VEE2. A 1-µF bypass cap is recommended between VCC1 and GND1 due to less current comparing with output side power supplies. A 0.1-µF decoupling cap is also recommended for each power supply to filter out high frequency noise. The decoupling capacitors must be low ESR and ESL to avoid high frequency noise, and should be placed as close as possible to the VCC1, VCC2 and VEE2 pins to prevent noise coupling from the system parasitics of PCB layout.

10 Layout

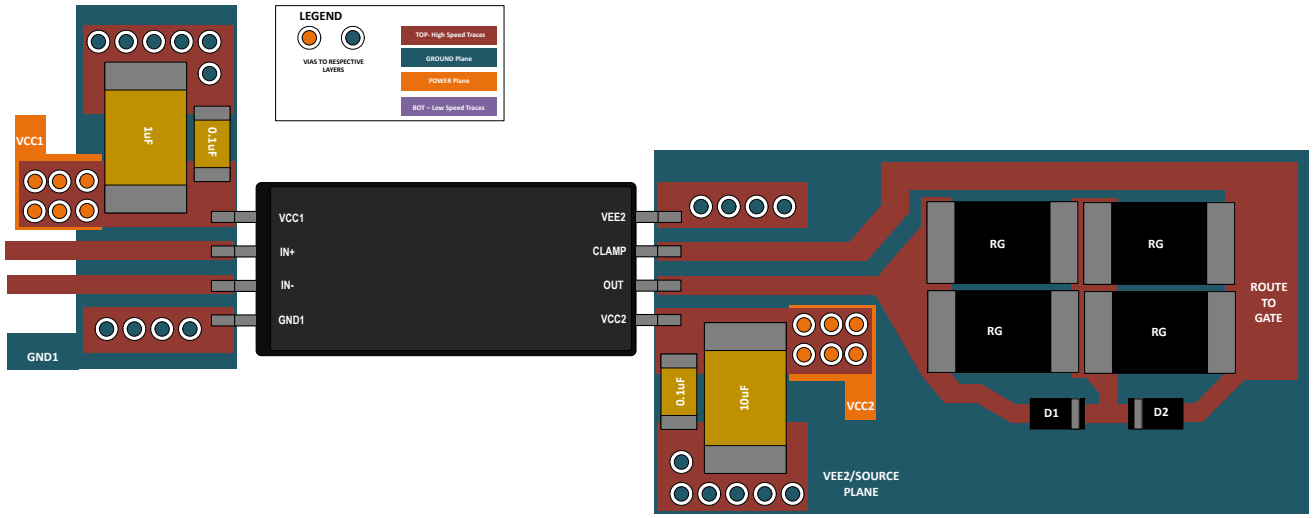
10.1 Layout Guidelines

Designers must pay close attention to PCB layout to achieve optimum performance since this device has an extra-wide body. Some key guidelines are:

- Component placement:
  - Low-ESR and low-ESL capacitors must be connected close to the device between the V_{CC1} and GND1 pins and between the V_{CC2} and V_{EE2} pins to bypass noise and to support high peak currents when turning on the external power transistor.
  - To avoid large negative transients on the V_{EE2} pins connected to the switch node, the parasitic inductances between the source of the top transistor and the source of the bottom transistor must be minimized.
  - Highly recommended to use this part with gate resistor at least 5Ω to ensure additional robustness.
  - Recommended Layout is shown in the Layout Example in the next section, which is critical to ensure robust performance.
- Grounding considerations:
  - Limiting the high peak currents that charge and discharge the transistor gates to a minimal physical area is essential. This limitation decreases the loop inductance and minimizes noise on the gate terminals of the transistors. The gate driver must be placed as close as possible to the transistors.
- High-voltage considerations:
  - To ensure isolation performance between the primary and secondary side, avoid placing any PCB traces or copper below the driver device. A PCB cutout or groove is recommended in order to prevent contamination that may compromise the isolation performance.
- Thermal considerations:
  - A large amount of power may be dissipated by the UCC5350L-Q1 if the driving voltage is high, the load is heavy, or the switching frequency is high. Proper PCB layout can help dissipate heat from the device to the PCB and minimize junction-to-board thermal impedance (θ_{JB}).
  - Increasing the PCB copper connecting to the V_{CC2} and V_{EE2} pins is recommended, with priority on maximizing the connection to V_{EE2}. However, the previously mentioned high-voltage PCB considerations must be maintained.
  - If the system has multiple layers, TI also recommends connecting the V_{CC2} and V_{EE2} pins to internal ground or power planes through multiple vias of adequate size. These vias should be located close to the IC pins to maximize thermal conductivity. However, keep in mind that no traces or coppers from different high voltage planes are overlapping.

10.2 Layout Example

The following diagram shows shows a PCB layout example with the signals and key components labeled.



A. No PCB traces or copper are located between the primary and secondary side, which ensures isolation performance.

Figure 10-1. Layout Example

10.3 PCB Material

Use standard FR-4 UL94V-0 printed circuit board. This PCB is preferred over cheaper alternatives because of lower dielectric losses at high frequencies, less moisture absorption, greater strength and stiffness, and the self-extinguishing flammability-characteristics.

Figure 10-2 shows the recommended layer stack.

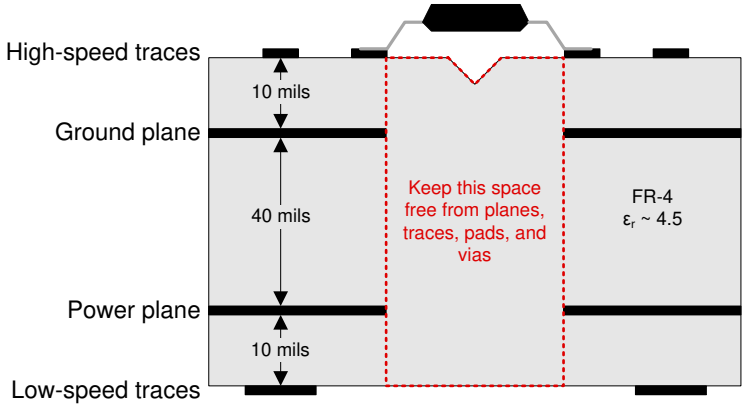


Figure 10-2. Recommended Layer Stack

11 Device and Documentation Support

11.1 Device Support

11.1.1 Third-Party Products Disclaimer

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11.2 Documentation Support

11.2.1 Related Documentation

For related documentation see the following:

- Texas Instruments, *Digital Isolator Design Guide*
- Texas Instruments, *Isolation Glossary*
- Texas Instruments, *SN6501 Transformer Driver for Isolated Power Supplies* data sheet
- Texas Instruments, *SN6505A Low-Noise 1-A Transformer Drivers for Isolated Power Supplies* data sheet
- Texas Instruments, *UCC5390ECDWV Isolated Gate Driver Evaluation Module* user's guide
- Texas Instruments, *UCC53x0xD Evaluation Module* user's guide

11.3 Certifications

UL Online Certifications Directory, *"FPPT2.E181974 Nonoptical Isolating Devices - Component"* Certificate Number: 20170718-E181974,

11.4 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

11.5 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

11.6 Trademarks

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11.7 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

11.8 Glossary

TI Glossary	This glossary lists and explains terms, acronyms, and definitions.

12 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

DATE	REVISION	NOTES
March 2025	*	Initial Release

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
UCC5350MCQDWLRQ1	Active	Production	SOIC (DWL) | 8	500 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 125	53MCQ
UCC5350MCQDWLRQ1.A	Active	Production	SOIC (DWL) | 8	500 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 125	53MCQ
UCC5350MCQDWLRQ1.B	Active	Production	SOIC (DWL) | 8	500 | LARGE T&R	-	Call TI	Call TI	-40 to 125	

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

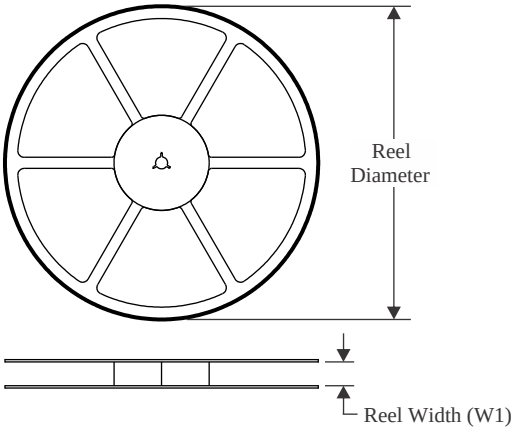
(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

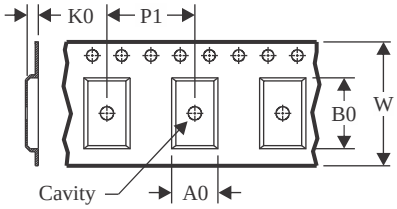
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

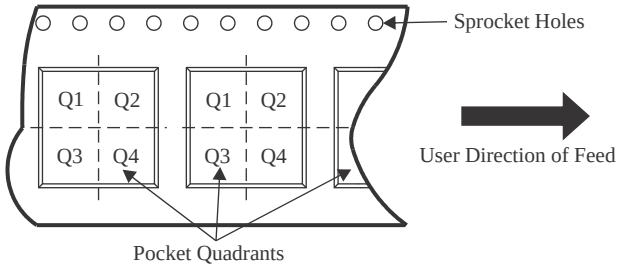


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

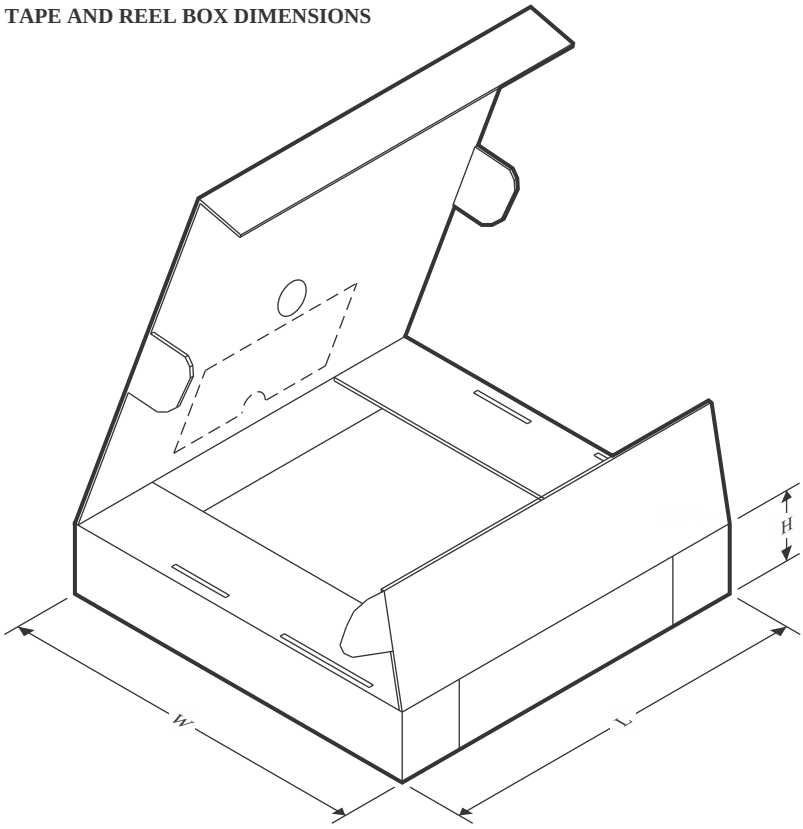
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
UCC5350MCQDWLRQ1	SOIC	DWL	8	500	330.0	24.4	18.55	7.2	4.5	24.0	24.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

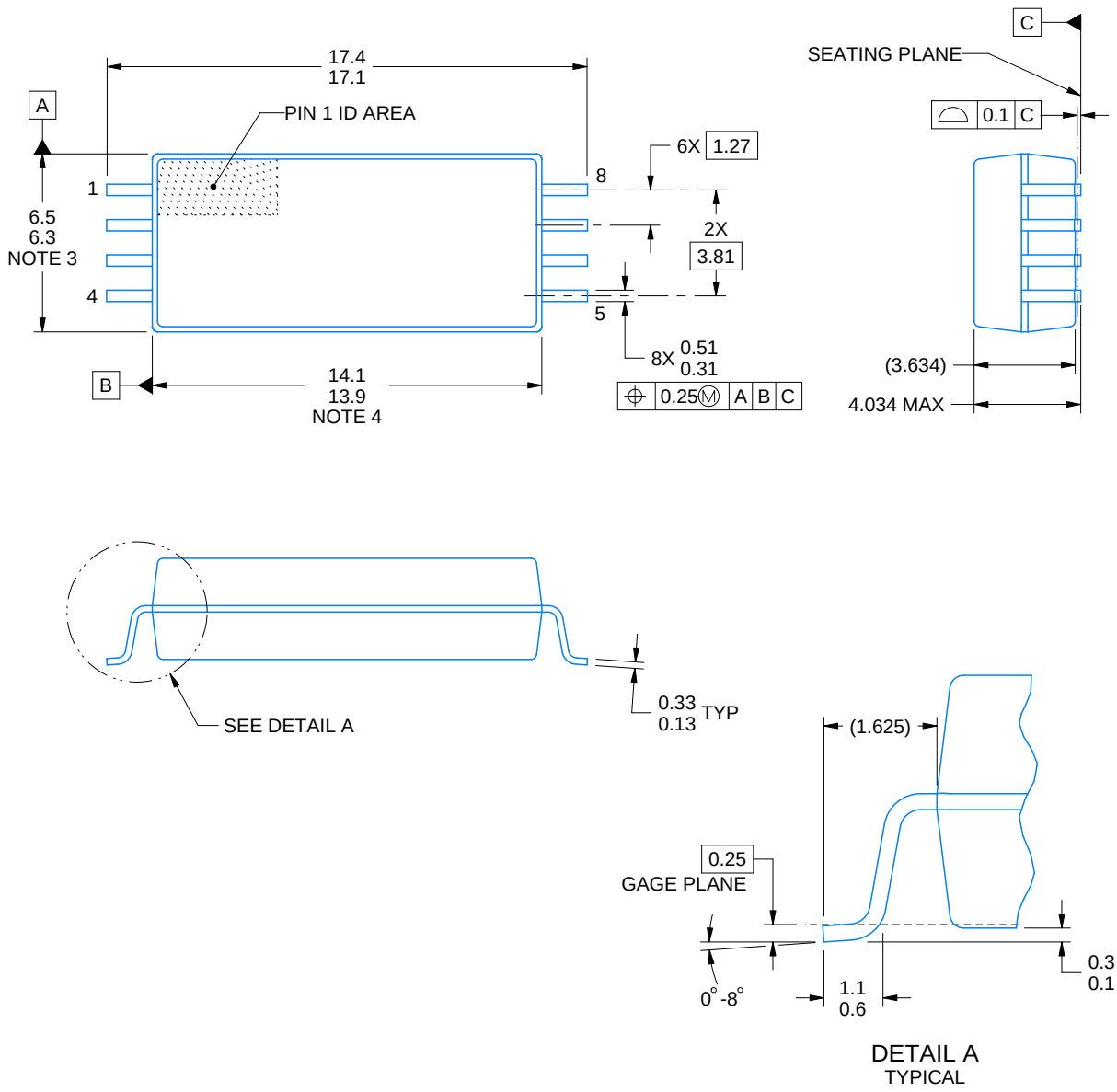
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
UCC5350MCQDWLRQ1	SOIC	DWL	8	500	356.0	356.0	45.0

PACKAGE OUTLINE

DWL0008A

SOIC - 4.034 mm max height

PLASTIC SMALL OUTLINE



4224743/A 01/2019

NOTES:

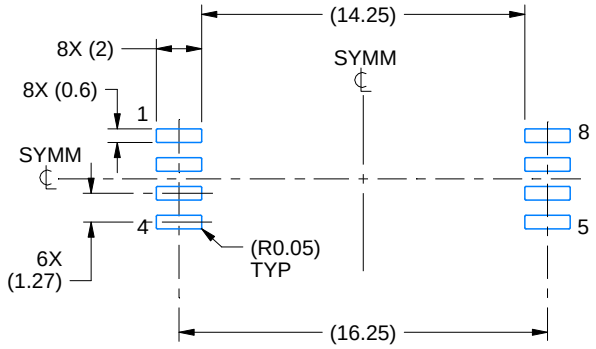
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0,15 mm per side.
4. This dimension does not include interlead flash.

EXAMPLE BOARD LAYOUT

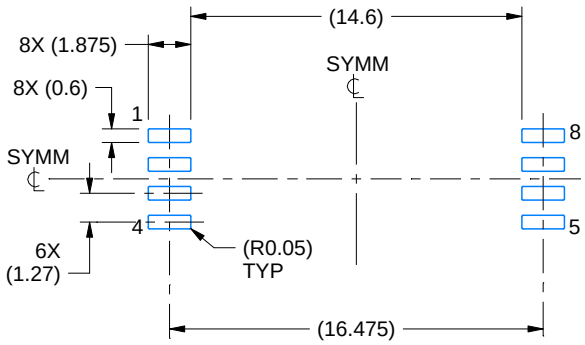
DWL0008A

SOIC - 4.034 mm max height

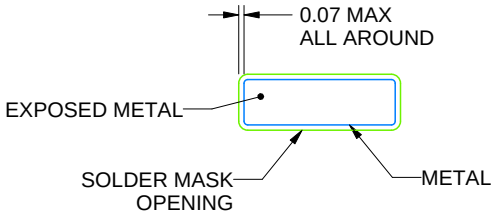
PLASTIC SMALL OUTLINE



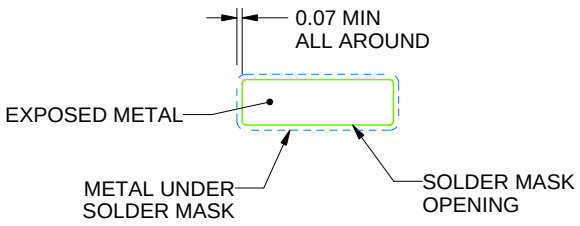
LAND PATTERN EXAMPLE
STANDARD
EXPOSED METAL SHOWN
SCALE:3X



LAND PATTERN EXAMPLE
PCB CLEARANCE & CREEPAGE OPTIMIZED
EXPOSED METAL SHOWN
SCALE:3X



NON SOLDER MASK
DEFINED
(PREFERRED)



SOLDER MASK
DEFINED

SOLDER MASK DETAILS

4224743/A 01/2019

NOTES: (continued)

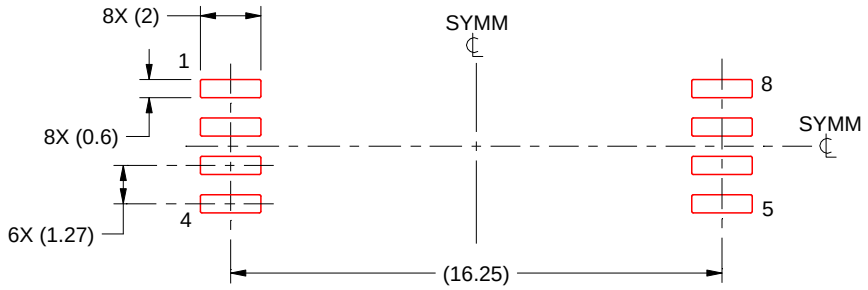
5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

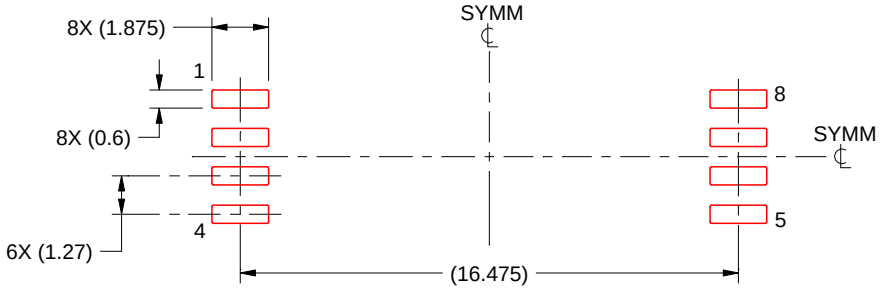
DWL0008A

SOIC - 4.034 mm max height

PLASTIC SMALL OUTLINE



SOLDER PASTE EXAMPLE
STANDARD
BASED ON 0.125 mm THICK STENCIL
SCALE:4X



SOLDER PASTE EXAMPLE
PCB CLEARANCE & CREEPAGE OPTIMIZED
BASED ON 0.125 mm THICK STENCIL
SCALE:4X

4224743/A 01/2019

NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

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