# UCC5881-Q1 Isolated 20A Adjustable Gate Drive IGBT/SiC MOSFET Gate Driver With Advanced Protection Features For Automotive Applications

## 1 Features

- Dual-output driver with real time variable drive strength
  - ±15A and ±5A drive current outputs
  - Digital input pins (GD*) for drive strength adjustment without SPI
  - 3 resistor settings R1, R2, or R1||R2
  - Integrated 4A active Miller clamp or optional external drive for Miller clamp transistor
- Primary-side and secondary-side active short circuit (ASC) support
- Under-voltage and over-voltage protection on internal and external supplies
- Driver die temperature sensing and over temperature protection
- Short-circuit protection:
  - 110ns response time to DESAT event
  - DESAT protection – selections up to 14V
  - Shunt resistor based short-circuit (SC) and over-current (OC) protection
  - Configurable protection threshold values and blanking times
  - Programmable soft turn-off (STO) and two-level soft turn-off (2STO) current
- Integrated 10-bit ADC
  - Able to measure power switch temperature, DC Link voltage, driver die temperature, DESAT pin voltage, VCC2 voltage
  - Programmable digital comparators
- Advanced VCE/VDS clamping circuit
- Functional Safety-Compliant
  - Developed for functional safety applications
  - Documentation available to aid ISO 26262 system design up to ASIL D
- Integrated diagnostics:
  - Built in self-test (BIST) for protection comparators
  - Gate threshold voltage measurement for power device health monitoring
  - INP to transistor gate path integrity
  - Internal clock monitoring
  - Fault alarm and warning outputs (nFLT*)
  - ISO communication data integrity check
- SPI based device reconfiguration, verification, supervision, and diagnosis
- 150V/ns CMTI
- AEC-Q100 qualified with the following results:
  - Device temperature grade 1: -40°C to +125°C ambient operating temperature

- Device HBM ESD classification level 2
- Device CDM ESD classification level C2b

## 2 Applications

- EV and HEV traction inverter
- EV and HEV power modules

## 3 Description

The UCC5881-Q1 device is an isolated, highly configurable adjustable drive strength gate driver targeted to drive high power SiC MOSFETs and IGBTs in EV/HEV applications. Power transistor protections are included, such as shunt resistor based over-current, over-temperature (PTC, NTC, or diode), and DESAT detection, with selectable soft turn-off or two-level soft turn-off during these faults. An integrated 10-bit ADC enables monitoring of up to 2 analog inputs, VCC2, DESAT, and the gate driver temperature for enhanced system management. Diagnostics and detection functions are integrated to simplify the design of ASIL compliant systems. The parameters and thresholds for these features are configurable using the SPI, which allows the device to be used with nearly any SiC MOSFET or IGBT.

**Device Information**

| PART NUMBER | PACKAGE[1] | PACKAGE SIZE[2] | BODY SIZE (NOM) |
|---|---|---|---|
| UCC5881-Q1 | DFC (SSOP, 32) | 10.3mm × 10.3mm | 10.5mm x 7.5mm |

(1) For all available packages, see the orderable addendum at the end of the data sheet.

(2) The package size (length × width) is a nominal value and includes pins, where applicable.
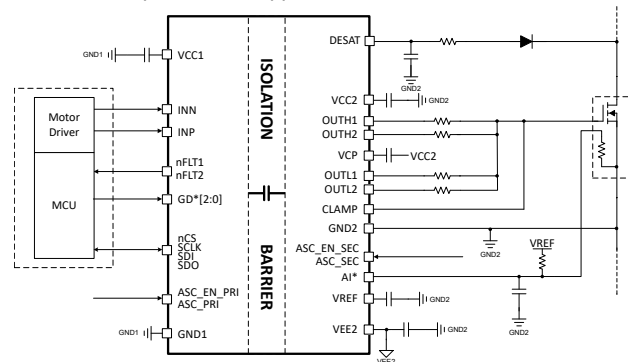


**Simplified Schematic**

# 4 Device and Documentation Support

## 4.1 Device Support

### 4.1.1 Third-Party Products Disclaimer

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## 4.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

## 4.3 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

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## 4.4 Trademarks

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## 4.5 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

## 4.6 Glossary

TI Glossary     This glossary lists and explains terms, acronyms, and definitions.

# 5 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

| DATE | REVISION | NOTES |
|---|---|---|
| December 2024 | * | Initial Release |

# 6 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

## PACKAGING INFORMATION

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead finish/ Ball material (6) | MSL Peak Temp (3) | Op Temp (°C) | Device Marking (4/5) | Samples |
|---|---|---|---|---|---|---|---|---|---|---|---|
| UCC5881QDFCRQ1 | ACTIVE | SSOP | DFC | 32 | 2000 | RoHS & Green | NIPDAU | Level-3-260C-168 HR | -40 to 125 | UCC5881Q | Samples |

**(1)** The marketing status values are defined as follows:
**ACTIVE:** Product device recommended for new designs.
**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.
**OBSOLETE:** TI has discontinued the production of the device.

**(2)** **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

**(3)** MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

**(4)** There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

**(5)** Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

**(6)** Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

**Important Information and Disclaimer:** The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

## TAPE AND REEL INFORMATION

**REEL DIMENSIONS**

**TAPE DIMENSIONS**



| A0 | Dimension designed to accommodate the component width |
|----|---|
| B0 | Dimension designed to accommodate the component length |
| K0 | Dimension designed to accommodate the component thickness |
| W | Overall width of the carrier tape |
| P1 | Pitch between successive cavity centers |

**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**



*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| UCC5881QDFCRQ1 | SSOP | DFC | 32 | 2000 | 330.0 | 16.4 | 10.75 | 10.7 | 2.7 | 12.0 | 16.0 | Q1 |

**TAPE AND REEL BOX DIMENSIONS**



*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|---|---|---|---|---|---|---|---|
| UCC5881QDFCRQ1 | SSOP | DFC | 32 | 2000 | 350.0 | 350.0 | 43.0 |

10.63 / 9.97 TYP

A

PIN 1 ID AREA

1

10.5 / 10.1 NOTE 3

16

32

30X 0.6

2X 9

17

32X 0.35 / 0.15

⊕ 0.25 Ⓜ C A B

B

7.6 / 7.4 NOTE 4

C

SEATING PLANE

⌂ 0.1 C

2.65 MAX

SEE DETAIL A

0.33 / 0.10 TYP

0.25

GAGE PLANE

0° - 8°

1.27 / 0.40

(1.4)

0.3 / 0.1

**DETAIL A**
TYPICAL

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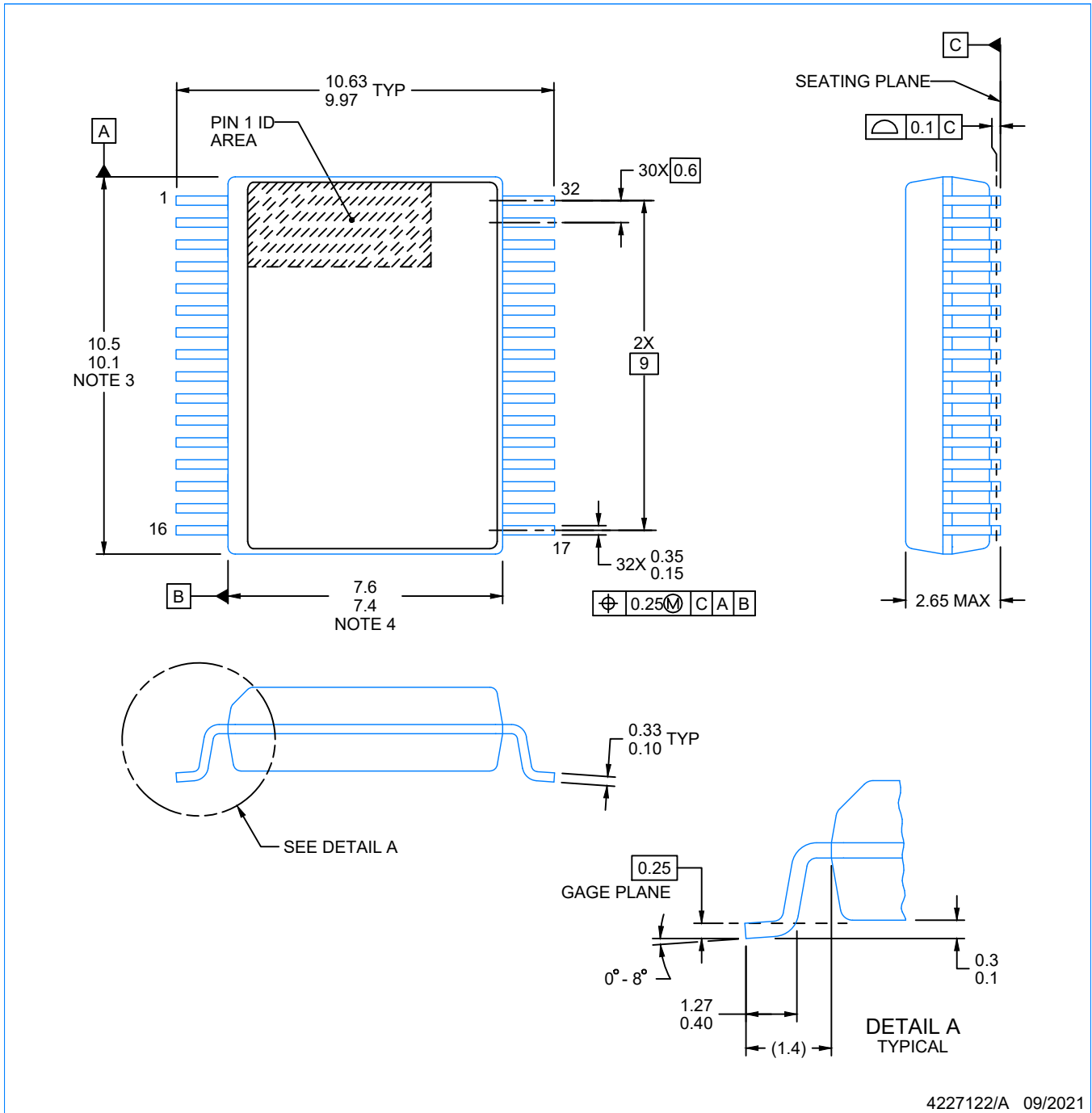
NOTES:

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm, per side.
5. Reference JEDEC registration MS-013.

16X (2)

SYMM

SEE DETAILS

1

32X (0.41)

SYMM

30X (0.6)

32

16

17

R0.05 TYP

(9.3)

IPC-7351 NOMINAL
7.3 mm CLEARANCE/CREEPAGE

16X (1.65)

SYMM

SEE DETAILS

1

32X (0.41)

SYMM

30X (0.6)

32

16

17

R0.05 TYP

(9.75)

HV / ISOLATION OPTION
8.1 mm CLEARANCE/CREEPAGE
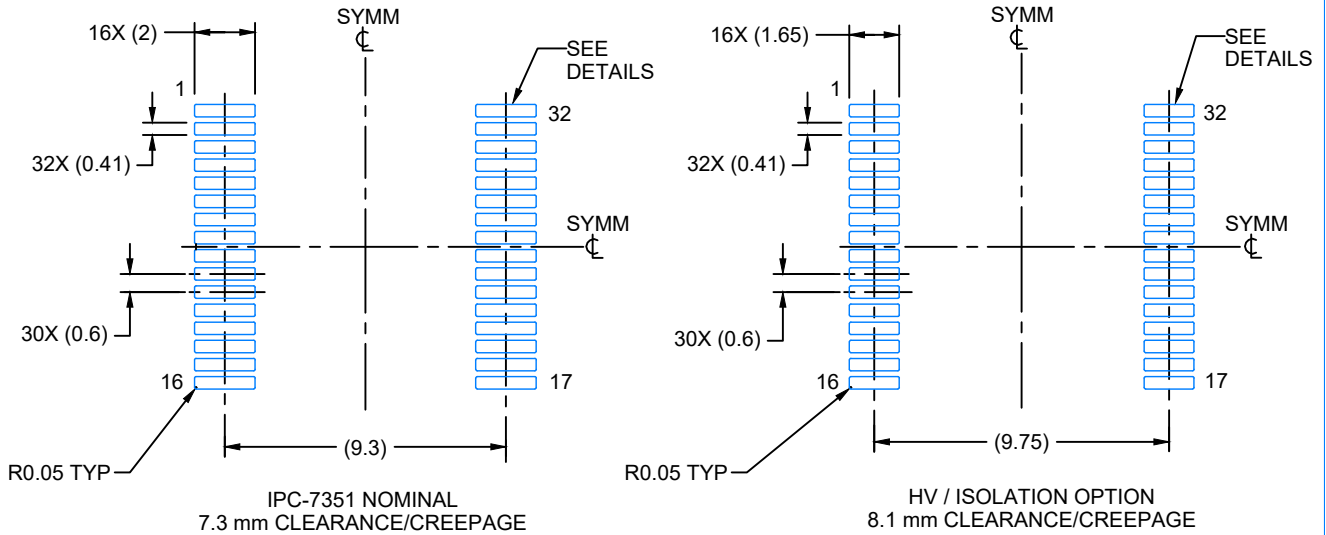
LAND PATTERN EXAMPLE
SCALE:4X

METAL

SOLDER MASK OPENING

0.07 MAX
ALL AROUND

NON SOLDER MASK
DEFINED

SOLDER MASK OPENING

METAL UNDER SOLDER MASK

0.07 MIN
ALL AROUND

SOLDER MASK
DEFINED
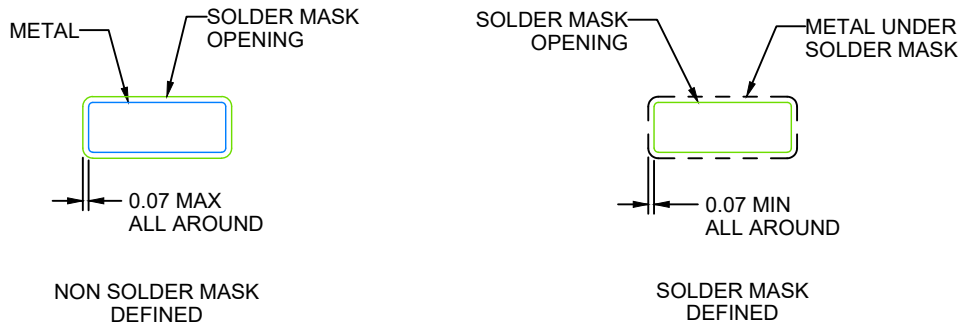
SOLDER MASK DETAILS

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NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

IPC-7351 NOMINAL
7.3 mm CLEARANCE/CREEPAGE

HV / ISOLATION OPTION
8.1 mm CLEARANCE/CREEPAGE
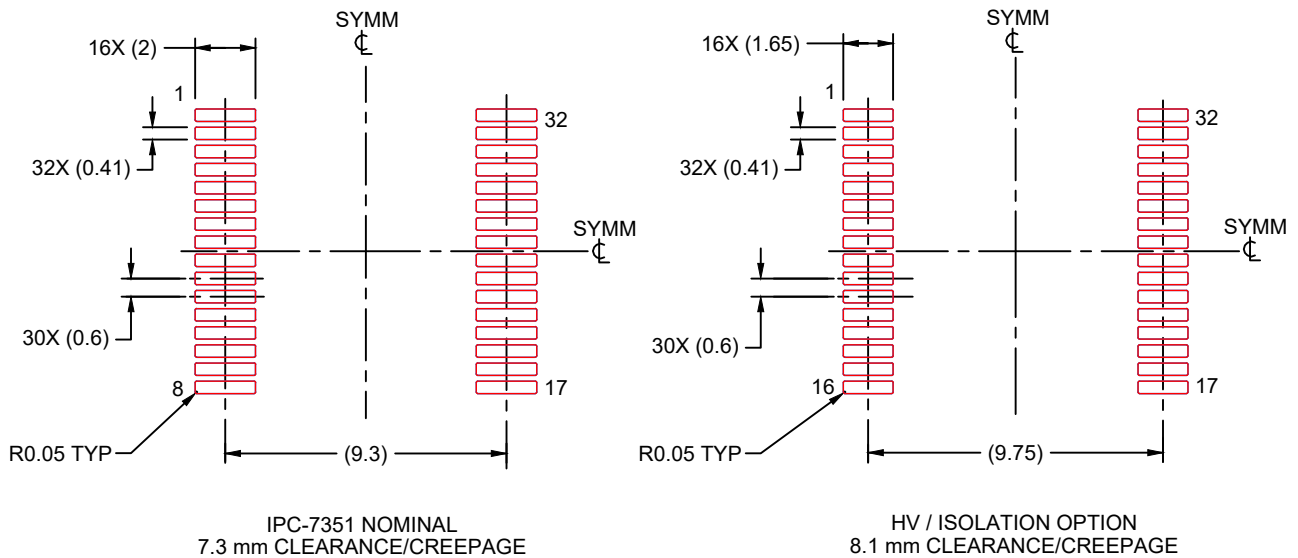
SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:4X

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NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.