User's Guide

SLAU264A–October 2008–Revised September 2012

TLV320AIC3254EVM-K

This user's guide describes the characteristics, operation, and use of the TLV320AIC3254EVM-K. This evaluation module (EVM) features a complete stereo audio codec with several inputs and outputs, extensive audio routing, mixing, and effects capabilities. A complete circuit description, schematic diagram, and bill of materials are also included.

The following related documents are available through the Texas Instruments Web site at www.ti.com.

EVM-Compatible Device Data Sheets

Device	Literature Number
TLV320AIC3254	SLAS549
TAS1020B	SLES025
REG1117-3.3	SBVS001
TPS767D318	SLVS209
SN74LVC125A	SCAS290
SN74LVC1G125	SCES223
SN74LVC1G07	SCES296

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1 EVM Overview

1.1 Features

- Full-featured evaluation board for the TLV320AIC3254 stereo audio codec.
- USB connection to PC provides power, control, and streaming audio data for easy evaluation.
- Onboard microphone for ADC evaluation
- Connection points for external control and digital audio signals for quick connection to other circuits/input devices.

The TLV320AIC3254EVM-K is a complete evaluation kit, which includes a universal serial bus (USB)-based motherboard and evaluation software for use with a personal computer running the Microsoft Windows™ operating system (Win2000 or XP).

1.2 Introduction

The TLV320AIC3254EVM is in the Texas Instruments (TI) modular EVM form factor, which allows direct evaluation of the device performance and operating characteristics and eases software development and system prototyping.

The TLV320AIC3254EVM-K is a complete evaluation/demonstration kit, which includes a USB-based motherboard called the USB-MODEVM Interface board and evaluation software for use with a personal computer (PC) running the Microsoft Windows operating systems.

The TLV320AIC3254EVM-K is operational with one USB cable connection to a PC. The USB connection provides power, control, and streaming audio data to the EVM for reduced setup and configuration. The EVM also allows external control signals, audio data, and power for advanced operation, which allows prototyping and connection to the rest of the development or system evaluation.

2 EVM Description and Basics

This section provides information on the analog input and output, digital control, power, and general connection of the TLV320AIC3254EVM-K.

2.1 TLV320AIC3254EVM-K Block Diagram

The TLV320AIC3254EVM-K consists of two separate circuit boards, the USB-MODEVM and the TLV320AIC3254EVM. The USB-MODEVM is built around the TAS1020B streaming audio USB controller with an 8051-based core. The motherboard features two positions for modular EVMs, or one double-wide serial modular EVM can be installed. The TLV320AIC3254EVM is one of the double-wide modular EVMs that is designed to work with the USB-MODEVM.

The simple diagram of Figure 1 shows how the TLV320AIC3254EVM is connected to the USB-MODEVM. The USB-MODEVM Interface board is intended to be used in USB mode, where control of the installed EVM is accomplished using the onboard USB controller device. Provision is made, however, for driving all the data buses (I^2C™, SPI™, I^2S, etc.) externally. The source of these signals is controlled by SW2 on the USB-MODEVM. See Table 1 for details on the switch settings.

The USB-MODEVM has two EVM positions that allow for the connection of two small evaluation module or one larger evaluation module. The TLV320AIC3254EVM is designed to fit over both of the smaller evaluation module slots as shown in Figure 1

2.1.1 USB-MODEVM Interface Board

The simple diagram of Figure 1 shows only the basic features of the USB-MODEVM Interface board.

Because the TLV320AIC3254EVM is a double-wide modular EVM, it is installed with connections to both EVM positions, which connects the TLV320AIC3254 digital control interface to the I^2C port realized using the TAS1020B, as well as the TAS1020B digital audio interface.

In the factory configuration, the board is ready to be used with the USB-MODEVM. To view all the functions and configuration options available on the USB-MODEVM board, see the USB-MODEVM Interface Board schematic in Appendix G.

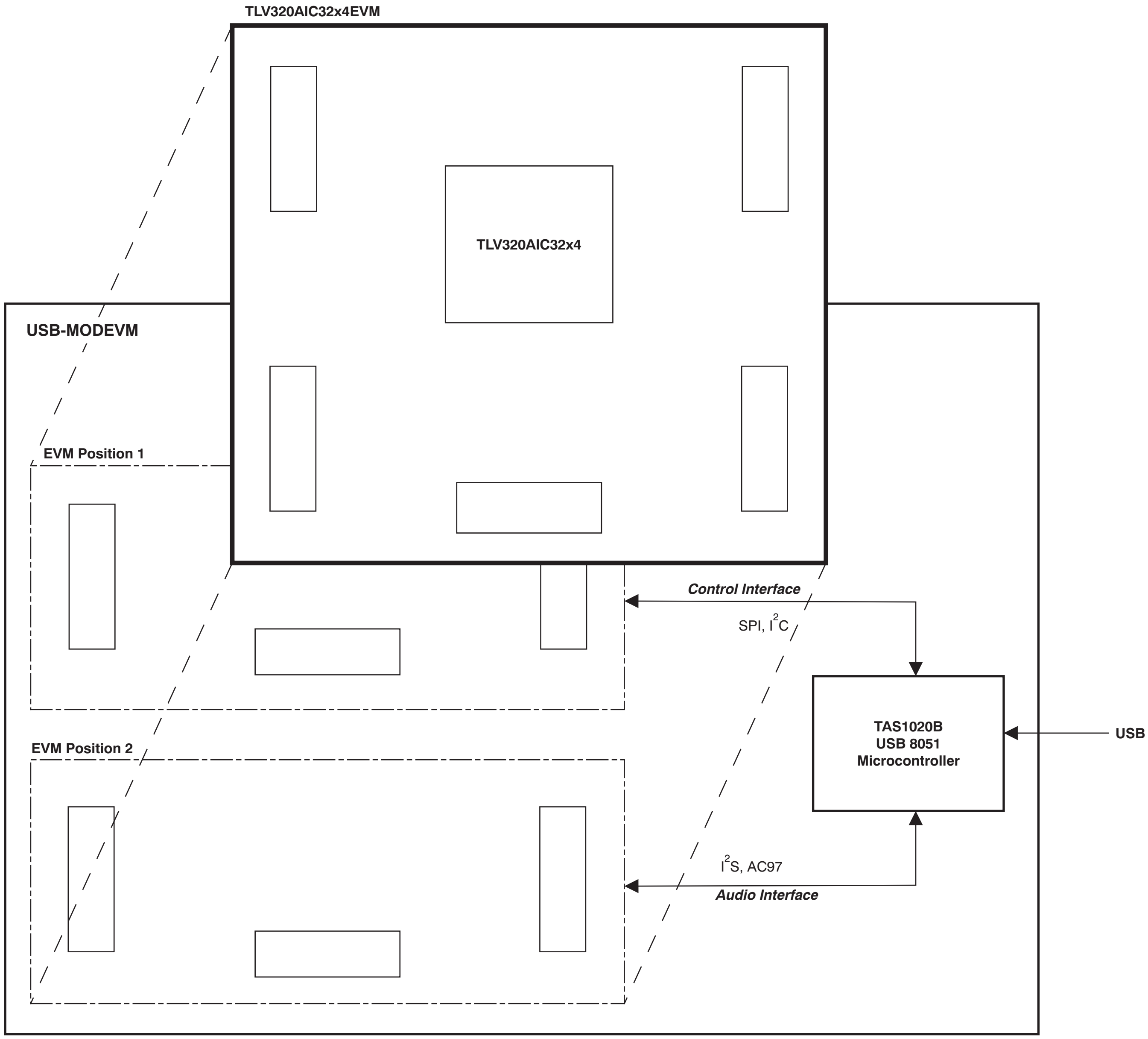


Figure 1. TLV320AIC3254EVM-K Block Diagram

2.2 Default Configuration and Connections

2.2.1 USB-MODEVM

Table 1 provides a list of the SW2 settings on the USB-MODEVM. For use with the TLV320AIC3254EVM, SW-2 positions 1, 3, 4, 5, 6, and 7 must be set to ON, whereas SW-2.2 and SW-2.8 must be set to OFF. If the TLV320AIC3254EVM is to be used with an external audio interface, SW2.4 and SW2.5 also need to be set to OFF and such interface must be connected as explained in Section 2.4

Table 1. USB-MODEVM SW2 Settings

SW-2 Switch Number	Label	Switch Description
1	A0	USB-MODEVM EEPROM I^2C Address A0 ON: A0 = 0 OFF: A0 = 1
2	A1	USB-MODEVM EEPROM I^2C Address A1 ON: A1 = 0 OFF: A1 = 1
3	A2	USB-MODEVM EEPROM I^2C Address A2 ON: A2 = 0 OFF: A2 = 1
4	USB I^2S	I^2S Bus Source Selection ON: I^2S Bus connects to TAS1020 OFF: I^2S Bus connects to USB-MODEVM J14
5	USB MCK	I^2S Bus MCLK Source Selection ON: MCLK connects to TAS1020 OFF: MCLK connects to USB-MODEVM J14
6	USB SPI	SPI Bus Source Selection ON: SPI Bus connects to TAS1020 OFF: SPI Bus connects to USB-MODEVM J15
7	USB RST	RST Source Selection ON: EVM Reset Signal comes from TAS1020 OFF: EVM Reset Signal comes from USB-MODEVM J15
8	EXT MCK	External MCLK Selection ON: MCLK Signal is provided from USB-MODEVM J10 OFF: MCLK Signal comes from either selection of SW2-5

2.2.2 TLV320AIC3254 Jumper Locations

Table 2 provides a list of jumpers found on the EVM and their factory default conditions.

Table 2. List of Jumpers and Switches

Jumper	Default Position	Jumper Description
W1	2-3	When connecting 2-3, microphone bias comes from the MICBIAS pin on the device; when connecting 1-2, microphone (mic) bias is supplied through TP8.
W2	Installed	Connects onboard Mic negative terminal to the circuit.
W3	Installed	Connects onboard Mic positive terminal to the circuit.
W4	Open	Provides mic bias to J5.3 (disconnect W2 and W3 before installing this jumper). Use for stereo electret microphones only.
W5	Installed	Provides mic bias to J5.2 and onboard Mic positive terminal.
W6	Installed	Sets the mic bias resistance to 1 kΩ. Use for differential electret mic configurations.
W7	Installed	Connects J5.3 and onboard Mic negative terminal to the circuit.
W8	2-3	Connects J5.3 and onboard Mic negative terminal to AVSS or 1-kΩ resistor.
W9	Open	Connects 16-Ω load to HPL outputs.
W10	Open	Connects 16-Ω load to HPR outputs.
W11	Open	When installed, shorts across the output capacitor on HPL; remove this jumper if using AC-coupled output drive
W12	Open	When installed, shorts across the output capacitor on HPR; remove this jumper if using AC-coupled output drive
W13	Installed	When installed, it selects onboard EEPROM as firmware source.
W14	1-2	When set to 1-2, SCLK/MIC_DET is used for SPI SCLK. When set to 2-3, SCLK/MIC_DET is used for headset detection.

Table 2. List of Jumpers and Switches (continued)

Jumper	Default Position	Jumper Description
W15	Open	When installed, connects GPIO4 to reset AND gate (U3).
W16	Installed	Provides a means of measuring IOVDD current.
W17	Installed	Provides a means of measuring DVDD current.
W18	Installed	Provides a means of measuring LDOin/HPVDD current. **???**
W19	Installed	Provides a means of measuring AVDD current.
W20	2-3	Sets U6 voltage source as +5VD or +5VA for LDOin/HPVDD.
W21	Installed	Connects +3.3VD voltage source to IOVDD node.
W22	Open	When installed, shorts across the input capacitor on IN2_L for DC measurement option. Remove this jumper for audio connections.
W23	Open	When installed, shorts across the input capacitor on IN2_R for DC measurement option. Remove this jumper for audio connections.
SW1	I2C	When set to I2C, the I^2C signals from P12/J12 are connected to the codec and SPI_SELECT is set low. When set to SPI, the SPI signals from P12/J12 are connected to the codec and SPI_SELECT is pulled to IOVDD.
SW2	LOW	When set to LOW, AVDD and DVDD are connected to +1.8VA and +1.8VD, respectively, and LDO_SELECT is set low. When set to HI, AVDD, and DVDD are disconnected from other supplies and LDO_SELECT is pulled to IOVDD.

2.3 Analog Signal Connections

2.3.1 Analog Inputs

The analog input sources can be applied directly to terminal blocks J2, J3, and J4 or input jacks J1 and J5. The connection details can be found in Appendix A.

2.3.2 Analog Output

The analog outputs are available from terminal blocks J6 and J8 or output jacks J7, J9, and J10. Note that J10 is provided for signal-to-noise ratio (SNR) measurements only. The connection details can be found in Appendix A.

2.4 Digital Signal Connections

The digital inputs and outputs of the EVM can be monitored through P12 and P22. If external signals need to be connected to the EVM, digital inputs must be connected via J14 and J15 on the USB-MODEVM and the SW2 switch must be changed accordingly (see Section 2.2.1). The connector details are available in Section A.2.

2.5 Power Connections

The TLV320AIC3254EVM can be powered independently when being used in stand-alone operation or by the USB-MODEVM when it is plugged onto the motherboard.

2.5.1 Stand-Alone Operation

When used as a stand-alone EVM, power is applied to P23/J23 directly, making sure to reference the supplies to the appropriate grounds on that connector.

CAUTION

Verify that all power supplies are within the safe operating limits shown on the TLV320AIC3254 data sheet before applying power to the EVM.

P23/J23 provides connection to the common power bus for the TLV320AIC3254EVM. Power is supplied on the pins listed in Table 6.

The TLV320AIC3254EVM-K motherboard (the USB-MODEVM Interface board) supplies power to P23/J23 of the TLV320AIC3254EVM. Power for the motherboard is supplied either through its USB connection or via terminal blocks on that board.

2.5.2 USB-MODEVM Operation

The USB-MODEVM Interface board can be powered from several different sources:

- USB
- 6-Vdc to 10-Vdc AC/DC external wall supply (not included)
- Laboratory power supply

When powered from the USB connection, JMP6 must have a shunt from pins 1–2 (this is the default factory configuration). When powered from 6-Vdc to 10-Vdc power supply, either through the J8 terminal block or J9 barrel jack, JMP6 must have a shunt installed on pins 2–3. If power is applied in any of these ways, onboard regulators generate the required supply voltages, and no further power supplies are necessary.

If laboratory supplies are used to provide the individual voltages required by the USB-MODEVM Interface, JMP6 must have no shunt installed. Voltages are then applied to J2 (+5VA), J3 (+5VD), J4 (+1.8VD), and J5 (+3.3VD). The +1.8VD and +3.3VD can also be generated on the board by the onboard regulators from the +5VD supply; to enable this configuration, the switches on SW1 need to be set to enable the regulators by placing them in the ON position (lower position, looking at the board with text reading right-side up). If +1.8VD and +3.3VD are supplied externally, disable the onboard regulators by placing SW1 switches in the OFF position.

Each power supply voltage has an LED (D1-D7) that illuminates when the power supplies are active.

3 TLV320AIC3254EVM-K Setup and Installation

The following section provides information on using the TLV320AIC3254EVM-K, including setup, program installation, and program usage.

NOTE: If using the EVM in stand-alone mode, the software must be installed per the following instructions, but the hardware configuration may be different.

3.1 Software Installation

1. Download the latest version of the AIC3254 Control Software (CS) located in the TLV320AIC3254EVM-K Product Folder.
2. Open the self-extracting installation file.
3. Extract the software to a known folder.
4. Install the EVM software by double-clicking the **Setup** executable, and follow the directions. The user may be prompted to restart their computer.

This installs all the TLV320AIC3254EVM-K software and required drivers onto the PC.

3.2 EVM Connections

1. Ensure that the TLV320AIC3254EVM is installed on the USB-MODEVM Interface board, aligning J11, J12, J21, J22, and J23 with the corresponding connectors on the USB-MODEVM.
2. Verify that the jumpers and switches are in their default conditions.
3. Attach a USB cable from the PC to the USB-MODEVM Interface board. The default configuration provides power, control signals, and streaming audio via the USB interface from the PC. On the USB-MODEVM, LEDs D3, D4, D5, and D7 illuminate to indicate that the USB is supplying power.
4. For the first connection, the PC recognizes new hardware and begins an initialization process. The user may be prompted to identify the location of the drivers or allow the PC to automatically search for them. Allow the automatic detection option.
5. Once the PC confirms that the hardware is operational, D2 on the USB-MODEVM illuminates to indicate that the firmware has been loaded and the EVM is ready for use. If D2 does not illuminate, verify that the EEPROM jumper and switch settings conform to Table 1 and Table 2.

After the TLV320AIC3254EVM-K software installation (described in Section 3.2) is complete, evaluation and development with the TLV320AIC3254 can begin.

The TLV320AIC3254EVM-K software can now be launched. The user sees an initial screen that looks similar to Figure 2.

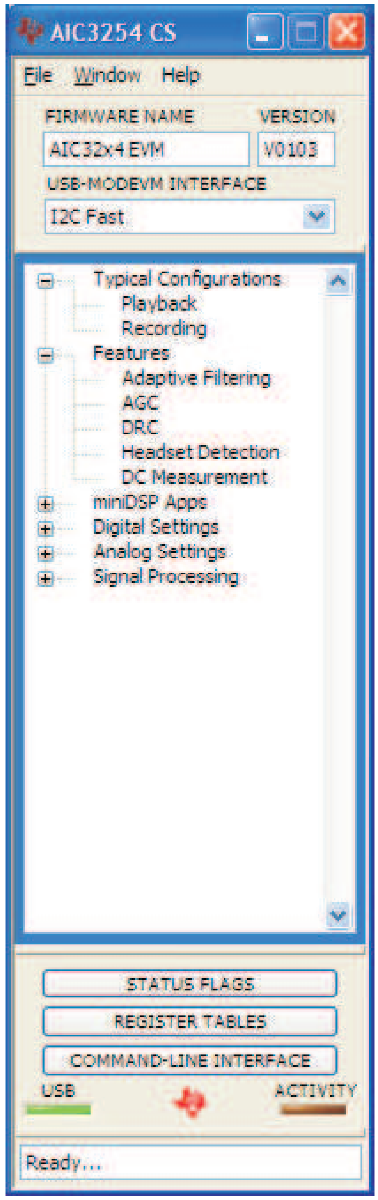


Figure 2. Initial Screen of TLV320AIC3254EVM-K Software

If running the software in Windows Vista or Windows 7, right-click the AIC3254EVM-K CS shortcut and select *Properties*. Configure the *Compatibility* tab as shown in Figure 3

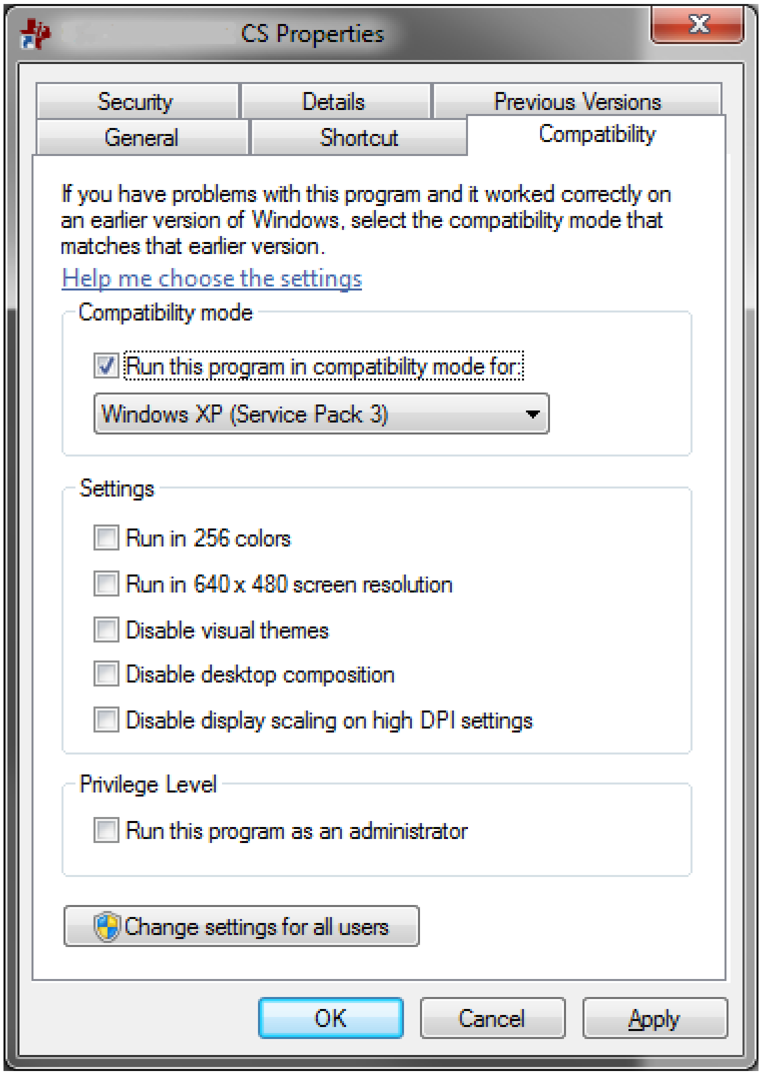


Figure 3. Compatibility Tab

4 AIC3254 Control Software

The AIC3254 Control Software (CS) is an intuitive, easy-to-use, powerful tool to learn, evaluate, and control the TLV320AIC3254. This tool was specifically designed to make learning the TLV320AIC3254 software easy. The following sections describe the operation of this software.

NOTE: For configuration of the codec, the TLV320AIC3254 block diagram located in the TLV320AIC3254 data sheet is a good reference to help determine the signal routing.

4.1 Main Panel Window

The Main Panel window, shown in Figure 2, provides easy access to all the features of the AIC3254 CS. The Firmware Name and Version boxes provide information about the firmware loaded into the EVM's EEPROM.

The USB-MODEVM Interface drop-down menu allows the user to select which communication protocol the TAS1020B USB Controller uses to communicate with the TLV320AIC3254 or to toggle the TAS1020B GPIO pins. The TLV320AIC3254 supports I^2C Standard, I^2C Fast, and 8-bit register SPI. The USB-MODEVM Interface selection is global to all panels, including the Command-Line Interface. To communicate to the TLV320AIC3254 using SPI, SW1 must be switched towards SPI and W14 must be set to 1-2 on the TLV320AIC3254EVM.

The Panel Selection Tree provides access to typical configurations, features, and other panels that allow the user to control the TLV320AIC3254. The tree is divided into several categories which contain items that pop up panels. A panel can be opened by double-clicking any item inside a category in the Panel Selection Tree.

Below the Panel Selection Tree are three buttons that pop up the following:

- Status Flags - Allows the user to monitor the TLV320AIC3254 status flags.
- Register Tables - A tool to monitor register pages.
- Command-Line Interface - A tool to execute/generate scripts and monitor register activity.

The USB LED indicates if the EVM kit is recognized by the software and the ACTIVITY LED illuminates every time a command request is sent.

The dialog box at the bottom of the Main Panel provides feedback of the current status of the software.

4.1.1 Typical Configurations

This category can help users to quickly become familiar with the TLV320AIC3254. Each of the panels that can be accessed through this menu have controls relevant to the selected configuration; a tab shows the script that will be loaded for that particular configuration. Each script includes a brief description of the selected configuration, as shown in Figure 4.

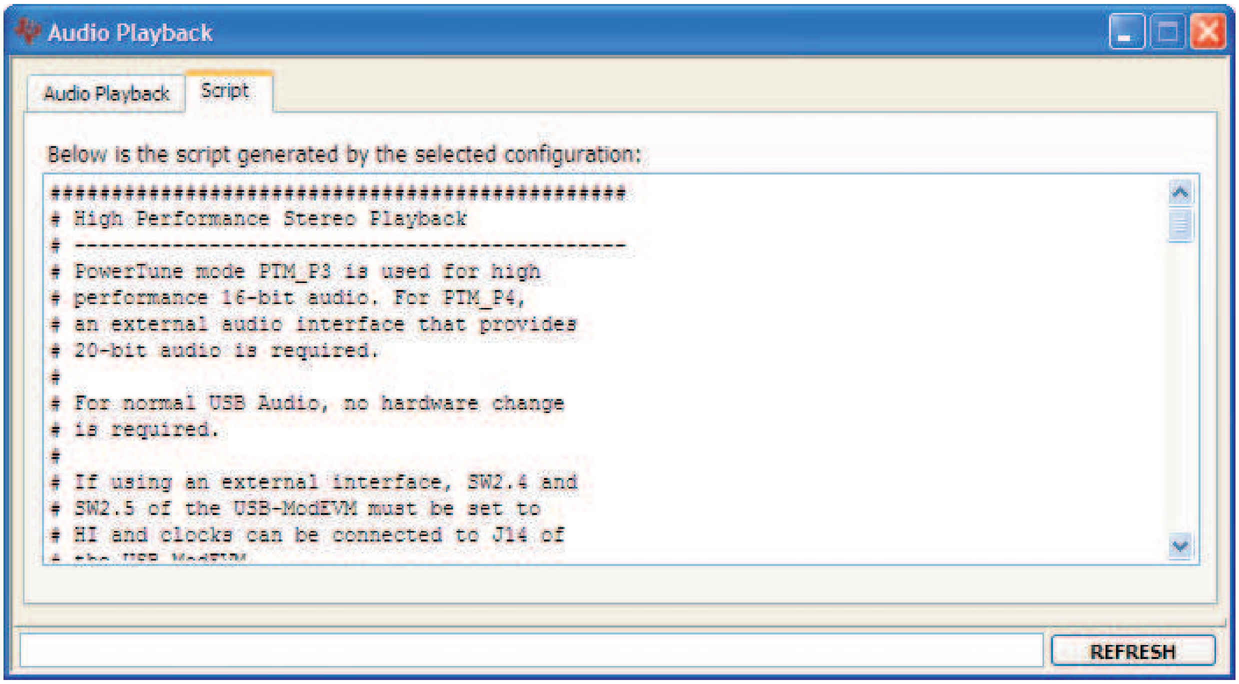


Figure 4. Playback Script Tab

4.1.1.1 Playback

The Playback panel (shown in Figure 5) has the following configurations:

- High Performance Stereo Playback - this configuration programs the TLV320AIC3254 in PowerTune™ mode PTM_P3, for low-noise, high-performance stereo playback through both line and headphone outputs.
- Low Power Stereo Playback - this configuration programs the TLV320AIC3254 in PowerTune ™ mode PTM_P1 for low-power stereo playback through both line and headphone outputs.
- Direct Analog Bypass - this configuration routes IN1_L/IN1_R to HPL/HPR.
- PGA Analog Bypass - this configuration routes IN1_L/IN1_R to the analog input amplifier (Mic PGA) which is then routed to both the line and headphone amplifiers.

The analog inputs and outputs used for these configurations can be accessed as follows:

1. IN1_L / IN1_R - Jack J1 or terminal block J2.
2. Line outputs - Jack J7 or terminal block J6.
3. Headphone outputs - Jack J9 or terminal block J8.

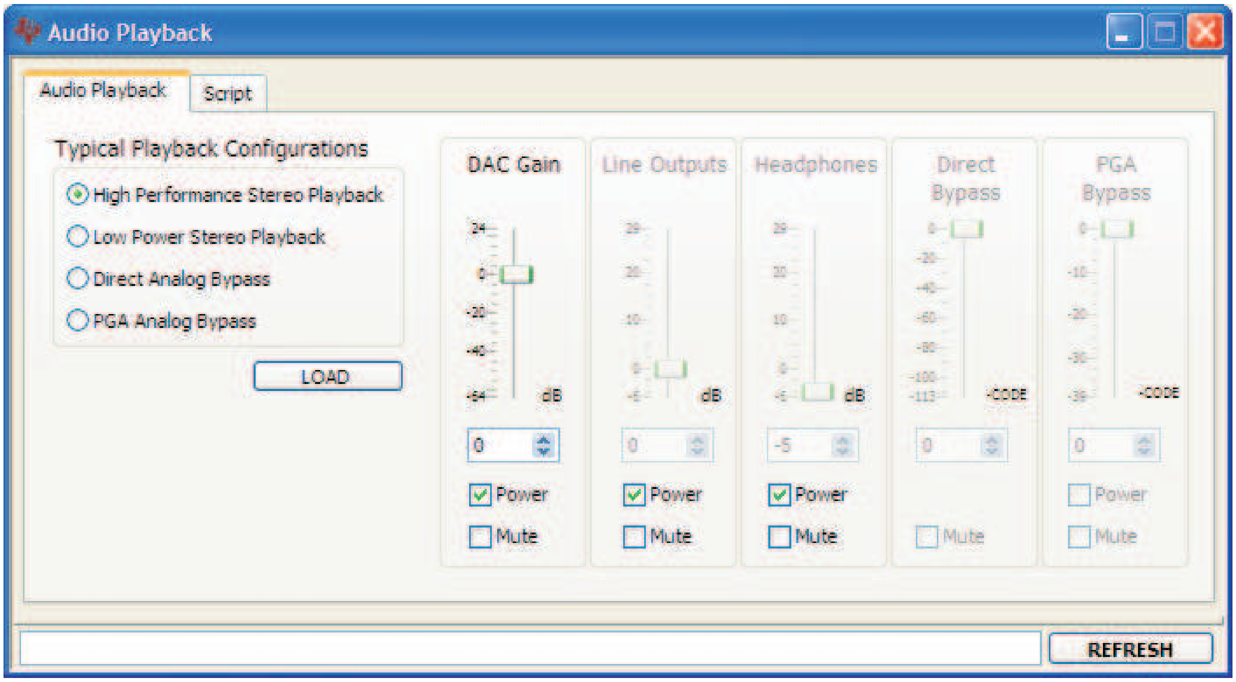


Figure 5. Playback Panel

4.1.1.2 Recording

The Recording panel (shown in Figure 6) has the following configurations:

- High Performance Stereo Recording - this configuration programs the TLV320AIC3254 in PowerTune ™ mode PTM_R4, for low-noise, high-performance stereo recording. IN1_L and IN1_R are routed in a single ended fashion.
- Low Power Stereo Recording - this configuration programs the TLV320AIC3254 in PowerTune ™ mode PTM_R1 for low-power stereo playback. IN1_L and IN1_R are routed in a single ended fashion.
- Differential On-Board Microphone - this configuration programs the TLV320AIC3254's IN3_L and IN3_R as a differential pair. Jumpers related to the onboard microphone (W1 to W8) must be set to their default configuration as described in Table 2.

  The analog inputs used for these configurations can be accessed as follows:

  1. IN1_L / IN1_R - Jack J1 or terminal block J2.
  2. IN3_L / IN3_R - Terminal block J4. Note that the onboard jack J5 must not be used for a differential configuration.

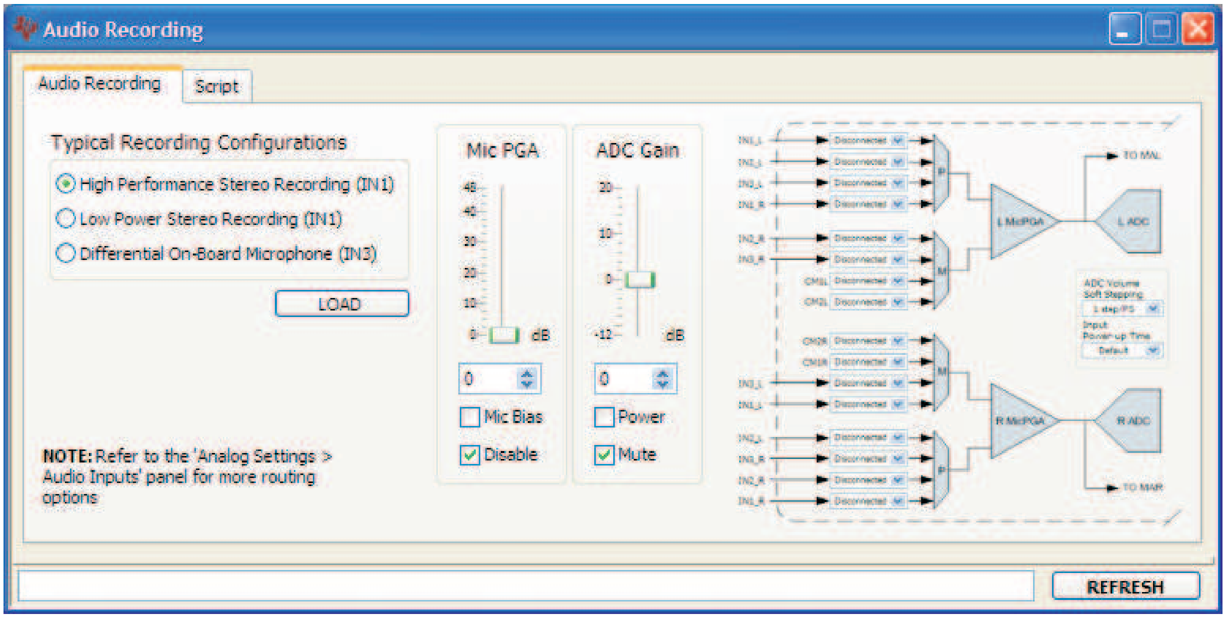


Figure 6. Recording Panel

4.1.2 Features

The **Features** category allows the user to evaluate various features of the TLV320AIC3254. Each of the **Features** panels include an **Information** tab that explains the feature and provides hardware setup information for easy evaluation, as seen in Figure 7.

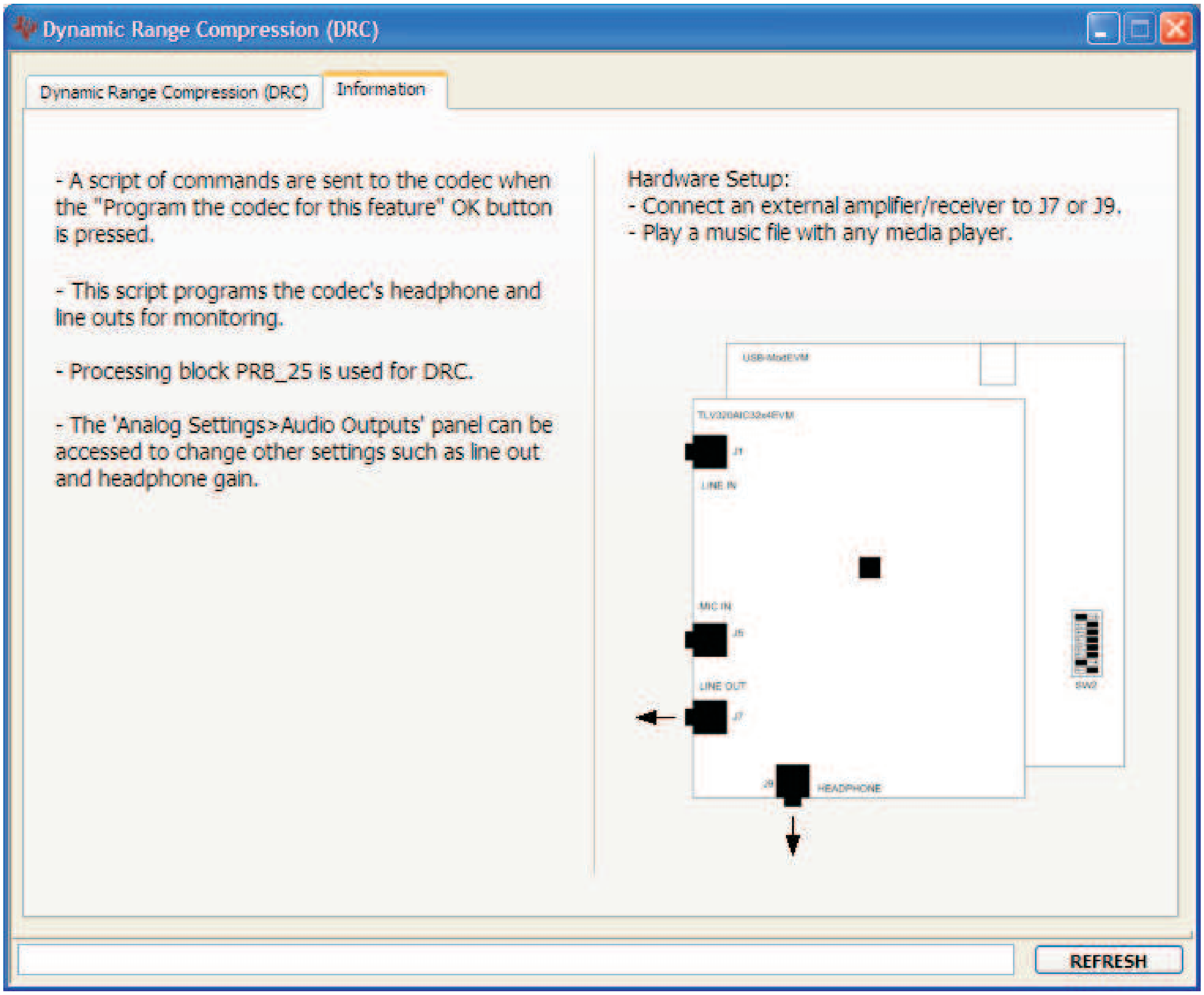


Figure 7. DRC Information Tab

Any item in the **Features** category can be accessed by a double-click. As soon as a **Features** panel opens, a pop-up message appears asking to program the codec for that feature (see Figure 8). A command script is sent to the codec if the **OK** button is clicked. This script programs all registers necessary to evaluate the feature. This can be bypassed by clicking the **Cancel** button.

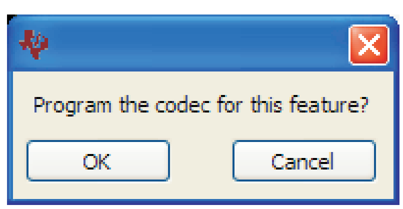


Figure 8. Program Codec Pop-Up Window

The script corresponding to each feature can be accessed at the Installation Directory\DATA\EVM folder. Also, each script can be manually customized and loaded as the feature's start-up script as long as the file name remains the same.

4.1.2.1 Adaptive Filtering

The TLV320AIC3254 features double-buffered filter coefficients which allow real-time filtering. The TLV320AIC3254 features up to six cascaded biquads and a first-order IIR filter per DAC channel in various signal processing blocks. Note that the TLV320AIC3254 has the potential for a larger amount of biquad sections if the embedded miniDSP is used for signal processing (see Section 4.1.3.1).

The Parametric Equalizer tab (shown in Figure 9) allows the user to modify the frequency response of the digital input signal that is fed afterwards into the DAC channels. This application can be useful to fine-tune the audio frequency response for a particular small speaker and enclosure system combination. The processing block PRB_P2 (which is used for this application) has one IIR filter and six biquads in cascade per audio channel. The first biquad (BQ0) is configured as a gain control which provides headroom and compensation gain to the subsequent biquads in the cascade. Biquads BQ1 to BQ5 are configured for EQ and/or shelf filters.

The **Gain Q** (quality) and **fc** (center frequency) parameters are available for the EQ filters whereas **Gain fc** (corner frequency) and **Shelf Response** are available for the shelf filters. These parameters can be modified using their corresponding control. Also, by dragging a cursor in the frequency response window, the gain and fc for each biquad can be modified.

The PRB_P2 biquad coefficients are defined as 1.23, 2s complement format. Coefficients that are equal or larger than unity must be normalized to comply with such format when converting from decimal format. This can be achieved by dividing all numerators of a biquad by a scale factor equal to the largest numerator divided by 2^{23} minus one (if the numerator is equal or larger than unity). Normalization results in an attenuated version of the same frequency response curve. The scale factor can then be used to compensate for the attenuation at another unused biquad.

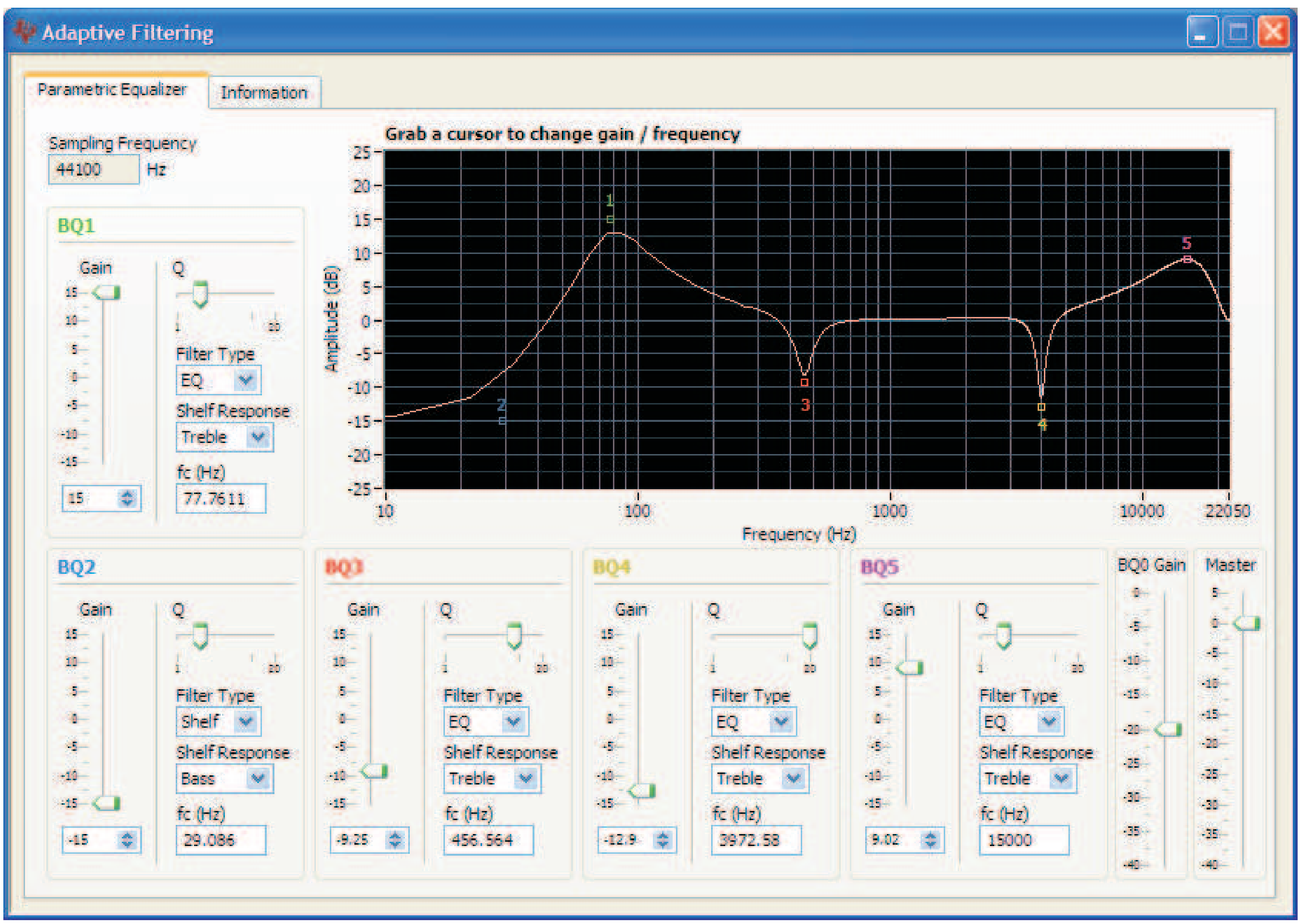


Figure 9. Adaptive Filtering Panel

4.1.2.2 Automatic Gain Control

The left-channel Automatic Gain Control (AGC) can be enabled by checking the **Enable Left AGC** box (Figure 10). Pressing the **Capture Audio** button records the left-channel audio. Its corresponding data is displayed in the audio capture graph window. The small white window located at the bottom right of the AGC tab displays the audio waveform of the recorded data. Ensure that the AIC32x4 EVM is selected as the computer's default audio capture device before pressing this button. To set the TLV320AIC3254EVM-K as the default audio device, open the Windows™ Control Panel → Sounds and Audio Devices Properties and set the AIC32x4 EVM as the default audio recording device. Also, do not use any other media player or audio recording software while the control software is recording.

The **target level** and **noise threshold** parameters can be modified by dragging the horizontal cursor lines located at the audio capture graph window. Its numeric values are displayed to the right of the graph. Noise threshold can be disabled by unchecking the **Enable Noise Threshold** box. The **AGC Max Gain** control sets the maximum allowed AGC PGA Gain. The **AGC Gain** indicator bar continuously displays the contents of Page 0/Register 93 if the **Enable Polling** box is checked.

Other parameters can be accessed by checking the **Advanced?** box. For more information about AGC, see the **Information** tab and the data sheet.

Other flags related to this feature can be accessed at the **Status Flags** panel.

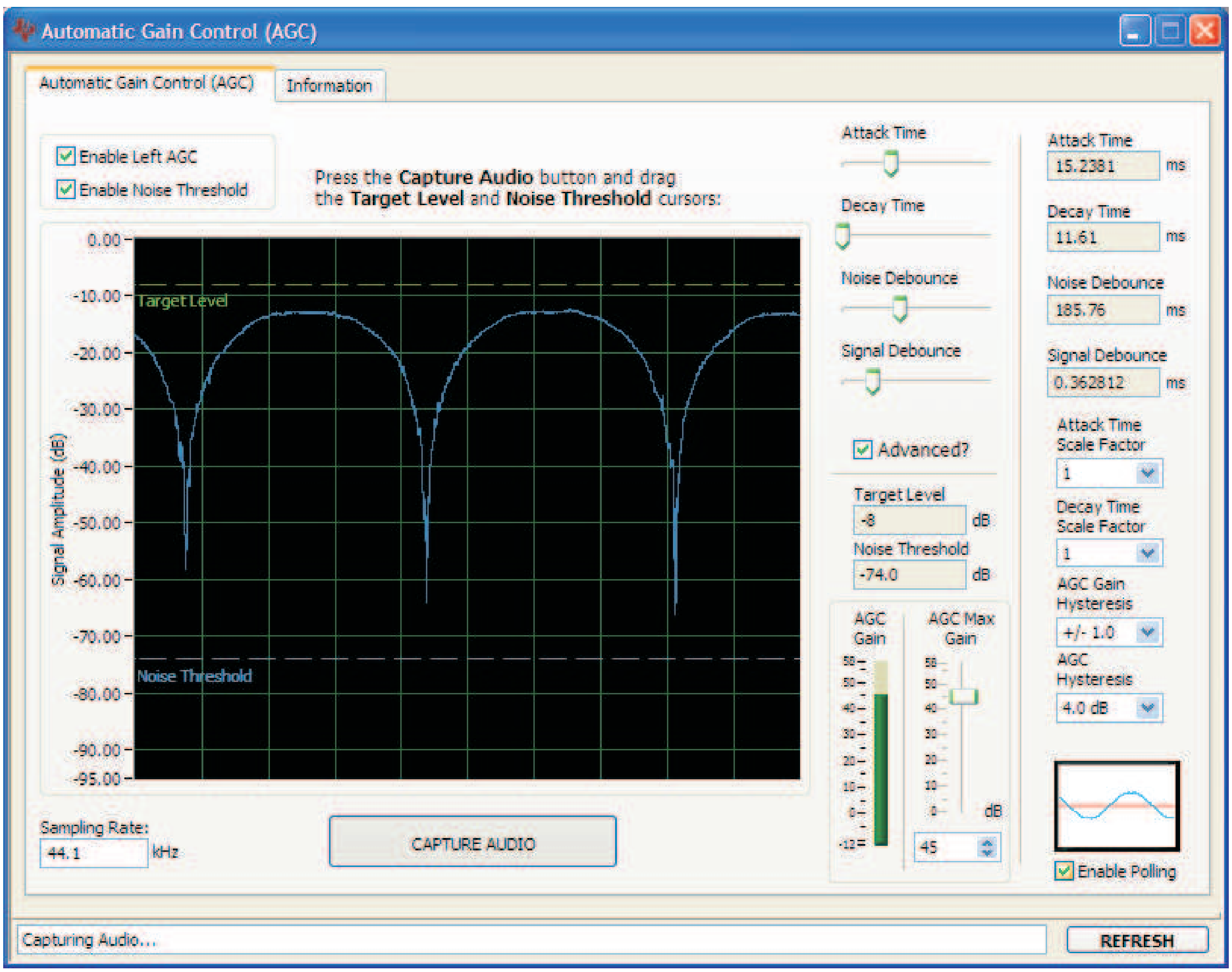


Figure 10. Automatic Gain Control Panel

4.1.2.3 Dynamic Range Compression

Dynamic Range Compression (DRC) can be enabled by checking the **Enable Left DRC** and **Enable Right DRC** boxes.

The level transfer characteristic graph is a function of the applied digital gain and the threshold parameter. The graph line is separated into two piece-wise linear regions where the red line represents the level range in which the DRC attenuation takes place, and the green line represents the level range in which the signal is not affected by DRC. As an example, setting the threshold to -24 dB with a gain to 24 dB implies that an input signal strength variation from -48 dB (threshold - gain) to 0 dB results in an output signal strength variation from -24 dB to 0 dB, or a compression ratio of 2:1. Similarly, a threshold of -3 dB with a gain of 24 dB implies that an input signal strength variation from -27 dB to 0 dB results in an output signal strength variation from -3 dB to 0 dB, or a ratio of 9:1. Note that a gain less than 0 dB does not result in expansion.

The **Attack** and **Decay** are time domain parameters that control the rate in which the applied gain reaches the target gain after the threshold level is crossed. As an example, a fast attack rate quickly reaches the target gain once the output signal crosses the programmed threshold region.

Other flags related to this feature can be accessed at the **Status Flags** panel.

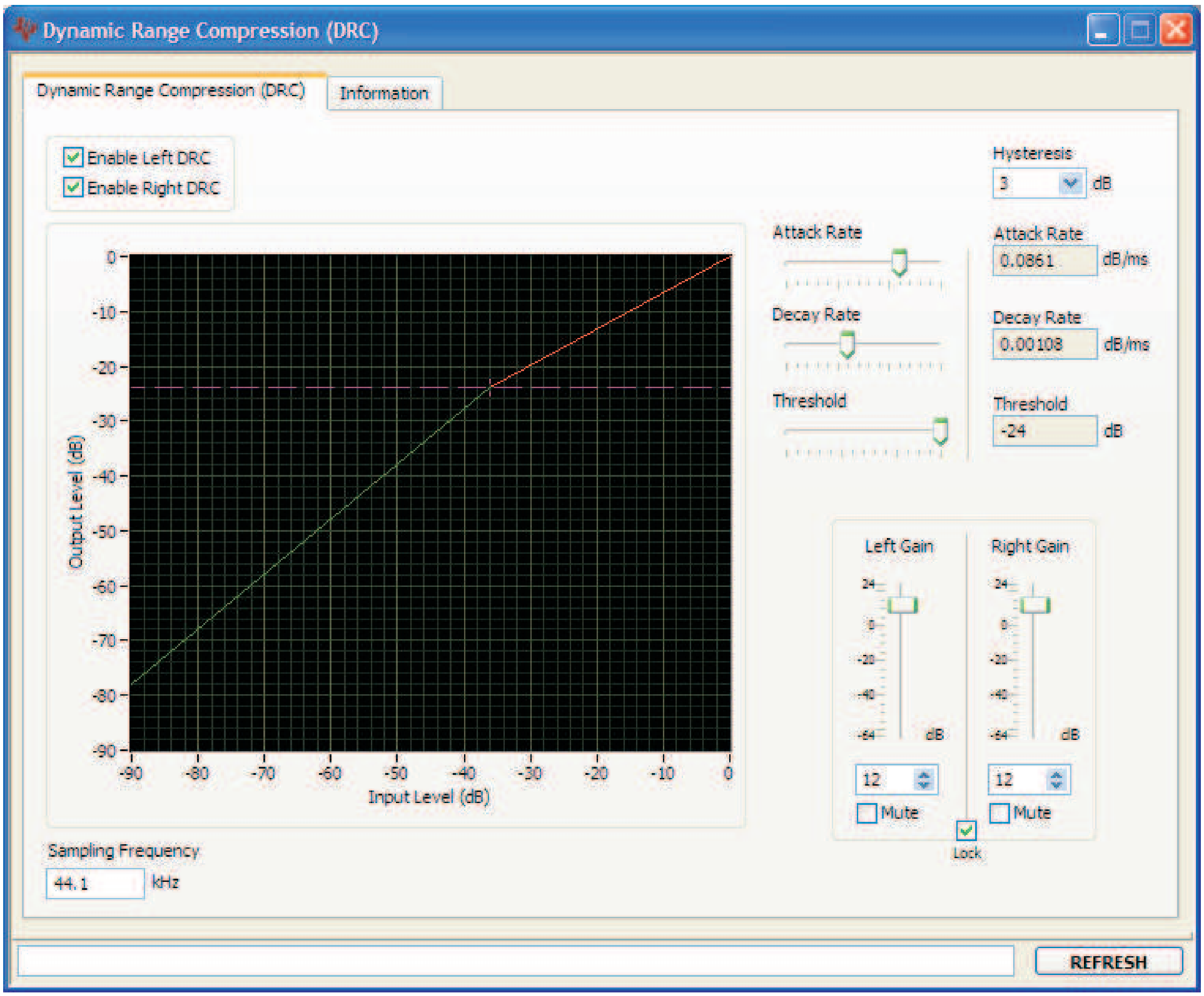


Figure 11. Dynamic Range Compression Panel

4.1.2.4 Headset Detection

The TLV320AIC3254EVM provides two terminal blocks (J8 and J4) that can be used to connect different types of cellular headset jacks. For proper headset detection, the jack connections must comply with the figure shown in the **Headset Detection** section of the datasheet.

The **Headset Detection** panel provides hardware setup information for a four-conductor stereo + cellular jack, as seen in Figure 12.

As an example, if stereo headphones are connected to the four-conductor jack, the tip and ring carry the AC-coupled HPL and HPR signal to the headphone speakers whereas the shield shorts the SCLK/MFP3 pin to ground. This results in a stereo headset detection.

Checking the **Enable Polling** box displays the headset type at the **Headset Type Detected** box.

Other flags related to this feature can be accessed at the **Status Flags** panel.

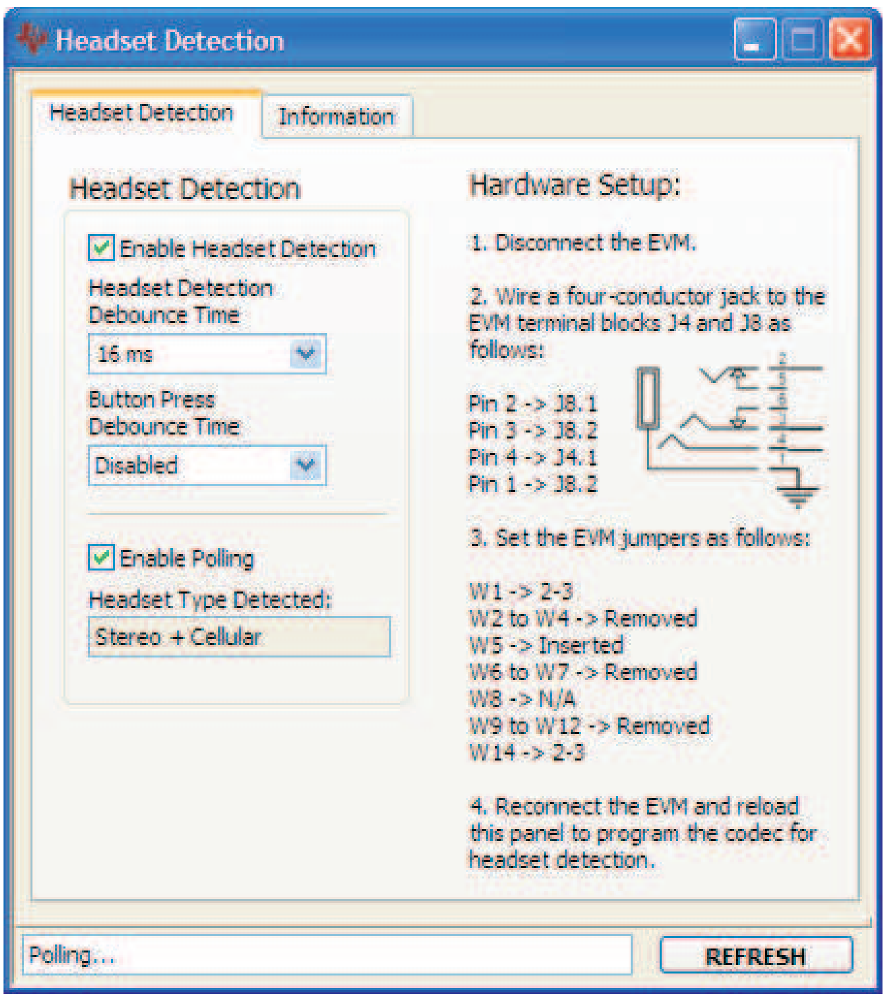


Figure 12. Headset Detection Panel

4.1.2.5 DC Measurement

Terminal block J3 on the TLV320AIC3254EVM can be used to evaluate the DC measurement feature. The **Information** tab provides the hardware setup information.

The **Left ADC (V)** and **Right ADC (V)** boxes convert the register data to voltage. The voltage is derived from the **References** shown at the upper right corner of the **DC Measurement** tab. The DC measurement register data is in 2.22, 2s complement format.

Checking the **Enable Polling** box displays the DC measurement data.

Other flags related to this feature can be accessed at the **Status Flags** panel.

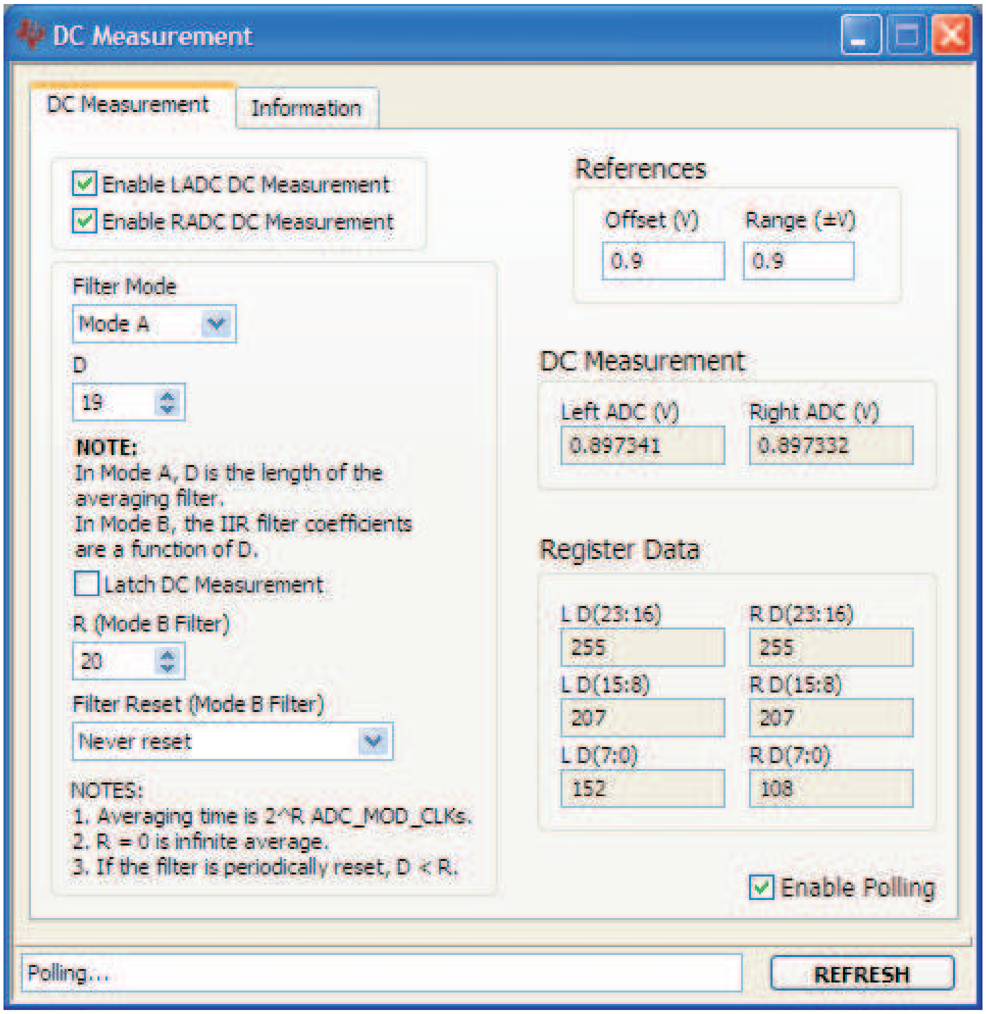


Figure 13. DC Measurement Panel

4.1.3 miniDSP Applications

The TLV320AIC3254 features two miniDSP cores, one for the ADC and another for the DAC.

Currently, the AIC3254 CS has two DAC miniDSP applications: Equalizers and Spectrum Analyzer. Visit the TLV320AIC3254EVM-K product folder for updates and availability on new miniDSP applications.

See the miniDSP section in the data sheet (SLAS549) for information on how to develop custom miniDSP algorithms.

4.1.3.1 Equalizers

The Equalizers miniDSP application features 20 cascaded biquad filters per DAC channel (Figure 14). Each of the 40 20-Band EQ sliders modify its corresponding biquad filter in the cascade as a function of gain. Each **Master** slider controls the digital volume control of the TLV320AIC3254. All sliders can be set to track the opposing channel slider movement by turning on the **Lock L+R** switch. Preset configurations are available at the red selection box below the graphic equalizer. A frequency slider movement changes any preset to Custom.

The **Small Speaker EQ** section, contains filter presets that are suitable for small speaker applications. Emphasizing certain frequencies and reducing low-frequency energy provides higher volume with less distortion and more intelligible speech and music for small speakers. These presets use the first seven biquads of the cascade for filtering whereas the rest of the 13 graphic equalizer sliders can be used to emphasize other frequencies. This feature is enabled by setting the green ON/OFF switch to ON.

Although an option is available to program the codec for this feature when the panel pops up, provision is made to re-program this miniDSP application by clicking the **Program EQ into miniDSP** button.

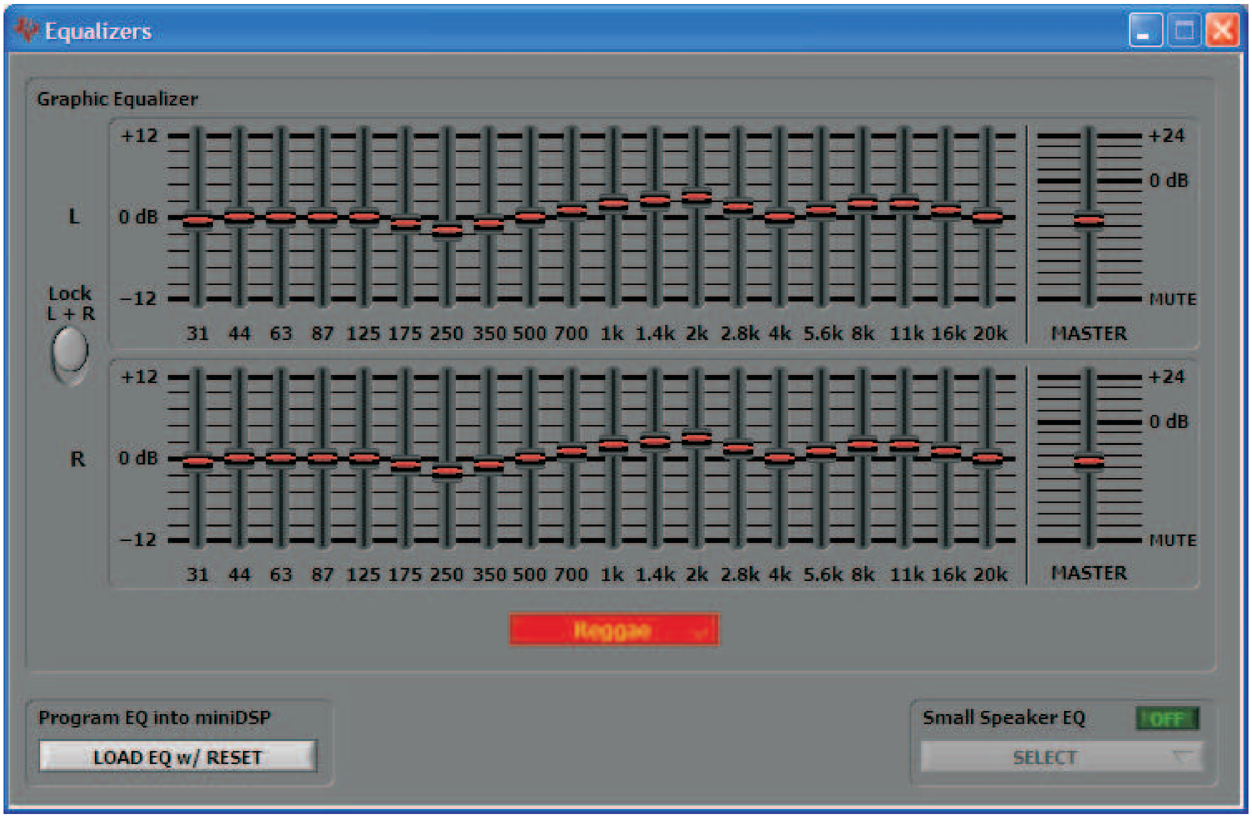


Figure 14. Equalizers miniDSP Application

4.1.3.2 *Spectrum Analyzer*

The 20-Band Spectrum Analyzer provides a visual representation of the frequency content of the input signal (Figure 150. If **Both Channels** is selected in the selection box below the display window, the AIC3254 CS polls the registers related to both channels. To enable polling, set the ON/OFF switch to ON.

Modifying the DAC volume control does not affect the spectrum reading because the analysis is done before the DAC volume control.

Although an option is available to program the codec for this feature when the panel pops up, provision is made to re-program this miniDSP application by clicking the **Program Spectrum Analyzer into miniDSP** button.

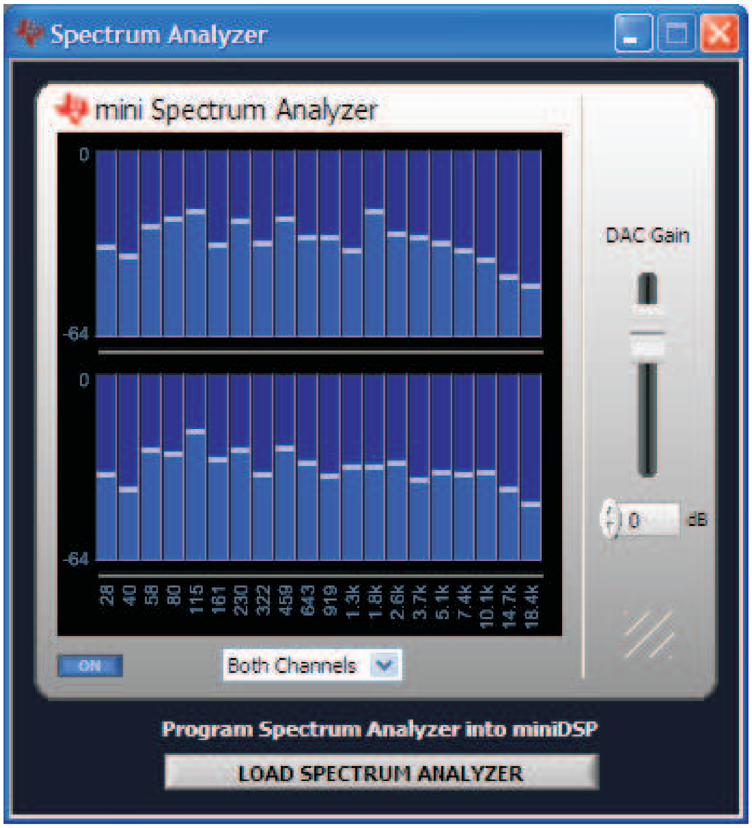


Figure 15. Spectrum Analyzer

4.1.4 Control Categories

The **Digital Settings**, **Analog Settings**, and **Signal Processing** categories provide control of many registers and other features of the TLV320AIC3254 . These categories are intended for the advanced user. Hovering the mouse cursor on top of a control displays a tip strip that contains page, register, and bit information. As an example, hovering on top of IN1_R of the Audio Inputs panel, as shown in Figure 16 displays p1_r55_b7-6 which means that this control writes to Page 1/Register 55/Bits D7 to D6.

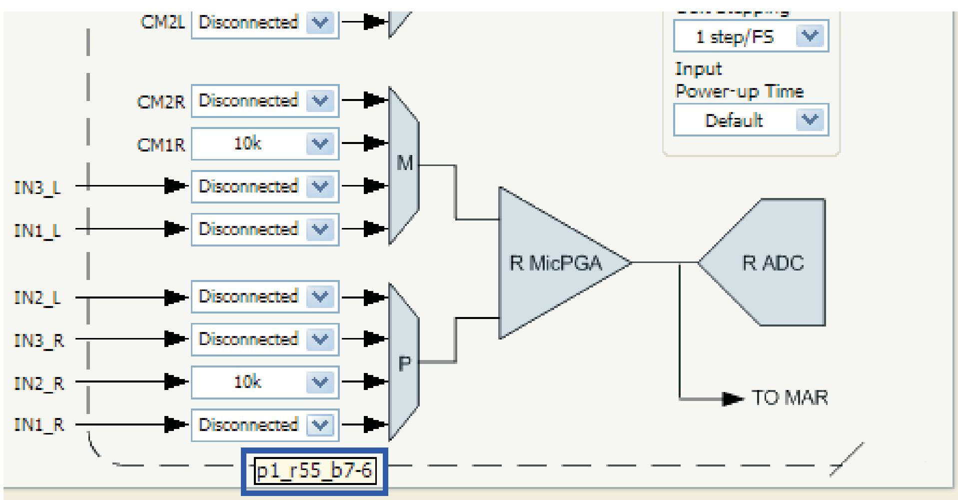


Figure 16. Audio Inputs Panel

Before changing a control, see the data sheet to ensure that a particular control is compatible with the current state of the codec. As an example, some controls in the **Analog Setup** panel must be modified in a particular order as described in the data sheet. Other controls must only be modified with a specific hardware setup, such as powering up the AVDD LDO.

All controls update their status with respect to the register contents in the following conditions:

- A panel is opened.
- The **Execute Command Buffer** button in the **Command-Line Interface** is pressed.
- The **Refresh** button at the bottom right of a panel is pressed.

4.2 Status Flags Panel

The TLV320AIC3254 status flags can monitored in the **Status Flags** panel (Figure 17) which is located below the **Panel Selection Tree** . Pressing the **POLL** button continuously reads all the registers relevant to each flag and updates those flags accordingly. The rate at which the registers are read can be modified by changing the value in the **Polling Interval** numeric control. Note that a smaller interval reduces responsiveness of other controls, especially volume sliders, due to bandwidth limitations. By default, the polling interval is 200 ms and can be set to a minimum of 20 ms.

The **Sticky Flags** tab contains indicators whose corresponding register contents clear every time a read is performed to that register. To read all the sticky flags, click the **Read Sticky Flags** button.

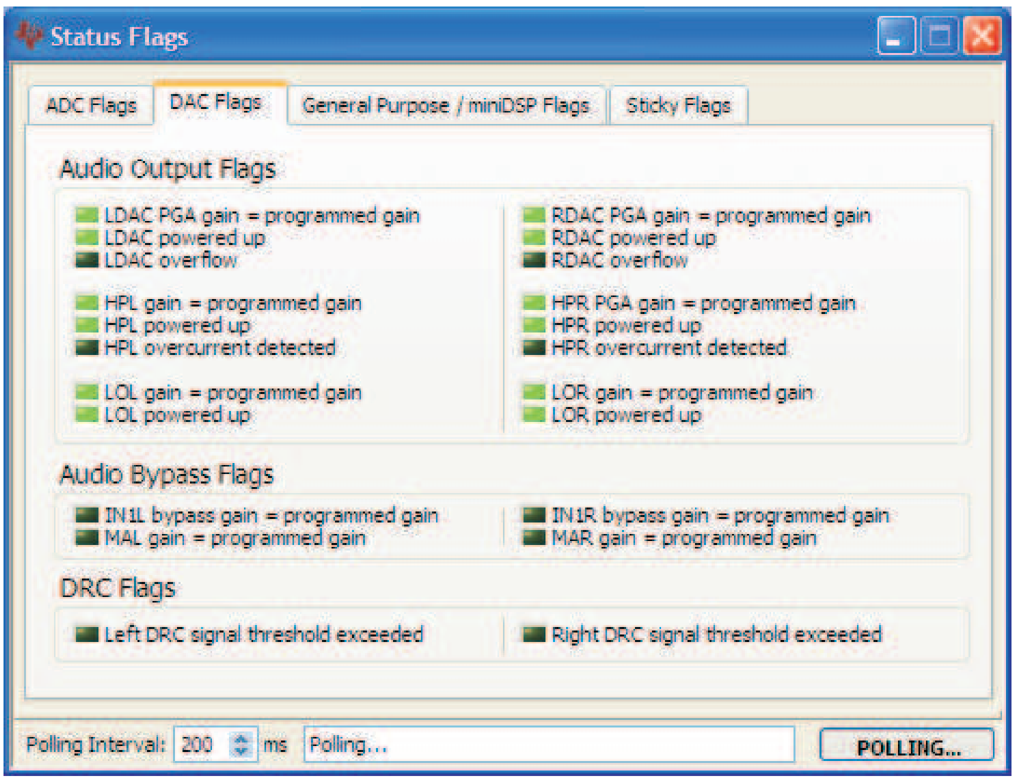
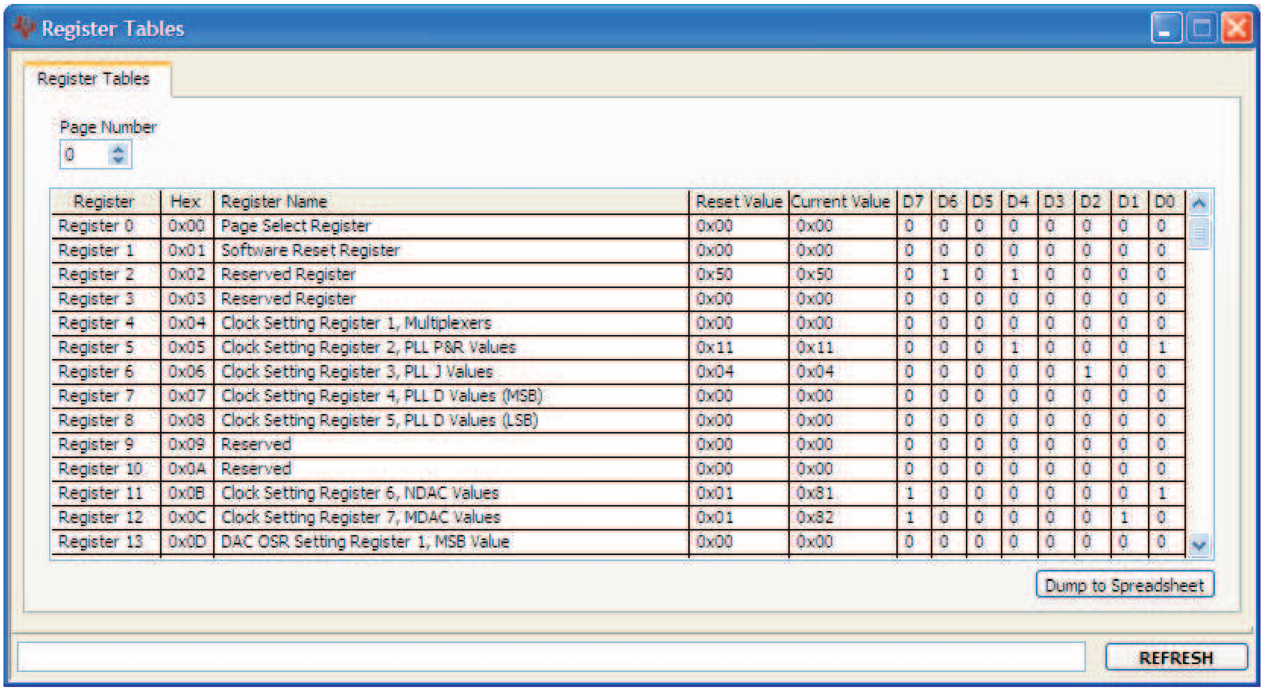


Figure 17. Status Flags Panel

4.3 Register Tables Panel

The contents of configuration and coefficient pages of the TLV320AIC3254 can be accessed through the **Register Tables** panel (Figure 18).

The **Page Number** control changes to the page to be displayed in the register table. The register table contains page information such as the register name, reset value, current value, and a bitmap of the current value. The contents of the selected page can be exported into a spreadsheet by clicking the **Dump to Spreadsheet** button.



Register	Hex	Register Name	Reset Value	Current Value	D7	D6	D5	D4	D3	D2	D1	D0
Register 0	0x00	Page Select Register	0x00	0x00	0	0	0	0	0	0	0	0
Register 1	0x01	Software Reset Register	0x00	0x00	0	0	0	0	0	0	0	0
Register 2	0x02	Reserved Register	0x50	0x50	0	1	0	1	0	0	0	0
Register 3	0x03	Reserved Register	0x00	0x00	0	0	0	0	0	0	0	0
Register 4	0x04	Clock Setting Register 1, Multiplexers	0x00	0x00	0	0	0	0	0	0	0	0
Register 5	0x05	Clock Setting Register 2, PLL P&R Values	0x11	0x11	0	0	0	1	0	0	0	1
Register 6	0x06	Clock Setting Register 3, PLL J Values	0x04	0x04	0	0	0	0	0	1	0	0
Register 7	0x07	Clock Setting Register 4, PLL D Values (MSB)	0x00	0x00	0	0	0	0	0	0	0	0
Register 8	0x08	Clock Setting Register 5, PLL D Values (LSB)	0x00	0x00	0	0	0	0	0	0	0	0
Register 9	0x09	Reserved	0x00	0x00	0	0	0	0	0	0	0	0
Register 10	0x0A	Reserved	0x00	0x00	0	0	0	0	0	0	0	0
Register 11	0x0B	Clock Setting Register 6, NDAC Values	0x01	0x81	1	0	0	0	0	0	0	1
Register 12	0x0C	Clock Setting Register 7, MDAC Values	0x01	0x82	1	0	0	0	0	0	1	0
Register 13	0x0D	DAC OSR Setting Register 1, MSB Value	0x00	0x00	0	0	0	0	0	0	0	0

Figure 18. Register Tables Panel

4.4 *Command-Line Interface Panel*

The **Command-Line Interface** panel provides a means to communicate with the TLV320AIC3254 using a simple scripting language (described in Section G.3). The TAS1020B USB Controller (located on the USB-MODEVM motherboard) handles all communication between the PC and the TLV320AIC3254.

A script is loaded into the command buffer, either by loading a script file using the **File** menu or by pasting text from the clipboard using the Ctrl-V key combination (Figure 19).

When the command buffer is executed, the return data packets which result from each individual command are displayed in the **Command History** control. This control is an array (with a maximum size of 100 elements) that contains information about each command as well as status. The **Interface** box displays the interface used for a particular command in the **Command History** array. The Command box displays the type of command executed (i.e., write, read) for a particular interface. The Flag Retries box displays the number of read iterations performed by a **Wait for Flag** command (see Section G.3 for details). The **Register Data** array displays the register number and data bytes that correspond to a particular command.

The **Information** tab provides additional information related to the **Command History** as well as additional settings. The **Syntax** and **Examples** tabs provide useful information related to the scripting language.

The **File** menu provides some options for working with scripts. The first option, *Open Script File...*, loads a command file script into the command buffer. This script can then be executed by pressing the **Execute Command Buffer** button. The contents of the **Command Buffer** can be saved using the *Save Script File...* option.

Both the **Command Buffer** and **Command History** can be cleared by clicking their corresponding **Clear** buttons.

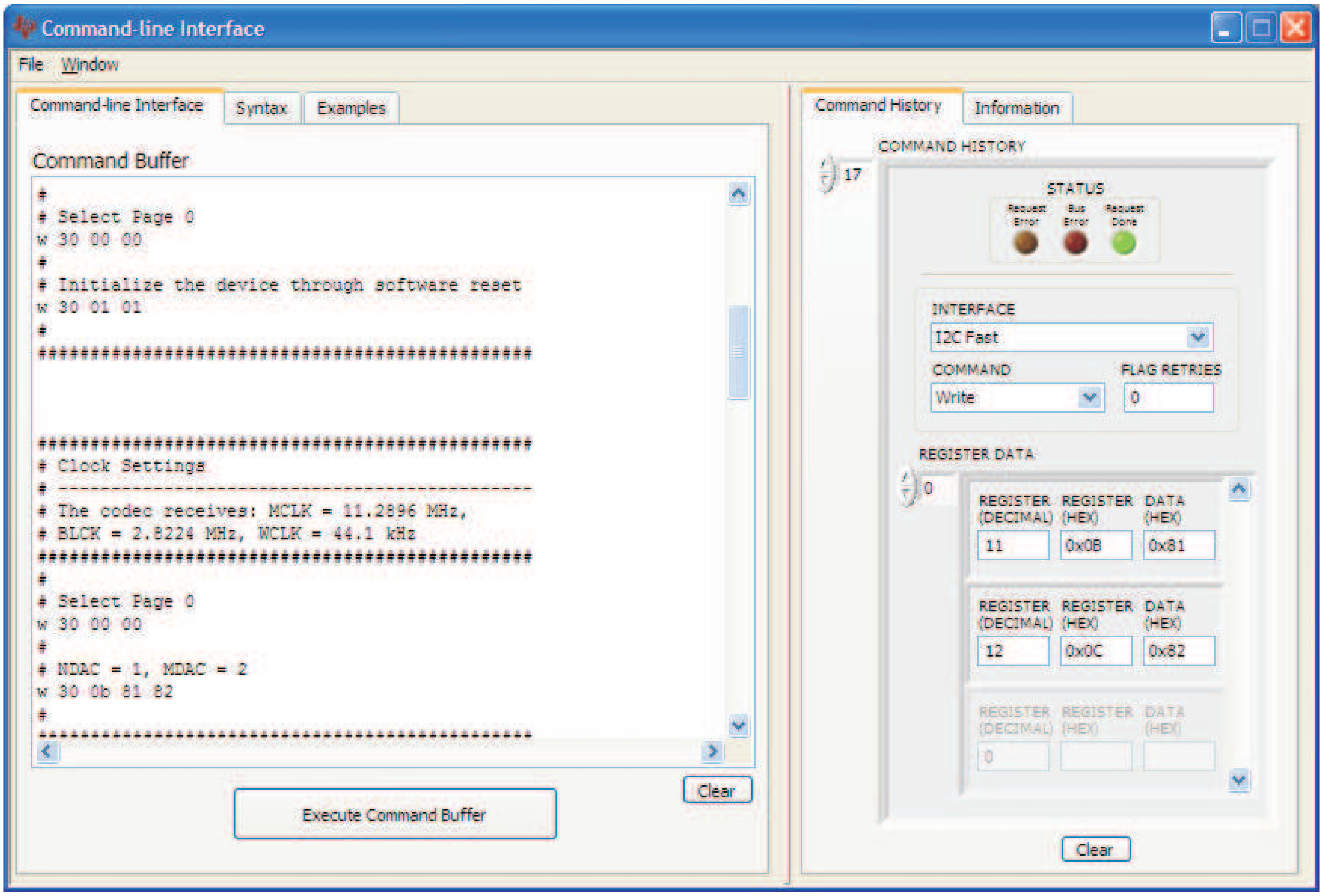


Figure 19. Command-line Interface Panel

Appendix A EVM Connector Descriptions

This appendix contains the connection details for each of the main connectors on the EVM.

A.1 Analog Interface Connectors

A.1.1 Analog Dual-Row Socket Details, J11 and J21

The TLV320AIC3254EVM has two analog dual-row sockets located at the bottom of the board. These sockets provide support to the EVM and connect the analog ground plane of the EVM to the USB-MODEVM analog ground. Consult Samtec at www.samtec.com or call 1-800-SAMTEC-9 for a variety of mating connector options. Table 3 summarizes the analog interface pinout for the TLV320AIC3254EVM.

Table 3. Analog Interface Pinout

PIN NUMBER	SIGNAL	DESCRIPTION
J11.1	NC	Not Connected
J11.2	NC	Not Connected
J11.3	NC	Not Connected
J11.4	NC	Not Connected
J11.5	NC	Not Connected
J11.6	NC	Not Connected
J11.7	NC	Not Connected
J11.8	NC	Not Connected
J11.9	AGND	Analog Ground
J11.10	NC	Not Connected
J11.11	AGND	Analog Ground
J11.12	NC	Not Connected
J11.13	AGND	Analog Ground
J11.14	NC	Not Connected
J11.15	NC	Not Connected
J11.16	NC	Not Connected
J11.17	AGND	Analog Ground
J11.18	NC	Not Connected
J11.19	AGND	Analog Ground
J11.20	NC	Not Connected
J21.1	NC	Not Connected
J21.2	NC	Not Connected
J21.3	NC	Not Connected
J21.4	NC	Not Connected
J21.5	NC	Not Connected
J21.6	NC	Not Connected
J21.7	NC	Not Connected
J21.8	NC	Not Connected
J21.9	AGND	Analog Ground
J21.10	NC	Not Connected
J21.11	AGND	Analog Ground
J21.12	NC	Not Connected
J21.13	AGND	Analog Ground
J21.14	NC	Not Connected
J21.15	NC	Not Connected
J21.16	NC	Not Connected
J21.17	AGND	Analog Ground
J21.18	NC	Not Connected
J21.19	AGND	Analog Ground

Table 3. Analog Interface Pinout (continued)

PIN NUMBER	SIGNAL	DESCRIPTION
J21.20	NC	Not Connected

A.1.2 Analog Screw Terminal and Audio Jack Details, J1 to J10

The analog inputs and outputs can be accessed through screw terminals or audio jacks.

Table 4 summarizes the screw terminals and audio jacks available on the TLV320AIC3254EVM.

Table 4. Alternate Analog Connectors

DESIGNATOR	PIN 1	PIN 2	PIN3	PIN4	PIN5
J1 (IN1)	AGND	IN1_L	IN1_R	NC	NC
J2 (IN1)	IN1_L	AGND	IN1_R		
J3 (IN2)	IN2_L	AGND	IN2_R		
J4 (EXT MIC IN)	IN3_L	AGND	IN3_R / NC		
J5 (MIC INPUT)	AGND	IN3_L	IN3_R / NC	IN3_L	IN3_R / NC
J6 (LINE OUT)	LOL	AGND	LOR		
J7 (LINE OUT)	AGND	LOL	LOR	NC	NC
J8 (HEADPHONE)	HPL	AGND	HPR		
J9 (HEADPHONE OUTPUT)	AGND	HPL	HPR	NC	NC
J10 (HEADPHONE TEST ONLY)	AGND	HPL	HPR	NC	NC

A.2 Digital Interface Connectors, P12/J12 and P22/J22

The TLV320AIC3254EVM is designed to easily interface with multiple control platforms. Samtec part numbers SSW-110-22-F-D-VS-K and TSM-110-01-T-DV-P provide a convenient 10-pin, dual-row header/socket combination at P12/J12 and P22/J22. These headers/sockets provide access to the digital control and serial data pins of the device. Consult Samtec at www.samtec.com or call 1-800- SAMTEC-9 for a variety of mating connector options. Table 5 summarizes the digital interface pinout for the TLV320AIC3254EVM.

Table 5. Digital Interface Pinout

PIN NUMBER	SIGNAL	DESCRIPTION
P12.1/J12.1	NC	Not Connected
P12.2/J12.2	NC	Not Connected
P12.3/J12.3	SCLK	SPI Serial Clock
P12.4/J12.4	DGND	Digital Ground
P12.5/J12.5	NC	Not Connected
P12.6/J12.6	NC	Not Connected
P12.7/J12.7	/SS	SPI Chip Select
P12.8/J12.8	NC	Not Connected
P12.9/J12.9	NC	Not Connected
P12.10/J12.10	DGND	Digital Ground
P12.11/J12.11	MOSI	SPI MOSI Slave Serial Data Input
P12.12/J12.12	NC	Not Connected
P12.13/J12.13	MISO	SPI MISO Slave Serial Data Output
P12.14/J12.14	$\overline{\text{RESET}}$	TAS1020B Reset
P12.15/J12.15	NC	Not Connected
P12.16/J12.16	SCL	I^2C Serial Clock
P12.17/J12.17	NC	Not Connected
P12.18/J12.18	DGND	Digital Ground
P12.19/J12.19	NC	Not Connected
P12.20/J12.20	SDA	I^2C Serial Data Input/Output
P22.1/J22.1	NC	Not Connected
P22.2/J22.2	NC	Not Connected
P22.3/J22.3	BCLK	Audio Serial Data Bus Bit Clock (Input/Output)
P22.4/J22.4	DGND	Digital Ground
P22.5/J22.5	NC	Not Connected
P22.6/J22.6	NC	Not Connected
P22.7/J22.7	WCLK	Audio Serial Data Bus Word Clock (Input/Output)
P22.8/J22.8	NC	Not Connected
P22.9/J22.9	NC	Not Connected
P22.10/J22.10	DGND	Digital Ground
P22.11/J22.11	DIN	Audio Serial Data Bus Data Input (Input)
P22.12/J22.12	NC	Not Connected
P22.13/J22.13	DOUT	Audio Serial Data Bus Data Output (Output)
P22.14/J22.14	NC	Not Connected
P22.15/J22.15	NC	Not Connected
P22.16/J22.16	NC	Not Connected
P22.17/J22.17	MCLK	Master Clock Input
P22.18/J22.18	DGND	Digital Ground
P22.19/J22.19	NC	Not Connected
P22.20/J22.20	NC	Not Connected

Note that P22/J22 comprises the signals needed for an I2S™ serial digital audio interface; the control interface (I2C™ and RESET) signals are routed to P12/J12.

A.3 Power Supply Connector Pin Header, P23/J23

P23/J23 provides connection to the common power bus for the TLV320AIC3254EVM. Power is supplied on the pins listed in Table 6.

Table 6. Power Supply Pin Out

SIGNAL	PIN NUMBER		SIGNAL
NC	P23.1/J23.1	P23.2/J23.2	NC
+5VA	P23.3/J23.3	P23.4/J23.4	NC
DGND	P23.5/J23.5	P23.6/J23.6	AGND
+1.8VD	P23.7/J23.7	P23.8/J23.8	NC
+3.3VD	P23.9/J23.9	P23.10/J23.10	+5VD

The TLV320AIC3254EVM-K motherboard (the USB-MODEVM Interface board) supplies power to P23/J23 of the TLV320AIC3254EVM. Power for the motherboard is supplied either through its USB connection or via terminal blocks on that board.

Appendix B TLV320AIC3254EVM Schematic

The schematic diagram for the TLV320AIC3254EVM is provided as a reference.

AIC3204_54_RHB
AIC3204_54_RHB.SCH

Daughtercard_Interface
Daughtercard_Interface.SCH

Revision History		
REV	ECN Number	Approved

TYPICAL INPUT CONFIGURATIONS (IN3_L & IN3_R)

		EXTERNAL ELECTRET MICROPHONE CONFIGURATION				JACK LINE INPUT CONFIGURATION				ONBOARD ELECTRET MICROPHONE CONFIGURATION	
INPUT TYPE		GND L	GND L L	GND R L	+ 1 2 3 -	GND L	GND L L	GND R L	+ 1 2 3 -		
MODE		SINGLE-ENDED MONO	SINGLE-ENDED MONO	SINGLE-ENDED STEREO	DIFFERENTIAL MONO	SINGLE-ENDED MONO	SINGLE-ENDED MONO	SINGLE-ENDED STEREO	DIFFERENTIAL MONO	SINGLE-ENDED MONO	DIFFERENTIAL MONO
CODEC INPUTS		IN3_L	IN3_L	IN3_L IN3_R	IN3_L IN3_R	IN3_L	IN3_L IN3_R	IN3_L IN3_R	IN3_L IN3_R	IN3_L	IN3_L IN3_R
ONBOARD MIC JUMPERS	W2	OUT	OUT	OUT	OUT	OUT	OUT	OUT	OUT	IN	IN
	W3	OUT	OUT	OUT	OUT	OUT	OUT	OUT	OUT	IN	IN
INPUT CONFIG JUMPER SETTINGS	W4	OUT	OUT	IN	OUT	OUT	OUT	OUT	OUT	OUT	OUT
	W5	IN	IN	IN	IN	OUT	OUT	OUT	OUT	IN	IN
	W6	OUT	OUT	OUT	IN	N/A	N/A	N/A	N/A	OUT	IN
	W7	OUT	OUT	IN	IN	OUT	IN	IN	IN	IN	IN
	W8	1-2	1-2	OUT	2-3	1-2	OUT	OUT	OUT	1-2	2-3
DESCRIPTION		Microphone bias provided on tip. IN3_R AC coupled to GND. Ring not connected to circuit.	Microphone bias provided on tip. IN3_R AC coupled to GND. Ring not connected to circuit.	Stereo electret microphones. Bias provided to both inputs. Ring is connected to IN3_R.	Differential electret microphone. IN3_L & IN3_R configured as differential pair.	IN3_R is AC-coupled to AVSS.	Ring is connected to IN3_R.	Ring is connected to IN3_R.	Differential line in. IN3_L & IN3_R configured as differential pair.	Single Ended - Mono.	Differential - Mono.

TEXAS INSTRUMENTS

DATA ACQUISITION PRODUCTS
HIGH PERFORMANCE ANALOG DIVISION
SEMICONDUCTOR GROUP

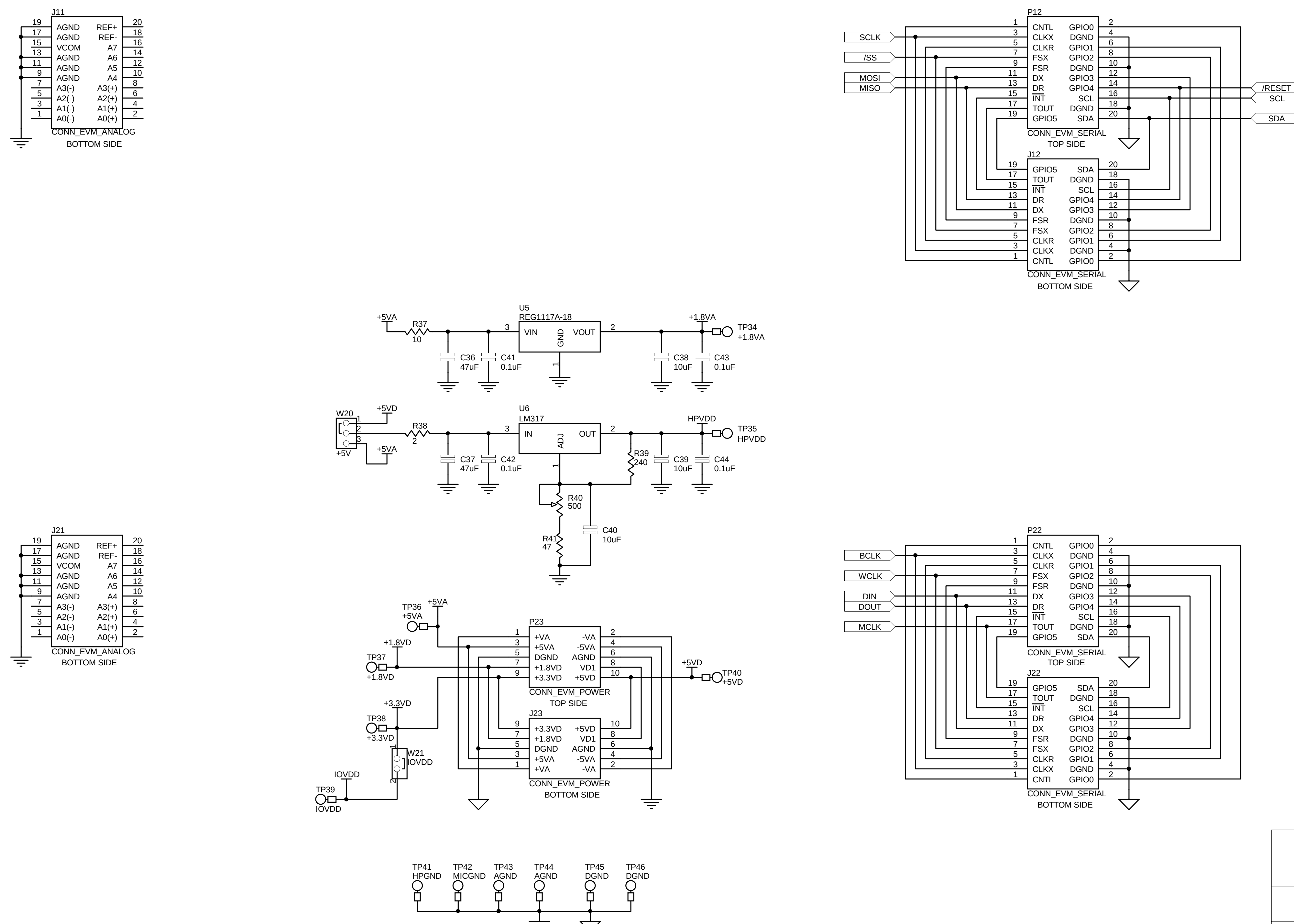
12500 T.I. Boulevard, Dallas, Texas 75243 USA

ENGINEER **Mike Tsecouras**
DRAWN BY **Steve Leggio**
DOCUMENT CONTROL NO. **N/A**
SHEET **1** OF **3**   FILE

TITLE **TLV320AIC3204_54_RHB_EVM**

SIZE **A**   DATE **20-Aug-2008**   REV **A**

REVISION HISTORY		
REV	ENGINEERING CHANGE NUMBER	APPROVED

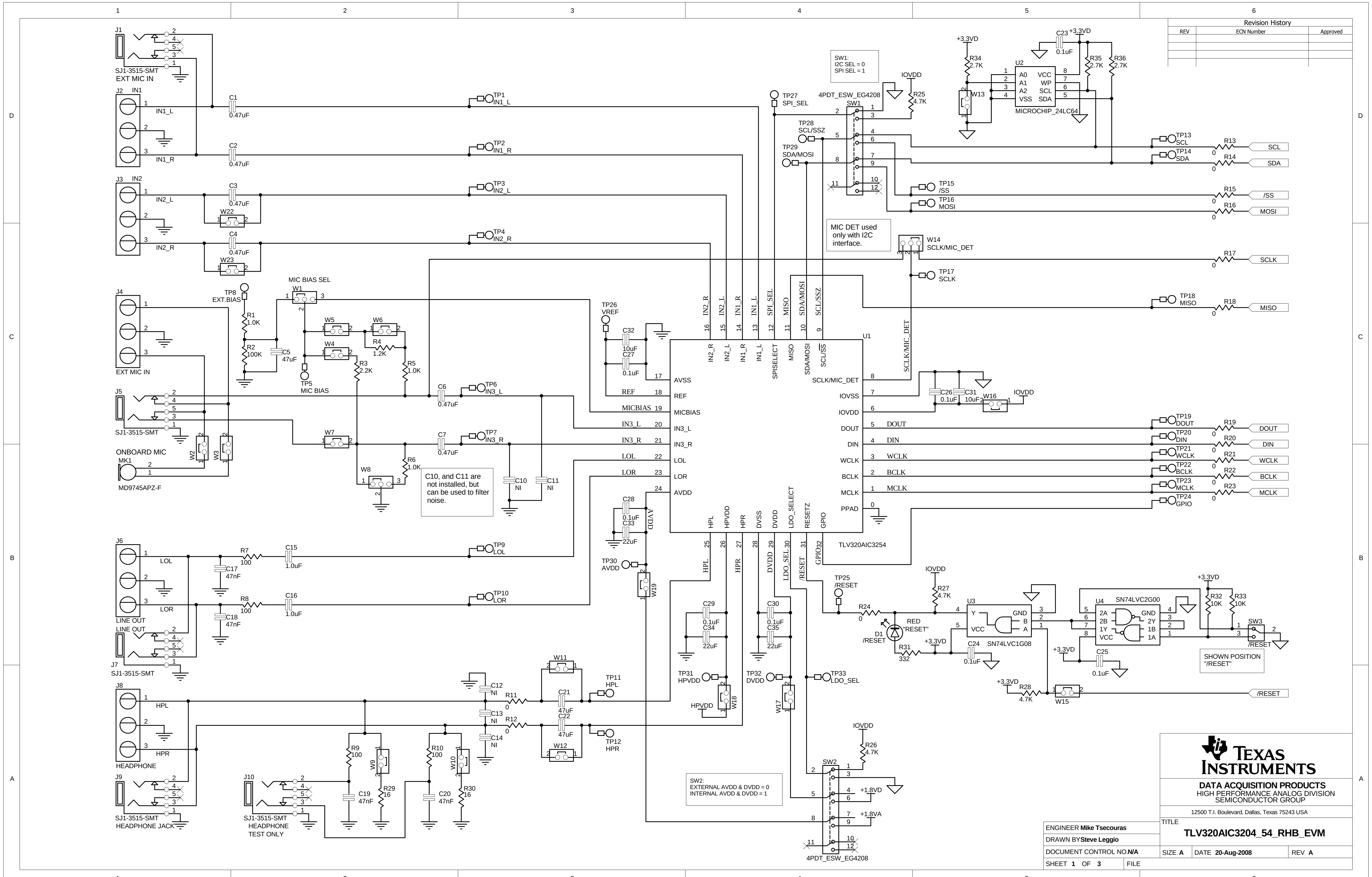


TEXAS INSTRUMENTS

DATA ACQUISITION PRODUCTS
HIGH-PERFORMANCE ANALOG DIVISION
SEMICONDUCTOR GROUP

12500 T.I. Boulevard, Dallas, Texas 75243 USA

ENGINEER **MIKE TSECOURAS**	TITLE **TLV320AIC3204_54_RHB_EVM**
DRAWN BY **STEVE LEGGIO**	
DOCUMENT CONTROL NO. **N/A**	SIZE **B** DATE **20-Aug-2008** REV **A**
SHEET **2** OF **3**	FILE


Revision History
REV
ECN Number
Approved
SW1:
I2C SEL = 0
SPI SEL = 1
MIC DET used only with I2C interface.
C10, and C11 are not installed, but can be used to filter noise.
SW2:
EXTERNAL AVDD & DVDD = 0
INTERNAL AVDD & DVDD = 1
SHOWN POSITION "/RESET"
TLV320AIC3254
MICROCHIP_24LC64
SN74LVC1G08
SN74LVC2G00
4PDT_ESW_EG4208
SJ1-3515-SMT
EXT MIC IN
LINE OUT
HEADPHONE
HEADPHONE JACK
HEADPHONE TEST ONLY
ONBOARD MIC
MD9745APZ-F
MIC BIAS SEL
RED "RESET"
TEXAS INSTRUMENTS
DATA ACQUISITION PRODUCTS
HIGH PERFORMANCE ANALOG DIVISION
SEMICONDUCTOR GROUP
12500 T.I. Boulevard, Dallas, Texas 75243 USA
ENGINEER Mike Tsecouras
DRAWN BY Steve Leggio
DOCUMENT CONTROL NO. N/A
SHEET 1 OF 3
FILE
TITLE
TLV320AIC3204_54_RHB_EVM
SIZE A
DATE 20-Aug-2008
REV A

Appendix C TLV320AIC3254EVM Layout Views

C.1 Layout Views

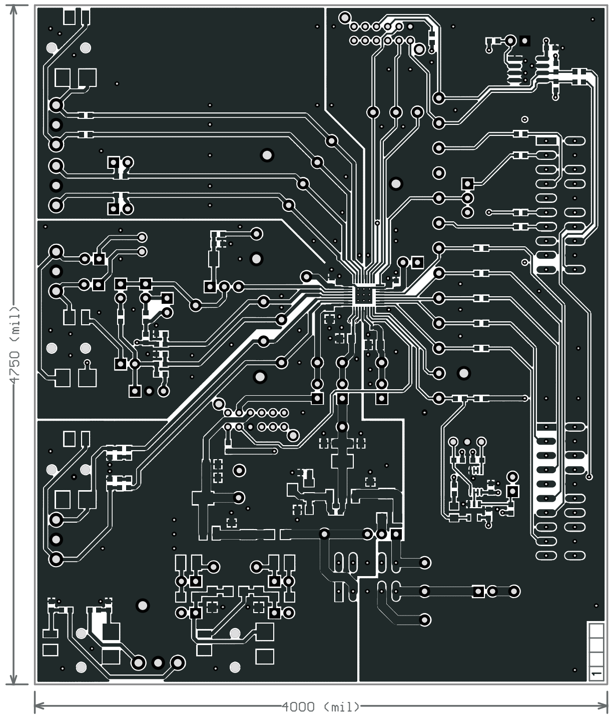


Figure 20. Top Layer

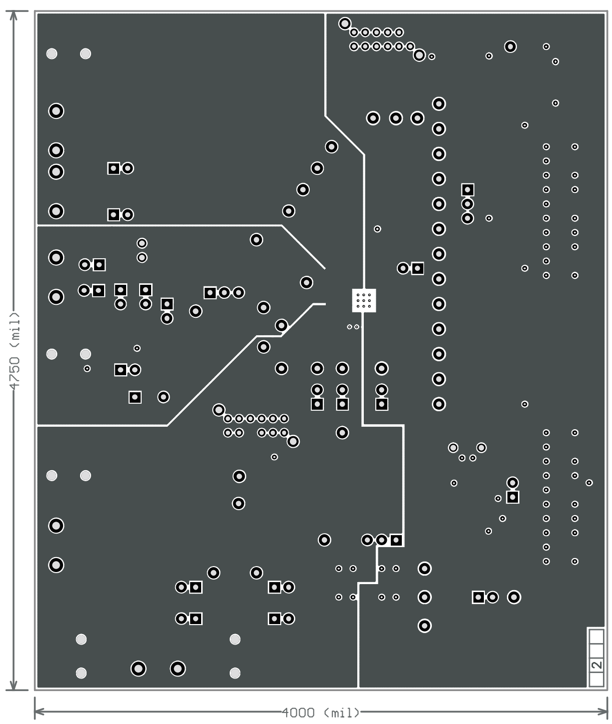


Figure 21. Mid-Layer 1

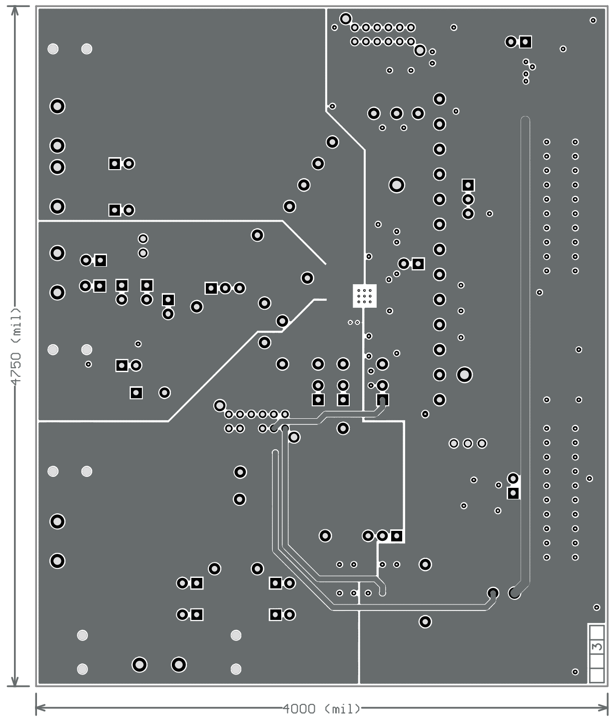


Figure 22. Mid-Layer 2

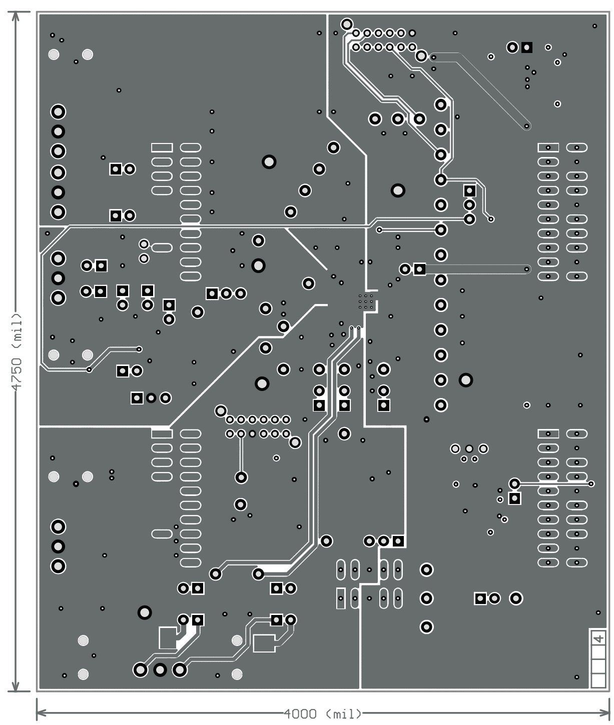


Figure 23. Bottom Layer

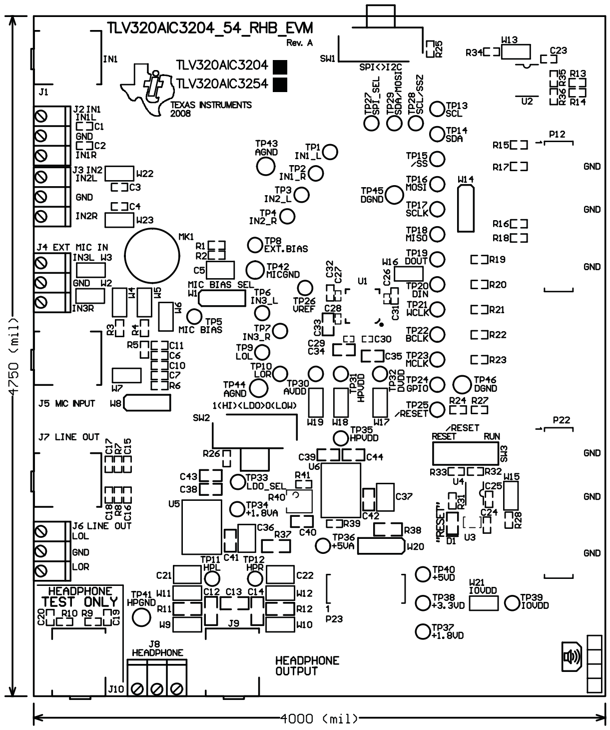


Figure 24. Top Overlay

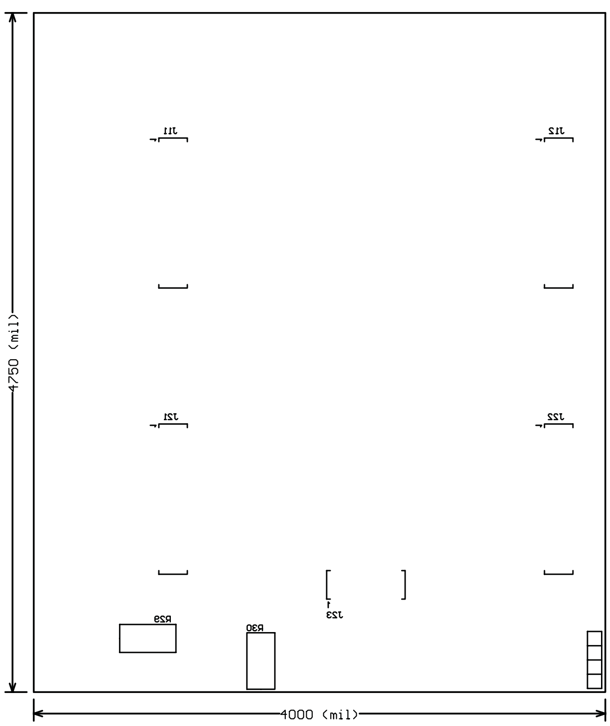


Figure 25. Bottom Overlay

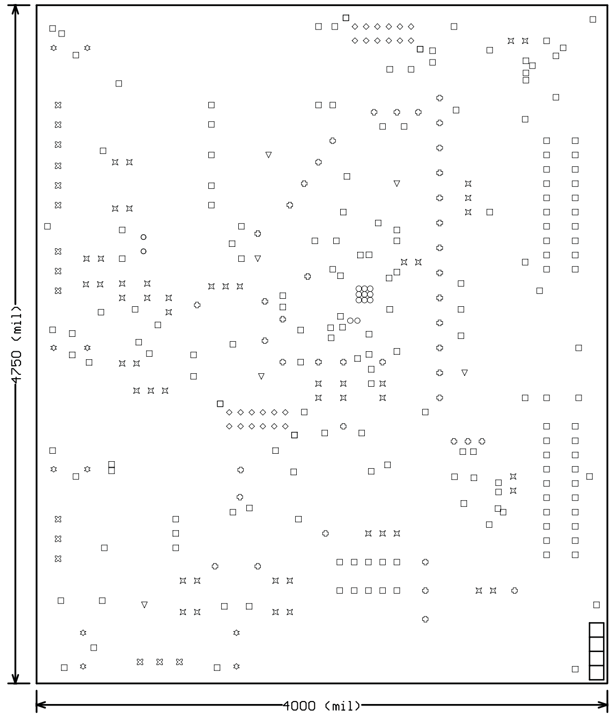


Figure 26. Drill Drawing

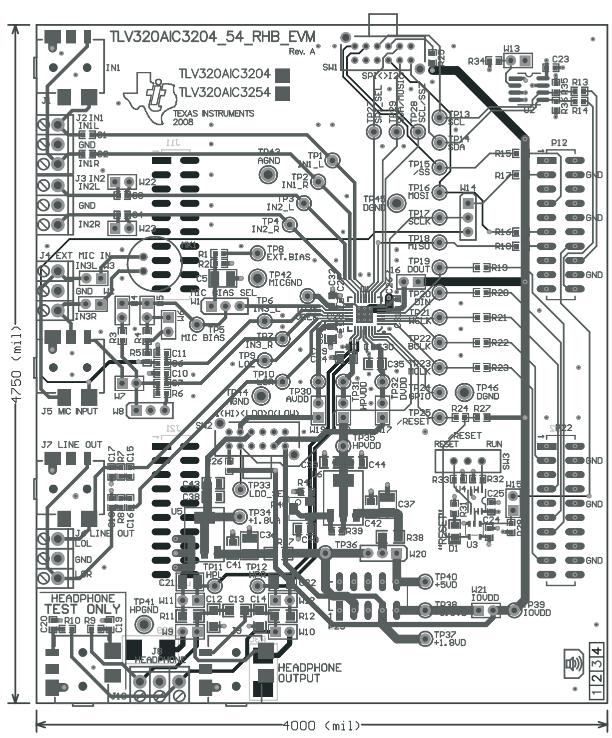


Figure 27. Composite

Appendix D TLV320AIC3254EVM Bill of Materials

The complete bill of materials for the TLV320AIC3254EVM is provided as a reference.

Table 7. TLV320AIC3254EVM Bill of Materials

PCB					
Qty	**Value**	**Ref Des**	**Description**	**Vendor**	**Part number**
1		N/A	TLV320AIC3204_54_RHB_EVM_Rev A (PCB)	Texas Instruments	
RESISTORS					
Qty	**Value**	**Ref Des**	**Description**	**Vendor**	**Part number**
2	0	R11, R12	RES ZERO OHM 1/4W 5% 1206 S.D.	Panasonic	EJ-8GEY0R00V
12	0	R13, R14, R15, R16, R17, R18, R19, R20, R21, R22, R23, R24	RES ZERO OHM 1/10W 5% 0603 S.D.	Panasonic	EJ-3GEY0R00V
1	2	R38	RESISTOR 2.0 OHM 1/4W 5% 1206	Panasonic	EJ-8GEYJ2R0V
1	10	R37	RES 10 OHM 1/4W 5% 1206 S.D.	Panasonic	EJ-8GEYJ100V
2	16	R29, R30	RES 16 OHM 1W 5% 2512 S.D.	Panasonic	EJ-1TYJ160U
1	47	R41	RES 47 OHM 1/10W 5% 0603 S.D.	Panasonic	EJ-3GEYJ470V
4	100	R7, R8, R9, R10	RES 100 OHM 1/10W 1% 0603 S.D.	Panasonic	EJ-3EKF1000V
1	240	R39	RES 240 OHM 1/10W 5% 0603 S.D.	Panasonic	EJ-3GEYJ241V
1	332	R31	RES 332 OHM 1/10W 1% 0603 SMD	Panasonic	ERJ-3EKF3320V
1	500	R40	TRIMPOT 500 OHM 4MM TOP ADJ SMD	Bourns Inc.	3214W-1-501E
3	1.0K	R1, R5, R6	RES 1.00K OHM 1/10W 1% 0603 SMD	Panasonic	ERJ-3EKF1001V
1	1.2K	R4	RES 1.20K OHM 1/10W 1% 0603 SMD	Panasonic	ERJ-3EKF1201V
1	2.2K	R3	RES 2.2K OHM 1/10W 5% 0603 SMD	Panasonic	ERJ-3GEYJ222V
3	2.7K	R34, R35, R36	RES 2.7K OHM 1/10W 5% 0603 SMD	Panasonic	ERJ-3GEYJ272V
4	4.7K	R25, R26, R27, R28	RES 4.7K OHM 1/10W 5% 0603 SMD	Panasonic	ERJ-3GEYJ472V
2	10K	R32, R33	RES 10K OHM 1/10W 5% 0603 SMD	Panasonic	ERJ-3GEYJ103V
1	100K	R2	RES 100K OHM 1/10W 1% 0603 SMD	Panasonic	ERJ-3EKF1003V
CAPACITORS					
Qty	**Value**	**Ref Des**	**Description**	**Vendor**	**Part number**
4	47000pF	C17, C18, C19, C20	CAP CER 47000PF 50V X7R 10% 0603	TDK Corporation	C1608X7R1H473K
5	0.1uF	C26, C27, C28, C29, C30	CAP CER .10UF 6.3V X5R 10% 0402	TDK Corporation	C1005X5R0J104K
3	0.1uF	C23, C24, C25	CAP CER .1UF 25V X7R 0603	TDK Corporation	C1608X7R1E104K
4	0.1uF	C41, C42, C43, C44	CAP .1UF 25V CERAMIC X7R 0805	Panasonic	ECJ-2VB1E104K
6	0.47uF	C1, C2, C3, C4, C6, C7	CAP CER .47UF 10V X5R 10% 0603	Panasonic	C1608X5R1A474K
2	1.0uF	C15, C16	CAP CERAMIC 1UF 10V X5R 0603	Panasonic	ECJ-BVB1A105K
2	10uF	C31, C32	CAP CERAMIC 10UF 6.3V X5R 0603	Panasonic	ECJ-1VB0J106M

Table 7. TLV320AIC3254EVM Bill of Materials (continued)

3	10uF	C38, C39, C40	CAP CERAMIC 10UF 10V X5R 0805	Panasonic	ECJ-2FB1A106K
3	22uF	C33, C34, C35	CAP CER 22UF 6.3V X5R 20% 0805	TDK Corporation	C2012X5R0J226M
5	47uF	C5, C21, C22, C36, C37	CAP CER 47UF 10V X5R 1210	Murata	GRM32ER61A476KE20L
2	no value - not installed	C10, C11	CAP 0603	N/A	N/A
3	no value - not installed	C12, C13, C14	CAP 1206	N/A	N/A
INTEGRATED CIRCUITS					
Qty	**Value**	**Ref Des**	**Description**	**Vendor**	**Part number**
1		U1	Audio Codec	Texas Instruments	TLV320AIC3254IRHB
1		U2	IC SERIAL EEPROM 64K 2.5V 8-SOIC	MicroChip	24LC64-I/SN
1		U3	Single 2-Input Positive-AND Gate	Texas Instruments	SN74LVC1G08DBVR
1		U4	Dual 2-Input Positive-NAND Gate	Texas Instruments	SN74LVC2G00DCTR
1		U5	Single Output LDO, 1.0A, Fixed(1.8V)	Texas Instruments	REG1117A-1.8
1		U6	3-Pin 1.5-A Adjustable Voltage Regulator	Texas Instruments	LM317DCY
MISCELLANEOUS ITEMS					
Qty	**Value**	**Ref Des**	**Description**	**Vendor**	**Part number**
1		D1	LED THIN 635NM RED DIFF 0805 SMD	Lumex	SML-LXT0805IW-TR
1		MK1	Omnidirectional Microphone Cartridge	Knowles Acoustics	MD9745APZ-F
			or alternate	Knowles Acoustics	MD9745APA-1
2		SW1-SW2	SWITCH SLIDE 4PDT 30V RT ANGLE	E-Switch	EG4208
1		SW3	SWITCH SLIDE SPDT 30V.2A PC MNT	E-Switch	EG1218
5		J2, J3, J4, J6, J8	Screw Terminal Block, 3 Position	On Shore Technology	ED555/3DS
5		J1, J5, J7, J9, J10	3.5mm Audio Jack, T-R-S, SMD	CUI Inc.	SJ1-3515-SMT
			or alternate	KobiConn	161-3335-E
11	not installed	TP26, TP30, TP31, TP32, TP34, TP35, TP36, TP37, TP38, TP39, TP40	TEST POINT PC MINI .040"D RED	Keystone Electronics	5000
29	not installed	TP1, TP2, TP3, TP4, TP5, TP6, TP7, TP8, TP9, TP10, TP11, TP12, TP13, TP14, TP15, TP16, TP17, TP18, TP19, TP20, TP21, TP22, TP23, TP24, TP25, TP27, TP28, TP29, TP33	TEST POINT PC MINI .040"D WHITE	Keystone Electronics	5002
6		TP41, TP42, TP43, TP44, TP45, TP46	TEST POINT PC MULTI PURPOSE BLK	Keystone Electronics	5011
2		P12, P22	20 Pin SMT Plug Header	Samtec	TSM-110-01-L-DV-P
4		J11, J12, J21, J22	20 pin SMT Socket Header	Samtec	SSW-110-22-F-D-VS-K
1		P23	10 Pin SMT Plug Header	Samtec	TSM-105-01-L-DV-P

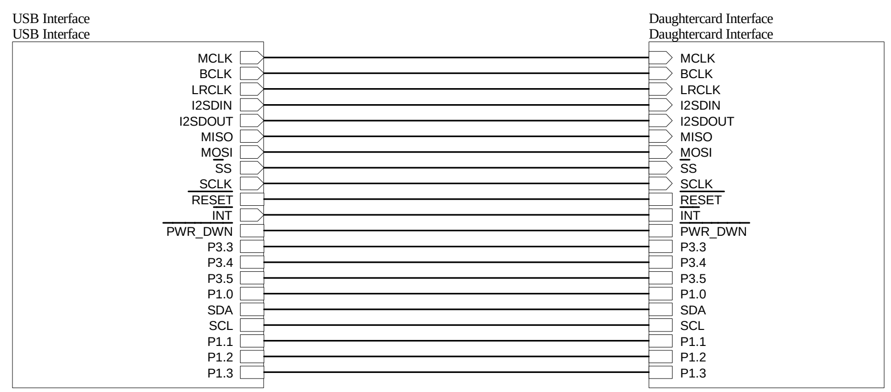
Table 7. TLV320AIC3254EVM Bill of Materials (continued)

1		J23	10 pin SMT Socket Header	Samtec	SSW-105-22-F-D-VS-K
14		W2, W3, W4, W5, W6, W7, W9, W10, W11, W12, W13, W15, W22, W23	2 Pin Thru-hole Plug Header (Jumper), 0 .1" spacing	Samtec	TSW-102-07-L-S
5		W16, W17, W18, W19, W21	Bus Wire (18-22 Gauge)		
4		W1, W8, W14, W20	3 Position Jumper , 0 .1" spacing	Samtec	TSW-103-07-L-S
	Installed per test procedure.	Installed per test procedure.	Header Shorting Block	Samtec	SNT-100-BK-T
ATTENTION: All components must be Rhos compliant. Some part numbers may be either leaded or Rhos. Verify that purchased components are Rhos compliant.					

Appendix E USB-MODEVM Schematic

The schematic diagram for USB-MODEVM Interface Board is provided as a reference.

REVISION HISTORY		
REV	ENGINEERING CHANGE NUMBER	APPROVED



TEXAS INSTRUMENTS

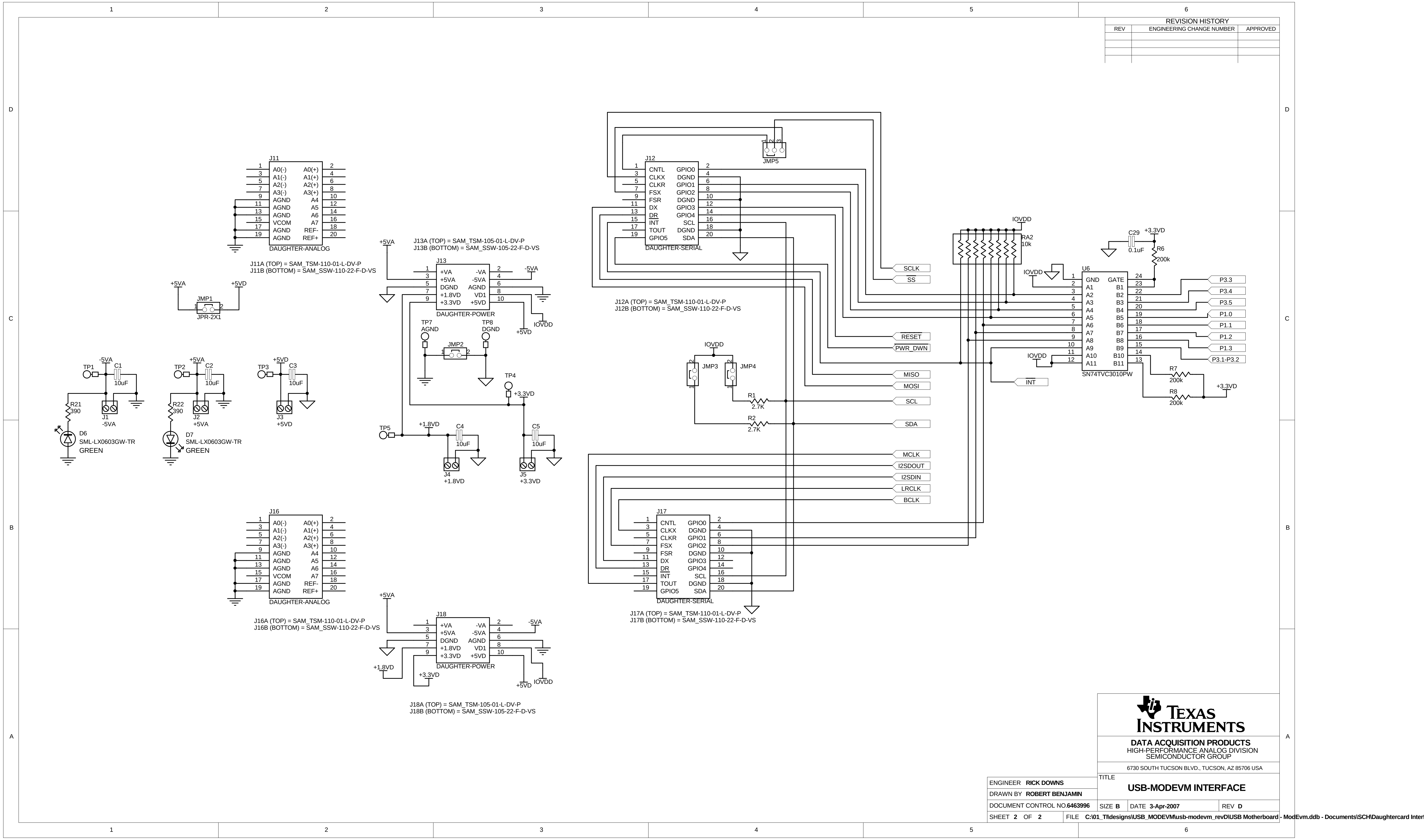
DATA ACQUISITION PRODUCTS
HIGH-PERFORMANCE ANALOG DIVISION
SEMICONDUCTOR GROUP

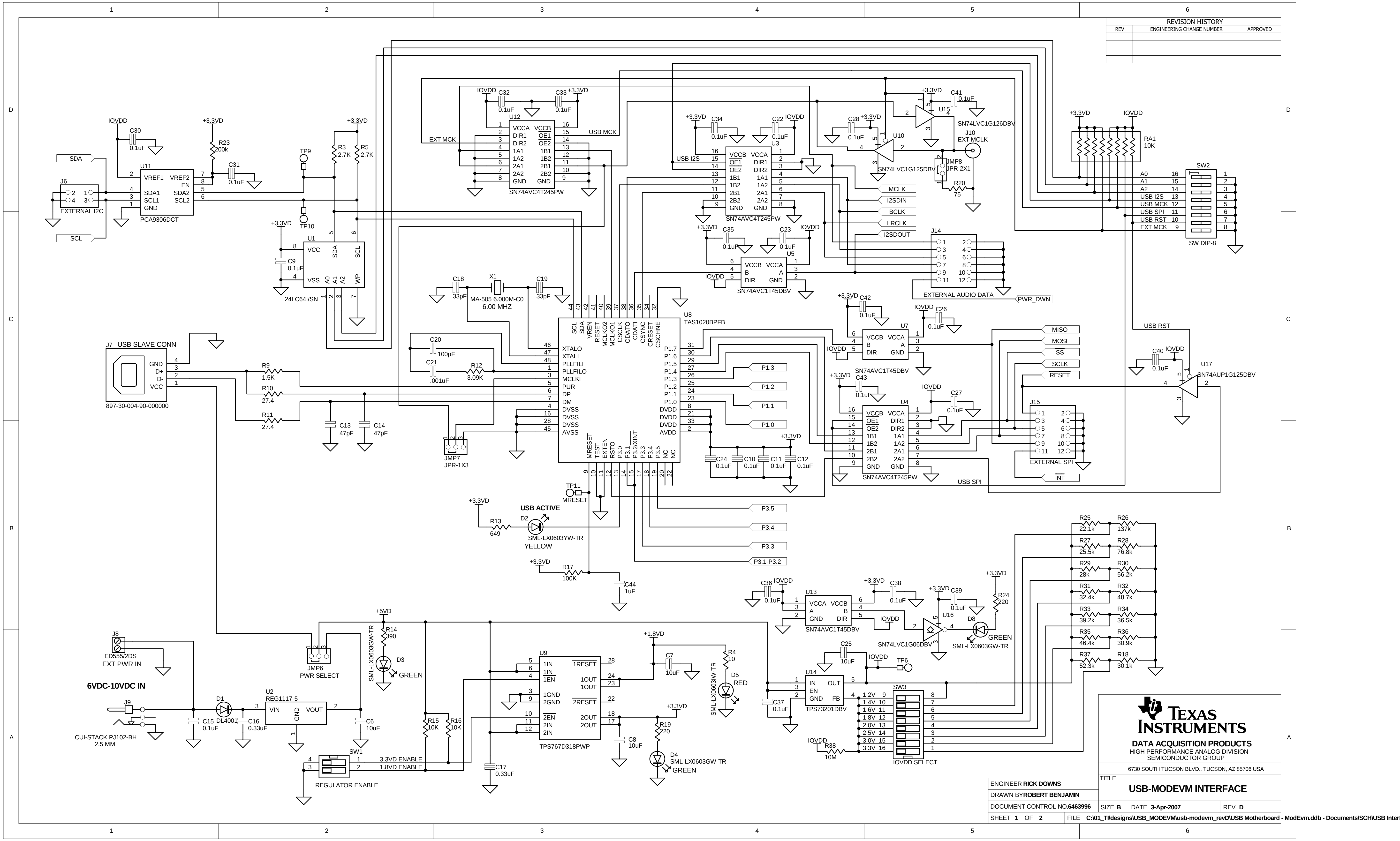
6730 SOUTH TUCSON BLVD., TUCSON, AZ 85706 USA

ENGINEER **FRYE D. ZERKETTS**
DRAWN BY **I. C. SPOTTS**
DOCUMENT CONTROL NO. **1234567**
SHEET **1** OF **1**

TITLE
untitled

SIZE **B** DATE **dd MMM yyyy** REV **A**
FILE **???**


REVISION HISTORY
REV | ENGINEERING CHANGE NUMBER | APPROVED
J11 DAUGHTER-ANALOG
J11A (TOP) = SAM_TSM-110-01-L-DV-P
J11B (BOTTOM) = SAM_SSW-110-22-F-D-VS
J13A (TOP) = SAM_TSM-105-01-L-DV-P
J13B (BOTTOM) = SAM_SSW-105-22-F-D-VS
J13 DAUGHTER-POWER
J12 DAUGHTER-SERIAL
J12A (TOP) = SAM_TSM-110-01-L-DV-P
J12B (BOTTOM) = SAM_SSW-110-22-F-D-VS
JMP5
RA2 10k
U6 SN74TVC3010PW
C29 0.1uF
R6 200k
R7 200k
R8 200k
SCLK
SS
RESET
PWR_DWN
MISO
MOSI
SCL
SDA
MCLK
I2SDOUT
I2SDIN
LRCLK
BCLK
INT
P3.3
P3.4
P3.5
P1.0
P1.1
P1.2
P1.3
P3.1-P3.2
JMP1 JPR-2X1
JMP2
JMP3
JMP4
R1 2.7K
R2 2.7K
TP1 TP2 TP3 TP4 TP5
TP7 AGND
TP8 DGND
R21 390
R22 390
D6 SML-LX0603GW-TR GREEN
D7 SML-LX0603GW-TR GREEN
C1 10uF
C2 10uF
C3 10uF
C4 10uF
C5 10uF
J1 -5VA
J2 +5VA
J3 +5VD
J4 +1.8VD
J5 +3.3VD
J16 DAUGHTER-ANALOG
J16A (TOP) = SAM_TSM-110-01-L-DV-P
J16B (BOTTOM) = SAM_SSW-110-22-F-D-VS
J17 DAUGHTER-SERIAL
J17A (TOP) = SAM_TSM-110-01-L-DV-P
J17B (BOTTOM) = SAM_SSW-110-22-F-D-VS
J18 DAUGHTER-POWER
J18A (TOP) = SAM_TSM-105-01-L-DV-P
J18B (BOTTOM) = SAM_SSW-105-22-F-D-VS
TEXAS INSTRUMENTS
DATA ACQUISITION PRODUCTS
HIGH-PERFORMANCE ANALOG DIVISION
SEMICONDUCTOR GROUP
6730 SOUTH TUCSON BLVD., TUCSON, AZ 85706 USA
ENGINEER RICK DOWNS
DRAWN BY ROBERT BENJAMIN
DOCUMENT CONTROL NO. 6463996
SHEET 2 OF 2
TITLE USB-MODEVM INTERFACE
SIZE B
DATE 3-Apr-2007
REV D
FILE C:\01_TIdesigns\USB_MODEVM\usb-modevm_revD\USB Motherboard - ModEvm.ddb - Documents\SCH\Daughtercard Interface


REVISION HISTORY
REV
ENGINEERING CHANGE NUMBER
APPROVED
EXTERNAL I2C
PCA9306DCT
24LC64I/SN
SN74AVC4T245PW
SN74AVC1T45DBV
SN74LVC1G126DBV
SN74LVC1G125DBV
J10 EXT MCLK
EXTERNAL AUDIO DATA
SW DIP-8
J7 USB SLAVE CONN
897-30-004-90-000000
MA-505 6.000M-C0
6.00 MHZ
U8 TAS1020BPFB
SN74AUP1G125DBV
EXTERNAL SPI
USB ACTIVE
SML-LX0603YW-TR
YELLOW
EXT PWR IN
6VDC-10VDC IN
CUI-STACK PJ102-BH
2.5 MM
REG1117-5
JMP6 PWR SELECT
SW1 REGULATOR ENABLE
3.3VD ENABLE
1.8VD ENABLE
TPS767D318PWP
TPS73201DBV
SN74LVC1G06DBV
IOVDD SELECT
SML-LX0603GW-TR
GREEN
RED
TEXAS INSTRUMENTS
DATA ACQUISITION PRODUCTS
HIGH PERFORMANCE ANALOG DIVISION
SEMICONDUCTOR GROUP
6730 SOUTH TUCSON BLVD., TUCSON, AZ 85706 USA
ENGINEER RICK DOWNS
DRAWN BY ROBERT BENJAMIN
DOCUMENT CONTROL NO. 6463996
SHEET 1 OF 2
TITLE
USB-MODEVM INTERFACE
SIZE B
DATE 3-Apr-2007
REV D
FILE C:\01_TI\designs\USB_MODEVM\usb-modevm_revD\USB Motherboard - ModEvm.ddb - Documents\SCH\USB Interface

Appendix F USB-MODEVM Bill of Materials

The complete bill of materials for USB-MODEVM Interface Board is provided as a reference.

Table 8. USB-MODEVM Bill of Materials

Designators	Description	Manufacturer	Mfg. Part Number
R4	10Ω 1/10W 5% Chip Resistor	Panasonic	ERJ-3GEYJ1300V
R10, R11	27.4Ω 1/16W 1% Chip Resistor	Panasonic	ERJ-3EKF27R4V
R20	75Ω 1/4W 1% Chip Resistor	Panasonic	ERJ-14NF75R0U
R19	220Ω 1/10W 5% Chip Resistor	Panasonic	ERJ-3GEYJ221V
R14, R21, R22	390Ω 1/10W 5% Chip Resistor	Panasonic	ERJ-3GEYJ391V
R13	649Ω 1/16W 1% Chip Resistor	Panasonic	ERJ-3EKF6490V
R9	1.5KΩ 1/10W 5% Chip Resistor	Panasonic	ERJ-3GEYJ1352V
R1–R3, R5–R8	2.7KΩ 1/10W 5% Chip Resistor	Panasonic	ERJ-3GEYJ272V
R12	3.09KΩ 1/16W 1% Chip Resistor	Panasonic	ERJ-3EKF3091V
R15, R16	10KΩ 1/10W 5% Chip Resistor	Panasonic	ERJ-3GEYJ1303V
R17, R18	100kΩ 1/10W 5%Chip Resistor	Panasonic	ERJ-3GEYJ1304V
RA1	10KΩ 1/8W Octal Isolated Resistor Array	CTS Corporation	742C163103JTR
C18, C19	33pF 50V Ceramic Chip Capacitor, ±5%, NPO	TDK	C1608C0G1H330J
C13, C14	47pF 50V Ceramic Chip Capacitor, ±5%, NPO	TDK	C1608C0G1H470J
C20	100pF 50V Ceramic Chip Capacitor, ±5%, NPO	TDK	C1608C0G1H101J
C21	1000pF 50V Ceramic Chip Capacitor, ±5%, NPO	TDK	C1608C0G1H102J
C15	0.1µF 16V Ceramic Chip Capacitor, ±10%, X7R	TDK	C1608X7R1C104K
C16, C17	0.33µF 16V Ceramic Chip Capacitor, ±20%, Y5V	TDK	C1608X5R1C334K
C9–C12, C22–C28	1µF 6.3V Ceramic Chip Capacitor, ±10%, X5R	TDK	C1608X5R0J1305K
C1–C8	10µF 6.3V Ceramic Chip Capacitor, ±10%, X5R	TDK	C3216X5R0J1306K
D1	50V, 1A, Diode MELF SMD	Micro Commercial Components	DL4001
D2	Yellow Light Emitting Diode	Lumex	SML-LX0603YW-TR
D3– D7	Green Light Emitting Diode	Lumex	SML-LX0603GW-TR
D5	Red Light Emitting Diode	Lumex	SML-LX0603IW-TR
Q1, Q2	N-Channel MOSFET	Zetex	ZXMN6A07F
X1	6MHz Crystal SMD	Epson	MA-505 6.000M-C0
U8	USB Streaming Controller	Texas Instruments	TAS1020BPFB
U2	5V LDO Regulator	Texas Instruments	REG1117-5
U9	3.3V/1.8V Dual Output LDO Regulator	Texas Instruments	TPS767D318PWP
U3, U4	Quad, 3-State Buffers	Texas Instruments	SN74LVC125APW
U5–U7	Single IC Buffer Driver with Open Drain o/p	Texas Instruments	SN74LVC1G07DBVR
U10	Single 3-State Buffer	Texas Instruments	SN74LVC1G125DBVR
U1	64K 2-Wire Serial EEPROM I^2C	Microchip	24LC64I/SN
	USB-MODEVM PCB	Texas Instruments	6463995
TP1–TP6, TP9–TP11	Miniature test point terminal	Keystone Electronics	5000
TP7, TP8	Multipurpose test point terminal	Keystone Electronics	5011
J7	USB Type B Slave Connector Thru-Hole	Mill-Max	897-30-004-90-000000
J13, J2–J5, J8	2-position terminal block	On Shore Technology	ED555/2DS
J9	2.5mm power connector	CUI Stack	PJ-102B
J130	BNC connector, female, PC mount	AMP/Tyco	414305-1
J131A, J132A, J21A, J22A	20-pin SMT plug	Samtec	TSM-110-01-L-DV-P
J131B, J132B, J21B, J22B	20-pin SMT socket	Samtec	SSW-110-22-F-D-VS-K
J133A, J23A	10-pin SMT plug	Samtec	TSM-105-01-L-DV-P
J133B, J23B	10-pin SMT socket	Samtec	SSW-105-22-F-D-VS-K
J6	4-pin double row header (2x2) 0.1"	Samtec	TSW-102-07-L-D
J134, J135	12-pin double row header (2x6) 0.1"	Samtec	TSW-106-07-L-D
JMP1–JMP4	2-position jumper, 0.1" spacing	Samtec	TSW-102-07-L-S

Table 8. USB-MODEVM Bill of Materials (continued)

Designators	Description	Manufacturer	Mfg. Part Number
JMP8–JMP14	2-position jumper, 0.1" spacing	Samtec	TSW-102-07-L-S
JMP5, JMP6	3-position jumper, 0.1" spacing	Samtec	TSW-103-07-L-S
JMP7	3-position dual row jumper, 0.1" spacing	Samtec	TSW-103-07-L-D
SW1	SMT, half-pitch 2-position switch	C&K Division, ITT	TDA02H0SK1
SW2	SMT, half-pitch 8-position switch	C&K Division, ITT	TDA08H0SK1
	Jumper plug	Samtec	SNT-100-BK-T

Appendix G USB-MODEVM Protocol

G.1 USB-MODEVM Protocol

The USB-MODEVM is defined to be a Vendor-Specific class and is identified on the PC system as an NI-VISA device. Because the TAS1020B has several routines in its ROM which are designed for use with HID-class devices, HID-like structures are used, even though the USB-MODEVM is not an HID-class device. Data is passed from the PC to the TAS1020B using the control endpoint.

Data is sent in a HIDSETREPORT (see Table 9).

Table 9. USB Control Endpoint HIDSETREPORT Request

Part	Value	Description
bmRequestType	0x21	00100001
bRequest	0x09	SET_REPORT
wValue	0x00	don't care
wIndex	0x03	HID interface is index 3
wLength	calculated by host	
Data		Data packet as described in Table 10.

The data packet consists of the following bytes, shown in Table 10:

Table 10. Data Packet Configuration

BYTE NUMBER	TYPE	DESCRIPTION
0	Interface	Specifies serial interface and operation. The two values are logically ORed. Operation: READ 0x00 WRITE 0x10 Interface: GPIO 0x08 SPI_16 0x04 I2C_FAST 0x02 I2C_STD 0x01 SPI_8 0x00
1	I²C Slave Address	Slave address of I²C device or MSB of 16-bit reg addr for SPI
2	Length	Length of data to write/read (number of bytes)
3	Register address	Address of register for I²C or 8-bit SPI; LSB of 16-bit address for SPI
4..64	Data	Up to 60 data bytes could be written at a time. EP0 maximum length is 64. The return packet is limited to 42 bytes, so advise only sending 32 bytes at any one time.

Example usage:
Write two bytes (AA, 55) to device starting at register 5 of an I²C device with address A0:

```
[0] 0x11
[1] 0xA0
[2] 0x02
[3] 0x05
[4] 0xAA
[5] 0x55
```

Do the same with a fast mode I^2C device:

```
[0] 0x12
[1] 0xA0
[2] 0x02
[3] 0x05
[4] 0xAA
[5] 0x55
```

Now with an SPI device which uses an 8-bit register address:

```
[0] 0x10
[1] 0xA0
[2] 0x02
[3] 0x05
[4] 0xAA
[5] 0x55
```

Now, do a 16-bit register address, as found on parts like the TSC2101. Assume the register address (command word) is **0x10E0**:

[0] 0x14
[1] 0x10 → **Note:** the I^2C address now serves as MSB of reg addr.
[2] 0x02
[3] 0xE0
[4] 0xAA
[5] 0x55

In each case, the TAS1020 returns, in an HID interrupt packet, the following:

[0] interface byte | status

status:

REQ_ERROR 0x80
INTF_ERROR 0x40
REQ_DONE 0x20

[1] for I^2C interfaces, the I^2C address as sent
for SPI interfaces, the read back data from SPI line for transmission of the corresponding byte

[2] length as sent

[3] for I^2C interfaces, the reg address as sent
for SPI interfaces, the read back data from SPI line for transmission of the corresponding byte

[4..60] echo of data packet sent

If the command is sent with no problem, the returning byte [0] is the same as the sent one logically ORed with 0x20 - in the preceding first example, the returning packet is:

```
[0] 0x31
[1] 0xA0
[2] 0x02
[3] 0x05
[4] 0xAA
[5] 0x55
```

If for some reason the interface fails (for example, the I²C device does not acknowledge), it comes back as:

```
[0] 0x51 → interface | INTF_ERROR
[1] 0xA0
[2] 0x02
[3] 0x05
[4] 0xAA
[5] 0x55
```

If the request is malformed, that is, the interface byte (byte [0]) takes on a value which is not as previously described, the return packet is:

```
[0] 0x93 → the user sent 0x13, which is not valid, so 0x93 returned
[1] 0xA0
[2] 0x02
[3] 0x05
[4] 0xAA
[5] 0x55
```

The preceding examples used writes. Reading is similar:
Read two bytes from device starting at register 5 of an I²C device with address A0:

```
[0] 0x01
[1] 0xA0
[2] 0x02
[3] 0x05
```

The return packet is:

```
[0] 0x21
[1] 0xA0
[2] 0x02
[3] 0x05
[4] 0xAA
[5] 0x55
```

assuming that the values written starting at Register 5 were actually written to the device.

G.2 GPIO Capability

The USB-MODEVM has seven GPIO lines. Access them by specifying the interface to be 0x08, and then using the standard format for packets—but addresses are unnecessary. The GPIO lines are mapped into one byte (see Table 11):

Table 11. GPIO Pin Assignments

Bit 7	6	5	4	3	2	1	0
x	P3.5	P3.4	P3.3	P1.3	P1.2	P1.1	P1.0

Example: write P3.5 to a 1, set all others to 0:

`[0] 0x18` → write, GPIO
`[1] 0x00` → this value is ignored
`[2] 0x01` → length - ALWAYS a 1
`[3] 0x00` → this value is ignored
`[4] 0x40` → 01000000

The user can also read back from the GPIO to see the state of the pins. Assume the previous example was just written to the port pins.

Example: read the GPIO

`[0] 0x08` → read, GPIO
`[1] 0x00` → this value is ignored
`[2] 0x01` → length - ALWAYS a 1
`[3] 0x00` → this value is ignored

The return packet is:

```
[0] 0x28
[1] 0x00
[2] 0x01
[3] 0x00
[4] 0x40
```

G.3 Writing Scripts

A script is simply a text file that contains data to send to the serial control buses.

Each line in a script file is one command. No provision is made for extending lines beyond one line, except for the **>** command. A line is terminated by a carriage return.

The first character of a line is the command. Commands are:

i Set interface bus to use
r Read from the serial control bus
w Write to the serial control bus
> Extend repeated write commands to lines below a **w**
Comment
b Break
d Delay

f Wait for Flag

The first command, **i**, sets the interface to use for the commands to follow. This command must be followed by one of the following parameters:

i2cstd	Standard mode I^2C bus
i2cfast	Fast mode I^2C bus
spi8	SPI bus with 8-bit register addressing
spi16	SPI bus with 16-bit register addressing
gpio	Use the USB-MODEVM GPIO capability

For example, if a fast mode I^2C bus is to be used, the script begins with:

i i2cfast

A double quoted string of characters following the **b** command can be added to provide information to the user about each breakpoint. When the script is executed, the software's command handler halts as soon as a breakpoint is detected and displays the string of characters within the double quotes.

The Wait for Flag command, **f,** reads a specified register and verifies if the bitmap provided with the command matches the data being read. If the data does not match, the command handler retries for up to 200 times. This feature is useful when switching buffers in parts that support the adaptive filtering mode. The command f syntax follows:

```
f [i2c address] [register] [D7][D6][D5][D4][D3][D2][D1][D0] where 'i2c address' and 'register'
are in hexadecimal format and 'D7' through 'D0' are in binary format with values of 0, 1 or X for
don't care.
```

Anything following a comment command **#** is ignored by the parser, provided that it is on the same line.

The delay command **d** allows the user to specify a time, in milliseconds, that the script pauses before proceeding. **The delay time is entered in decimal format.**

A series of byte values follows either a read or write command. Each byte value is expressed in hexadecimal, and each byte must be separated by a space. Commands are interpreted and sent to the TAS1020B by the program using the protocol described in Section G.1.

The first byte following an **r** (read) or **w** (write) command is the I^2C slave address of the device (if I^2C is used) or the first data byte to write (if SPI is used—note that SPI interfaces are not standardized on protocols, so the meaning of this byte varies with the device being addressed on the SPI bus). The second byte is the starting register address that data will be written to (again, with I^2C; SPI varies—see Section G.1 for additional information about what variations may be necessary for a particular SPI mode). Following these two bytes are data, if writing; if reading, the third byte value is the number of bytes to read, (expressed in hexadecimal).

For example, to write the values 0xAA 0x55 to an I^2C device with a slave address of 0x30, starting at a register address of 0x03, the user writes:

```
#example script i i2cfast w 30 03 AA 55 r 30 03 02
```

This script begins with a comment, specifies that a fast I^2C bus will be used, then writes *0xAA 0x55* to the I^2C slave device at address 0x30, writing the values into registers 0x03 and 0x04. The script then reads back two bytes from the same device starting at register address 0x03. Note that the slave device value does not change. It is unnecessary to set the $R/\overline{W}$ bit for I^2C devices in the script; the read or write commands does that.

If extensive repeated write commands are sent and commenting is desired for a group of bytes, the **>** command can be used to extend the bytes to other lines that follow. A usage example for the **>** command follows:

```
#example script for '>' command i i2cfast # Write AA and BB to registers 3 and 4, respectively w
30 03 AA BB # Write CC, DD, EE and FF to registers 5, 6, 7 and 8, respectively > CC DD EE FF #
Place a commented breakpoint b "AA BB CC DD EE FF was written, starting at register 3" # Read
back all six registers, starting at register 3 r 30 03 06
```

The following example demonstrates usage of the Wait for Flag command, **f**:

```
#example script for 'wait for flag' command i i2cfast # Switch to Page 44 w 30 00 2C # Switch
buffers w 30 01 05 # Wait for bit D0 to clear. 'x' denotes a don't care. f 30 01 xxxxxxx0
```

Any text editor can be used to write these scripts; Jedit is an editor that is highly recommended for general usage. For more information, go to: http://www.jedit.org.

Once the script is written, it can be used in the command window by running the program, and then selecting *Open Script File...* from the File menu. Locate the script and open it. The script is then displayed in the command buffer. The user can also edit the script once it is in the buffer and save it by selecting *Save Script File...* from the File menu.

Once the script is in the command buffer, it can be executed by pressing the *Execute Command Buffer* button. If there are breakpoints in the script, the script executes to that point, and the user is presented with a dialog box with a button to press to continue executing the script. When ready to proceed, push that button and the script continues.

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Exceeding the specified input range may cause unexpected operation and/or irreversible damage to the EVM. If there are questions concerning the input range, please contact a TI field representative prior to connecting the input power.

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