

# TPS22960 Low-Input Voltage, Dual-Load Switch With Controlled Turnon

## 1 Features

- Integrated dual-load switch
- Input voltage range: 1.62V to 5.5V
- Low ON-state resistance
  - $r_{ON} = 342\text{m}\Omega$  at  $V_{IN} = 5.5\text{V}$
  - $r_{ON} = 435\text{m}\Omega$  at  $V_{IN} = 3.3\text{V}$
  - $r_{ON} = 523\text{m}\Omega$  at  $V_{IN} = 2.5\text{V}$
  - $r_{ON} = 737\text{m}\Omega$  at  $V_{IN} = 1.8\text{V}$
- 500mA maximum continuous switch current
- Low quiescent current and shutdown current
- Controlled switch output rise time: 75 $\mu\text{s}$  or 660 $\mu\text{s}$
- Integrated quick output discharge transistor
- ESD performance tested per JESD 22
  - 2000V human body model (A114-B, Class II)
  - 1000V charged-device model (C101)
- 8-pin SOT (DCN) package: 3mm × 3mm
- 8-pin UQFN (RSE) package: 1.5mm × 1.5mm

## 2 Applications

- GPS Devices
- Cell Phones/PDAs
- MP3 Players
- Digital Cameras

## 3 Description

The TPS22960 is a small low- $r_{ON}$  dual-channel load switch with controlled turnon. The devices contain two P-channel MOSFETs that can operate over an input voltage range of 1.62V to 5.5V. Each switch is independently controlled by on/off inputs (ON1 and ON2), which are capable of interfacing directly with low-voltage control signals. In TPS22960 a 85 $\Omega$  on-chip load resistor is added for quick discharge when the switch is turned off.

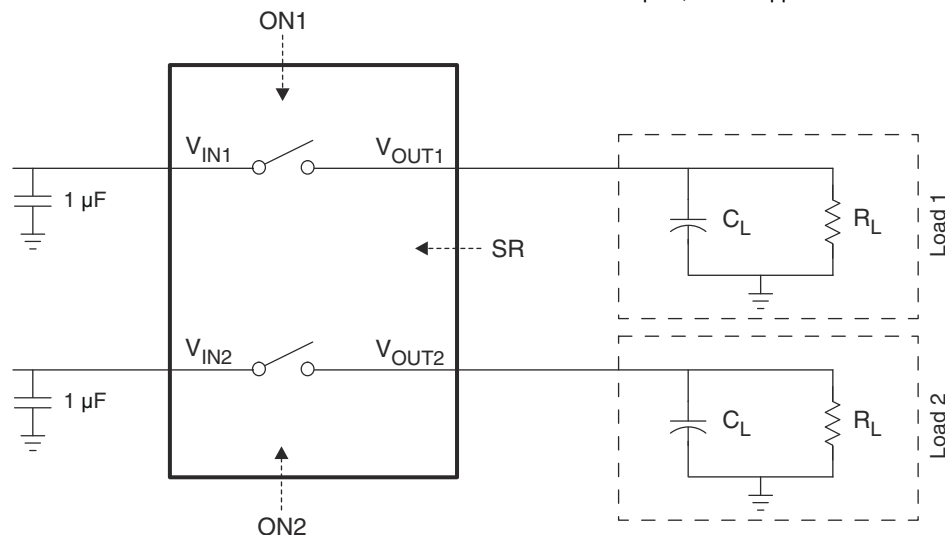
The rise time (slew-rate) of the device is internally controlled in order to avoid inrush current, and it can be slowed down if needed using the SR pin: at 3.3V, TPS22960 features a 75 $\mu\text{s}$  rise time with the SR pin tied to ground and 660 $\mu\text{s}$  with the SR pin tied to high.

The TPS22960 is available in a space-saving 8-pin UQFN package and in an 8-pin SOT package. It is characterized for operation over the free-air temperature range of  $-40^{\circ}\text{C}$  to  $85^{\circ}\text{C}$ .

### Package Information

PART NUMBER	PACKAGE <sup>(1)</sup>	PACKAGE SIZE <sup>(2)</sup>
TPS22960	DCN (SOT, 8)	2.90mm × 1.63mm
	RSE (UQFN, 8)	1.50mm × 1.50mm

- (1) For all available packages, see the orderable addendum at the end of the data sheet.
- (2) The package size (length × width) is a nominal value and includes pins, where applicable.



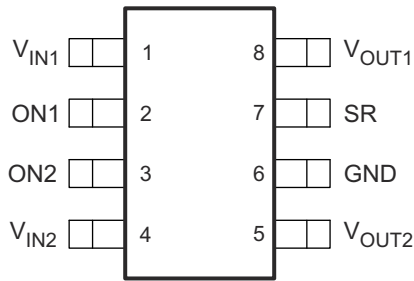
**Simplified Diagram**



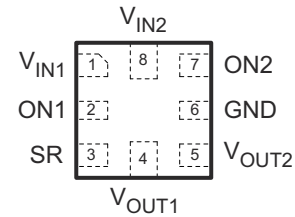
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## 4 Pin Configuration and Functions



**Figure 4-1. DCN Package, 8-pin SOT (Top View)**



**Figure 4-2. RSE Package, 8-pin UQFN (Top View)**

**Table 4-1. Pin Functions**

NAME	PIN		I/O	DESCRIPTION
	SOT	UQFN		
V <sub>IN1</sub>	1	1	I	Switch 1 input; bypass this input with a ceramic capacitor to GND.
ON1	2	2	I	Switch 1 control input, active high. Do not leave floating.
ON2	3	7	I	Switch 2 control input, active high. Do not leave floating.
V <sub>IN2</sub>	4	8	I	Switch 2 input; bypass this input with a ceramic capacitor to GND.
V <sub>OUT2</sub>	5	5	O	Switch 2 output.
GND	6	6	—	Ground.
SR	7	3	I	Slew rate control pin. SR = GND translates into a 75- $\mu$ s rise time; SR = high translates into a 660- $\mu$ s rise time.
V <sub>OUT1</sub>	8	4	O	Switch 1 output.

## 5 Specifications

### 5.1 Absolute Maximum Ratings

(see <sup>(1)</sup>)

		MIN	MAX	UNIT
V <sub>IN</sub>	Input voltage	-0.3	6	V
V <sub>OUT</sub>	Output voltage		V <sub>IN</sub> + 0.3	V
V <sub>ON</sub>	Input voltage	-0.3	6	V
I <sub>MAX</sub>	Maximum continuous switch current		0.5	A
T <sub>A</sub>	Operating free-air temperature	-40	85	°C
T <sub>J</sub>	Maximum junction temperature		125	°C
T <sub>stg</sub>	Storage temperature	-65	150	°C

- (1) Stresses beyond those listed under absolute maximum ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

### 5.2 ESD Ratings

		VALUE	UNIT
V <sub>(ESD)</sub>	Electrostatic discharge		
	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001 <sup>(1)</sup>	2000	V
	Charged-device model (CDM), per JEDEC specification JESD22-C101 <sup>(2)</sup>	1000	

- (1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.  
 (2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

### 5.3 Recommended Operating Conditions

		MIN	MAX	UNIT	
V <sub>IN</sub>	Input voltage	1.62	5.5	V	
V <sub>OUT</sub>	Output voltage		V <sub>IN</sub>	V	
V <sub>IH</sub>	High-level input voltage: ON1, ON2, SR	V <sub>INx</sub> = 3.0 V to 5.5 V	1.5	5.5	V
		V <sub>INx</sub> = 1.62 V to 3.0 V	1.4	5.5	
V <sub>IL</sub>	Low-level input voltage: ON1, ON2, SR	V <sub>INx</sub> = 3.0 V to 5.5 V		0.5	V
		V <sub>INx</sub> = 1.62 V to 3.0 V		0.4	
C <sub>IN</sub>	Input capacitor	1 <sup>(1)</sup>		μF	

- (1) See [Section 8.1](#).

### 5.4 Thermal Information

THERMAL METRIC <sup>(1)</sup>	DCN (SOT)	RSE (UQFN)	UNIT	
	8 PINS	8 PINS		
R <sub>θJA</sub>	Junction-to-ambient thermal resistance	254	124	°C/W
R <sub>θJC(top)</sub>	Junction-to-case (top) thermal resistance	122	67	°C/W
R <sub>θJB</sub>	Junction-to-board thermal resistance	181	31.5	°C/W
ψ <sub>JT</sub>	Junction-to-top characterization parameter	22	2.9	°C/W
ψ <sub>JB</sub>	Junction-to-board characterization parameter	178	31.5	°C/W
R <sub>θJC(bot)</sub>	Junction-to-case (bottom) thermal resistance	—	—	°C/W

- (1) For more information about traditional and new thermal metrics, see *Semiconductor and IC Package Thermal Metrics (SPRA953)*.

## 5.5 Electrical Characteristics

 $V_{IN} = 1.62\text{ V to }5.5\text{ V}$ ,  $T_A = -40^\circ\text{C to }85^\circ\text{C}$  (unless otherwise noted)

PARAMETER		TEST CONDITIONS	$T_A$	MIN	TYP <sup>(1)</sup>	MAX	UNIT			
$I_{IN}$	Quiescent current (each switch)	$I_{OUTx} = 0$ , $V_{INx} = V_{ON}$	$V_{INx} = 5.5\text{ V}$	Full	0.64	2	$\mu\text{A}$			
			$V_{INx} = 3.3\text{ V}$	Full	0.35	1.2				
			$V_{INx} = 2.5\text{ V}$	Full	0.24	0.8				
			$V_{INx} = 1.8\text{ V}$	Full	0.15	0.5				
$I_{IN(OFF)}$	OFF-state supply current (each switch)	$V_{ON} = \text{GND}$ , $V_{OUTx} = \text{Open}$	$V_{INx} = 5.5\text{ V}$	Full	0.47	3.6	$\mu\text{A}$			
			$V_{INx} = 3.3\text{ V}$	Full	0.25	1.8				
			$V_{INx} = 2.5\text{ V}$	Full	0.18	1.3				
			$V_{INx} = 1.8\text{ V}$	Full	0.11	1.2				
$r_{ON}$	ON-state resistance (each switch)	$I_{OUT} = -200\text{ mA}$	$V_{INx} = 5.5\text{ V}$	25°C	342	400	$\text{m}\Omega$			
				Full		465				
			$V_{INx} = 3.3\text{ V}$	25°C	435	500				
				Full		595				
			$V_{INx} = 2.5\text{ V}$	25°C	523	620				
				Full		720				
			$V_{INx} = 1.8\text{ V}$	25°C	737	1100				
				Full		1300				
			$V_{INx} = 1.62\text{ V}$	25°C	848	1300				
				Full		1500				
			$r_{PD}$	Output pulldown resistance	$V_{IN} = 3.3\text{ V}$ , $V_{ON} = 0$ , $I_{OUT} = 30\text{ mA}$	25°C		85	120	$\Omega$
			$I_{ON}$	ON-state input leakage current	$V_{ON} = 1.62\text{ V to }5.5\text{ V or GND}$	Full			0.25	$\mu\text{A}$

(1) Typical values are at  $T_A = 25^\circ\text{C}$ .

## 5.6 Switching Characteristics

 $V_{IN} = 3.3\text{ V}$ ,  $T_A = 25^\circ\text{C}$ ,  $R_{L\_CHIP} = 85\ \Omega$  (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP <sup>(1)</sup>	MAX	UNIT
$t_{ON}$	Turn-ON time	$R_L = 33\ \Omega$ , $C_L = 0.1\ \mu\text{F}$	$SR = V_{IN}$	635		$\mu\text{s}$
			$SR = \text{GND}$	67		
$t_{OFF}$	Turn-OFF time	$R_L = 33\ \Omega$ , $C_L = 0.1\ \mu\text{F}$	$SR = V_{IN}$	4.5		$\mu\text{s}$
			$SR = \text{GND}$	4.2		
$t_r$	$V_{OUT}$ rise time	$R_L = 33\ \Omega$ , $C_L = 0.1\ \mu\text{F}$	$SR = V_{IN}$	660		$\mu\text{s}$
			$SR = \text{GND}$	75		
$t_f$	$V_{OUT}$ fall time	$R_L = 33\ \Omega$ , $C_L = 0.1\ \mu\text{F}$	$SR = V_{IN}$	4.5		$\mu\text{s}$
			$SR = \text{GND}$	4.5		

(1) Typical values are at the specified  $V_{IN} = 3.3\text{ V}$  and  $T_A = 25^\circ\text{C}$ .

### 5.7 Typical DC Characteristics

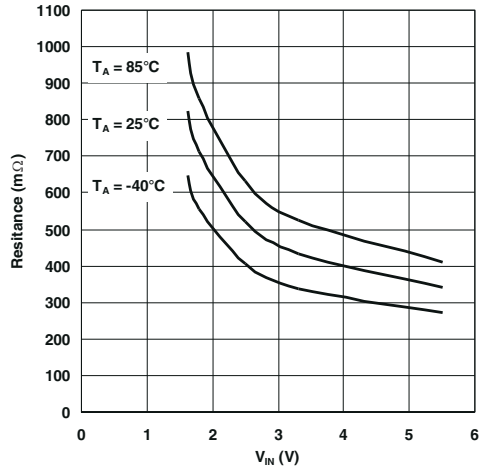


Figure 5-1. ON Resistance vs Input Voltage

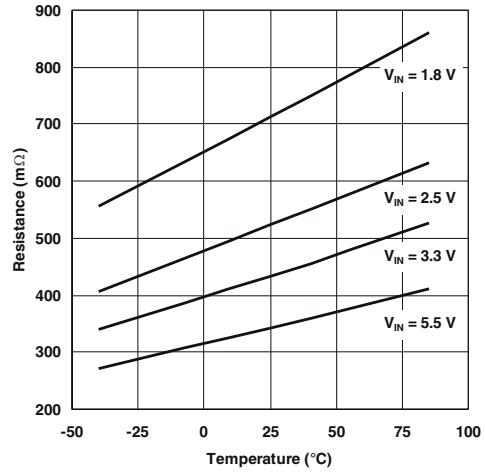


Figure 5-2. ON Resistance vs Temperature

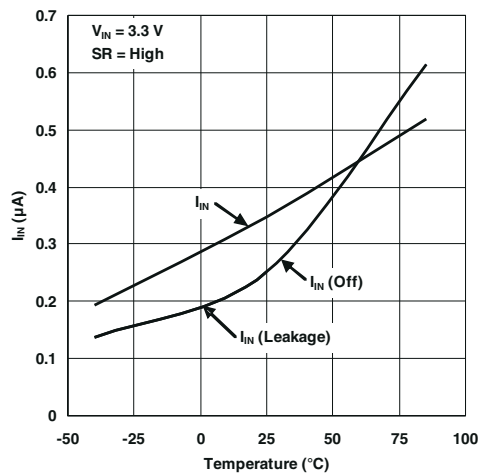


Figure 5-3. Quiescent Current vs Temperature

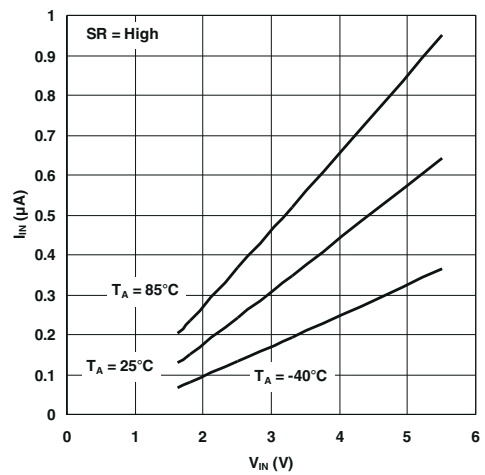


Figure 5-4. Quiescent Current vs Input Voltage

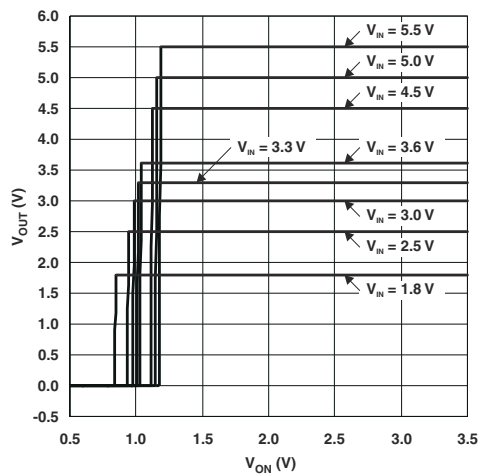


Figure 5-5. ON Threshold

## 5.8 Typical Switching Characteristics

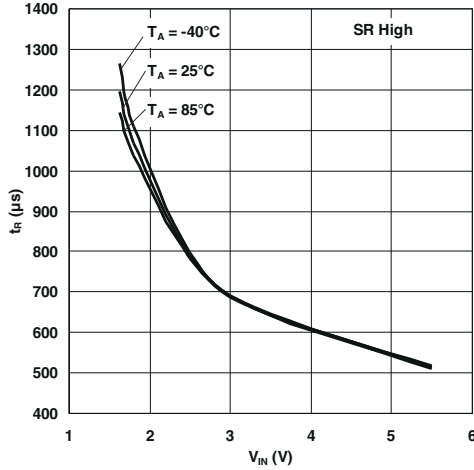


Figure 5-6. Rise Time vs Input Voltage

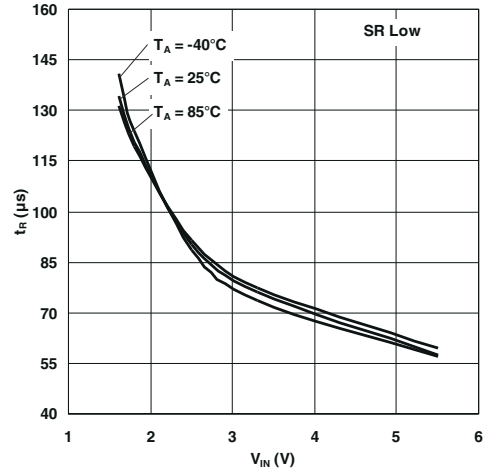


Figure 5-7. Rise Time vs Input Voltage

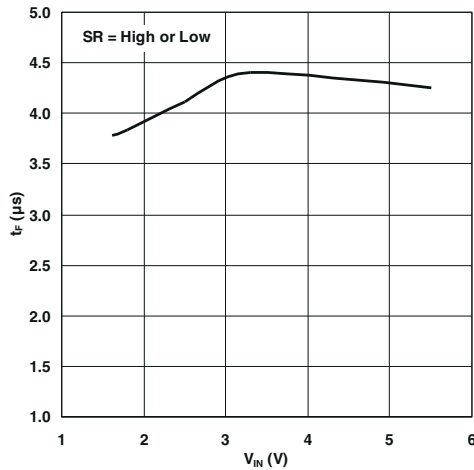


Figure 5-8. Fall Time vs Input Voltage

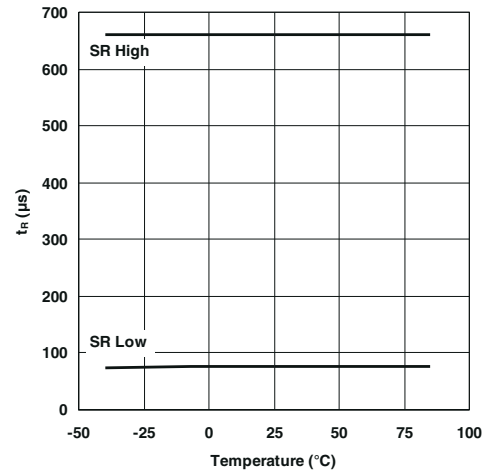


Figure 5-9. Rise Time vs Temperature

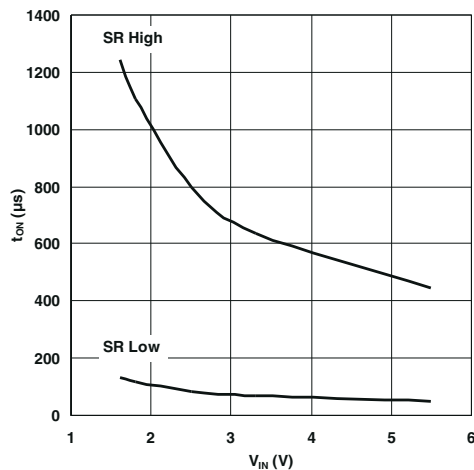


Figure 5-10. On Time vs Input Voltage

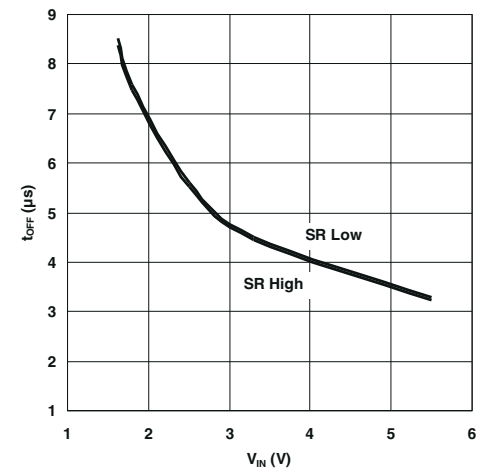


Figure 5-11. Off Time vs Input Voltage

### 5.8 Typical Switching Characteristics (continued)

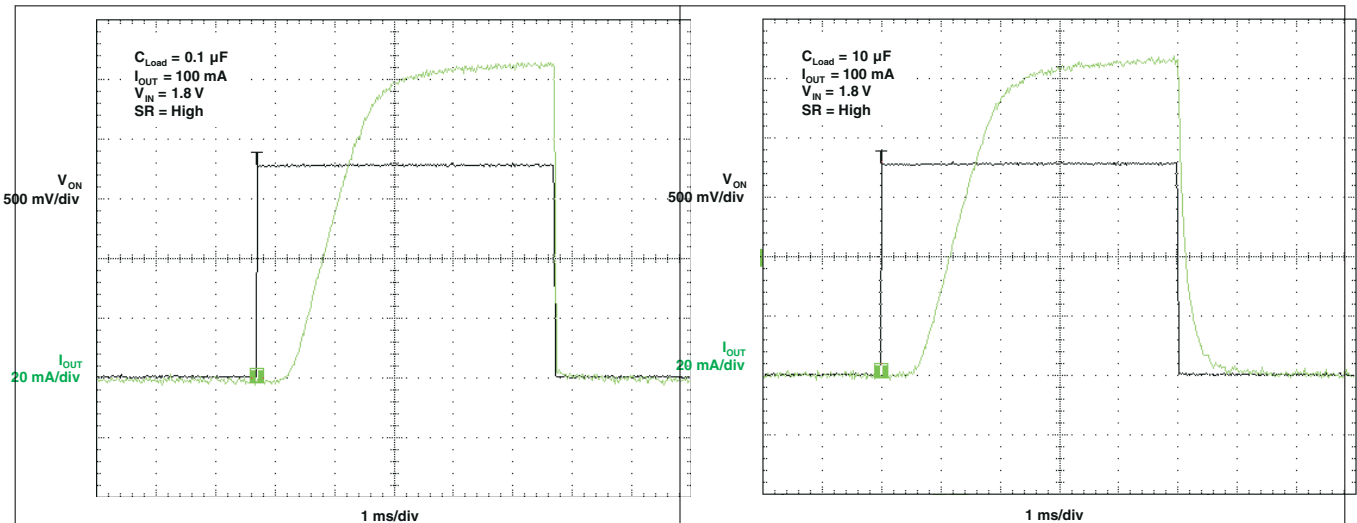


Figure 5-12.  $t_{ON}$  Response

Figure 5-13.  $t_{ON}$  Response

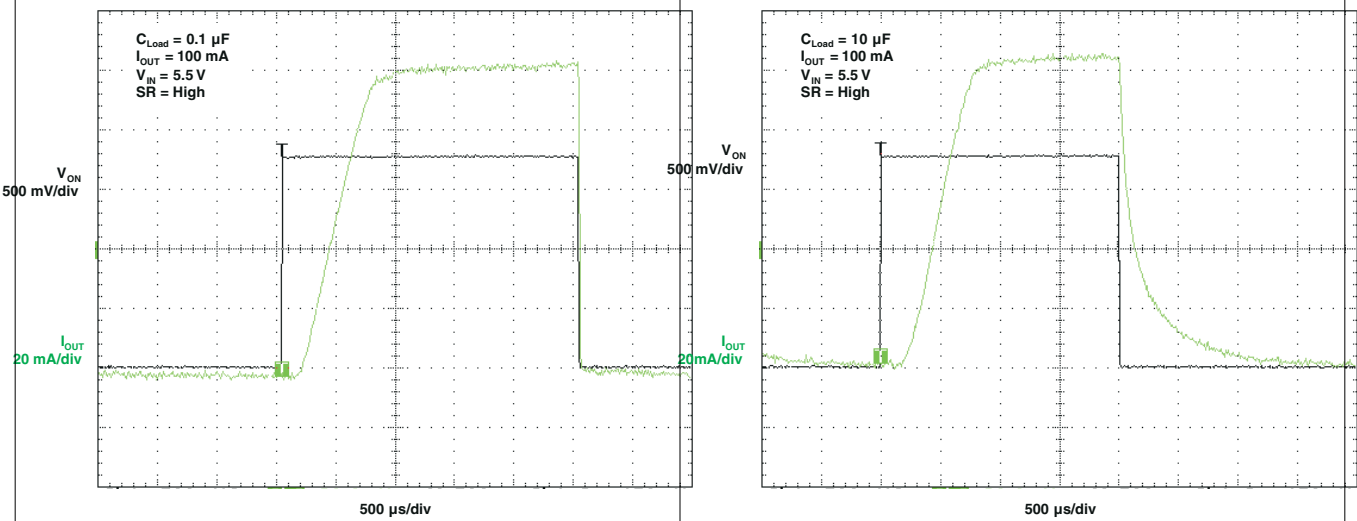


Figure 5-14.  $t_{ON}$  Response

Figure 5-15.  $t_{ON}$  Response

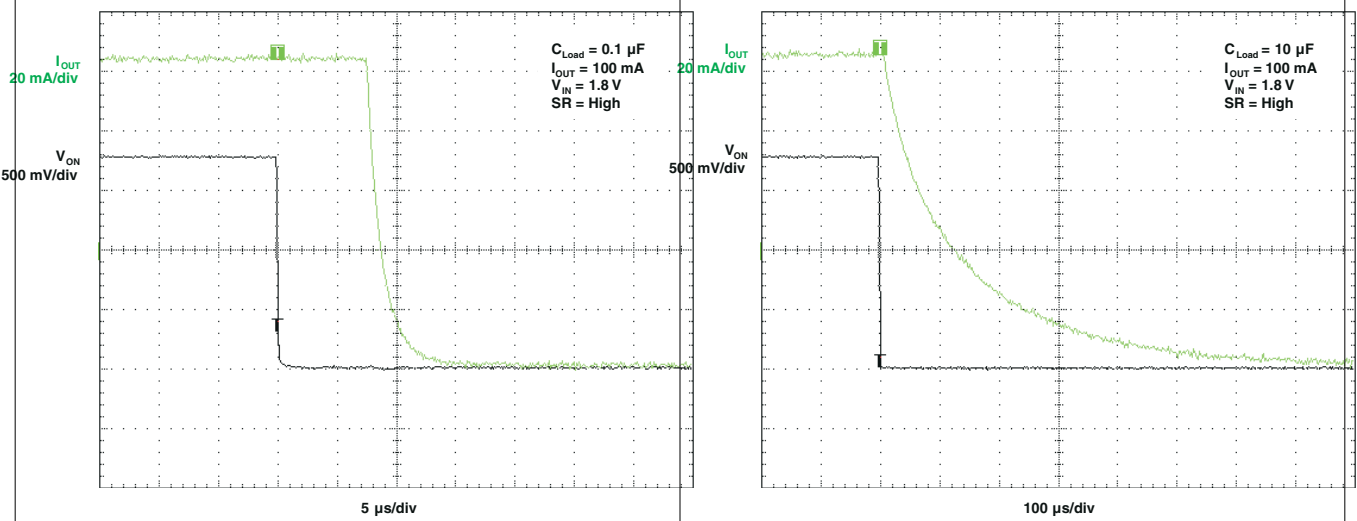


Figure 5-16.  $t_{OFF}$  Response

Figure 5-17.  $t_{OFF}$  Response



### 5.8 Typical Switching Characteristics (continued)

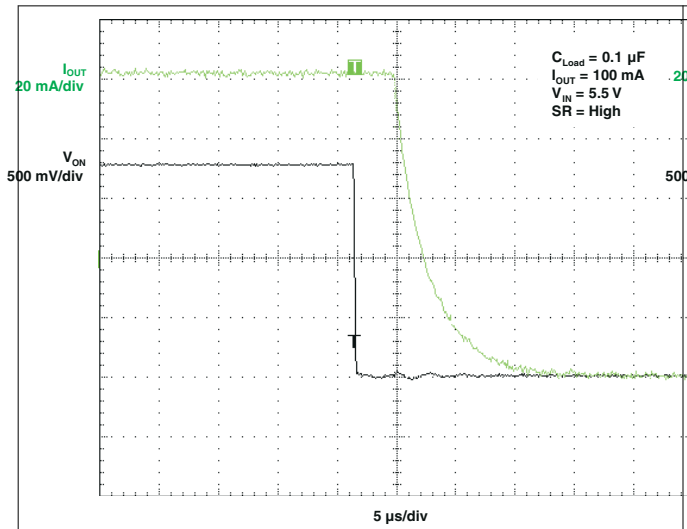


Figure 5-18.  $t_{OFF}$  Response

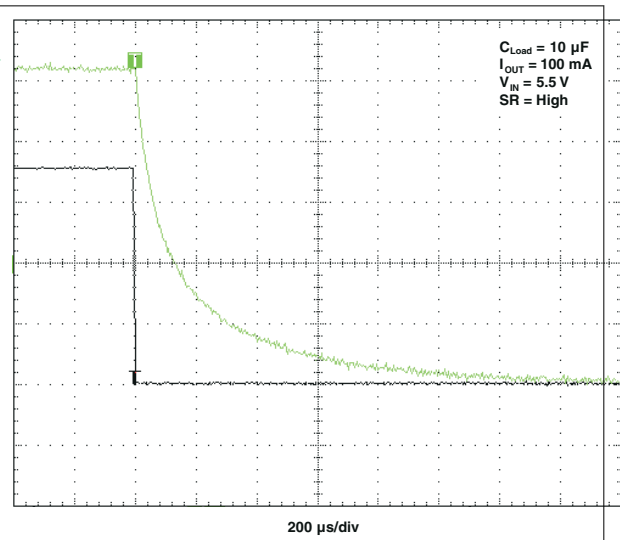


Figure 5-19.  $t_{OFF}$  Response

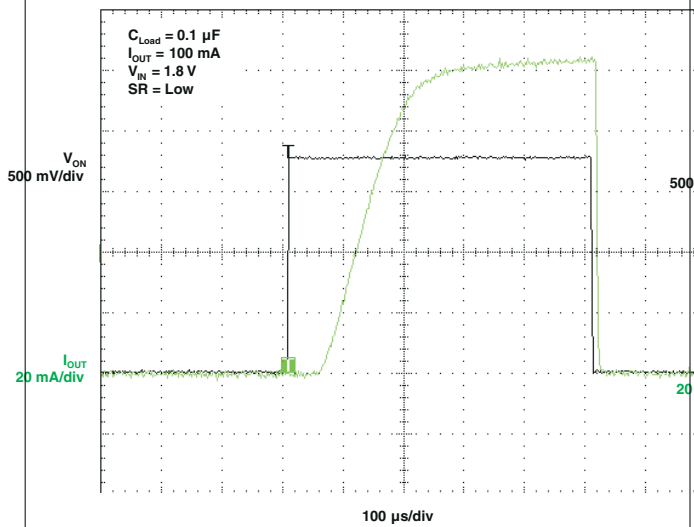


Figure 5-20.  $t_{ON}$  Response

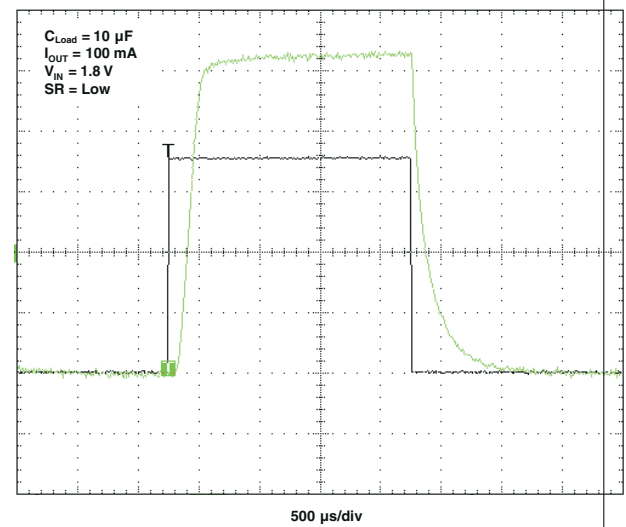


Figure 5-21.  $t_{ON}$  Response

### 5.8 Typical Switching Characteristics (continued)

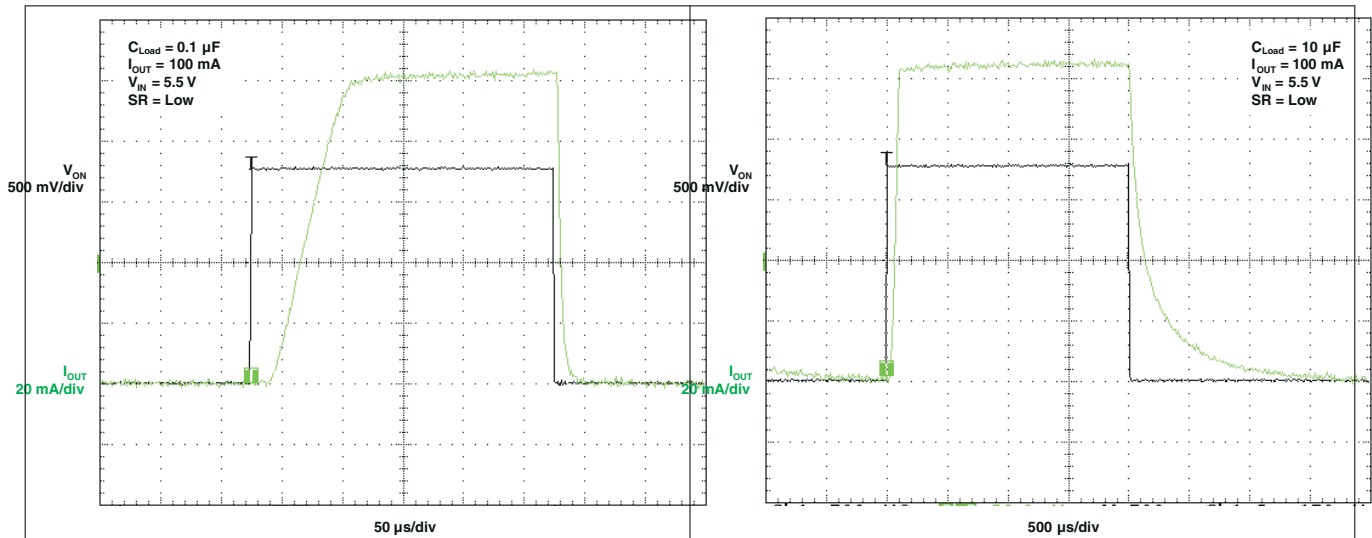


Figure 5-22.  $t_{ON}$  Response

Figure 5-23.  $t_{ON}$  Response

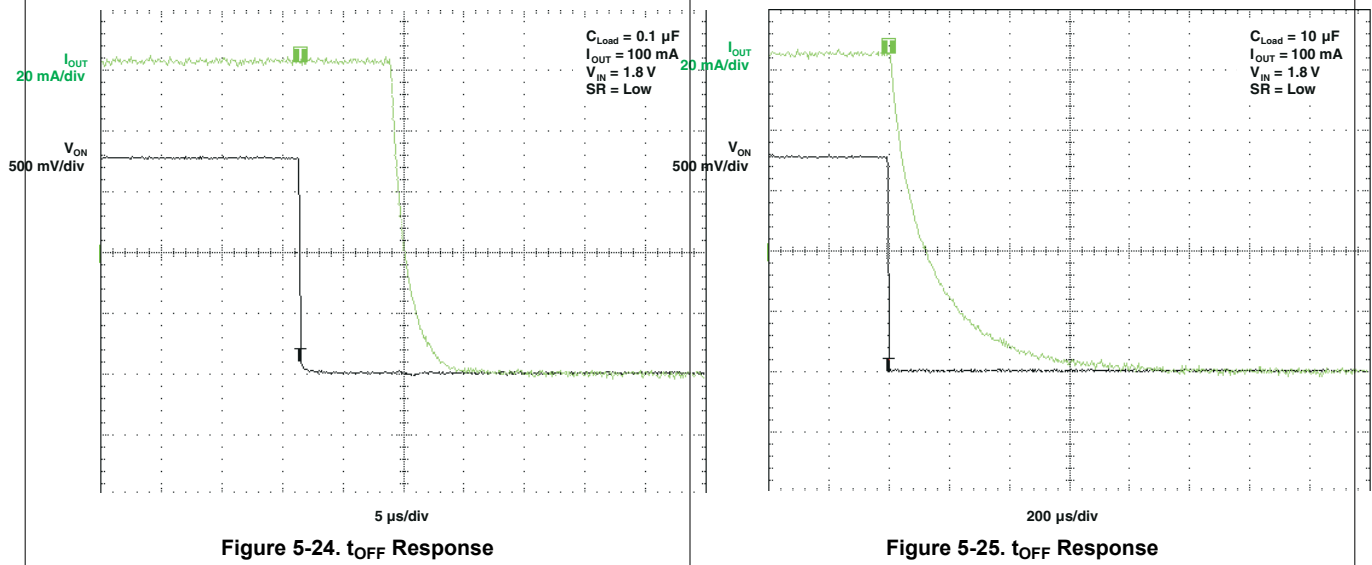
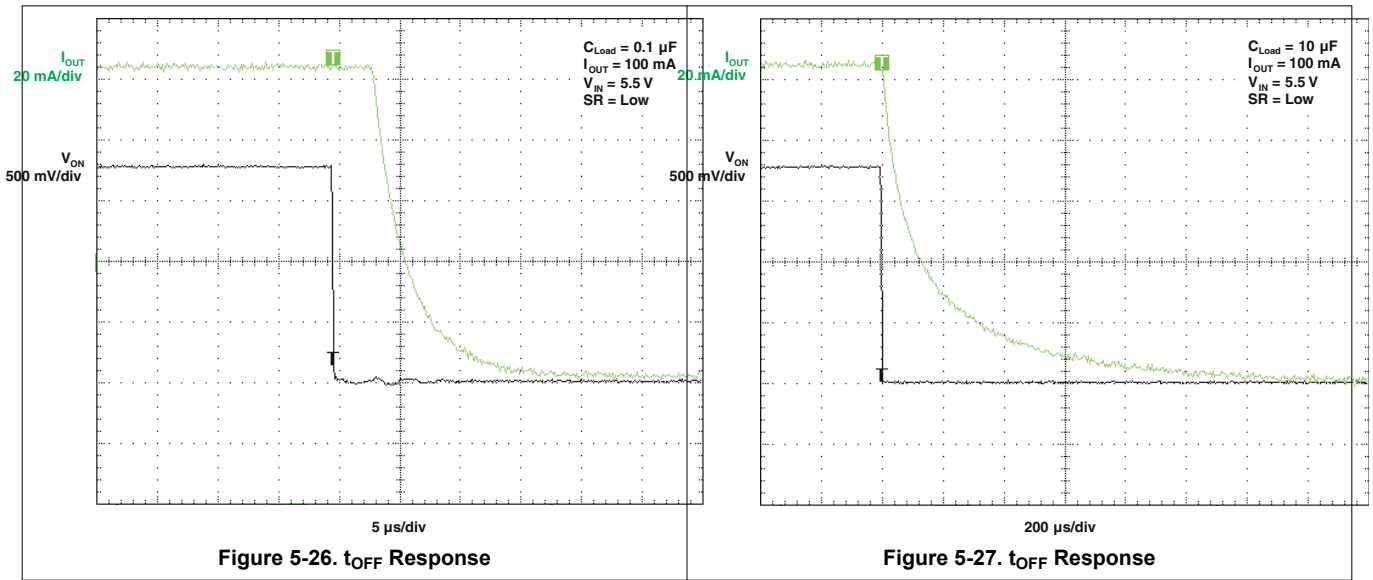


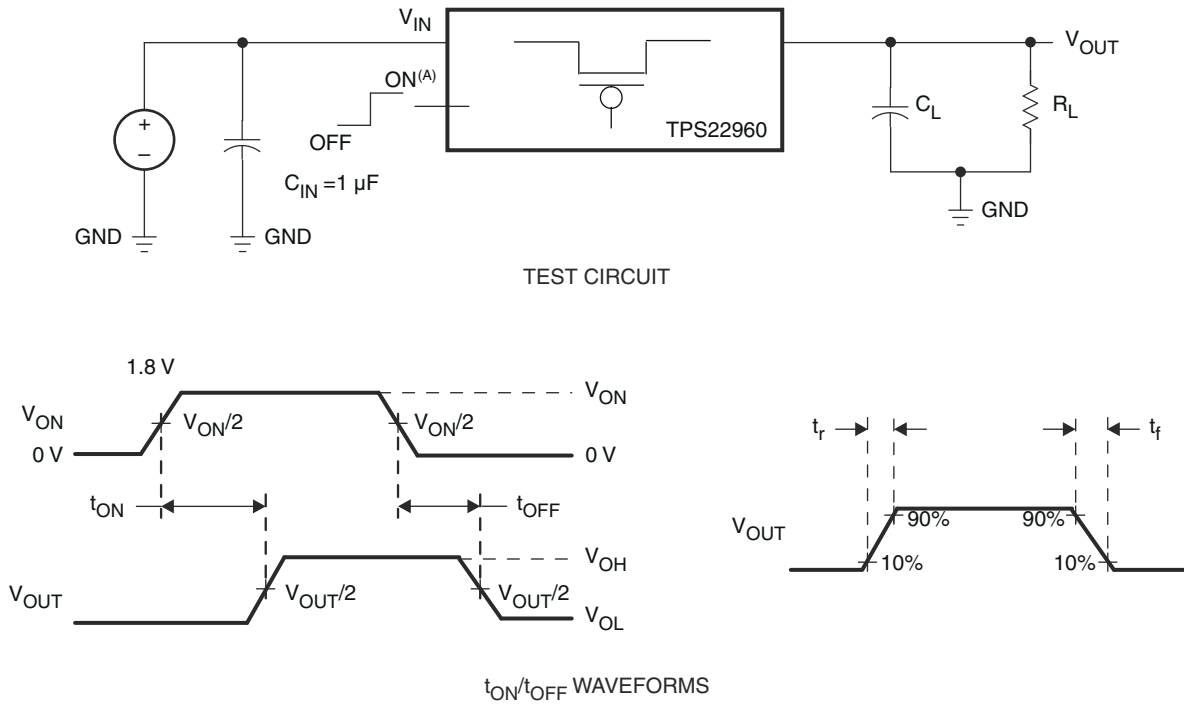
Figure 5-24.  $t_{OFF}$  Response

Figure 5-25.  $t_{OFF}$  Response

### 5.8 Typical Switching Characteristics (continued)



## 6 Parameter Measurement Information



A. t<sub>rise</sub> and t<sub>fall</sub> of the control signal is 100ns.

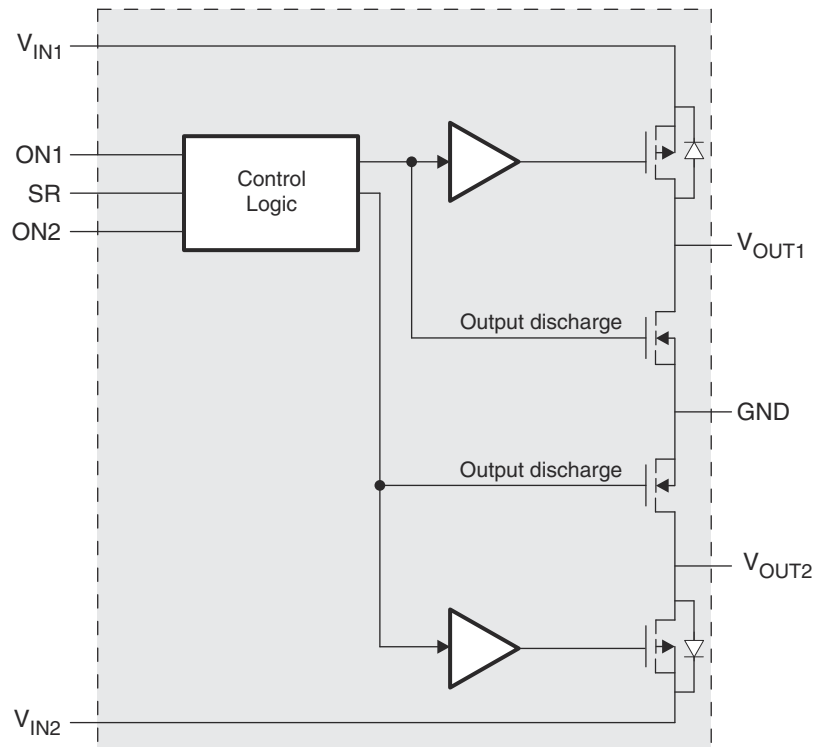
**Figure 6-1. Test Circuit and t<sub>ON</sub>/t<sub>OFF</sub> Waveforms**

## 7 Detailed Description

### 7.1 Overview

The TPS22960 is a dual-channel load switch. The two channels can be independently controlled using the ONx pins. Each channel has an 85-Ω quick discharge resistance from  $V_{OUTX}$  to GND when disabled. A single control pin (SR) is used to set the slew rate for both channels..

### 7.2 Functional Block Diagram



## 7.3 Feature Description

This section will discuss the features of the TPS22960 which have been summarized in [Table 7-1](#).

**Table 7-1. Feature Summary**

DEVICE	$r_{ON}$ AT 3.3 V (TYP)	SLEW RATE AT 3.3 V (TYP)	QUICK OUTPUT DISCHARGE <sup>(1)</sup>	MAX OUTPUT CURRENT	ENABLE
TPS22960	435 m $\Omega$	75 $\mu$ s with SR = low 660 $\mu$ s with SR = high	Yes	500 mA	Active High

(1) This feature discharges the output of the switch to ground through an 85- $\Omega$  resistor, preventing the output from floating.

### 7.3.1 Output Slew Rate (SR) Control

The slew rate (rise time) of the device is internally controlled in order to avoid inrush current, and it can be slowed down if needed using the SR pin. At 3.3 V, TPS22960 features a 75- $\mu$ s rise time with the SR pin tied to ground, and a 660- $\mu$ s rise time with the SR pin tied high. Both channels will have the same slew rate set by the SR pin.

### 7.3.2 Quick Output Discharge (QOD)

Each channel of the TPS22960 includes an independent QOD feature. When the channel is disabled, a discharge resistor is connected between VOUTx and GND. This resistor has a typical value of 85  $\Omega$  and prevents the output from floating while the switch is disabled.

## 7.4 Device Functional Modes

**Table 7-2. Configurable Logic Function Table**

ONx	V <sub>INx</sub> TO V <sub>OUTx</sub>	V <sub>OUTx</sub> TO GND
L	OFF	ON
H	ON	OFF

## 8 Application and Implementation

### Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

### 8.1 Application Information

#### 8.1.1 ON/OFF Control

The ON pin controls the state of the switch. Activating ON continuously holds the switch in the on state, as long as there is no fault. ON is active HI and has a low threshold, making it capable of interfacing with low voltage signals. The ON pin is compatible with standard GPIO logic threshold. It can be used with any microcontroller with 1.2-V, 1.8-V, 2.5-V, or 3.3-V GPIOs.

#### 8.1.2 Input Capacitor

To limit voltage drop or voltage transients, sufficient capacitance needs to be placed on the input side of the load switch (from  $V_{IN}$  to GND). In most cases, a 1- $\mu\text{F}$  ceramic capacitor,  $C_{IN}$ , placed close to the pins is usually sufficient. However, when switching heavy capacitive loads, higher values of  $C_{IN}$  may be needed to prevent the system supply voltage from dropping.

#### 8.1.3 Output Capacitor

The integral body diode in the PMOS switch will allow reverse current flow if  $V_{OUT}$  exceeds  $V_{IN}$ . A  $C_L$  greater than  $C_{IN}$  can cause  $V_{OUT}$  to exceed  $V_{IN}$  if the system supply is removed. In the case where the system supply could be removed and reverse current is a concern, a  $C_{IN}$  greater than  $C_L$  is recommended.

### 8.2 Typical Application

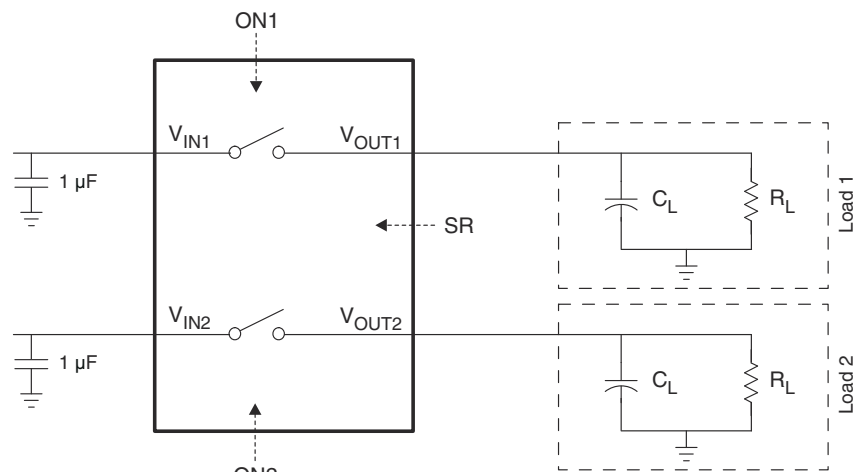


Figure 8-1. Typical Application Schematic

## 8.2.1 Design Requirements

For this design example, use input parameters in [Table 8-1](#).

**Table 8-1. Design Parameters**

PARAMETER	EXAMPLE VALUE
$V_{IN}$	3.3 V
$C_L$	22 $\mu$ F
Maximum acceptable inrush current	200 mA

## 8.2.2 Detailed Design Procedure

### 8.2.2.1 Inrush Current

When the switch is enabled, the output capacitors must be charged up from 0 V to the set value (in this example, 3.3 V). This charge arrives in the form of inrush current. Inrush current can be calculated using the following equation:

$$\text{Inrush Current} = C \times dV / dt \quad (1)$$

Where:

$C$  = output capacitance

$dV$  = output voltage

$dt$  = rise time

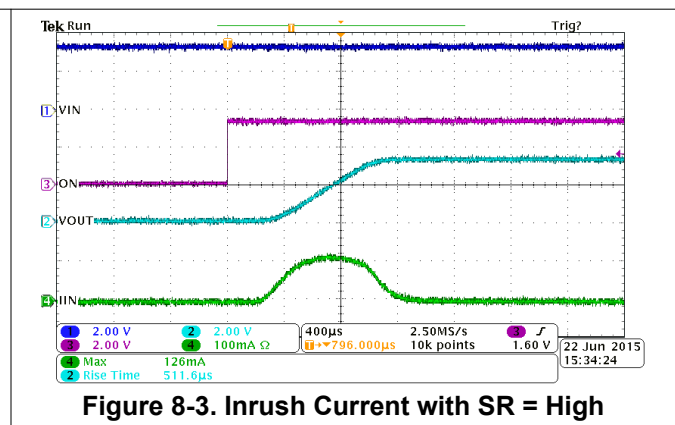
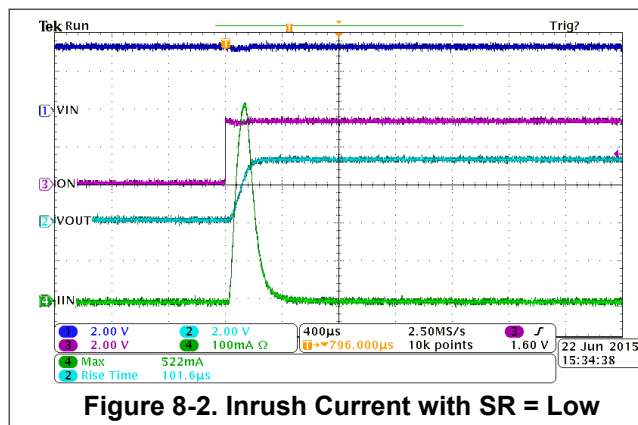
The TPS22960 offers selectable rise time control for  $V_{OUT}$ . This feature allows the user to control the inrush current during turnon. [Equation 1](#) can be used to find the required rise time to limit the inrush current to the design requirements

$$200 \text{ mA} = 22 \mu\text{F} \times (3.3 \text{ V} \times 80\%) / dt \quad (2)$$

$$dt = 290 \mu\text{s} \quad (4)$$

To ensure an inrush current of less than 200 mA, SR must be set high for a rise time greater than 290  $\mu$ s. The following application curves show the different inrush for each SR setting in this design example.

### 8.2.3 Application Curves



## 8.3 Power Supply Recommendations

The device is designed to operate from an input voltage range of 1.62 V to 5.5 V. The power supply should be well-regulated and placed as close to the device terminals as possible. It must be able to withstand all transient



and load current steps. In most situations, using an input capacitance of 1  $\mu\text{F}$  is sufficient to prevent the supply voltage from dipping when the switch is turned on. In cases where the power supply is slow to respond to a large transient current or large load current step, additional bulk capacitance may be required on the input

The requirements for larger input capacitance can be mitigated by selecting the slower slew rate +SR=high. This will cause the load switch to turn on more slowly and limit the inrush current.

## 8.4 Layout

### 8.4.1 Layout Guidelines

For best performance, all traces should be as short as possible. To be most effective, the input and output capacitors should be placed close to the device to minimize the effects that parasitic trace inductances may have on normal and short-circuit operation. Using wide traces for  $V_{\text{IN}}$ ,  $V_{\text{OUT}}$ , and GND will help minimize the parasitic electrical effects along with minimizing the case to ambient thermal impedance.

### 8.4.2 Layout Example

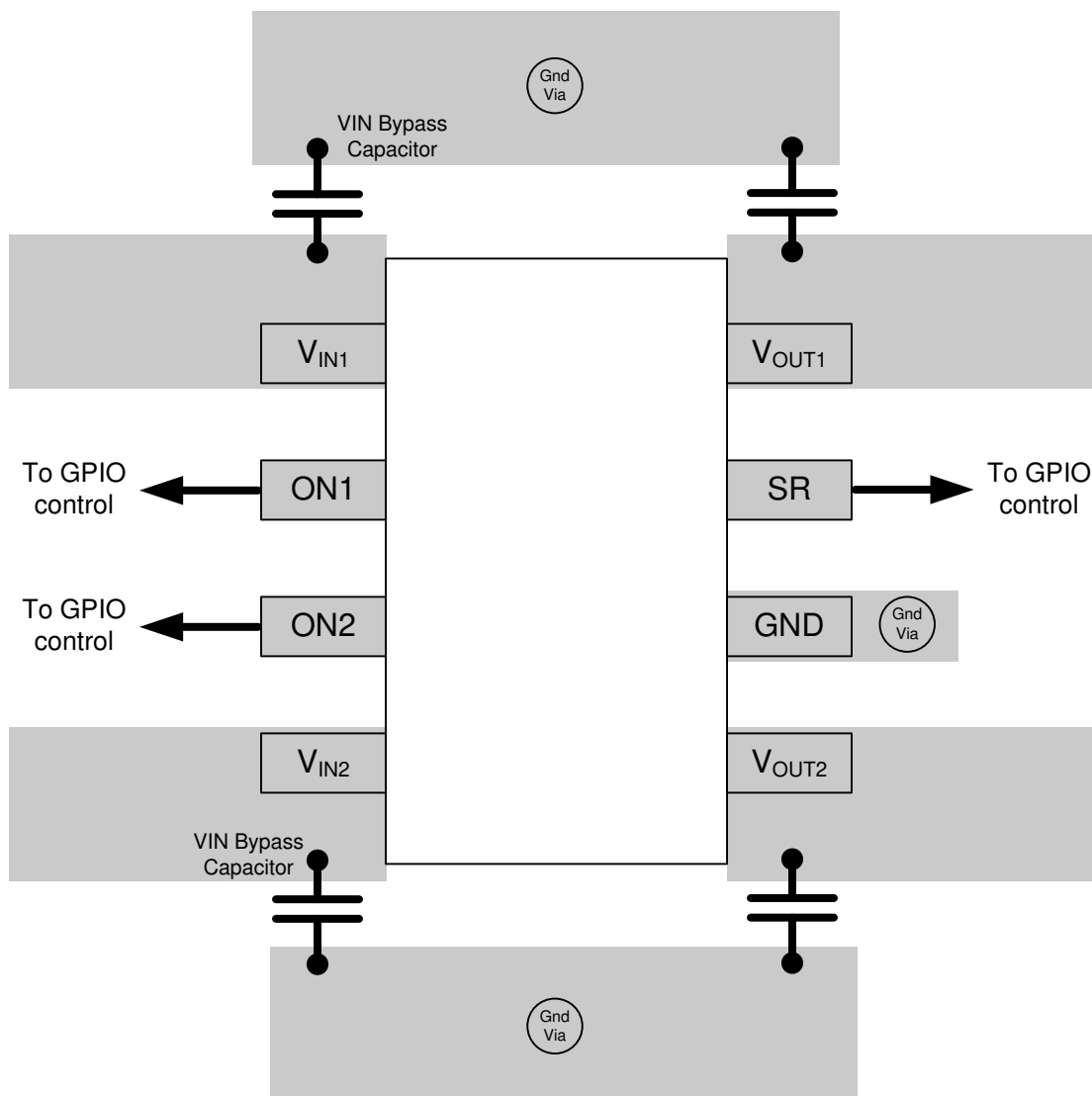


Figure 8-4. DCN Package Layout

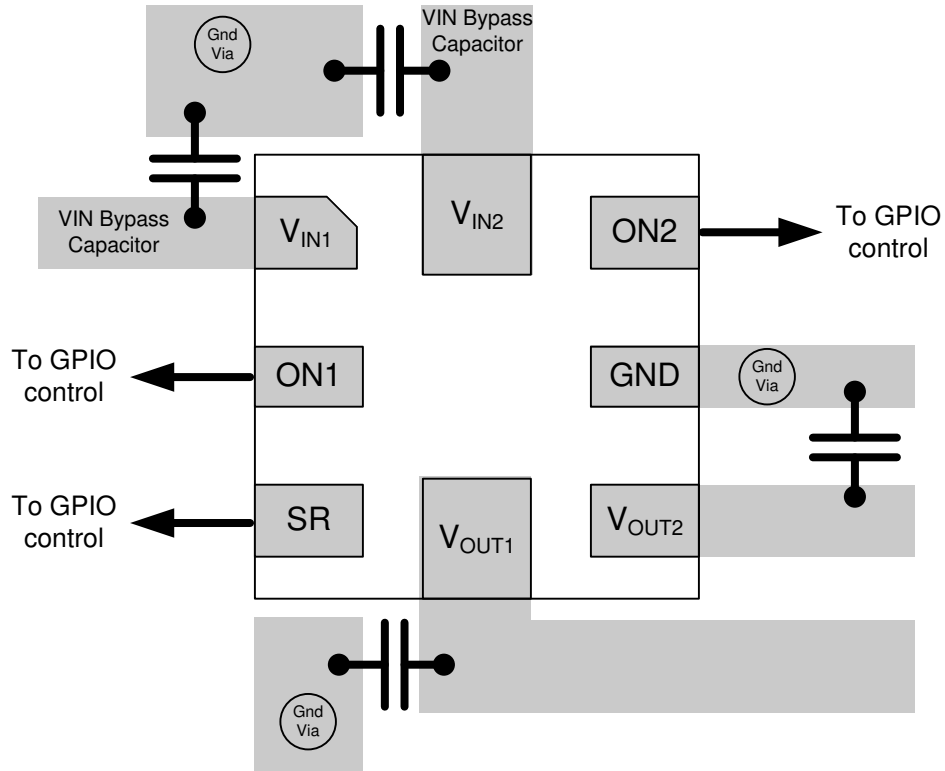


Figure 8-5. RSE Package Layout

## 9 Device and Documentation Support

### 9.1 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on [ti.com](http://ti.com). Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

### 9.2 Support Resources

[TI E2E™ support forums](#) are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's [Terms of Use](#).

### 9.3 Trademarks

TI E2E™ is a trademark of Texas Instruments.  
All trademarks are the property of their respective owners.

### 9.4 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

### 9.5 Glossary

[TI Glossary](#) This glossary lists and explains terms, acronyms, and definitions.

## 10 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

<b>Changes from Revision D (February 2016) to Revision E (April 2024)</b>	<b>Page</b>
• Updated the numbering format for tables, figures, and cross-references throughout the document.....	1
• Changed maximum $I_{IN(OFF)}$ at $V_{IN}=1.8V$ from $0.9\mu A$ : to $1.2\mu A$ in the <i>Electrical Characteristics</i> section.....	4

<b>Changes from Revision C (July 2015) to Revision D (February 2016)</b>	<b>Page</b>
• Made changes to <a href="#">Section 8.1</a> .....	1

## 11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

**PACKAGING INFORMATION**

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPS22960DCNR	ACTIVE	SOT-23	DCN	8	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	(NFRO, NFRR)	<a href="#">Samples</a>
TPS22960RSER	ACTIVE	UQFN	RSE	8	3000	RoHS & Green	NIPDAUAG	Level-1-260C-UNLIM	-40 to 85	72	<a href="#">Samples</a>
TPS22960RSET	ACTIVE	UQFN	RSE	8	250	RoHS & Green	NIPDAUAG	Level-1-260C-UNLIM	-40 to 85	72	<a href="#">Samples</a>

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

**TAPE AND REEL INFORMATION**

**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS22960DCNR	SOT-23	DCN	8	3000	180.0	8.4	3.23	3.17	1.37	4.0	8.0	Q3
TPS22960RSER	UQFN	RSE	8	3000	180.0	8.4	1.7	1.7	0.7	4.0	8.0	Q2
TPS22960RSET	UQFN	RSE	8	250	180.0	8.4	1.6	1.6	0.66	4.0	8.0	Q2

## TAPE AND REEL BOX DIMENSIONS

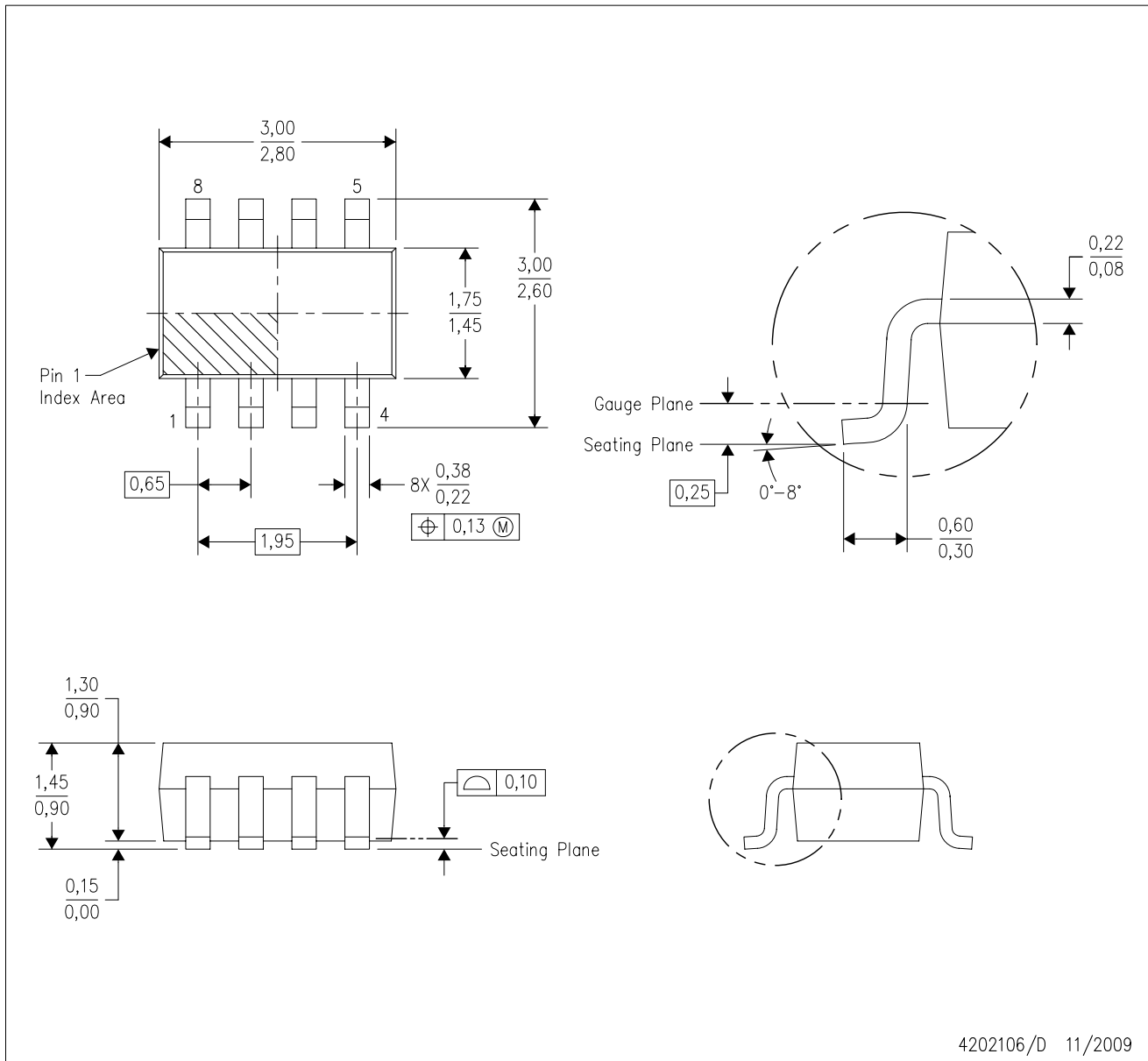


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS22960DCNR	SOT-23	DCN	8	3000	183.0	183.0	20.0
TPS22960RSER	UQFN	RSE	8	3000	183.0	183.0	20.0
TPS22960RSET	UQFN	RSE	8	250	183.0	183.0	20.0

DCN (R-PDSO-G8)

PLASTIC SMALL-OUTLINE PACKAGE (DIE DOWN)



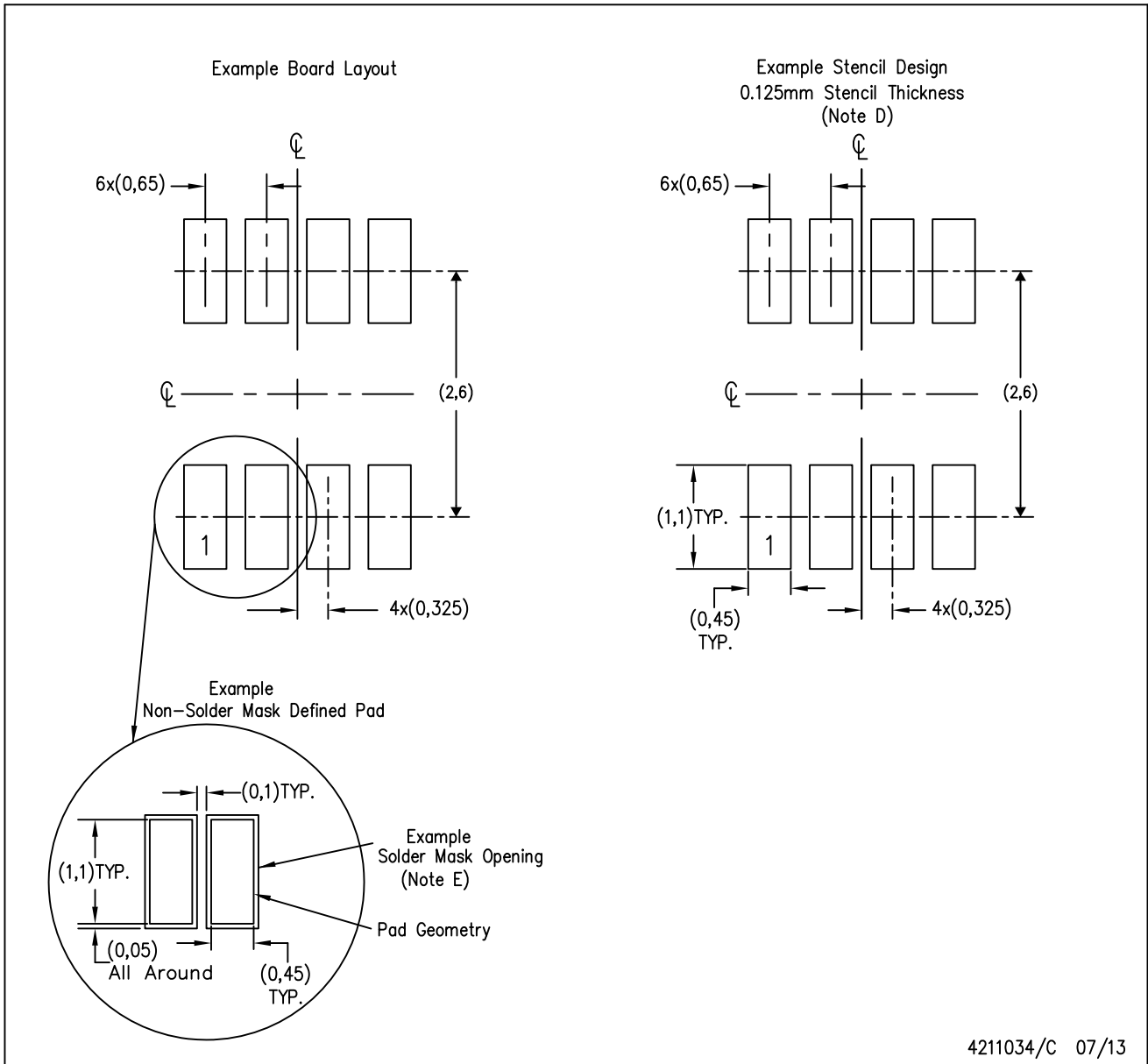
4202106/D 11/2009

- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. Package outline exclusive of metal burr & dambar protrusion/intrusion.
  - D. Package outline inclusive of solder plating.
  - E. A visual index feature must be located within the Pin 1 index area.
  - F. Falls within JEDEC MO-178 Variation BA.
  - G. Body dimensions do not include flash or protrusion. Mold flash and protrusion shall not exceed 0.25 per side.

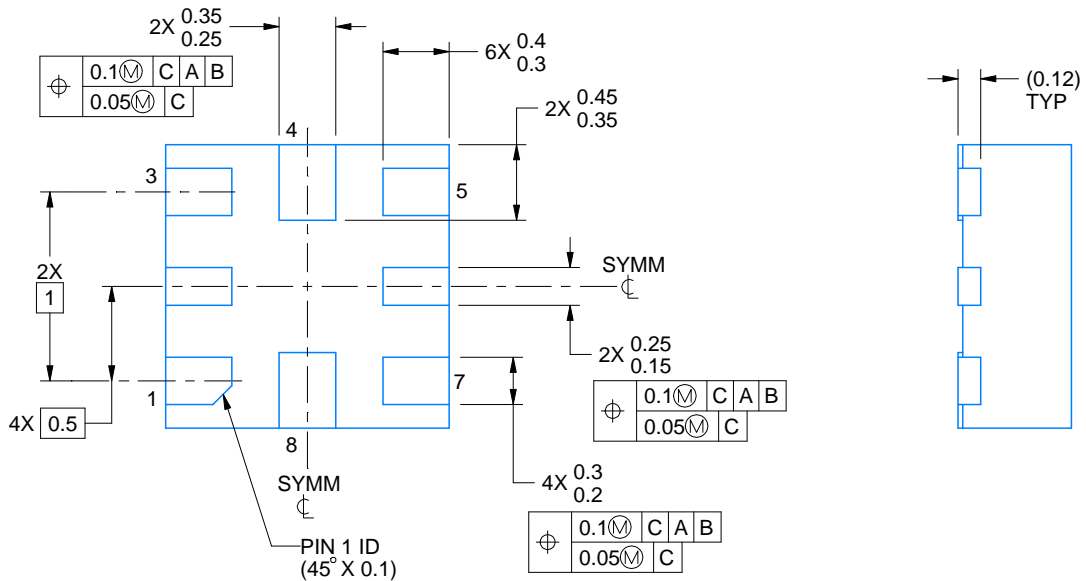
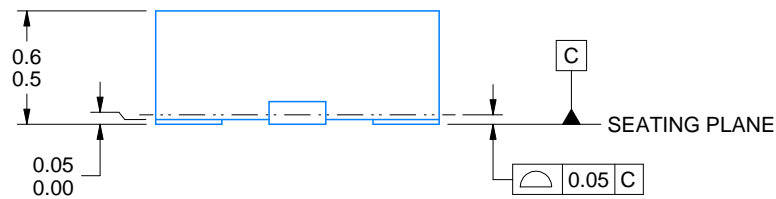
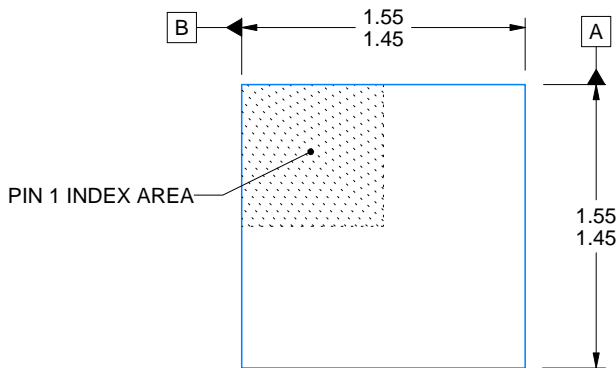
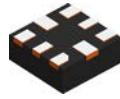


DCN (R-PDSO-G8)

PLASTIC SMALL-OUTLINE PACKAGE (DIE DOWN)



- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. Publication IPC-7351 is recommended for alternate designs.
  - D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525.
  - E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.



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NOTES:

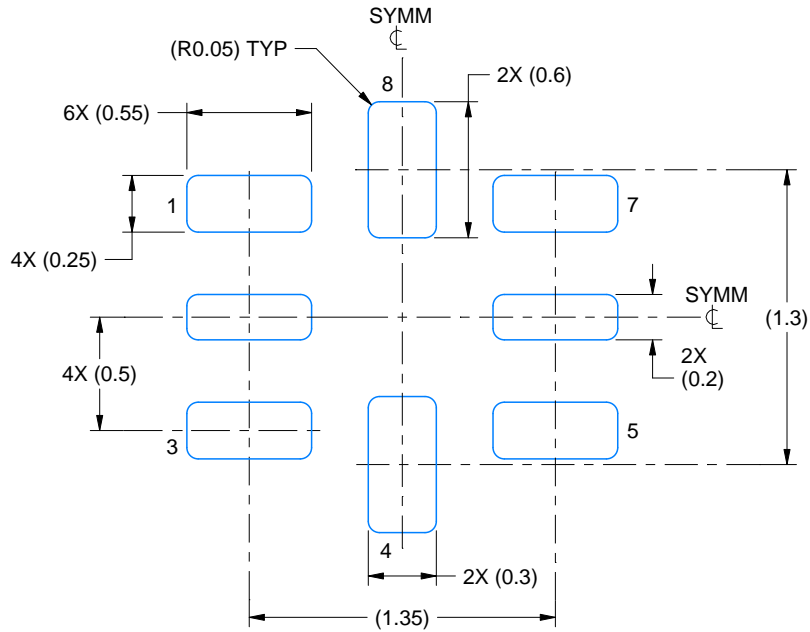
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.

# EXAMPLE BOARD LAYOUT

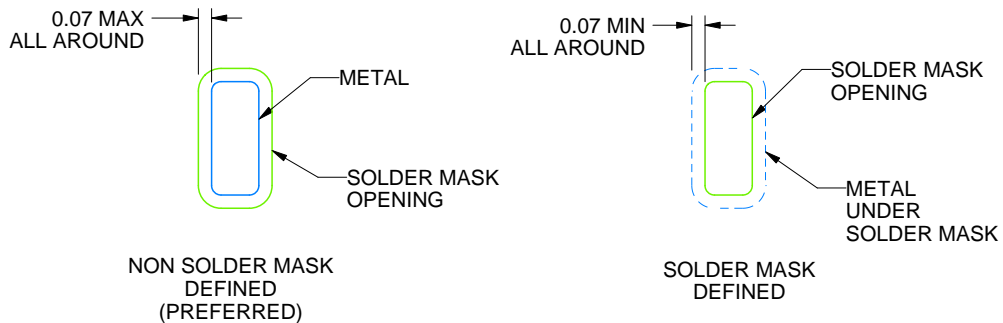
RSE0008A

UQFN - 0.6 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



LAND PATTERN EXAMPLE  
SCALE:30X



SOLDER MASK DETAILS  
NOT TO SCALE

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NOTES: (continued)

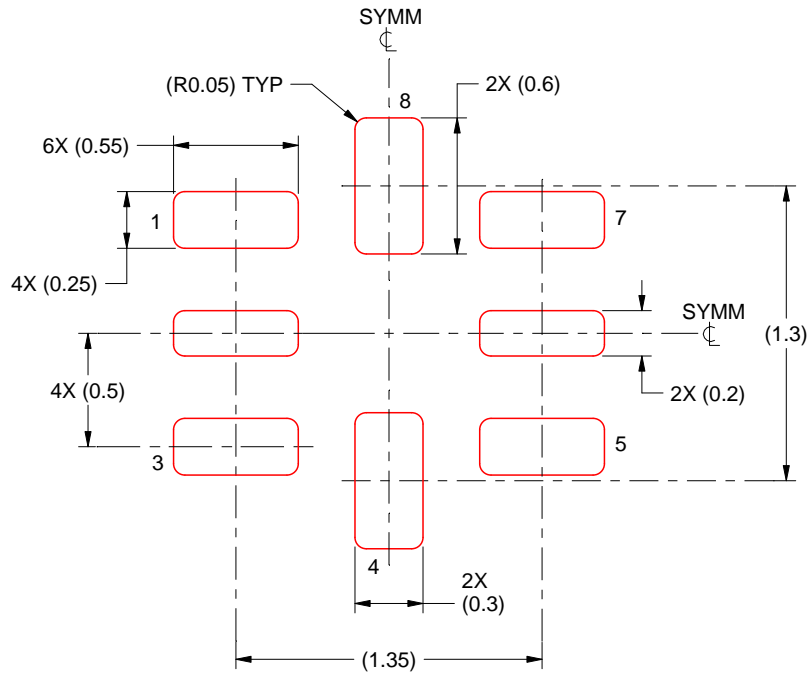
3. For more information, see Texas Instruments literature number SLUA271 ([www.ti.com/lit/slua271](http://www.ti.com/lit/slua271)).

# EXAMPLE STENCIL DESIGN

RSE0008A

UQFN - 0.6 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



SOLDER PASTE EXAMPLE  
BASED ON 0.1 mm THICKNESS  
SCALE: 30X

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NOTES: (continued)

5. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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