User's Guide

LMZ31704 2-Phase Power Module Evaluation Module User's Guide

ABSTRACT

The LMZ31710 device is a 2.95-V to 17-V input, 10-A output, SIMPLE SWITCHER® power module, which integrates the PWM controller, power MOSFETs, shielded inductor, and passives in a low-profile, QFN package. For applications requiring greater than 10 A, it is possible to parallel up to six LMZ31710 devices. This user's guide provides information on the correct usage of the test board and an explanation of the test points and jumpers on the board.

Table of Contents

1 Description

This test board features the LMZ31710 device configured for parallel operation. The test board operates over the entire input voltage range of the LMZ31710 device (2.95 to 17 V) with the option to select a split input power rail. The output voltage can be set to one of four popular values by using a configuration jumper (P4). This board can be configured to accept an external clock to set the switching frequency. Using a jumper, each paralleled LMZ31710 device can be configured to operate in phase with the controller or 180° out-of-phase. Input and output capacitors are included on the board to accommodate the entire range of input and output voltages. Current monitoring test points are available to measure the current of each device. Monitoring test points are provided to allow measurement of the following:

- Efficiency
- Power dissipation
- Input ripple
- Output ripple
- Line and load regulation
- Transient response

Control test points are provided to use the PWRGD, inhibit/UVLO, synchronization (CLK_IN), and slow-start or tracking features.

2 Getting Started

Figure 2-1 and Figure 2-2 highlight the user interface items associated with both the 2× and 4× LMZ31710 parallel test board. The polarized PVIN power terminal blocks are used to connect to the host input supply, and the polarized VOUT power terminal blocks are used to connect to the load. These terminal blocks can accept up to 16 AWG wire. The polarized VBIAS terminal block is used along with the VIN SELECT jumper (P1) when optional split power supply operation is desired. Refer to the *LMZ31710 10-A Module, 2.95-V to 17-V Input and Current Sharing in QFN Package* data sheet for further information on split power supply operation. Refer to Table 2-1 for terminal block numbering for either the 2× or 4× LMZ31710 parallel test board.

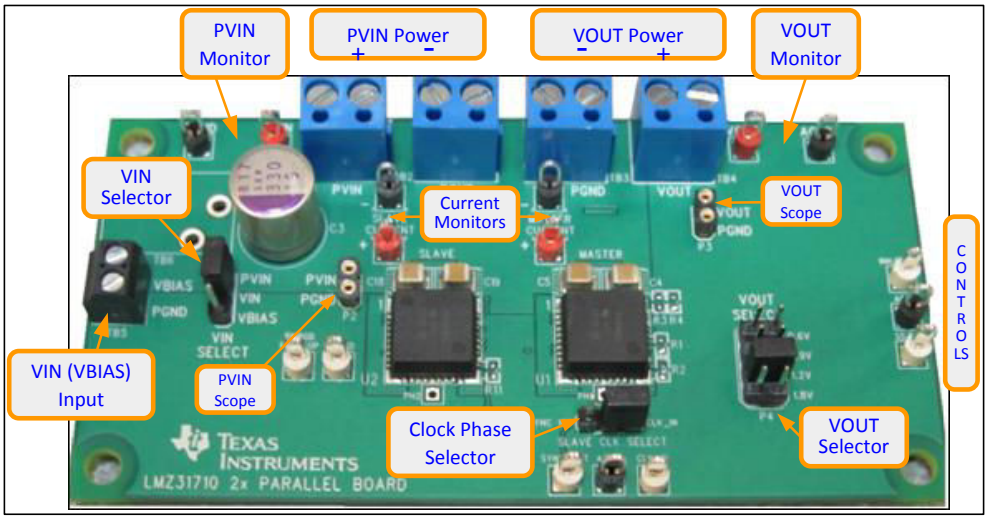


Figure 2-1. 2× LMZ31710 Test Board User Interface

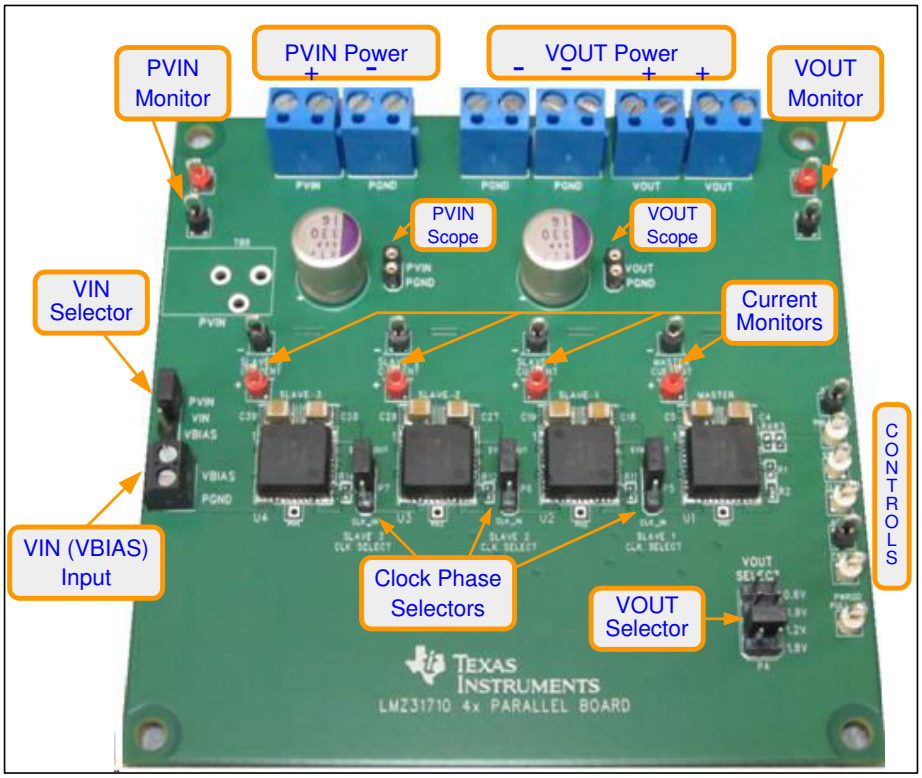


Figure 2-2. 4× LMZ31710 Test Board User Interface

Table 2-1. Terminal Block Numbering

Function	2× LMZ31710	4× LMZ31710
PVIN Power	TB1	TB1
PGND (Input)	TB2	TB2
PGND (Output)	TB3	TB3, TB4
VOUT Power	TB4	TB5, TB6
VBIAS Input	TB5	TB7

The PVIN monitor and VOUT monitor test points located near the power terminal blocks are intended as voltage monitoring points where digital voltmeters can connect to measure PVIN and VOUT.

CAUTION

Do not use these PVIN and VOUT monitoring test points as the input supply or output load connection points. The PCB traces connecting to these test points are not designed to support high currents. High currents can damage the PCB traces.

The PVIN Scope and VOUT Scope test points can be used to monitor PVIN and VOUT waveforms with an oscilloscope. These test points are intended for use with un-hooded scope probes outfitted with a low-inductance ground lead (ground spring) mounted to the scope barrel. The two sockets of each test point are on 0.1-inch centers. The scope probe tip should be connected to the socket labeled PVIN, or VOUT, and the scope ground lead should be connected to the socket labeled PGND.

The current monitor test points located above each LMZ31710 device are intended to be used with digital voltmeters to monitor the current across a 1-mΩ sense resistor located on the bottom of the board. The controls test points located on the perimeter of the board are made available to test the features of the device. Any external connections made to these test points should be referenced to an AGND test point. Refer to Section 3 for more information on the individual control test points.

The VOUT SELECT jumper (P4) is provided for selecting the desired output voltage. Before applying power to the test board, ensure that the jumper is present and properly positioned for the intended output voltage. Always remove input power before changing the jumper settings.

3 Test Point Descriptions

Wire-loop test points and scope probe test points have been provided as convenient connection points for digital voltmeters (DVM) or oscilloscope probes to aid in the evaluation of the test board. Table 3-1 provides a description of each test point.

Table 3-1. Test Point Descriptions

Test Point	Description
AGND	Control and monitor grounds. Reference the DVMs and any signals associated with the control test points to any of the analog ground points.
CLK_IN	Connects to the RT/CLK pin of the LMZ31710 devices. An external clock signal can be applied to this point to synchronize the devices to an appropriate frequency.
INH/UVLO	Connect this point to control ground to inhibit the LMZ31710 devices. Allow this point to float to enable the device. An external resistor divider (R3 and R4) can be connected between this point, control ground, and PVIN to adjust the undervoltage lockout of the device.
PVIN	Input voltage monitor. Connect the DVM to this point to measure efficiency.
PVIN Scope (P2)	Input voltage scope monitor. Connect an oscilloscope to this set of points to measure input ripple voltage.
PWRGD	Monitors the power good signal of the LMZ31710. This is an open-drain signal that requires an external pullup resistor if monitoring is desired. TI recommends a 10-kΩ to 100-kΩ pullup resistor.
PWRGD PULL_UP	Power-good pullup voltage connection point. Connect an external voltage (< 6 V) to this pin to supply a voltage for the PWRGD signal. A 100-kΩ pullup resistor is located on the bottom-side of the board.
SS/TR	Connects to the slow-start connection of the LMZ31710 devices. An external capacitor can be connected from this point to control ground to increase the slow-start time of the devices. This point can also be used as an input for tracking applications.
SYNC_OUT	This output provides a clock signal that is 180° out of phase with the PH node of the LMZ31710 device and can be used to synchronize other devices.
VOUT	Output voltage monitor. Connect DVM to this point for measuring efficiency, line regulation, and load regulation.
VOUT Scope (P3)	Output voltage scope monitor. Connect an oscilloscope to this set of points to measure output ripple voltage and transient response.

4 Operation Notes

To operate the test board using a single power supply, the VIN SELECT jumper (P1) must be in the default PVIN-VIN position as shown in Figure 2-1 and Figure 2-2. In this position, the PVIN and VIN pins of the LMZ31710 devices are connected together. When connected together the input voltage range is 4.5 to 17 V. Refer to the *LMZ31710 10-A Module, 2.95-V to 17-V Input and Current Sharing in QFN Package* data sheet for further information on the input voltage range, UVLO operation, and optional split power supply operation when using an external Vbias supply.

After a valid input voltage is present, the output voltage ramps to the selected value in approximately 1.2 ms. The soft-start time can be increased by adding a SS capacitor to the C12 position on the bottom of the test board. Refer to the *LMZ31710 10-A Module, 2.95-V to 17-V Input and Current Sharing in QFN Package* data sheet for further information on adjusting the soft-start time.

All LMZ31710 devices on the test board must be synchronized to the same frequency. This can be accomplished by either applying an external clock signal to the CLK_IN test point and running the clock to each device, or by setting the frequency of the controller device using the RRT resistor (R2) and running the Sync_Out signal to the remaining target devices. The Clock Phase Selector for each device is used to select either the external clock or the Sync_Out clock signal. The Sync_Out signal is a clock signal that is the same as the switching frequency, but is 180° out of phase. The test boards are set-up to operate at a free-running frequency of 300 kHz. To change the free-running switching frequency, the value of R2 can be changed according to the *LMZ31710 10-A Module, 2.95-V to 17-V Input and Current Sharing in QFN Package* data sheet.

Table 4-1 lists the switching frequency ranges for each of the VOUT selections. Several factors such as duty cycle, minimum on-time, minimum off-time, and current limit influence selection of the switching frequency.

Table 4-1. Switching Frequency Range

Frequency Range		
VOUT (V)	**PVIN = 12 V**	**PVIN = 5 V**
0.6	200 to 250 kHz	200 to 550 kHz
0.9	200 to 300 kHz	200 to 800 kHz
1.2	200 to 450 kHz	200 to 1000 kHz
1.8	300 to 600 kHz	300 to 1200 kHz

5 Current Limitations

When operating LMZ31710 devices in parallel, the maximum output current the solution can provide must be calculated using Equation 1. Due to internal variances between devices, the amount of output current must be de-rated to ensure none of the devices operate above the maximum output current of a single device (10 A). See Figure 5-1 for typical current balancing between four LMZ31710 devices.

$$IOUTmax = 0.9 \times (n \times 10)\ (A) \quad (1)$$

where

- n is the number of LMZ31710 devices being paralleled.

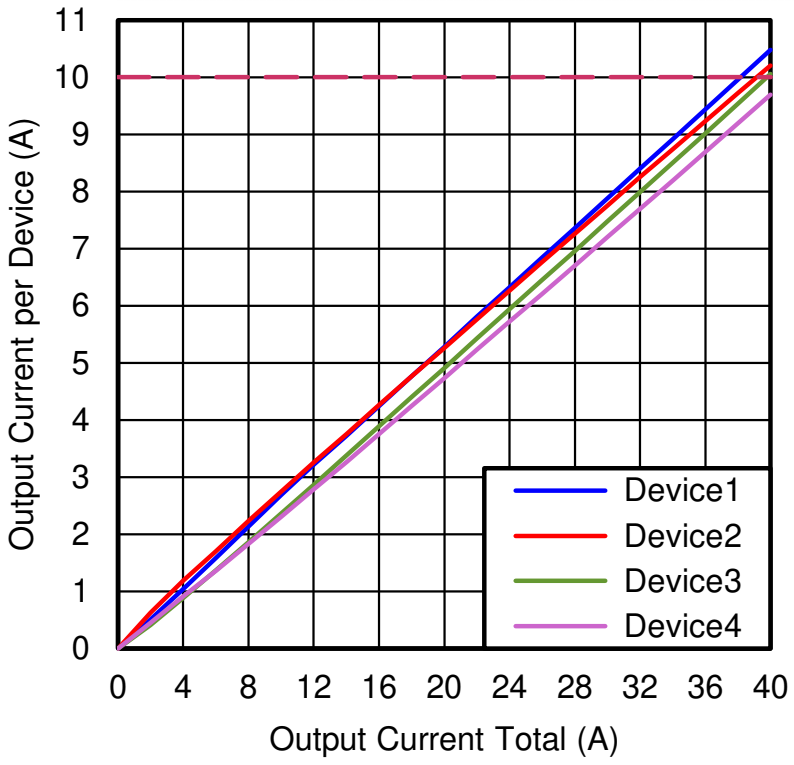


Figure 5-1. Typical Current Balancing

6 Performance Data

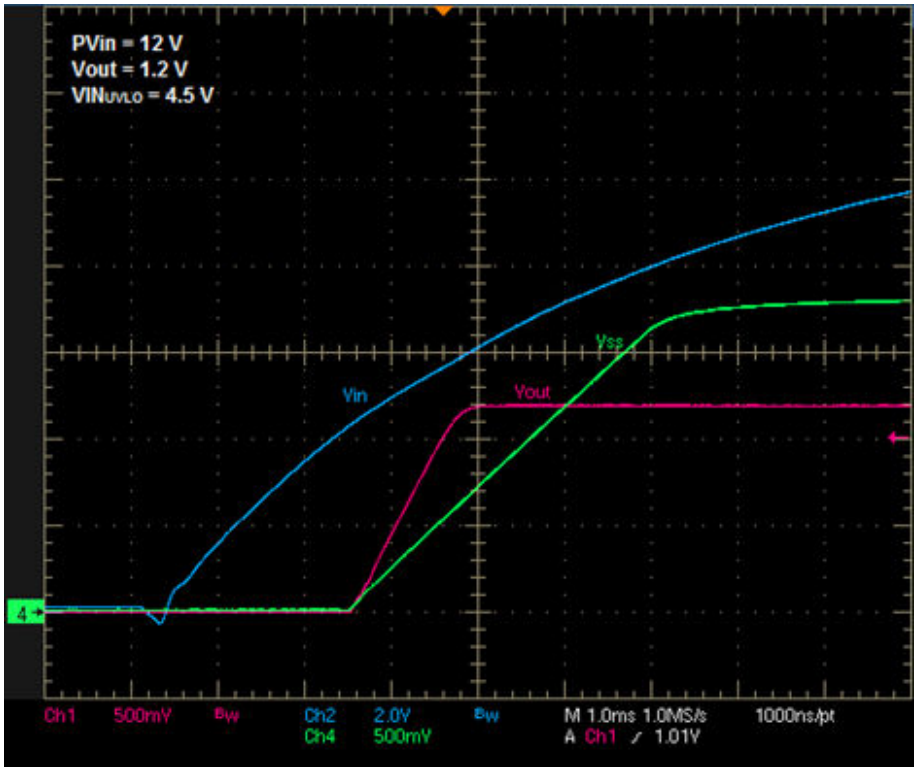


Figure 6-1. UVLO Start-Up Waveform

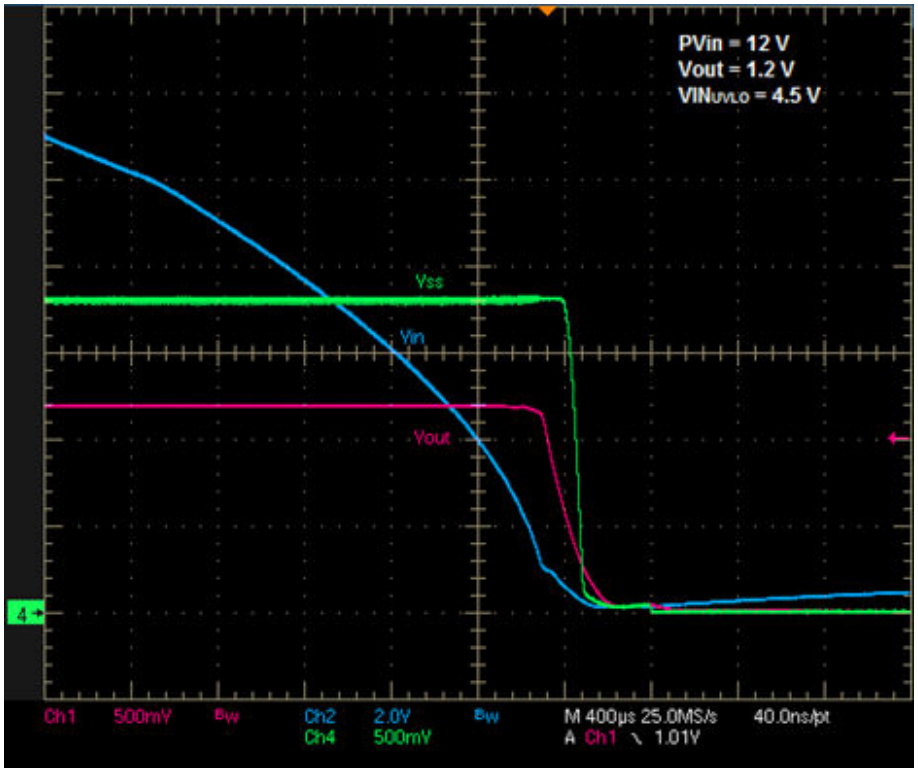


Figure 6-2. UVLO Shutdown Waveform

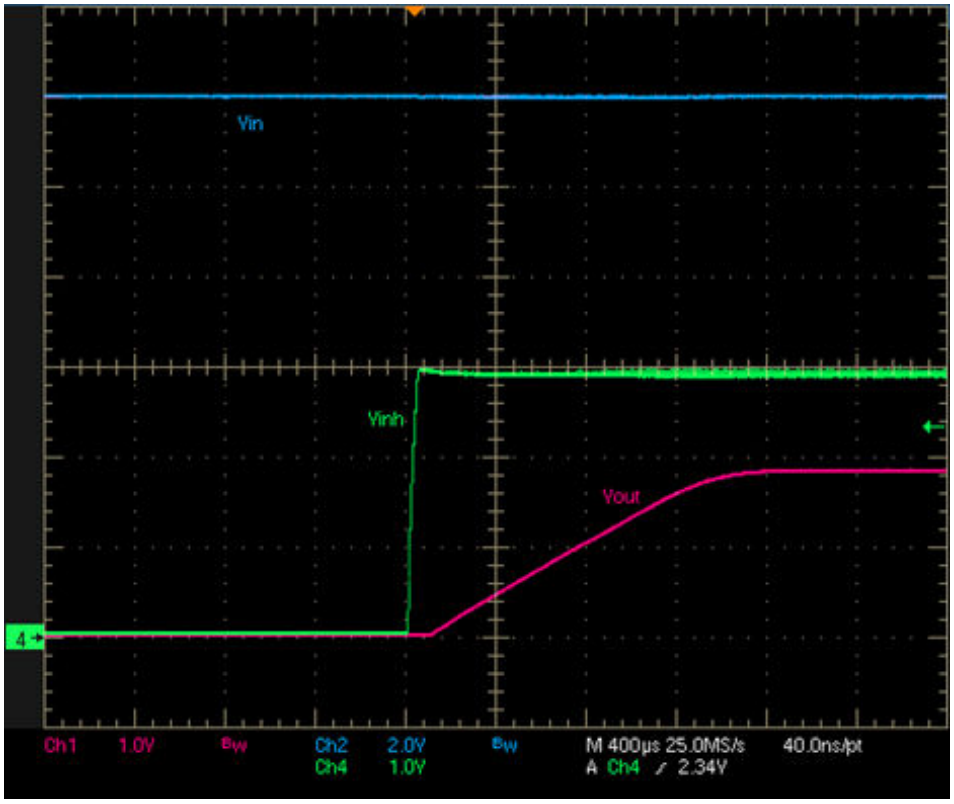


Figure 6-3. INH Start-Up Waveform

Figure 6-4. INH Shutdown Waveform

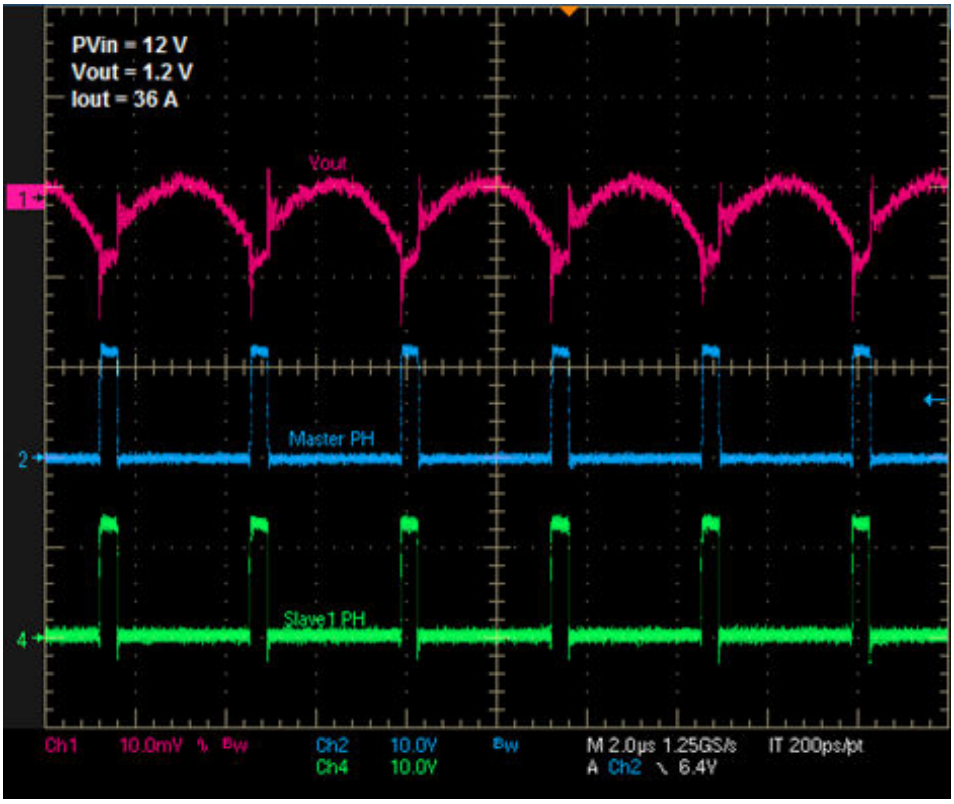


Figure 6-5. Output Voltage Ripple – In-Phase

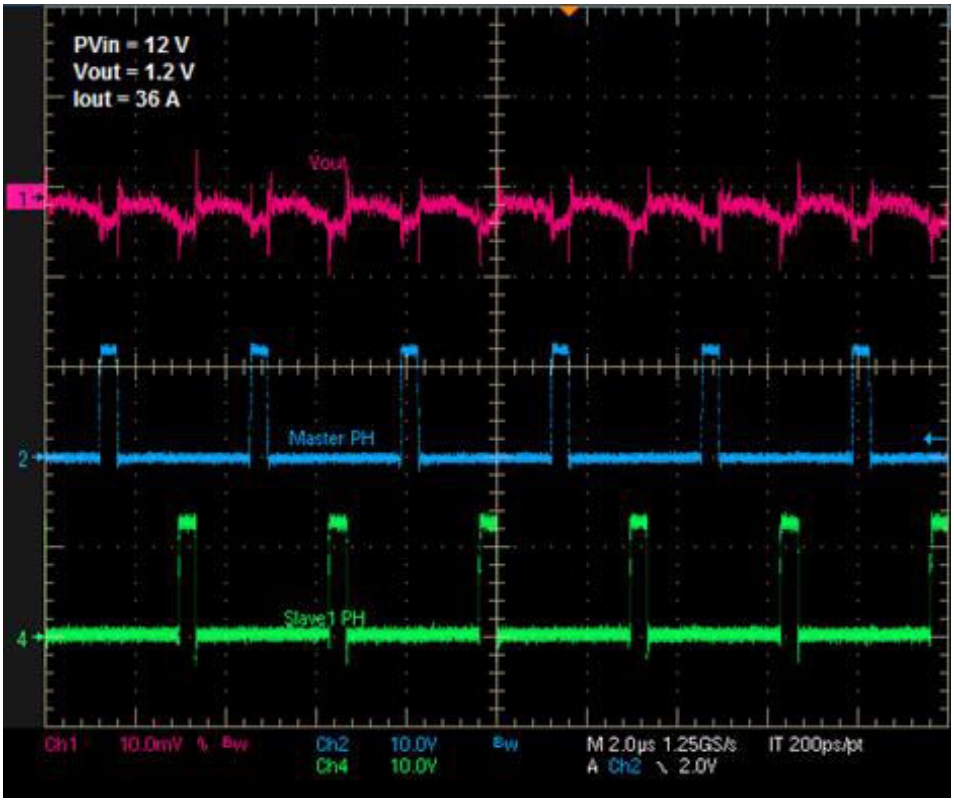


Figure 6-6. Output Voltage Ripple – 180° Out-of-Phase

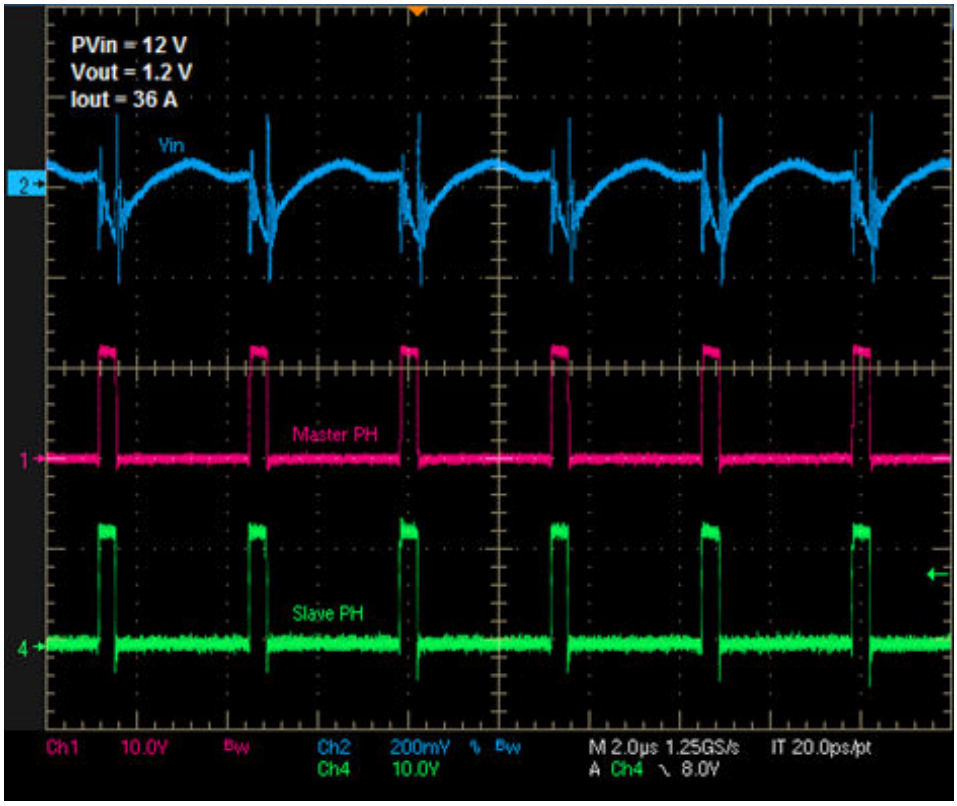


Figure 6-7. Input Voltage Ripple – In-Phase

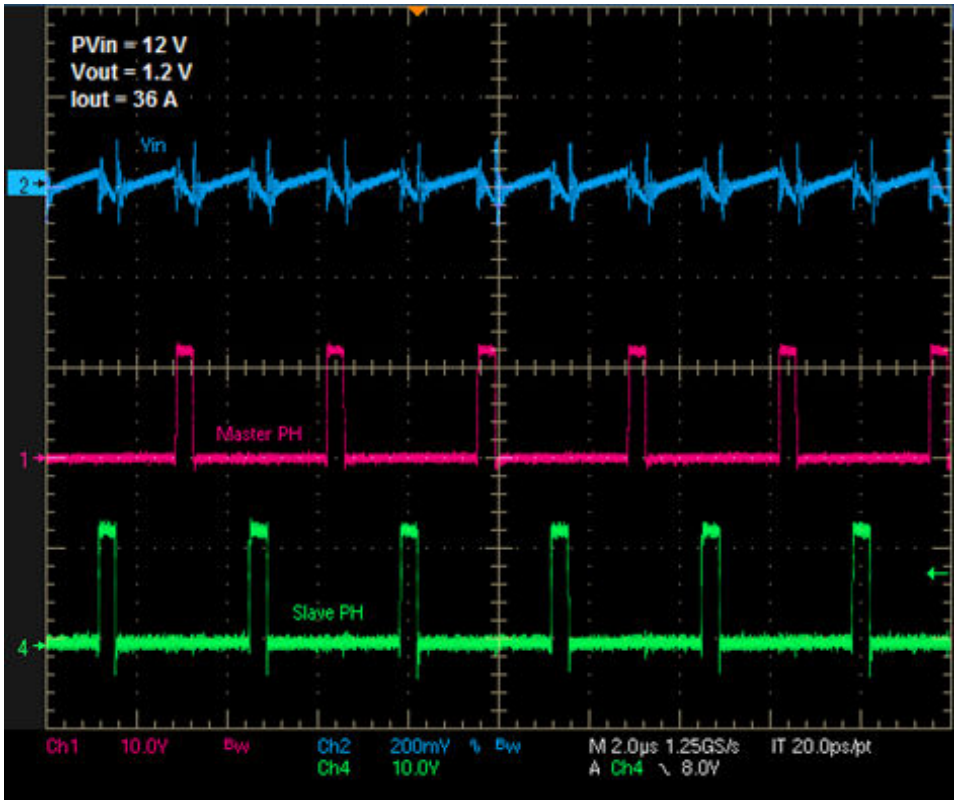


Figure 6-8. Input Voltage Ripple – 180° Out-of-Phase

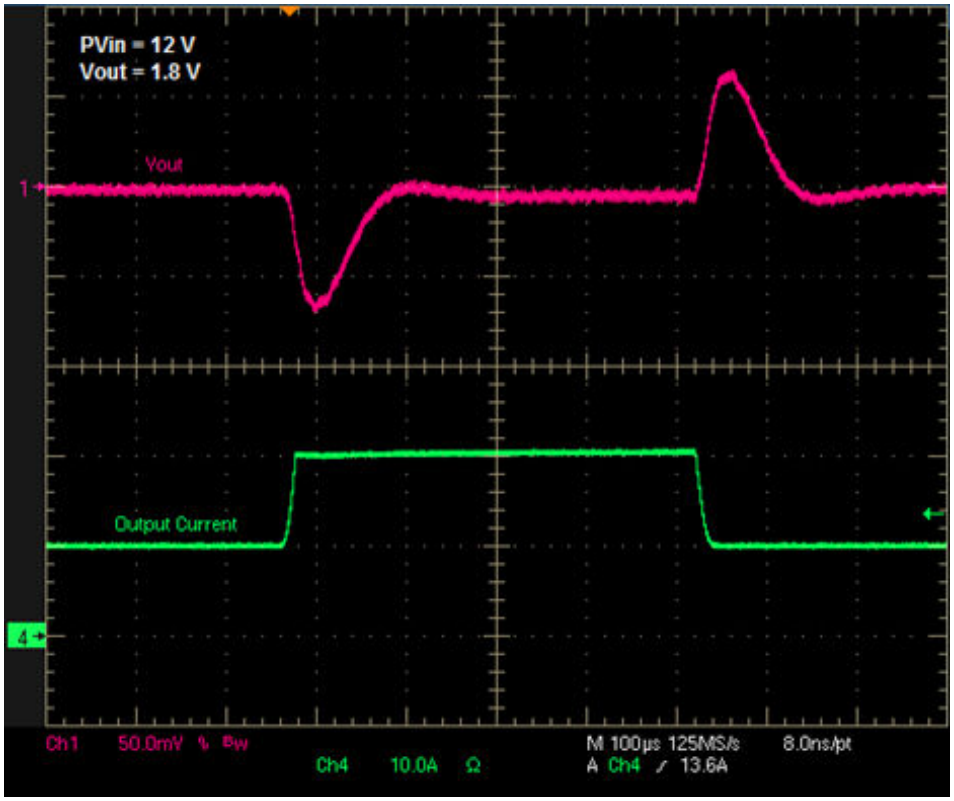
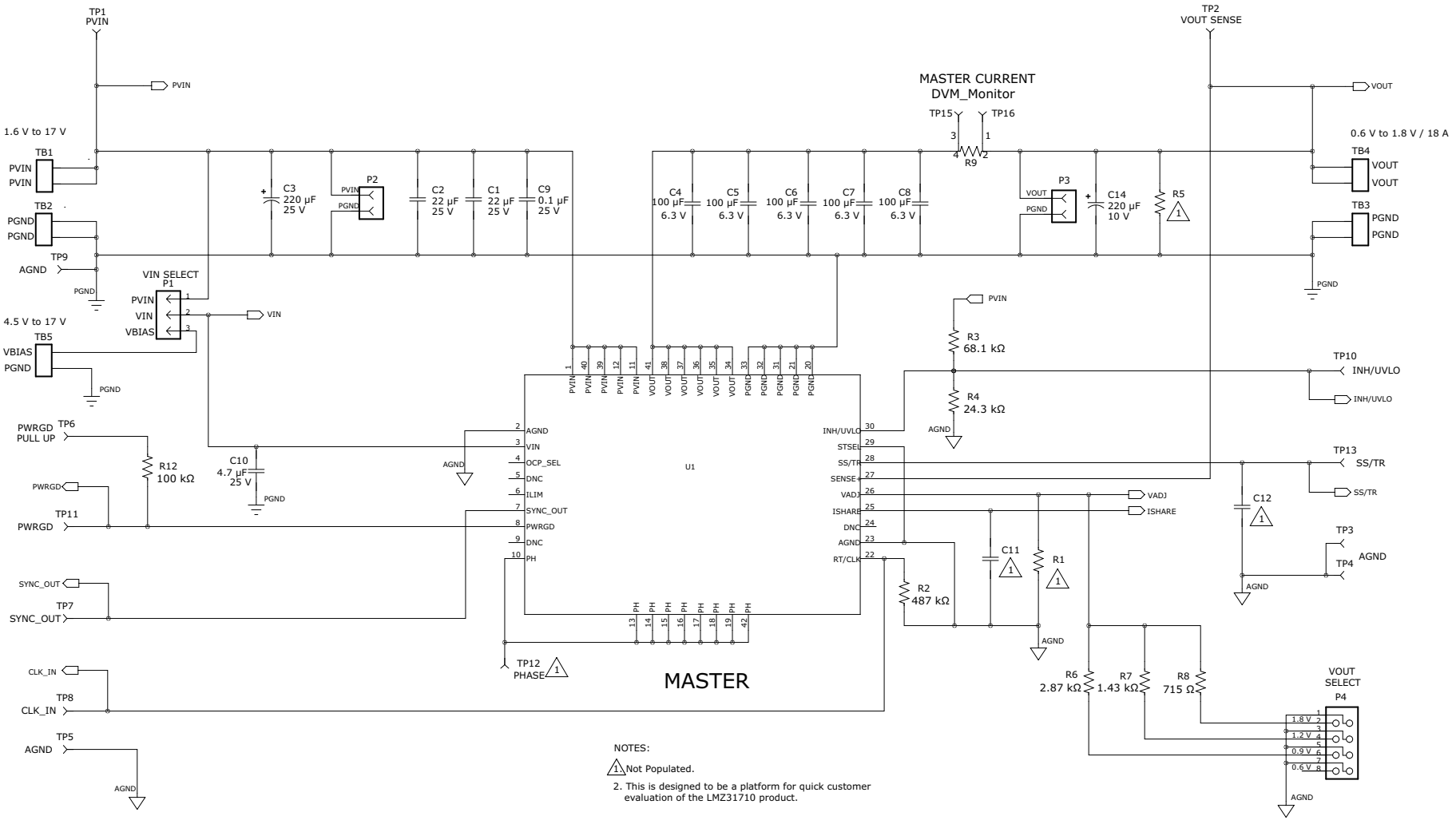


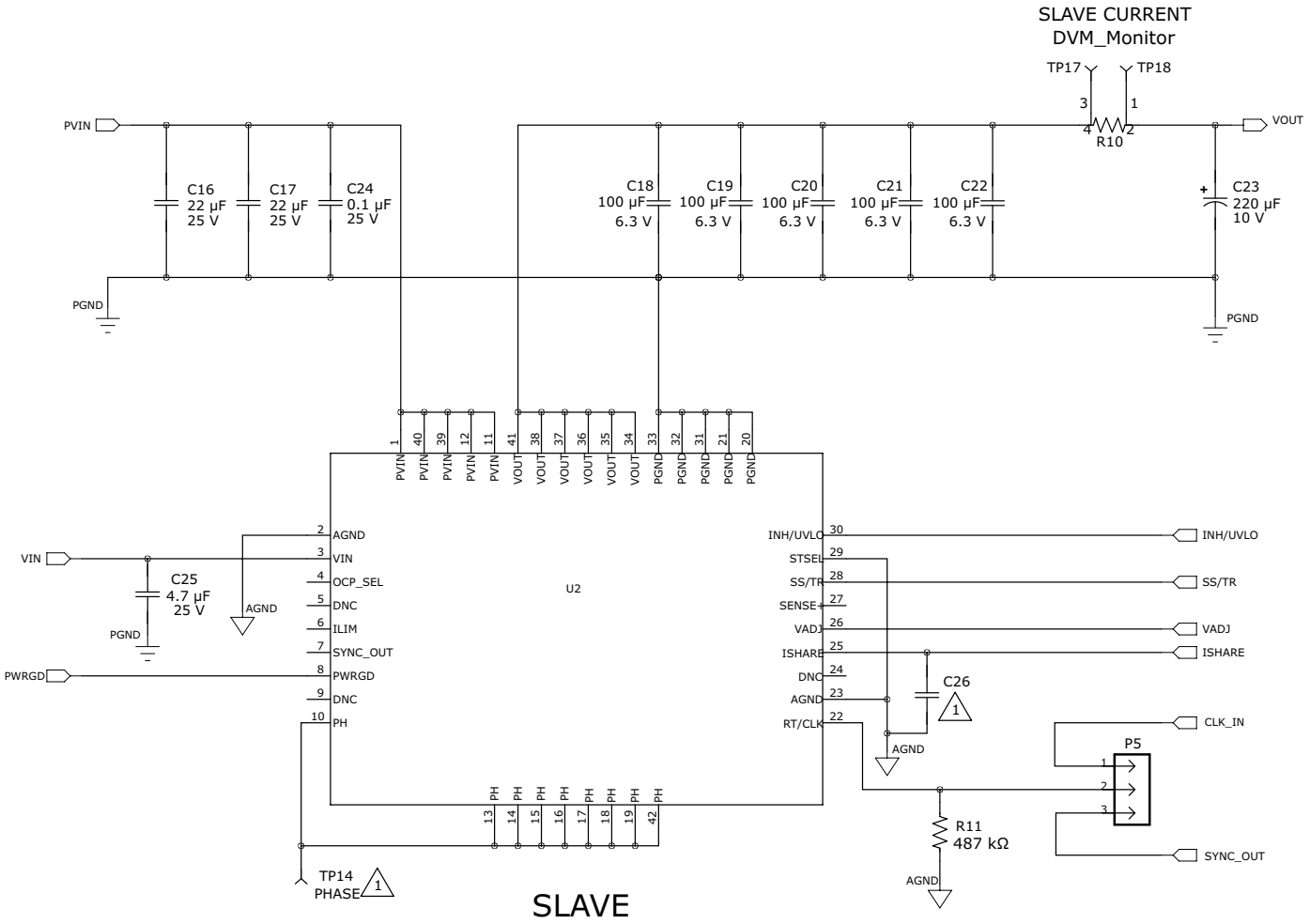
Figure 6-9. Transient Response – 10-A Load Step (1 A/µs)

7 2× Parallel Bill of Material

RefDes	Part Type	Value
C1, C2, C16, C17	C1210	22 µF
C4, C5, C6, C7, C8, C18, C19, C20, C21, C22	C1210	100 µF
C9, C24	C0805	0.1 µF
C10, C25	C0805	4.7 µF
C11, C12, C26	C0805	DNL
C3	CAP_ALUM_FC-A	220 µF
C14, C23	CAP_POSCAP_D	220 µF
P1, P5	MALE HEADER_1X3	PEC03SAAN
P2, P3	FEMALE HEADER_1X2	SOCKET 2 PIN
P4	MALE HEADER_2X4	PEC04DAAN
R1	R0402	NOT POPULATED
R2, R11	R0402	487 k
R3	R0402	68.1 k
R4	R0402	24.3 k
R5	R0805	NOT POPULATED
R6	R0603_1%	2.87 k
R7	R0603_1%	1.43 k
R8	R0603_1%	715 Ω
R9, R10	57-WSL3637	R001R 1%
R12	R0603	100 k
TB1, TB2, TB3, TB4	TBLK_15A_2X5.1MM	ED120/2DS
TB5	TBLK_6A_2X3.5MM	ED555/2DS
TB6	CONN_DC_PJ-102AH	PJ-102AH
TP6, TP7, TP8, TP10, TP11, TP13	TP-5012-WHITE	5012
TP1, TP2, TP15, TP17	TP-5010-RED	5010
TP3, TP4, TP5, TP9, TP16, TP18	TP-5011-BLACK	5011
TP12, TP14	TP-038	STD
U1, U2	LMZ31710RVQ	LMZ31710RVQ

8 2× Parallel Schematic





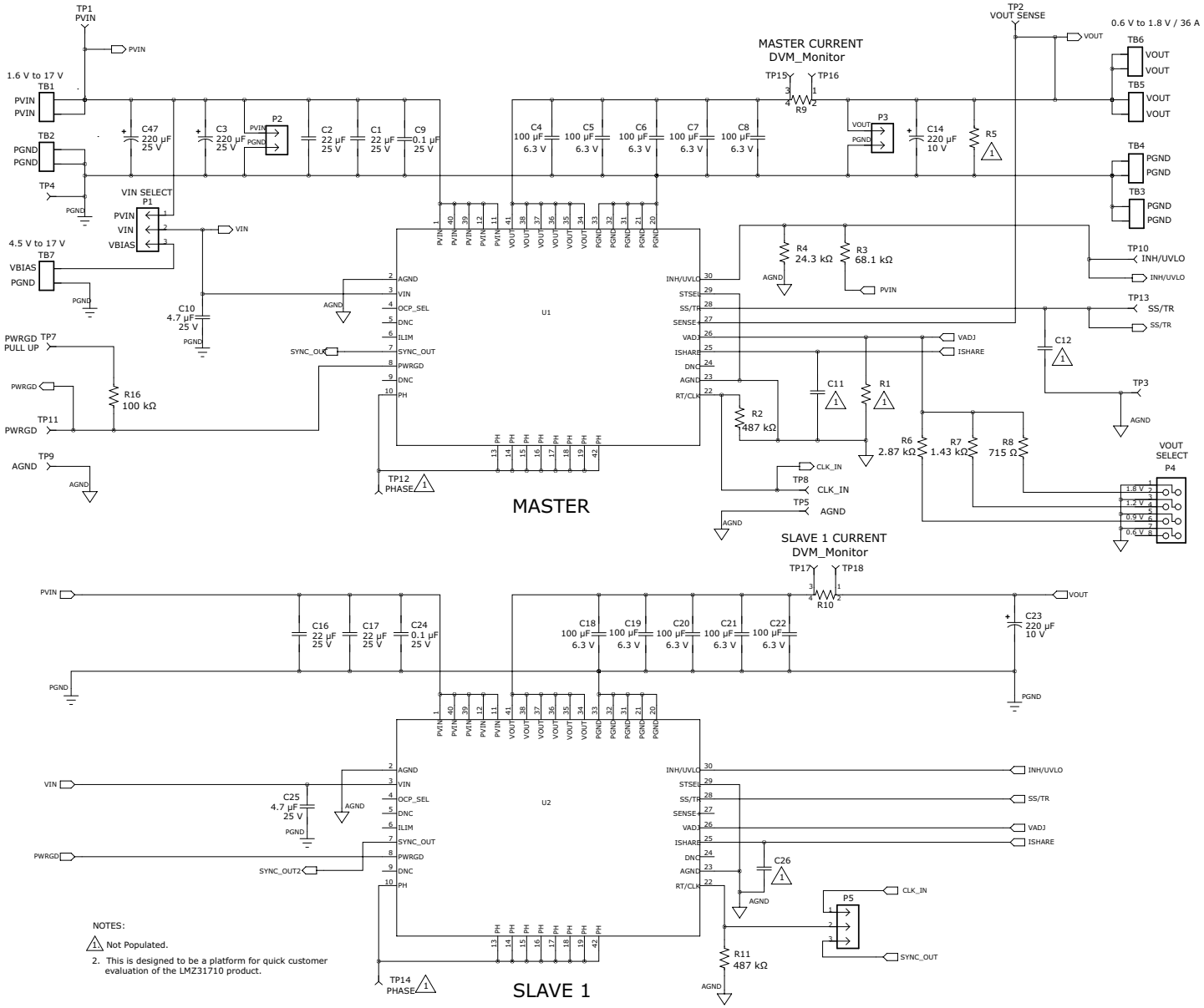
NOTES:

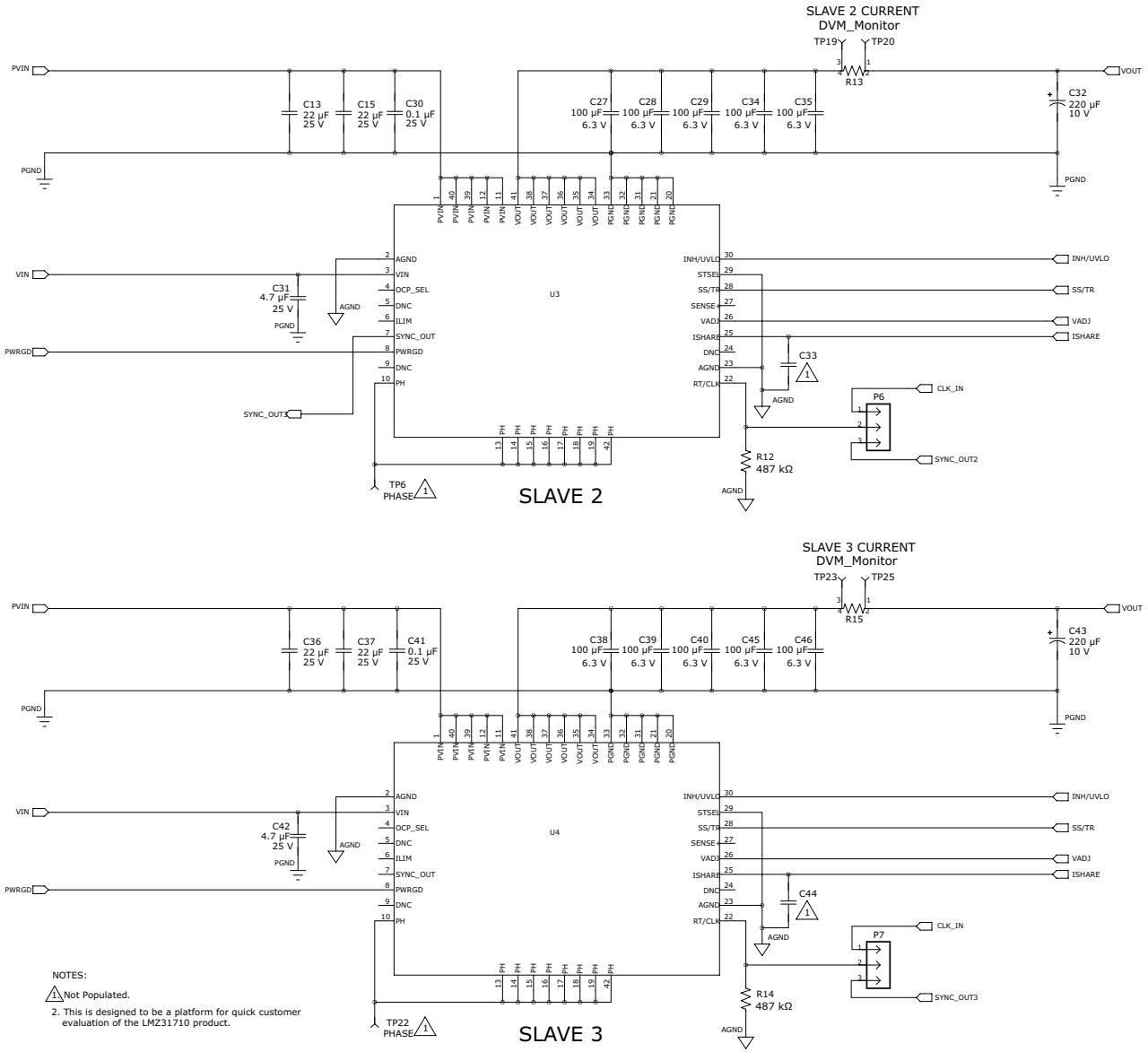
1. Not Populated.
2. This is designed to be a platform for quick customer evaluation of the LMZ31710 product.

9 4× Parallel Bill of Material

RefDes	Part Type	Value
C1, C2, C13, C15, C16, C17,C36, C37	C1210	22 µF
C4, C5, C6, C7, C8, C18, C19, C20, C21, C22, C27, C28, C29, C34,C35, C38, C39, C40, C45, C46	C1210	100 µF
C9, C24, C30, C41	C0805	0.1 µF
C10, C25, C31, C42	C0805	4.7 µF
C11, C12, C26, C33, C44	C0805	DNL
C3, C47	CAP_ALUM_FC-A	220 µF
C14, C23, C32, C43	CAP_POSCAP_D	220 µF
P1, P5, P6, P7	HEADER_1X3	PEC03SAAN
P2, P3	HEADER_1X2	NOT POPULATED
P4	HEADER_2X4	PEC04DAAN
R1	R0402	NOT POPULATED
R2, R11, R12, R14	R0402	487 k
R3	R0402	68.1 k
R4	R0402	24.3 k
R5	R0805	NOT POPULATED
R6	R0603_1%	2.87 k
R7	R0603_1%	1.43 k
R8	R0603_1%	715 Ω
R9, R10, R13, R15	57-WSL3637	R001R 1%
R16	R0603	100k
TB1, TB2, TB3, TB4, TB5, TB6	TBLK_15A_2X5.1MM	ED120/2DS
TB7	TBLK_6A_2X3.5MM	ED555/2DS
TP1, TP2, TP15, TP17, TP19, TP23	TP-5010-RED	5010
TP3, TP4, TP5, TP9, TP16, TP18, TP20, TP25	TP-5011-BLACK	5011
TP7, TP8, TP10, TP11, TP13	TP-5012-WHITE	5012
TP6, TP12, TP14, TP22	TP-038	STD
U1, U2, U3, U4	LMZ31710RVQ	LMZ31710RVQ

10 4× Parallel Schematic





11 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision * (February 2014) to Revision A (January 2022)	Page
• Updated the numbering format for tables, figures, and cross-references throughout the document.	2
• Updated the user's guide title	2

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