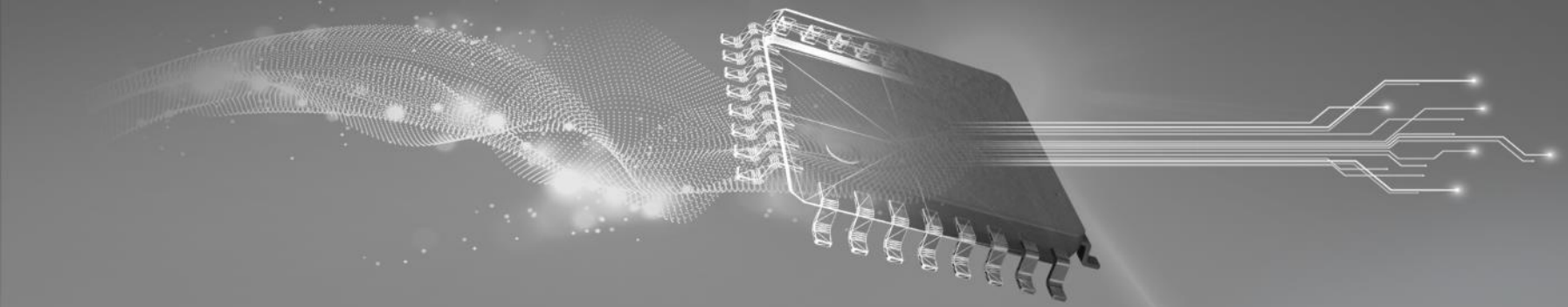
TI TECH DAYS



Getting started with the new PSpice® for TI design and simulation tool

Ian Williams

APP – LP – LDO

Texas Instruments

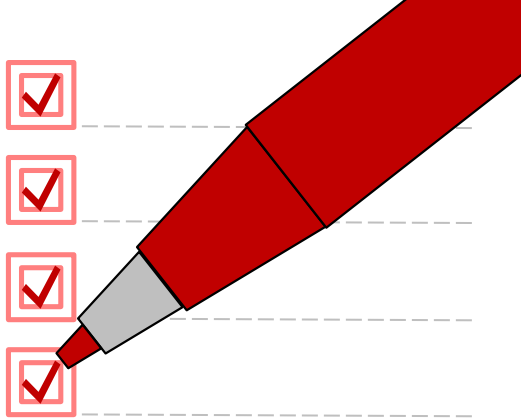
About me – Ian Williams

Business lead, Low-Voltage LDOs

- **Career**
  - BSEE University of Texas at Dallas, 2009
  - TI since 2009, LDO since July 2020
- **Expertise**
  - 11 years working with various types of amplifiers
  - Co-creator of GWL amplifier SPICE model architecture
  - Co-creator of TI Precision Labs – Op Amps
- **Fun fact**
  - Big music guy – have performed at festivals, DJ'd at clubs and on FM radio, and even met my wife at Coachella 2013

Agenda

- TI simulation tools overview **– 10 min.**
- PSpice® for TI deep dive **– 10 min.**
  - Features and limitations
  - Built-in model library
- Setup and simulation examples **– 25 min.**
  - Operational amplifier: OPA211
  - Power supply: TPS7A52
  - Modeling Application: Power MOSFET
- Additional resources



???

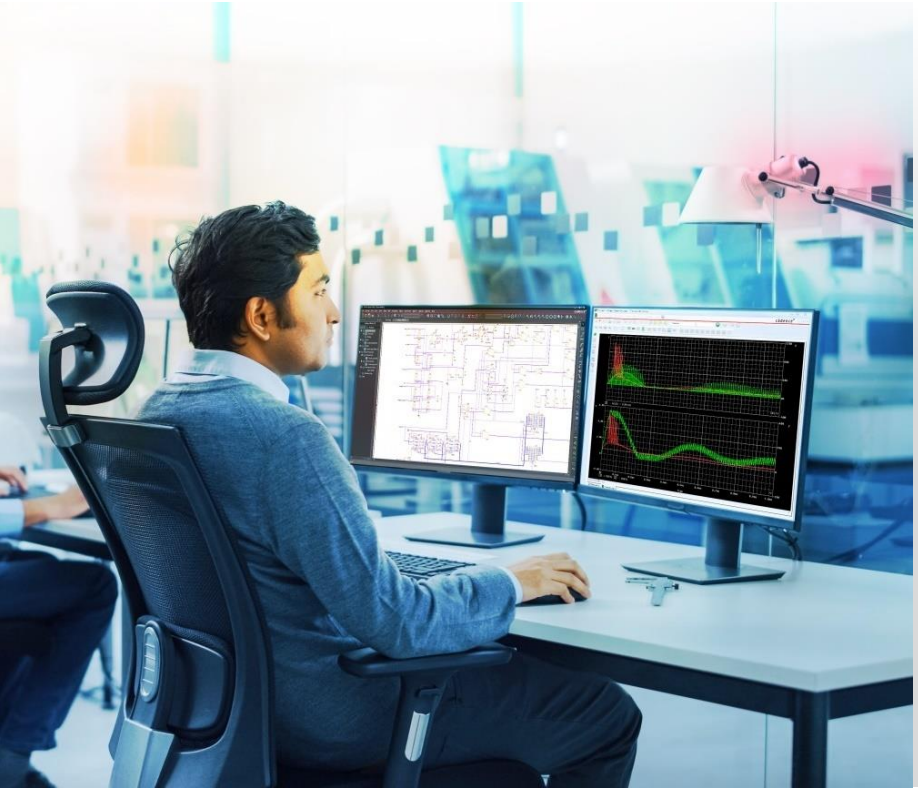
Please ask your questions in the chat!

Part 1
TI simulation tools overview

Tip: SPICE stands for “Simulation Program with Integrated Circuit Emphasis”

Time for some audience participation…

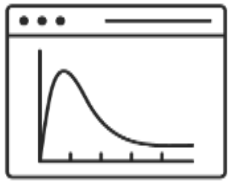
Introducing PSpice® for TI



PSpice for TI will help engineers speed time to market and reduce development costs, delivering:

- **Full-featured simulation of entire systems.**
  - Advanced capabilities, including Monte Carlo and worst-case analysis.
  - Synchronized library of >5,700 models and counting.
  - No design size limitations.
  - Easy transition to layout and prototype.
- **Integrated design resources.**
  - Quick access to TI product information.
  - No need to manually upload new TI models.

Why is TI partnering with Cadence?



Short design timelines

Today's design engineers must produce accurate designs on tight deadlines — in many cases, reducing the prototyping and evaluation phases of their designs.

Growing demand

There is an increased need for simulation software to test new design concepts, accelerate product development and demonstrate regulatory compliance.

Source: ABI Research

Desire for more advanced simulation

Existing simulation tools in the market lack advanced analysis capabilities, model portability and flexibility, and easy library synchronization.

"Tools that are intuitive and include system-level simulation capabilities can cut the development time and speed time to market." – Kevin Anderson, Omdia

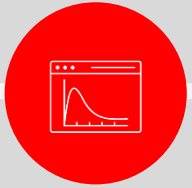
Is PSpice for TI replacing other TI tools?

Fundamentals & skill-building

- Educational e-books
- Technical articles
- TI Precision Labs
- Power Supply Design Seminars (PSDS)
- Additional videos at training.ti.com

Investigation & brainstorming

- Easy part selection on TI.com
- Reference designs for specific applications
- Application notes and technical white papers



Design & simulation

- Evaluation modules
- WEBENCH® Power Designer
- Filter Design Tool
- Analog Engineer's Calculator, Circuit Cookbooks & Pocket Reference
- TINA-TI™

PSpice® for TI

Design support

- e2e.ti.com
- Forums for expert answers to technical questions

PSpice for TI vs. TINA-TI

	PSpice for TI	TINA-TI
Analysis / simulation		
AC, Noise, BIAS point, DC sweep, Transient, Fourier	**Yes**	**Yes**
Variable sweeps	**Temperature, component, parametric**	**Temperature, component**
Monte Carlo analysis	**Yes**	**No**
Worst case analysis	**Yes**	**No**
Libraries / components		
Internal libraries	**~5700**	**~1300**
Automatic library updates	**Yes**	**No**
Built-in modeling application	**Yes**	**No**
Schematics		
Create hierarchical schematic	**Yes**	**No**
Multipage schematics	**Yes**	**No**

Part 2
PSpice for TI deep dive

Tip: PSpice for TI runs offline!

Software features and limitations FAQ

Q. Does PSpice for TI work offline?

A. Yes, an internet connection is not required to run.

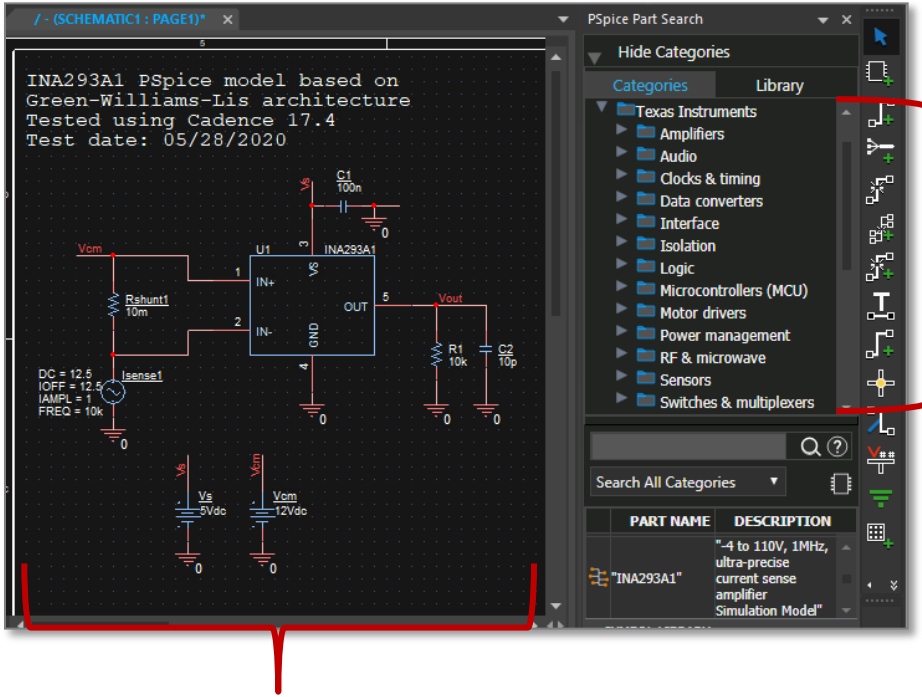
Q. Is there a maximum number of nodes?

A. No, there are no design size limitations. You can also use multi-page schematics and hierarchical blocks.

Q. Are there any other limits to be aware of?

A. Yes. The tool is designed primarily as a SPICE simulation environment for use with the built-in TI models. If third-party models are imported, then only three nodes can be probed simultaneously.

Built-in TI model library

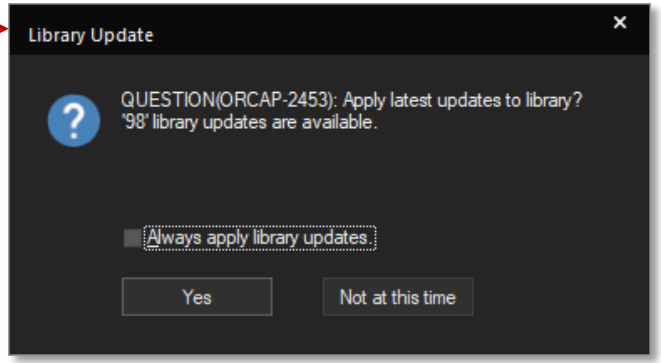


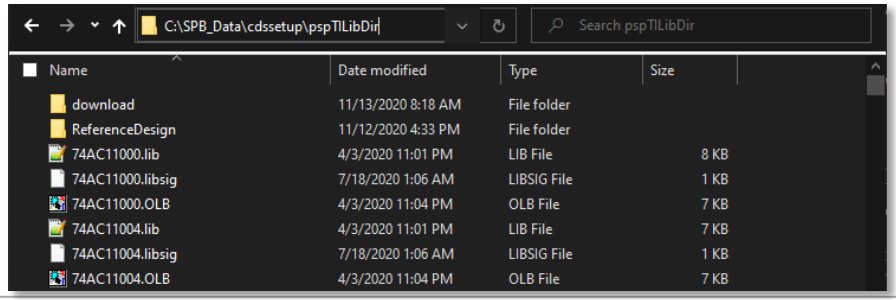
Matches the product tree on TI.com

Includes device-specific test benches
To accelerate your development

How do I update the TI model library?

- Updates to the model library are automatically detected and performed at software startup.
  - The user can choose not to update.
- The model library is installed locally on the user's hard drive. Models can be copied and imported into other tools if desired.
  - Location: **C:\SPB_Data\cdssetup\pspTILibDir**





Are models editable?

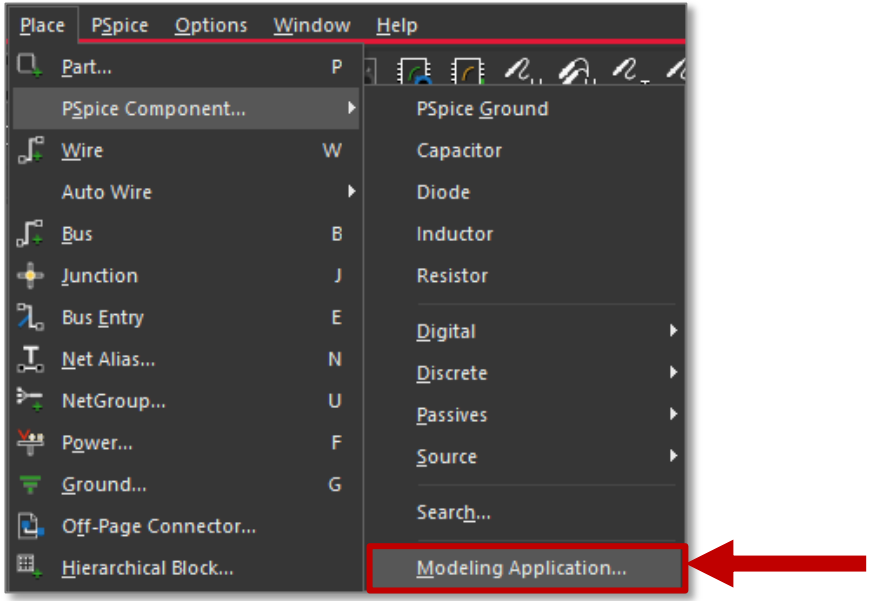
- Models are text files and may be edited with a text editor (I recommend Notepad++) from the library directory
  - **Note:** editing TI models breaks their signature, causing the tool to treat them as 3rd-party
- Some models have user-editable parameters. Editing these **does not** break signature.
- If you edit a model and save it in the same location, it will get over-written during the next library update.

```
.SUBCKT 74AC11000 Y A B VCC AGND
XU1 Y A B VCC AGND LOGIC_GATE_2PIN_OD_LVC_2i_NAND_PP_CMOS_74AC11000
.ENDS
.SUBCKT LOGIC_GATE_2PIN_OD_LVC_2i_NAND_PP_CMOS_74AC11000 OUT A B VCC GND
.PARAM VCC_ABS_MAX = 7
.PARAM VCC_MAX = 5.5
.PARAM RA = 220000000
.PARAM RB = 220000000
.PARAM CA = 3.5e-12
.PARAM CB = 3.5e-12
.PARAM ROEZ = 104.99999999999999
.PARAM COEZ = 3.5e-12
RA  A  GND {RA}
RB  B  GND {RB}
CA  A  GND {CA}
CB  B  GND {CB}
XUA NA A VCC GND LOGIC_INPUT_LVC_2i_NAND_PP_CMOS_74AC11000
XUB NB B VCC GND LOGIC_INPUT_LVC_2i_NAND_PP_CMOS_74AC11000
XUG NA NB NOUTG VCC GND LOGIC_FUNCTION_2_LVC_2i_NAND_PP_CMOS_74AC11000
XOUTPD NOUTG NOUTTPD VCC GND TPD_LVC_2i_NAND_PP_CMOS_74AC11000
XUOUT NOUTTPD NOUT_INT VCC GND LOGIC_PP_OUTPUT_LVC_2i_NAND_PP_CMOS_74AC11000
XICC VCC GND NVIOUT LOGIC_ICC_LVC_2i_NAND_PP_CMOS_74AC11000
SICC VCC GND VCC GND SW1
```

Model file example

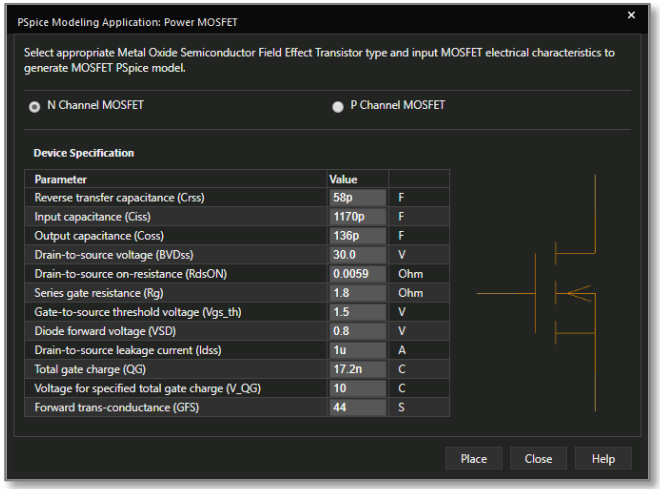
Modeling application

- Used to add customizable, parameterized components to your design:
  - Power MOSFETs
  - Power diodes
  - Passives with parasitics
  - Independent sources
  - Switches
  - Transformers
- Click *Place* → *PSpice Component…* → *Modeling Application* in the top menu bar
- **Note:** these components ***do not*** trigger the probe limit

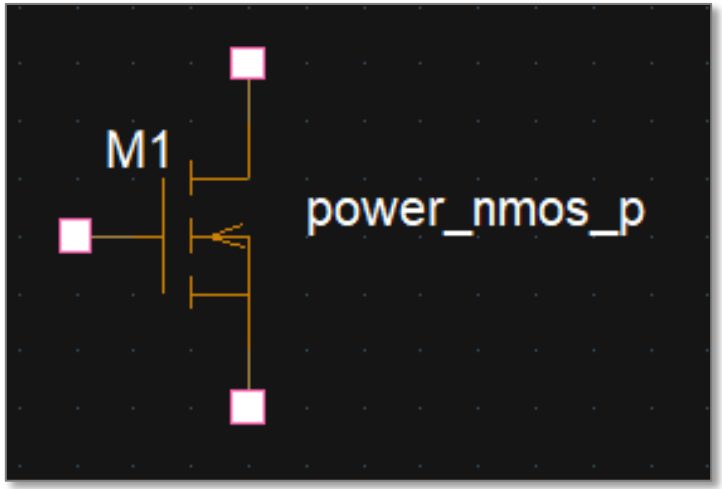


Modeling application, cont.

- A simple UI opens for each type of component with editable fields
- Customize each parameter to your liking, then click *Place* to drop in schematic
  - **Note:** Device parameters can still be edited from their properties once in the schematic



Power MOSFET window



Power NMOS in schematic

Additional included model libraries

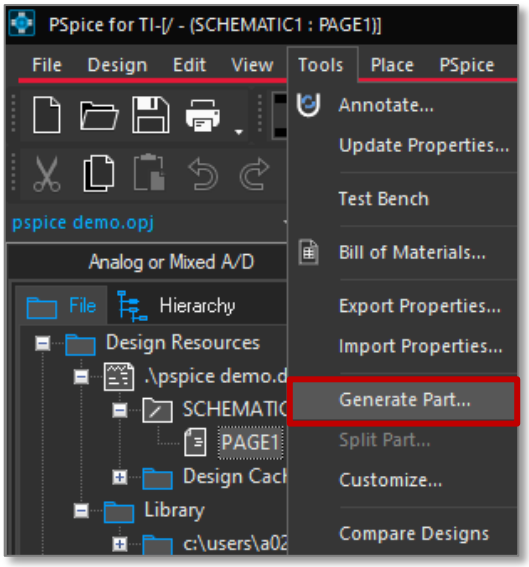
- These standard PSpice libraries are also included:

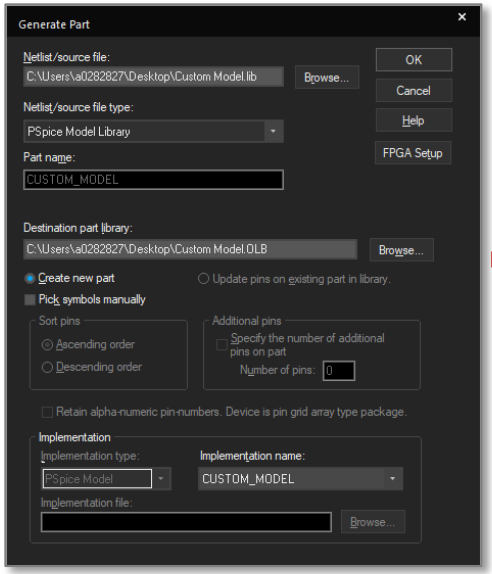
Library	Description
ABM	Analog behavioral models for various math functions
ANALOG	Passives, dependent sources, switches, transmission lines
BREAKOUT	Customizable versions of many device types
DIG_MISC	Digital timing control, pull-up / pull-down resistors
DIG_PRIM	Logic gates, flip-flops
SOURCE	Independent voltage and current sources
SPECIAL	Parameters, simulation control, library management, utilities

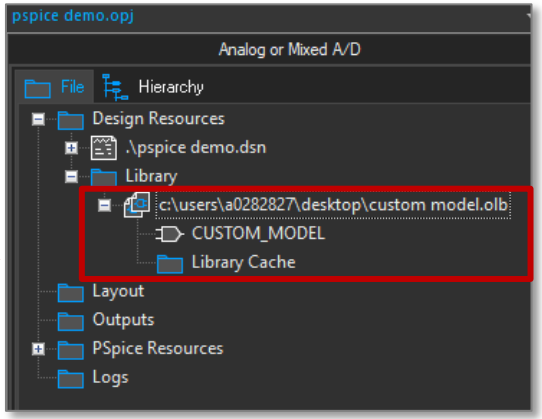
- **Note:** components from these libraries ***do not*** trigger the probe limit

Importing third-party or custom models

- With your ***project*** (.opj) selected, click *Tools* → *Generate Part*
- Browse to your model file in the new window, make your selections, and click *OK*
- The new model appears in your project's library







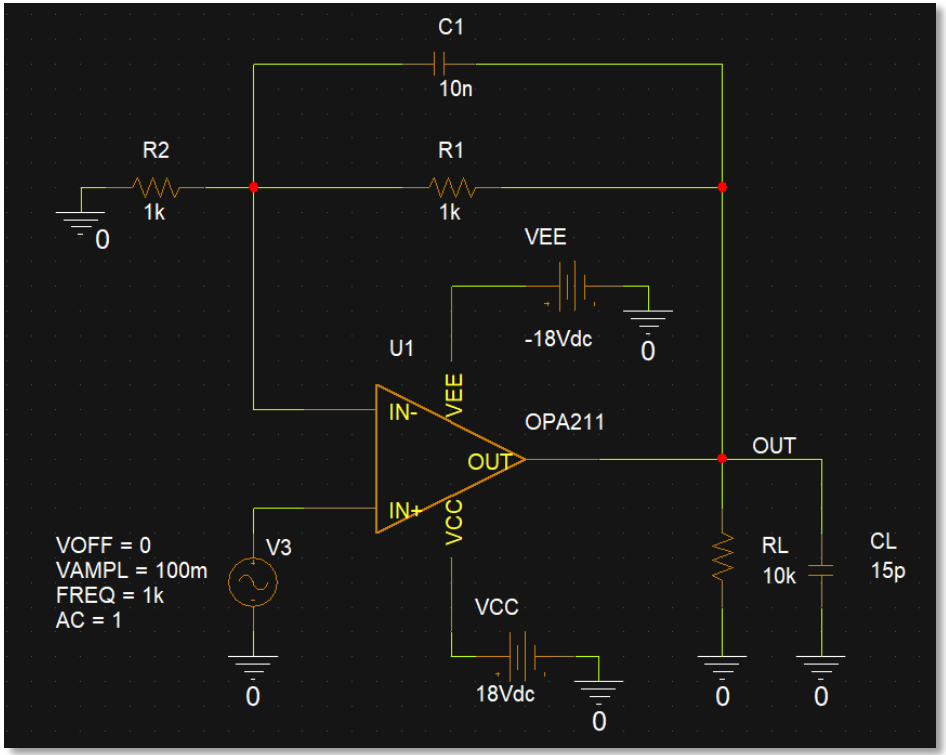
Types of models on TI.com

Type	Description
PSpice	Analog / mixed-signal model for use in **PSpice-based** simulators. Packaged in a way to be easy to import and use in PSpice / Cadence / OrCAD.
TINA-TI	Analog / mixed-signal model for use in **PSpice-based** simulators. Packaged in a way to be easy to import and use in TINA-TI.
HSPICE (uncommon)	Analog / mixed-signal model for use in **HSPICE-based** simulators. HSPICE is a branch of SPICE similar to PSpice, but models are not directly compatible.
SIMPLIS	Switch-mode power supply model for use in **SIMPLIS**.
IBIS	I/O Buffer Information Specification model, typically used for digital pin timing analysis. Compatible with a broad range of industry simulators.

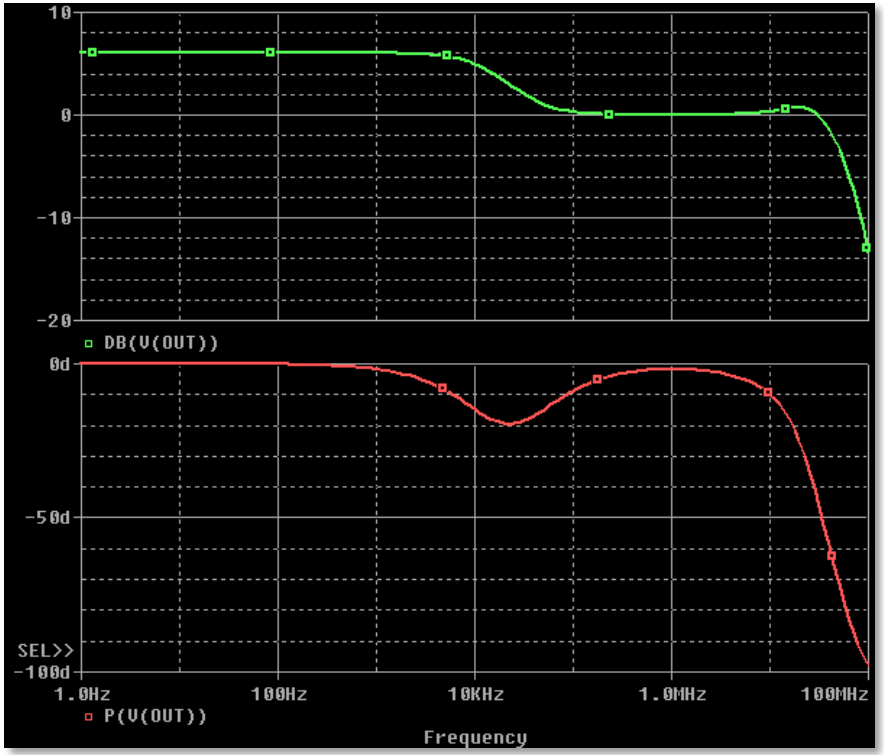
Part 3
Setup and simulation examples

Tip: Enabling AutoConverge in your sim profile can fix a broad range of convergence issues.

Operational amplifier example – OPA211

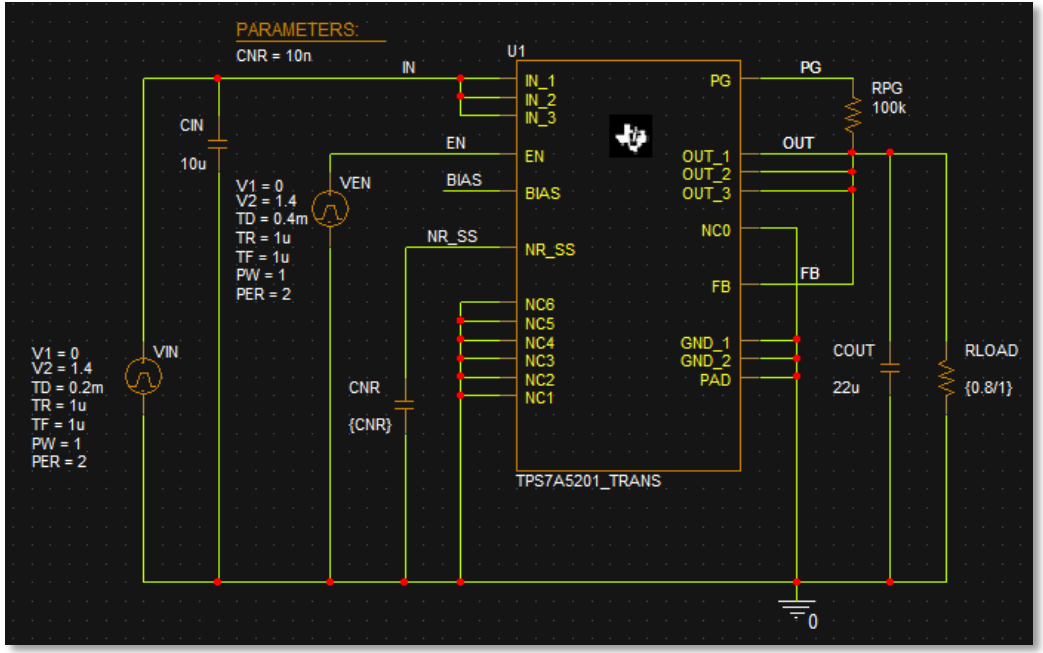


Schematic capture

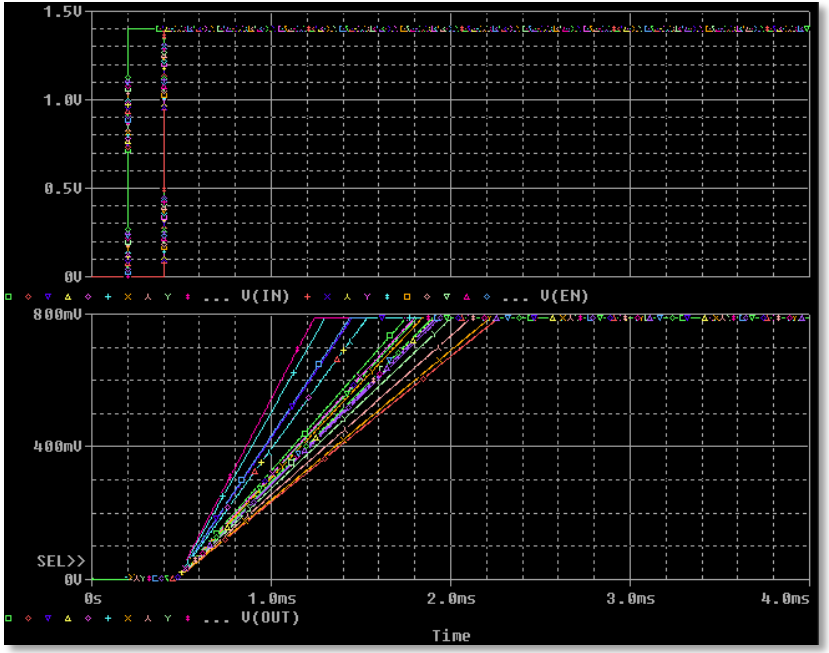


AC simulation result

Power supply example – TPS7A52

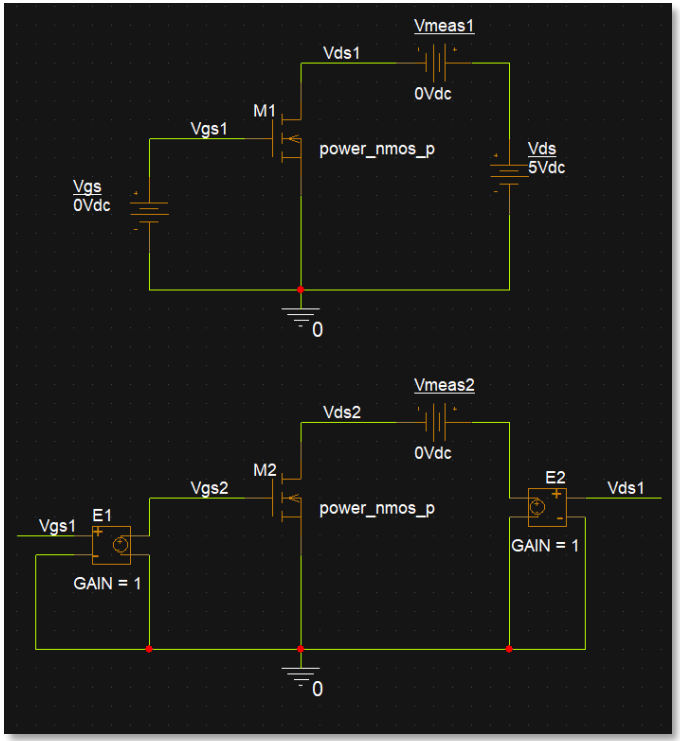


Schematic capture

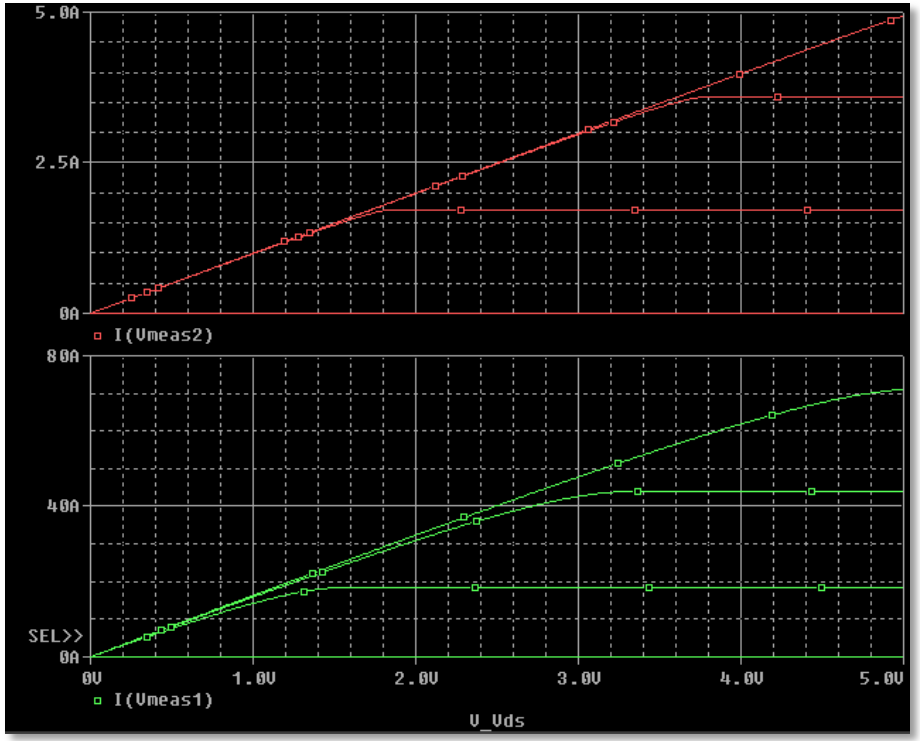


Transient simulation result

Modeling Application – Power MOSFET



Schematic capture



DC simulation result

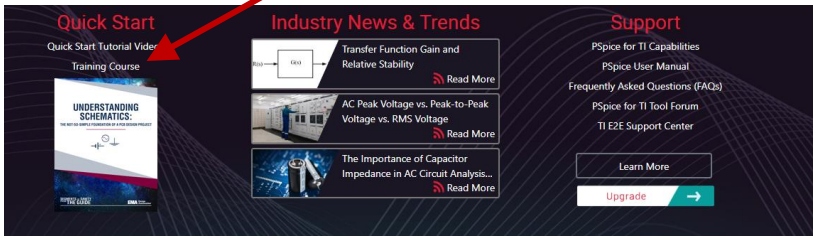
Part 4
Additional Resources

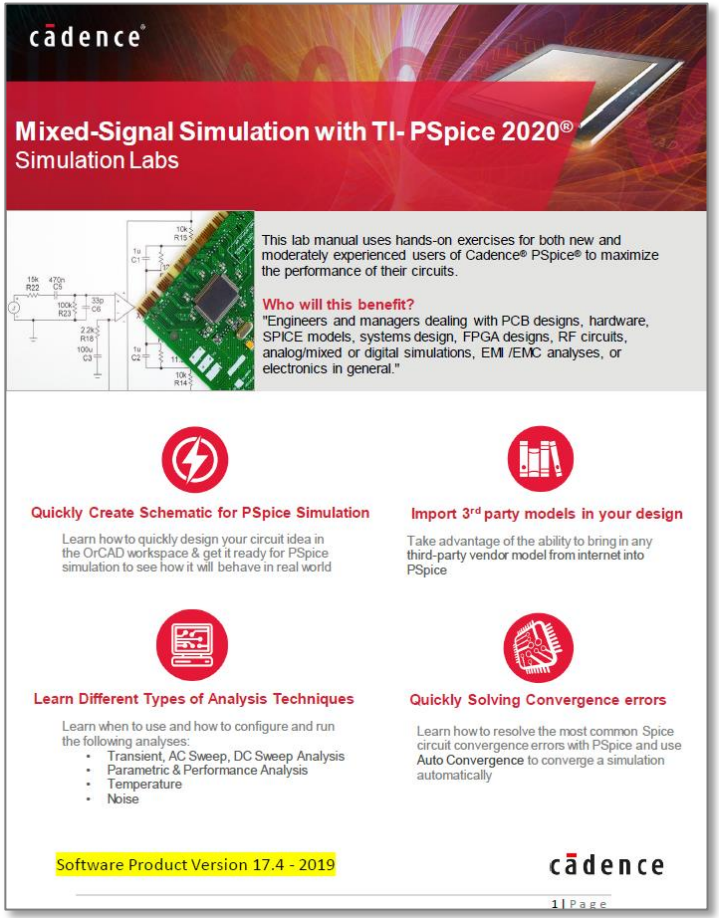
Tip: Choose the “Last Plot” setting in your sim profile to preserve results display settings between runs.

Additional resources

Hands-on training manual

- Self-guided, step-by-step tutorial that walks the user through the entire tool workflow
  - Includes basic and more advanced content
  - Includes debugging and troubleshooting
- Available from the PSpice for TI start page:
  - Click *Training Course*





Additional resources, cont.

Overview content


How to simulate complex analog power and signal-chain circuits with PSpice for TI

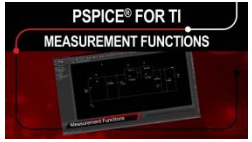
How to simulate complex analog power and signal-chain circuits with PSpice® for TI

[Link]

PSpice for TI overview video

[Link]

Technical training videos

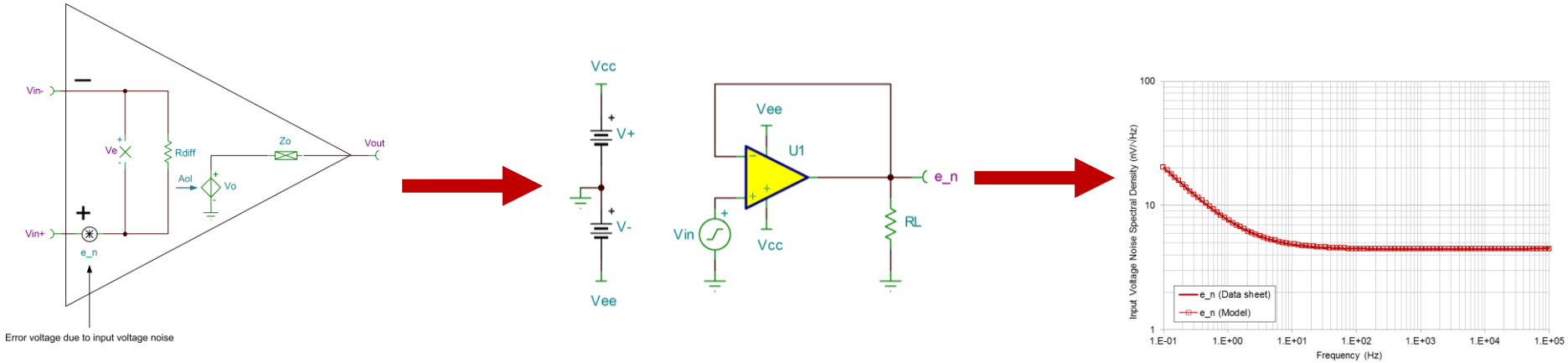


[Link to videos]

TI.com/pspice-for-ti

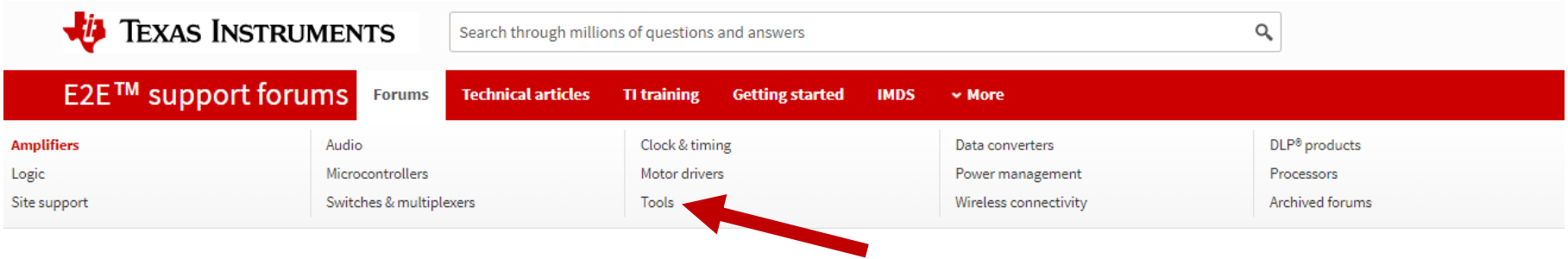
“Trust, but verify” SPICE models

- Series of articles that covers verifying parameters of amplifier models:
  - Part 1: Output impedance
  - Part 2: Small-signal bandwidth
  - Part 3: Input-referred errors
  - Part 4: Noise



Direct support from TI

- For tool-related support: Simulation, hardware & system design tools forum
- For specific model or product support: post to that product's forum
  - i.e. For amplifier support, post to the Amplifiers forum



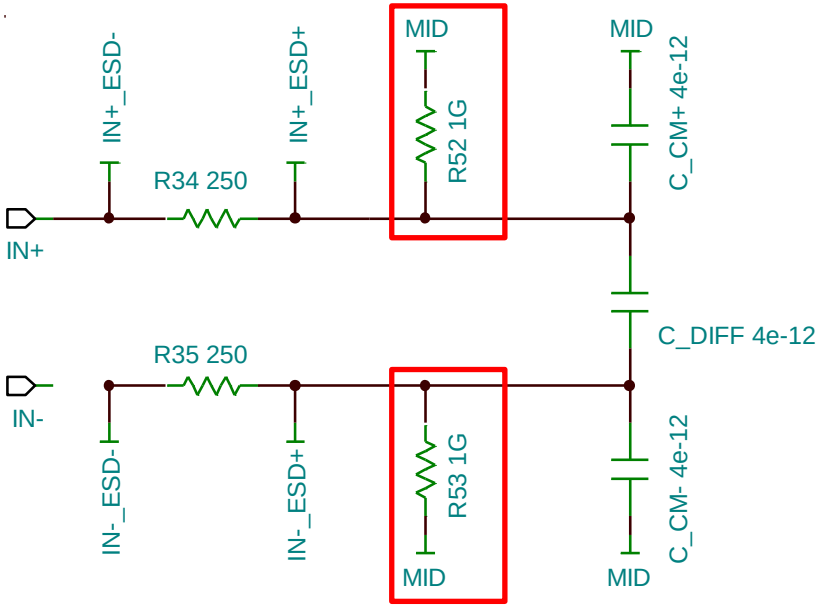
Note: these forums are all supported by TI applications engineers who are graded on responsiveness and quality of support. You should get an initial reply in 24h.

SPICE tips – analysis parameters

Option	Default	Relaxed	Effect
AutoConverge	Off	On	Relaxes multiple parameters if needed to enable convergence
ABSTOL	1e-12	1e-10	Sets the absolute tolerance of nodal currents between DC iterations
RELTOL	1e-3	3e-3	Sets the relative tolerance of the nodal voltages at each DC iteration compared to the first
GMIN	1e-12	1e-10	Adds conductance parallel to every p-n junction
CSHUNT	0	1e-15	Adds capacitance from every node to ground

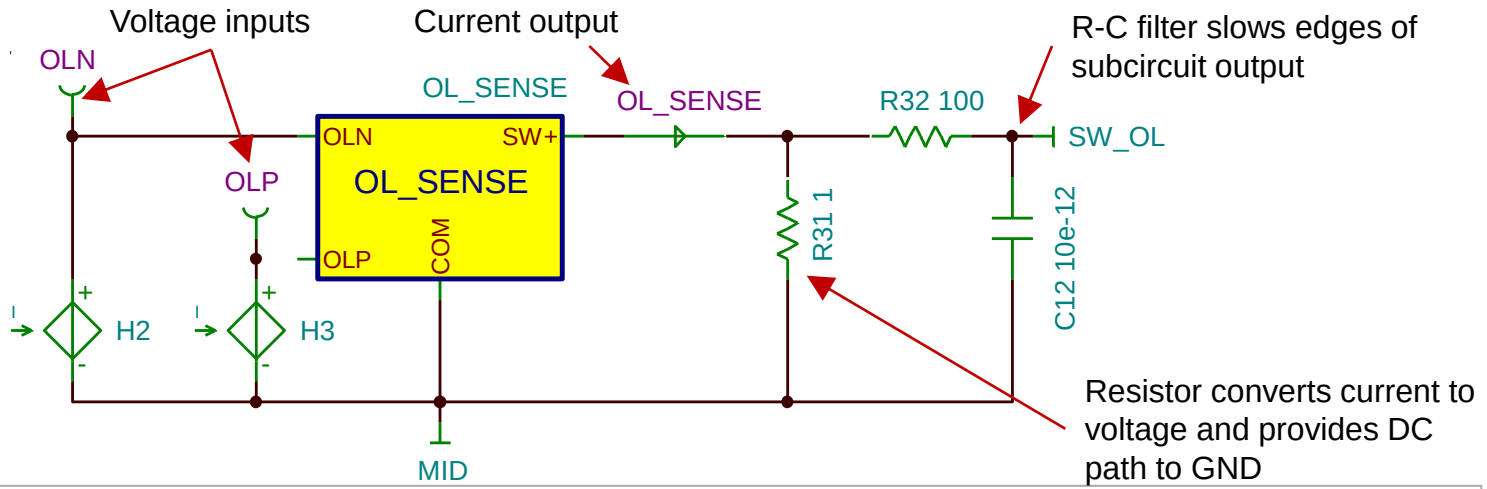
SPICE tips – DC path to GND

- Ensure DC path to ground at every node
  - Can force a path with large resistors (1T, etc.) that don't affect electrical performance
  - Try to use the smallest value possible



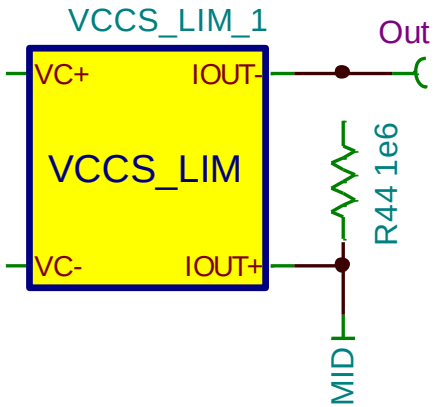
SPICE tips – linear circuits

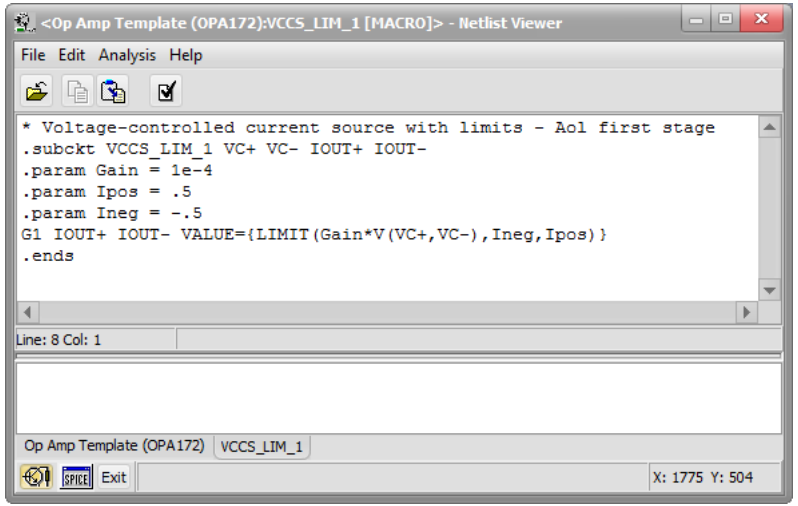
- Design functional blocks with as linear behavior as possible
  - Sharp transitions or discontinuities cause issues with convergence checks
  - Use R-C filter networks to reduce bandwidth of subcircuits for smooth transitions
  - Use voltage inputs and current outputs wherever possible



SPICE tips – bounded matrix

- Keep matrix equations as tightly bounded as possible
  - Place limits on gain and buffer stages
  - Use only as much gain as required
  - Scale resistances to keep node voltages and currents in similar ranges

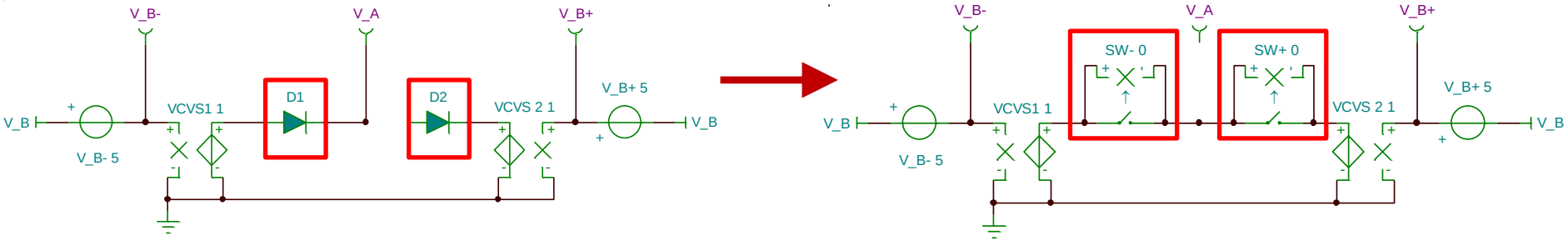




SPICE tips – simplified components

- Replace complex components with simple approximations if exact component modeling isn't necessary
  - **Example:** ideal diode → voltage-controlled switch

Diode equation: $i_D = I_S(e^{\frac{qV_D}{kT}} - 1)$



Thank you!

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