National's Clock Design Tool v1.1 Instructions

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National Semiconductor

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1) BASIC NCDT OPERATION

1.1) Quick Overview

The primary purpose of National's Clock Design Tool is to:

- Aid the user in selecting a National Timing device as their clocking solution.
- Aid the user in designing a loop filter for optimum phase noise/jitter for their selected solution.

The Design Tool may be used to

- Enter desired output frequencies for automatic device recommendation (*wizard mode*).
- Enter desired input frequencies (optional) for automatic device recommendation (*wizard mode*).
- Select a solution from a list of National devices (*wizard mode*).
- Select a device configuration from a list of a configuration options (*wizard mode*).
- View recommended loop filter values for a design.
- Enter custom phase noise values for a reference, PLL, VCO, or VCXO.
- Redesign a loop filter based on the design tool's recommendation or using user specified loop-bandwidth and phase margin.
- Save the design for future reference.
- Load a previously saved design.
- Check for new versions of the design tool.
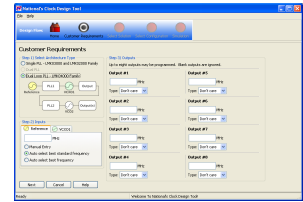
Input requirements
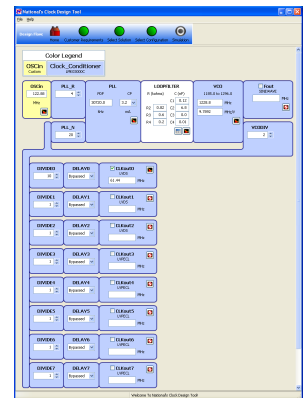
Simulation

Wizard mode

For most users, wizard mode will be the best path to creating a design for simulation. One benefit of the wizard mode is the software will auto-calculate VCO frequency and divider values for PLL and output dividers to achieve the specific frequency requirements as entered by the user.

Wizard mode icon

Once the wizard mode is started (Customer Requirements screen), the required user-defined inputs are:

1. Architecture Type. (Designs with a single PLL or two PLLs in series)
2. Reference and/or VCXO1 definition. (optional)
3. Output frequency and type definition.

Once defined, two additional steps are required:

1. Select Solution: Selecting from the National parts which satisfy the design requirements.

2. Select Configuration: Selecting from the presented configurations the National part can use to achieve the design requirements.

   Note: The program will automatically score and display the best solution/configuration based on internal calculations.

   (See Section 2.5 Picking a Solution and 2.6 Picking a Configuration)

Once the simulation screen has been reached, users will then be able to:
- Calculate loop values for loop filters.
- Update phase noise profiles for blocks like oscillators and VCXOs.
- View RMS jitter measurements of available outputs
- Copy phase noise simulation traces to clipboard for pasting into Excel or other programs.
- Save the design: To save a design, click File – Save.

Manual-mode

Clicking the Manual-mode new design icon, the user may directly select a device from a list. Once selected the simulation screen will populate with some default values. From this point the user is responsible for every aspect of the configuration. VCO frequencies, divider values, clock output frequencies, etc.

Manual-mode icon

1.2) Installing National's Clock Design Tool

To install the software, run the program "NCDT_Install.exe" and follow the on-screen instructions.

1.3) Starting National's Clock Design Tool

There are three ways to start this program:
1. Start Menu
2. Desktop Icon [optional, select during install]
3. Start Bar Icon [optional, select during install]

Checking for updates to National's Clock Design Tool

Automatically check for updates to National's Clock Design Tool by clicking the "Check web for latest version" button from the Home Screen.
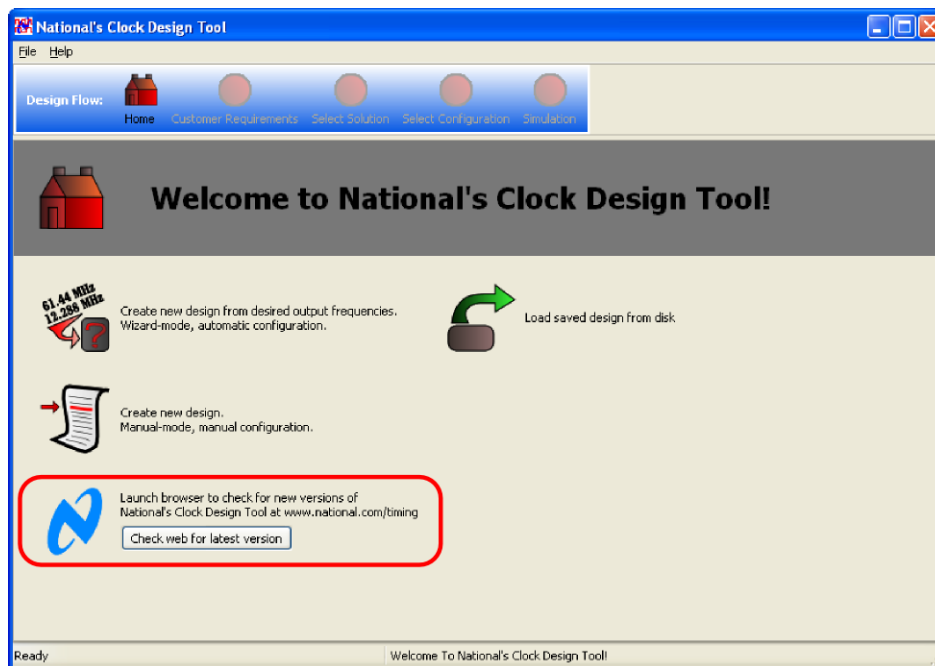
Figure 1: Home Screen - Check for Update

Keep up to date on the latest National has to offer in Timing devices and PLLs at the website:
http://www.national.com/timing.

2) NATIONAL'S CLOCK DESIGN TOOL INTERFACE

2.1) User Interface Map

Figure 2 shows an overview of the various screens in the design tool and simple process flow. The following pages will introduce each screen and explain operational details.

Home

Customer Requirements

Select Solution

Select Configuration

Pick Part

Simulation

Phase Noise Display

Loop Filter Design

Load Custom
Phase Noise
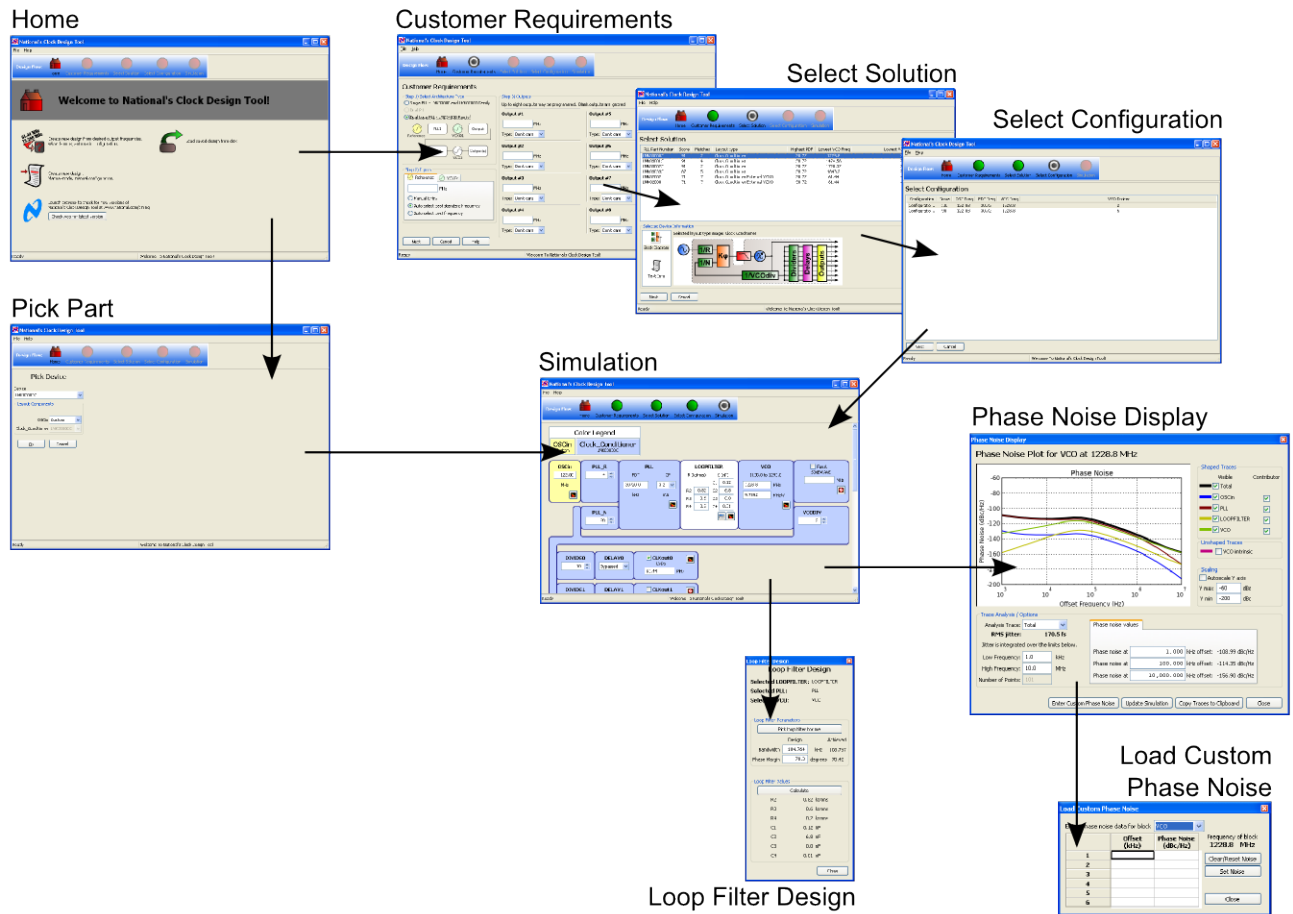
Figure 2: Interface Map

2.2) The Home Screen
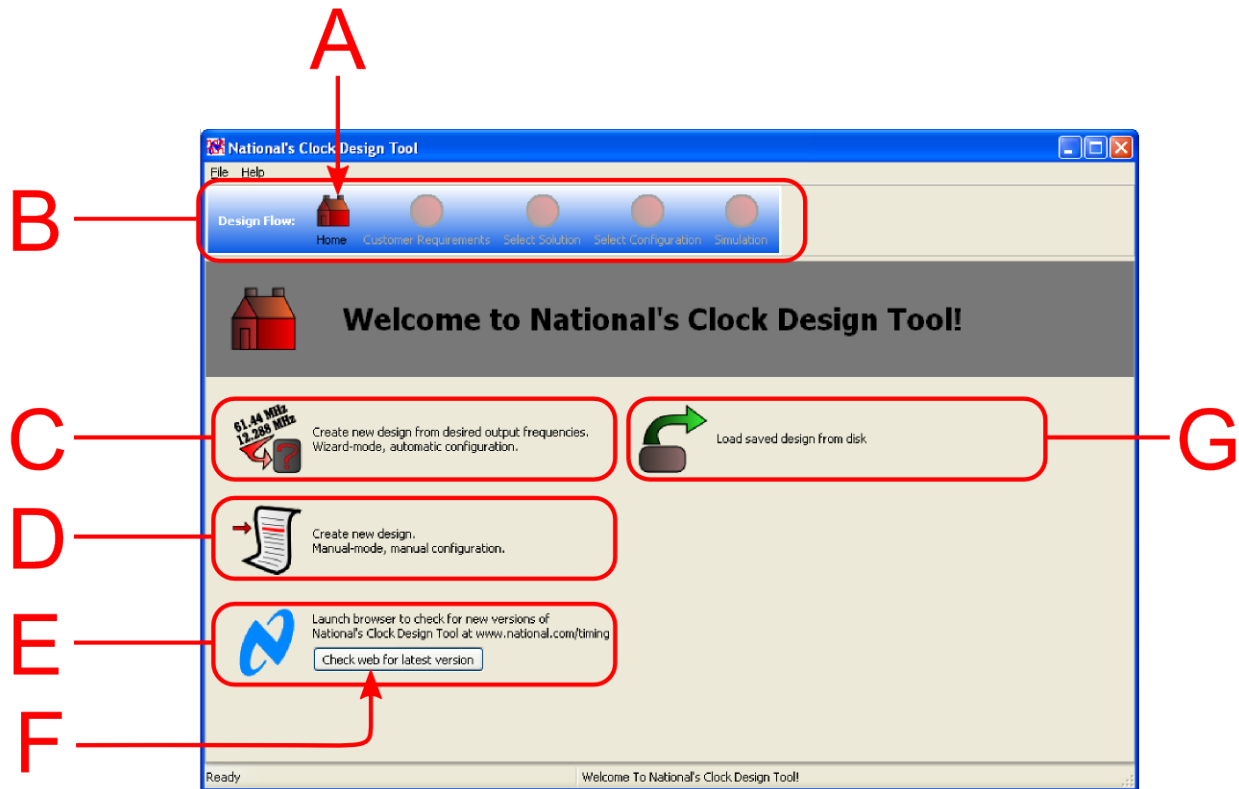
Figure 3: Home Screen

The Home Screen is displayed after the tool starts. It can be accessed at any time by pressing the house icon (A) in the design flow bar (B).

Options from this screen include
- Create a new design using wizard mode (C)
- Create a new design by picking a National part directly (D) – for advanced users.
- Check the website for new versions (E)
  - Internet access is required to click the 'Check web for latest version' button (F).
  - Or, press the hyper-link to launch a web browser to the webpage, http://www.national.com/timing
- Load a previously saved design from disk (G)
  - When loading a previously saved design, you will return to the exact place in the software from which the design was last saved.

2.3) Design Flow Toolbar

Figure 4: Various states of the Design Flow toolbar

The design flow toolbar highlights the current position in the design flow with a black and white dot icon, once the user is beyond the home screen (B-F above).

The toolbar's design allows the user to quickly move between different screens in the design tool. Available screens include:
- Home Screen (A)
- Customer Requirements (B)
- Select Solution (C)
- Select Configuration (D)
- Simulation Screen (E) and (F)
    - Line (E) shows the design flow toolbar after a wizard mode design has been completed
    - Line (F) shows the design flow toolbar after a manual-mode design. (since none of the intermediate steps were used to arrive at simulation, they are not shown as green dots in the design flow toolbar)

Any of the non-shaded, green, icons are clickable to navigate back to that point in the design.
(Ex: adjust frequencies, device solution choice, or device configuration choice)

2.4)   Customer Requirements Screen

Figure 5: Customer Requirements

After selecting the wizard mode option from the home page, the Customer Requirements screen is displayed. Shown as (A) in Figure 5 above.

Three panels of information are used to search for solutions. The minimum user entry required to pass this screen is for at least one frequency to be entered in an output to continue to the next screen.

Step 1) Select Architecture Type
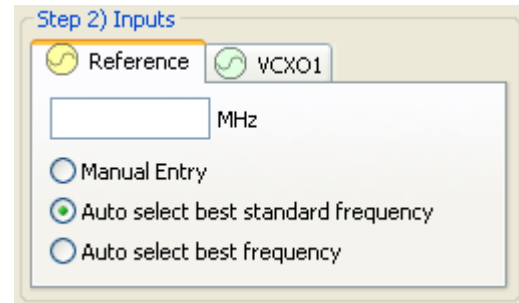Shown as (B) in Figure 5.
- Single PLL – The LMK03000 and LMK02000 family a single PLL is used to generate frequencies.
- Dual PLL – Not yet implemented
- Dual Loop PLL – The LMK04000 family has two PLLs in series as shown in the block diagram.
  - See APPENDIX A for more information on this option.

Step 2) Inputs

Shown as (C) in Figure 5.

The input frequency can be specified in three different ways.

- Manual Entry
- Auto select best standard frequency
- Auto select best frequency

Note: Depending on the architecture chosen in the first step, VCXO1 may also be shown for specification of input type.

Step 3) Outputs

Shown as (D) in Figure 5. Up to eight different outputs may be entered. Once the frequency has been entered, the output type may be optionally specified.
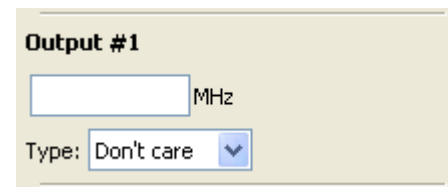
Frequencies

When entering frequencies, mixed fractions may be used. For example 74.25/1.001 is a common frequency for video applications and can be entered directly (74 + 16/91 is also valid). The ability to enter mixed fractions prevents rounding errors, allowing exact solutions to be solved. Note 74.176 MHz does not equal 74.25/1.001.

Entering frequencies with integer relationships will increase the probability of a solution being found. For example, if outputs of 100 MHz and 200 MHz are desired, a minimum VCO frequency of 200 MHz would be needed to achieve the 100 MHz output and 200 MHz output by using divide by 2 and 1 respectively. However if the outputs 100 MHz and 101 MHz were needed, for integer dividers, a minimum VCO frequency of 10,100 MHz is required! The dividers 101 and 100 would be used to achieve the output frequency. The other option would be to used a Dual PLL option or two Single PLL solutions together at the same time. See Applicate Note AN-1865[1] for more information on frequency planning.

Output Types

Currently options for output type include:

- Don't care
- LVDS
- LVPECL
- 2VPECL   - Currently only LMK04000 (Dual Loop) supports this output
- LVCMOS   - Currently only LMK04000 (Dual Loop) supports this output
- SINEWAVE   - This will be an RF output from a VCO or VCXO.

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1   See www.national.com/an/AN/AN-1865.pdf for more information on frequency planning.

2.5) Select Solution Screen
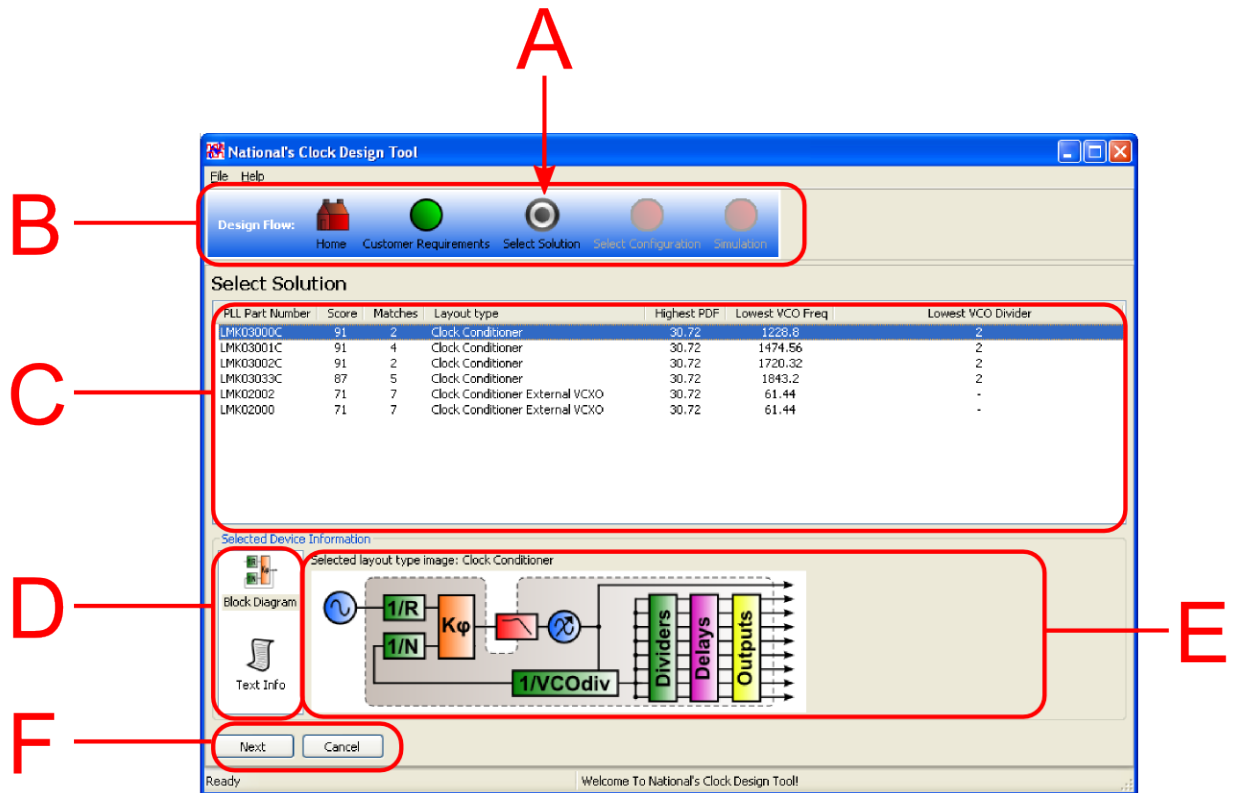
Figure 6: Select Solution

The Select Solution screen is displayed after the customer requirements screen in the design flow, see the black and white dot icon (A) for current step, Figure 6 above.

Picking a Solution
The listbox (C), Figure 6, highlights the National parts which will meet the frequency and output requirements as entered from the customer requirements screen. Different devices will use different VCO frequencies and divider values to achieve the same result. The various solutions are scored to estimate which solution will have the best performance. The higher scored devices are listed first.

Each solution will have a number of "Matches". This means there are multiple ways to program the selected device to achieve the frequency requirements. This will be discussed further in the *Select Configuration Screen* section of this manual. To give the user an idea of the parameters available to each listed solution, one of the parameters from the matches is displayed. The parameters will be unique for different architectures and are listed below.

Single PLL
"Highest PDF," "Lowest VCO Frequency," and "Lowest VCODIV"
Dual Loop
"Highest VCXO Freq," "Highest PDF2," "Lowest VCO2 Freq," and "Lowest VCODIV"

The design tool defaults to the first solution in this list.

Device Information

The icons in (D), Figure 6, allows a block diagram or text information to be displayed in region (E) describing the currently selected solution. Region (E) shows a generalized block diagram of the device. When "Text Info" is selected the block in Figure 7 is shown.
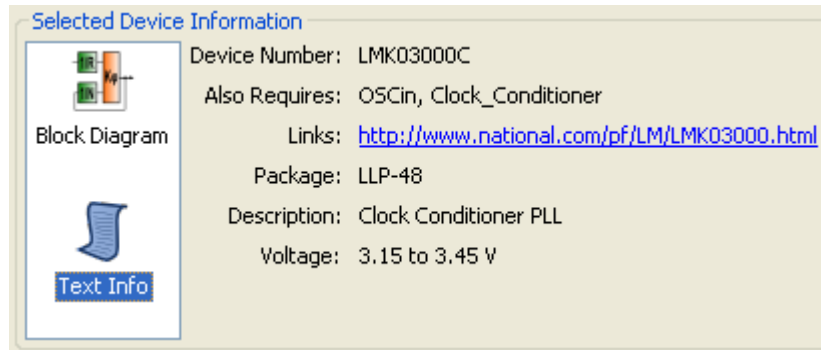
Figure 7: Text Info displayed

2.6) Select Configuration Screen
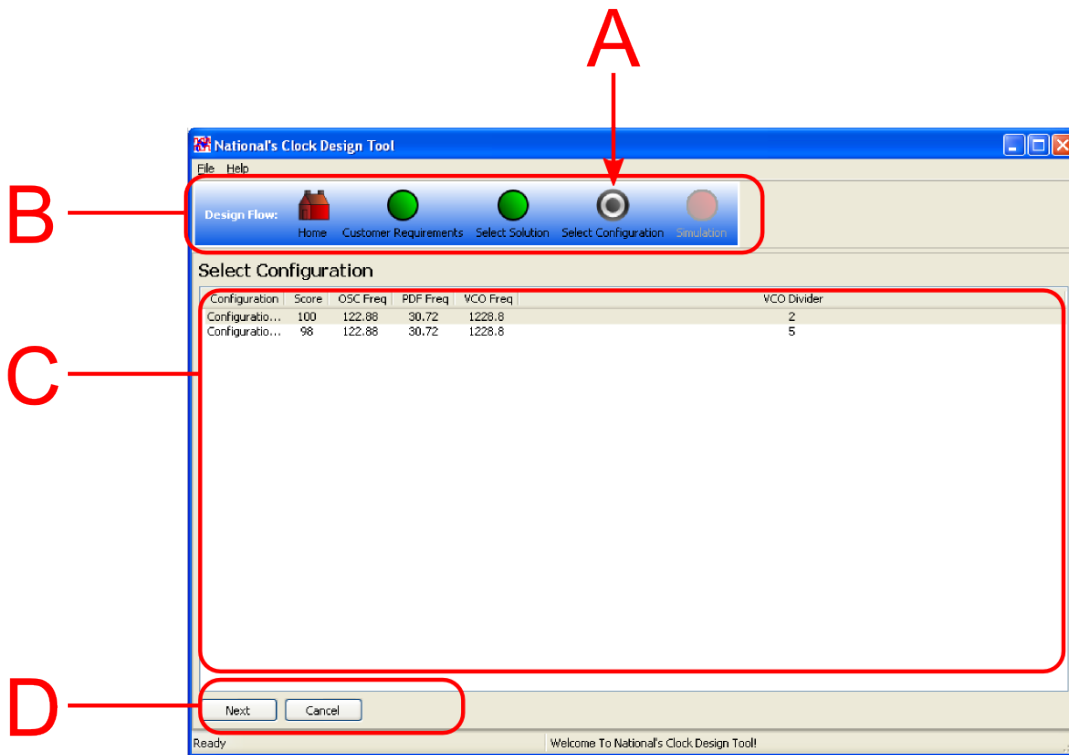
Figure 8: Select Configuration

The select configuration screen is displayed after the select solution screen in the design flow. The black and white dot icon (A) shows we are currently at the select configuration screen. Press the green dot icon in this position, later on in the design flow to return to this screen.

Picking a Configuration
The listbox (C), Figure 8, shows the various configurations the device may use to achieve the frequency requirements as entered on the customer requirements screen. It is possible that different VCO frequencies and divider values will achieve the same result. The various configurations are scored to estimate which configuration will have the best performance. The configurations are listed in order by Score. The columns describing the different configurations may differ depending on architectures selected at the customer requirements screen and are listed below.

Single PLL
"OSC Freq", "PDF", "VCO Freq" and "VCODIV"
Dual Loop
"OSC Freq", "VCXO Freq", "PDF2", "VCO2 Freq" and "VCODIV"

The design tool defaults to the first configuration in this list.

2.7) Simulation Screen
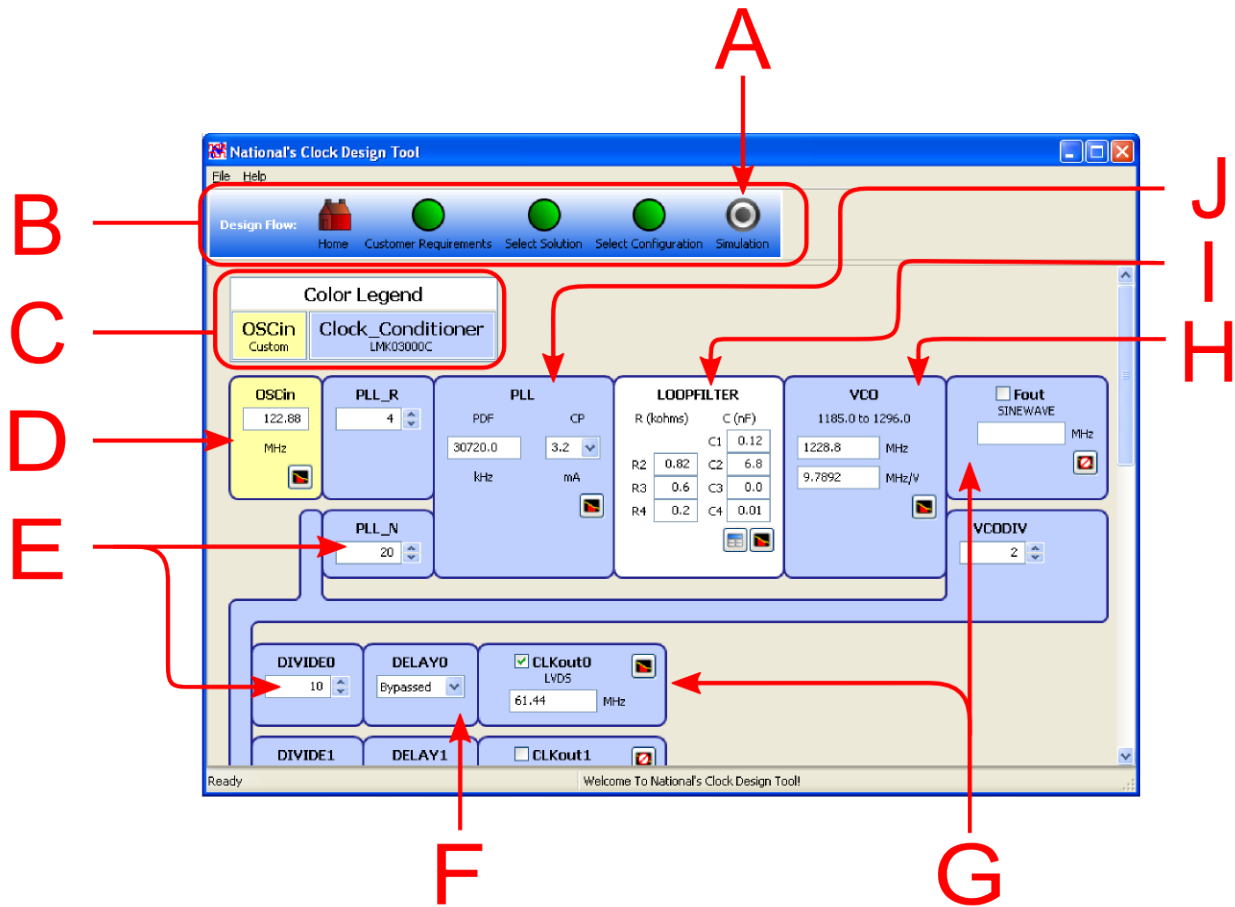
Figure 9: Simulation Screen

The simulation screen is displayed after the select configuration screen in the design flow. The black and white dot icon (A), Figure 9, shows we are currently at the simulation screen. This is the final step in the design flow. User simulation may now begin.

A legend of devices used is shown in (C).

Warnings
When the design tool detects certain parameters out of range, it will turn the entry box red as shown in Figure 10. Mousing over the entry box will display a tool-tip describing the warning.
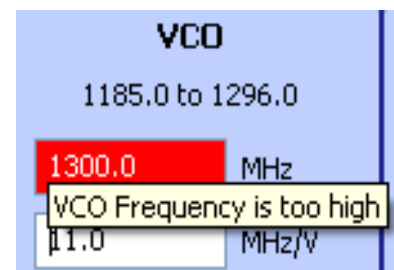
Figure 10: Simulation warning example

Block Buttons on the Simulation Screen

Some of the blocks in the simulation screen have buttons which allow for simulation, design, or inspection to be performed.

Loop Filter Calculations button
Displays a loop filter design screen.

Refer to 2.8) Loop Filter Design Screen below.

Phase Noise button
The phase noise button will display a phase noise display screen which will allow the phase noise traces of this and preceding blocks to be displayed. Analysis of the jitter over a bandwidth, phase noise at a particular offset, etc. may be made from this window. The LOOPFILTER block has a customized phase traces setup.

Refer to 2.9) Phase Noise Display Screen below.

Below, the legend is the block diagram of the selected solution. Many individual oscillator, VCO, divider, PLL, etc, blocks make up the entire simulation.

Reference Block   Properties: Frequency
Buttons: Shown as (D) in Figure 9.
The reference block is a simple block which contains the reference frequency of a device. This frequency will be used by the blocks which follow it.

Changing the frequency does not change scale for the phase noise of the block. Changing the frequency will change the frequency of all blocks following it.

Divider Block   Properties: Divide value
                                     Shown as (E) in Figure 9. Also: PLL_R, VCODIV, DIVIDE1
The divider block represents a divider in the device. Programming it will alter the frequency of following blocks.

PLL Block   Properties: Phase Detector Frequency (PDF), Charge Pump (CP)
Buttons: Shown as (J) in Figure 9.
Although the term PLL (Phased Lock Loop) technically includes the phase detector, charge pump, loop filter, and VCO, the PLL block represents only the phase detector and charge pump in the device.

Note: When displaying phase noise for a PLL block, the displayed noise is technically the noise measured at the output of the N divider.

Loop filter Block   Properties: Resistor and capacitor values - R2, R3, R4, C1, C2, C3, C4
Buttons: ▦ ◣   Shown as (I) in Figure 9.

The loop filter block shows the values of the resistors and capacitors for use in the user's design. This information is one of the primary purposes for the use of the design tool. Also, the user can change the loop filter values and see the impact on phase noise. If the phase noise screen display screen is already open, be sure to press the update button on the phase noise screen after changing loop filter component values to update the phase noise plot.

VCO (or VCXO) Block   Properties: Frequency range (VCO only), Frequency, Tuning sensitivity
Buttons: ◣   Shown as (H) in Figure 9.

The frequency range displayed is for the VCO being used. It is possible to use frequencies outside of the VCO (or VCXOs) range. The tuning sensitivity (KVCO) is automatically linearly interpolated over the range of the VCO.

Delay Block   Properties: Delay value
            Shown as (F) in Figure 9.

The delay block represents a delay in the device. Programming it will affect phase noise.

Output Block   Properties: Enabled, Type, Frequency
Buttons: ◣   Shown as (G) in Figure 9.

The output block indicates if the output is enabled by the checkbox next to the output name. Click to enable/disable. The output block also indicates what type of output the block represents. LVDS, LVPECL, 2VPECL, LVCMOS, or SINEWAVE. If enabled, the output block will also display the output frequency and allow the user to further simulate phase noise.

2.8) Loop Filter Design Screen

Figure 11: Loop Filter Design

The loop filter design screen is displayed when the user clicks the loop filter calculator button (Figure 12) on the simulation page.

Title block (B), Figure 11, region shows information about the block the loop filter occupies and the block name of the PLL and VCO (or VCXO) with which the loop filter is associated.

Figure 12: Loop Filter Calculator button

The button (C) "Pick loop filter for me" selects a loop bandwidth and phase margin (D) to determine a recommend loop filter to minimize jitter in the bandwidth 200 Hz to 2 MHz from the noise sources of the reference, PLL, and VCO. Once the loop bandwidth and phase margin has been estimated fo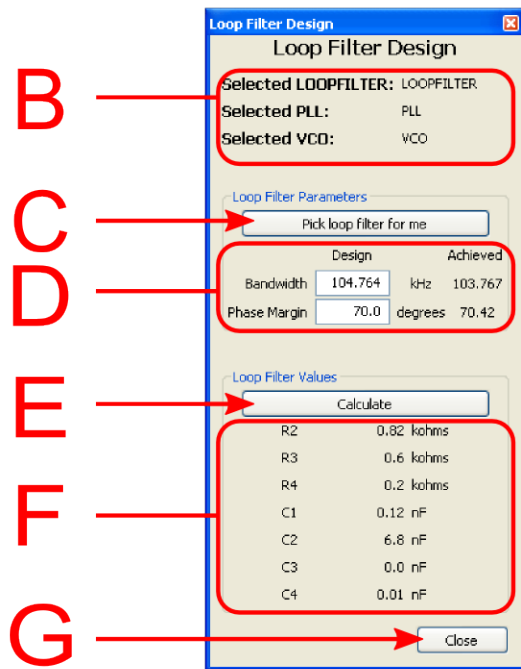r best jitter, the "Calculate" (E) button is automatically pressed for the user and the loop filter component values (F) are updated.

Otherwise the "Calculate" button (E) can be pressed after to design a loop filter to achieve the current bandwidth and phase margin values entered into the loop filter parameters box (D). The loop filter component values (F) are updated.

The close button (G) will close the window.

Note: when a design is created for the first time, the loop filter values are populated with the 'pick loop filter for me' values. If the phase noise profiles of any oscillator, PLL, or VCO is updated, re-calculating the recommended loop filter may improve jitter results.

2.9) Phase Noise Display Screen

Figure 13: Phase Noise Display Screen

The phase noise display screen is displayed when the user clicks the phase noise display button (Figure 14) from the simulation page (Figure 9). When the phase noise display not allowed button is visible (Figure 15), it indicates the user must first <u>enable</u> the output before phase noise simulation is allowed.

The title of the screen (A), Figure 13, shows the name of the current block on which the phase noise analysis was activated and the frequency that block is operating at.

The shaped traces box (B) shows which traces are visible and which traces contribute to the "Total" trace. The unshaped traces box (C) allows the user to turn on the phase noise of the current block's "unshaped" noise.

<u>Shaped traces</u> – A phase locked loop (PLL) shapes the noise of contributing blocks. Inside the loop bandwidth the PLL and/or reference oscillator will be the dominate noise source. Outside the loop bandwidth the VCO (or VCXO) will be dominate noise source. This causes the PLL and reference noise to be "shaped" by the VCO outside the loop bandwidth and the VCO noise to be "shaped" inside the loop bandwidth.

<u>Unshaped traces</u> – Displays the phase noise of the current block as if there were no PLL and it was measured standalone.

The plotting window (D), Figure 13, shows the phase noise plot.

The scaling box (E) allows the plotting Y axis to be changed.

The trace analysis (F) selects the trace to calculate RMS jitter over and the frequency bandwidth limits for this calculation. The frequency bandwidth limits also controls the X axis of the phase noise plot.

The phase noise values (G) allows the phase noise of the selected trace (F) to be accurately measured by selecting up to three offsets to display the phase noise value at. If an offset which is not valid (outside of the X axis range) the box changes color to yellow and the phase noise value for the minimum or maximum range is displayed.

The "Enter Custom Phase Noise" button (H) allows the user to enter custom phase noise values for different blocks. See Load Custom Phase Noise Screen, Page 21, next for more information.

The "Update Simulation" button (I) updates the phase noise plot. The plot will need updating after any changes to frequencies, divider values, charge pump current, loop filter values, in the simulation window.

The "Copy Traces to Clipboard" button (J) will copy all the displayed traces to the clipboard. These traces may then be pasted into any other application. Of particular interest to the user is the ability to paste them into a spreadsheet for further analysis.

The "Close" button (K) will close the window.

2.10) Load Custom Phase Noise Screen
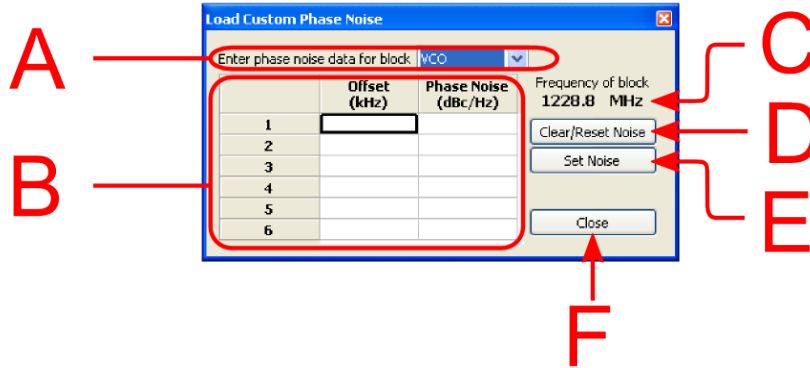
Figure 16: Load Custom Phase Noise Screen

The load custom phase noise screen is displayed when the user clicks the "Enter Custom Phase Noise" button in the "Phase Noise Display" screen.

This screen allows the user to customize the phase noise of a previous block in the drop down box (A). The phase noise offsets and phase noise values are entered into the grid (B). A <u>minimum</u> of one row must be entered. Phase noise values are for the frequency of the block shown in (C). To clear the grid and reset the noise press the "Clear/Reset Noise" button (D). After the grid has been filled with the user's values, press the "Set Noise" button (E) to update the phase noise plot with the new noise.

Press the "Close" button (F) to close the screen.

3) TYPICAL USE EXAMPLE

User Design Goal

What National parts can use use a dirty 61.44 MHz clock input and output two clean 122.88 MHz LVPECL clocks along with a clean 30.72 MHz LVDS clock? What is the phase noise performance from 1 kHz to 10 MHz? What is the RMS jitter from 1 kHz to 10 MHz?

Summary of design goal:
- 61.44 MHz Reference (dirty)
- 3 Outputs
    - 122.88 MHz LVPECL
    - 122.88 MHz LVPECL
    - 30.72 MHz LVDS

This example will provide a walk through of:
- Entering the user inputs into the design wizard.
- Picking the recommended National solution.
- Adjusting simulation options to simulate the user case.
- Changing the design to a dual loop design to see how a device which supports a dual loop architecture may improve phase noise.

3.1) First - Choose Wizard option from home page

The wizard allows the user to enter input and output frequencies.
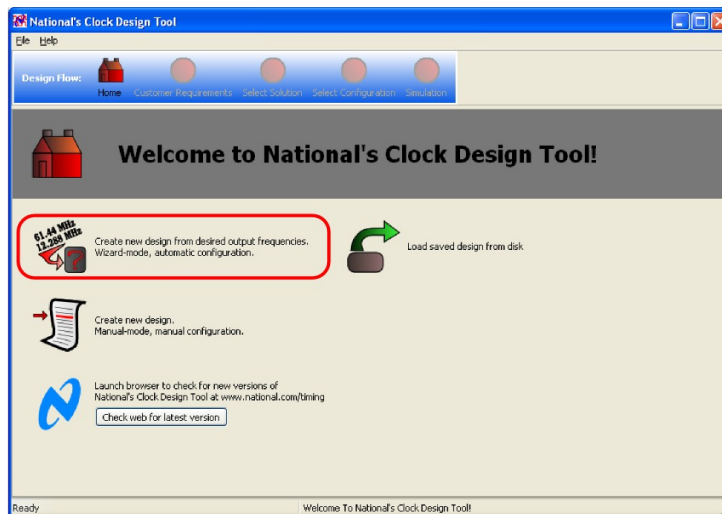
Figure 17: Selecting wizard mode.

3.2) Second - Populate the Customer Requirements screen

- Step 1) Select Single PLL Architecture (default)
- Step 2) Fill in Inputs (will toggle automatically to Manual Entry)
- Step 3) Fill in required outputs and output types
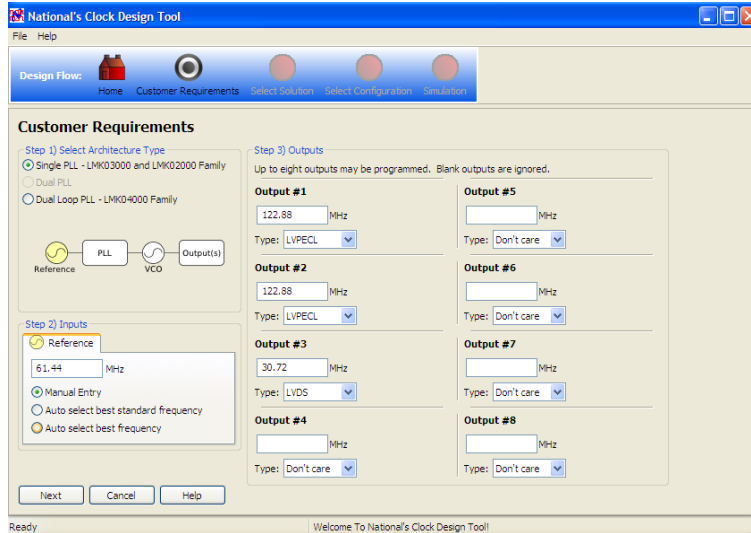
Figure 18: Populated Customer Requirements screen from design goals above.

3.3) Third - Choose Solution

All solutions capable of providing the output frequency requirements, given the input on the Customer Requirements screen, are displayed. Select the default configuration, which is scored the highest, the LMK03001C.
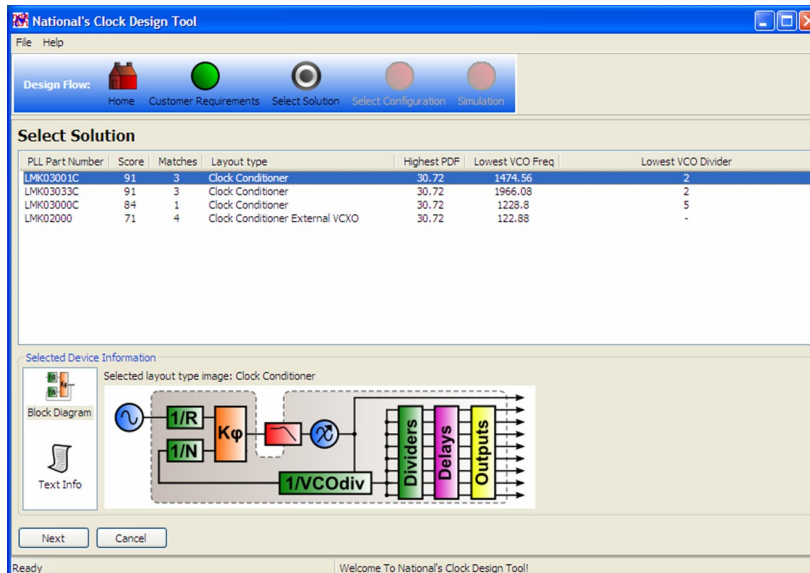
Figure 19: Selecting recommended solution.

3.4) Fourth - Choose Configuration

Various configurations for the selected device (LMK03001C) which may be used to achieve the entered frequency and output requirements are now displayed. These configurations are scored to estimate which one will achieve the best performance. For this example select the default highest scored configuration.
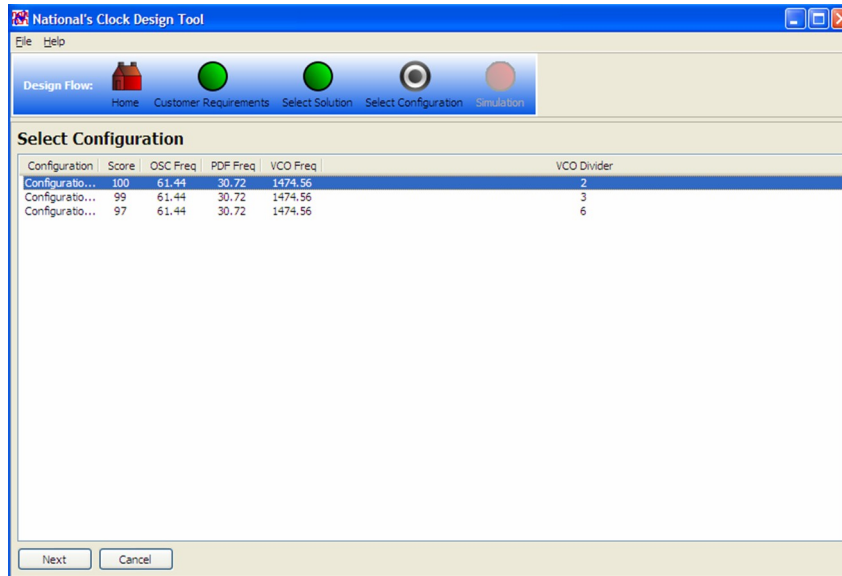
Figure 20: Selecting recommended configuration.

3.5) Fifth - Simulation

The initial solution has been reached. This screen is the starting point to...

- View phase noise plots.
- Enter custom phase noise data for certain blocks.
- Change loop filter design.

Q: Why are some clock outputs not checked (enabled) on this screen?

A: For the LMK03001C, CLKout0 – CLKout2 are LVDS outputs. CLKout3 – CLKout7 are LVPECL. The user specified 1 LVDS and 2 LVPECL outputs on the first screen of the wizard. If the type of output was not specified the output frequencies would be shown in the first available output blocks.

Figure 21: Simulation screen of new design.

One of the design questions included, what is the phase noise and RMS jitter in the 1 kHz to 10 MHz bandwidth? The user design goal also specified a dirty 61.44 MHz input clock.

To simulate the phase noise and enter phase noise parameters for the 61.44 MHz clock input press the phase noise button (🚩) on the **CLKout3** output block.

Viewing Phase Noise Plot – CLKout3 Phase Noise Plot (Initial)
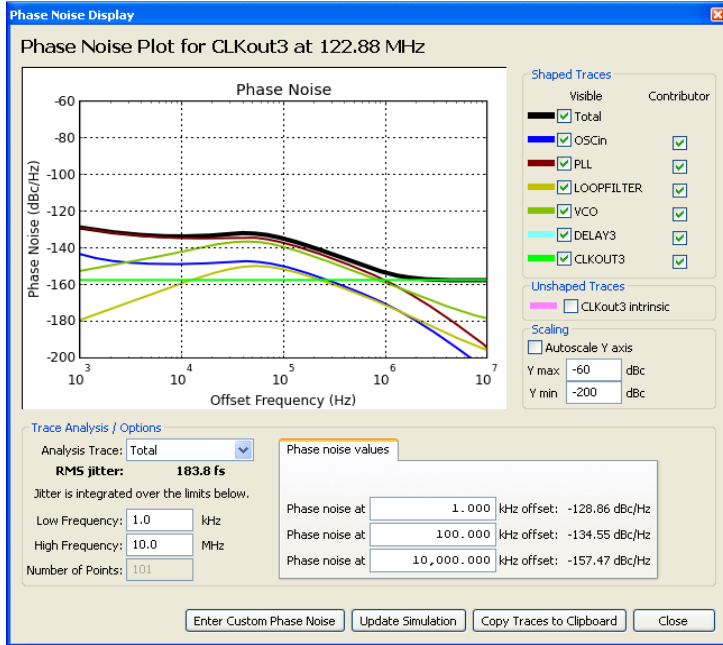
Figure 22: CLKout3 Phase Noise

Pressing the phase noise button on the CLKout3 output block will display Figure 22.
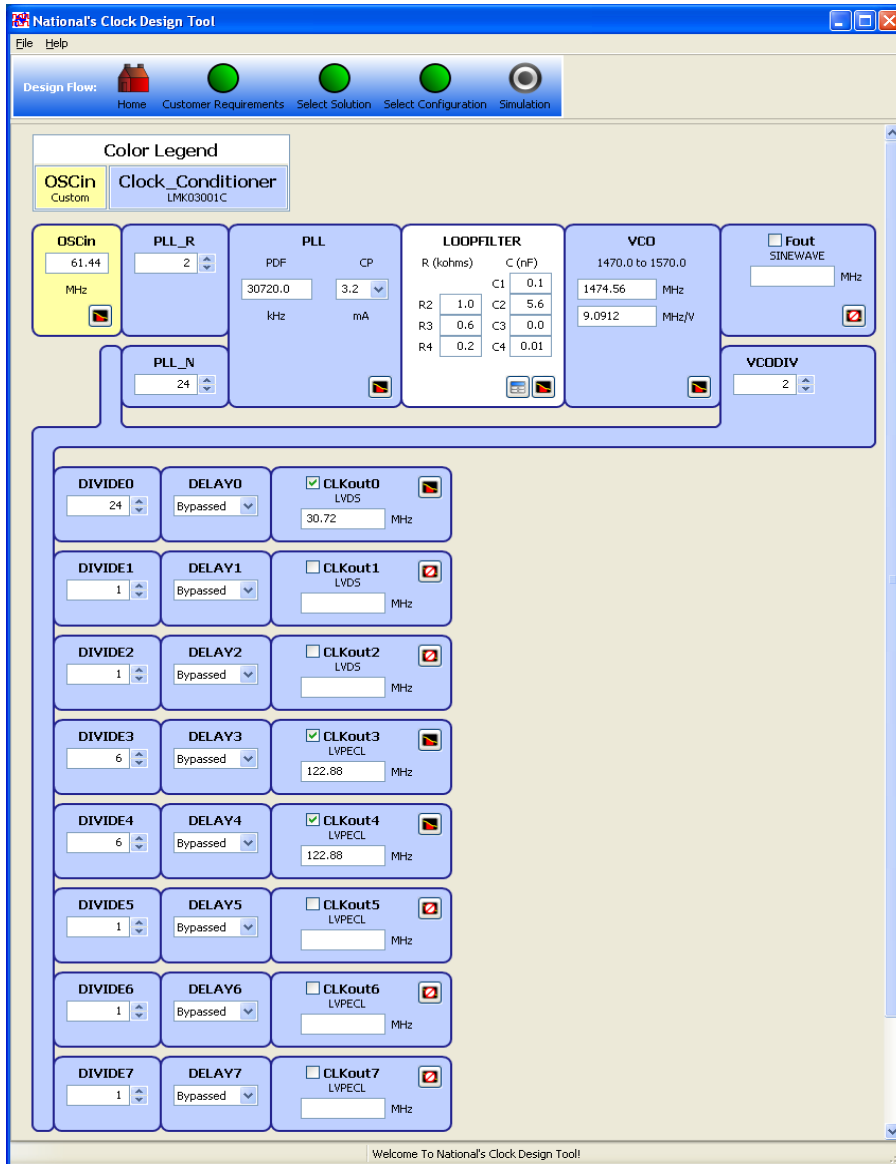
According to this screen, the RMS phase noise integrated from 1 kHz to 10 MHz of CLKout3 at 122.88 MHz is 183.8 fs.

Next, simulate how the phase noise would be affected by entering custom phase noise data for a noisy reference oscillator in the OSCin block.

To enter the phase noise data, click on the "Enter Custom Phase Noise" button.

Custom Phase Noise Entry – For a dirty OSCin reference.
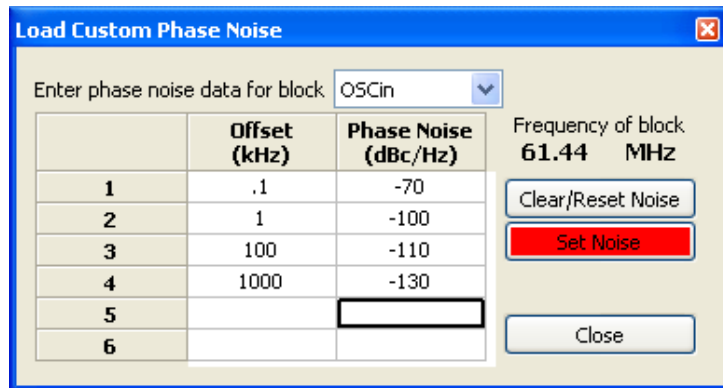
Figure 23: Entering custom phase noise for the reference clock.

Pressing "Enter Custom Phase Noise" button in Figure 22 opens the Load Custom Phase Noise screen.

Update the reference (OSCin) to be a noisy clock source.

- First, select OSCin from the block drop-down list.
- Next, enter the phase noise offsets and noise levels.

When complete, click on the flashing red "**Set Noise**" button to view the updated phase noise plot for CLKout3.   This will update the plot in Figure 22 and display Figure 30.

National's Clock Design Tool

Updated Phase Noise Plot from Custom OSCin Data
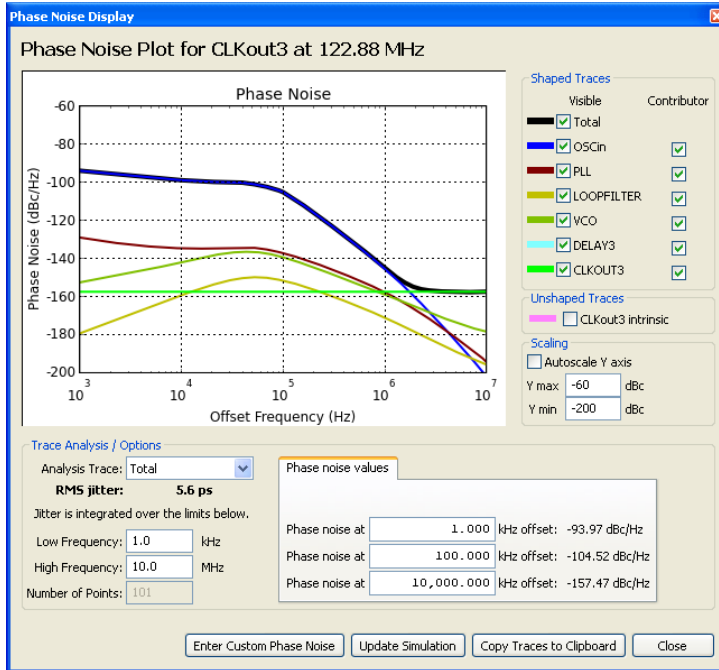
Figure 24: Phase noise plot with noisy clock and original loop filter design.

This is the updated phase noise plot for CLKout3 resulting from manually entering the "noisy" custom phase noise data for OSCin.

Note: the jitter measurement has increased from 183.8 fs to 5.6 ps. This is because the wide loop bandwidth is passing all the reference noise to the output.

To help mitigate the "noisy reference input," re-design the loop filter.

Mitigate Phase Noise by redesigning the loop filter

Figure 25: Loop filter block with loop filter calculator icon highlighted.

Press the calculator icon on the loop filter block to open the loop filter design screen.

Loop Filter Design – Redesigning loop filter

Figure 26: Before

Figure 27: After

The initial Loop Filter Design screen is shown in Figure 26. The parameters and loop filter values were automatically designed based on the original OSCin phase noise by the wizard mode when the simulation page was displayed.
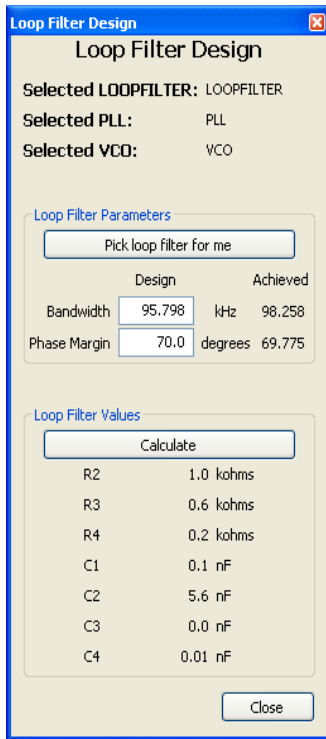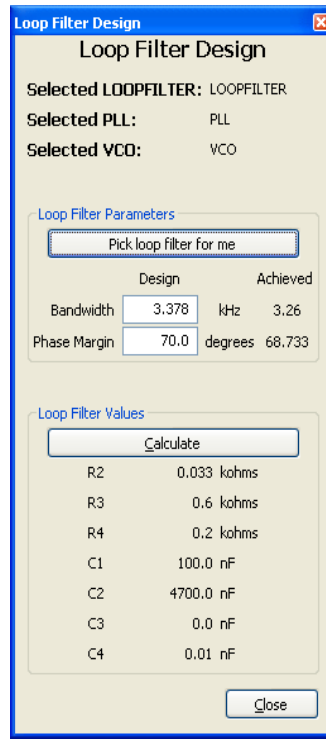
Now that the new OSCin phase noise has been entered, this loop filter is no longer optimum for minimum phase noise.

To automatically generate a loop bandwidth and phase margin, click on the "Pick loop filter for me" button. After clicking this button, the calculate button for Loop Filter Values will automatically be pressed to reflect the changes.

The before and after of the loop filter values are shown in Figure 26 and Figure 27.

Once the updated loop filter values are displayed, close the Loop Filter Design screen.

Next, go back to the CLKout3 Phase Noise Display to see how the updated loop filter values improve the noisy OSCin reference.

CLKout3 Phase Noise Display (after loop filter redesigned)
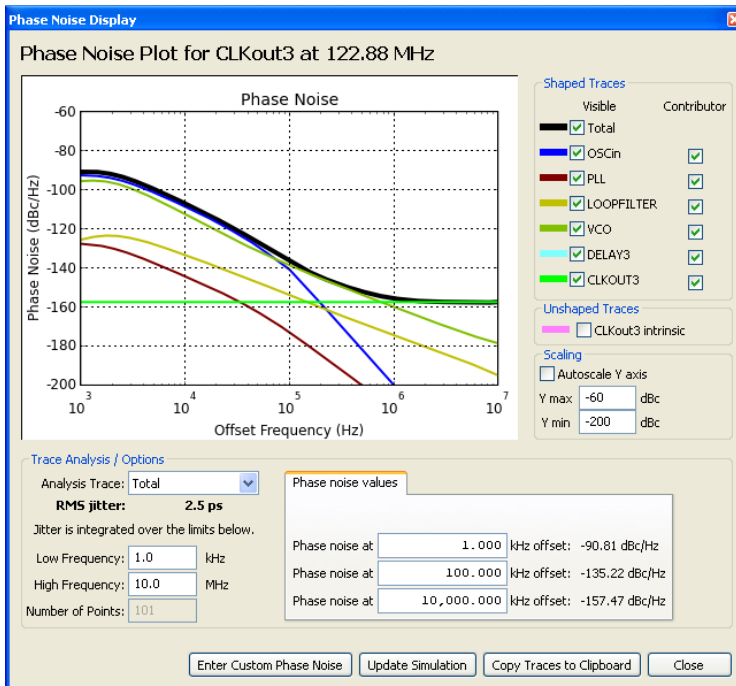
Figure 28: Phase noise plot with redesigned LOOPFILTER1.

If the Phase Noise Display was not closed when re-designing the loop filter, the "Update Simulation" button will be highlighted red and flashing. Clicking this button will update the phase noise plot based on the revised loop filter.

Note: If the Phase Noise Display screen was closed, re-opening it will automatically update the phase noise plot.

Since the integrated VCO performance is lower than the reference input beyond a certain offset (approximately the loop bandwidth), the narrower loop bandwidth allows the VCO to clean the dirty reference input rather than allow the PLL to pass the reference noise to the output.

The RMS jitter has improved from 5.6 ps to 2.5 ps. Note that an LC VCO can have high phase noise close to the carrier, like 10 Hz to 1 kHz compared to an external VCXO. If much of the jitter is close in, then it is probable that a dual loop architecture which uses an external VCXO will improve phase noise. The next step will revise the design to a dual loop architecture for comparison.

3.6)   Sixth - Compare with a Dual Loop Architecture

To continue the simulation, go back to the Customer Requirements screen by clicking the customer requirements green dot icon.

The same requirements from the original scenario are still populated.
- 61.44 MHz Reference (dirty)
- 3 Outputs
  - 122.88 MHz LVPECL
  - 122.88 MHz LVPECL
  - 30.72 MHz LVDS

Now change the architecture type from "Single PLL – LMK03000 and LMK02000 Family" to "Dual Loop PLL – LMK04000 Family."

Note: for the LMK04000 family, there is an additional tab available for a VCXO1 input. For this example, leave the VCXO1 tab at the default setting "Auto select best frequency".
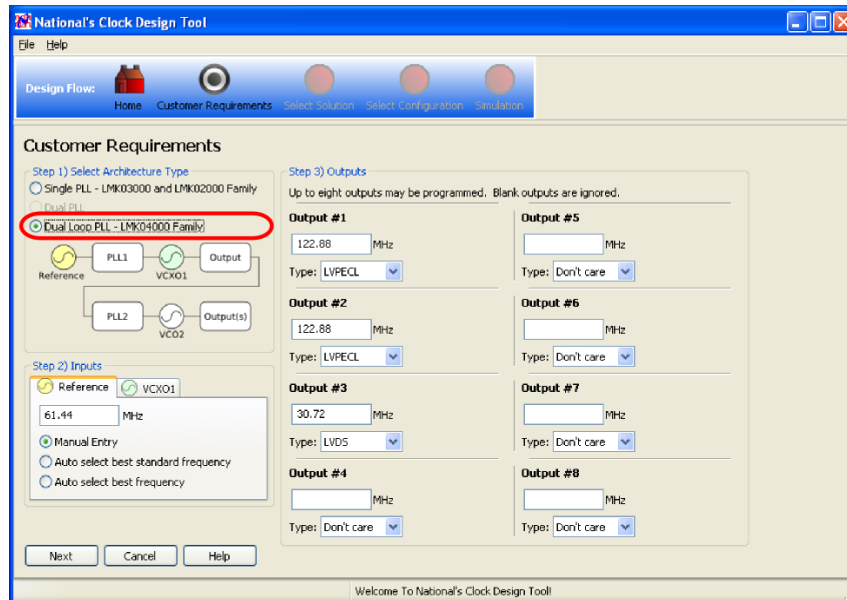
Figure 29: Changing Architecture type to "Dual Loop."

Now return to the simulation screen by using the default selections for both Select Solution screen and Select Configuration screen.

Select Solution Screen

As before, solutions capable of providing the output frequency requirements, given the input, as entered on the Customer Requirements screen are displayed. In this example, choose the default solution – LMK04031.
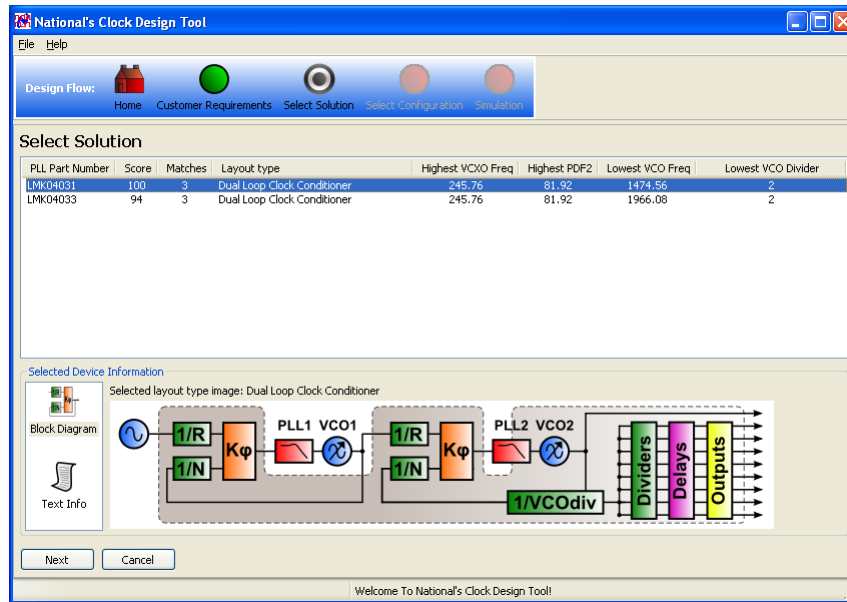
Figure 30: Select default device.

Select Configuration Screen

As before, choose the default highest scored configuration.
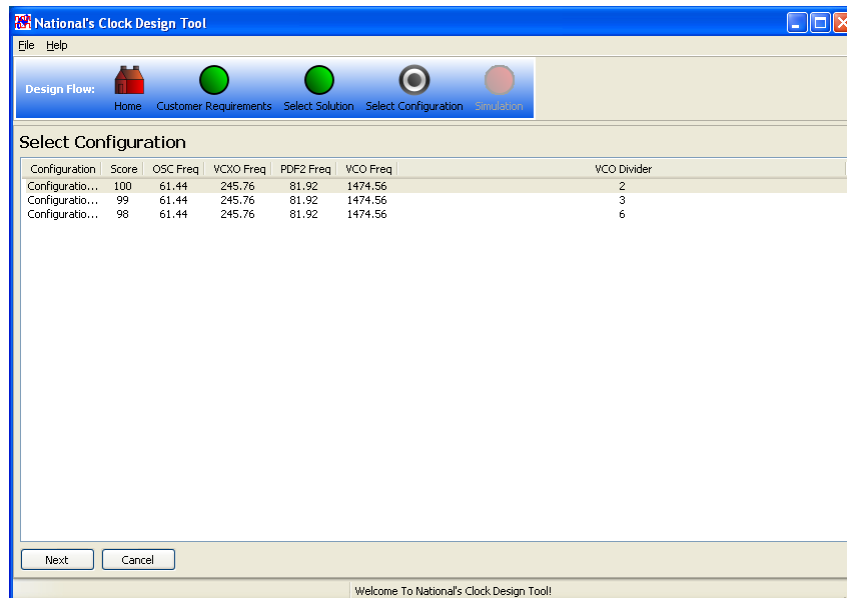
Figure 31: Select default configuration.

Simulation Screen

The simulation screen is shown with a dual loop architecture. Note that blocks for PLL1 and PLL2 exist.

The loop filter block for PLL1 is named LOOPFILTER1, the loop filter block for PLL2 is named LOOPFILTER2.

To view the phase noise display screen for CLKout3 click the phase noise button on the CLKout3 block.
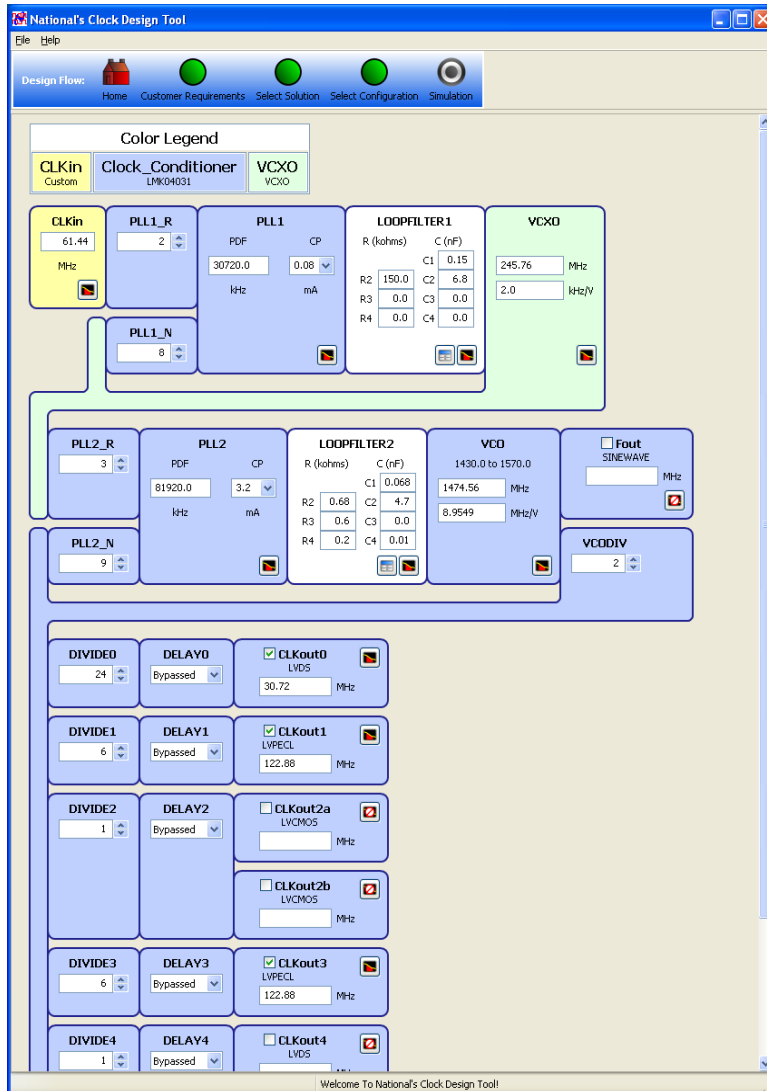
Figure 32: Dual loop architecture Simulation screen.

CLKout3 Phase Noise Plot (Dual Loop Initial)
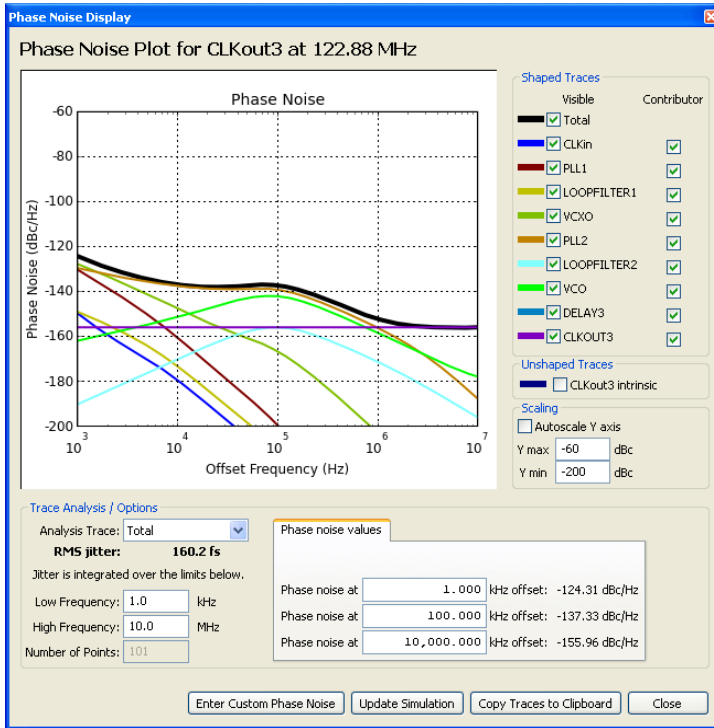
Figure 33: Dual loop architecture default phase noise plot.

In reviewing the output performance of CLKout3 at 122.88 MHz, this phase noise plot is displayed.

Notice the difference between the initial Phase Noise RMS jitter from the Single PLL and this plot:

- Single PLL = 183.8 fs
- Dual PLL = 160.2 fs

Next, simulate how the phase noise would be affected by loading custom phase noise data for the reference oscillator in the OSCin block.

Click on the "Enter Custom Phase Noise" button to update simulation data .

Custom Phase Noise Entry

Figure 34: Entering noisy reference, CLKin. (Note for LMK03000 Family the reference pin is called OSCin)

Select CLKin from the block drop-down list.

As per the user design, update the reference (OSCin) to be a noisy clock source.

- First, select OSCin from the block drop-down list.
- Next, enter the phase noise offsets and noise levels .

When complete, click on the flashing red "**Set Noise**" button to view the updated Phase Noise plot for CLKout3.

National's Clock Design Tool

Updated Phase Noise Plot from Custom CLKin Data
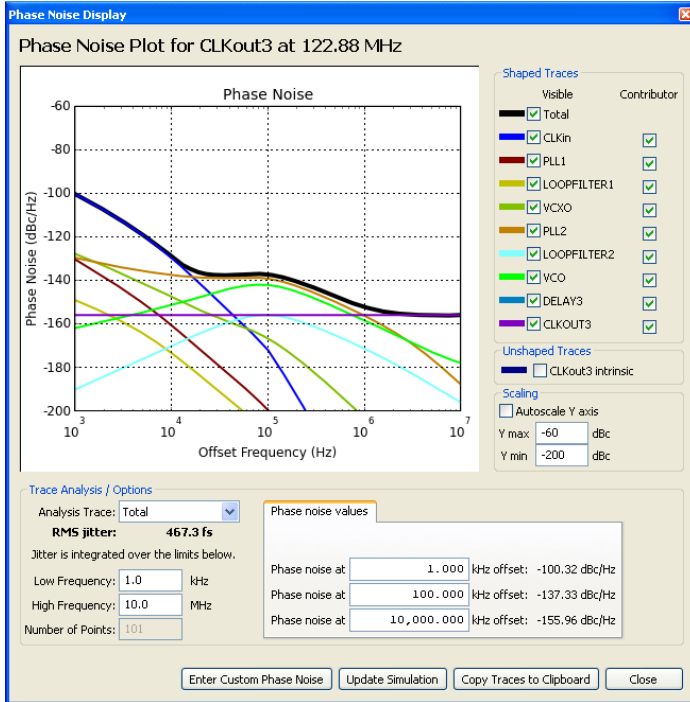
Figure 35: Dual loop architecture with noisy CLKin.

This is the updated phase noise plot for CLKout3 resulting from manually entering the "noisy" custom phase noise data for CLKin.

Note: the jitter measurement has increased from 160.2 fs to 467.3 fs. This is because the loop bandwidth of the VCXO is passing some of the reference noise to the output.

To help mitigate the "noisy reference input" just simulated, adjust the loop filter settings.

Note this time the noisy reference didn't cause the noise to increase as much as happened with the Single PLL. This is because the loop bandwidth of PLL1 is only 527 Hz while the Single PLL bandwidth was 98 kHz (Figure 26). The wider loop bandwidth, passed more noise to the output.

Mitigating Phase Noise – Update LOOPFILTER1 Settings
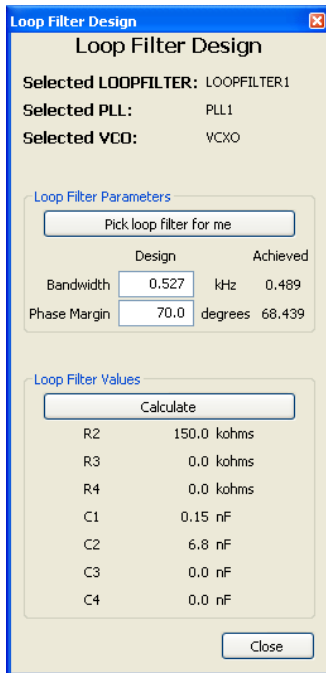
Figure 36: Before
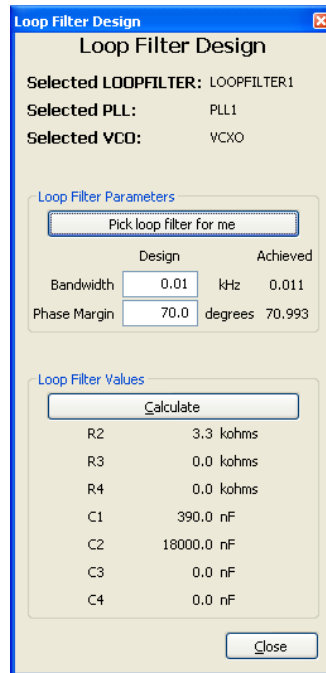
Figure 37: After

From the Simulation Screen, click on the loop filter calculator icon for LOOPFILTER1. Since the noise has to pass through this PLL first and this is the PLL which has a VCXO, we will use this PLL to "clean" the reference signal.

The initial Loop Filter Design screen is shown in Figure 36, this loop filter was designed using the original CLKin phase noise by the wizard mode when the simulation page was displayed.

Now that the new CLKin phase noise has been entered, this loop filter is no longer optimum for minimum phase noise.

To automatically guess a loop bandwidth and phase margin, click on the "Pick loop filter for me" button. After guessing at a loop bandwidth and phase margin, the calculate button will automatically be pressed to update the loop filter values.

The before and after of the loop filter values are shown in Figure 36 and Figure 37.

Once the updated loop filter values are displayed, close the Loop Filter Design screen. Next, go back to the CLKout3 Phase Noise Display to see how the updated loop filter values improve the noisy OSCin reference.

CLKout3 Phase Noise Plot (After Loop Filter Redesigned)
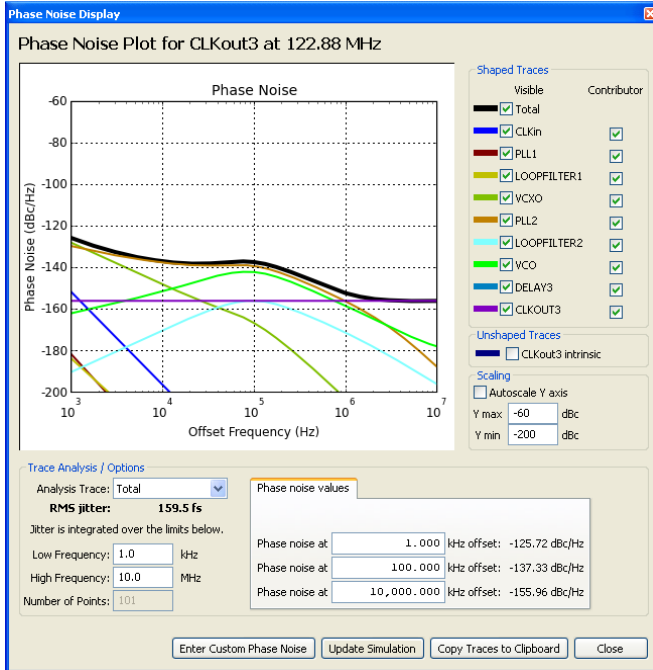
Figure 38: Dual loop architecture "cleaning" noisy CLKin.

As in the Single PLL example, when returning to CLKout3's phase noise plot – the Update Simulation button will need to be clicked (should be flashing in red) to display the new plot.

Notice the improved CLKin contribution and lowered RMS jitter performance.

Finally, compare the RMS jitter performance between the two examples:
- Single PLL – 2.5 ps
- Dual Loop PLL – 159.5 fs

It is important to recognize that the performance achieved by the Dual Loop PLL will depend on the noise performance of the VCXO used to clean the reference signal. Further, depending where the noise of the dirty reference is located at the Single PLL architecture may provide equally good performance – this typically occurs when the noise is beyond 10 kHz. Refer to AN-1734[2] for more information on this topic. When the noise of the reference clock is closer to the carrier, as in this example, the Dual Loop architecture shows it's value.

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2   See http://www.national.com/an/AN/AN-1734.pdf for more information on cleaning noisy clocks.

APPENDIX A – DUAL LOOP ARCHITECTURE

Dual Loop architecture theory

The dual loop architecture of the LMK04000 family permits a dirty reference signal to be cleaned, multiplied, and distributed.
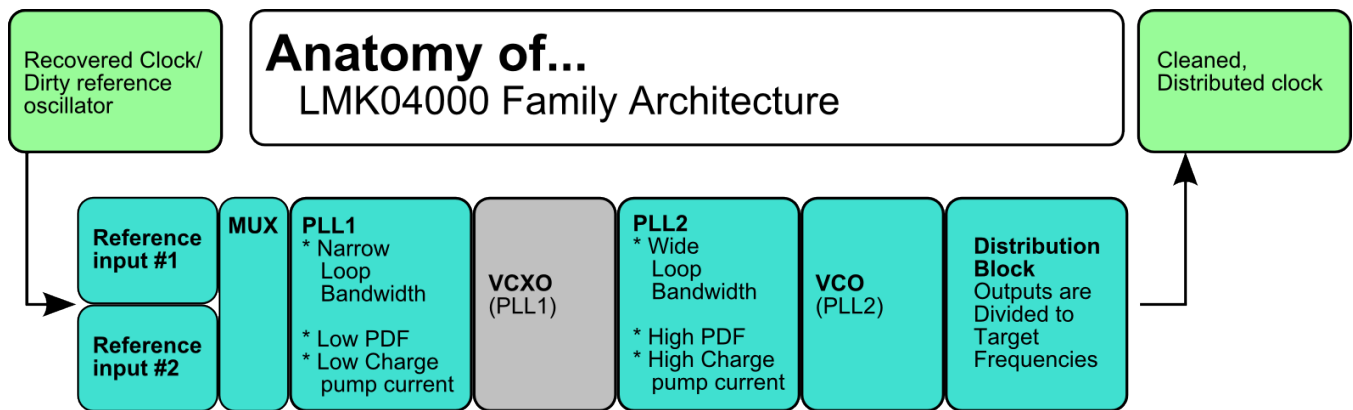
Figure 39: Anatomy of LMK04000

In the architecture shown in Figure 39, a signal with poor phase noise performance enters PLL1 and is cleaned with a low frequency/low cost VCXO. This becomes the new reference signal and is applied to PLL2 reference input. PLL2 with the LC VCO performs frequency multiplication of its clean reference. Finally the Distribution Block allows the high frequency LC VCO to be divided into the desired target frequencies resulting in low jitter clocks being distributed to target systems with skew control if needed.

Figure 40 examines what constitutes the output phase noise of any given PLL/VCO. Understanding the architecture in Figure 39 can be applied to understand the finer details of how the LMK04000 achieves its low phase noise even with a dirty reference oscillator. Figure 41 walks through the "life" of the reference signal from input into PLL1 to Distribution.
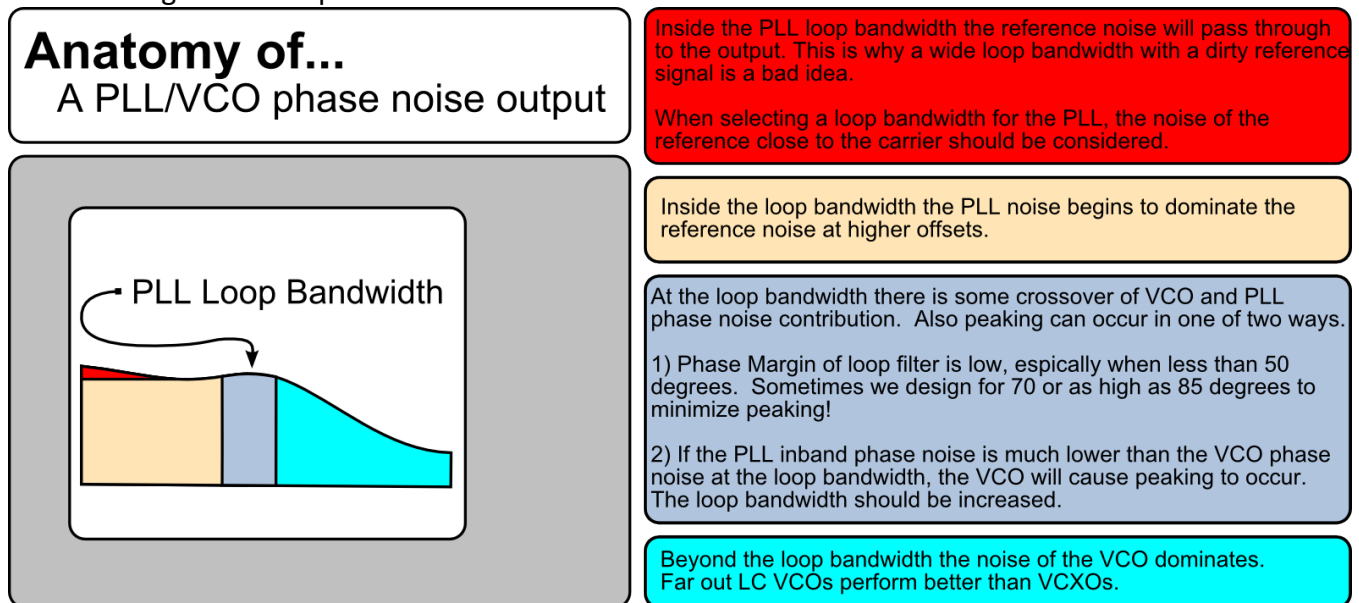
Figure 40: Anatomy of PLL/VCO phase noise output

LMK04000 Family in Action

A dirty signal's trip through an LMK04000 Family device

Refer to Figure 41 as reading through the following steps.

Step 1) The dirty signal is presented to the input of the LMK04000.

Step 2) Dirty signal goes into the reference input of PLL1. PLL1/VCXO has a very narrow loop filter designed so that the VCXO's noise will dominate the output of the PLL1/VCXO block. This is the cleaning portion of the process. The VCXO is selected for low cost and is typically a lower frequency. The higher the frequency of VCXO, the better for the step 4.

Step 3) Refer to Figure 40. This signal's blue area, the VCO (or VCXO) dominated area goes very close to the carrier.

Step 4) The signal of step 3 is presented to the reference input of PLL2. PLL2/VCO has a loop filter designed for optimum phase noise output. The optimum loop bandwidth of this filter is a frequency slightly greater than where the integrated VCO's and PLL2 phase noise crosses. The integrated VCO's phase noise when operating without a PLL is also shown. Note, the higher the phase detector frequency (the lower the N), and the higher the charge pump current – the lower the horizontal level of PLL in-band noise will be. The lower the in-band noise, the larger the loop bandwidth should be designed for optimum noise performance.

Step 5) Refer to Figure 40. This signal now looks a bit more like the one shown in the diagram, the low in-band phase noise of the PLL is "cleaning" the high close-in phase noise of the integrated VCO. The PLL is now able to "clean" the VCO without concern of a noisy reference.

Step 6) The multiplied frequency of the input is now available for distribution and division to target outputs. As the frequency is divided, the jitter of the signal will remain the same until the residual noise floor of the output buffers is reached. At this point the uniform scaling of frequency and phase noise profile is no longer valid. The frequency continues to lower but the phase noise profile does not increase measured jitter.

Step 7) Distribution of signal to targets.
7a – Output is in bypass mode. Output phase noise profile is slightly higher due to additive jitter.
7b – Output is divided, but not so much that the output buffer phase noise floors are reached. According to theory, 6 dB per division by two will be attained by the phase noise profile.
7c – Output is divided, but the theoretical 6 dB per division by 2 no longer applies. The residual phase noise of the output buffers has been reached at offsets further from the carrier.

Dirty Signal Cleaned by LMK04000 Family Device

Phase noise of VCXO Standalone

PLL1
* Narrow Loop Bandwidth
* Low PDF
* Low Charge pump current

2

VCXO (PLL1)

Recovered Clock/ Ditry reference oscillator

1

Clock with phase noise dominated by VCXO of PLL1

3

6

Distribution Block
Outputs are Divided to Target Frequencies

5

Cleaned Clock ready for distribution

150 fs RMS jitter

VCO (PLL2)

PLL2
* Wide Loop Bandwidth
* High PDF
* High Charge pump current

4

Phase noise of VCO Standalone

Output 1
Output 2
Output 3

7a

7b

7c

Distributed Clock Bypass.

+ additive jitter

151 fs RMS jitter

Distributed Clock Divide by 2.

~6 dB PN reduction
+ additive jitter

151 fs RMS jitter

Distributed Clock Divide by 4.

~12 dB PN reduction
+ additive jitter
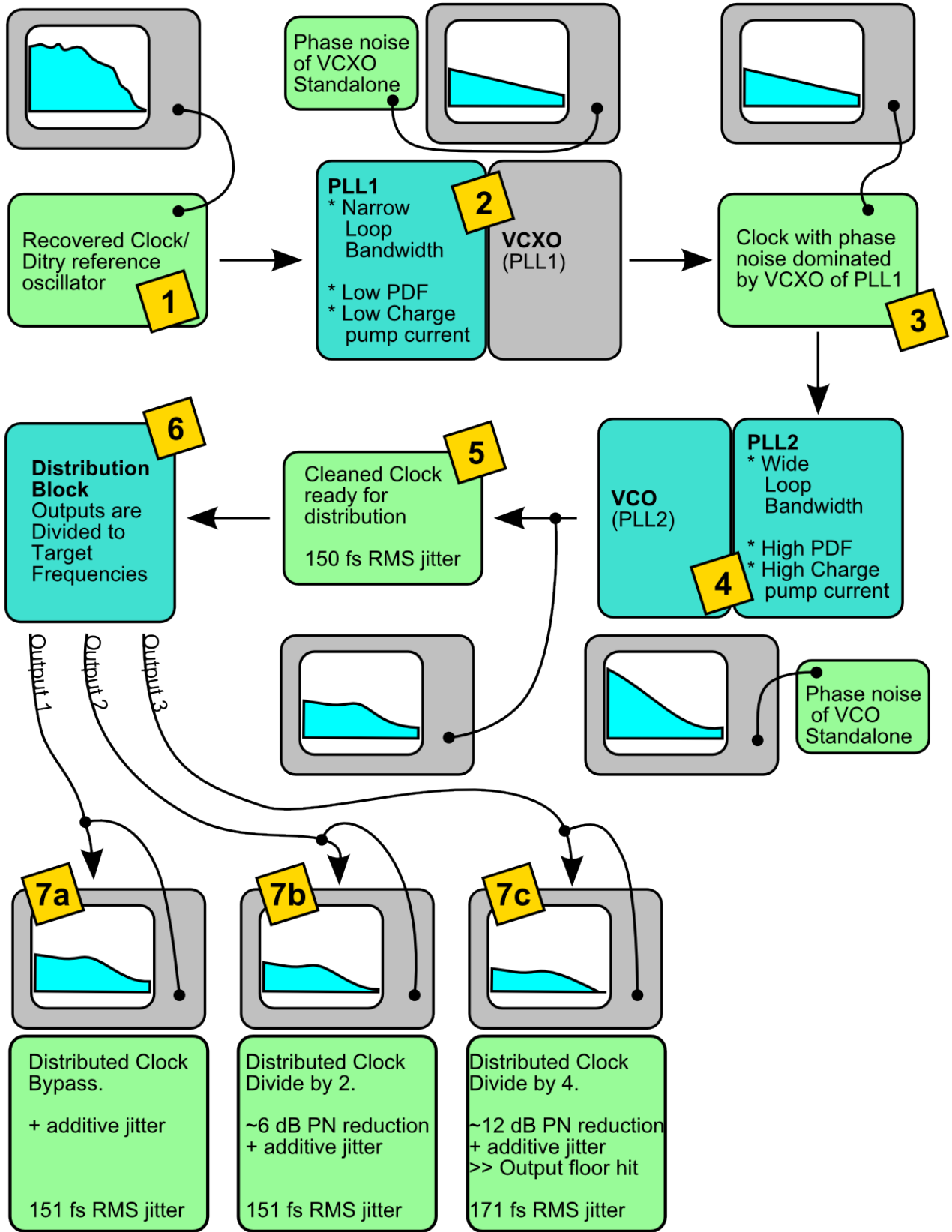>> Output floor hit

171 fs RMS jitter

Figure 41: Dirty Signal Cleaned with a Dual Loop architecture (LMK04000 Family)

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