Input Currents for High-Resolution ADCs

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ABSTRACT

Designing circuits using high-resolution ADCs (analog-to-digital converters) requires attention to many details. One detail often overlooked is the input impedance of the ADC. This becomes important as the output impedance of the source becomes high (e.g., when driven by a bridge or an RTD). This application report explains how the input sampling works and how input impedance can be calculated in the ADS1216, ADS1217, and ADS1218 family of ADCs.

This family of ADCs are of the delta-sigma ($\Delta\Sigma$) variety that use oversampling as a means of achieving high resolution.

These 24-bit, 8-channel ADCs offer precision and a wide dynamic range operating from 2.7V to 5.25V supplies. Internal buffers create high-impedance inputs allowing for direct connections to transducers or low-level voltage signals. The first product in this family is the ADS1216, which has an input range of $\pm V_{REF}$ (in PGA gain = 1). The ADS1218 takes the ADS1216 and adds on 4kBytes of flash memory. The ADS1217 is similar to the ADS1216 except that the input range is doubled to $\pm 2V_{REF}$ (in PGA gain = 1).

This application report also applies to the ADS1240, ADS1241, ADS1242, and ADS1243; a similar family of 24-bit ADCs with two and four input channels. Furthermore, this report applies to the MSC1210, MSC1211, and MSC1212, which incorporate a similar 8-channel ADC.

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1 Input Circuitry

To understand how input impedance can be calculated, it is important to see how the input circuits operate in this family of devices. The input circuit for the ADS1216, ADS1217, and ADS1218 are similar in operation. These parts sample the input signal by using internal capacitors that are continuously charged and discharged. Figure 1 shows the basic operation of the sampling of the modulator.
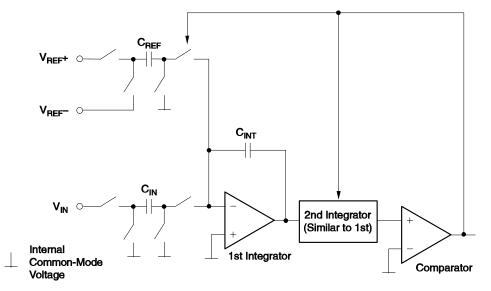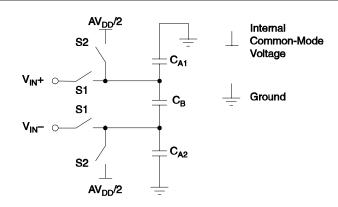

Figure 1. Differential Half-Circuit Representation of the Modulator in the ADS1216, ADS1217, and the ADS1218
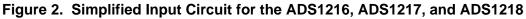
The input is sampled and integrated with samples of the reference. It passes through a second integrator and then a comparator. The comparator outputs a pulse-width modulated signal that has a density proportional to the input signal.

Figure 1 should be seen as a representation of the sampling used to get the input signal. Note that it uses a differential half-circuit representation. The actual circuitry has a differential input with a $V_{IN}+$ and $V_{IN}-$ input.

The input can be modeled in the following circuit shown in Figure 2. The timing diagram is shown in Figure 3. In this circuit, charge is sampled by a capacitor and discharged to an internal common-mode voltage (roughly $AV_{DD}/2$). The input impedance is determined by the size of the input sampling capacitor, the clock frequency of the input stage, and the common-mode input voltage. In the sampling of the input, C_B models the input sampling of C_{IN}. C_{A1} and C_{A2} model the transfer of charge from the sampling capacitor to the integrator as it is tied to an internal common-mode voltage.

Figure 2. Simplified Input Circuit for the ADS1216, ADS1217, and ADS1218

Figure 3. Timing Diagram for the Input Switches

Consider first a simple capacitor that is charged and discharged as shown in Figure 4 with the same switch timing shown in Figure 3. Current is defined as the change in charge over time. The switched capacitor charges and discharges, pulling a fixed amount of charge with each clock cycle from the inputs.

Figure 4. Simple Switched Capacitor Example

The average current load (I_{AVG}) of this circuit is:

$$I_{AVG} \equiv \frac{Q}{t} = \frac{CV}{t} = CVf_{CLK}$$

(1)

Defining the effective impedance as Z_{eff}:

$$Z_{eff} \equiv \frac{V}{I_{AVG}}$$

(2)

The resulting combination with Equation 1 results in:

$$Z_{eff} = \frac{1}{Cf_{CLK}}$$

(3)

Applying these equations to the effective input circuit in Figure 2, we get the following model for input resistance of the ADS1216, ADS1217, and ADS1218. Z_{effA1} and Z_{effA2} are the same size (approximately half of Z_{effB}). As mentioned before, the internal common-mode voltage is typically $AV_{DD}/2$.

Figure 5. Effective Input Impedances for the ADS1216, ADS1217, and ADS1218
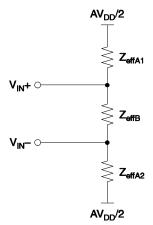
The inputs switches are not run at the clock frequency of the device. They run off of either the modulator clock speed or multiples of it as the PGA is increased (this is explained further as the input current changes with the PGA). This MODCLK runs at a frequency of f_{MOD} and is determined by the external clock (f_{OSC}) and the SPEED bit in the setup register. Table 1 shows how f_{MOD} changes with the SPEED bit.

Table 1. The SPEED Bit as it Relates Clock Frequency and Modulator Frequency

SPEED BIT	f_{MOD}
0 (default)	$f_{OSC}/128$
1	$f_{OSC}/256$

As different frequency oscillators are used, the input impedance will change. Table 2 gives examples of the input impedance values as the clock frequency changes, with the PGA in a gain of 1 and the SPEED bit off. The values of the ADS1216 and ADS1218 are identical. In the ADS1217, the sampling capacitors are half of their counterparts and, therefore, the input impedances are approximately twice as large.

Table 2. Oscillator Frequency vs Input Impedance, PGA = 1, SPEED Bit Off, Buffer Off

f_{OSC} (MHz)	f_{MOD} (kHz)	ADS1216,1218		ADS1217	
		Z_{effA} (MΩ)	Z_{effB} (MΩ)	Z_{effA} (MΩ)	Z_{effB} (MΩ)
1	7.81	32	15	48	25
2	15.6	16	7.5	24	13
2.45	19.2	13	6.1	20	10
4	31.3	8.0	3.8	12	6.3
4.91	38.3	6.5	3.1	10	5.1
8	62.5	4.0	1.9	6.0	3.1

TEXAS INSTRUMENTS

2   Input Impedance and Gain

A PGA ranging from 1 to 128 is implemented in the integrator. Gain is achieved in this family of ADCs by either changing the size of the sampling capacitor (C_{IN}) or the reference sampling capacitor (C_{REF}) along with the clock frequency of the first integrator. Both will affect the input impedance of the circuit.

Referring back to the circuit shown in Figure 1, Table 3 shows how C_{IN}, C_{REF}, and the sampling frequency change with gain.

Table 3. PGA Gain vs Sampling Frequency

PGA	Full-Scale Input Voltage	C_{IN} (pF)	C_{REF} (pF)	1st Integrator CLK Frequency (kHz)
1	$\pm V_{REF}$	9	12	f_{MOD}
2	$\pm V_{REF}/2$	18	12	f_{MOD}
4	$\pm V_{REF}/4$	36	12	f_{MOD}
8	$\pm V_{REF}/8$	36	6	f_{MOD} x 2
16	$\pm V_{REF}/16$	36	3	f_{MOD} x 4
32	$\pm V_{REF}/32$	36	1.5	f_{MOD} x 8
64	$\pm V_{REF}/64$	36	0.75	f_{MOD} x 16
128	$\pm V_{REF}/128$	36	0.375	f_{MOD} x 16

Values for the input sampling capacitors shown are for the ADS1216 and ADS1218. The full-scale input voltage for the ADS1217 is double the given input ranges and the C_{IN} values are half the given values for each PGA gain.

Given the oscillator frequency, the input impedance can be calculated. If the clock frequency is 2.4576MHz, the input impedance will be approximately:

$$Z_{eff} = \frac{1}{C_{IN}(f_{SAMP})}$$

(4)

Table 4. PGA Gain vs Input Impedance, XTAL = 2.4576MHz, SPEED Bit Off, Buffer Off

PGA	ADS1216,1218		ADS1217	
	Z_{effA}	Z_{effB}	Z_{effA}	Z_{effB}
1	13MΩ	6.1MΩ	20MΩ	10MΩ
2	6.5MΩ	3.1MΩ	10MΩ	5.1MΩ
4	3.3MΩ	1.5MΩ	5.0MΩ	2.6MΩ
8	1.6MΩ	760kΩ	2.5MΩ	1.3MΩ
16	820kΩ	380kΩ	1.3MΩ	640kΩ
32	410kΩ	190kΩ	630kΩ	320kΩ
64	200kΩ	90kΩ	310kΩ	160kΩ
128	200kΩ	90kΩ	310kΩ	160kΩ

It is important to note where the impedances come from. The PGA in gains of 1, 2, and 4 is implemented by changing the input sampling capacitor (as shown in Table 3). In these first three gains, the sampling frequency remains the same. The remaining gains are implemented by changing the sampling of the input signal. For the PGA in gains of 8, 16, 32, and 64, the sampling frequency doubles at each gain. At a PGA gain of 128, the input impedance does not change from a gain of 64.

The values in Table 4 are valid when the part is working in the normal operating range. When the inputs go beyond the given full-scale range, the input impedance may seem larger. The reason is because the op amp in the first modulator loses the ability to fully drive the charge out of the input sampling capacitors in the sampling phase, thus reducing the current that is drawn from the inputs.

3 Input Impedance with the Buffer On

In some applications, low input impedance can adversely affect the measurement. For these cases, the ADS1216, ADS1217, and ADS1218 (as well as the ADS1240, ADS1241, ADS1242, ADS1243, MSC1210, MSC1211, and MSC1212) have input buffers that can be used to increase the input impedance. Although it is not infinite, the input impedance is greatly increased from normal operation.

The inputs of the ADS1216, ADS1217, and ADS1218 have a multiplexer that allows the user to select operation of any of the eight input channels. After the multiplexer, a chopper technique is used prior to the buffer to remove offset and 1/f noise of the buffer. Figure 6 shows the circuitry around the input buffer.
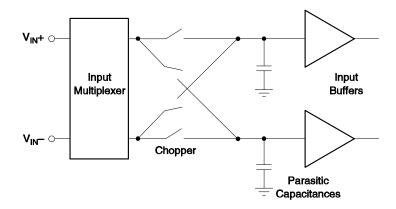

Figure 6. The Input Shown with the Input Multiplexer and the Buffer

As the buffer is used, the input switches that sample the signal are fed directly by the buffers. This eliminates the normal input impedance that is seen from the input sampling. However, the chopper before the buffer shown in Figure 6 contributes to the input resistance. The inputs are switched from $V_{IN}+$ to $V_{IN}-$. Parasitic capacitances that sit on the inputs of the buffer are then charged to either $V_{IN}+$ to $V_{IN}-$. The resulting equivalent circuit is a simple resistor. Unlike the equivalent model in the non-buffer case, there is only a differential resistive component and no common-mode resistive components. The equivalent input impedance is shown in Figure 7.
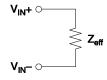

Figure 7. The Equivalent Input Resistance of the ADS1216, ADS1217, and ADS1218, Input Buffer On

It is important to note that this resistance is a function of chopper frequency and the parasitic capacitance alone. It is the same for the ADS1216, ADS1217, and ADS1218. More importantly, it is the same for all PGA gains. It is only changed by the oscillator frequency and the SPEED bit. Approximate input impedances are given in Table 5.

Table 5. Oscillator Frequency vs Input Impedance with the Buffer On for All PGAs, SPEED Bit Off

f_{OSC} (MHz)	Z_{eff} (G)
1	12
2	6.0
2.45	4.9
4	3.0
4.91	2.4
8	1.5

With the SPEED bit on, the input impedances are twice the given value because the chopping is done at half the original rate.

In addition to the parasitic capacitances that cause an input impedance, there is also the affect of the multiplexer on the input current. As with all multiplexers, the switches that select the input channel are transistors, the drain and sources of which are reverse bias to the body of the device. Like the reverse bias current of a diode, this will have a leakage term that doubles every 5°C to 10°C. Luckily, the switches are small and the current is always smaller than even the input currents with the buffers on (roughly 0.1nA at 85°C).

4 Conclusion

The ADS1216, ADS1217, and ADS1218 are 24-bit $\Delta\Sigma$ ADCs that require attention to detail to achieve high performance. One important detail that is often overlooked is the current that goes into the input sampling ciruitry.

This application report has examined factors that may affect that input impedance. These factors include the clock frequency, the SPEED bit, the gain of the device, and the use of the input buffers. All of these factors can influence the accuracy of the measurement, especially if using a measurement source with a high output impedance.

Although this report concentrates on the ADS1216, ADS1217, and ADS1218, it also applies to another family of similar parts. The ADS1240, ADS1241, ADS1242, and ADS1243 use the same input structure as the ADS1216 and ADS1218. The ADS1240 and ADS1242 are 24-bit, 2-channel ADCs, whereas the ADS1241 and ADS1243 are 24-bit, 4-channel ADCs.

This application report can be useful in working with the MSC1210, MSC1211, and MSC1212, which use a similar 24-bit, 8-channel ADC and combines it with an enhanced 8051 core with on-chip flash memory.

Each comes with different functionality and pin counts. Refer to the data sheets, located at www.ti.com, for more information.

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