Application Report
SBAA159–December 2008

Using the ADS1672 in Digital Filter Bypass Mode

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ABSTRACT

Data acquisition systems that must be very flexible and provide a high level of precision are often not economical to produce. Frequently, the only solution to designing such a system is to take the modulator output of a high-precision, delta-sigma (ΔΣ) data converter and marry it with programmable logic, such as a focal-plane grid array (FPGA). This paper discusses how to use the high-speed, multi-bit ADS1672 from Texas Instruments in digital filter bypass mode.

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1 Introduction

The ADS1672 is a high-speed, high-precision analog-to-digital converter (ADC). This converter was built using advanced multi-bit delta-sigma architecture. The chopper-stabilized front end gives the converter low drift and low offset characteristics. The converter features two digital filters. The first filter (wide bandwidth) was designed to for ac, wide-bandwidth applications. The filter response provides very little passband ripple up to 305 kHz. The second filter (low latency) was designed for applications where low latency is required, but a flat passband transfer curve is not essential. Low-latency applications typically involve step signals and/or multiplexed analog channels.

Measurement and automated test systems must be able to measure a plethora of input signals. These signals can vary in signal amplitude as well as frequency content. Additionally, the time required to digitize these signals can vary. In the case of feedback systems, for instance, it is important that the cycle latency be as short as possible. Cycle latency is the period from when the converter starts to acquire the signal and the time it takes for an accurate representation of that signal to arrive at the output.

Data acquisition systems that require a great deal of flexibility are often configured to change the transfer curve of the data converter by varying the back-end digital filter. This back-end digital filter determines the group delay, conversion accuracy, and cycle latency of the converter.

The ADS1672 can be operated in digital filter bypass mode. In bypass mode, the onboard digital filters are shut down and the modulators outputs are directly connected to the pins of the converter. These output streams can be combined using error cancellation logic, and then fed into a custom filter configuration to achieve the desired filter response and system characteristics.

Figure 1 illustratees the concept of a flexible data acquisition system with the ADS1672 and an FPGA.

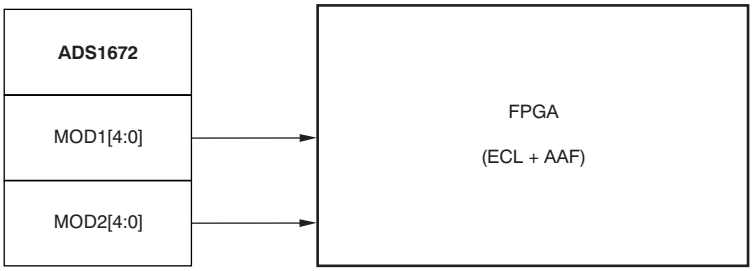


Figure 1. Flexible Data Acquisition System Block Diagram

2 ADS1672 Bypass Mode Pinout

In Figure 2, the ADS1672 operates in bypass mode at power-up with the pinout shown. The state of pins 14 through 17 sets the mode to either bypass mode or normal mode. If the pins are grounded, the part operates in normal mode. If all the pins are set to DVDD, the part runs in normal mode at power-up.

Using the ADS1672 in bypass mode re-assigns a total of 14 pins. The new pinout is shown in Figure 2. Shaded pins indicate a change to the pin configuration from the standard device pinout.

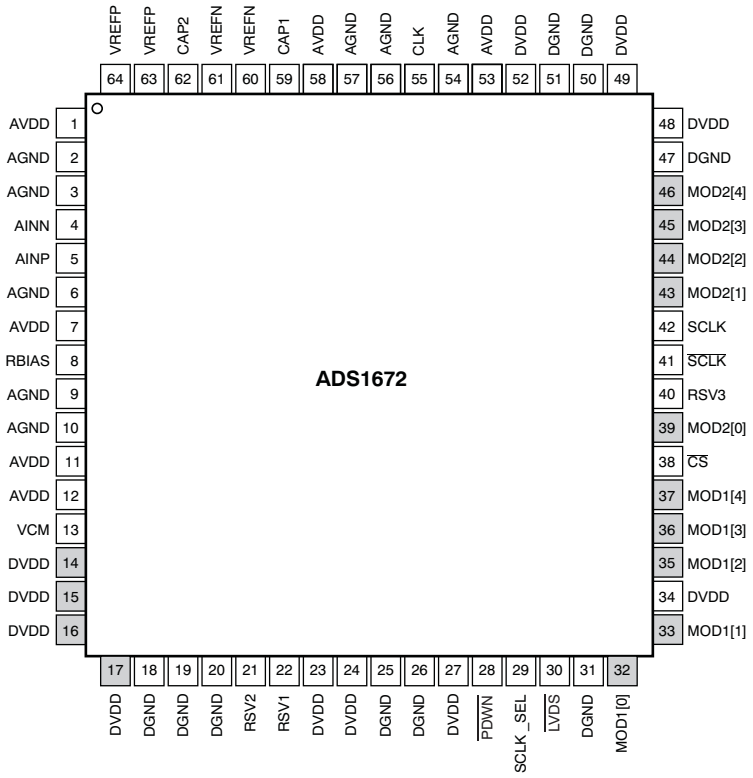


Figure 2. Bypass Mode Pinout

Table 1 provides a detailed description of the pin configuration for the ADS1672 in bypass mode.

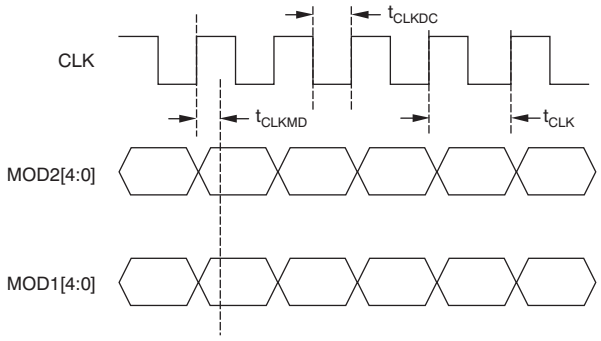
Table 1. ADS1672 Bypass Mode Pin Configurations

Pin		Input/Output	Description
Name	**No.**		
AVDD	1, 7, 11, 12, 53, 58	—	Analog supply pins
AGND	2, 3, 6, 9, 10, 54, 56, 57	—	Analog ground
AINN	4	Input	Negative analog input
AINP	5	Input	Positive analog input
RBIAS	8	—	Analog bias setting resistor
VCM	13	—	Terminal for external bypass capacitor connection to internal common-mode voltage. Connect 1-μF capacitor to ground.
DVDD	14, 15, 16, 17, 23, 24, 27, 34, 48, 49, 52	—	Digital supply pins
DGND	18, 19, 20, 25, 26, 31, 47, 50, 51	—	Digital ground
RSV2	21	—	Reserved pin. Short to DGND.
RSV1	22	—	Reserved pin. Short to DGND.
$\overline{\text{PDWN}}$	28	Input	Power-down control; active low.
SCLK_SEL	29	Input	Set to DGND.
$\overline{\text{LVDS}}$	30	Input	Set to DGND.
MOD1[0]	32	Output	Modulator 1, bit 0; LSB.
MOD1[1]	33	Output	Modulator 1, bit 1
MOD1[2]	35	Output	Modulator 1, bit 2
MOD1[3]	36	Output	Modulator 1, bit 3
MOD1[4]	37	Output	Modulator 1, bit 4; MSB.
$\overline{\text{CS}}$	38	-	Leave floating.
MOD2[0]	39	Output	Modulator 2, bit 0; LSB.
RSV3	40	—	Reserved; this pin must be left floating. Do not connect or short to ground.
$\overline{\text{SCLK}}$	41	—	This pin must be left floating. Do not connect or short to ground.
SCLK	42	—	This pin must be left floating. Do not connect or short to ground.
MOD2[1]	43	Output	Modulator 2, bit 1
MOD2[2]	44	Output	Modulator 2, bit 2
MOD2[3]	45	Output	Modulator 2, bit 3
MOD2[4]	46	Output	Modulator 2, bit 4
CLK	55	Input	Master clock input
CAP1	59	—	Terminal for 1-μF external bypass capacitor
VREFN	60, 61	Input	Negative reference voltage. Short to analog ground.
CAP2	62	—	Terminal for 1-μF external bypass capacitor
VREFP	63, 64	Input	Positive reference voltage

3 Digital Interface Timing

The advanced architecture of the ADS1672 consists of two modulators. Data from these two 5-bit modulators must be latched on the falling edge of every modulator (CLK) clock cycle. The raw data streams from both modulators must then be processed through error cancellation logic before being processed by the digital filter. This error cancellation logic generates a 7-bit representation of the input signal.

Figure 3 shows the modulator data retrieval timing sequence. Table 2 summarizes the timing requirements for this sequence.



Note: Chip select is tied low.

Figure 3. Modulator Data Retrieval Timing

Proposed timing requirement conditions: At T_A = –40°C to +85°C, AVDD = 5 V, DVDD = 3 V.

Table 2. Timing Requirements for Figure 3

SYMBOL	DESCRIPTION	MIN	TYP	MAX	UNIT
t_{CLK}	CLK period ($1/f_{CLK}$)	50			ns
t_{CLKMD}	CLK rising edge to Modulator 1 and Modulator 2 data valid.		14		ns
t_{CLKDC}	CLK pulse low width	0.45		0.56	t_{CLK}

4 Error Cancellation Logic (ECL)

As noted earlier, the data output from the two 5-bit modulators must be processed through error cancellation logic. This error cancellation logic generates a 7-bit signed representation of the input signal. Modulator outputs are unsigned values.

Modulator 1 (MOD1) and Modulator 2 (MOD2) outputs must be combined to form a 10-bit digital word using Equation 1.

$$\text{Digital Word} = (\text{MOD1} - 8) \times 4z^{-3} + \text{MOD2} \times (1 - 2z^{-1} + z^{-2}) \quad (1)$$

Where:

- MOD1: 5-bit output from Modulator 1.
- MOD2: 5-bit output from Modulator 2.

5 Application Test Results

The hardware for this application can be configured as shown in Figure 4. The modulator (CLK) should be a clean square wave in order to achieve specified datasheet linearity. The output data from the modulator are available on every falling clock edge.

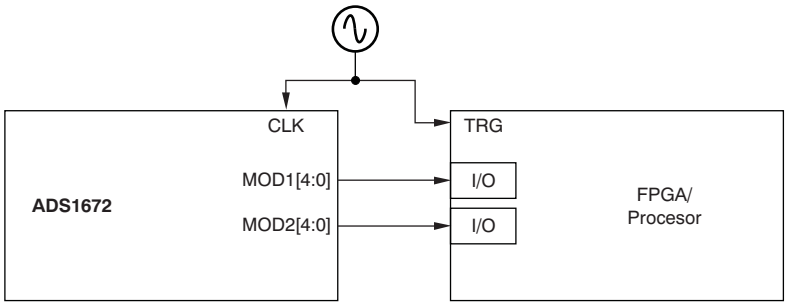


Figure 4. Hardware Connections

The processor (or FPGA) that captures the data must process the data through the error cancellation circuit. The output can then be post-processed, as Figure 5 shows.

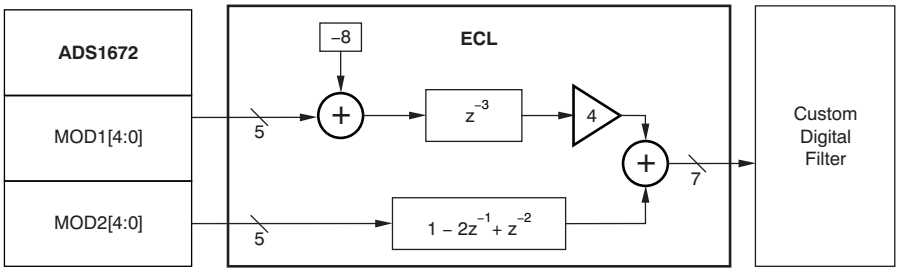


Figure 5. Full System Block Diagram

The latency of this system is five clock cycles, as Figure 6 shows. The data are sampled on the falling clock edge and available at the modulator output one-half clock cycle later. This output sample *N* can be latched into the error correction logic on the falling edge. After the three clock delays through ECL, the digital representation of sample *N* is available.

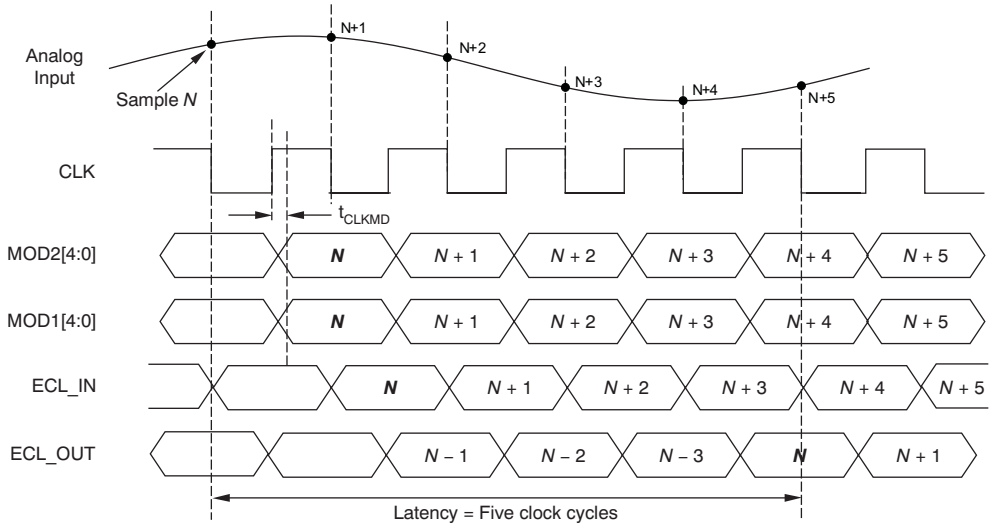


Figure 6. Cycle Latency

The data for the graphs shown in Figure 7 through Figure 12 were collected with the ADS1672 in bypass mode. The back-end implementation of the error cancellation logic and a *brick wall* filter (SNR BW of 312.5 kHz) was implemented on a PC. The tones shown in Figure 7 are tones from the chopper front end. These tones are sufficiently attenuated by the on-chip digital filters and thus do not alias back into the baseband.

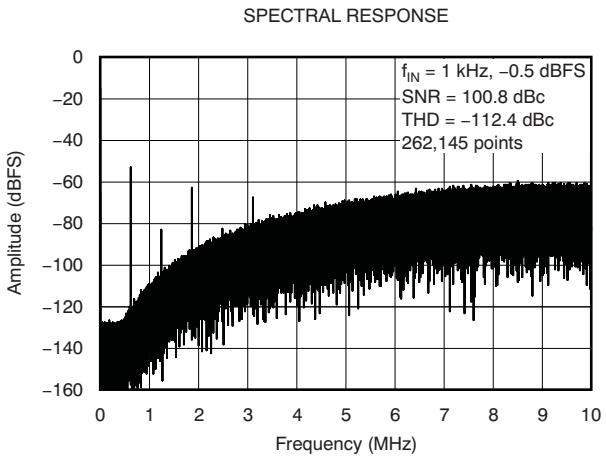


Figure 7. Spectral Response of Modulator Output at f_{IN} = 1 kHz, –0.5 dbFS

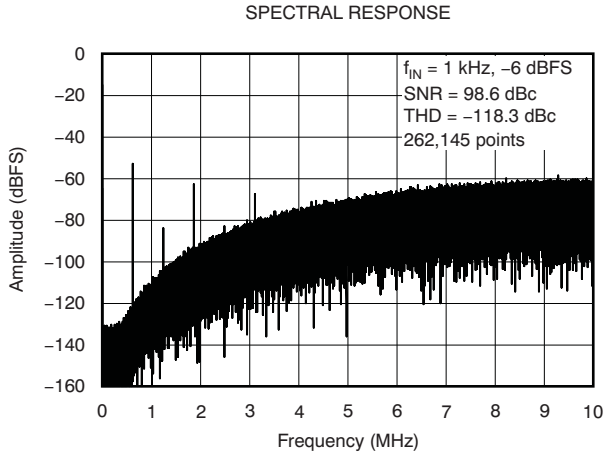


Figure 8. Spectral Response of Modulator Output at f_{IN} = 1 kHz, –6 dbFS

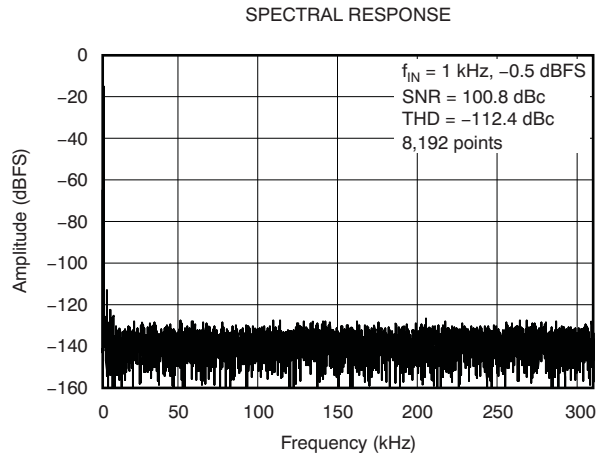


Figure 9. FFT After 312.5 kHz *Brick Wall* Filter at f_{IN} = 1 kHz, –0.5 dbFS

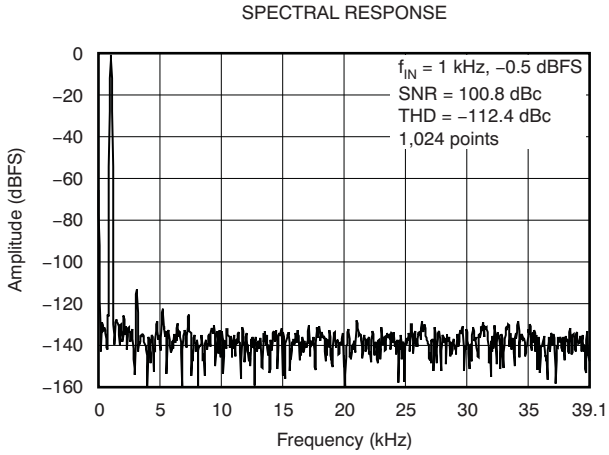


Figure 10. Enlarged View (8x) of FFT After 312.5 kHz *Brick Wall* Filter at f_{IN} = 1 kHz, –0.5 dbFS

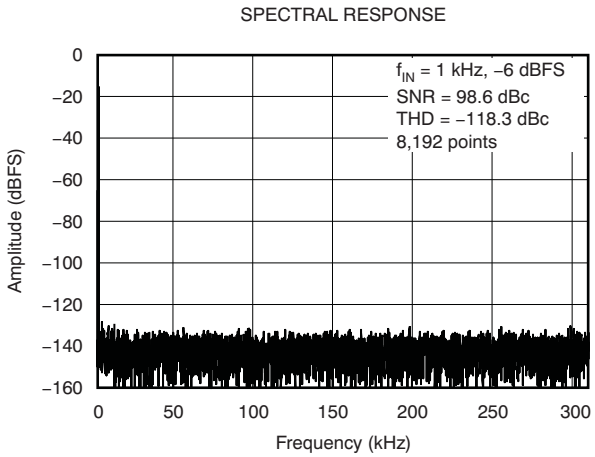


Figure 11. FFT After 312.5 kHz *Brick Wall* Filter at f_{IN} = 1 kHz, –6 dbFS

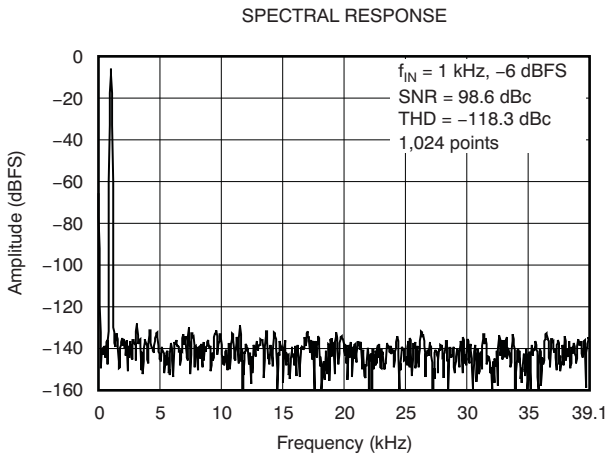


Figure 12. Enlarged View (8x) of FFT After 312.5 kHz *Brick Wall* Filter at f_{IN} = 1 kHz, –6 dbFS

6 Conclusion

Although not shown or discussed here, dc performance of the ADS1672 ADC is also entirely a result of the analog portion of the chip (that is, the modulators). The digital filters of the ADC help to reduce the overall noise and attenuate out-of-band noise. It does not improve or degrade the linearity, offset error, gain error, and other critical specifications of the chip. Achieving specified datasheet performance is possible with careful analog circuit layout and proper digital filter design.

Using the ADS1672 in bypass mode is a very attractive solution for measurement and automated test systems that must measure an abundance of input signals and respond appropriately.

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