

# Circuit for Offset Adjustment of Input Signals Using Precision DAC for Measurement Equipment



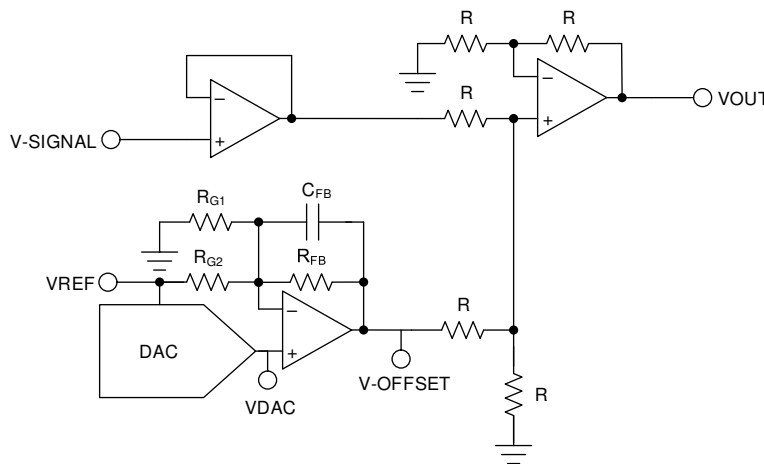
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## Design Goals

Power Supply	DAC Output	Voltage Output	Current Output
VCC: 24V, VSS: -5V, VDD: 5V	0V to 2.5V	0V to 5V	0A to 10A

## Design Description

Signal-measurement equipment like the *oscilloscope (DSO)* and *data acquisition (DAQ)* must manage input signals that are not within the input range of the measurement analog-to-digital converter (ADC). To bring the unknown input signal in the measurement range of the ADC, the first operation needed is offset control. A programmable offset control circuit providing both positive and negative offset, performs this function. This circuit uses a precision digital-to-analog converter (DAC), followed by a unipolar-to-bipolar conversion circuit using an op amp. The output of this circuit is fed to a summing amplifier that adds this DC output to the input signal.



## Design Notes

1. Choose a DAC with the required resolution and output range
2. Choose an op amp with low offset and low drift to minimize error. Thermal noise can be an additional requirement in some applications
3. Choose  $R_{G1}$ ,  $R_{G2}$ , and  $R_{FB}$  such that the desired output offset is met
4. Choose the compensation capacitor  $C_{FB}$  such that it is larger than the input capacitance of the op-amp inputs

## Design Steps

1. Select the DAC80504 device: a 16-bit, 4-channel buffered voltage output DAC with 2.5V internal reference. Devices with an external reference option or devices with accessible internal references are desirable in this application as the reference is used to create an offset. The DAC selection in this design should primarily be based on DC error contributions, typically described by offset-error, gain-error, and integrated non-linearity (INL) error.

2. Select an op amp such as the OPA227 operational amplifier that combines low noise and wide bandwidth with high precision to make it the optimal choice for applications requiring both AC and precision DC performance. Amplifier input offset voltage ( $V_{OS}$ ) is a key consideration for this design.  $V_{OS}$  of an operational amplifier is a typical data sheet specification, but in-circuit performance is also impacted by drift overtemperature, the common-mode rejection ratio (CMRR), and power supply rejection ratio (PSRR); therefore, give consideration to these parameters as well.
3. The DC transfer function of the offset voltage is given by:

$$V_{\text{OFFSET}} = V_{\text{DAC}} \left( 1 + \frac{R_{\text{FB}}}{R_{\text{G2}}} + \frac{R_{\text{FB}}}{R_{\text{G1}}} \right) - V_{\text{REF}} \left( \frac{R_{\text{FB}}}{R_{\text{G2}}} \right)$$

- First, using the previous transfer function, consider the negative full-scale output case when  $V_{\text{DAC}}$  is equal to 0V,  $V_{\text{REF}}$  is equal to 2.5V, and  $V_{\text{OFFSET}}$  is equal to -5V. This case is used to calculate the ratio of  $R_{\text{FB}}$  to  $R_{\text{G2}}$  and is shown in the following equation:

$$-5\text{V} = -\frac{R_{\text{FB}}}{R_{\text{G2}}}(2.5\text{V})$$

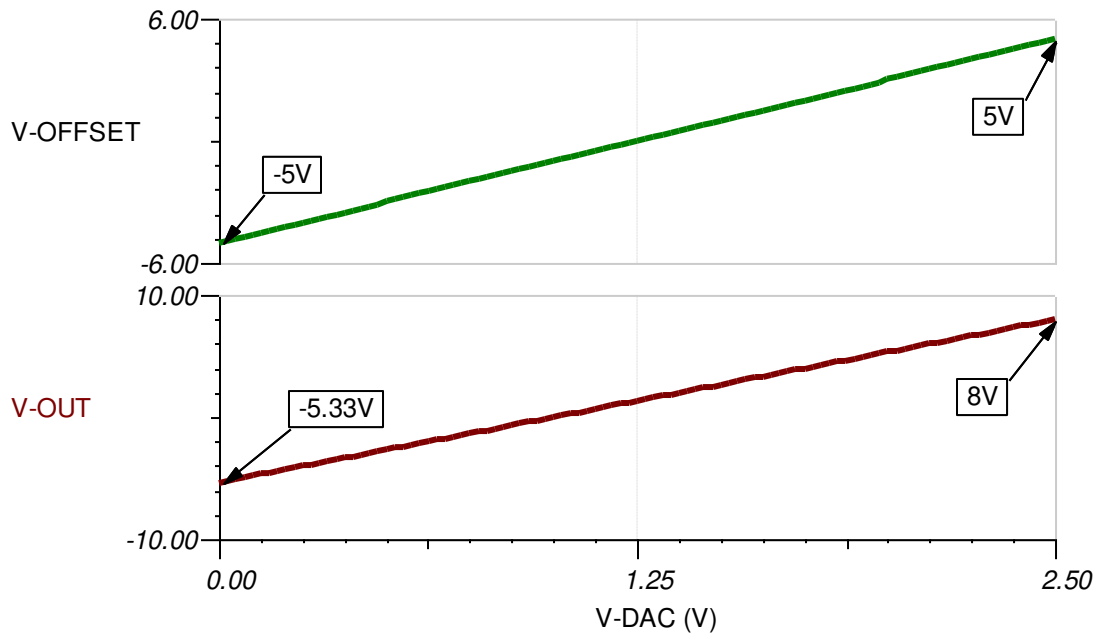
That gives,  $R_{\text{FB}} = 2 \times R_{\text{G2}}$ .

- Second, consider the positive full-scale output case when  $V_{\text{DAC}}$  is equal to 2.5 V,  $V_{\text{REF}}$  is equal to 2.5V, and  $V_{\text{OUT}}$  is equal to 5V. This case is used to calculate the ratio of  $R_{\text{FB}}$  to  $R_{\text{G1}}$  and is shown in the following equation:

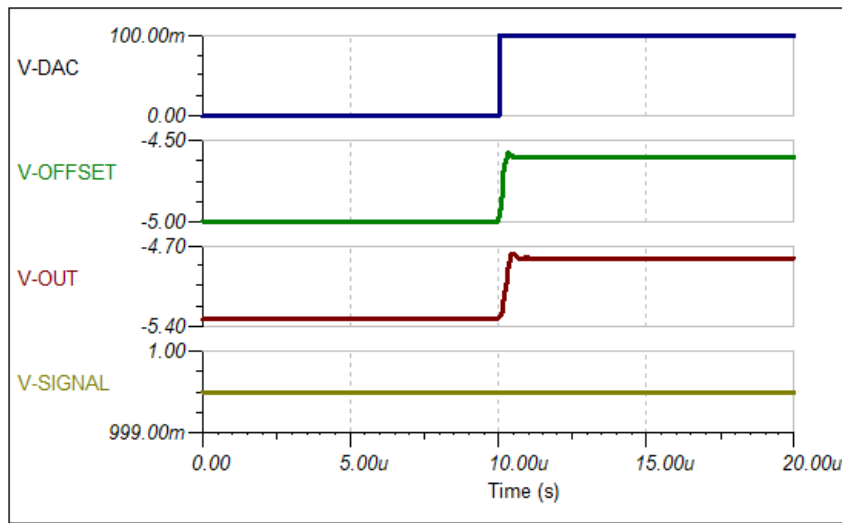
$$5\text{V} = \left( 1 + \frac{R_{\text{FB}}}{R_{\text{G2}}} + \frac{R_{\text{FB}}}{R_{\text{G1}}} \right) (2.5\text{V}) - \left( \frac{R_{\text{FB}}}{R_{\text{G2}}} \right) (2.5\text{V})$$

This means,  $R_{\text{G1}} = R_{\text{FB}}$ .

- Finally, select a value of  $R_{\text{G2}}$  to calculate the ideal values of  $R_{\text{FB}}$  and  $R_{\text{G1}}$ . The key considerations for seeding the value of  $R_{\text{G2}}$  should be the drive strength of the reference source as well as choosing small resistor values to minimize noise contributed by the resistor network. For this design,  $R_{\text{G2}}$  was chosen to be 8k $\Omega$ , which will limit the peak current draw from the reference source to approximately 312 $\mu\text{A}$ , under nominal conditions. The 312 $\mu\text{A}$  is well within the 5-mA limit of the DAC80504 device. By putting the value of  $R_{\text{G2}}$  in previous equations,  $R_{\text{G1}}$  and  $R_{\text{FB}}$  is calculated as  $R_{\text{G1}} = R_{\text{FB}} = 16\text{k}\Omega$ .
4. In general, the compensation capacitor  $C_{\text{FB}}$  is not set by fixed equations, but rather by choosing values while observing the output small-signal step response. Through simulation in this example, select  $C_{\text{FB}} \geq 22\text{pF}$ .



**Figure 1-1. DC Transfer Characteristics**



**Figure 1-2. Small-Signal Step Response Without Compensation**

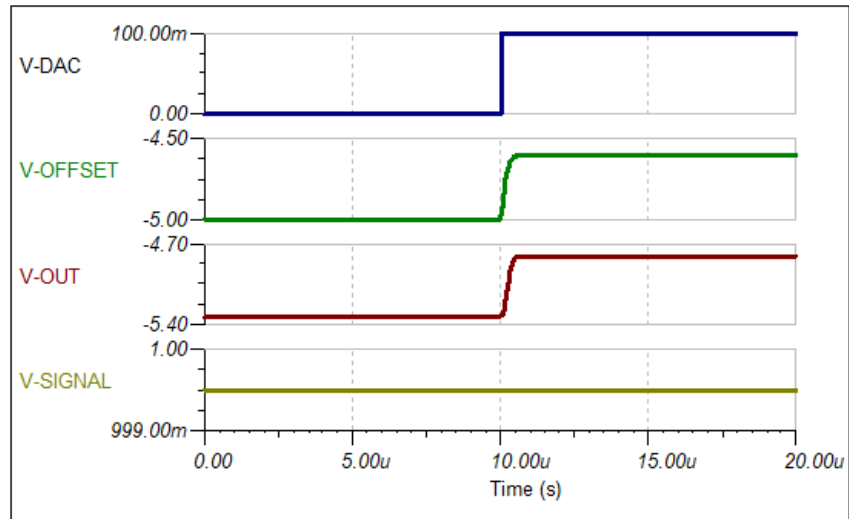


Figure 1-3. Small-Signal Step Response With  $C_{FB} = 22\text{pF}$

### Design Featured Devices and Alternative Parts

Device	Key Features	Link
DAC80504	4-channel, true 16-bit, SPI, voltage-output DAC with precision internal reference	<a href="#">True 16-bit, 4-channel, SPI, voltage-output DAC in QFN package with precision internal reference</a>
DAC80508	8-channel, true 16-bit, SPI, voltage-output DAC with precision internal reference	<a href="#">16-Bit, Ultralow Glitch, Voltage Output, Digital to Analog Converter</a>
DAC80004	Ultra-small, true 16-bit quad voltage output DAC with 1LSB INL/DNL	<a href="#">Ultra-Small, true 16-bit quad voltage output DAC with 1LSB INL/DNL</a>
DAC8560	16-bit, single-channel, low-power, ultra-low glitch, voltage output DAC with 2.5V, 2ppm/°C reference	<a href="#">16-bit, single-channel, low-power, ultra-low glitch, voltage output DAC with 2.5V, 2ppm/°C reference</a>
OPA227	High precision, low noise operational amplifiers	<a href="#">High Precision, Low Noise Operational Amplifiers</a>
OPA188	Precision, low-noise, rail-to-rail output, 36-V zero-drift operational amplifier	<a href="#">Precision, Low-Noise, Rail-to-Rail Output, 36V Zero-Drift Operational Amplifier</a>

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