DEM-DAI3168A EVM

PCM3168A Evaluation Module

User's Guide

Literature Number: SBAU150
April 2009

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About This Manual

This document provides the information needed to set up and operate the DEM-DAI3168A EVM evaluation module, a test platform for the 24-bit, 96/192-kHz, 6-in/8-out PCM3168A audio codec. For a more detailed description of the PCM3168A , refer to the product data sheet available from the Texas Instruments web site at http://www.ti.com. Support documents are listed in the section of this guide entitled ***Related Documentation from Texas Instruments***.

How to Use This Manual

Throughout this document, the abbreviation *EVM* and the term *evaluation module* are synonymous with the DEM-DAI3168A EVM. The abbreviation *DUT* refers to the PCM3168A device. Unless specifically noted, the information presented in this manual applies to the PCM3168A.

Chapter 1 describes the hardware setup guide for the EVM, including the necessary information required to configure the EVM switches and jumpers for product evaluation.

Chapter 2 explains how to use the software provided with the DEM-DAI3168A EVM for controlling the PCM3168A.

Chapter 3 includes the EVM electrical schematics, printed circuit board (PCB) layouts, and the bills of material for both the DEM-DAI3168A and the DEM-DAI/MCODEC.

Information About Cautions and Warnings

This document contains caution statements.

CAUTION

This is an example of a caution statement. A caution statement describes a situation that could potentially damage your software or equipment.

The information in a caution or a warning is provided for your protection. Please read each caution and warning carefully.

Related Documentation From Texas Instruments

The following document provides information regarding Texas Instruments integrated circuits used in the assembly of the DEM-DAI3168A EVM. These documents are available from the TI web site. The last character of the literature number corresponds to the document revision that is current at the time of the writing of this document. Newer revisions may be available from the TI web site at http://www.ti.com/ or call the Texas Instruments Literature Response Center at (800) 477–8924 or the Product Information Center at (972) 644–5580. When ordering, identify the document(s) by both title and literature number.

Data Sheet	Literature Number
PCM3168A Product data sheet	SBAS452
DIR9001 Product data sheet	SLES198
DIT4096 Product data sheet	SBOS225B
TUSB3410 Product data sheet	SLLS519G
MSP430F169 Product data sheet	SLAS368E
OPA2134 Product data sheet	SBOS058

If You Need Assistance

If you have questions regarding either the use of this evaluation module or the information contained in the accompanying documentation, please contact the Texas Instruments Product Information Center at (972) 644–5580 or visit the TI web site at www.ti.com.

FCC Warning

This equipment is intended for use in a laboratory test environment only. It generates, uses, and can radiate radio frequency energy and has not been tested for compliance with the limits of computing devices pursuant to subpart J of part 15 of FCC rules, which are designed to provide reasonable protection against radio frequency interference. Operation of this equipment in other environments may cause interference with radio communications, in which case the user at his own expense is required to take whatever measures may be required to correct this interference.

Trademarks

EVM Hardware

The DEM-DAI3168A is a complete evaluation platform which consists of the DEM-DAI/MCODEC and the DEM-PCM3168A boards for the PCM3168A, a 24-bit, 96/192-kHz, 6-in/8-out audio codec. All necessary connectors and circuitry are provided in order to interface with a range of audio test systems and commercial audio equipment.

Topic **Page**

1.1 Block Diagram

Figure 1-1 shows a block diagram of the DEM-DAI/MCODEC with the DEM-PCM3168A (DUT daughterboard).

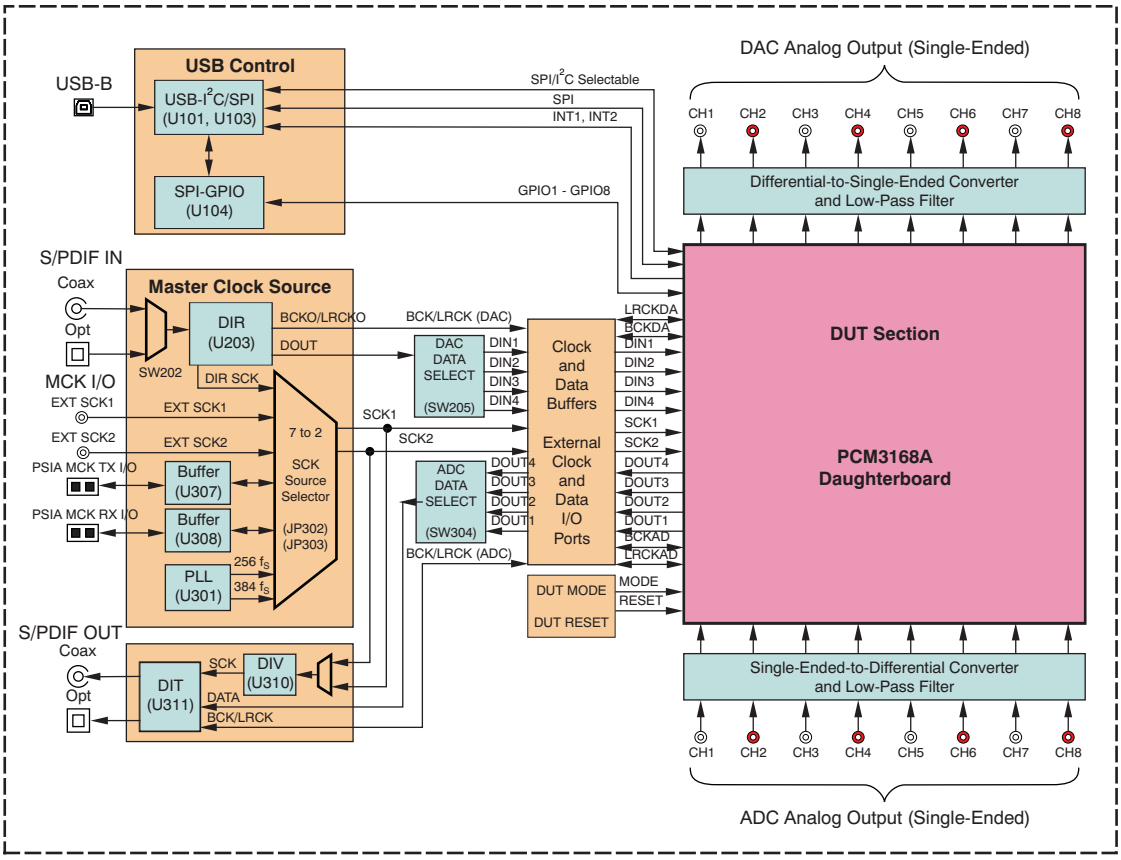


Figure 1-1. DEM-DAI/MCODEC Block Diagram

1.2 Features

The DEM-DAI3168A has the following features:

- Evaluation module for the PCM3168A 6-input, 8-output multi-channel codec
- Easy sound demonstration and evaluation through S/PDIF input/output
- Software control capability by application software; hardware control capability without application software
- Input/output with buffer and termination to easily connect with external PCB/system, signal generator, or analyzer

1.3 EVM Package Contents and Required Items

1.3.1 Electrostatic Discharge Warning

Many of the components on the DEM-DAI3168A EVM are susceptible to damage by electrostatic discharge (ESD). Customers are advised to observe proper ESD handling precautions when unpacking and handling the EVM, including the use of a grounded wrist strap at an approved ESD workstation.

CAUTION

Failure to observe ESD handling procedures may result in damage to EVM components.

1.3.2 EVM Package Contents

Upon opening the DEM-DAI3168A EVM package, ensure that the following items are included:

- Motherboard: DEM-DAI/MCODEC (1)
- PCM3168A Daughterboard: DEM-PCM3168A (1) (previously mounted on motherboard)

Note: The complete software tool suite, including the application software for the EVM, TUSB3410 driver, and related documents can be downloaded from the TI web site at http://www.ti.com/.

If either item is missing, please contact the Texas Instruments' Product Information Center nearest you to inquire about a replacement.

1.3.3 Required Items

These additional items are required for proper EVM operation and are not included with the EVM package.

- Regulated power supplies (+5 V, 1 A, and ±15 V, 1 A)
- Power-supply cable (with banana plug connector)
- Microsoft® Windows® OS PC with USB port
  - Configured with Windows 98SE, ME, 2000, or XP operating system
- USB cable (with A-B Connector)
- Measurement equipment (such as Audio Analyzer™)

1.4 Getting Started

1.4.1 Power-Supply Connection and Configuration

Three power supplies are required to operate this EVM: 15 V, –15 V, and 5 V, are required. A regulated power supply is necessary for proper operation and in order to maximize performance. Power supplies are connected at the banana jacks as illustrated in Figure 1-2.

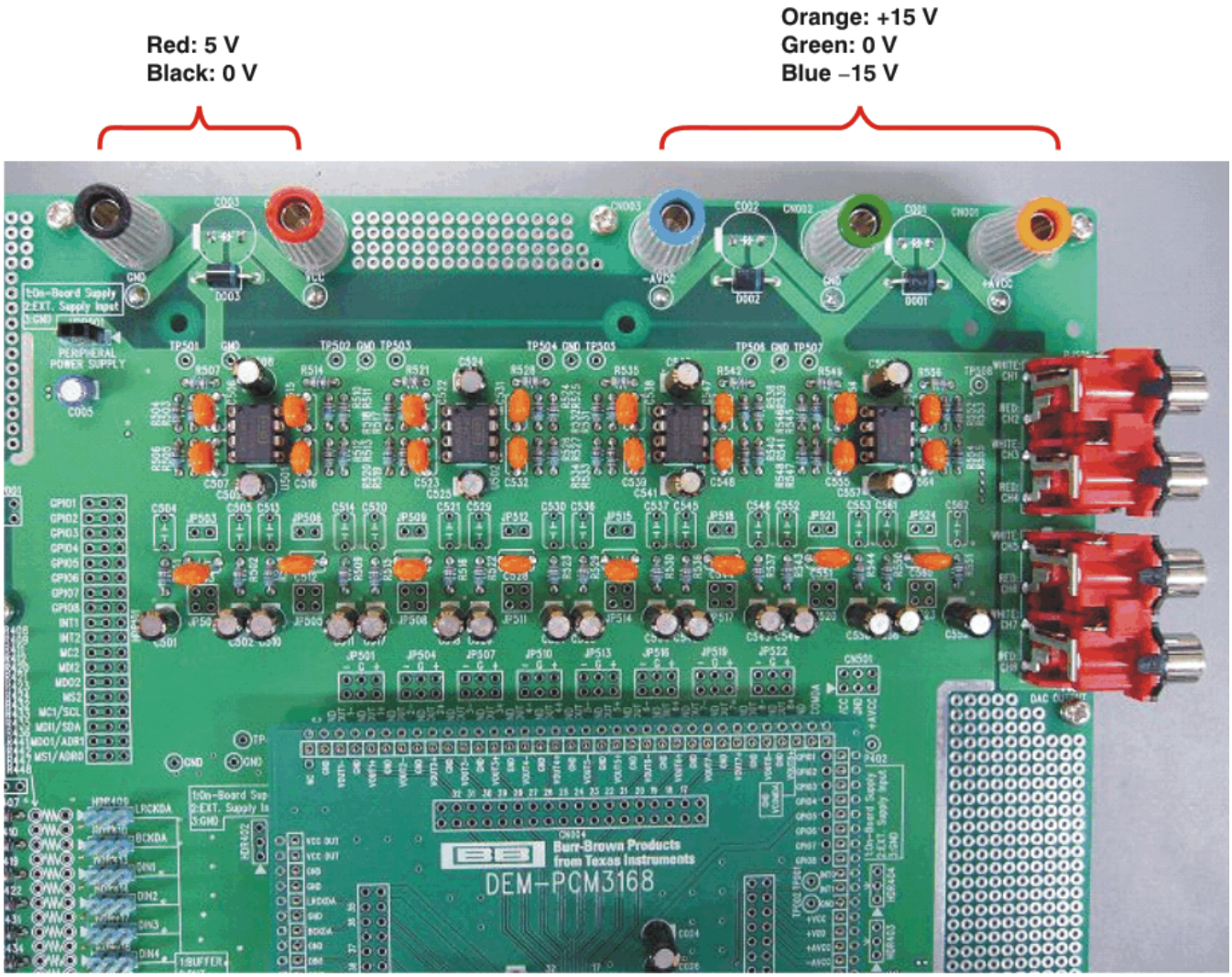


Figure 1-2. Power-Supply Connection and Configuration

1.4.2 Analog and S/PDIF I/O Configurations

Figure 1-3 illustrates an example connection of a digital signal through an S/PDIF port. If a four-wire PCM connection of SCK, BCK, LRCK, and DATA is desired, making an external connection with circled part ***E*** of Figure 1-3 is necessary instead of making external connections with parts A and B. Refer to the appropriate schematic diagram (see Section 4.1) for details of the actual connection. Audio input/output is available as a default condition by supplying power and connecting the points indicated below:

A. S/PDIF input (DAC digital input)
B. S/PDIF output (ADC Digital output)
C. DAC analog output (CH1-CH8)
D. ADC analog input (CH1-CH8)
E. Four-wire PCM Interface (SCK, BCK, LRCK, DIN/DOUT) connection (left side: with buffer; right side: without buffer)

These areas correspond to those shown in Figure 1-3.

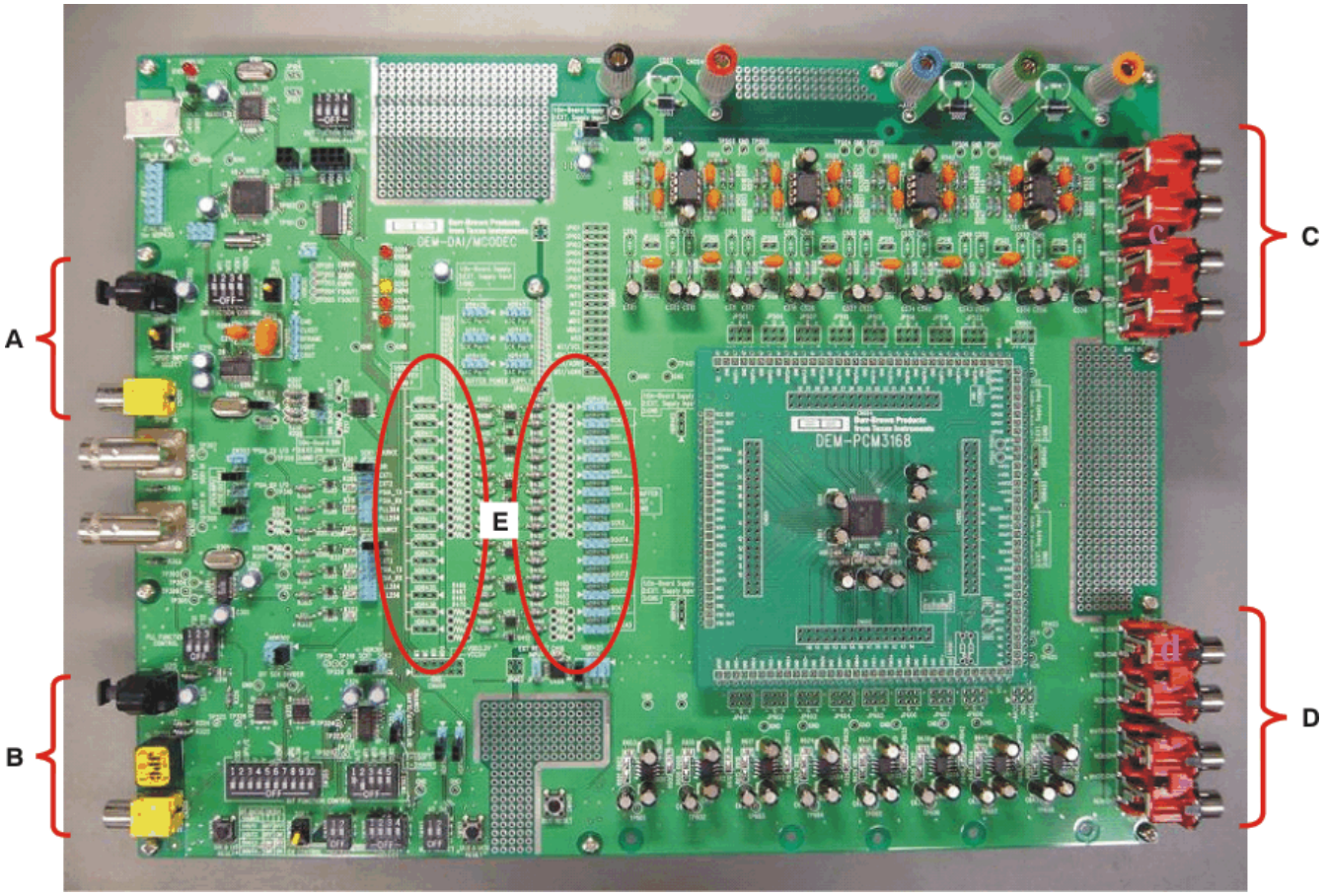


Figure 1-3. Analog and S/PDIF I/O Configurations

1.5 Hardware Description and Configuration Control

Figure 1-4 shows the hardware description and default configuration of the motherboard.

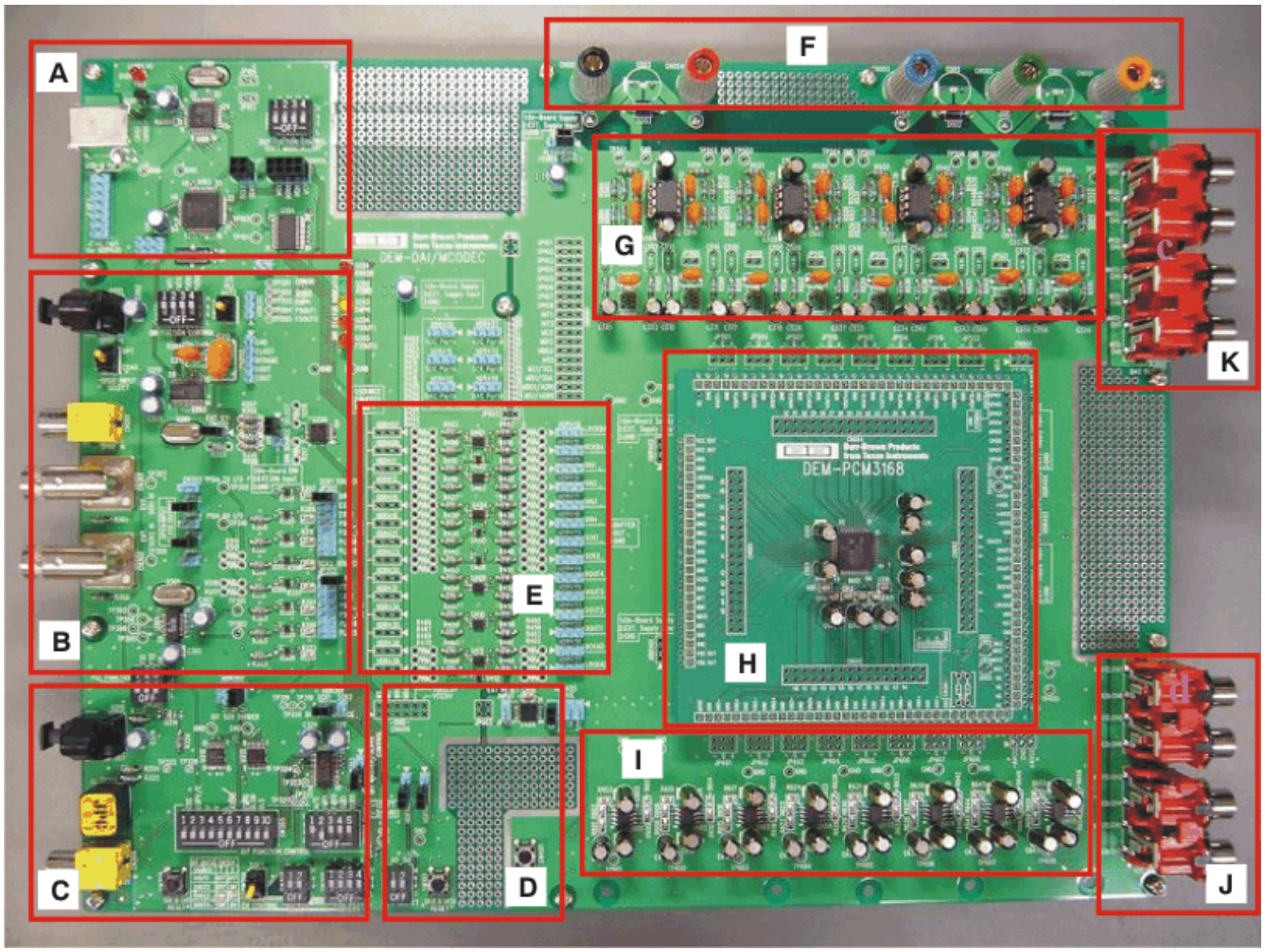


Figure 1-4. Hardware Description and Configuration

The areas indicated by letters the correspond to Figure 1-4 are:

A. USB interface and controller
B. DIR (S/PDIF IN) and master clock generator
C. DIT (S/PDIF OUT) and channel status setting
D. Data path control and DUT reset
E. Buffer and termination for external clocks and data I/Os
F. Power-supply inputs (5 V and ±15 V)
G. Differential to single-ended converter with low-pass filter (LPF) for digital-to-analog converter (DAC)
H. DUT daughterboard
I. Single-Ended to differential converter with LPF for analog-to-digital converter (ADC)
J. Analog input for ADC
K. Analog output for DAC

1.5.1 Clock and Function Control Block

Figure 1-5 shows the clock and function control blocks highlighted.

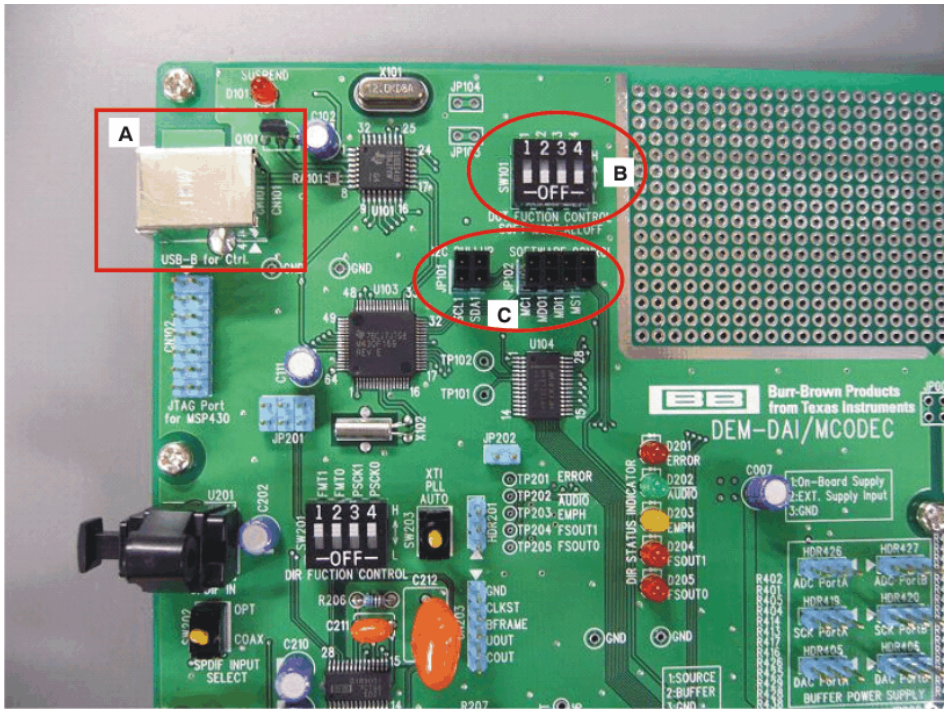


Figure 1-5. USB Control Block

A. USB Type B Connector (CN101)

When the application software is used in software control mode, a USB cable from the PC is connected to the EVM. If the PCM3168A default setting is used, a PC connection is not required even if software control mode(SPI™ or I²C™) is selected. Additionally, if hardware control mode is selected, a connection with PC is also not required.

B. Switch for DUT Configuration and Control in Hardware Control Mode (SW101)

This switch is used for the DUT configuration and control in hardware control mode. When *SPI* software control mode is selected, all switches F1 through F4 should be set to OFF. When software control mode *I²C* is selected, F1 and F4 of SW101 should be set according to the appropriate I²C address as shown in Table 1-1, and the address of the application software (refer to Section 2.2) must be same as the I²C address selected from Table 1-1.

C. Jumper for Control Circuit at Software control mode (JP101, JP102)

For hardware control mode, all jumpers should be open. In SPI software control mode, all jumpers should be closed. In I²C software control mode, the jumpers MDO1 and MS1 should be open.

Table 1-1. SW101: I²C Address Setting

F1	F4	I²C ADDRESS (ADR 1,0)
L	L	00
L	H	01
H	L	10
H	H	11

1.5.2 DIR Block

The DIR block is highlighted in Figure 1-6.

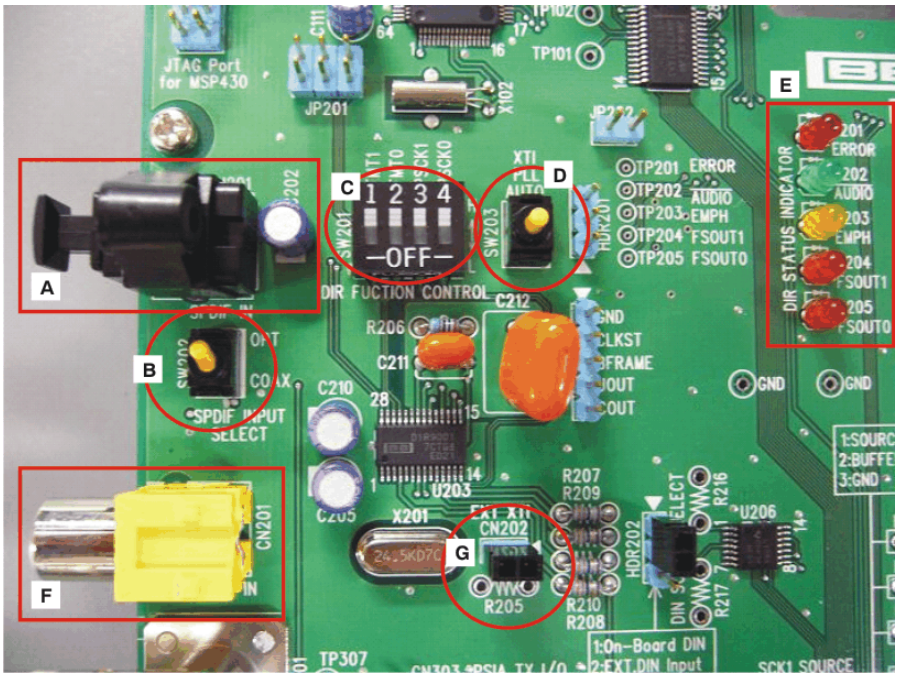


Figure 1-6. DIR Block

The DIR block features these sections (letters correspond to indicators shown in Figure 1-6).

A. S/PDIF optical input connector (U201)
   This connector is used to receive input data to the DAC in parallel with a coaxial connector.

B. Switch for S/PDIF input selection (SW202)
   This switch is used to select either an optical or a coaxial connection.

C. Switch for DIR data format and SCKO selection (SW201)
   These switches are used to select the desired data format and SCKO ratio to sampling frequency (f_S) of DIR. The default setting is I^2S™ format and 512 f_S SCKO.

D. Switch for DIR mode selection (SW203)
   This switch is used to select the clock source for the DIR clock output, SCKO. *PLL* or *AUTO* must be selected in order to distribute the recovered clock by DIR as the system clock for DUT.

E. LED indicators to show DIR condition (D201–D205)
   These LEDs indicate the DIR operating condition. If the Error LED is off, this state indicates that the DIR is locked to S/PDIF input, as summarized in Table 1-2.

Table 1-2. Error LED Truth Table

Error LED State	DIR Operating Condition
On, in red	No signal or unlocked
Off	Locked to S/PDIF

F. S/PDIF coaxial input connector (CN201)
   This connector is used to receive input data to the DAC in parallel with an optical connector.

G. Jumper of crystal oscillator setting for DIR9001 (CN202)
   This jumper is used to stop the DIR9001 crystal oscillator from closing. The DIR9001 decoding operation is possible even if the crystal oscillator is stopped. Note that it is recommended to stop the crystal oscillator when performing a sound evaluation.

1.5.3 Master Clock Source Block

Figure 1-7 illustrates the master clock source block.

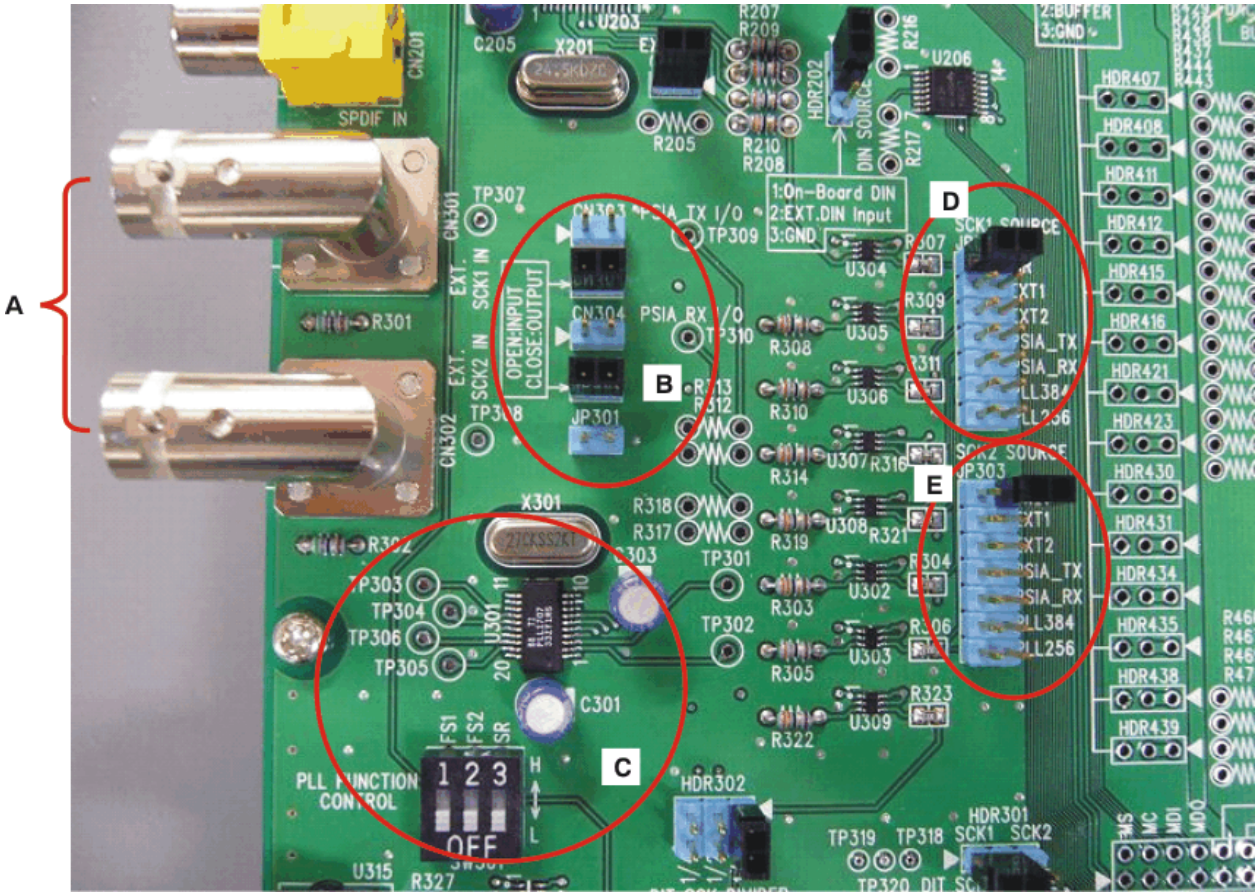


Figure 1-7. Master Clock Source Block

The master clock source block has these features (letters correspond to indicators shown in Figure 1-7):

A. External SCK input connectors (× 2) (CN301, CN302)

These are used to input external clocks as SCKs of the EVM in place of the DIR clock output or the onboard PLL clock output; 3.3 V LV-TTL with 50-Ω termination is available.

B. Master Clock I/O for PSIA-2722 (CN304, CN305, JP304, JP305)

This I/O is used to connect with Audio Precision PSIA-2722™ or other circuits. A 3.3-V LV-TTL level and Thevenin termination are available on CN303 for PSIA Tx and on CN304 for PSIA Rx, and input/output configuration can be set through JP304 for CN303 and JP305 for CN304 (open: input; close: output).

C. PLL1707 master clock generator (U301, SW301)

An audio clock of 256 f_S/384 f_S or 512 f_S/768 f_S can be generated from a 27-MHz crystal resonator. The default setting is 48 kHz 512f_S (FS1: Off, FS2: Off, SR: On).

D. SCK1 clock source selection (JP302)

These jumpers are used to select the SCK1 source distributed for the PCM3168A. Default setting is DIR selected.

E. SCK2 clock source selection (JP303)

These jumpers should be open for general evaluation of this EVM .

1.5.4 DIT Block

Figure 1-8 shows the DIT block.

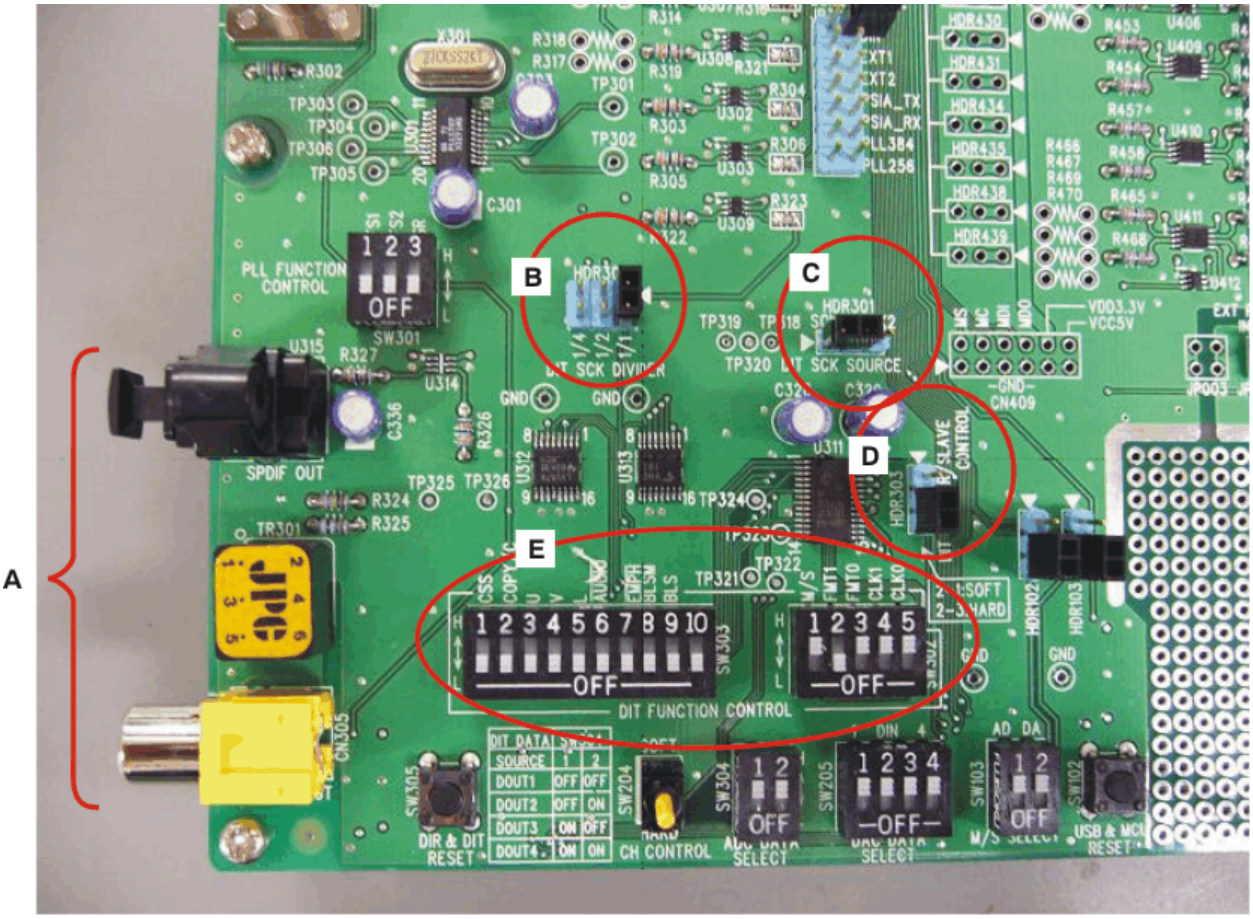


Figure 1-8. DIT Block

The DIT block has these features (letters correspond to indicators shown in Figure 1-8):

A. S/PDIF output connector (U315, CN305)

These connectors are used to output ADC conversion data. Optical and coaxial connections are available simultaneously without any additional setting.

B. SCK dividing ratio selection for DIT (HDR302)

This jumper is used to select the SCK dividing ratio for DIT. If 256 f_S, 384 f_S, or 512 f_S is selected for SCK, the dividing ratio should be 1/1. If SCK is greater than 512 f_S, a divider circuit can be used.

C. SCK source clock selection for DIT (HDR301)

This jumper is used to select the SCK source clock distributed for DIT. In general, SCK1 should be selected.

D. Mode control method selection for DIT (HDR303)

This jumper is used to select the DIT mode (master or slave) control method, SW302, or application software. If SOFT is selected, its setting is configured by the application software; if HARD is selected, the configuration is set with SW302.

E. Function setting for DIT (SW302, SW303)

SW302 is used to select the SCK frequency, data format, and set the master/slave mode selection. The default setting for SW302 is master, SCK = 512 f_S, and I^2S format.

SW303 is used to set the channel status data. This switch can be left as is for a general evaluation of the PCM3168A. To use this switch, refer to the DIT4096 product data for details.

1.5.5 Buffer and Termination Block

The Buffer Control block is illustrated in Figure 1-9.

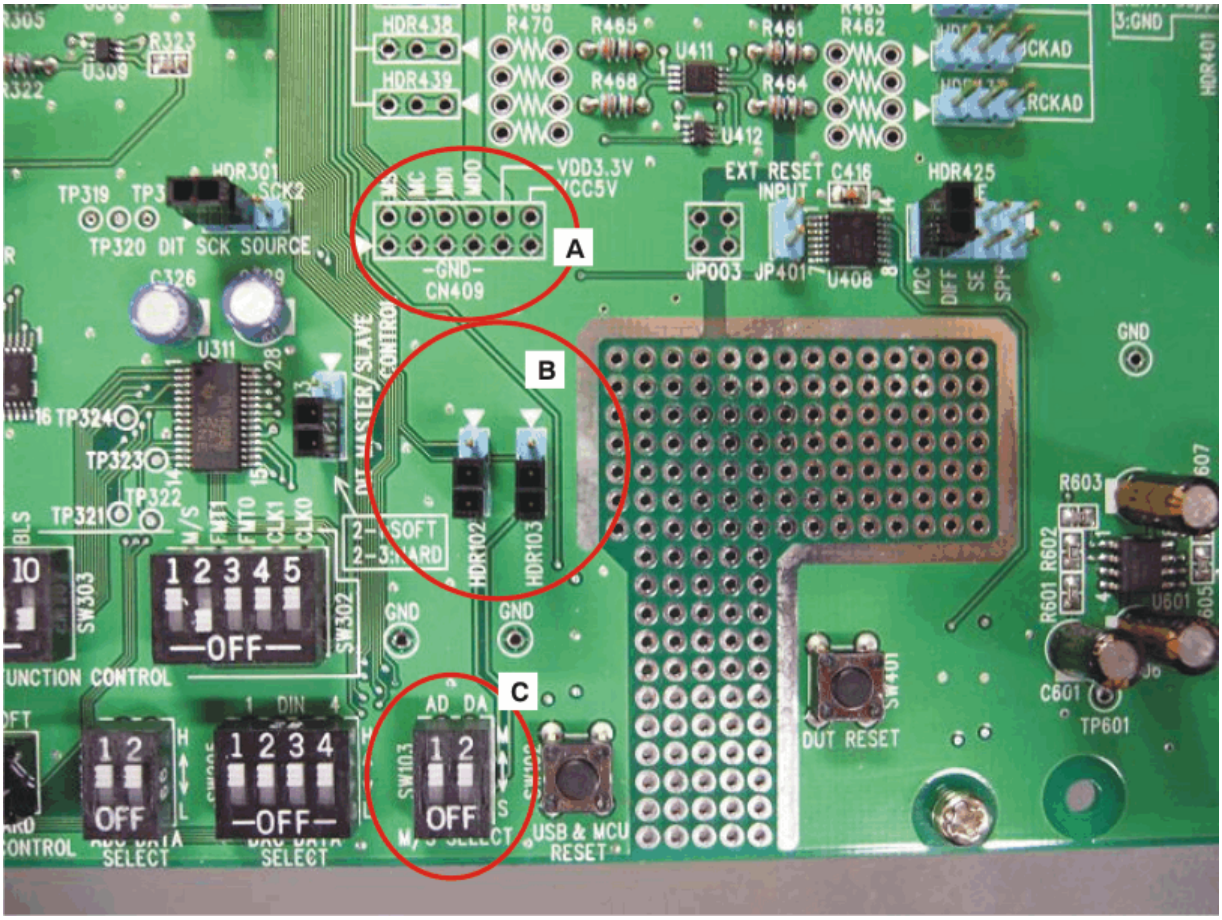


Figure 1-9. Buffer Control Block

The areas indicated by letters that correspond to Figure 1-9 are:

A. Extended connector for mode control (CN409)

   This connector is not mounted and should be unconnected for standard/general evaluation.

B. Control method selection for setting the signal direction of the LRCK/BCK buffer (HDR102, HDR103)

   These headers are used to select the signal direction control method of the LRCK/BCK buffers. When SOFT is selected, the signal direction is set according to the master/slave mode selection for the ADC/DAC of the PCM3168A. When HARD is selected, the signal direction is set by SW103, as explained in C.

C. Buffer direction setting switch (SW103)

   This switch sets the direction of the LRCK/BCK buffer with independent control of the ADC/DAC. If HARD is selected by HDR102/HDR103 (as discussed in B), this switch is available. This switch should be set opposite of the PCM3168A master/slave mode setting, because the *M/S* indication on the EVM means the direction of the DIR/DIT side. The *DA* switch is for setting the direction of LRCKDA/BCKDA; the *AD* switch sets the direction of LRCKAD/BCKAD.

1.5.6 DUT Reset and Mode Control Block

The DUT Reset and Mode Control block are presented in Figure 1-10.

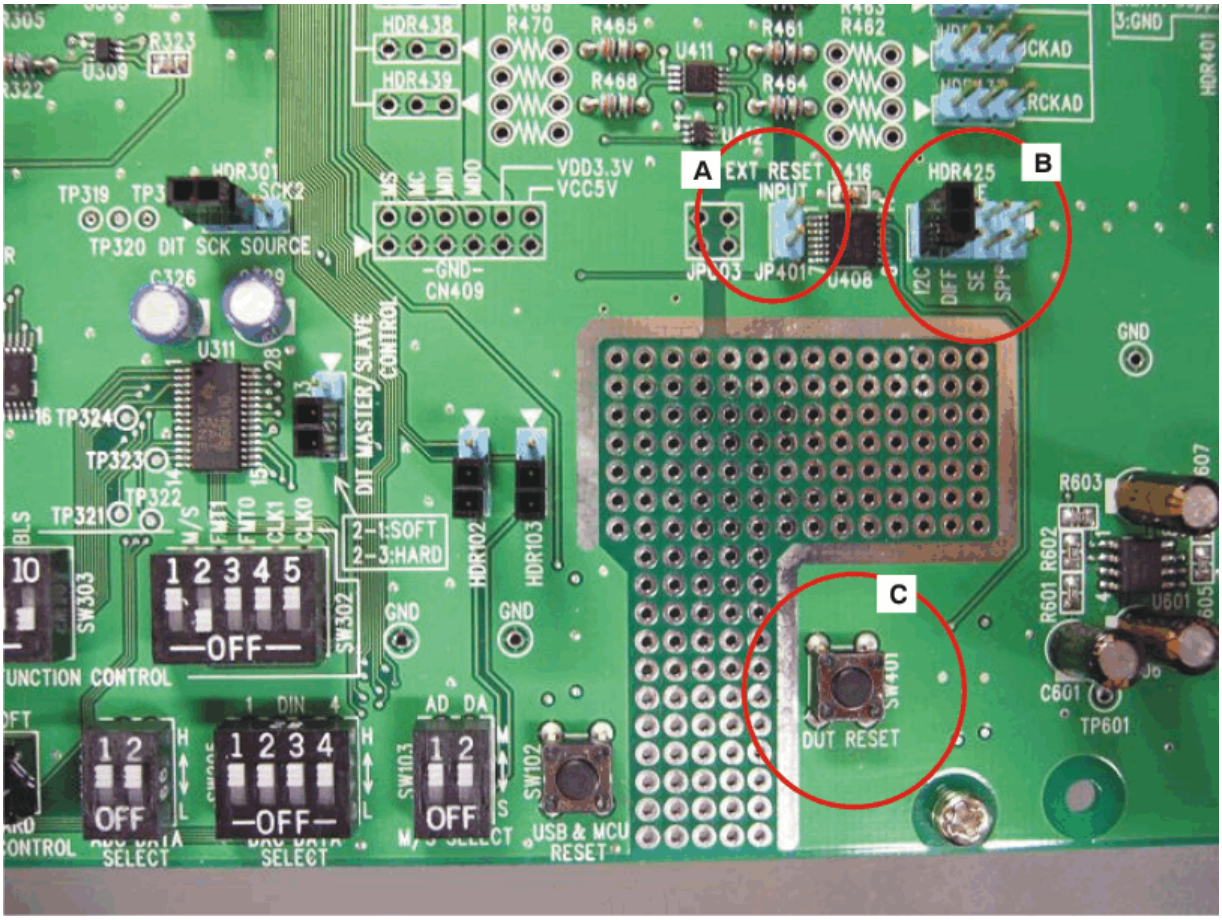


Figure 1-10. DUT Reset and Mode Control Block

The areas indicated by letters that correspond to Figure 1-10 are:

A. EXT Reset input (JP401)

This input connects with an external reset signal source. This reset is performed in parallel with a reset by the application software and a reset by the DUT reset switch (explained in C) with an OR function.

B. PCM3168A MODE pin setting (HDR425)

This jumper sets the PCM3168A MODE pin. The default setting is SPI software control mode. *DIFF* and *SE* represent differential and single-ended (respectively) hardware control mode; I^2C is for another software control mode. In hardware control mode, JP101/102 should all be open; configuration control is done through SW101. Because the PCM3168A accepts a mode change at reset, the DUT reset must be performed after a mode change.

C. DUT Reset switch (SW401)

This switch forces only the PCM3168A device to be reset. This reset is done in parallel with a reset by the application software and an external reset (explained in A) with an OR function. A power-on reset function is also available. When the PCM3168A mode is changed by HDR425, a DUT reset must also be performed.

1.5.7 Peripheral Circuit Reset Block

Figure 1-11 shows the Peripheral Circuit Reset block.

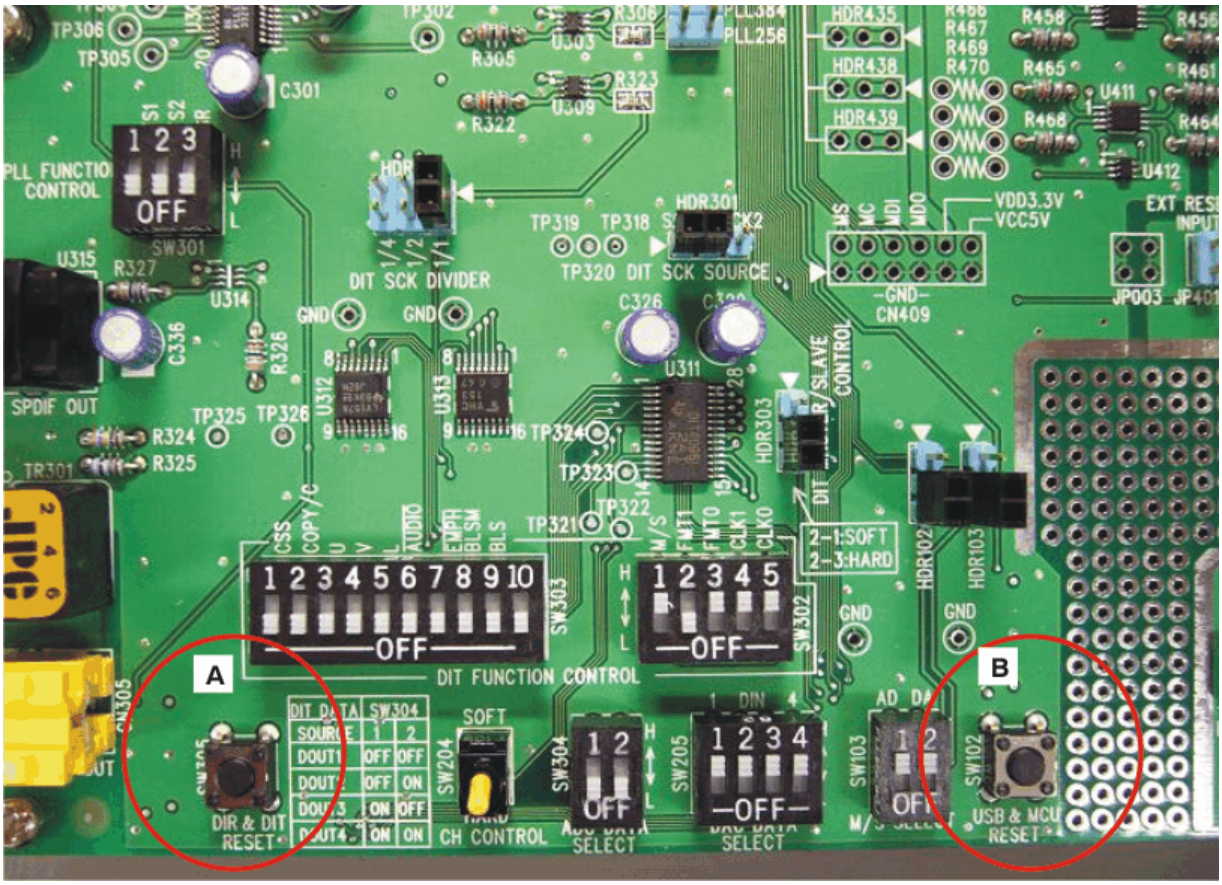


Figure 1-11. Peripheral Circuit Reset Block

The areas indicated by letters that correspond to Figure 1-11 are:

A. Reset switch for *DIR* and *DIT* (SW305)

   This switch is used to reset the DIR and DIT circuits. Because a power-on reset feature is available, using this switch is generally not needed.

B. Reset switch for *USB* and *MCU* (SW102)

   This switch is used to reset the USB and MCU circuits. Because a power-on reset feature is available, using this switch is generally not necessary. If this switch is used after a connection between the application software and the EVM is made, the connection is no longer available, and pushing the ***Reconnect*** button in the application software is required.

1.5.8 Audio Data Path Control Block

The PCM3168A has a 6-channel ADC and an 8-channel DAC. However, the S/PDIF receiver and transmitter allow processing only one pair of stereo input and output signals, respectively. On the DEM-DAI3168A evaluation board, S/PDIF input data can be shared among four pairs (maximum) of stereo digital input signals to the 8-channel DAC. Additionally, S/PDIF output data can be selected from one of the three pairs of stereo digital output signals from the 6-channel ADC.

These S/PDIF signal path controls can be set either by switches or the application software. Selection of switches or the application software is done through SW204.

- SW204 = HARD: S/PDIF signal path is controlled by SW205/304.
- SW204 = SOFT: S/PDIF signal path is controlled by the application software.

Control details at HARD mode is described in Figure 1-12. Control details for SOFT mode are discussed with regard to Figure 1-13.

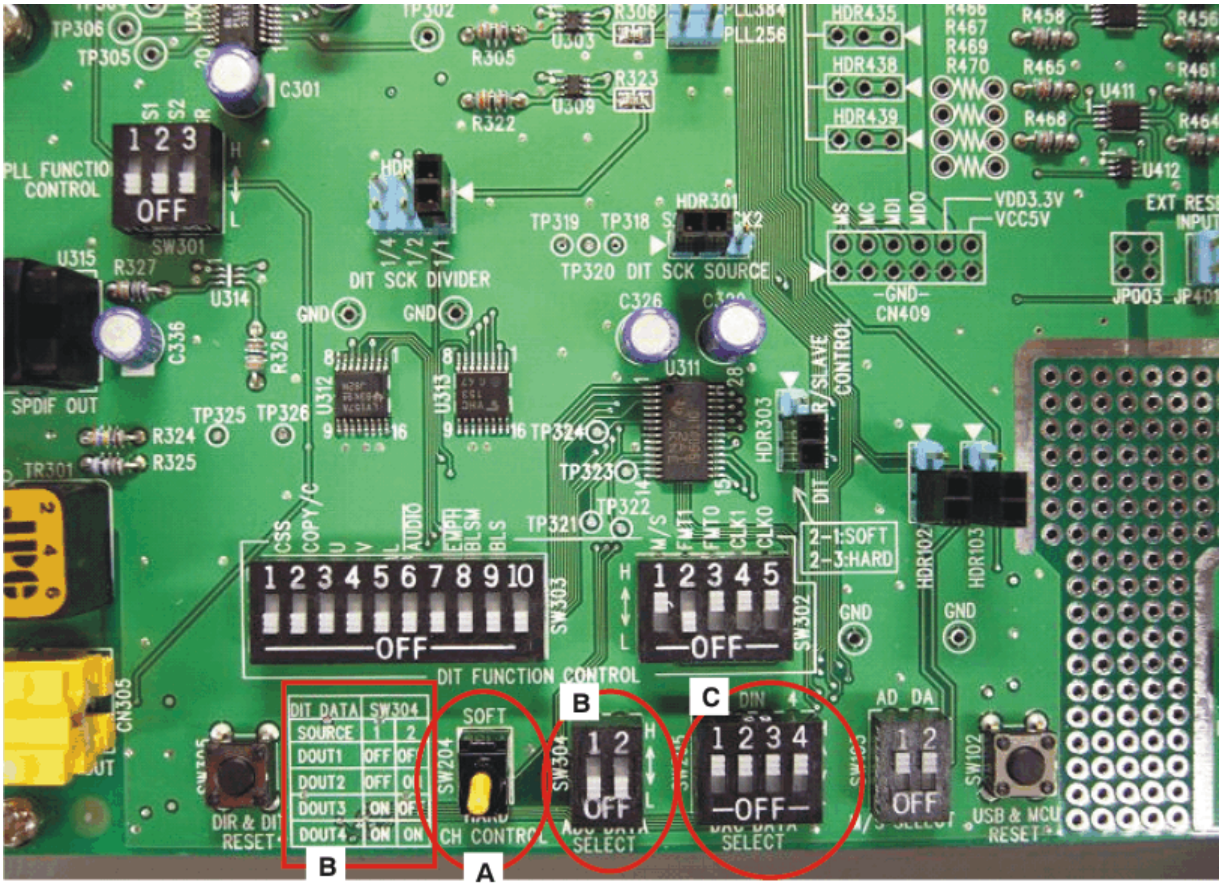


Figure 1-12. Audio Data Control Block

The areas indicated by letters that correspond to Figure 1-12 are:

A. Data path control method selection (SW204)

This switch selects the data path control method, either through SW205/304 or the application software. The default setting is *HARD*.

Hardware Control

The data path control by SW205/304 is available if HARD mode is selected by SW204.

B. Input data selection for DIT (SW304)

This switch selects which ADC conversion data of DOUT1 to DOUT4 is input to DIT. The table in left circle of Figure 1-13 shows the relationship between the setting of SW304 and the data path.

C. Input data control for DAC/DUT (SW205)

This switch controls the input data for DAC/DUT. SW1-4 corresponds with DIN1-4, respectively.

- ON: DIR data to DINx
- OFF: Low level to DINx.

Figure 1-13 shows the window for audio signal routing via software control.

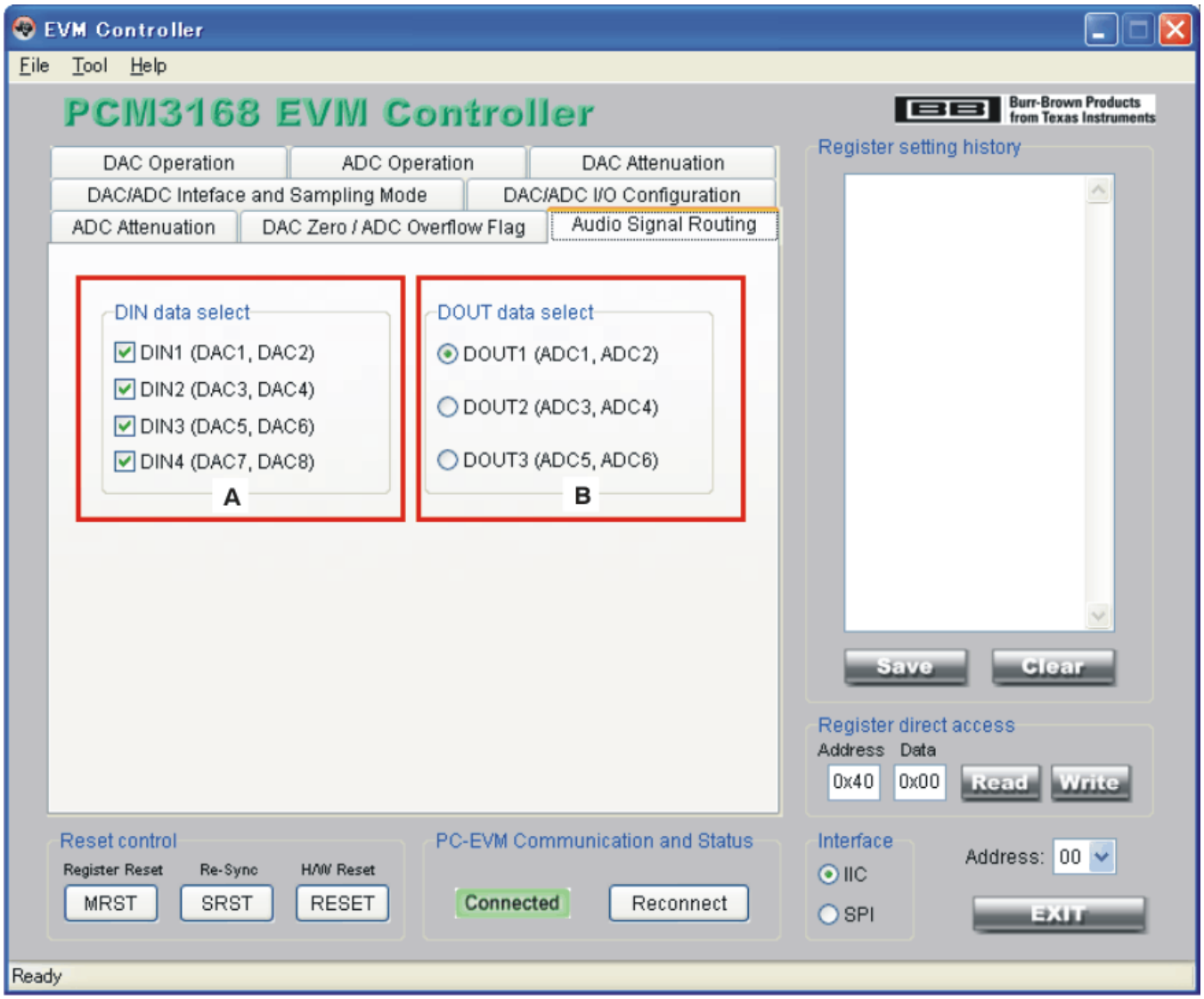


Figure 1-13. Audio Signal Routing by Software Control

Software Control

Data path control by application software is available if SOFT mode is selected by SW204.

A. Selection of DIN data (that is, DAC input)

This checkbox selects which PCM3168A DIN data are connected with the DIR output. The default setting is for all of DIN1-4 to accept DIR output.

B. Selection of DOUT data (that is, ADC output)

This checkbox selects which PCM3168A DOUT data are connected with the DIT input. The default setting is DOUT1.

1.6 Switch Settings

Note: Throughout this document, shaded cells in tables indicate default settings.

1.6.1 SW101 for PCM3168A Mode Control in Hardware Control Mode

Table 1-3, Table 1-4, and Table 1-5 summarize the settings for SW101 in a variety of modes.

Table 1-3. SW101 (1, 4): PCM3168A I/F Mode and Sampling

MD1 (F1)	MD0 (F4)	I/F Mode		Sampling Mode	
		ADC	DAC	ADC	DAC
OFF	OFF	Slave	Slave	Auto	Auto
OFF	ON	Master, 512 fS	Slave	Single Rate	Auto
ON	OFF	Master, 384 fS	Slave	Dual Rate	Auto
ON	ON	Master, 256 fS	Slave	Dual Rate	Auto

Table 1-4. SW101 (3): PCM3168A FMT

FMT (F3)	Description
OFF	I^2S
ON	I^2S TDM

Table 1-5. SW101 (2): PCM3168A De-Emphasis

DEMP (F2)	Description
OFF	De-emphasis Disable
ON	44.1-kHz De-emphasis Enable

Note: When software control mode (SPI) is selected, SW101 should be set to *OFF*. When software control mode (I^2C) is selected, the I^2C slave address can be changed through F1 and F4 of SW101. These values must be consistent with the I^2C address in the application software.

1.6.2 SW201, SW202, and SW203 for DIR9001 Operation Control

Table 1-6 through Table 1-9 summarize the options for SW201, SW202, and SW203 with regard to DIR9001 operation control.

Table 1-6. SW201: DIR9001 SCK Control

PSCK1	PSCK0	Description
OFF	OFF	128 f_S
OFF	ON	256 f_S
ON	OFF	384 f_S
ON	ON	512 f_S

Table 1-7. SW201: DIR9001 Format Control

FMT1	FMT0	Description
OFF	OFF	16-bit, Right-justified
OFF	ON	24-bit, Right-justified
ON	OFF	24-bit, Left-justified
ON	ON	24-bit, I^2S

Table 1-8. SW203: DIR9001 CKSEL Control

Position	Description
XTI	XTI source, DATA = L (Not recovered clock)
PLL	PLL source (Recovered clock from incoming bi-phase)
AUTO	Depends on PLL state (Lock: PLL, Unlock: XTI)

Table 1-9. SW202: S/PDIF Input Selection for DIR9001

Position	Description
COAX	Coaxial input; CN201 is selected as S/PDIF input
OPT	Optical input; U201 is selected as S/PDIF input

1.6.3 SW301 and SW302 for PLL1707 and DIT4096 Control

Table 1-10 through Table 1-14 summarize the settings for SW301 and SW302 with regard to PLL1707 and DIT4096 operating controls.

Table 1-10. SW301 (3): PLL1707 Sampling Rate

SR	Description
OFF	Standard (256 f_S/384 f_S)
ON	Double (512 f_S/768 f_S)

Table 1-11. SW301 (1, 2): PLL1707 Frequency Control

FS1	FS2	Description f_S (SCKI 256 f_S/SCKI 384 f_S)
OFF	OFF	48 kHz (12.288 MHz/18.432 MHz)
OFF	ON	32 kHz (8.192 MHz/12.288 MHz)
ON	OFF	44.1 kHz (11.2896 MHz/16.9344 MHz)
ON	ON	Reserved

Table 1-12. SW302 (2, 3): DIT4096 Format

FMT1	FMT0	Description
OFF	OFF	24-bit, Left-justified
OFF	ON	24-bit, I^2S
ON	OFF	24-bit, Right-justified
ON	ON	16-bit, Right-justified

Table 1-13. SW302 (4, 5): DIT4096 SCK

CLK1	CLK0	Description
OFF	OFF	Unused
OFF	ON	256 f_S
ON	OFF	384 f_S
ON	ON	512 f_S

Table 1-14. SW302(1):DIT4096 Master/Slave

M/S	Description
OFF	Slave
ON	Master

Note: SW303 is used to set the CS/V/U bits of the DIT4096. For complete details, refer to the DIT4096 product data sheet.

1.6.4 SW204, SW205, and SW304 for Data Path Control

Table 1-15 through Table 1-17 describe the options for SW204, SW205, and SW304 with regard to data path control.

Table 1-15. SW204: Data Path Control Method Selection

CONTROL	Description
SOFT	Data path control is set by application software
HARD	Data path control is set by SW205 for DAC and SW304 for ADC

Table 1-16. SW205: DAC Data Path Control

DIN1	DIN2	DIN3	DIN4	Description
ON	X	X	X	DIN1: DIR DOUT
OFF				DIN1:Low Fixed
X	ON	X	X	DIN2: DIR DOUT
	OFF			DIN2: Low Fixed
X	X	ON	X	DIN3: DIR DOUT
		OFF		DIN3: Low Fixed
X	X	X	ON	DIN4: DIR DOUT
			OFF	DIN4: Low Fixed

Table 1-17. SW304: ADC Data Path Control

1	2	Description
OFF	OFF	DOUT1: DIT SDATA
OFF	ON	DOUT2: DIT SDATA
ON	OFF	DOUT3: DIT SDATA
ON	ON	DOUT4: DIT SDATA

1.6.5 SW102, SW305, SW401 for RESET/SW103, HDR425 for DUT

Table 1-18 shows the options for SW102, SW305, and SW401 with regard to Reset control. Table 1-19 and Table 1-20 describe SW103 with regard to the master or slave data path direction and HDR425 with regard to PCM3168A MODE pin configuration, respectively.

Table 1-18. SW102, SW305, and SW401: RESET Control

SW102	SW305	SW401	Description
ON/OFF	X	X	USB and MCU reset control
X	ON/OFF	X	DIR and DIT reset control
X	X	ON/OFF	DUT (PCM3168A) reset control

Table 1-19. SW103: Master/Slave Data Path Direction Control

AD	DA	Description
OFF (S)	X	DUT (PCM3168A): Master, EVM (DIT): Slave for ADC data
ON (M)	X	DUT (PCM3168A): Slave, EVM (DIT): Master for ADC data
X	OFF (S)	DUT (PCM3168A): Master, EVM (DIT): Slave for DAC data
X	ON (M)	DUT (PCM3168A): Slave, EVM (DIT): Master for DAC data

Table 1-20. HDR425: PCM3168A MODE Pin Setting

I^2C	DIFF	SE	SPI	Description
OPEN	OPEN	OPEN	SHORT	Software control mode through SPI
OPEN	OPEN	SHORT	OPEN	Hardware control mode with differential input ADC
OPEN	SHORT	OPEN	OPEN	Hardware control mode with single-ended input ADC
SHORT	OPEN	OPEN	OPEN	Software control mode through I^2C

EVM Software

This chapter describes the function and usage of the application software for the DEM-DAI3168A EVM and PCM3168A.

Topic **Page**

2.1 Application Software Overview

2.1.1 Background Information

- What is the application software available for this device?
  - This software is used to write and read PCM3168A register settings from a Windows-based PC.
- Which versions of Windows OS are supported?
  - This software operates on Windows 98SE, ME, 2000, or XP.
- What type of evaluations are this application software required for?
  - This software is required when evaluation of the PCM3168A is done with either register control through SPI or over an I^2C serial control interface. This software is not required for evaluation with the device in its default condition even if SPI or I^2C control mode would be used in the end application. In the case of hardware control mode selection, this software is not required.
- How is the evaluation board (EVM) connected to the PC?
  - Connection is made via a USB interface (USB version 1.1 or 2.0).
- What is the software installation sequence?
  - First, install the virtual COM port driver software for the TUSB3410. Then, the DEM-DAI3168A application software should be installed.

2.1.2 Setup Before Using Application Software

Follow these required steps before using the application software.

Step 1. **Software Installation**

Download these software tools from the PCM3168A product folder on the TI web site.

- Virtual COM port driver software (that is, the USB driver software) for the TUSB3410
- Application software for the DEM-DAI3168A

Step 2. **Installation Procedure for Virtual COM Port Driver Software**

Refer to the documentation in the downloaded file (*Virtual COM Port Driver Installation Instructions.pdf*; also available at http://focus.ti.com/docs/toolsw/folders/print/tusbwinvcp.html)

Step 3. **Installation Procedure for Application Software**

There is no installer software required. Copy the downloaded application software folder to the desired local folder. To uninstall the software, delete the local folder.

2.1.3 Software Launching Procedure

Note: This procedure is very important in order for the DEM-DAI3168A to be properly detected by the PC.

Step 1. Set HDR425 on the DEM-DAI3168A to SPI mode. (If you prefer to use I^2C mode, set HDR425 to I^2C mode.)

Step 2. Turn on the power supply for the DEM-DAI3168A.

Step 3. Connect the USB connector on DEM-DAI3168A to the PC.

Step 4. Launch the application software (that is, *EVM3168.exe*). The default control mode for the application software is SPI; if you prefer to use I^2C mode, change the control mode setting to I^2C, and then push the ***Reconnect*** button in the application software. After that, the preferred setting (SPI or I^2C mode) is stored on the PC for both the DEM-DAI3168A and the software.

Error Message at Software Launching

If the DEM-DAI3168A is not correctly detected by the application software, the error message shown in Figure 2-1 will appear on the PC. After pushing ***OK***, the application software will launch with an indication of *No EVM* in red, and controlling the DEM-DAI3168A is impossible. In this case, check the USB connection between the DEM-DAI3168A and PC, and the power-supply connection and voltage; unplug and reconnect these cables as needed, then try launching the software again by pushing the ***Reconnect*** button.

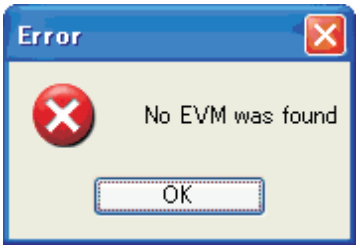


Figure 2-1. Error Message at Software Launch

2.1.4 Serial Control Selection of I²C/SPI

Serial Control (SPI/I²C)

The PCM3168A supports both I²C and SPI serial control interfaces. The DEM-DAI3168A application software also supports both interfaces under the following guidelines. (Note that the default setting is SPI for both the EVM and application software.)

Interface Setting on DEM-DAI3168A

After setting the desired interface mode by HDR425, reset the PCM3168A by pressing SW401 or powering on the EVM.

Interface Setting on Application Software

The interface mode setting is available as part of the application software GUI. After setting the desired mode using the GUI, push the ***Reconnect*** button.

Error Message at Different Setting Between Software and EVM

When SPI mode is set in the software and I²C mode is set on the EVM, no error message will be shown on the PC. However, when I²C mode is set in the software and SPI mode is set on the EVM, an error message window will be displayed.

2.2 Application Software Configuration and Troubleshooting

2.2.1 USB Connection Recognized

The window shown in Figure 2-2 appears when the PC recognizes the USB connection between the application software and the EVM. As Figure 2-2 illustrates, the indicator displays ***Connected*** in green. You can begin to use the application software.

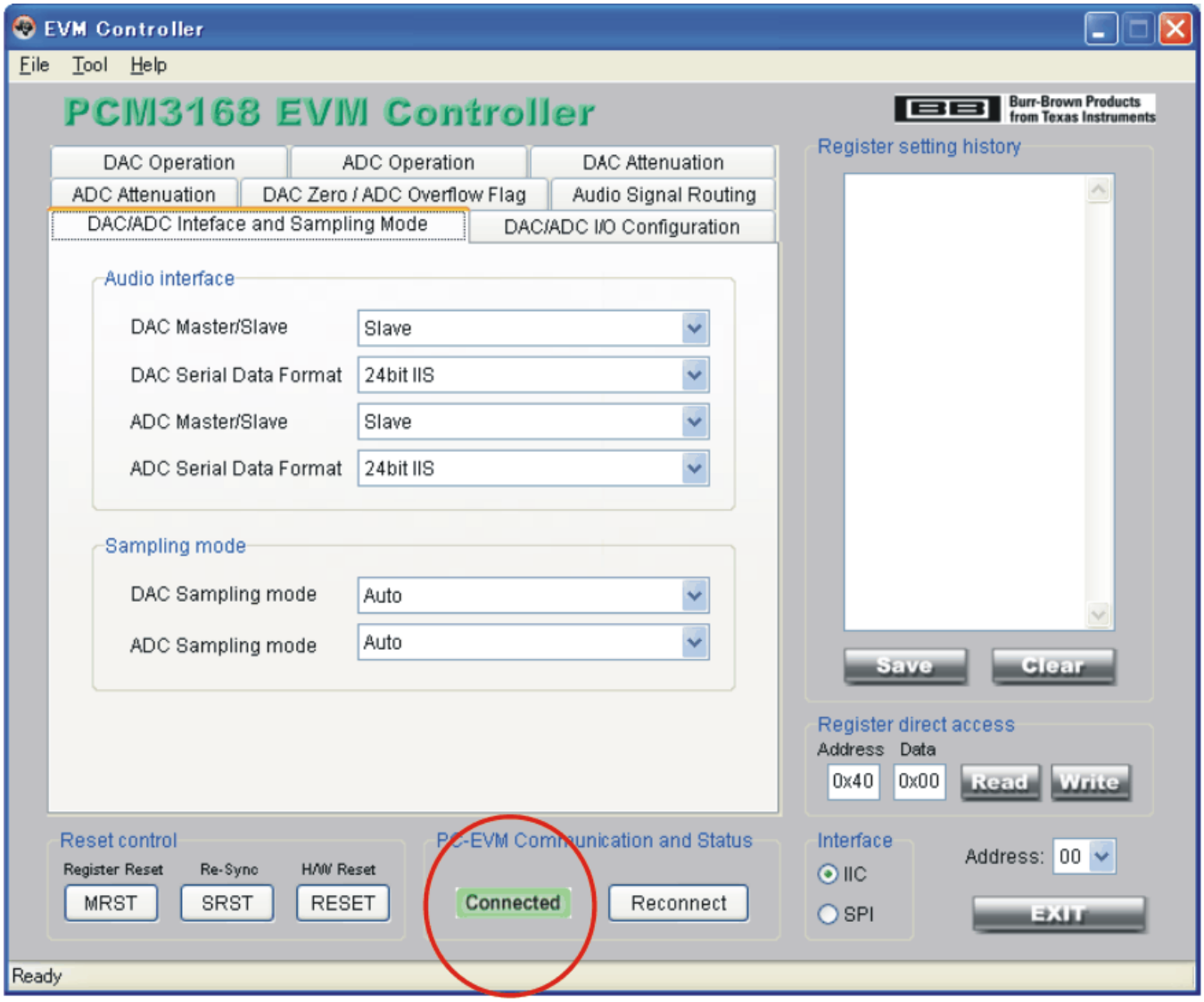


Figure 2-2. USB Connection Recognized

2.2.2 USB Connection Not Recognized

If the PC does not recognize the USB connection, the software displays the screen shown in Figure 2-3. If the indicator shows ***No EVM*** in red, push the ***Reconnect*** button. If the problem continues, check the following items.

- Are the power supplies correctly distributed for the EVM?
- Is the EVM properly connected to the PC?
- Is the USB port on the PC active?
- Is the USB (Virtual COM Port) driver software correctly installed on the PC?
- Is SPI/I^2C mode coincident between the application software and the EVM setting for the PCM3168A?
- If I^2C mode is selected, is the I^2C slave address the same for the application software and the EVM setting on the PCM3168A?

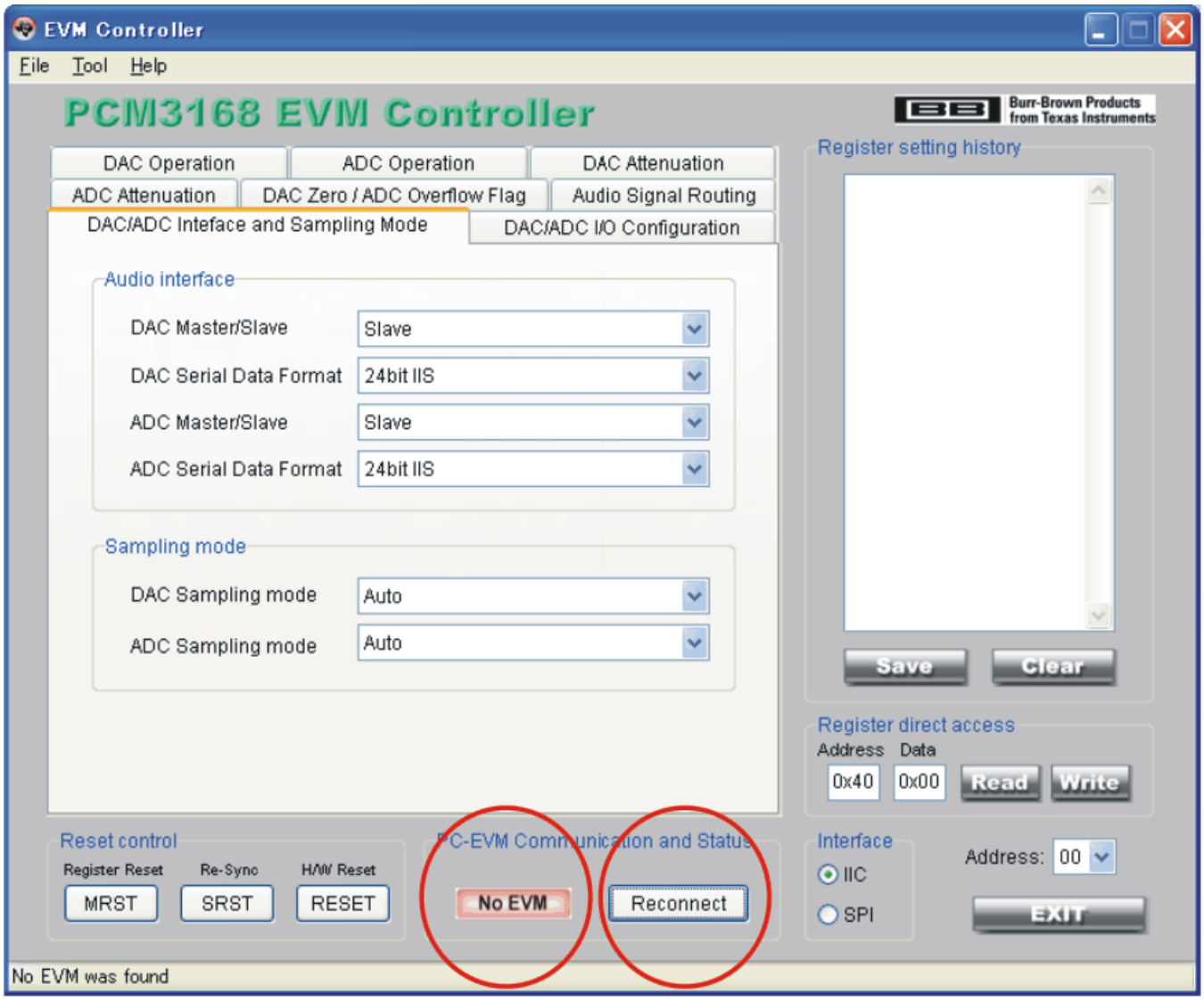


Figure 2-3. USB Connection Not Recognized

2.3 Application Software Operation

This section overview the various controls available in the application software.

Figure 2-4 shows the RESET and Reconnect buttons highlighted.

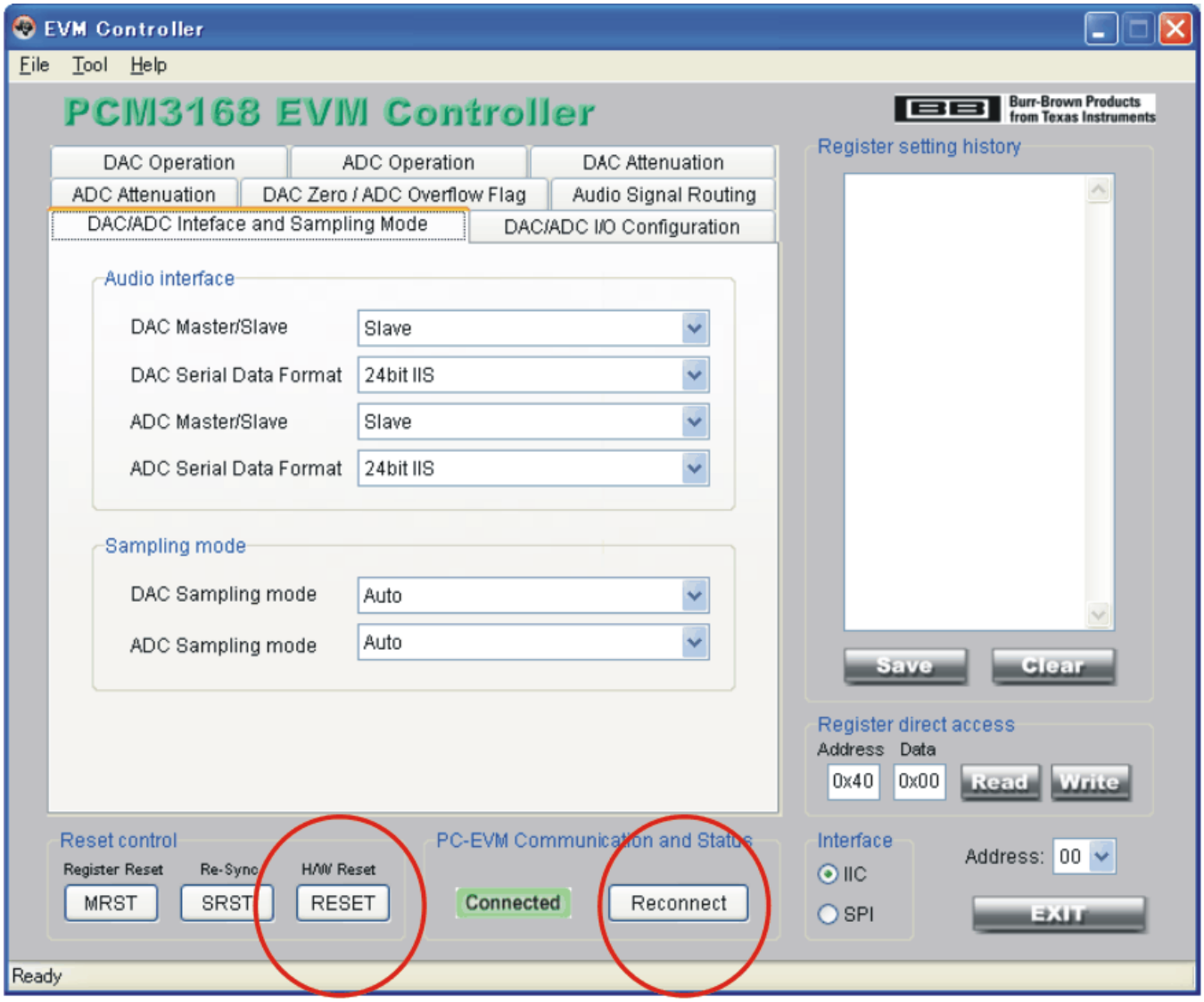


Figure 2-4. RESET and Reconnect Buttons

RESET

This button resets the PCM3168A through its RESET pin (pin 4, RST). This function is available in parallel with reset by pressing the DUT RESET switch (SW401) and the external reset (JP401) with OR function. This function is equivalent to SW401, the DUT RESET switch on the EVM.

Reconnect

This button sends a reconnection request between the PC and the EVM. When the control interface mode (I^2C or SPI) or the I^2C slave address changes, pushing this button is required. For recovery after releasing the USB cable or turning off the EVM power supply, pushing this button is also required.

Figure 2-5 highlights the control interface options.

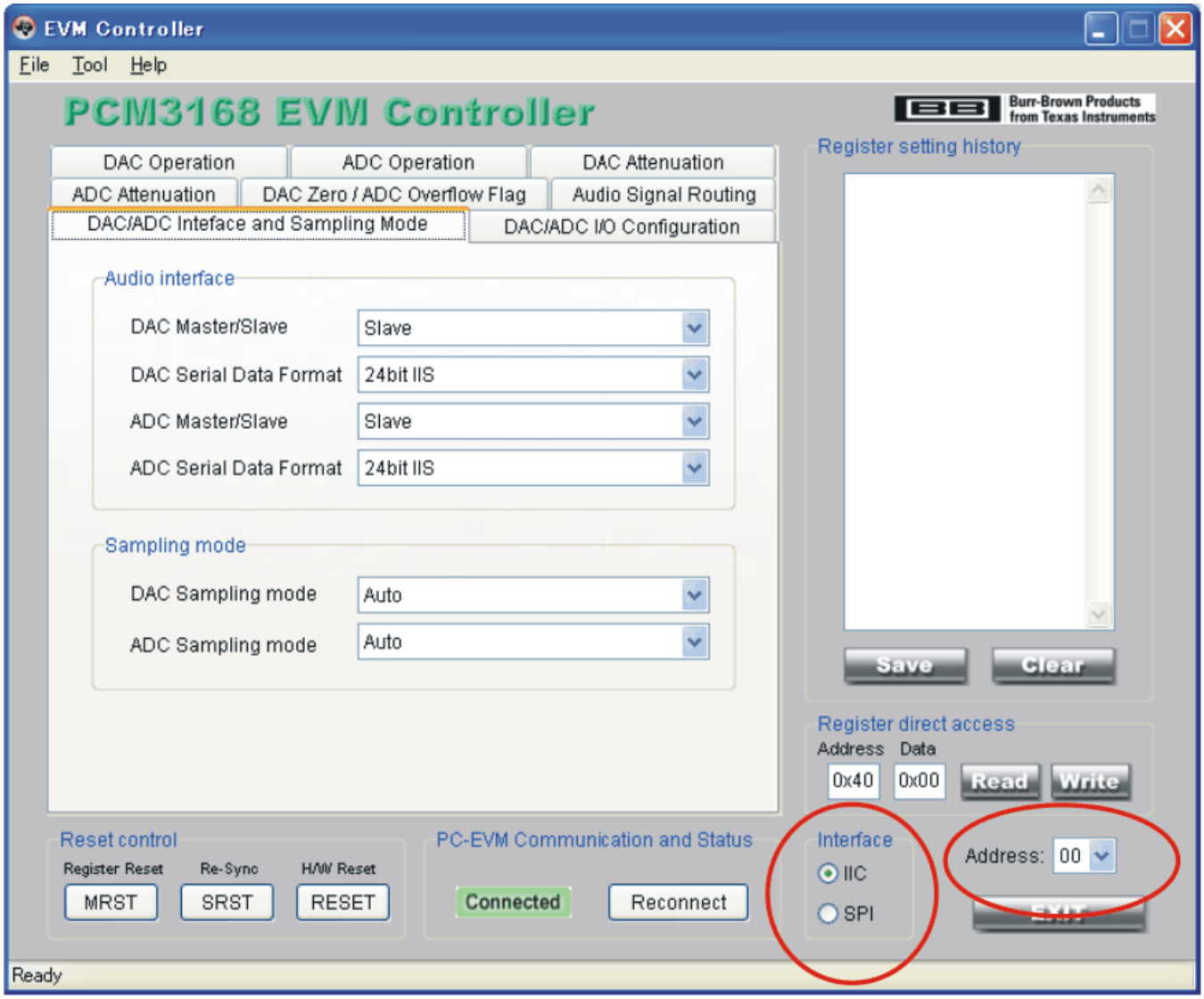


Figure 2-5. Control Interface Settings

Control Interface Mode Setting Radio Button

The default setting for the software is SPI mode. The software must have the same setting as HDR425 on the EVM. When the interface setting or the I^2C address changes, the ***Reconnect*** button must be pushed.

The preferred mode setting is saved in the software .ini file (automatically generated by the application software); thus, the same setting is applied at subsequent software startups.

I^2C Address Selection

The I^2C address of the EVM and the software must be the same. When the I^2C address in the software is changed, the ***Reconnect*** button must be pushed.

Figure 2-6 indicates the register setting history functions.

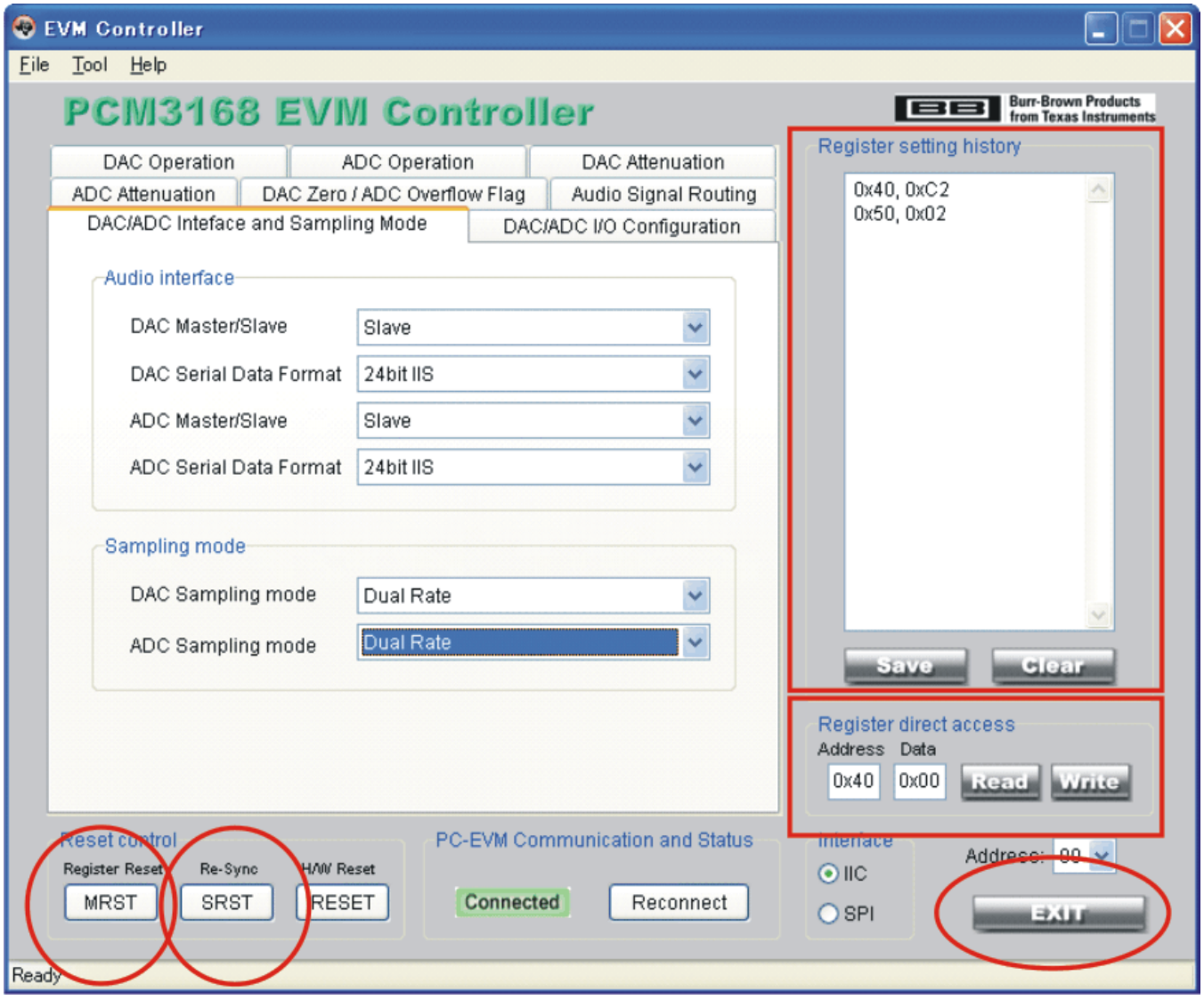


Figure 2-6. Register Setting History

Register Setting History

The Register Setting history is shown as *Register Address, Register Data* in hexadecimal. The history data can be downloaded as a comma-separated value (.csv)-format file; to download the file, press the ***Save*** button. There is also an upload function available from the File menu (see Figure 2-15).

The ***Clear*** button clears the history displayed in this window.

Register Direct Access

Both functions of reading and writing any data are available.

MRST (Mode Register Reset) Button

This button initializes all of the PCM3168A register settings. After reset, the application software settings also return to the respective default values.

SRST (System Reset) Button

This button resynchronizes the PCM3168A. Register settings are not cleared.

EXIT Button

This button exits and closes the application software.

The DAC and ADC interface and sampling mode tab is shown in Figure 2-7.

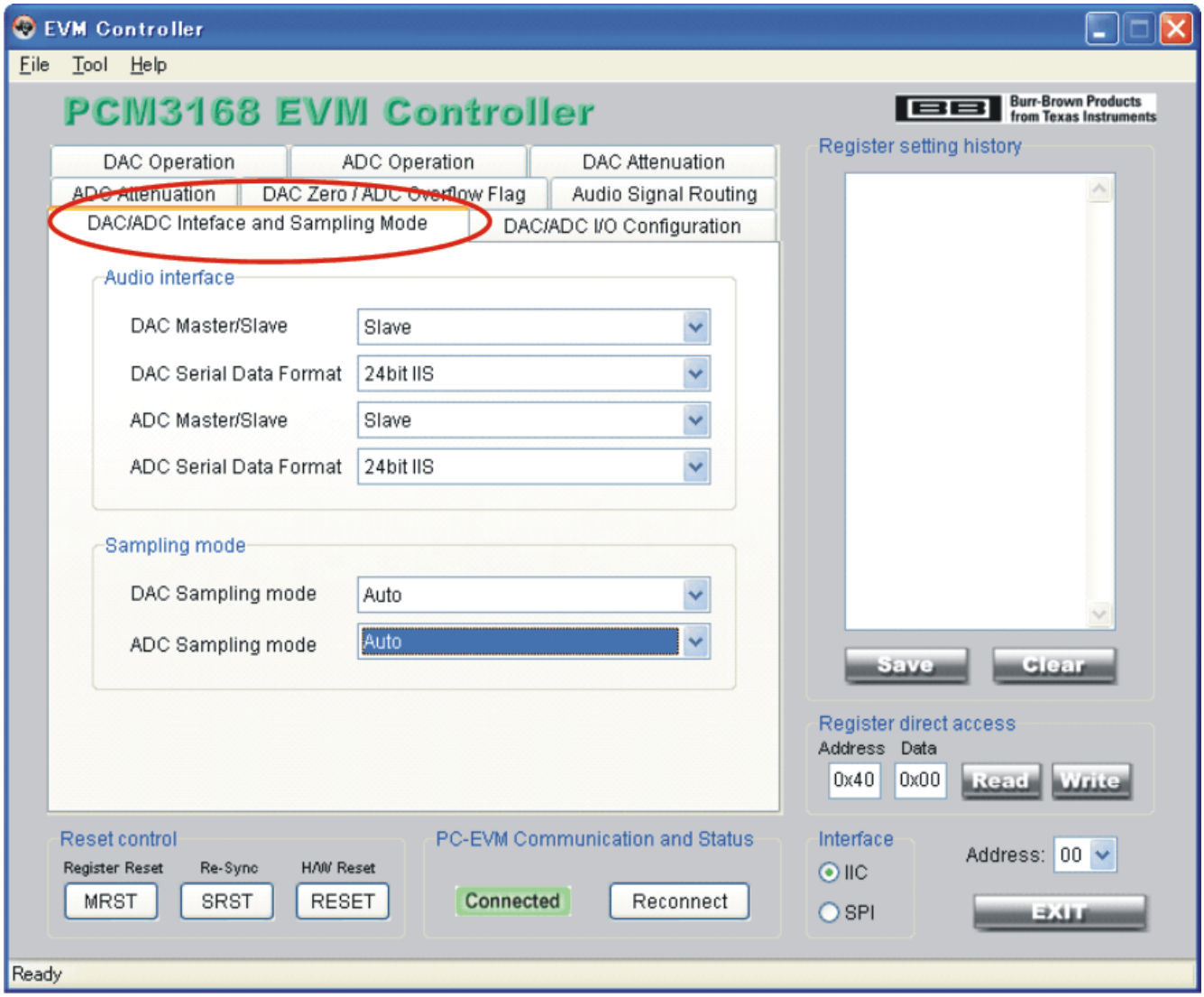


Figure 2-7. DAC/ADC Interface and Sampling Mode Tab

This window shows the startup screen of the application software. In this tab, the audio interface and sampling mode for the PCM3168A ADC/DAC sections can be independently set. The following settings are available for the ADC and DAC sections, respectively:

- DAC audio interface mode and format
- ADC audio interface mode and format
- DAC oversampling mode
- ADC oversampling mode

Figure 2-8 illustrates the DAC and ADC input/output configuration tab.

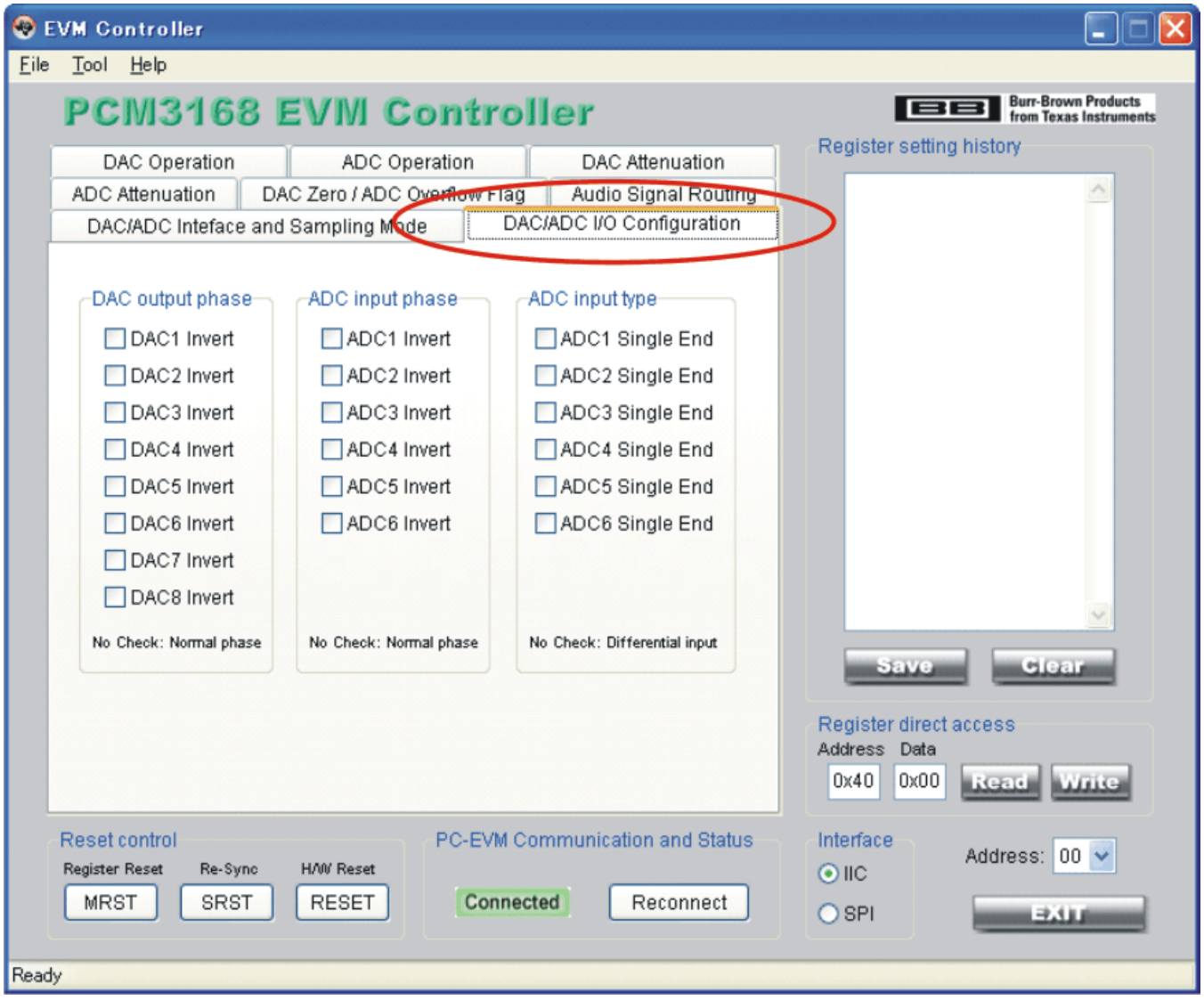


Figure 2-8. DAC/ADC I/O Configuration Tab

The following settings for the PCM3168A are available by ADC/DAC channel:

- DAC output phase
- ADC input phase
- ADC input configuration (differential or single-ended)

Figure 2-9 shows the ADC attenuation tab.

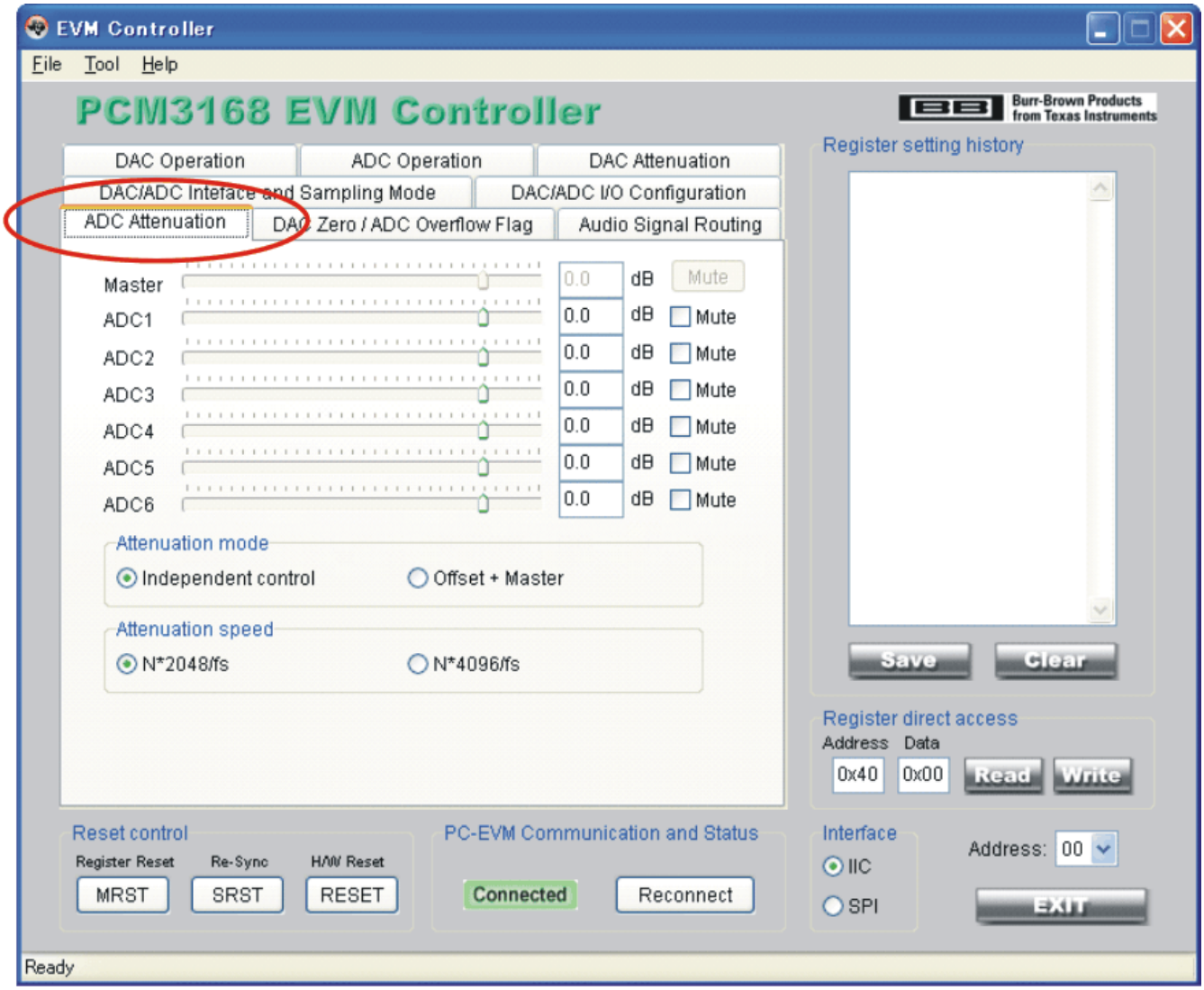


Figure 2-9. ADC Attenuation Tab

This tab features the following settings for the PCM3168A:

- ADC master attenuation level
- ADC attenuation level by channel (CH1 through CH6)
- ADC mute
- ADC attenuation mode
- ADC attenuation speed

Figure 2-10 illustrates the DAC Zero/ADC Overflow Flag tab.

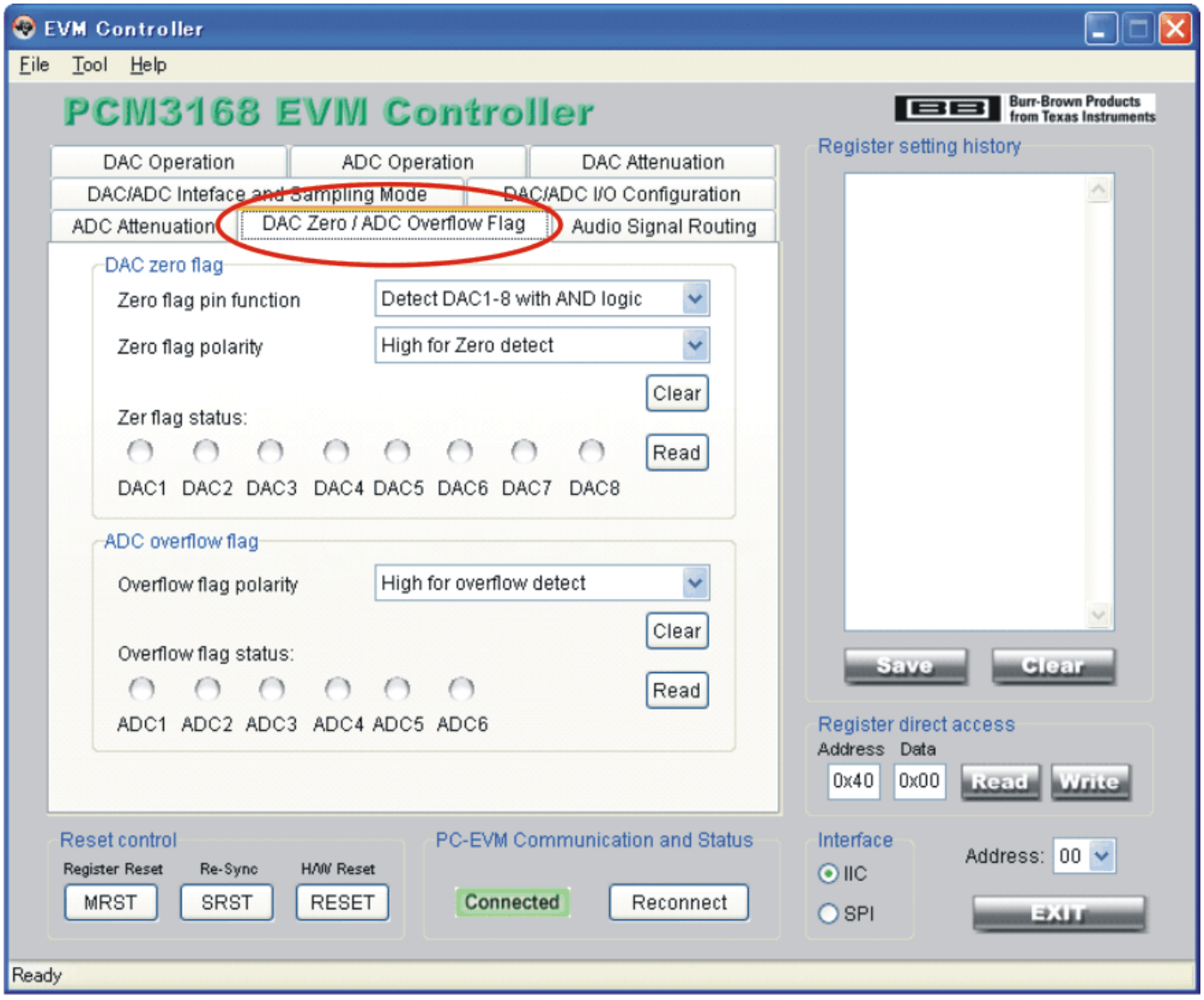


Figure 2-10. DAC Zero/ADC Overflow Flag Tab

The following settings and controls for the PCM3168A are available in this tab:

- DAC zero flag function and polarity
- DAC zero flag register read-out function
- ADC overflow flag polarity
- ADC overflow flag register read-out function

The Audio Signal Routing tab is shown in Figure 2-11.

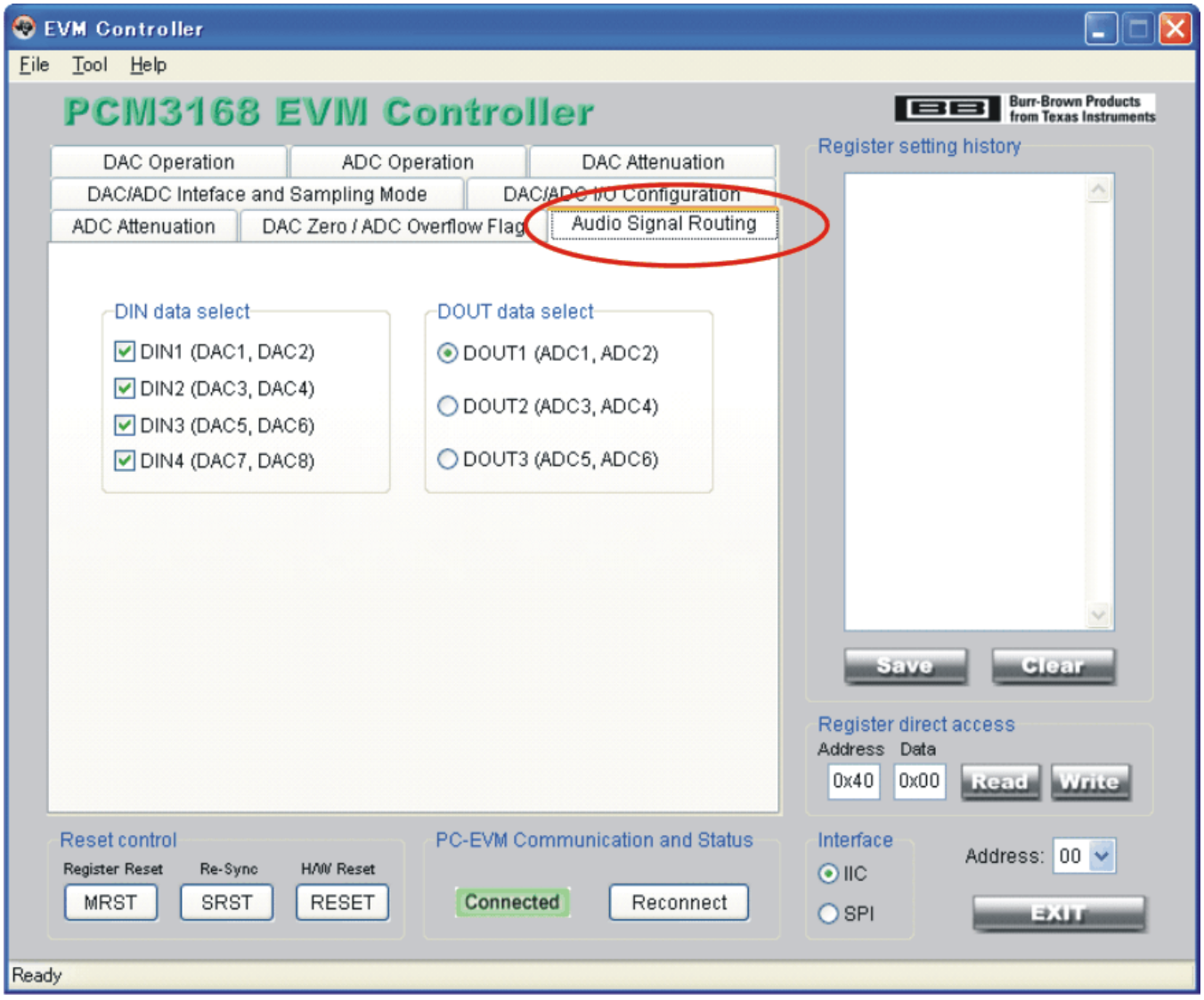


Figure 2-11. Audio Signal Routing Tab

This tab controls the EVM signal path for the PCM3168A. Specifically, the user can set these configurations:

- DIN data select for setting which DAC digital input accepts DIR output data
- DOUT data select for setting which ADC digital output is allowed as DIT input data

The DAC Operation tab is illustrated in Figure 2-12.

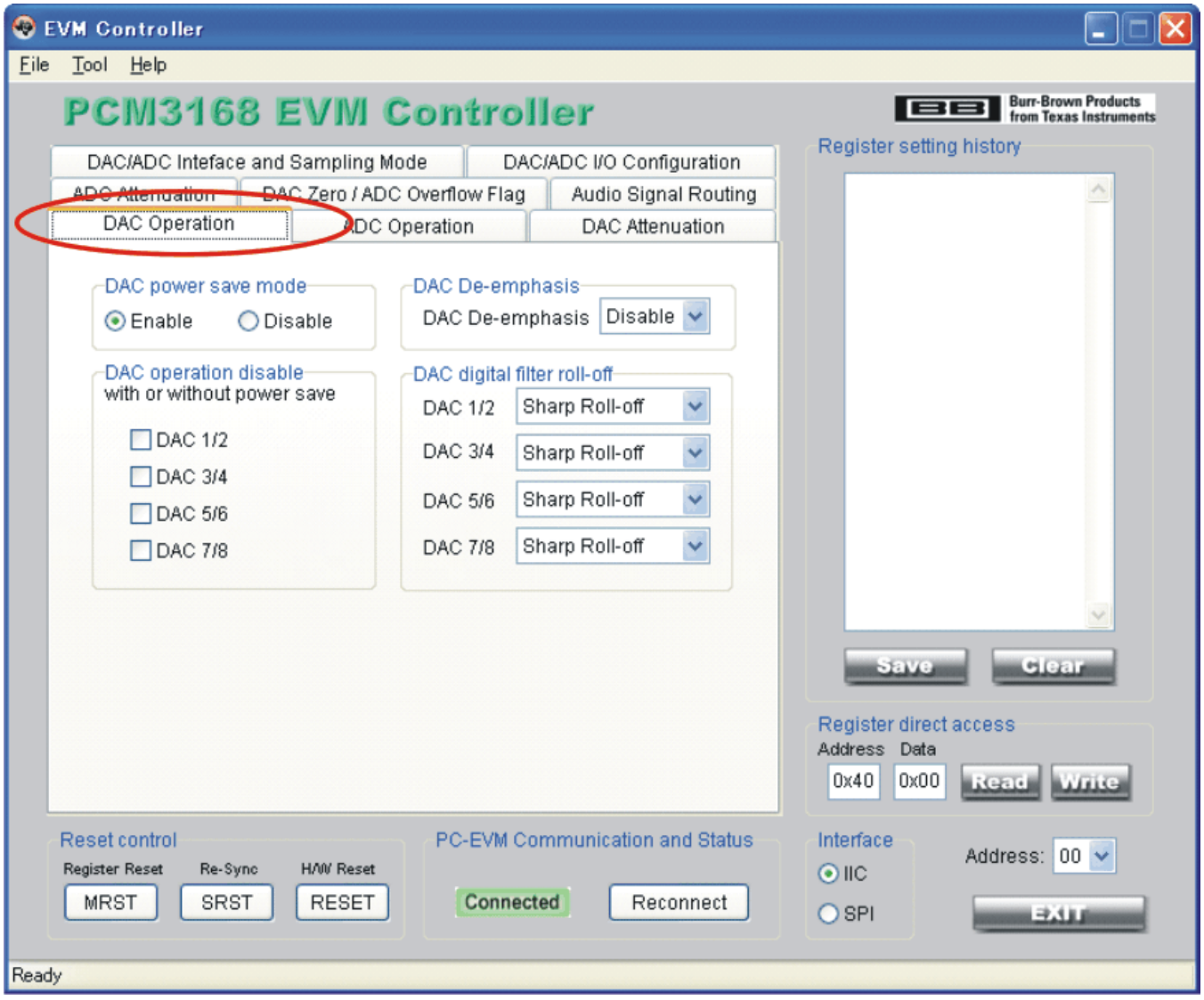


Figure 2-12. DAC Operation Tab

The following settings for PCM3168A are available in the DAC Operation tab:

- DAC power-save mode
- DAC operation disable control (with or without power save)
- DAC de-emphasis
- DAC digital filter roll-off

The ADC Operation tab is shown in Figure 2-13.

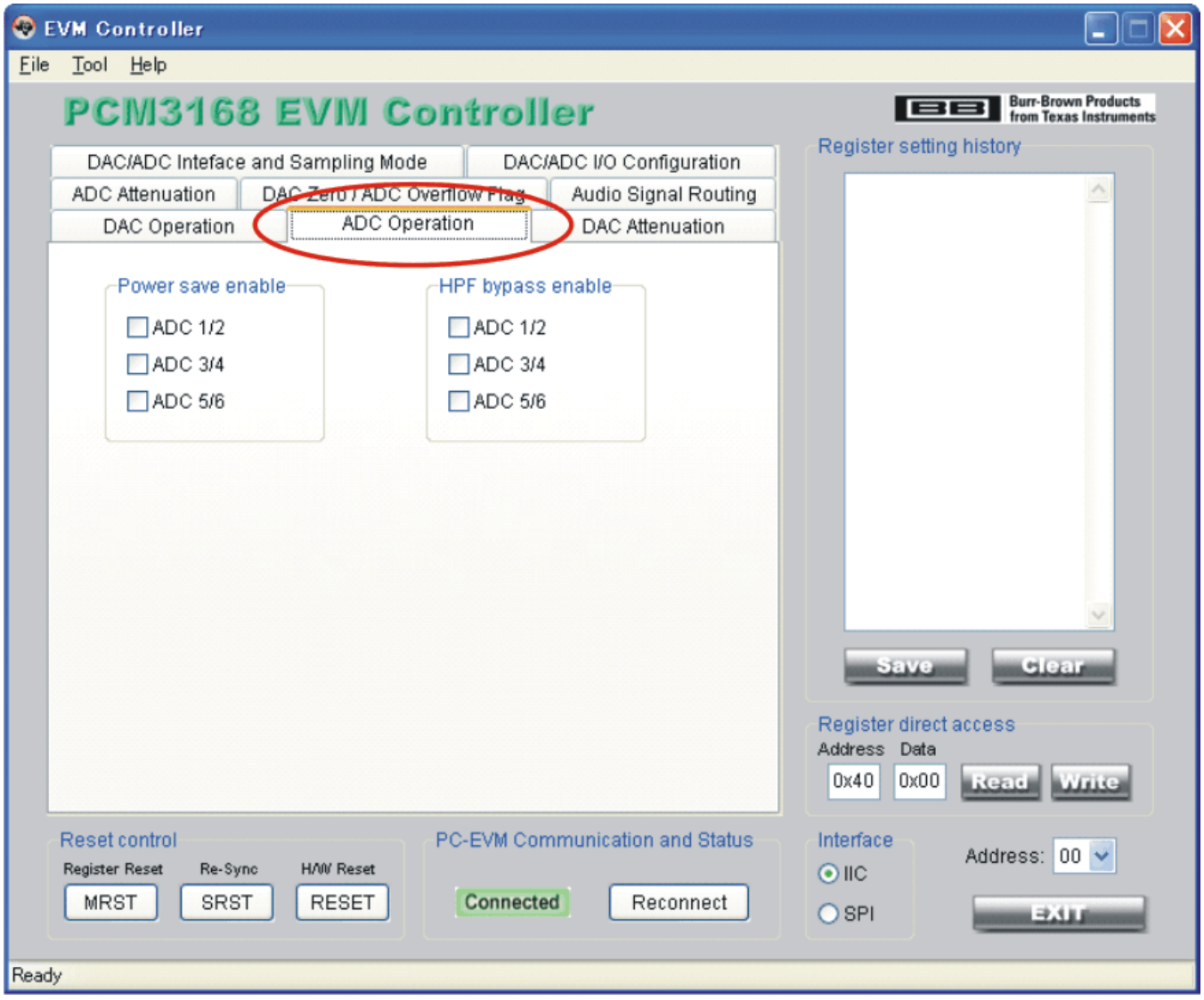


Figure 2-13. ADC Operation Tab

The following controls for PCM3168A are available in this tab:

- ADC power-save enable
- ADC high-pass filter (HPF) bypass enable

Figure 2-14 displays the DAC attentuation control tab.

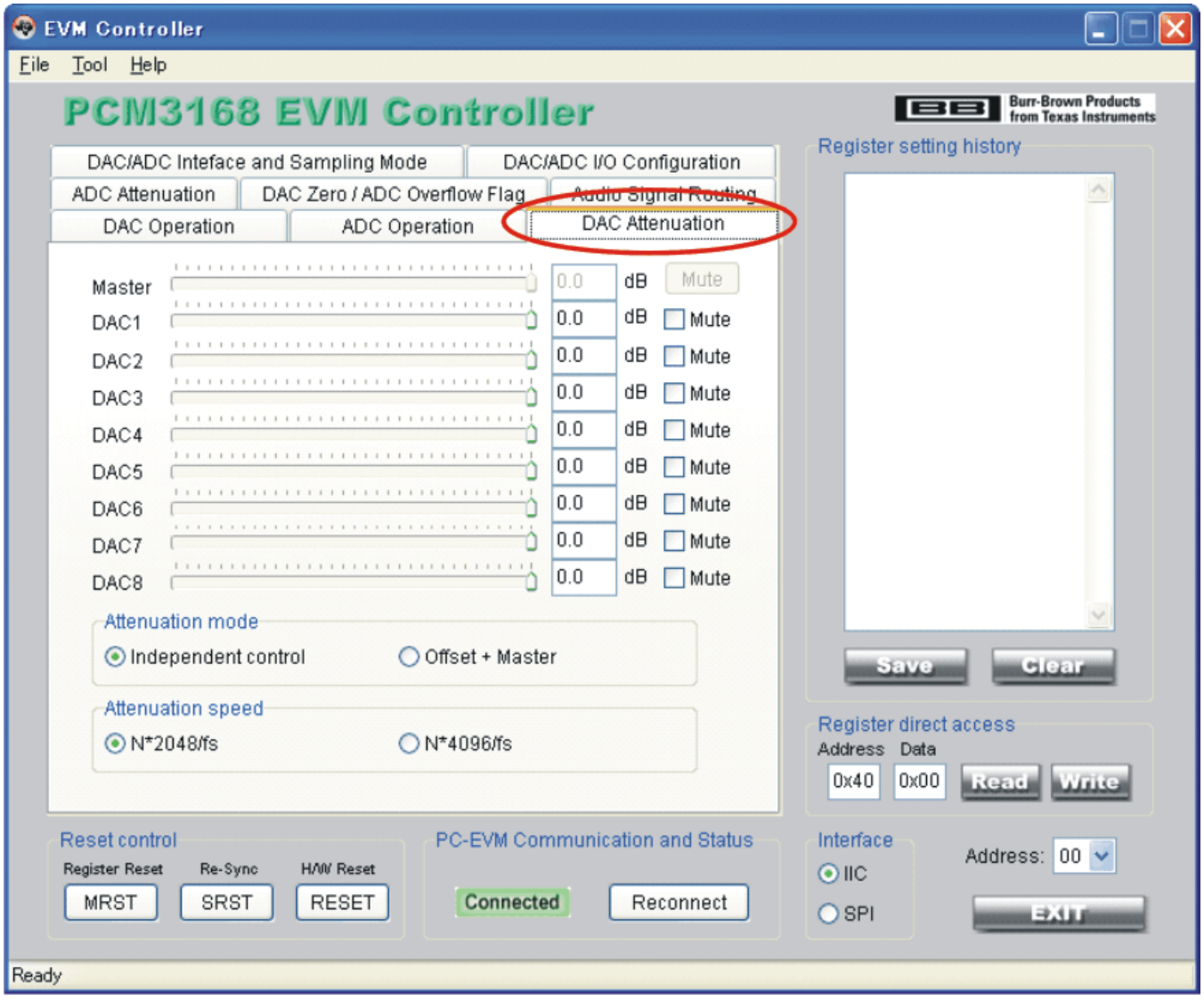


Figure 2-14. DAC Attenuation Tab

The following settings for PCM3168A are available in this tab:

- DAC master attenuation level
- DAC attenuation level by channel (CH1 through CH8)
- DAC mute
- DAC attenuation mode
- DAC attenuation speed

Figure 2-15 shows the Open Script and Save Register options (available from the ***File*** dropdown menu).

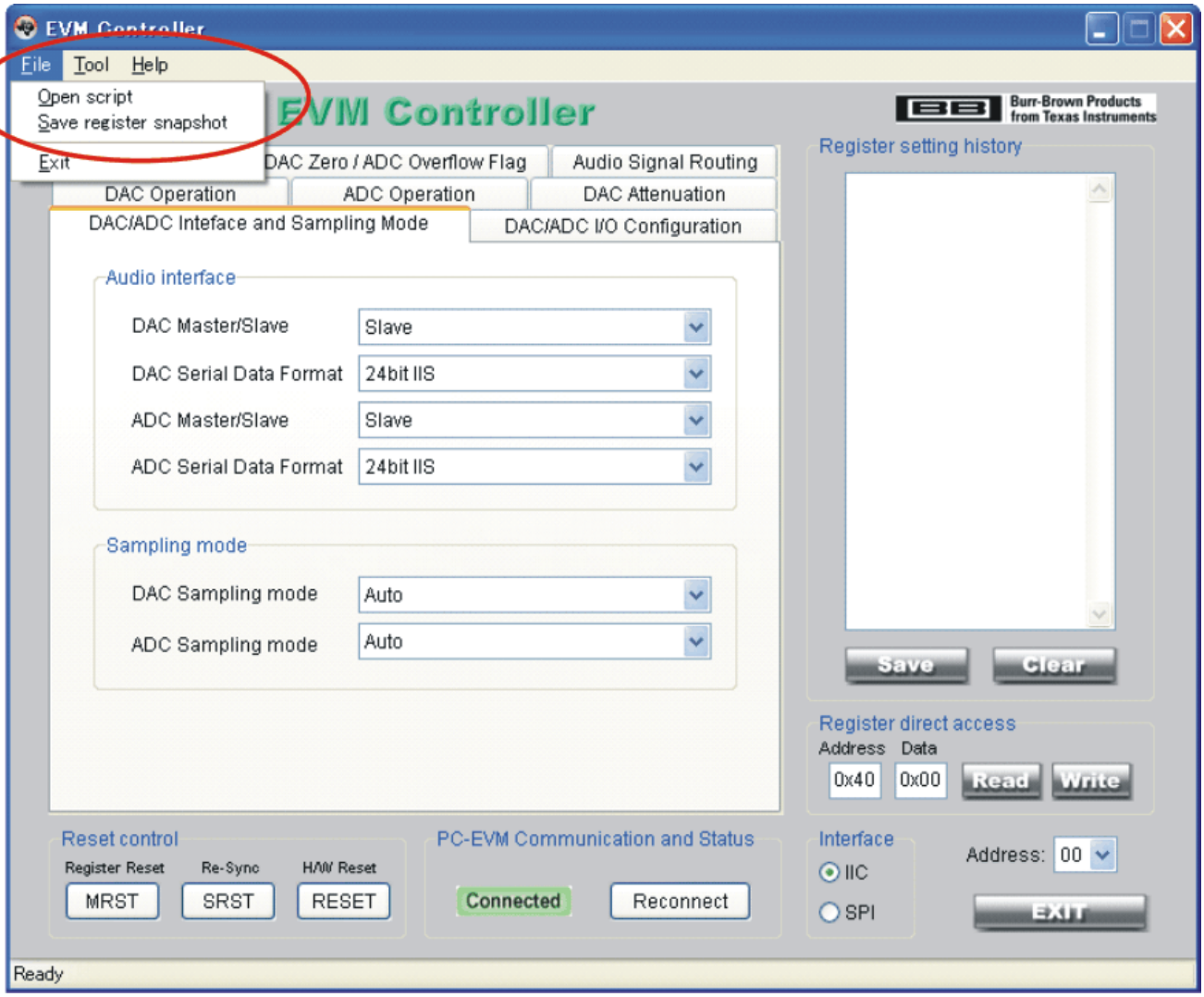


Figure 2-15. Open Script and Save Register Snapshot Menu

Open Script Menu

This menu uploads a previously saved register setting snapshot from an archived .csv file.

Save Register Snapshot Menu

This menu downloads a register setting snapshot in .csv file format. The saved register setting snapshot can be uploaded by above Open Script menu.

Figure 2-16 illustrates the Register map menu option. This menu shows all registers of the PCM3168A in a new window in register map format (see Figure 2-17).

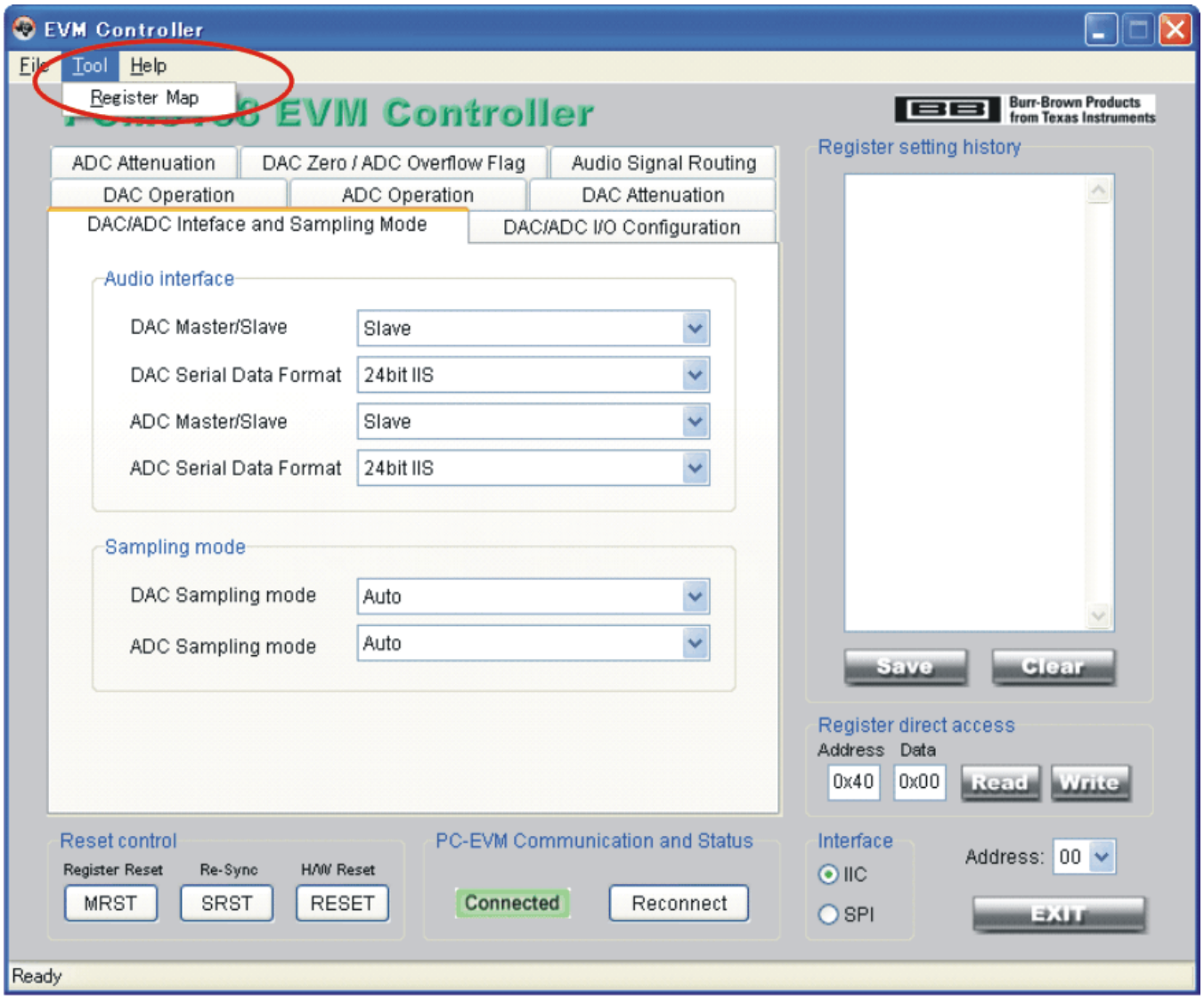
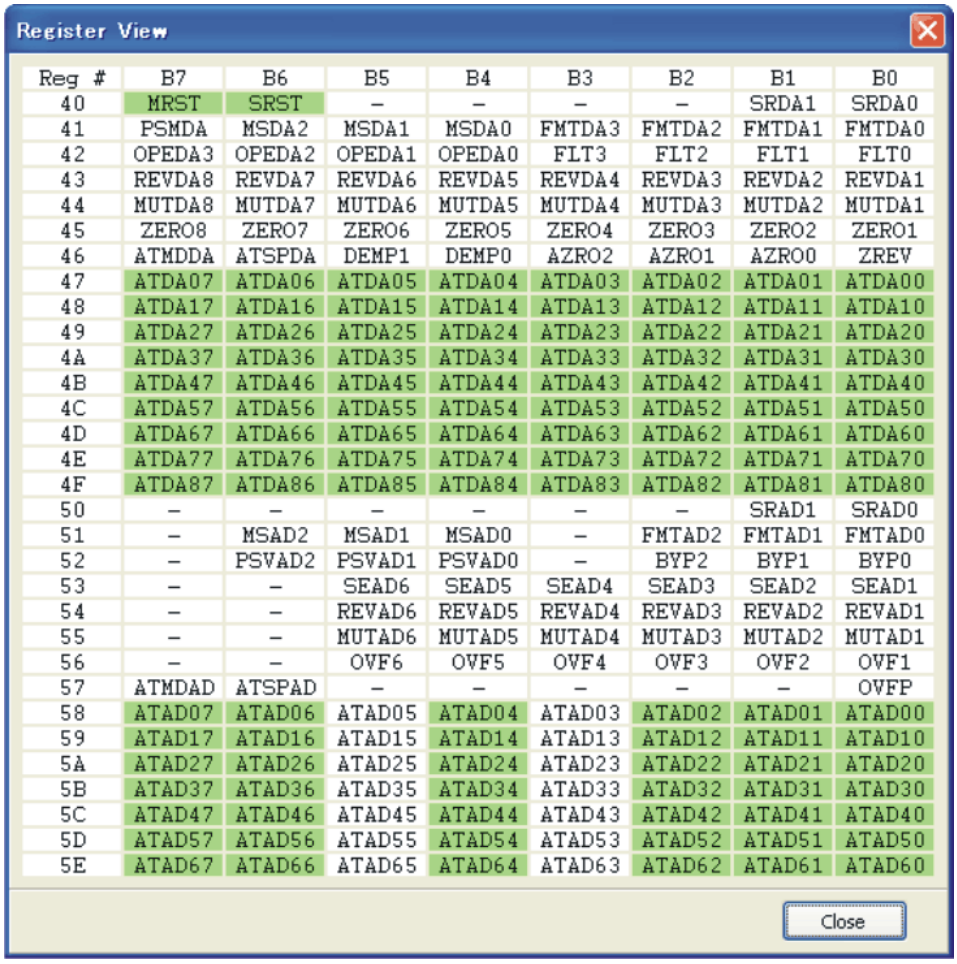


Figure 2-16. Register Map Menu



Reg #	B7	B6	B5	B4	B3	B2	B1	B0
40	MRST	SRST	–	–	–	–	SRDA1	SRDA0
41	PSMDA	MSDA2	MSDA1	MSDA0	FMTDA3	FMTDA2	FMTDA1	FMTDA0
42	OPEDA3	OPEDA2	OPEDA1	OPEDA0	FLT3	FLT2	FLT1	FLT0
43	REVDA8	REVDA7	REVDA6	REVDA5	REVDA4	REVDA3	REVDA2	REVDA1
44	MUTDA8	MUTDA7	MUTDA6	MUTDA5	MUTDA4	MUTDA3	MUTDA2	MUTDA1
45	ZERO8	ZERO7	ZERO6	ZERO5	ZERO4	ZERO3	ZERO2	ZERO1
46	ATMDDA	ATSPDA	DEMP1	DEMP0	AZRO2	AZRO1	AZRO0	ZREV
47	ATDA07	ATDA06	ATDA05	ATDA04	ATDA03	ATDA02	ATDA01	ATDA00
48	ATDA17	ATDA16	ATDA15	ATDA14	ATDA13	ATDA12	ATDA11	ATDA10
49	ATDA27	ATDA26	ATDA25	ATDA24	ATDA23	ATDA22	ATDA21	ATDA20
4A	ATDA37	ATDA36	ATDA35	ATDA34	ATDA33	ATDA32	ATDA31	ATDA30
4B	ATDA47	ATDA46	ATDA45	ATDA44	ATDA43	ATDA42	ATDA41	ATDA40
4C	ATDA57	ATDA56	ATDA55	ATDA54	ATDA53	ATDA52	ATDA51	ATDA50
4D	ATDA67	ATDA66	ATDA65	ATDA64	ATDA63	ATDA62	ATDA61	ATDA60
4E	ATDA77	ATDA76	ATDA75	ATDA74	ATDA73	ATDA72	ATDA71	ATDA70
4F	ATDA87	ATDA86	ATDA85	ATDA84	ATDA83	ATDA82	ATDA81	ATDA80
50	–	–	–	–	–	–	SRAD1	SRAD0
51	–	MSAD2	MSAD1	MSAD0	–	FMTAD2	FMTAD1	FMTAD0
52	–	PSVAD2	PSVAD1	PSVAD0	–	BYP2	BYP1	BYP0
53	–	–	SEAD6	SEAD5	SEAD4	SEAD3	SEAD2	SEAD1
54	–	–	REVAD6	REVAD5	REVAD4	REVAD3	REVAD2	REVAD1
55	–	–	MUTAD6	MUTAD5	MUTAD4	MUTAD3	MUTAD2	MUTAD1
56	–	–	OVF6	OVF5	OVF4	OVF3	OVF2	OVF1
57	ATMDAD	ATSPAD	–	–	–	–	–	OVFP
58	ATAD07	ATAD06	ATAD05	ATAD04	ATAD03	ATAD02	ATAD01	ATAD00
59	ATAD17	ATAD16	ATAD15	ATAD14	ATAD13	ATAD12	ATAD11	ATAD10
5A	ATAD27	ATAD26	ATAD25	ATAD24	ATAD23	ATAD22	ATAD21	ATAD20
5B	ATAD37	ATAD36	ATAD35	ATAD34	ATAD33	ATAD32	ATAD31	ATAD30
5C	ATAD47	ATAD46	ATAD45	ATAD44	ATAD43	ATAD42	ATAD41	ATAD40
5D	ATAD57	ATAD56	ATAD55	ATAD54	ATAD53	ATAD52	ATAD51	ATAD50
5E	ATAD67	ATAD66	ATAD65	ATAD64	ATAD63	ATAD62	ATAD61	ATAD60

Figure 2-17. Register View Window

The Register View window has three options (available in the application software):

Open Register View Window

Select *Tools* → *Register Map*.

Register View Window Color Indicators

Green shaded cells (as shown in Figure 2-17) indicate a register value of '1'. White shaded cells indicate a register value of '0'.

Register View Window Operation

After updating a register setting through the application software, the update is applied to this register view.

Typical Performance and Example Data

This chapter presents typical performance and example measurement data of the PCM3168A when measured with the DEM-DAI3168A.

Topic **Page**

3.1 Typical Performance Data

Figure 3-1 and Figure 3-2 illustrate baseline PCM3168A ADC and DAC performance (respectively) on the DEM-DAI3168A using the S/PDIF Input/Output configuration.

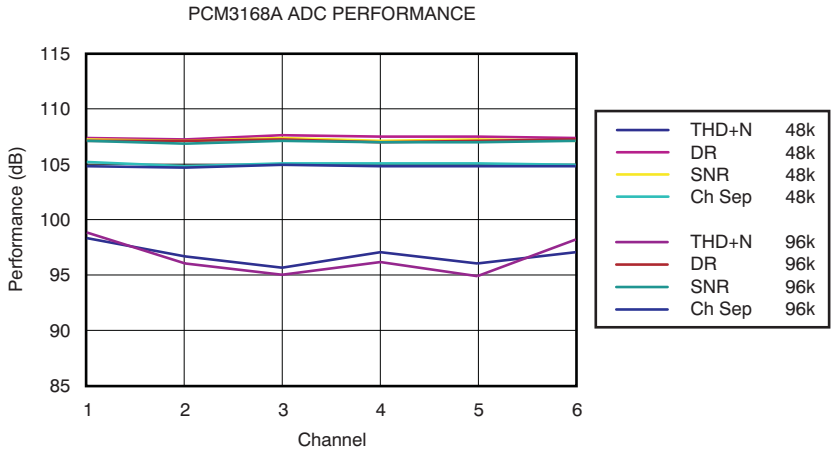


Figure 3-1. PCM3168A ADC Performance in Differential Input Mode

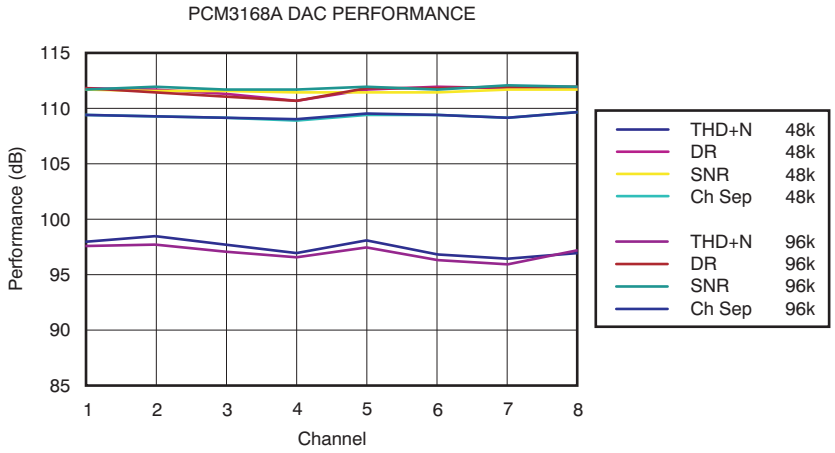


Figure 3-2. PCM3168A DAC Performance with Recommended LPF and D2S Buffer Amp

3.2 Measurement Data Example for ADC

Figure 3-3 through Figure 3-8 show example characteristic data measurements for the PCM3168A ADC.

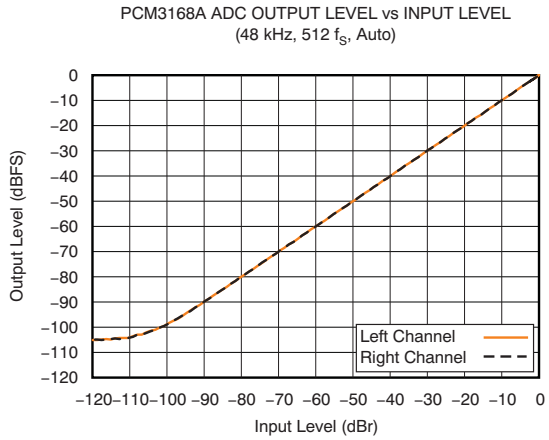


Figure 3-3. Output Level vs Input Level

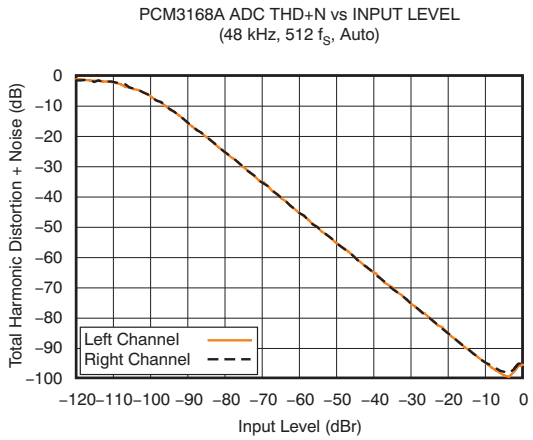


Figure 3-4. THD+N vs Input Level

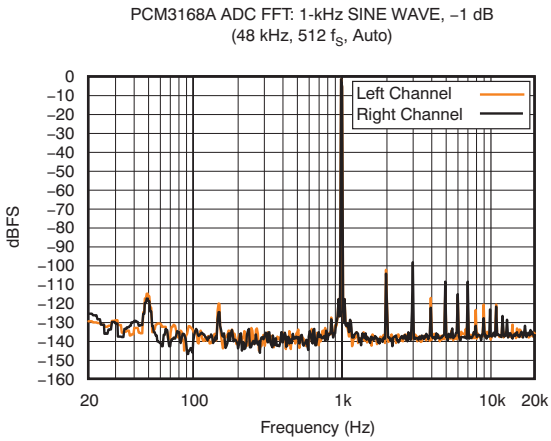


Figure 3-5. FFT for –1 dB of 1-kHz Sine Wave

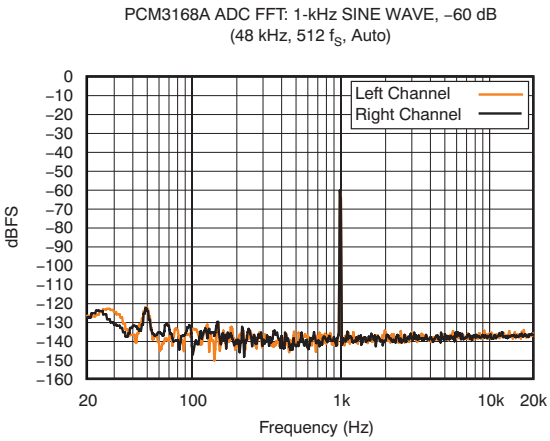


Figure 3-6. FFT for –60 dB of 1-kHz Sine Wave

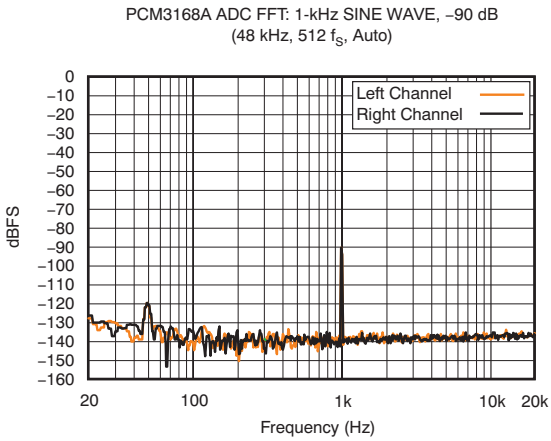


Figure 3-7. FFT for –90 dB of 1-kHz Sine Wave

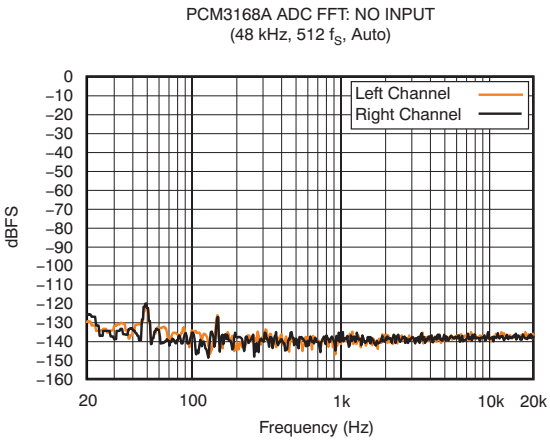


Figure 3-8. FFT for No Input Signal

3.3 Measurement Data Example for DAC

Figure 3-9 through Figure 3-14 show example performance measurements for the PCM3168A DAC.

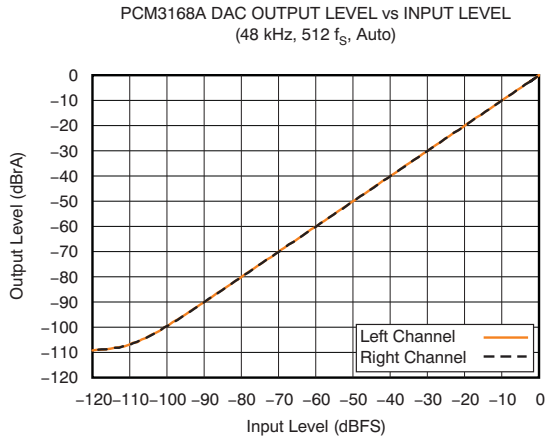


Figure 3-9. Output Level vs Input Level

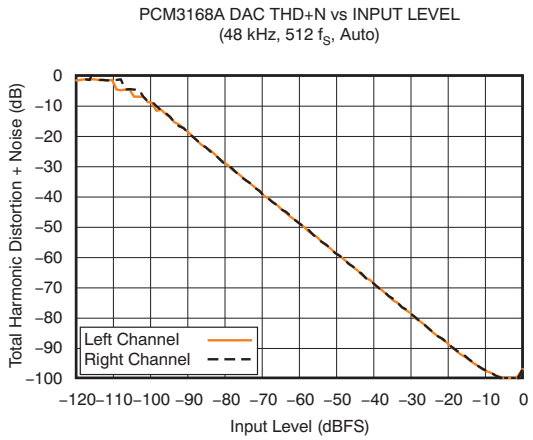


Figure 3-10. THD+N vs Input Level

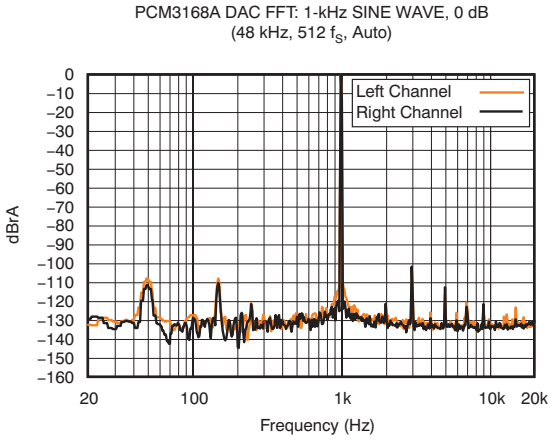


Figure 3-11. FFT for 0 dB of 1-kHz Sine Wave

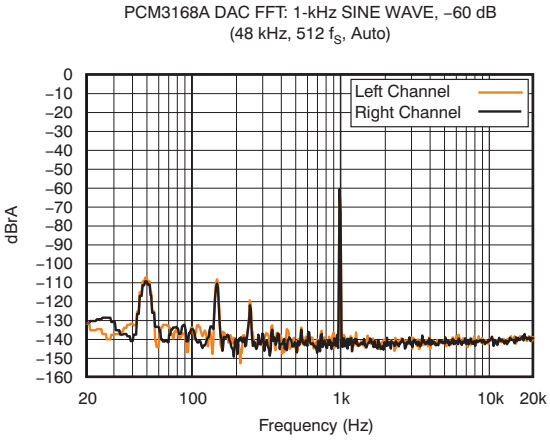


Figure 3-12. FFT for –60 dB of 1-kHz Sine Wave

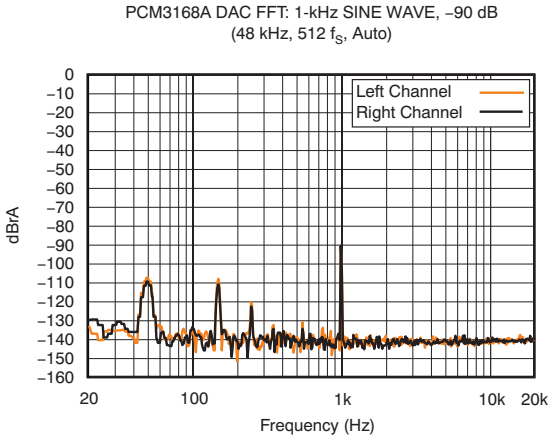


Figure 3-13. FFT for –90 dB of 1-kHz Sine Wave

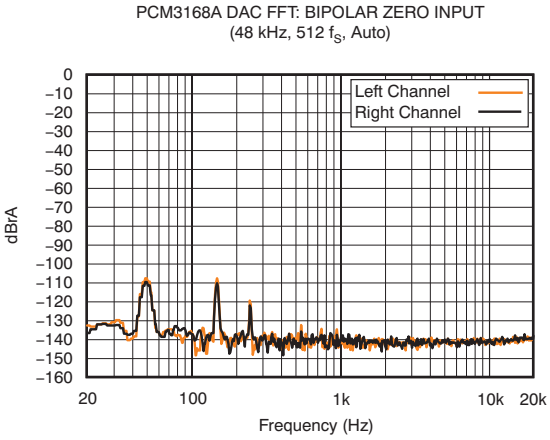


Figure 3-14. FFT for BPZ Input

Schematics and Printed Circuit Board Layouts

This chapter presents the schematics, printed circuit board (PCB) layouts, and bills of material (BOMs) of the DEM-DAI3168A, including the DEM-DAI/MCODEC and the DEM-PCM3168A.

Topic **Page**

4.1 Schematics

4.1.1 DEM-DAI/MCODEC Power Supply

The power supply section is shown in Figure 4-1.

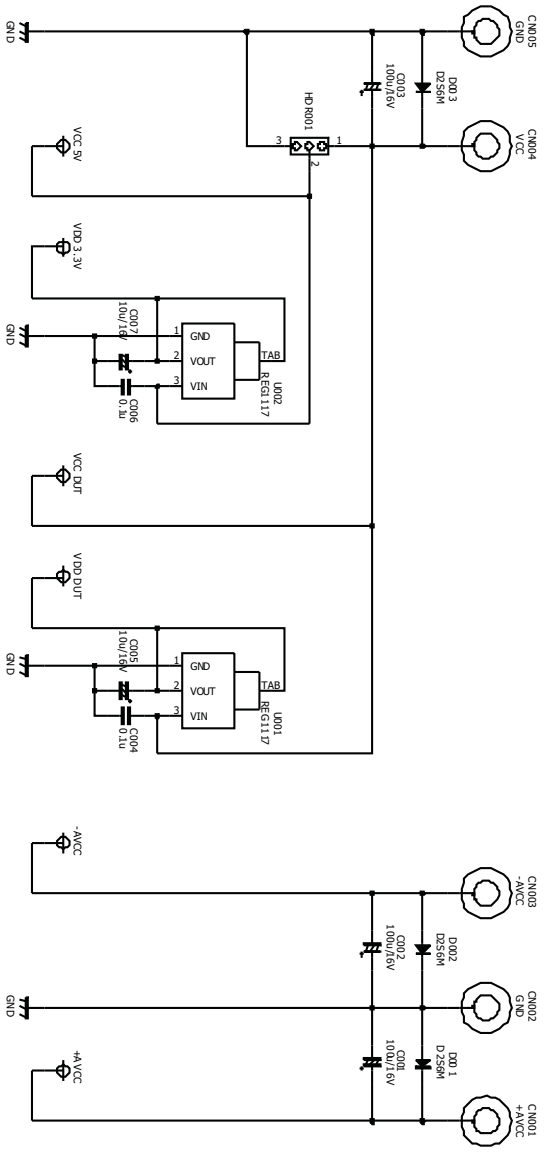


Figure 4-1. Power-Supply Section

4.1.2 DEM-DAI/MCODEC USB I/F and Control

The USB interface and control section is illustrated in Figure 4-2.

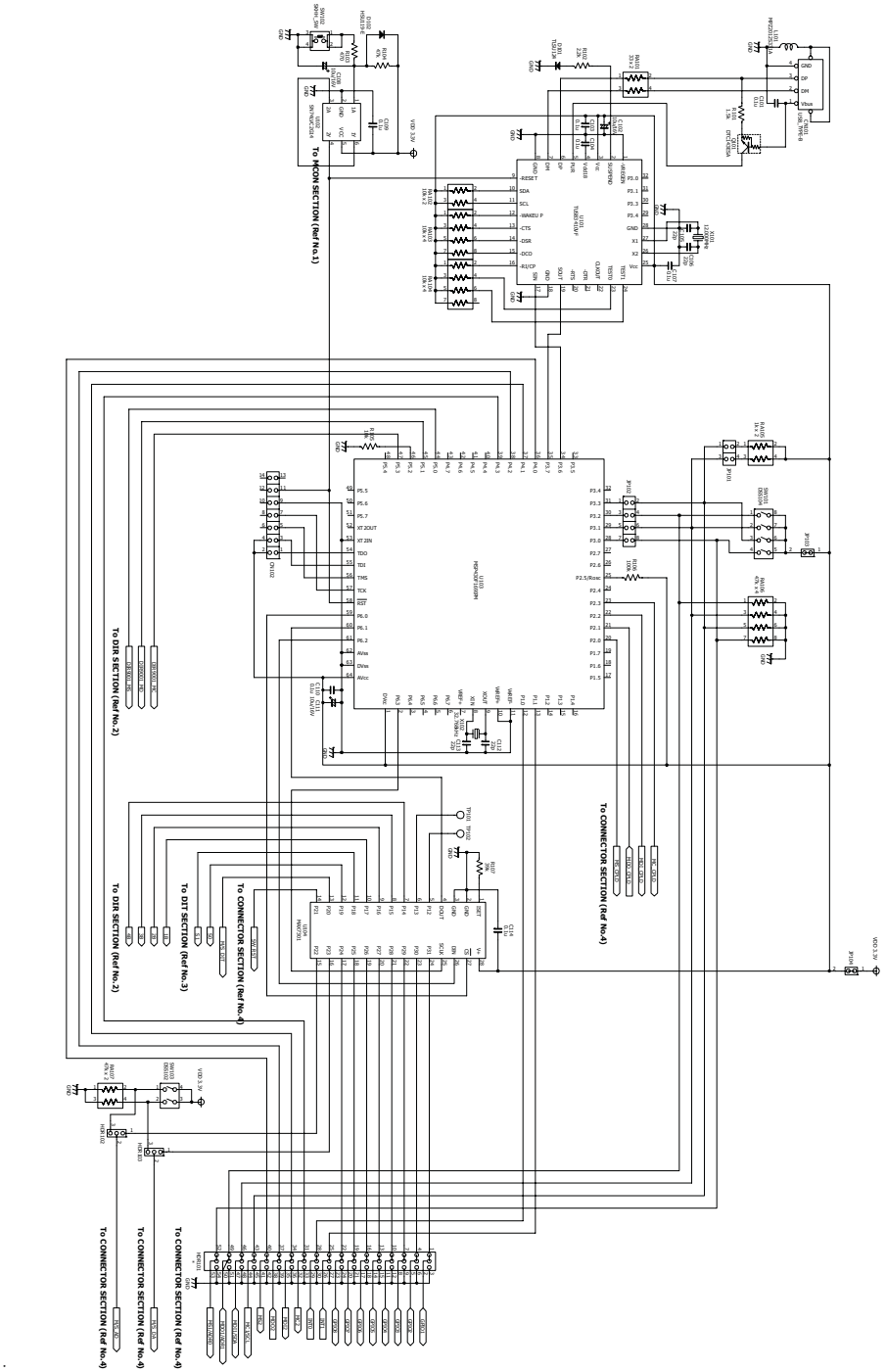


Figure 4-2. USB I/F and Control Section

4.1.3 DEM-DAI/MCODEC DIR

Figure 4-3 shows the DIR section.

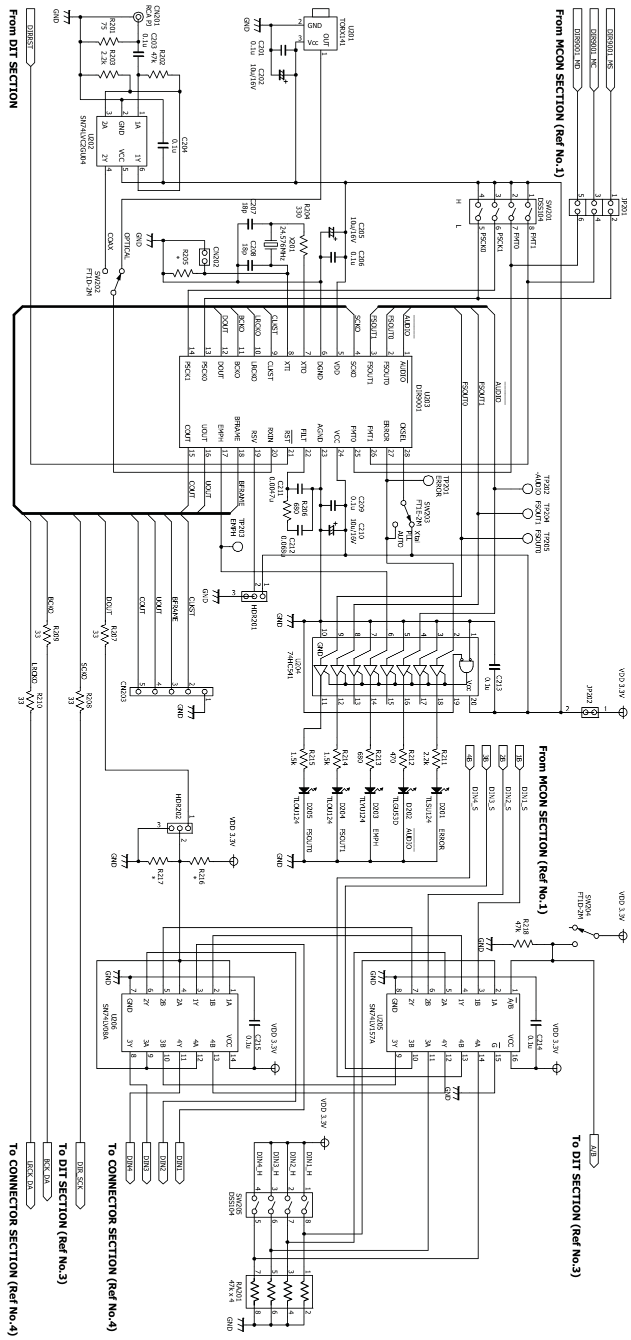


Figure 4-3. DIR Section

4.1.4 DEM-DAI/MCODEC DIT and PLL

Figure 4-4 illustrates the DIT and PLL sections.

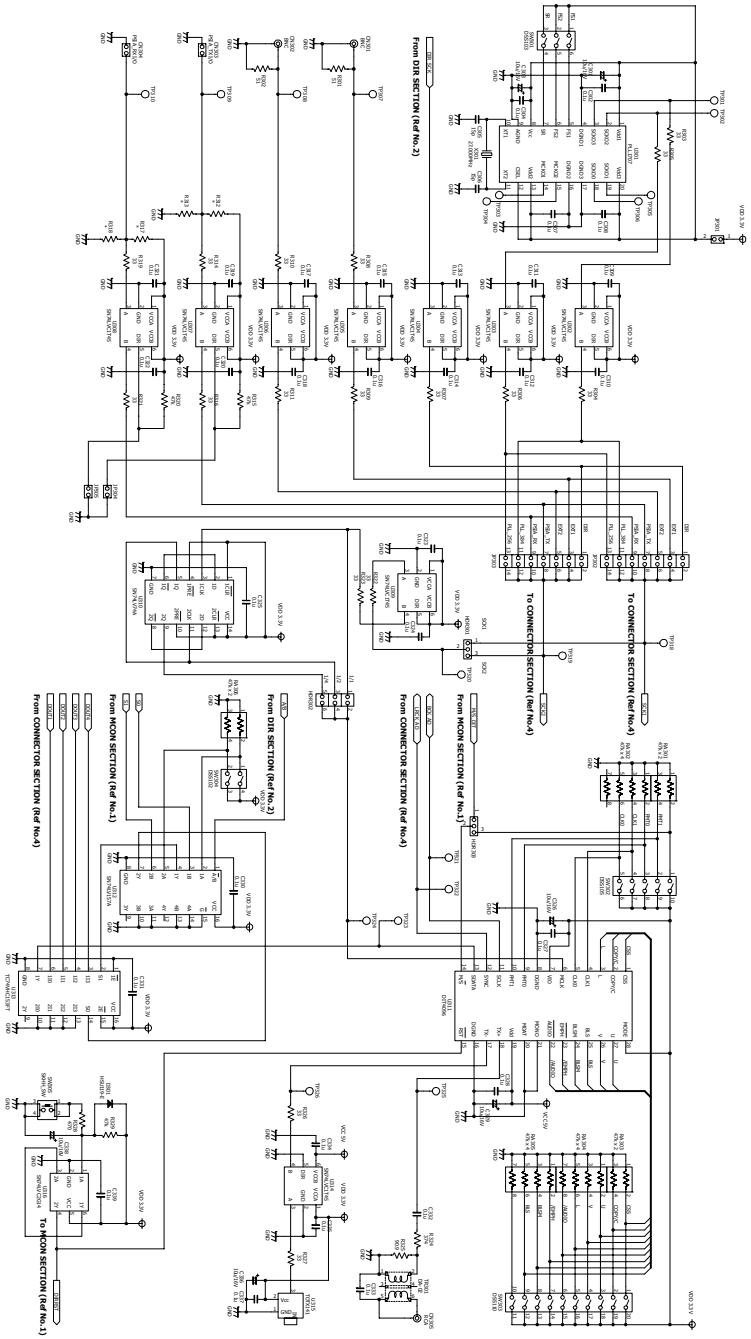


Figure 4-4. DIT and PLL Sections

4.1.5 DEM-DAI/MCODEC Audio Interface

The audio interface section is shown in Figure 4-5.

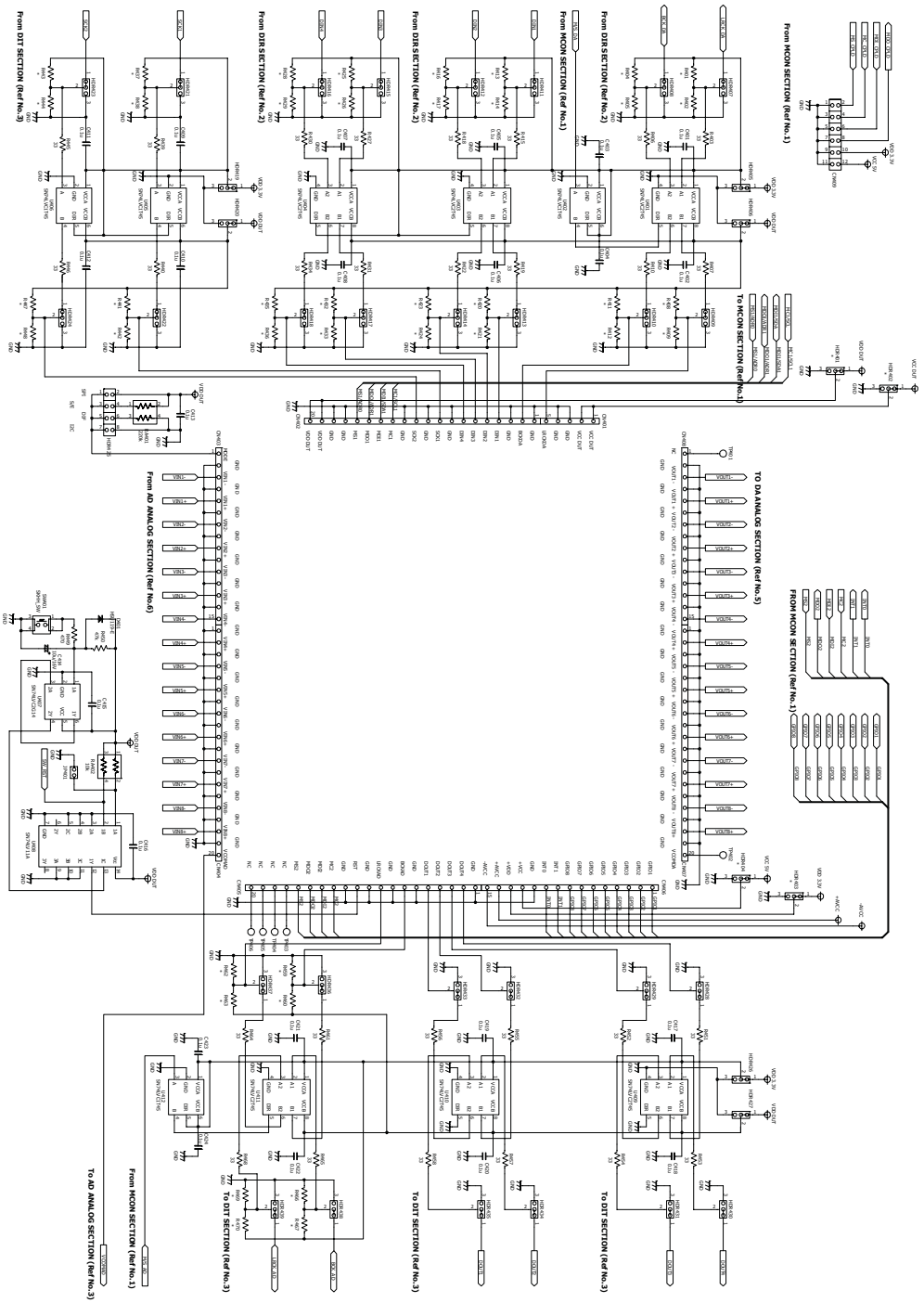


Figure 4-5. Audio Interface

4.1.6 DEM-DAI/MCODEC DA-Analog

The DA-Analog section is illustrated in Figure 4-6.

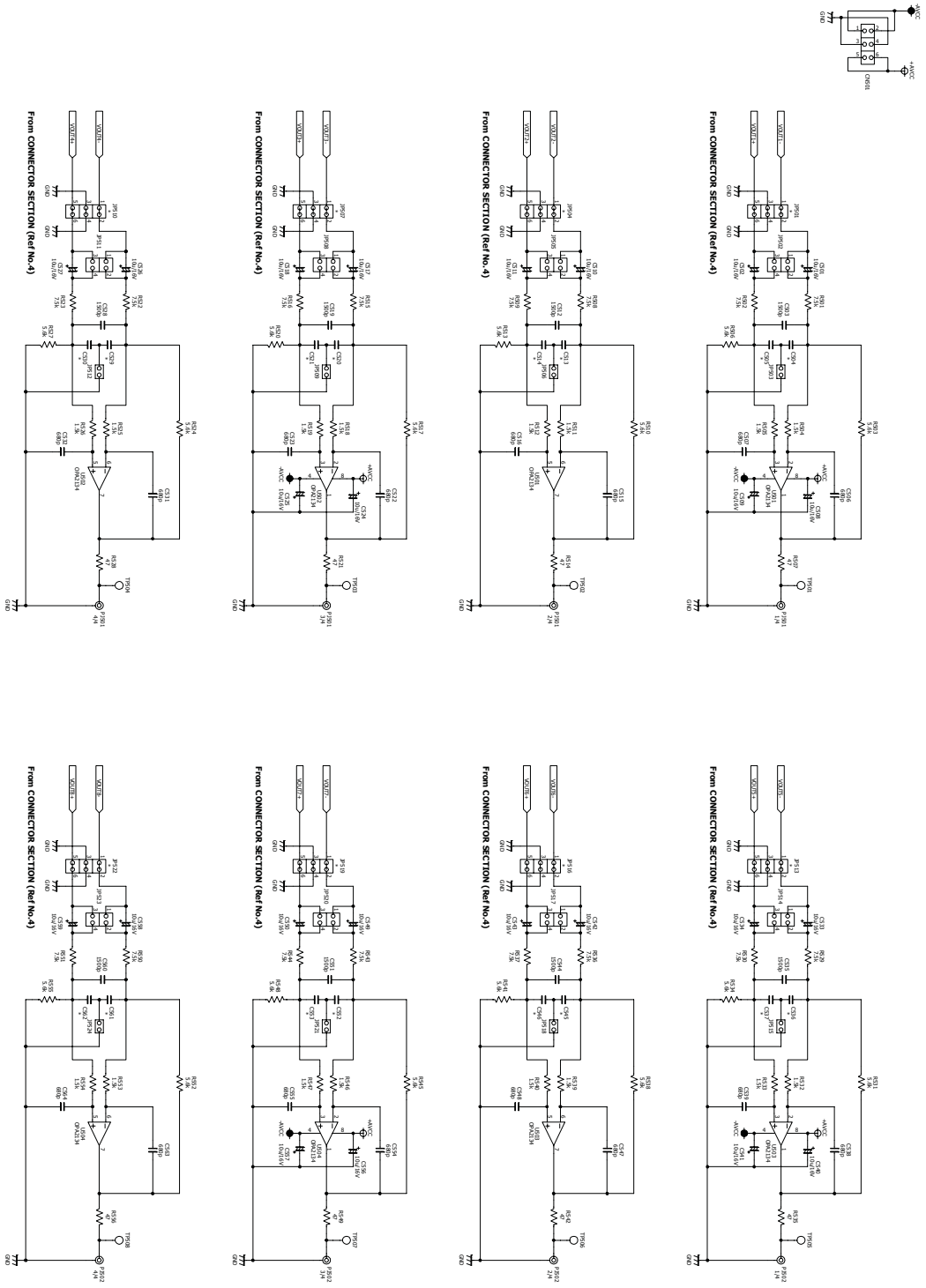


Figure 4-6. DA-Analog

4.1.7 DEM-DAI/MCODEC AD-Analog

The AD-Analog section is shown in Figure 4-7.

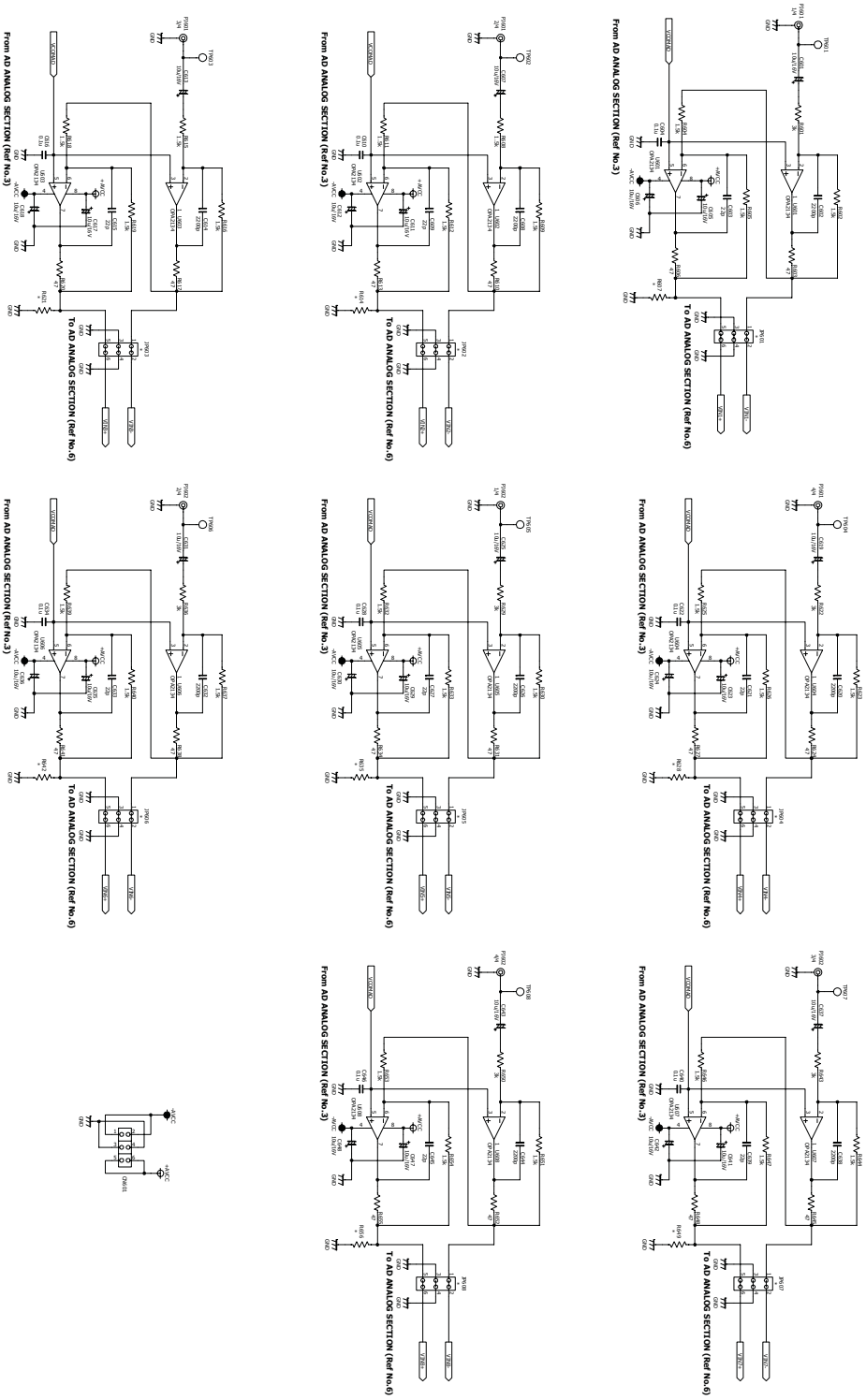


Figure 4-7. AD-Analog

4.1.8 DEM-PCM3168A (DUT Daughterboard)

Figure 4-8 shows the DEM-PCM3168A schematic.

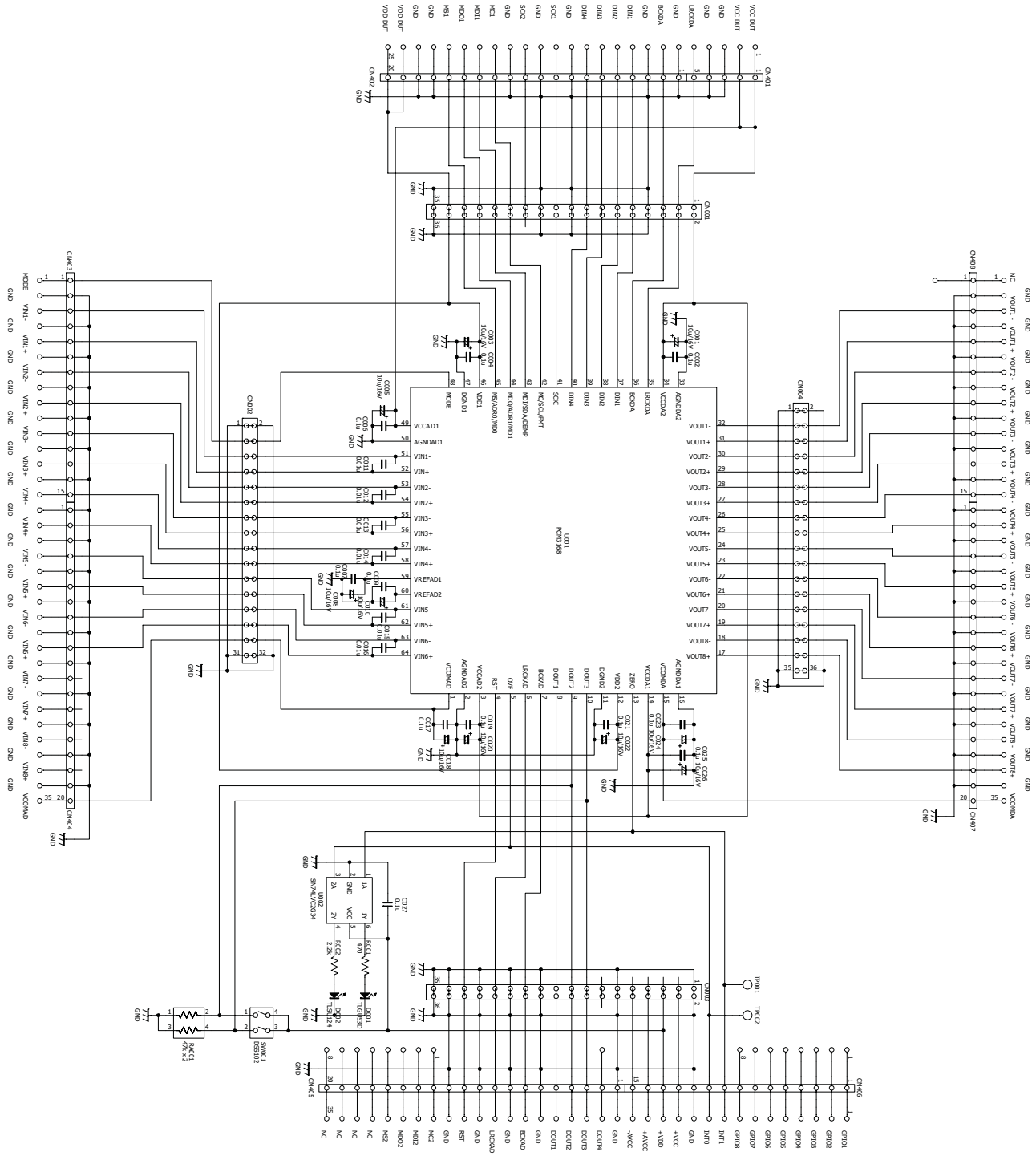


Figure 4-8. DEM-PCM3168A

4.2 Printed Circuit Board Layouts

Note: Board layouts are not to scale. These figures are intended to show how the board is laid out; they are not intended to be used for manufacturing DEM-DAI3168A PCBs.

4.2.1 DEM-DAI/MCODEC Silk Plane (Top)

Figure 4-9 shows the silkscreen plane, top layer image.

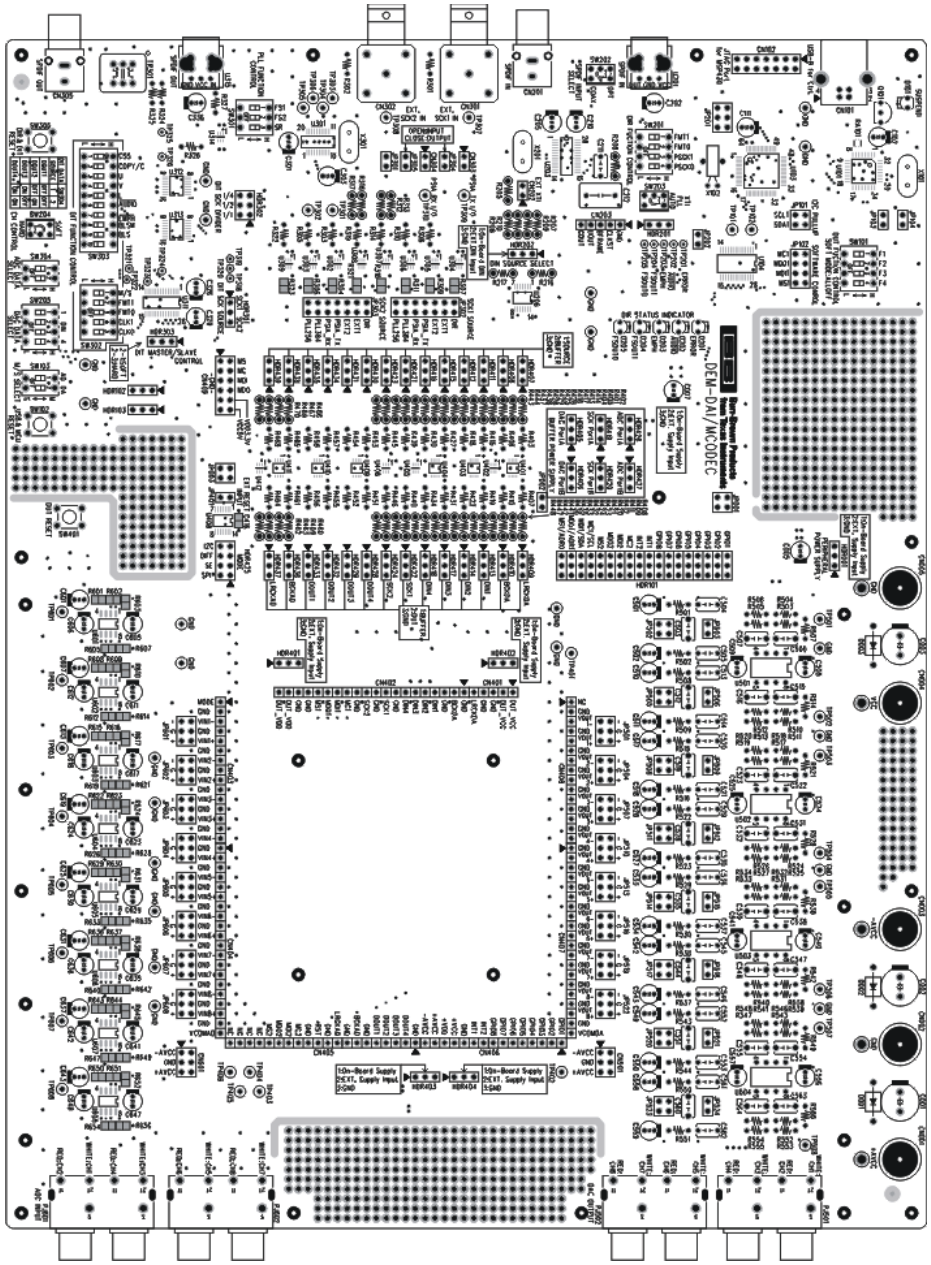


Figure 4-9. Silk Plane (Top)

4.2.2 DEM-DAI/MCODEC Silk Plane (Bottom)

Figure 4-10 shows the silkscreen plane, bottom layer image.

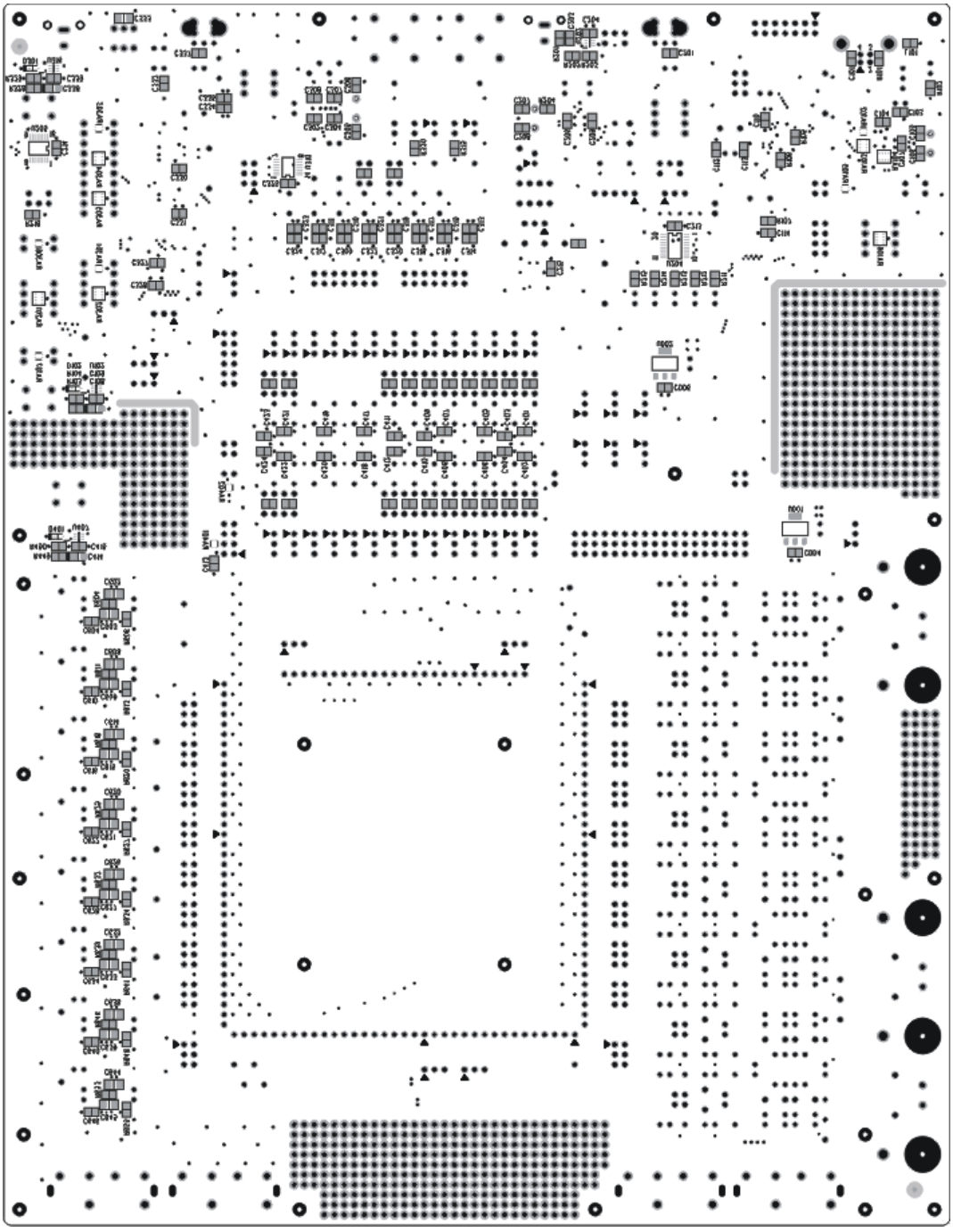


Figure 4-10. Silk Plane (Bottom)

4.2.3 DEM-DAI/MCODEC Layout Plane (Top)

Figure 4-11 shows the layout plane, top layer image.

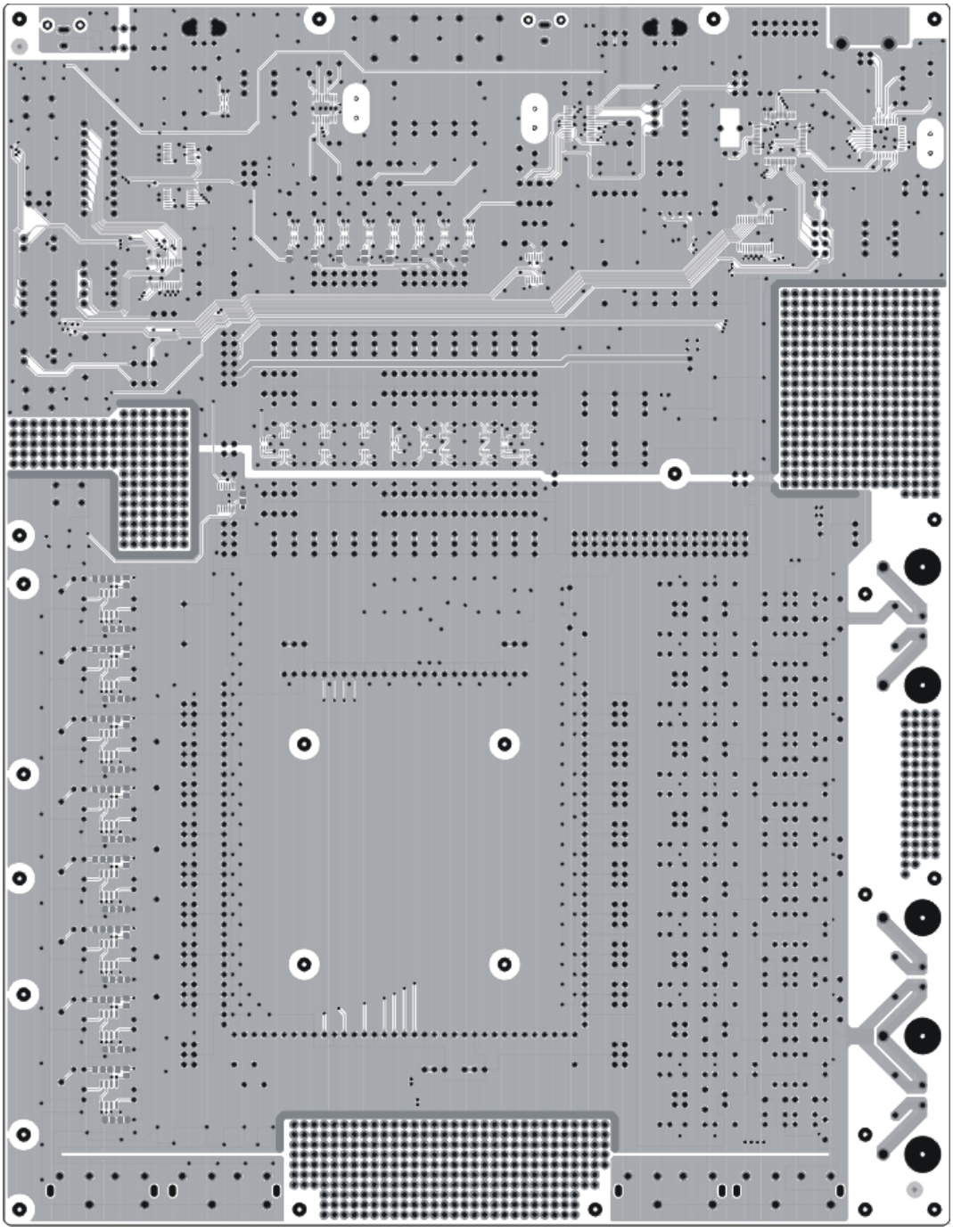


Figure 4-11. Layout Plane (Top)

4.2.4 DEM-DAI/MCODEC Layout Plane (Layer 2)

Figure 4-12 shows the layout plane, layer 2 image.

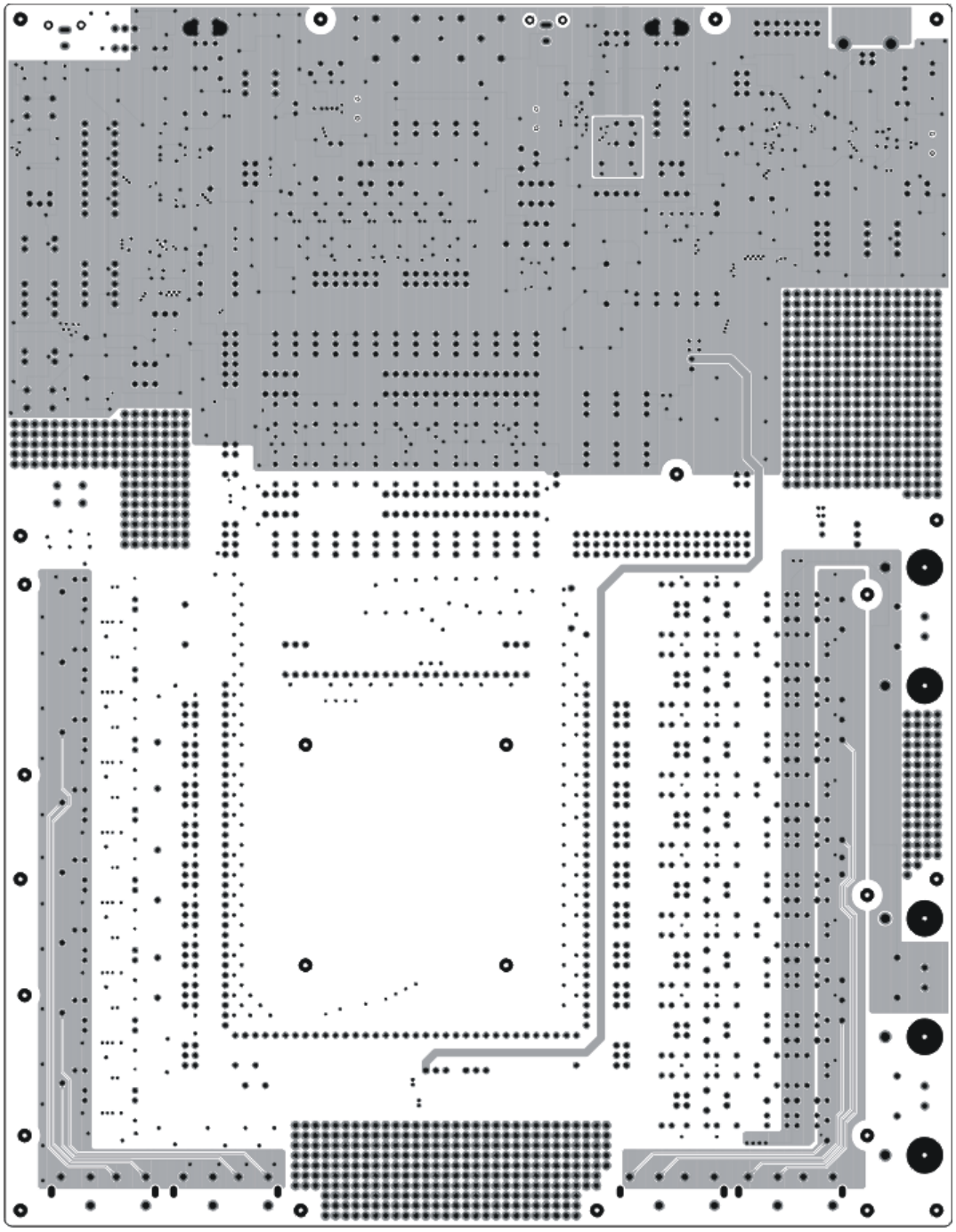


Figure 4-12. Layout Plane (Layer 2)

4.2.5 DEM-DAI/MCODEC Layout Plane (Layer 3)

Figure 4-13 shows the layout plane, layer 3 image.

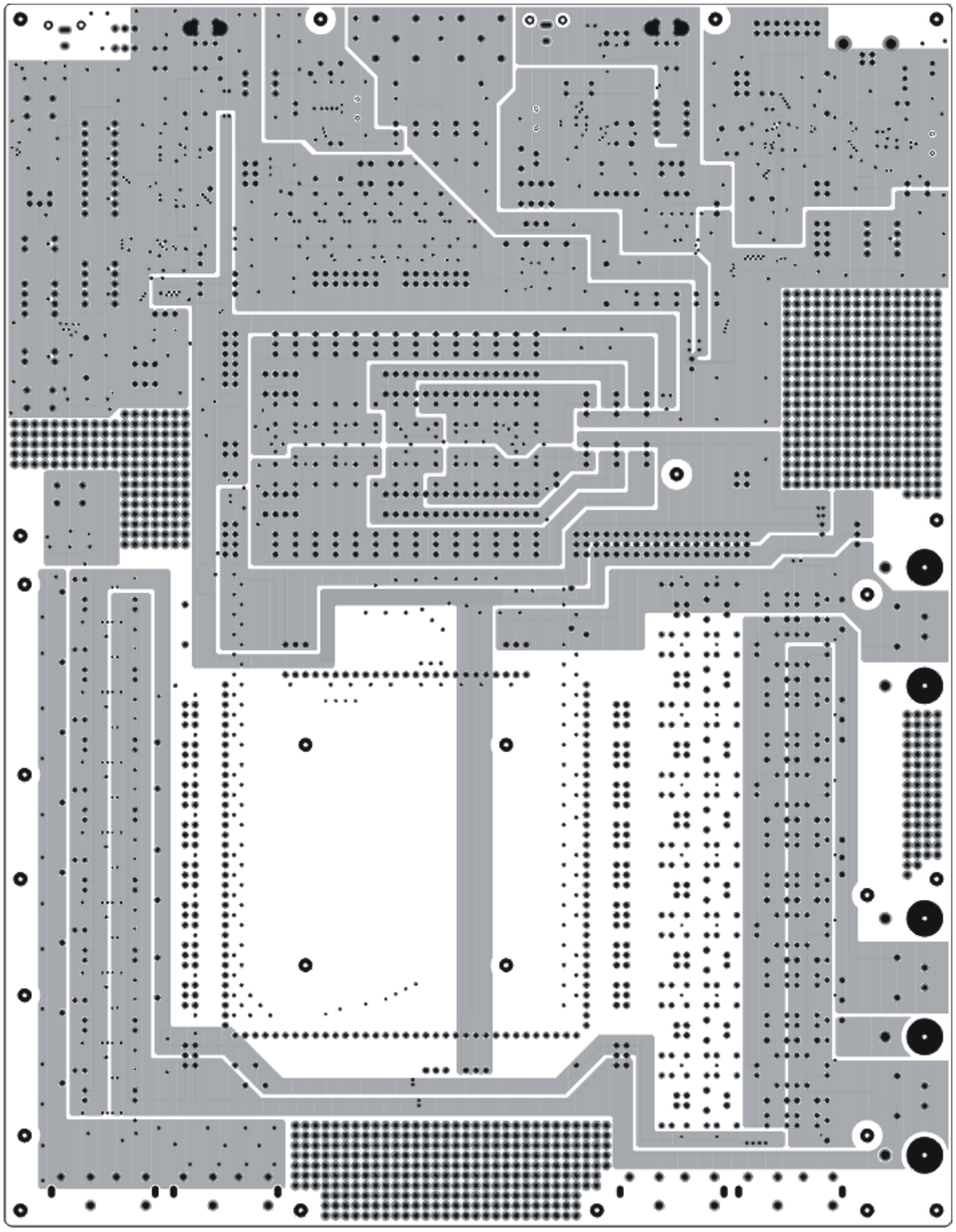


Figure 4-13. Layout Plane (Layer 3)

4.2.6 DEM-DAI/MCODEC Layout Plane (Bottom)

Figure 4-14 shows the layout plane, bottom layer image.

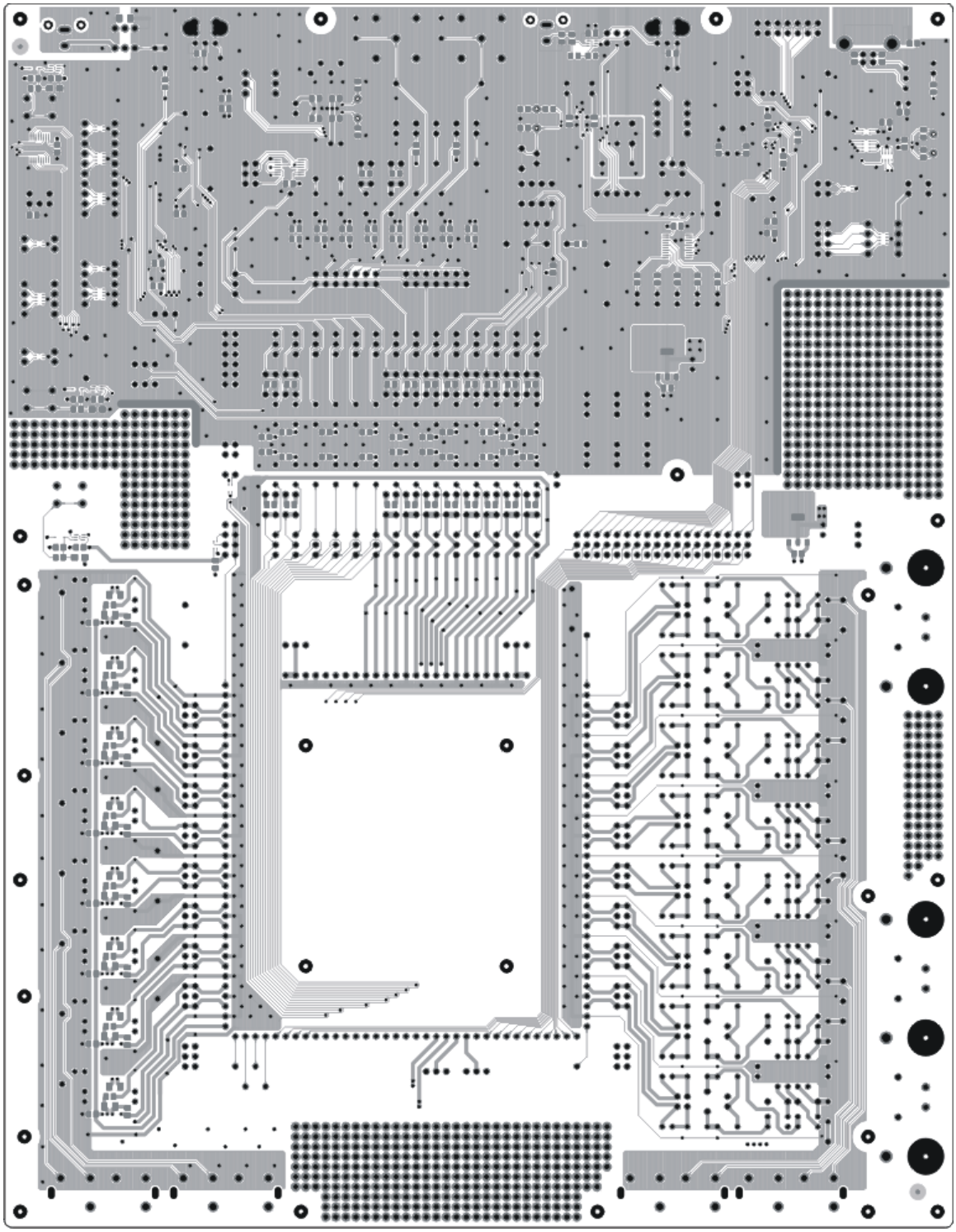


Figure 4-14. Layout Plane (Bottom)

4.2.7 DEM-PCM3168A (DUT Daughterboard) Silk Plane (Top)

Figure 4-15 shows the silkscreen plane, top layer image for the DUT daughterboard.

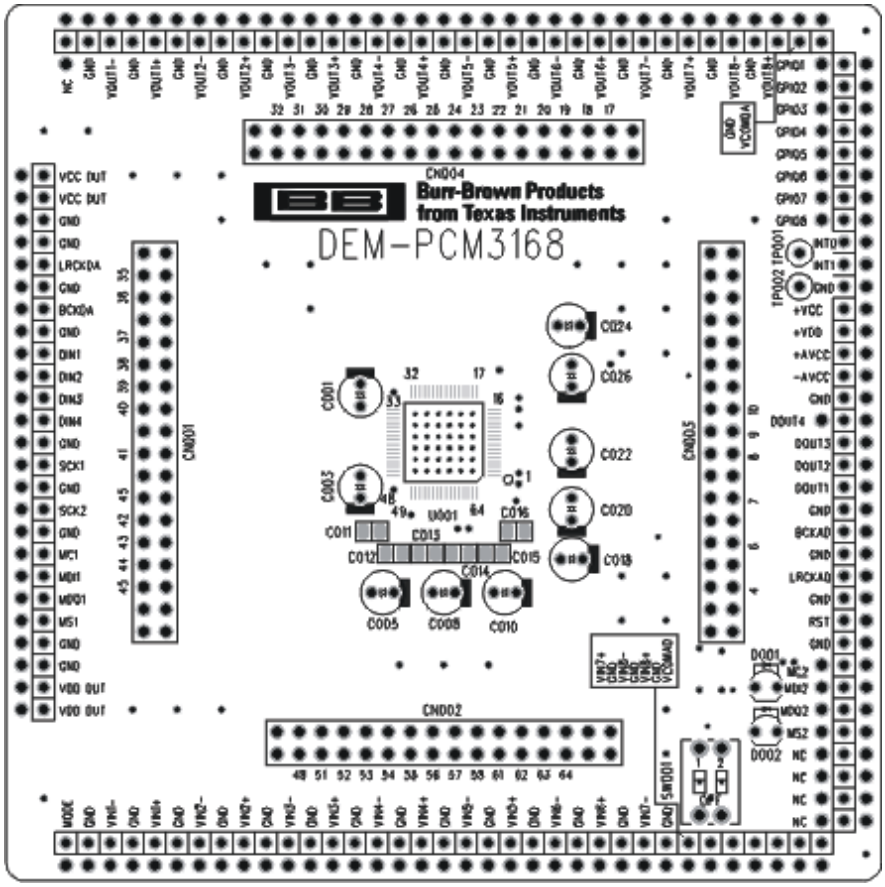


Figure 4-15. Silk Plane (Top)

4.2.8 DEM-PCM3168A (DUT Daughterboard) Silk Plane (Bottom)

Figure 4-16 shows the silkscreen plane, bottom layer image for the DUT daughterboard.

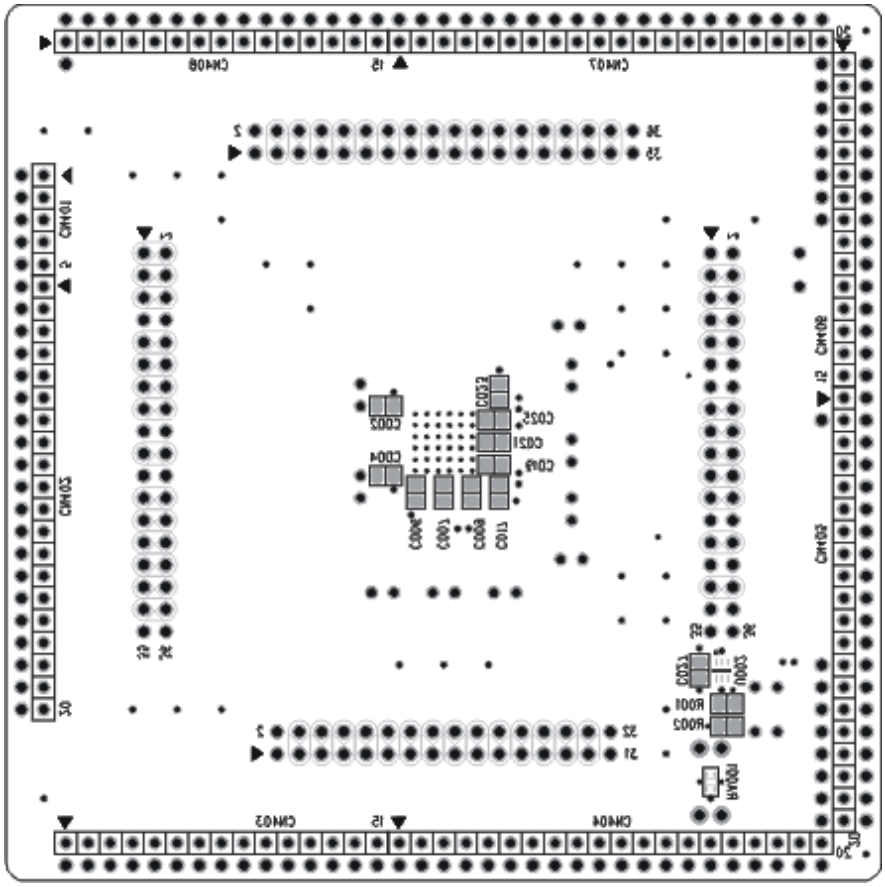


Figure 4-16. Silk Plane (Bottom)

4.2.9 DEM-PCM3168A (DUT Daughterboard) Layout Plane (Top)

Figure 4-17 shows the layout plane, top layer image for the DUT daughterboard.

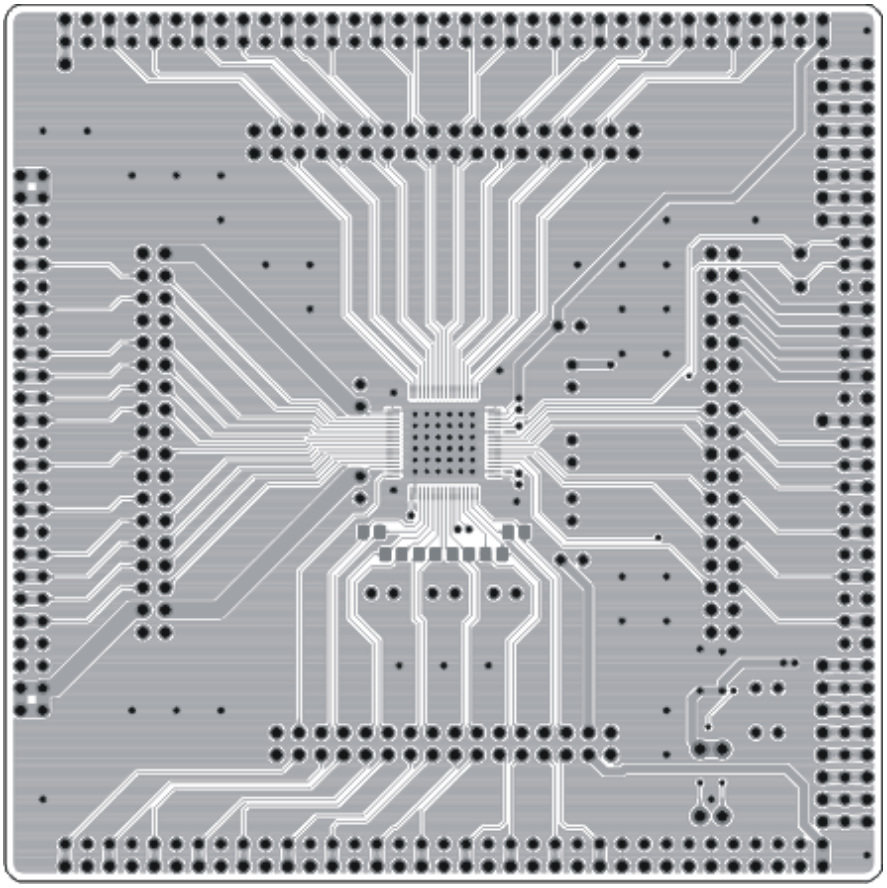


Figure 4-17. Layout Plane (Top)

4.2.10 DEM-PCM3168A (DUT Daughterboard) Layout Plane (Layer 2)

Figure 4-18 shows the layout plane, layer 2 image for the DUT daughterboard.

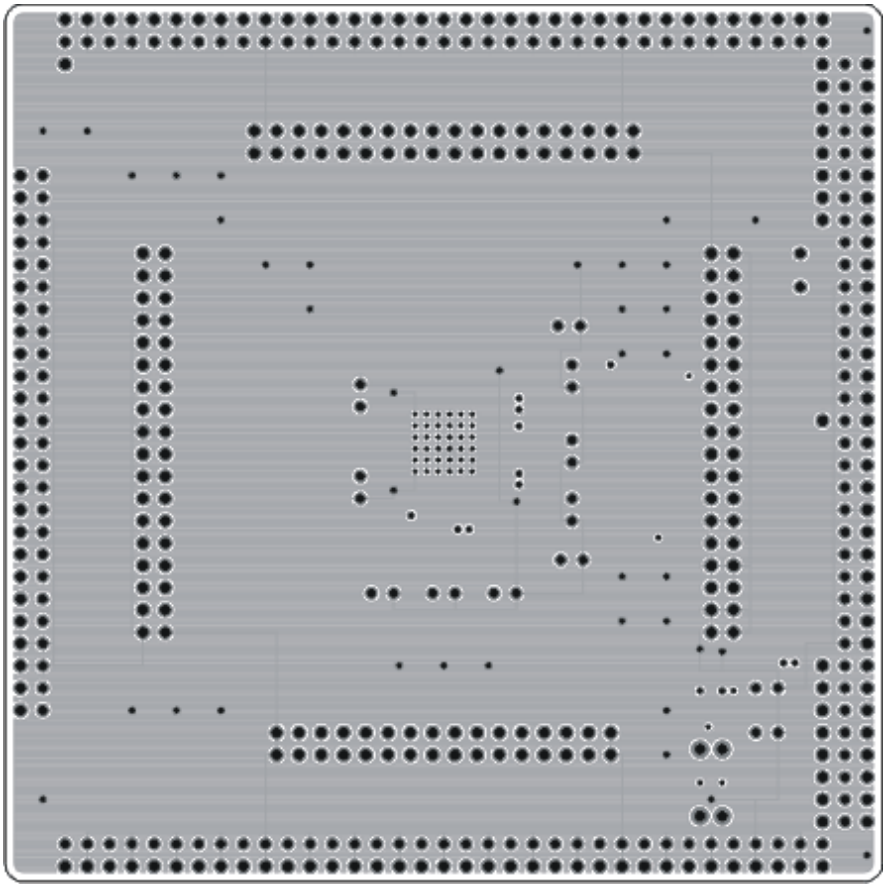


Figure 4-18. Layout Plane (Layer 2)

4.2.11 DEM-PCM3168A (DUT Daughterboard) Layout Plane (Layer 3)

Figure 4-19 shows the layout plane, layer 3 image for the DUT daughterboard.

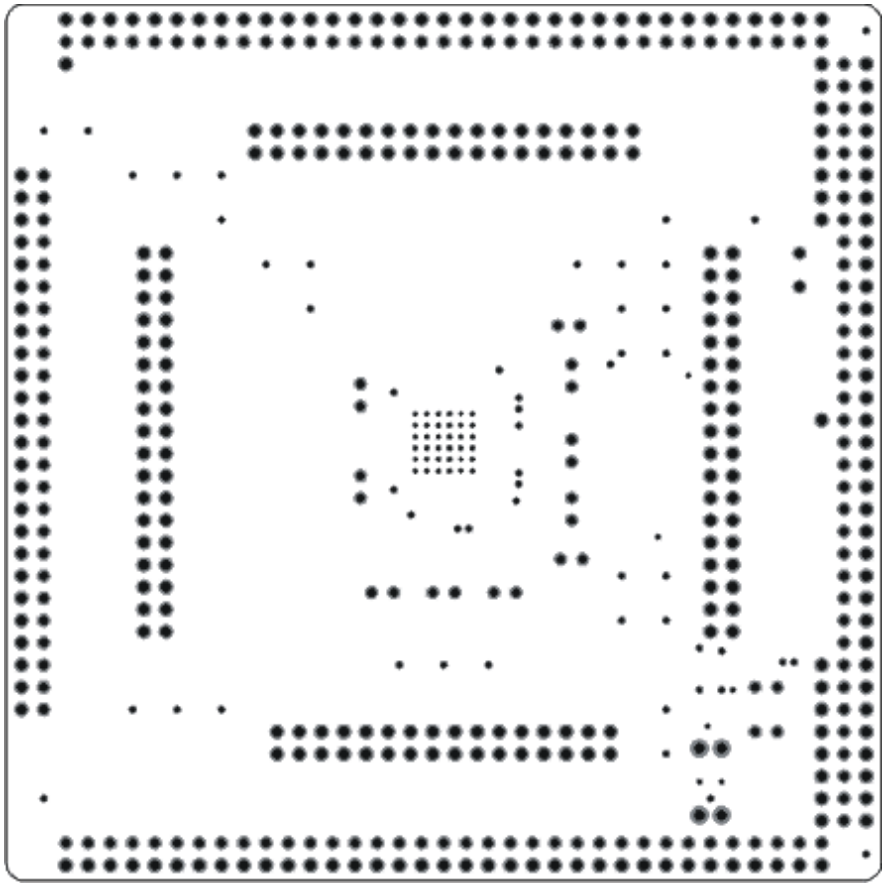


Figure 4-19. Layout Plane (Layer 3)

4.2.12 DEM-PCM3168A (DUT Daughterboard) Layout Plane (Bottom)

Figure 4-20 shows the layout plane, bottom layer image for the DUT daughterboard.

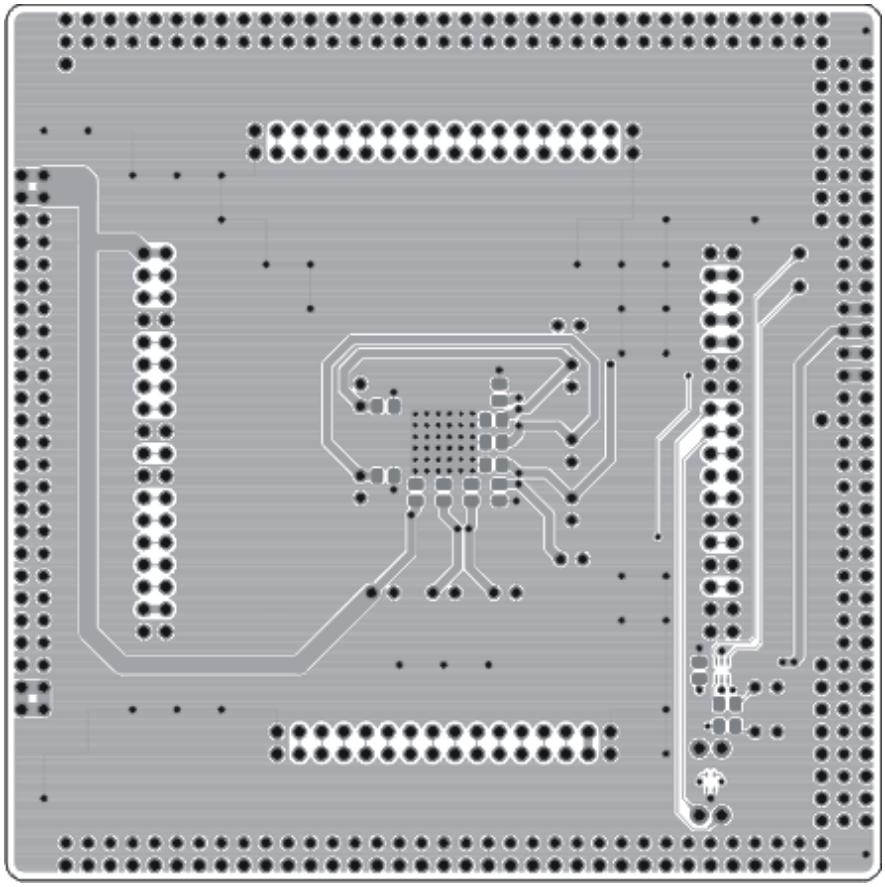


Figure 4-20. Layout Plane (Bottom)

4.3 Bills of Material (BOMs)

Table 4-1 lists the BOM information for the DEM-DAI/MCODEC_USB board. Table 4-2 includes the BOM information for the DEM-PCM3168A board.

Table 4-1. Bill of Materials: DEM-DAI/MCODEC_USB

Qty	Reference Designators	Part Name, Type	Specification	Manufacturer Part No	Manufacturer
2	C305, C306	Chip Ceramic Capacitor	15 pF, J		Murata
2	C207, C208	Chip Ceramic Capacitor	18 pF, J		Murata
4	C105, C106, C112, C113	Chip Ceramic Capacitor	22 pF, J		Murata
79	C004, C006, C101, C103, C104, C107, C109, C110, C114, C201, C203, C204, C206, C209, C213-C215, C302, C304, C307-C325, C327, C328, C330-C335, C337, C339, C401-C413, C415-C424, C604, C610, C616, C622, C628, C634, C640, C646	Chip Ceramic Capacitor	0.1 µF	GRM188B11E104KA01	Murata
16	C506, C507, C515, C516, C522, C523, C531, C532, C538, C539, C547, C548, C554, C555, C563, C564	Polypropylene Capacitor	680 pF, J	APSF0100J681	NISSEI
24	C503, C512, C519, C528, C535, C544, C551, C560, C602, C603, C608, C609, C614, C615, C620, C621, C626, C627, C632, C633, C638, C639, C644, C645	Polypropylene Capacitor	1500 pF, J	APSF0100J152	NISSEI
1	C211	Polypropylene Capacitor	0.0047 µF, J	APSF0100J472	NISSEI
1	C212	Polypropylene Capacitor	0.068 µF, J	APSF0100J683	NISSEI
3	C108, C338, C414	Chip Tantalum Capacitor	10 µF/16 V	ESVA1C106M	NEC TOKIN
12	C005, C007, C102, C111, C202, C205, C210, C301, C303, C326, C329, C336	OS Capacitor	10 µF/16 V	16SS10M	SANYO
48	C501, C502, C508-C511, C517, C518, C524-C527, C533, C534, C540-C543, C549, C550, C556-C559, C601, C605-C607, C611-C613, C617- C619, C623-C625, C629-C631, C635-C637, C641-C643, C647, C648	Electrolytic Capacitor	10 µF/16 V	R0A-16V100M	ELNA
3	C001, C002, C003	Electrolytic Capacitor	100 µF/16 V	R0A-16V101M	ELNA
8	R304, R306, R307, R309, R311, R316, R321, R323	Chip Resistor	33 Ω, D	RP0816	Susumu
16	R603, R606, R610, R613, R617, R620, R624, R627, R631, R634, R638, R641, R645, R648, R652, R655	Chip Resistor	47 Ω, D	RP0816	Susumu
1	R201	Chip Resistor	75 Ω, D	RR0816	Susumu
1	R204	Chip Resistor	330 Ω, D	RR0816	Susumu
4	R103, R212, R328, R449	Chip Resistor	470 Ω, D	RP0816	Susumu

Table 4-1. Bill of Materials: DEM-DAI/MCODEC_USB (continued)

Qty	Reference Designators	Part Name, Type	Specification	Manufacturer Part No	Manufacturer
1	R213	Chip Resistor	680 Ω, D	RR0816	Susumu
27	R101, R214, R215, R602, R604, R605, R609, R611, R612, R616, R618, R619, R623, R625, R626, R630, R632, R633, R637, R639, R640, R644, R646, R647, R651, R653, R654	Chip Resistor	1.5 kΩ, D	RP0816	Susumu
3	R102, R203, R211	Chip Resistor	2.2 kΩ, D	RP0816	Susumu
8	R601, R608, R615, R622, R629, R636, R643, R650	Chip Resistor	3 kΩ, D	RP0816	Susumu
1	R105	Chip Resistor	10 kΩ, D	RP0816	Susumu
1	R107	Chip Resistor	39 kΩ, D	RP0816	Susumu
7	R104, R202, R315, R320, R329, R450, R218	Chip Resistor	47 kΩ, D	RP0816	Susumu
1	R106	Chip Resistor	100 kΩ, D	RP0816	Susumu
41	R207, R208-R210, R303, R305, R308, R310, R314, R319, R322, R326, R327, R403, R406, R407, R410, R415, R418, R419, R422, R427, R430, R431, R434, R439, R440, R445, R446, R451-R458, R461, R464, R465, R468	Resistor	33 Ω, F, 1/4W		KOA
8	R507, R514, R521, R528, R535, R542, R549, R556	Resistor	47 Ω, F, 1/4W		KOA
	R301, R302	Resistor	51 Ω, F, 1/4W		KOA
1	R325	Resistor	90.9 Ω, F, 1/4W		KOA
1	R324	Resistor	374 Ω, F, 1/4W		KOA
1	R206	Resistor	680 Ω, F, 1/4W		KOA
16	R504, R505, R511, R512, R518, R519, R525, R526, R532, R533, R539, R540, R546, R547, R553, R554	Resistor	1.5 kΩ, F, 1/4W		KOA
16	R503, R506, R510, R513, R517, R520, R524, R527, R531, R534, R538, R541, R545, R548, R552, R555	Resistor	5.6 kΩ, F, 1/4W		KOA
16	R501, R502, R508, R509, R515, R516, R522, R523, R529, R530, R536, R537, R543, R544, R550, R551	Resistor	7.5 kΩ, F, 1/4W		KOA
1	RA101	Resistor Networks	33 Ω x 2	CN1J2	KOA
1	RA105	Resistor Networks	1 kΩ x 2	CN1J2	KOA
2	RA102, RA402	Resistor Networks	10 kΩ x 2	CN1J2	KOA
4	RA107, RA301, RA303, RA306	Resistor Networks	47 kΩ x 2	CN1J2	KOA
1	RA401	Resistor Networks	220 kΩ x 2	CN1J2	KOA
2	RA103, RA104	Resistor Networks	10 kΩ x 4	CN1J4	KOA
5	RA106, RA201, RA302, RA304, RA305	Resistor Networks	47 kΩ x 4	CN1J4	KOA
1	L101	Chip Ferrite Bead		MPZ2012S331A	TDK
1	TR301	Pulse Transformer		DA-02	JPC
3	D102, D301, D401	Chip Diode		HSU119-E	Renesas

Table 4-1. Bill of Materials: DEM-DAI/MCODEC_USB (continued)

Qty	Reference Designators	Part Name, Type	Specification	Manufacturer Part No	Manufacturer
3	D001, D002, D003	Diode		D2S6M	Shindengen
1	D202	LED	Green	TLGU53D	Toshiba
2	D204, D205	LED	Orange	TLOU124	Toshiba
2	D101, D201	LED	Red	TLSU124	Toshiba
1	D203	LED	Yellow	TLYU124	Toshiba
1	Q101	Digital Transistor		DTC143ESA	ROHM
12	U501-U504, U601-U608	Op Amp		OPA2134PA	TI
1	U204	Logic IC		SN74HC541	TI
1	U206	Logic IC		SN74LV08A	TI
2	U205, U312	Logic IC	Package: PW	SN74LV157A	TI
1	U310	Logic IC	Package: PW	SN74LV74A	TI
13	U302-U309, U314, U402, U405, U406, U411	Logic IC	Package: DCK	SN74LVC1T45	TI
3	U102, U316, U407	Logic IC	Package: DCK	SN74LVC2G14	TI
1	U202	Logic IC	Package: DCK	SN74LVC2GU04	TI
6	U401, U403, U404, U408-U410	Logic IC	Package: DCT	SN74LVC2T45	TI
1	U313	Logic IC		TC74VHC153FT	TOSHIBA
1	U203	IC	DIR	DIR9001	TI
1	U311	IC	DIT	DIT4096	TI
1	U301	IC	PLL	PLL1707	TI
1	U103	IC	MCU	MSP430F169IPM	TI
1	U101	IC	USB	TUSB3410VF	TI
1	U104	IC	MUX	MAX7301	MAXIM
2	U001, U002	Regulator IC	800 mA, 3.3 V	REG1117-3.3	TI
1	U201	TOSLINK	Receiver	TORX141	TOSHIBA
1	U315	TOSLINK	Transmitter	TOTX141	TOSHIBA
1	X101	Crystal Resonator	12.000 MHz	CX5032GB	Kinseki
1	X201	Crystal Resonator	24.576 MHz	CX5032GB	Kinseki
1	X301	Crystal Resonator	27.000 MHz	CX5032GB	Kinseki
1	X102	Crystal Resonator	32.768 kHz	FC-135, 12.5pF	EPSON
41	HDR001, HDR102, HDR103, HDR201, HDR202, HDR301, HDR303, HDR405-HDR424, HDR426-HDR439	TH-type Male Connector	3-pin	FFC-3AMEP1	HTK
5	JP202, JP301, JP304, JP305, JP401	TH-type Male Connector	2-pin	FFC-2BMEP1	HTK
9	JP101, JP502, JP505, JP508, JP511, JP514, JP517, JP520, JP523	TH-type Male Connector	4-pin	FFC-4BMEP1	HTK
2	HDR302, JP201	TH-type Male Connector	6-pin	FFC-6BMEP1	HTK
2	HDR425, JP102	TH-type Male Connector	8-pin	FFC-8BMEP1	HTK
2	JP302, JP303	TH-type Male Connector	14-pin	FFC-14BMEP1	HTK
1	CN203	TH-type Male Connector	5-pin	FFC-5AMEP1	HTK

Table 4-1. Bill of Materials: DEM-DAI/MCODEC_USB (continued)

Qty	Reference Designators	Part Name, Type	Specification	Manufacturer Part No	Manufacturer
3	CN202, CN303, CN304	TH-type Male Connector	2-pin	FFC-2BMEP1	HTK
1	CN102	TH-type Male Connector	14-pin	FFC-14BMEP1	HTK
1	CN401	Connector	5-pin	XB-3-7-5P	Mac8
3	CN403, CN406, CN408	Connector	15-pin	XB-3-7-15P	Mac8
4	CN402, CN404, CN405, CN407	Connector	20-pin	XB-3-7-20P	Mac8
5	CN001-CN005	Banana Jack	Yellow, Green, Blue, Red, Black	T-45	Sato Parts
2	CN201, CN305	RCA Pin Jack	RCA (Yellow)	LPR6520-0804	SMK
2	CN301, CN302	BNC Connector	BNC	BNC-LR-PC4	Daiichi Denshi
1	CN101	USB Connector type B	USB_TYPE-B	67068-8001	Molex
4	PJ501, PJ502, PJ601, PJ602	Pin Jack		YKC21-3034V	JARCO
2	SW103, SW304	DIP Switch		DSS102	Fujisoku
1	SW301	DIP Switch		DSS103	Fujisoku
3	SW101, SW201, SW205	DIP Switch		DSS104	Fujisoku
1	SW302	DIP Switch		DSS105	Fujisoku
1	SW303	DIP Switch		DSS110	Fujisoku
3	SW202, SW203, SW204	Toggle Switch		FT1D-2M	Fujisoku
3	SW305, SW401, SW102	Tact Switch			Alps
16	TP501–TP508, TP601–TP608	Test Pin		LC-2-G	Mac8
18	TP101, TP102, TP301–TP310, TP401–TP406	Test Pin		LC-3-G	Mac8
21	TP201–TP205, TP311–TP326	Test Pin		LC-4-G	Mac8

Table 4-2. Bill of Materials: DEM-PCM3168A

Qty	Reference Designators	Part Name, Type	Specification	Manufacturer Part No	Manufacturer
6	C011–C016	Chip Film Capacitor	0.01 μF, J, 2012	ECHU1C103J	Panasonic
11	C002, C004, C006, C007, C009, C017, C019, C021, C023, C025, C027	Chip Ceramic Capacitor	0.1 μF	GRM188B11E104KA01	Murata
10	C001, C003, C005, C008, C010, C018, C020, C022, C024, C026	Electrolytic Capacitor	10 μF/16 V	R0A-16V100M	ELNA
1	R001	Chip Resistor	470 Ω, D	RP0816	Susumu
1	R002	Chip Resistor	2.2 kΩ, D	RP0816	Susumu
1	RA001	Resistor Networks	47 kΩ x 2	CN1J2	KOA
1	D001	LED	Green	TLGU53D	Toshiba
1	D002	LED	Red	TLSU124	Toshiba
1	U002	IC	Package: DCK	SN74LVC2G34	TI
1	U001	IC	CODEC, DUT	PCM3168A	TI
1	SW001	DIP Switch		DSS102	Fujisoku
2	TP001, TP002	Test Pin		LC-3-G	Mac8

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During normal operation, some circuit components may have case temperatures greater than +55°C. The EVM is designed to operate properly with certain components above +55°C as long as the input and output ranges are maintained. These components include but are not limited to linear regulators, switching transistors, pass transistors, and current sense resistors. These types of devices can be identified using the EVM schematic located in the EVM User's Guide. When placing measurement probes near these devices during operation, please be aware that these devices may be very warm to the touch.

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