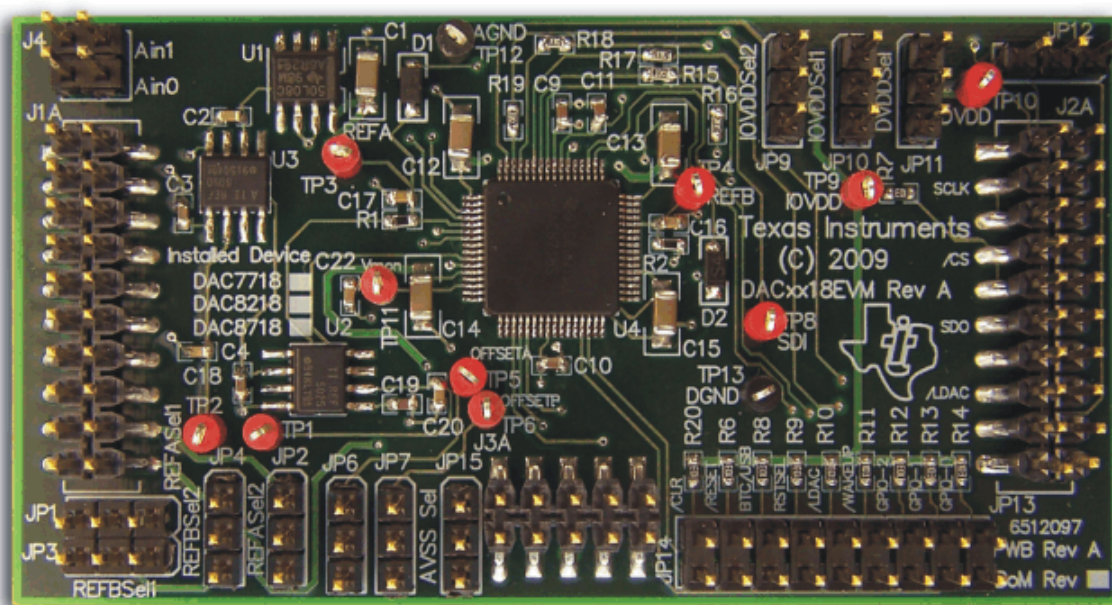# DAC7718EVM

DAC7718EVM

This user's guide describes the characteristics, operation, and use of the DAC7718EVM, an evaluation board for the DAC7718. The DAC7718 is a low-power, octal, 12-bit digital-to-analog converter (DAC). This device features low-power operation, good linearity, and low glitch. This evaluation module (EVM) allows evaluation of all aspects of the DAC7718 and gives control over every pin on the device. Complete circuit descriptions, schematic diagrams, and bills of material are included in this document.

The following related documents are available through the Texas Instruments web site at www.ti.com.

Related Documentation

Device	Literature Number
DAC7718	SBAS361
REF5025	SBOS410C
REF5050	SBOS410C
TL750L08	SLVS017T

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All other trademarks are the property of their respective owners.

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1   EVM Overview

1.1   *Features*

DAC7718EVM:

- Full-featured evaluation board for the DAC7718, a 12-bit, serial input, octal output digital-to-analog converter
- Onboard or external reference selection
- Configurable for single- or dual-supply operation
- Wide selection of digital and I/O voltages
- Hardware or software control of control logic

1.2   *Introduction*

The DAC7718 is a 12-bit, low-power, octal DAC that operates from independent AV_{DD}, AV_{SS}, and DV_{DD} supplies. It uses a high-speed serial peripheral interface, or SPI™ (up to 50MHz), to communicate with a DSP or a microprocessor using a compatible serial interface.

The DAC control logic can be controlled using onboard jumpers, or digitally through the J2 header.

The DAC7718EVM is designed for unipolar and bipolar (default) modes of operation. This flexibility allows for a wide range of supply voltages. Unipolar operation requires only a single analog voltage supply and bipolar operation requires two analog supplies.

The DAC7718EVM is an evaluation module built to the TI Modular EVM System specification. It can be connected to any modular EVM system interface card. The EVM ships in the TQFP-64 pin package.

Note that the DAC7718EVM has no microprocessor and cannot run software. To connect it to a computer, some type of interface is required.

2   Analog Interface

For maximum flexibility, the DAC7718EVM can interface to multiple analog sources. Samtec part numbers SSW-110-22-F-D-VS-K and TSM-110-01-T-DV-P provides a 10-pin, dual-row, header at J1. This header provides access to the analog input and output pins of the DAC. An additional connector, J4, and test points are added to the evaluation module to allow access to all of the analog pins on the DAC. Consult Samtec at http://www.samtec.com or call 1-800-SAMTEC-9 for a variety of mating connector options.

Table 1 summarizes the pinouts for analog interface J1.

Table 1. J1: Analog Interface Pinout

Pin Number	Signal	Description
J1.2	V_{OUT}-0	Analog output 0
J1.4	V_{OUT}-1	Analog output 1
J1.6	V_{OUT}-2	Analog output 2
J1.8	V_{OUT}-3	Analog output 3
J1.10	V_{OUT}-4	Analog output 4
J1.12	V_{OUT}-5	Analog output 5
J1.14	V_{OUT}-6	Analog output 6
J1.16	V_{OUT}-7	Analog output 7
J1.18	EXT-REFA	External reference source input for REF-A (V_{OUT}-0 to V_{OUT}-3)
J1.20	EXT-REFB	External reference source input for REF-B (V_{OUT}-4 to V_{OUT}-7)
J1.1-1.19 (odd)	GND	Analog ground connection

Table 2 summarizes the pinouts for analog interface J4.

Table 2. J4: Analog AIN Interface Pinout

Pin Number	Signal	Description
J4.2	AIN-0	Analog input 0
J4.4	AIN-1	Analog input 1
J4.1 and J1.3	GND	Analog ground connection

The analog interface is populated on the top and the bottom of the evaluation model. All of the output pins and the AIN-x pins are routed directly from the to the connector.

The GND pins of the DAC7718 are connected directly to the ground of the EVM board.

The DAC7718 has two auxiliary analog input pins, A_{IN}-0 and A_{IN}-1. These signals can be relayed to the V_{MON} output pin. Care must be taken to avoid overvoltage on these input pins. Make sure that the analog inputs do not exceed the Absolute Maximum Ratings found in the DAC7718 data sheet. The two A_{IN} pins can be accessed from the J4 header; see Table 2.

The DAC7718EVM has two external reference voltage options. J1.18 controls the external reference voltage for the REF-A input. J1.20 controls the reference for the REF-B input. When an external reference is used, jumpers JP1-JP4 must be configured properly. Test points TP3 and TP4 can be used to verify that the jumpers are configured properly and the correct reference voltage is applied to the DAC.

The output of the DAC7718 internal offset DAC is routed to test points TP5 and TP6. Jumpers JP6 and JP7 must be properly configured to route the OFFSET-A (TP5) and OFFSET-B (TP6) signals to the test points.

The V_{MON} output allows the user to relay any of the DAC outputs, as well as A_{IN}-0 or A_{IN}-1, to a single pin. V_{MON} is routed to test point TP11 and is connected to a 0.1µF capacitor.

3   Digital Interface

The DAC7718EVM is a serial input data converter. The evaluation module is designed for interfacing to multiple control platforms.

3.1   *Serial Data Interface*

Samtec part numbers SSW-110-22-F-D-VS-K and TSM-110-01-T-DV-P provide a 10-pin, dual-row, header/socket combination at J2. This header/socket provides access to the digital control and serial data pins from both J2A (top side) and J2B (bottom side) of the connector. The additional GPIO pins are connected to the JP13 header. Consult Samtec at http://www.samtec.com or call 1-800-SAMTEC-9 for a variety of mating connector options.

Table 3 describes the serial interface pins.

Table 3. J2: Serial Interface Pins

Pin No.	Signal Name	I/O Type	Pull-Up	Function
J2.1, J2.7, J2.9	$\overline{\text{CS}}$	In	None	SPI bus chip select; pins are shorted together
J2.2	$\overline{\text{CLR}}$	In	High	Level trigger clear pin
J2.3, J2.5	SCLK	In	None	DAC7718 SPI clock; pins are shorted together
J2.4	DGND	In/Out	None	Digital ground
J2.6	$\overline{\text{RESET}}$	In	High	Input register reset
J2.8	BTC/USB	In	High	Data format for DAC input
J2.10	DGND	In/Out	None	Digital ground
J2.11	SDO/SDI	In/Out	None	DAC7718 SPI data in/out
J2.12	$\overline{\text{WAKEUP}}$	In	High	Wake up device from sleep mode
J2.13	Unused	—	—	—
J2.14	GPIO0	In/Out	High	DAC7718 GPIO0 signal
J2.15	$\overline{\text{LDAC1}}$	In	High	GPIO signal to control LDAC for DAC output latch update
J2.16	Unused	—	—	—
J2.17	$\overline{\text{LDAC2}}$	In	High	Alternate GPIO signal to control LDAC for DAC output latch update
J2.18	DGND	In/Out	None	Digital ground
J2.19	GPIO1	In/Out	High	DAC7718 GPIO1 signal
J2.20	Unused	—	—	—

The SCLK signal and the $\overline{\text{CS}}$ signal can each be controlled by multiple pins on J2. Pins J2.3 and J2.5 have been shorted together to control SCLK. J2.1, 2.7 and J2.9 have been shorted together to control $\overline{\text{CS}}$.

Pins J2.2, J2.6, J2.8, J2.12, J2.14, J2.15, J2.17, and J2.19 have weak pull-up/-down resistors. These resistors provide default settings for many of the control pins. These signals can be controlled through the digital interface or jumpers found directly on the EVM. By default, these signals are pulled high through 10kΩ resistors. J2.1, J2.3, J2.5, J2.7, J2.9, J2.11 are the control line signals for the DAC7718. They are connected directly to the DAC through 33Ω resistors. The J2 header is the only way to access these pins. See the [DAC7718 product data sheet](#) for complete details on these pins.

The load DAC ($\overline{\text{LDAC}}$) pin is connected via jumper JP12 to either the J2.15 pin or the J2.17 pin. Updating the DAC registers can be completed in two different ways. First, the $\overline{\text{LDAC}}$ pin can be held low; in this approach, the input registers are immediately updated. Alternatively, the $\overline{\text{LDAC}}$ pin can be held high, and the DAC registers update when $\overline{\text{LDAC}}$ is taken low. By default, $\overline{\text{LDAC}}$ is pulled high through a 10kΩ resistor. A shunt can be placed across jumpers JP14.9 and JP14.10 to connect $\overline{\text{LDAC}}$ to the ground. See the [DAC7718 data sheet](#) for more information on updating the DAC.

GPIO signals GPIO0 and GPIO1 can be accessed at JP14 or the J2 header. GPIO2 can only be accessed at JP14. By default, these signals are each pulled high through a 10kΩ resistor. However, they can be tied to ground by vertically applying a shunt across the individual pins on JP14.

4   Power Supplies

Samtec part numbers SSW-105-22-F-D-VS-K and TSM-105-01-T-DV-P provide a 5-pin, dual-row, header/socket combination at J3. Table 4 lists the configuration details for J3. The voltage inputs to the DAC can be applied directly to the device. The DAC7718 requires multiple power supplies to operate. AV_{DD}, AV_{SS}, DV_{DD}, and IOV_{DD} are required to properly power the DAC. The power should be applied in the order: IOV_{DD}, DV_{DD}, then AV_{DD} and AV_{SS}, followed by reference voltage.

CAUTION
This sequence must be followed in order to prevent damage to the device.

Table 4. J3 Configuration: Power-Supply Input

Pin No.	Pin Name	Function	Required
J3.1	+VA	+4.75V to +24V analog supply	Yes
J3.2	–VA	-18V to -4.75V analog supply	Yes
J3.3	+5VA	+5V analog supply	No
J3.4	–5VA	–5V analog supply	No
J3.5	DGND	Digital ground input	Yes
J3.6	AGND	Analog ground input	Yes
J3.7	+1.8VD	1.8V digital supply	Optional
J3.8	VD1	Not used	No
J3.9	+3.3VD	3.3V digital supply	Optional
J3.10	+5VD	+5V	Optional

NOTE: To avoid damage to the , DV_{DD} must stay greater than or equal to IOV_{DD}.

The digital and analog ground inputs are short-circuited internally through a ground plane.

The digital supply voltage (DV_{DD}) for the DAC7718 is selectable between +5VD and +3.3VD via the JP11 jumper. Test point TP10 can be used to verify the digital supply voltage selected. Care must be taken to ensure that the EVM is not configured to be in a state where V_{REF} is greater than DV_{DD}. Diodes are put into place (D1 and D2) to add protection to the part.

The dc logic voltage for the DAC7718 (IOV_{DD}) is selectable between +5VD, +3.3 VD, or +1.8 VD using jumpers JP9 and JP10. These power-supply voltages are referenced to digital ground. Test point TP9 can be used to verify the selected IOV_{DD} voltage.

The DAC7718EVM is designed to work in either unipolar or bipolar mode. Each mode requires a different power-supply connection. In bipolar mode, AV_{SS} and AV_{DD} are powered through –VA and +VA directly. When unipolar mode is desired, JP15 allows AV_{SS} to be connected to the EVM board ground. AV_{DD} continues to be powered through +VA. Consult the DAC7718 data sheet for the restrictions on the power supplies for the two operating modes.

5   Voltage Reference

The DAC7718EVM has the ability to use two different reference voltages simultaneously for different output channels. REF-A and REF-B control the reference voltages for the DAC. Output channels V_{OUT}-0, V_{OUT}-1, V_{OUT}-2, and V_{OUT}-3 use REF-A as a reference. REF-B is used as a reference for output channels V_{OUT}-4, V_{OUT}-5, V_{OUT}-6, and V_{OUT}-7.

The evaluation module contains two different onboard reference sources and the option of using an external reference voltage. Jumpers JP1 through JP4 select the reference voltage from the REF5050(U3), REF5025(U2), or use an external reference. The REF5050 supplies 5.0V to the reference. The REF5025 supplies 2.5V to the reference. The outputs from the REF5025 and REF5050 can be accessed by test point TP1 and TP2, respectively. These reference voltages are additionally filtered through an RC filter before connected to the DAC7718. The TL751L08 is used to voltage regulate +VA to properly power the REF5025 and REF5050.

Jumpers JP2 (REF-A) and JP4 (REF-B) select between using an onboard reference or an external reference. If an onboard reference is selected, jumpers JP1 (REF-A) and JP3 (REF-B) are used to select between the 2.5V or the 5.0V reference. Pins J1.18 (REF-A) and J1.20 (REF-B) on header J1 are used to input an external reference. The reference voltages applied to the DAC can be observed at test points TP3 (REF-A) and TP4 (REF-B).

Note that if an external reference voltage is input to J1.18 or J1.20, it will be filtered through a RC filter with an 8Hz cutoff frequency. If the user desires to input his own reference signal without this filter, he can do so by connecting the reference signal directly to TP3 or TP4.

Figure 1 illustrates the reference test points.
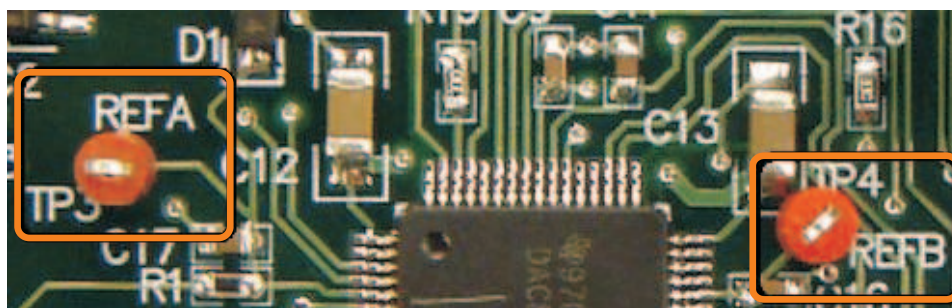
Figure 1. Reference Test Points

6 EVM Operation

This section provides information on the analog input, digital control, and general operating conditions of the DAC7718EVM.

6.1 Analog Output

The DAC7718 has eight analog outputs that are available through the J1 header. Each of these output are referenced to the board ground.

The OFFSET-A and OFFSET-B analog outputs are routed to TP5 and TP6. The OFFSET feature can only be used in bipolar mode. A shunt must be placed across pins 1 and 2 to view the output on the test points. The pins must be shorted directly to ground for unipolar/single-supply operation. For this mode, apply shunts across pins 2 and 3 of JP6 and JP7 to short the OFFSET-A/-B pins to ground.

V_{MON} is the channel monitor output. It can relay any of the eight analog output signals, the OFFSET-A/-B, the Ref Buffer A/B, or either of the two A_{IN} signals. The output pin has a 0.1µF capacitor connected. By default, the V_{MON} pin is in 3-state mode.

6.2 Digital Control

The digital control signals can be applied directly to J1 (top or bottom side). The DAC7718EVM can also be connected directly to a DSP or microcontroller interface board.

No specific evaluation software is provided with this EVM; however, various code examples are available that show how to use this EVM with a variety of digital signal processors from Texas Instruments. Please check the specific device product folders or send an e-mail to dataconvapps@list.ti.com for a listing of available code examples. The EVM Gerber files are also available on request.

6.3 Default Jumper Settings and Switch Positions

The DAC7718EVM has the ability to operate in either bipolar or unipolar mode. The proper jumper conditions depend on which mode the evaluation module operates in. Table 5 summarizes the jumpers found on the EVM.

Table 5. DAC7718EVM Jumpers

Jumper	Name	Description
JP1	REFASel1	Reference A: Select between 2.5V and 5.0V onboard reference voltage
JP2	REFASel2	Reference A: Select between using the onboard ref (from JP1) or an external reference
JP3	REFBSel1	Reference B: Select between 2.5V and 5.0V onboard reference voltage
JP4	REFBSel2	Reference B: Select between using the onboard reference (from JP3) or an external ref
JP6	OFFSETA	OFFSET DAC A
JP7	OFFSETB	OFFSET DAC B
JP9	IOVDDSel2	IOV_{DD}: Select between 1.8V or the result from IOVDDSel1 (JP10)
JP10	IOVDDSel1	Routes 5.0V or 3.3V to JP9
JP11	DVDDSel	DV_{DD}: Select between 5.0V and 3.3V
JP12	LDAC Selection	Routes $\overline{LDAC}$ pin to either J2.15 or J2.17
JP14	Digital	Digital control pins: Pulled high by default; apply shunt to tie pins to ground
JP15	AVSS Sel	Tie AVSS to J3.1

Figure 2 and Figure 3 show the default jumper conditions for bipolar and unipolar modes, respectively.
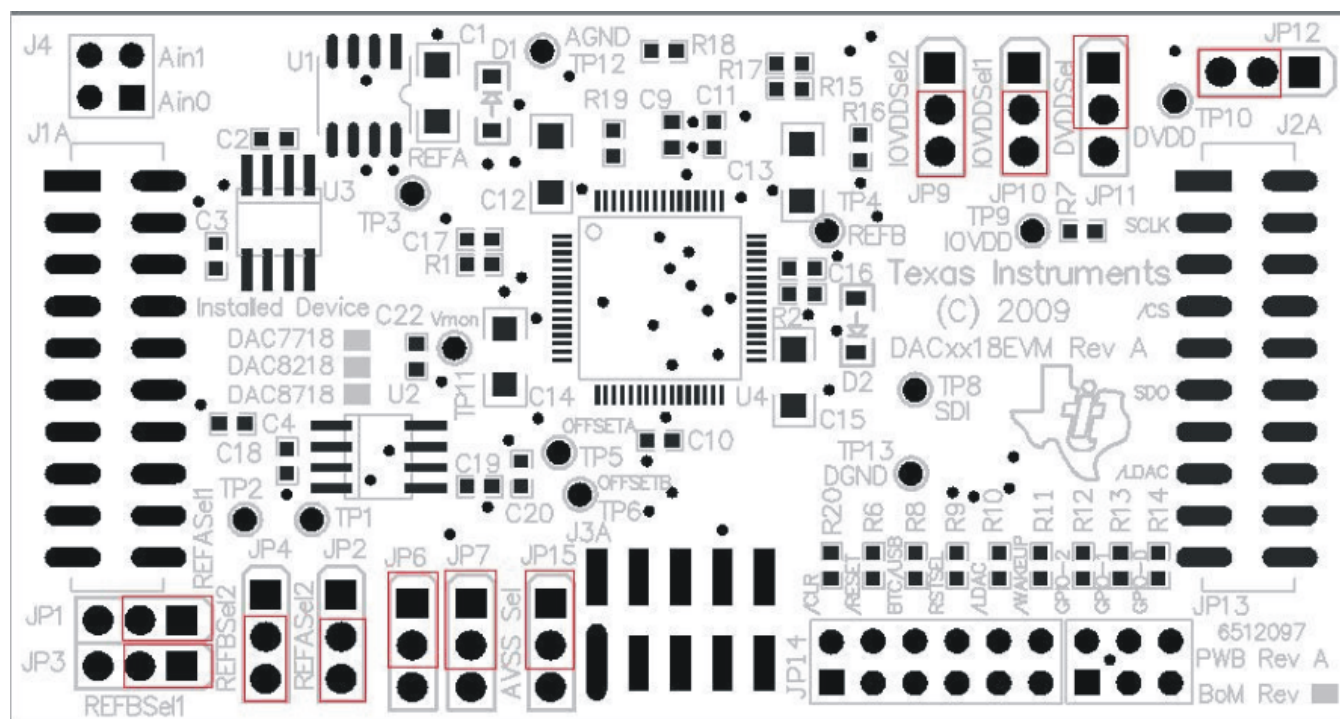

Figure 2. DAC7718EVM Default Jumper Locations for Bipolar Mode
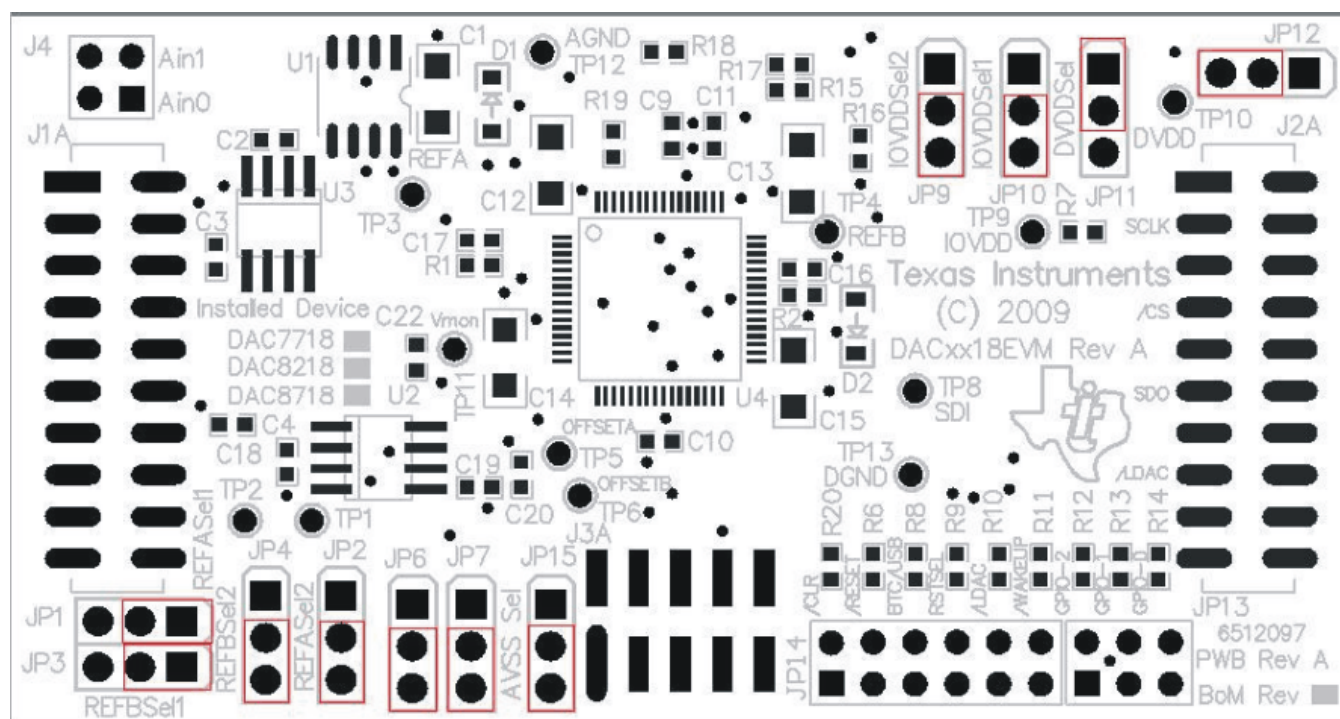

Figure 3. DAC7718EVM Default Jumper Locations for Unipolar Mode

Jumpers JP1 and JP2 are used to control the reference voltage for group A. JP1 is selectable by connecting a jumper across pins 1 and 2 (2.5V) or 2 and 3 (5.0V). By default, a jumper is placed across pins 1 and 2 to enable the 2.5V reference. JP2 selects whether to use the onboard reference selected by JP1 (shunt pins 2 and 3) or use an external reference (shunt pins 1 and 2) from pin J1.18.

Jumper JP3 and JP4 are used to control the reference voltage for group B. JP3 is selectable by connecting a jumper across pins 1 and 2 (2.5V) or 2 and 3 (5.0V). By default, a jumper is placed across pins 1 and 2 to enable the 2.5V reference. JP4 selects whether to use the onboard reference selected by JP3 (shunt pins 2 and 3) or use an external reference (shunt pins 1 and 2) from pin J1.20. By default, the EVM is set to use the onboard 2.5V reference for REF-A and REF-B.

Jumpers JP6 and JP7 control the output signals OFFSET-A and OFFSET-B, respectively. When the evaluation board is used in unipolar mode, pins 2 and 3 (on JP6 and JP7) must be shorted together to connect OFFSET-A and OFFSET-B to ground. When the EVM board is used in bipolar mode, the shunt must be applied across pins 1 and 2 on the jumpers (default mode). The OFFSET-A and OFFSET-B signals are now routed to TP5 and TP6.

JP9 and JP10 set the IOV_{DD} for the DAC7718. The IOV_{DD} is selectable between 1.8V, 3.3V, or 5.0V. Jumper JP10 selects between 5.0V (shunt pins 1 and 2) or 3.3V (shunt pins 2 and 3). JP9 selects between the result from JP10 (shunt pins 2 and 3) or 1.8V (shunt pins 1 and 2). By default, IOV_{DD} is set to 3.3V. See the schematic (appended to the end of this document) for more information.

Jumper JP11 selects the DV_{DD} voltage. Shunting pins 1 and 2 enable DV_{DD} to be 5.0V (default). Shunting pins 2 and 3 set DV_{DD} to 3.3V.

Jumper JP12 selects where to route the $\overline{LDAC}$ signal. By default, pins JP12.2 and JP12.3 are connected to route the $\overline{LDAC}$ signal to J2.15. The shunt can be placed across JP12.1 and JP12.2 to route the $\overline{LDAC}$ signal to J2.17.

The DAC7718 digital control inputs can be accessed through JP14 or the J2 header. $\overline{CLR}$, $\overline{RESET}$, BTC/USB, $\overline{WAKEUP}$, and $\overline{LDAC}$ are all initially pulled high to IOV_{DD} through 10kΩ resistors. These signals can be tied to ground by applying a shunt across the corresponding pins on J14 or through the J2 header.

JP14 is also used to access the GPIO signals. By default, all of the signals are pulled high to IOV_{DD} through 10kΩ resistors. Placing a shunt vertically across the corresponding GPIO pin ties the GPIO signal to ground. GPIO-0 and GPIO-1 can also be controlled through the J2 header.

JP15 is the AV_{SS} selection for the DAC. AV_{SS} can be connected to ground (shunt pins 2 and 3) for unipolar operation mode or pin J3.1 (shunt pins 1 and 2) for bipolar operation. In bipolar mode, a voltage can be applied to J3.1 to power the AV_{SS} of the DAC7718.

7   Schematics and Layout

Schematics for the DAC7718EVM are appended to this user's guide. The bill of materials is provided in Table 6.

7.1   Bill of Materials

> **NOTE:**   All components should be compliant with the European Union Restriction on Use of Hazardous Substances (RoHS) Directive. Some part numbers may be either leaded or RoHS. Verify that purchased components are RoHS-compliant. (For more information about TI's position on RoHS compliance, see the TI web site.)

Table 6. DAC7718EVM Bill of Materials[1]

Item No.	Qty	Ref Des	Description	Manufacturer	Mfr Part Number
1	5	C1, C12, C13, C14, C15	Capacitor, ceramic, 10µF, 25V X5R 1206 10%	Panasonic	ECJ-3YB1E106K
2	2	C2, C22	Capacitor, ceramic, 0.1µF, 16V 0603 X7R 10%	Panasonic	ECJ-1VB1C104K
3	6	C3, C9, C10, C11, C18, C19	Capacitor, ceramic, 1.0µF, 16V X5R 10% 0603	TDK	C1608X5R1C105K
4	4	C4, C16, C17, C20	Capacitor, ceramic, 10µF, 10V 0603 X5R 20%	Panasonic	ECJ-1VB1A106M
5	2	D1, D2	Diode, Schottky, 40V, 350MA SOD123	Micro Commercial Co	SD103AW-TP
6	2	J1A, J2A (Top Side)	10-pin, dual row, SM Header (20 Pos.)	Samtec	TSM-110-01-T-DV-P
7	2	J1B, J2B (Bottom Side)	10 socket dual row, SM Header (20 Pos.)	Samtec	SSW-110-22-F-D-VS-K
8	1	J3A (Top Side)	5-pin, dual row, SM Header (10 Pos.)	Samtec	TSM-105-01-T-DV-P
9	1	J3B[2] (Bottom Side)	5 Socket, dual row, SM Header (10 Pos.)	Samtec	SSW-105-22-F-D-VS-K
10	1	J4	Header strip, 4 pin (2x2)	Samtec	TSW-102-07-L-D
11	11	JP1, JP2, JP3, JP4, JP6, JP7, JP9, JP10, JP11, JP12, JP15	Header strip, 3 pin (1x3)	Samtec	TSW-103-07-L-S
12	1	JP13	Header strip, 6 pin (2x3)	Samtec	TSW-103-07-L-D
13	1	JP14	Header strip, 12 pin (2x6)	Samtec	TSW-106-07-L-D
14	2	R1, R2	Resistor, 2.00kΩ 1/10W 1% 0603 SMD	Panasonic	ERJ-3EKF2001V
15	10	R6, R7, R8, R9, R10, R11, R12, R13, R14, R20	Resistor, 10kΩ 1/10W 5% 0603 SMD	Yageo	RC0603JR-0710KL
16	5	R15, R16, R17, R18, R19	Resistor, 33Ω 1/10W 5% 0603 SMD	Panasonic	ERJ-3GEYJ330V
17	10	TP1, TP2, TP3, TP4, TP5, TP6, TP8, TP9, TP10, TP11	Test Point - Single .025-pin, Red	Keystone	5000
18	2	TP12, TP13	Test Point - Single .025-pin, Black	Keystone	5001
19	1	U1	Single output, 8V voltage regulator	Texas Instruments	TL750L08CD
20	1	U2	Precision voltage reference 2.5V	Texas Instruments	REF5025AID
21	1	U3	Precision voltage reference 5.0V	Texas Instruments	REF5050AID
22	1	U4	Octal, 12-bit, High-Accuracy DAC, TQFP Package	Texas Instruments	DAC7718SPAG

[1]   Manufacturer and part number for items may be substituted with electrically equivalent items.
[2]   J3B parts are not shown in the schematic diagram. J3B is installed on the bottom side of the PWB opposite to J3A.

Revision History

Changes from Original (February, 2010) to A Revision   **Page**

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

U1
TL750L08
Input Output
NC
NC Com
Com Com
Com

AVDD
C1 10uF

8V

U3
Vin DNC DNC NC Vout
TEMP GND TRIM
REF5050
C2 0.1uF
REF5V TP2 REF5V
C3 1uF
C4 10uF

TP12 AGND
TP13 DGND

EXT_REFA
REF5V JP2
REF2.5V JP1
REFASel2
REFASel1
R1 2K
TP3 REF_A
REF_A
C17 10uF
DVDD
D1 DIODE-SCHOTTKY

EXT_REFB
REF5V JP4
REF2.5V JP3
REFBSel2
REFBSel1
R2 2K
TP4 REF_B
REF_B
C16 10uF
DVDD
D2 DIODE-SCHOTTKY

U2
Vin DNC DNC Vout
TEMP GND TRIM
REF5025
8V
C18 1uF
REF2.5V TP1 REF2.5V
C19 1uF
C20 10uF

DVDD
C9 1uF
IOVDD
C10 1uF
AVDD
C12 10uF C13 10uF
AVSS
C14 10uF C15 10uF
C11 1uF

IOVDD

R20 10k R6 10k R7 10k R8 10k R9 10k R10 10k R11 10k

J4
Ain Header

J2A
/CLR GPIO0 CNTL
/RESET DGND CLKX
BTC/USB GPIO1 CLKR
GPIO2 FSX
/WAKEUP DGND FSR
GPIO0 GPIO3 DX
GPIO4 DR
SCL /INT
DGND TOUT
SDA GPIO5
Daughter Serial - Top

R15 33
R16 33
R17 33
R18 33

/RESET RSTSEL
/CLR
BTC/USB
/WAKEUP

R19 33

GPIO0
GPIO1

U4
CS
SCLK
DVDD-A DVDD-B IOVDD
AVDD-A AVDD-B
AVSS-A AVSS-B
Ain-0
Ain-1
SDI
SDO
Vmon
REF-A
REF-B
RST
RSTSEL
OFFSET-A
Vout-0
Vout-1
CLR
Vout-2
BTC/USB
Vout-3
WAKEUP
Vout-4
LDAC
Vout-5
GPIO-0
Vout-6
GPIO-1
GPIO-2
Vout-7
N/C
OFFSET-B
DACxx18
N/C
DGND-A DGND-B AGND-A AGND-B AGND-A AGND-B

JP12
LDAC Selection

J2B
/CLR /CS
/RESET SCLK
BTC/USB SCLK
/CS
/WAKEUP /CS
GPIO0 SDI
/LDAC1
/LDAC2
GPIO1
Daughter Serial - Bottom

TP8 SDI

IOVDD
GPIO0
GPIO1
GPIO2

R12 10k R13 10k R14 10k

JP14

JP13
JPR-2X3

TP11 Vmon
C22 0.1uF

TP5
JP6

TP7
JP7

TP6

J1
A0(+) A0(-)
A1(+) A1(-)
A2(+) A2(-)
A3(+) A3(-)
A4 AGND
A5 AGND
A6 VCOM
A7 AGND
REF- AGND
REF+ AGND
EXT_REFA
EXT_REFB
DAUGHTER-ANALOG

REF_A
REF_B

AVSS -VA
JP15
AVSS Selection

+VA AVDD

TP9 IOVDD
IOVDD
JP9
+1.8V
+5V
JP10
IOVDDSel2
IOVDDSel1

TP10 DVDD
DVDD
+5V
JP11
+3.3V
DVDDSe

+VA
+1.8V
+3.3V

J3A
+VA -VA
+5VA -5VA
DGND AGND
+1.8VD VD1
+3.3VD +5VD
DAUGHTER-POWER

-VA
+5V

ti
PRECISION ANALOG PRODUCTS
HIGH-PERFORMANCE ANALOG DIVISION
SEMICONDUCTOR GROUP
5411 EAST WILLIAMS BOULEVARD, TUCSON, AZ 85711 USA

TITLE
DACxx18EVM

ENGINEER
DRAWN BY
DOCUMENT CONTROL NO.
SIZE B DATE 10/2009 REV A
SHEET OF FILE 6512097

Evaluation Board/Kit Important Notice

Texas Instruments (TI) provides the enclosed product(s) under the following conditions:

This evaluation board/kit is intended for use for **ENGINEERING DEVELOPMENT, DEMONSTRATION, OR EVALUATION PURPOSES ONLY** and is not considered by TI to be a finished end-product fit for general consumer use. Persons handling the product(s) must have electronics training and observe good engineering practice standards. As such, the goods being provided are not intended to be complete in terms of required design-, marketing-, and/or manufacturing-related protective considerations, including product safety and environmental measures typically found in end products that incorporate such semiconductor components or circuit boards. This evaluation board/kit does not fall within the scope of the European Union directives regarding electromagnetic compatibility, restricted substances (RoHS), recycling (WEEE), FCC, CE or UL, and therefore may not meet the technical requirements of these directives or other related directives.

Should this evaluation board/kit not meet the specifications indicated in the User's Guide, the board/kit may be returned within 30 days from the date of delivery for a full refund. THE FOREGOING WARRANTY IS THE EXCLUSIVE WARRANTY MADE BY SELLER TO BUYER AND IS IN LIEU OF ALL OTHER WARRANTIES, EXPRESSED, IMPLIED, OR STATUTORY, INCLUDING ANY WARRANTY OF MERCHANTABILITY OR FITNESS FOR ANY PARTICULAR PURPOSE.

The user assumes all responsibility and liability for proper and safe handling of the goods. Further, the user indemnifies TI from all claims arising from the handling or use of the goods. Due to the open construction of the product, it is the user's responsibility to take any and all appropriate precautions with regard to electrostatic discharge.

EXCEPT TO THE EXTENT OF THE INDEMNITY SET FORTH ABOVE, NEITHER PARTY SHALL BE LIABLE TO THE OTHER FOR ANY INDIRECT, SPECIAL, INCIDENTAL, OR CONSEQUENTIAL DAMAGES.

TI currently deals with a variety of customers for products, and therefore our arrangement with the user **is not exclusive.**

TI assumes **no liability for applications assistance, customer product design, software performance, or infringement of patents or services described herein.**

Please read the User's Guide and, specifically, the Warnings and Restrictions notice in the User's Guide prior to handling the product. This notice contains important safety information about temperatures and voltages. For additional information on TI's environmental and/or safety programs, please contact the TI application engineer or visit www.ti.com/esh.

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This evaluation board/kit is intended for use for **ENGINEERING DEVELOPMENT, DEMONSTRATION, OR EVALUATION PURPOSES ONLY** and is not considered by TI to be a finished end-product fit for general consumer use. It generates, uses, and can radiate radio frequency energy and has not been tested for compliance with the limits of computing devices pursuant to part 15 of FCC rules, which are designed to provide reasonable protection against radio frequency interference. Operation of this equipment in other environments may cause interference with radio communications, in which case the user at his own expense will be required to take whatever measures may be required to correct this interference.

EVM Warnings and Restrictions

It is important to operate this EVM within the input voltage range of –16.5V to +21V and the output voltage range of –15V to +15V.

Exceeding the specified input range may cause unexpected operation and/or irreversible damage to the EVM. If there are questions concerning the input range, please contact a TI field representative prior to connecting the input power.

Applying loads outside of the specified output range may result in unintended operation and/or possible permanent damage to the EVM. Please consult the EVM User's Guide prior to connecting any load to the EVM output. If there is uncertainty as to the load specification, please contact a TI field representative.

During normal operation, some circuit components may have case temperatures greater than +30° C. The EVM is designed to operate properly with certain components above +60° C as long as the input and output ranges are maintained. These components include but are not limited to linear regulators, switching transistors, pass transistors, and current sense resistors. These types of devices can be identified using the EVM schematic located in the EVM User's Guide. When placing measurement probes near these devices during operation, please be aware that these devices may be very warm to the touch.

STANDARD TERMS FOR EVALUATION MODULES

1. *Delivery:* TI delivers TI evaluation boards, kits, or modules, including any accompanying demonstration software, components, and/or documentation which may be provided together or separately (collectively, an "EVM" or "EVMs") to the User ("User") in accordance with the terms set forth herein. User's acceptance of the EVM is expressly subject to the following terms.

    1.1 EVMs are intended solely for product or software developers for use in a research and development setting to facilitate feasibility evaluation, experimentation, or scientific analysis of TI semiconductors products. EVMs have no direct function and are not finished products. EVMs shall not be directly or indirectly assembled as a part or subassembly in any finished product. For clarification, any software or software tools provided with the EVM ("Software") shall not be subject to the terms and conditions set forth herein but rather shall be subject to the applicable terms that accompany such Software

    1.2 EVMs are not intended for consumer or household use. EVMs may not be sold, sublicensed, leased, rented, loaned, assigned, or otherwise distributed for commercial purposes by Users, in whole or in part, or used in any finished product or production system.

2   *Limited Warranty and Related Remedies/Disclaimers*:

    2.1 These terms do not apply to Software. The warranty, if any, for Software is covered in the applicable Software License Agreement.

    2.2 TI warrants that the TI EVM will conform to TI's published specifications for ninety (90) days after the date TI delivers such EVM to User. Notwithstanding the foregoing, TI shall not be liable for a nonconforming EVM if (a) the nonconformity was caused by neglect, misuse or mistreatment by an entity other than TI, including improper installation or testing, or for any EVMs that have been altered or modified in any way by an entity other than TI, (b) the nonconformity resulted from User's design, specifications or instructions for such EVMs or improper system design, or (c) User has not paid on time. Testing and other quality control techniques are used to the extent TI deems necessary. TI does not test all parameters of each EVM. User's claims against TI under this Section 2 are void if User fails to notify TI of any apparent defects in the EVMs within ten (10) business days after delivery, or of any hidden defects with ten (10) business days after the defect has been detected.

    2.3 TI's sole liability shall be at its option to repair or replace EVMs that fail to conform to the warranty set forth above, or credit User's account for such EVM. TI's liability under this warranty shall be limited to EVMs that are returned during the warranty period to the address designated by TI and that are determined by TI not to conform to such warranty. If TI elects to repair or replace such EVM, TI shall have a reasonable time to repair such EVM or provide replacements. Repaired EVMs shall be warranted for the remainder of the original warranty period. Replaced EVMs shall be warranted for a new full ninety (90) day warranty period.

WARNING

Evaluation Kits are intended solely for use by technically qualified, professional electronics experts who are familiar with the dangers and application risks associated with handling electrical mechanical components, systems, and subsystems.

User shall operate the Evaluation Kit within TI's recommended guidelines and any applicable legal or environmental requirements as well as reasonable and customary safeguards. Failure to set up and/or operate the Evaluation Kit within TI's recommended guidelines may result in personal injury or death or property damage. Proper set up entails following TI's instructions for electrical ratings of interface circuits such as input, output and electrical loads.

NOTE:

EXPOSURE TO ELECTROSTATIC DISCHARGE (ESD) MAY CAUSE DEGREDATION OR FAILURE OF THE EVALUATION KIT; TI RECOMMENDS STORAGE OF THE EVALUATION KIT IN A PROTECTIVE ESD BAG.

3 *Regulatory Notices:*

3.1 *United States*

3.1.1 *Notice applicable to EVMs not FCC-Approved:*

FCC NOTICE: This kit is designed to allow product developers to evaluate electronic components, circuitry, or software associated with the kit to determine whether to incorporate such items in a finished product and software developers to write software applications for use with the end product. This kit is not a finished product and when assembled may not be resold or otherwise marketed unless all required FCC equipment authorizations are first obtained. Operation is subject to the condition that this product not cause harmful interference to licensed radio stations and that this product accept harmful interference. Unless the assembled kit is designed to operate under part 15, part 18 or part 95 of this chapter, the operator of the kit must operate under the authority of an FCC license holder or must secure an experimental authorization under part 5 of this chapter.

3.1.2 *For EVMs annotated as FCC – FEDERAL COMMUNICATIONS COMMISSION Part 15 Compliant:*

CAUTION

This device complies with part 15 of the FCC Rules. Operation is subject to the following two conditions: (1) This device may not cause harmful interference, and (2) this device must accept any interference received, including interference that may cause undesired operation.

Changes or modifications not expressly approved by the party responsible for compliance could void the user's authority to operate the equipment.

FCC Interference Statement for Class A EVM devices

NOTE: This equipment has been tested and found to comply with the limits for a Class A digital device, pursuant to part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference when the equipment is operated in a commercial environment. This equipment generates, uses, and can radiate radio frequency energy and, if not installed and used in accordance with the instruction manual, may cause harmful interference to radio communications. Operation of this equipment in a residential area is likely to cause harmful interference in which case the user will be required to correct the interference at his own expense.

FCC Interference Statement for Class B EVM devices

NOTE: This equipment has been tested and found to comply with the limits for a Class B digital device, pursuant to part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference in a residential installation. This equipment generates, uses and can radiate radio frequency energy and, if not installed and used in accordance with the instructions, may cause harmful interference to radio communications. However, there is no guarantee that interference will not occur in a particular installation. If this equipment does cause harmful interference to radio or television reception, which can be determined by turning the equipment off and on, the user is encouraged to try to correct the interference by one or more of the following measures:

- *Reorient or relocate the receiving antenna.*
- *Increase the separation between the equipment and receiver.*
- *Connect the equipment into an outlet on a circuit different from that to which the receiver is connected.*
- *Consult the dealer or an experienced radio/TV technician for help.*

3.2 *Canada*

3.2.1 *For EVMs issued with an Industry Canada Certificate of Conformance to RSS-210 or RSS-247*

Concerning EVMs Including Radio Transmitters:

This device complies with Industry Canada license-exempt RSSs. Operation is subject to the following two conditions:

(1) this device may not cause interference, and (2) this device must accept any interference, including interference that may cause undesired operation of the device.

Concernant les EVMs avec appareils radio:

Le présent appareil est conforme aux CNR d'Industrie Canada applicables aux appareils radio exempts de licence. L'exploitation est autorisée aux deux conditions suivantes: (1) l'appareil ne doit pas produire de brouillage, et (2) l'utilisateur de l'appareil doit accepter tout brouillage radioélectrique subi, même si le brouillage est susceptible d'en compromettre le fonctionnement.

Concerning EVMs Including Detachable Antennas:

Under Industry Canada regulations, this radio transmitter may only operate using an antenna of a type and maximum (or lesser) gain approved for the transmitter by Industry Canada. To reduce potential radio interference to other users, the antenna type and its gain should be so chosen that the equivalent isotropically radiated power (e.i.r.p.) is not more than that necessary for successful communication. This radio transmitter has been approved by Industry Canada to operate with the antenna types listed in the user guide with the maximum permissible gain and required antenna impedance for each antenna type indicated. Antenna types not included in this list, having a gain greater than the maximum gain indicated for that type, are strictly prohibited for use with this device.

Concernant les EVMs avec antennes détachables

Conformément à la réglementation d'Industrie Canada, le présent émetteur radio peut fonctionner avec une antenne d'un type et d'un gain maximal (ou inférieur) approuvé pour l'émetteur par Industrie Canada. Dans le but de réduire les risques de brouillage radioélectrique à l'intention des autres utilisateurs, il faut choisir le type d'antenne et son gain de sorte que la puissance isotrope rayonnée équivalente (p.i.r.e.) ne dépasse pas l'intensité nécessaire à l'établissement d'une communication satisfaisante. Le présent émetteur radio a été approuvé par Industrie Canada pour fonctionner avec les types d'antenne énumérés dans le manuel d'usage et ayant un gain admissible maximal et l'impédance requise pour chaque type d'antenne. Les types d'antenne non inclus dans cette liste, ou dont le gain est supérieur au gain maximal indiqué, sont strictement interdits pour l'exploitation de l'émetteur

3.3 *Japan*

3.3.1 *Notice for EVMs delivered in Japan:* Please see http://www.tij.co.jp/lsds/ti_ja/general/eStore/notice_01.page 日本国内に輸入される評価用キット、ボードについては、次のところをご覧ください。

https://www.ti.com/ja-jp/legal/notice-for-evaluation-kits-delivered-in-japan.html

3.3.2 *Notice for Users of EVMs Considered "Radio Frequency Products" in Japan:* EVMs entering Japan may not be certified by TI as conforming to Technical Regulations of Radio Law of Japan.

If User uses EVMs in Japan, not certified to Technical Regulations of Radio Law of Japan, User is required to follow the instructions set forth by Radio Law of Japan, which includes, but is not limited to, the instructions below with respect to EVMs (which for the avoidance of doubt are stated strictly for convenience and should be verified by User):

1. Use EVMs in a shielded room or any other test facility as defined in the notification #173 issued by Ministry of Internal Affairs and Communications on March 28, 2006, based on Sub-section 1.1 of Article 6 of the Ministry's Rule for Enforcement of Radio Law of Japan,

2. Use EVMs only after User obtains the license of Test Radio Station as provided in Radio Law of Japan with respect to EVMs, or

3. Use of EVMs only after User obtains the Technical Regulations Conformity Certification as provided in Radio Law of Japan with respect to EVMs. Also, do not transfer EVMs, unless User gives the same notice above to the transferee. Please note that if User does not follow the instructions above, User will be subject to penalties of Radio Law of Japan.

【無線電波を送信する製品の開発キットをお使いになる際の注意事項】 開発キットの中には技術基準適合証明を受けて

いないものがあります。 技術適合証明を受けていないもののご使用に際しては、電波法遵守のため、以下のいずれかの

措置を取っていただく必要がありますのでご注意ください。

1. 電波法施行規則第6条第1項第1号に基づく平成18年3月28日総務省告示第173号で定められた電波暗室等の試験設備でご使用いただく。
2. 実験局の免許を取得後ご使用いただく。
3. 技術基準適合証明を取得後ご使用いただく。

なお、本製品は、上記の「ご使用にあたっての注意」を譲渡先、移転先に通知しない限り、譲渡、移転できないものとします。
        上記を遵守頂けない場合は、電波法の罰則が適用される可能性があることをご留意ください。 日本テキサス・イ

ンスツルメンツ株式会社

東京都新宿区西新宿６丁目２４番１号

西新宿三井ビル

3.3.3 *Notice for EVMs for Power Line Communication:* Please see http://www.tij.co.jp/lsds/ti_ja/general/eStore/notice_02.page

電力線搬送波通信についての開発キットをお使いになる際の注意事項については、次のところをご覧ください。https://www.ti.com/ja-jp/legal/notice-for-evaluation-kits-for-power-line-communication.html

3.4 *European Union*

3.4.1 *For EVMs subject to EU Directive 2014/30/EU (Electromagnetic Compatibility Directive):*

This is a class A product intended for use in environments other than domestic environments that are connected to a low-voltage power-supply network that supplies buildings used for domestic purposes. In a domestic environment this product may cause radio interference in which case the user may be required to take adequate measures.

4   *EVM Use Restrictions and Warnings:*

    4.1   EVMS ARE NOT FOR USE IN FUNCTIONAL SAFETY AND/OR SAFETY CRITICAL EVALUATIONS, INCLUDING BUT NOT LIMITED TO EVALUATIONS OF LIFE SUPPORT APPLICATIONS.

    4.2   User must read and apply the user guide and other available documentation provided by TI regarding the EVM prior to handling or using the EVM, including without limitation any warning or restriction notices. The notices contain important safety information related to, for example, temperatures and voltages.

    4.3   *Safety-Related Warnings and Restrictions:*

        4.3.1   User shall operate the EVM within TI's recommended specifications and environmental considerations stated in the user guide, other available documentation provided by TI, and any other applicable requirements and employ reasonable and customary safeguards. Exceeding the specified performance ratings and specifications (including but not limited to input and output voltage, current, power, and environmental ranges) for the EVM may cause personal injury or death, or property damage. If there are questions concerning performance ratings and specifications, User should contact a TI field representative prior to connecting interface electronics including input power and intended loads. Any loads applied outside of the specified output range may also result in unintended and/or inaccurate operation and/or possible permanent damage to the EVM and/or interface electronics. Please consult the EVM user guide prior to connecting any load to the EVM output. If there is uncertainty as to the load specification, please contact a TI field representative. During normal operation, even with the inputs and outputs kept within the specified allowable ranges, some circuit components may have elevated case temperatures. These components include but are not limited to linear regulators, switching transistors, pass transistors, current sense resistors, and heat sinks, which can be identified using the information in the associated documentation. When working with the EVM, please be aware that the EVM may become very warm.

        4.3.2   EVMs are intended solely for use by technically qualified, professional electronics experts who are familiar with the dangers and application risks associated with handling electrical mechanical components, systems, and subsystems. User assumes all responsibility and liability for proper and safe handling and use of the EVM by User or its employees, affiliates, contractors or designees. User assumes all responsibility and liability to ensure that any interfaces (electronic and/or mechanical) between the EVM and any human body are designed with suitable isolation and means to safely limit accessible leakage currents to minimize the risk of electrical shock hazard. User assumes all responsibility and liability for any improper or unsafe handling or use of the EVM by User or its employees, affiliates, contractors or designees.

    4.4   User assumes all responsibility and liability to determine whether the EVM is subject to any applicable international, federal, state, or local laws and regulations related to User's handling and use of the EVM and, if applicable, User assumes all responsibility and liability for compliance in all respects with such laws and regulations. User assumes all responsibility and liability for proper disposal and recycling of the EVM consistent with all applicable international, federal, state, and local requirements.

5.   *Accuracy of Information:* To the extent TI provides information on the availability and function of EVMs, TI attempts to be as accurate as possible. However, TI does not warrant the accuracy of EVM descriptions, EVM availability or other information on its websites as accurate, complete, reliable, current, or error-free.

6.   *Disclaimers:*

    6.1   EXCEPT AS SET FORTH ABOVE, EVMS AND ANY MATERIALS PROVIDED WITH THE EVM (INCLUDING, BUT NOT LIMITED TO, REFERENCE DESIGNS AND THE DESIGN OF THE EVM ITSELF) ARE PROVIDED "AS IS" AND "WITH ALL FAULTS." TI DISCLAIMS ALL OTHER WARRANTIES, EXPRESS OR IMPLIED, REGARDING SUCH ITEMS, INCLUDING BUT NOT LIMITED TO ANY EPIDEMIC FAILURE WARRANTY OR IMPLIED WARRANTIES OF MERCHANTABILITY OR FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF ANY THIRD PARTY PATENTS, COPYRIGHTS, TRADE SECRETS OR OTHER INTELLECTUAL PROPERTY RIGHTS.

    6.2   EXCEPT FOR THE LIMITED RIGHT TO USE THE EVM SET FORTH HEREIN, NOTHING IN THESE TERMS SHALL BE CONSTRUED AS GRANTING OR CONFERRING ANY RIGHTS BY LICENSE, PATENT, OR ANY OTHER INDUSTRIAL OR INTELLECTUAL PROPERTY RIGHT OF TI, ITS SUPPLIERS/LICENSORS OR ANY OTHER THIRD PARTY, TO USE THE EVM IN ANY FINISHED END-USER OR READY-TO-USE FINAL PRODUCT, OR FOR ANY INVENTION, DISCOVERY OR IMPROVEMENT, REGARDLESS OF WHEN MADE, CONCEIVED OR ACQUIRED.

7.   *USER'S INDEMNITY OBLIGATIONS AND REPRESENTATIONS.* USER WILL DEFEND, INDEMNIFY AND HOLD TI, ITS LICENSORS AND THEIR REPRESENTATIVES HARMLESS FROM AND AGAINST ANY AND ALL CLAIMS, DAMAGES, LOSSES, EXPENSES, COSTS AND LIABILITIES (COLLECTIVELY, "CLAIMS") ARISING OUT OF OR IN CONNECTION WITH ANY HANDLING OR USE OF THE EVM THAT IS NOT IN ACCORDANCE WITH THESE TERMS. THIS OBLIGATION SHALL APPLY WHETHER CLAIMS ARISE UNDER STATUTE, REGULATION, OR THE LAW OF TORT, CONTRACT OR ANY OTHER LEGAL THEORY, AND EVEN IF THE EVM FAILS TO PERFORM AS DESCRIBED OR EXPECTED.

8. *Limitations on Damages and Liability:*

   8.1 *General Limitations.* IN NO EVENT SHALL TI BE LIABLE FOR ANY SPECIAL, COLLATERAL, INDIRECT, PUNITIVE, INCIDENTAL, CONSEQUENTIAL, OR EXEMPLARY DAMAGES IN CONNECTION WITH OR ARISING OUT OF THESE TERMS OR THE USE OF THE EVMS , REGARDLESS OF WHETHER TI HAS BEEN ADVISED OF THE POSSIBILITY OF SUCH DAMAGES. EXCLUDED DAMAGES INCLUDE, BUT ARE NOT LIMITED TO, COST OF REMOVAL OR REINSTALLATION, ANCILLARY COSTS TO THE PROCUREMENT OF SUBSTITUTE GOODS OR SERVICES, RETESTING, OUTSIDE COMPUTER TIME, LABOR COSTS, LOSS OF GOODWILL, LOSS OF PROFITS, LOSS OF SAVINGS, LOSS OF USE, LOSS OF DATA, OR BUSINESS INTERRUPTION. NO CLAIM, SUIT OR ACTION SHALL BE BROUGHT AGAINST TI MORE THAN TWELVE (12) MONTHS AFTER THE EVENT THAT GAVE RISE TO THE CAUSE OF ACTION HAS OCCURRED.

   8.2 *Specific Limitations.* IN NO EVENT SHALL TI'S AGGREGATE LIABILITY FROM ANY USE OF AN EVM PROVIDED HEREUNDER, INCLUDING FROM ANY WARRANTY, INDEMITY OR OTHER OBLIGATION ARISING OUT OF OR IN CONNECTION WITH THESE TERMS, , EXCEED THE TOTAL AMOUNT PAID TO TI BY USER FOR THE PARTICULAR EVM(S) AT ISSUE DURING THE PRIOR TWELVE (12) MONTHS WITH RESPECT TO WHICH LOSSES OR DAMAGES ARE CLAIMED. THE EXISTENCE OF MORE THAN ONE CLAIM SHALL NOT ENLARGE OR EXTEND THIS LIMIT.

9. *Return Policy.* Except as otherwise provided, TI does not offer any refunds, returns, or exchanges. Furthermore, no return of EVM(s) will be accepted if the package has been opened and no return of the EVM(s) will be accepted if they are damaged or otherwise not in a resalable condition. If User feels it has been incorrectly charged for the EVM(s) it ordered or that delivery violates the applicable order, User should contact TI. All refunds will be made in full within thirty (30) working days from the return of the components(s), excluding any postage or packaging costs.

10. *Governing Law:* These terms and conditions shall be governed by and interpreted in accordance with the laws of the State of Texas, without reference to conflict-of-laws principles. User agrees that non-exclusive jurisdiction for any dispute arising out of or relating to these terms and conditions lies within courts located in the State of Texas and consents to venue in Dallas County, Texas. Notwithstanding the foregoing, any judgment may be enforced in any United States or foreign court, and TI may seek injunctive relief in any United States or foreign court.

IMPORTANT NOTICE AND DISCLAIMER

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TI objects to and rejects any additional or different terms you may propose.