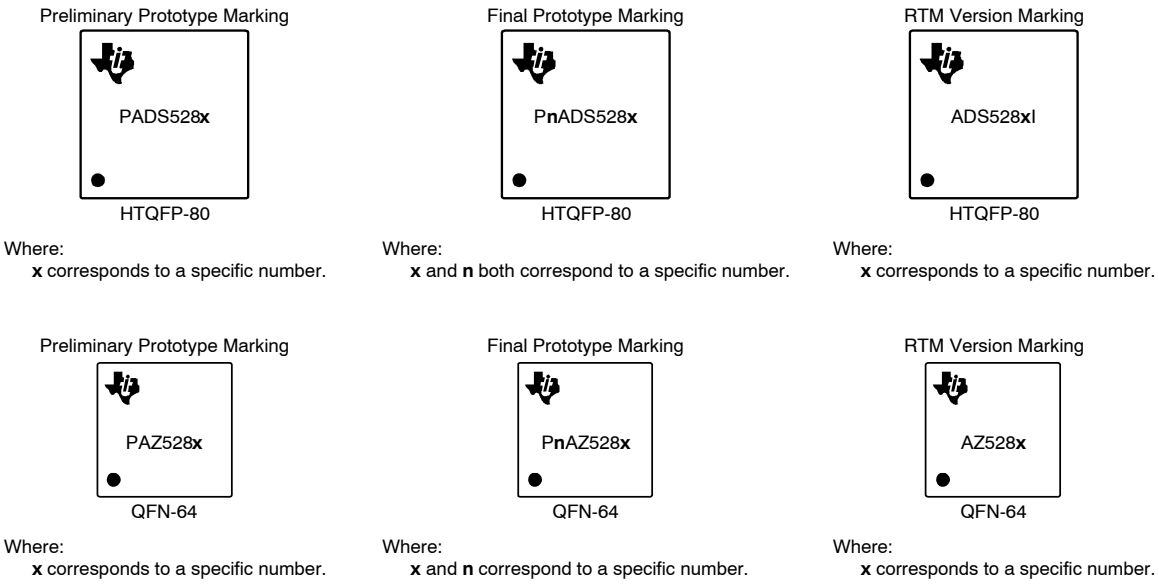
Errata to ADS528x, Data Sheet Literature Number SBAS397

Revision Identification

Figure 1 explains the ADS528x package marking for both the HTQFP-80 and QFN-64 packages for the device and the differences between the package marking on the preliminary prototype and how the package marking will appear in the final prototype version as well as the version that is released to market (RTM).

Figure 1. Package Symbolization Definition



This document describes the planned record of revisions to the design of the ADS528x family with respect to the *preliminary prototype version* of the silicon that is being sampled in Q1, 2007. The next version of silicon (referred to in these errata as the *final prototype*) incorporates all the corrections listed in these errata. These corrections will also be reflected in the RTM version of the product data sheet.

Errata Index

1. LVDS timing diagram.
2. Power-down mode.
3. Dither mode.
4. Pattern register bits.
5. SNR enhancement mode.

Erratum #1

Brief Description of Issue

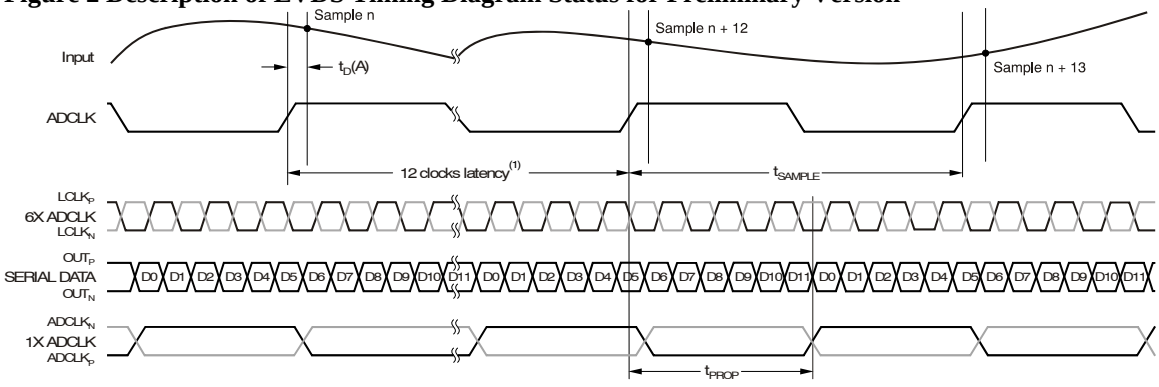
LVDS Timing Diagram:

1) Inverse polarity of $LCLK_N$ and $LCLK_P$.

Detailed Description of Issue

The timing diagram for the LVDS signals on the preliminary prototype version is shown in Figure 2. However, Page 6 of the ADS528x data sheet (SBAS397, published December 2006) shows an LVDS timing diagram that matches Figure 3, which is the way it will appear in the final prototype version of the silicon.

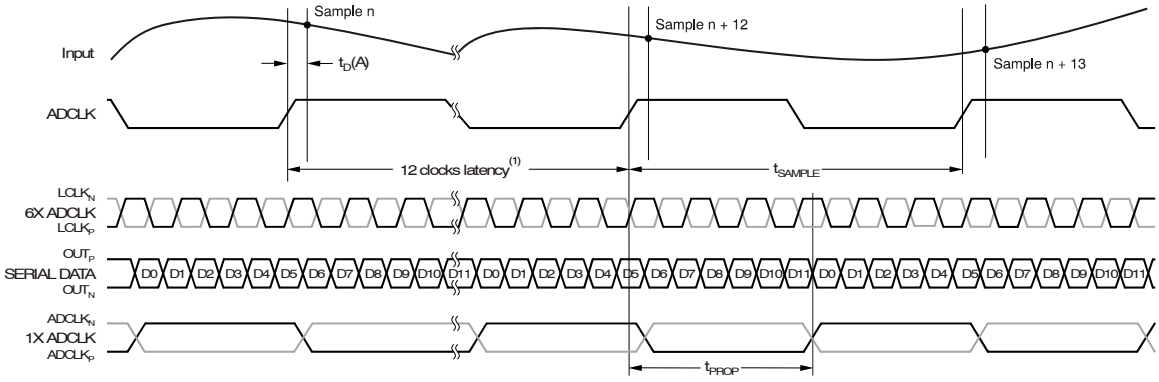
Figure 2 Description of LVDS Timing Diagram Status for Preliminary Version



NOTE: (1) Subject to change by an integer number of clocks.

Note the inversion in polarity of $LCLK_P$ and $LCLK_N$ in Figure 3, as compared to Figure 2. The first edge of $LCLK_P$ after the rising edge of $ADCLK_P$ will be a falling edge in the final prototype version, as is the case in the ADS527x family. The polarity inversion can also be described as a phase change of 180 degrees.

Figure 3 Description of LVDS Timing Diagram Status for Final Version



NOTE: (1) Subject to change by an integer number of clocks.

Impact to Customer

1) If the customer's prototype has built-in deskew capability, it is expected that there will be no impact to the deserializer in this revision. If deskew capability is not available, and the customer is using samples of the preliminary version for prototype development, it is recommended that the customer develop the prototype according to the timing diagram shown in Figure 2 (preliminary prototype version), and build in the capability to handle the polarity inversion of $LCLK_P$ and $LCLK_N$ on the final version.

SW or HW Workaround

N/A

Affected Devices

The TI ADSDeSer-50EVM high-speed deserializer (SBAU091) has built-in deskew capability. The change in polarity of $LCLK_P$ and $LCLK_N$ will therefore be corrected as a timing skew with respect to the data lines. Therefore, the TI ADS528x evaluation module will be able to work correctly with both the preliminary version as well as the final version **without any change in deserialization code**.

Erratum #2

Brief Description of Issue

Power-Down Mode:

1) Power consumption in power-down mode.

Detailed Description of Issue

The ADS528x can be programmed to go into complete power-down using the PD pin (pin 16). The preliminary version consumes about 20mW/channel in this mode. In the final version, the power in this mode is reduced to less than 5mW/channel.

Impact to Customer

The ADS528x consumes less power in power-down mode in the final version than in the preliminary version.

SW or HW Workaround

N/A

Affected Devices

N/A

Erratum #3

Brief Description of Issue

Dither Mode:

1) The addition of dither in an application causes SNR degradation on the preliminary silicon.

Detailed Description of Issue

After the ADC is powered up and properly reset, the ADC operates in a mode where a small amount of dither is added by default. In lab investigations on the preliminary version, this dithering has shown to degrade SNR by about 1dB. The dither can be disabled by using the SPI interface to program the appropriate register. Therefore, the best performance on the preliminary version is obtained by disabling the dither mode using the SPI interface.

The preliminary datasheet does not list the register bit for the dither mode because it is not expected to be required for use on the final silicon. Furthermore, all of the preliminary datasheet plots have been generated with the dither mode disabled through the SPI interface.

There will be no SNR degradation in the final version, even when dither mode is ON. Best performance will be obtained without having to program the SPI interface.

Impact to Customer

Customers using the TI ADS528x evaluation module can automatically configure the ADS528x into the mode with the best performance (dither enabled) by issuing a reset command through the software. Customers not using the TI ADS528x evaluation module are requested to contact the factory for details on how to program the SPI interface to disable the dither on the preliminary version. Note that on the final version, none of the above is required.

SW or HW Workaround

N/A

Affected Devices

In addition to resetting the SPI registers, the software reset button on the evaluation software accompanying the TI ADSDeSer-50EVM automatically issues the SPI interface command that disables the dither.

Erratum #4

Brief Description of Issue

LVDS Custom Pattern Register Bits Shifted:

1) The location of the LVDS custom pattern bits in the serial register map is different between the primary silicon and the final version.

Detailed Description of Issue

The location of the LVDS custom pattern bits in the serial register map on the initial silicon version is described in Table 1.

The location of the LVDS custom pattern bits in the serial register map on the final silicon version is detailed in Table 2.

Impact to Customer

Customers using the LVDS custom pattern mode must change their software on the final silicon version to reflect the change in location of the custom pattern bits.

SW or HW Workaround

N/A

Affected Devices

The software accompanying the TI ADSDeSer-50EVM will be changed to reflect the new position of the custom pattern bits in the final silicon version.

Table 1. Initial Silicon LVDS Custom Pattern Bits

ADDRESS IN HEX	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	NAME	DESCRIPTION
25											X	0					DUALCUSTOM_PAT	Enables mode wherein output toggles between two defined codes.
											0	X					SINGLE_CUSTOM_PAT	Enables mode wherein output is a constant specified code.
26					X	X	X	X	X	X	X	X	X	X	X	X	BITS_CUSTOM1<11:0>	12 bits for single custom pattern (and for the first code of the dual custom pattern). <11> is the MSB.
27					X	X	X	X	X	X	X	X	X	X	X	X	BITS_CUSTOM2<11:0>	12 bits for second code of the dual custom pattern.

Table 2. Final Silicon LVDS Custom Pattern Bits

ADDRESS IN HEX	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	NAME	DESCRIPTION
25											X	0					DUALCUSTOM_PAT	Enables mode wherein output toggles between two defined codes.
											0	X					SINGLE_CUSTOM_PAT	Enables mode wherein output is a constant specified code.
															X	X	BITS_CUSTOM1<11:10>	Two MSBs for single custom pattern (and for the first code of the dual custom pattern). <11> is the MSB.
													X	X			BITS_CUSTOM2<11:10>	Two MSBs for second code of the dual custom pattern.
26	X	X	X	X	X	X	X	X	X	X							BITS_CUSTOM1<9:0>	10 lower bits for single custom pattern (and for the first code of the dual custom pattern). <0> is the LSB.
27	X	X	X	X	X	X	X	X	X	X							BITS_CUSTOM2<9:0>	10 lower bits for second code of the dual custom pattern.

Erratum #5

Brief Description of Issue

SNR Enhancement Mode enabled by default in final version.

Detailed Description of Issue

In the preliminary version of silicon, SNR Enhancement Mode was disabled by default. To enable SNR Enhancement Mode, Register 43 needed to be written to as shown below.

SERIAL INTERFACE REGISTERS (continued)

ADDRESS IN HEX	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	DESCRIPTION	REMARKS
43	1															X	SNR enhancement mode for high programmable gain settings.	Setting D0 to 1 improves the SNR at high programmable gain settings, where the input FSR is lower than 2V. SNR could improve by as much as 2dBFs at the highest (12dB) programmable gain setting.

In the final version of silicon, this mode is enabled by default, and does not need to be written to. Also, this mode will not appear in the product data sheet that will be released with the final version of silicon.

Impact to Customer

Customers who were writing to Bit 0 of Register 43 to enable this mode do not need to do so any longer (though writing a '1' into this bit continues to operate the device in this mode).

SW or HW Workaround

N/A

Affected Devices

This mode will be removed from the software that accompanies the TI ADSDeSer-50EVM.

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