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Stabilizing Current-Feedback Op Amps While Optimizing Circuit Performance using PSpice

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ABSTRACT

Optimizing a circuit design with a current-feedback (CFB) op amp is a relatively straightforward task, once one understands how CFB op amps achieve stability. This application note explains a 2nd-order CFB model so that any designer can better understand the flexibility of the CFB op amp. This report discusses stability analysis, the effects of parasitic components due to printed circuit boards (PCBs), optimization of noise components, and changing the feedback resistor while maintaining amplifier performance and stability. Numerous other topics pertaining to CFBs are also addressed with detailed examples. All results are shown in PSpice, while associating stability of the frequency response to the time domain.

Contents

List of Figures

List of Tables

1 Introduction

The internal architecture of a current-feedback (CFB) amplifier differs from a voltage-feedback (VFB) op amp in the way that the device processes signals and achieves stability. Both architectures, however, amplify the signal from the input to the output with gain. Selecting one high-speed topology or the other (CFB or VFB) can be a difficult task if one is not aware of which parameters make a CFB amp a better choice for certain applications. This report offers a detailed discussion of TI CFB high-speed amplifiers. There are numerous examples cited using PSpice™ and circuit connections to demonstrate the analyses, parameter measurements, and the effects of parasitic components upon device and signal stability.

2 Understanding CFB Topologies

Although the CFB amp has been available for some time, it is often used inappropriately because designers fail to understand several critical internal characteristics. Furthermore, the relation of an external feedback resistor (as compared to a VFB amplifier) to the closed-loop stability is often misunderstood. Therefore, a brief review of the CFB circuit model helps to explain its signal processing capabilities.

The CFB amplifier was primarily designed to reduce or eliminate the Gain-Bandwidth Product associated with VFB amplifiers. This characteristic makes it easy to use the same amplifier in several parts of a design with different gain settings. Another distinguishing feature of CFBs is that they have large signal voltage swings or slew rates (SR). The SR specification is usually higher in CFB amplifier designs than in VFB applications, and is generally the term that approximates the larger signal voltage bandwidth. CFBs also generally have a lower quiescent current for a given bandwidth, thus making CFB amplifiers more attractive for designs where power consumption is important and multiple amplifiers are required.

Texas Instruments has been a leading innovator in improving CFB technology, particularly at the input and output stages of the device. First-generation CFB amp topology is similar to that shown in Figure 1.

In addition to its other distinguishing capabilities, the CFB topology creates an error current, which is the summation of the current terms at the inverting input pin. With this information, one can derive an equation for the CFB amplifier based on node analysis. After some careful math manipulation, the CFB open-loop frequency response (as well as the closed-loop frequency response) can be shown from the equation. More importantly, however, the equation shows the independence of gain in relation to the bandwidth and the dependence of stability, R_F. More detailed discussion of this connection will be given later.

The CFB amplifier is fairly well-balanced as long as the amplifier's load and feedback paths see a resistive component. The CFB amplifier becomes unstable when capacitance and inductance appear in such a way as to create unwanted results or undesirable effects. Learning how to select CFB resistors and deal with certain components to assure application stability is the focus of the balance of this paper.

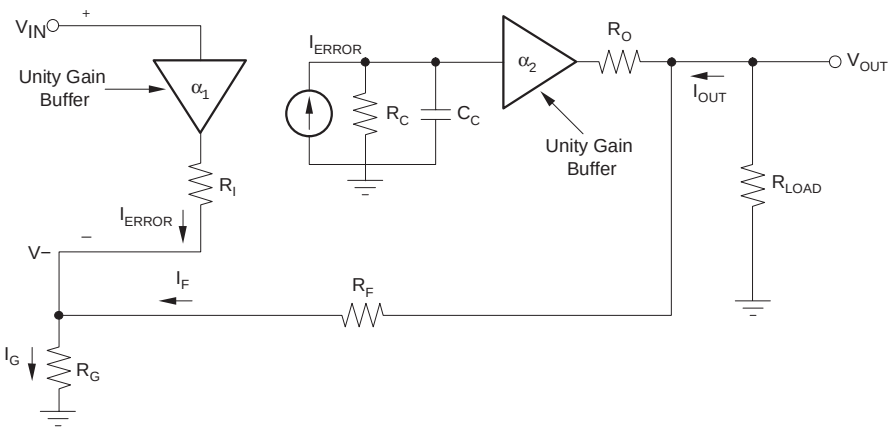

Figure 1. First-Generation Current-Feedback Op Amp Model

Figure 1 shows a first-order, closed-loop circuit model with a noise gain (NG) for a CFB amplifier, where noise gain is the amplifier closed-loop gain; in this case, NG = $\left\{1+\frac{R_F}{R_G}\right\}$.

Here the model includes the external resistive load and feedback network. Also shown is the output stage resistance for each of the two buffer stages. Writing the node equations to include these values helps us to understand the dependence effects of those terms for the open-loop frequency response.

$$I_{error} = I_G - I_F \tag{1}$$

$$I_{error} = \frac{V^-}{R_G} - \frac{V_{out} - V^-}{R_F} \tag{2}$$

$$V_{out} = I_{error}\left(\alpha_2 \cdot Z_{(s)}\right) - I_F \cdot R_O \tag{3}$$

$$V^- = \alpha_1 \cdot V_{in} - I_{error} \cdot R_I \tag{4}$$

Rearranging the terms for the closed-loop CFB amp transfer function generates the following:

$$\frac{V_{out}}{V_{in}} = \frac{\alpha_1\left(1+\frac{R_F}{R_G}\right)}{1+\frac{R_F+R_I\left(1+\frac{R_F}{R_G}\right)+R_O\left(1+\frac{R_I}{R_G}\right)}{\alpha_2 \cdot Z_{(s)}}} = \frac{\alpha_1 NG}{1+\frac{R_F+R_I NG+R_O\left(1+\frac{R_I}{R_G}\right)}{\alpha_2 \cdot Z_{(s)}}} \tag{5}$$

$$NG = \left(1+\frac{R_F}{R_G}\right) \tag{6}$$

$$Z_{(s)} = \frac{R_c}{sR_cC_c+1} \tag{7}$$

where $\alpha_1, \alpha_2 \approx 1$.

At low frequencies, $Z_{(S)}$ forces the denominator to approach 1; the numerator gain (defined as NG) is unaffected by gain-bandwidth changes. Again, one can see how the denominator is the absence of frequency or Gain-Bandwidth Product. Here, the bandwidth is only affected by the feedback resistor R_F, and the output resistor terms of the buffer.

Although these values are small, R_I (the input buffer amplifier output impedance) and R_O (output buffer output impedance) do affect the loop gain bandwidth. If these terms approach 0 and α is equal to 1, then the bandwidth dependence is strictly the result of $Z_{(S)}$ and R_F.

TI has improved this amplifier architecture by lowering R_I through the addition of a closed-loop input buffer amp. Thus, the R_I term is now reduced by a factor of 10, allowing for a lower inverting output impedance and improved performance in gain-bandwidth selections for a given bandwidth. This improved topology enables CFB op amps to be more suitable for multiple gain designs while maintaining a fairly constant signal bandwidth. The output buffer impedance is also reduced through similar techniques. Therefore, the output is 0Ω up to the point where the loop gain starts to decrease in value; then the impedance rises.

Figure 2 shows a circuit model with a closed-loop buffer.

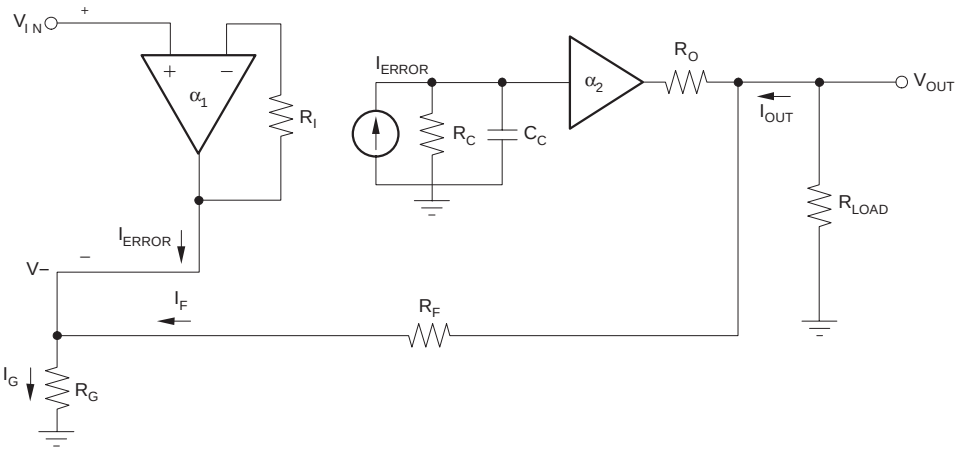

Figure 2. TI Current-Feedback Op Amp Model

With the output resistor $R_O \rightarrow 0$, the following series of equations show the transfer function for this new OPA series amplifier.

$$I_{error} = I_G - I_F \tag{8}$$

$$I_{error} = \frac{V^-}{R_G} - \frac{V_{out} - V^-}{R_F} \tag{9}$$

$$V_{out} = I_{error}\left(\alpha_2 \cdot Z_{(s)}\right) - I_F \tag{10}$$

$$V^- = \alpha_1 \cdot V_{in} - I_{error} \cdot R_I \tag{11}$$

Substituting and reducing the terms, the closed-loop transfer function is derived for the CFB amp.

$$\frac{V_{out}}{V_{in}} = \frac{\alpha_1\left(1 + \frac{R_F}{R_G}\right)}{1 + \frac{R_F + R_I\left(1 + \frac{R_F}{R_G}\right)}{\alpha_2 \cdot Z_{(s)}}} = \frac{\alpha_1 NG}{1 + \frac{R_F + R_I NG}{\alpha_2 \cdot Z_{(s)}}} \tag{12}$$

where R_I is the closed-loop output impedance but much smaller than previous CFB topologies on the order of 2Ω to 3Ω.

$$NG = \left(1 + \frac{R_F}{R_G}\right) \tag{13}$$

$$Z_{(s)} = \frac{R_c}{sR_cC_c + 1} \tag{14}$$

where $\alpha_1, \alpha_2 \approx 1$.

Once again, however, this is a first-order system, and does not have much relevance upon calculating stability and selecting the value of R_F for good phase margin.

2.1 CFB Model with 2nd-Order Pole

Current feedback for a CFB op amp $Z_{(s)}$ is derived from the internal capacitance, C_C, and the internal transimpedance gain resistor when R_C sets a high-frequency open-loop response. The transistor's parasitic capacitance and impedance introduce 2nd- and 3rd-order poles at high frequencies within the amplifier by R_2 and C_2. Those poles are generally several orders of magnitude higher than the first pole. The model shown in Figure 3 includes only a 2nd-order pole in order to help demonstrate selection of the feedback resistor, R_F.

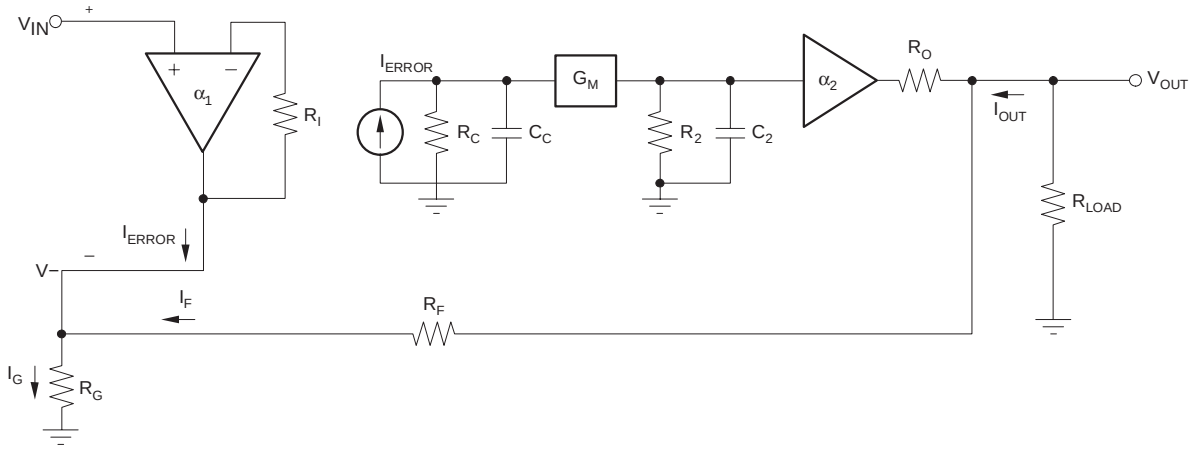

Figure 3. 2nd-Order CFB Model

$$\frac{V_{out}}{V_{in}} = \frac{\alpha_1\left(1 + \frac{R_F}{R_G}\right)}{1 + \frac{R_F + R_I\left(1 + \frac{R_F}{R_G}\right)}{\alpha_2 \cdot Z_{1(s)} \cdot G_M \cdot Z_{2(s)}}} = \frac{\alpha_1 NG}{1 + \frac{R_F + R_I NG}{\alpha_2 \cdot Z_{1(s)} \cdot G_M \cdot Z_{2(s)}}} \tag{15}$$

where $\alpha_{1 \text{ and }} \alpha_2 \approx 1$, but an additional pole is created:

$$Z_{2(s)} = \frac{1}{sR_2C_2 + 1} \tag{16}$$

and G_M is equal to $\frac{1}{R_2}$.

3 Setting CFB Stability Through Bode Analysis

Bode analysis is a common method to determine stability for any feedback amplifier or system. The amplifier is designed to have a minimal gain stability point, set by the designer of the amplifier. This point is referred to as the amplifier's *phase and gain margin*. Therefore, CFB amplifiers will always have a minimum stability point of operation, set by a recommended feedback resistor value found in the data sheet.

One can determine the phase and gain margin of a CFB op amp by applying Bode analysis. This measurement is calculated by creating an open-loop magnitude and phase plot, and then deriving the gain and phase margin. These procedures are easily done with any Spice™ program (in this case, PSpice) to simulate a TI-generated macro model for a CFB amplifier. Figure 5 shows a typical circuit measurement technique to generate the open-loop gain and phase margin and the closed-loop response.

The phase margin is derived by finding the closed-loop gain frequency intersection on the open-loop gain plot frequency roll-off, as shown in Figure 4. At the same time, plotting the phase function allows one to apply the same frequency scale for measuring the phase margin of the amplifier. The value is read from the phase plot while looking at the point where the amplifier's −3dB line intersects the frequency gain plot on the curve. Taking this phase value and subtracting it from 180° results in the amplifier's phase margin. (See Figure 4). As can be seen from the macro-models, CFB amplifiers generally have a phase margin between 60° to 65° to allow for a very flat frequency response. This characteristic is more fully explained later in this application note.

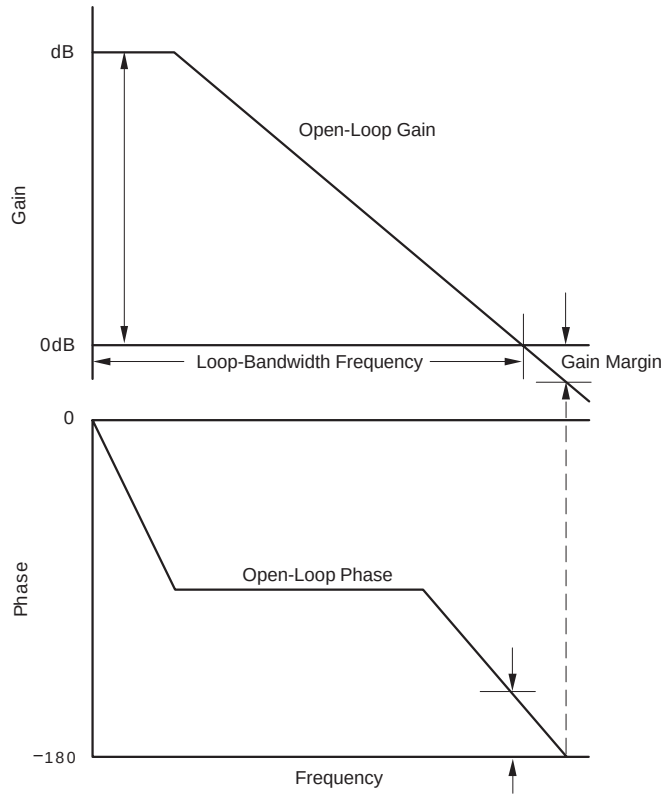

Figure 4. Typical Bode Plot

3.1 Generating an Open-Loop Transimpedance Plot

Generating the Bode plots for a CFB amplifier is easily done through PSpice by placing a dummy voltage source between the inverting node of the amplifier and the point where R_G and R_F tie together. Figure 5 shows this placement.

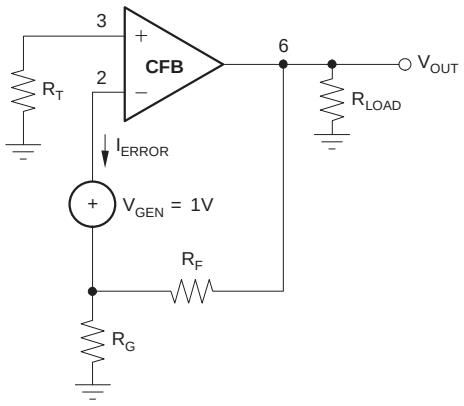

Figure 5. Open-Loop Simulation Model

Recall from the model that the error current times the internal open loop gain $Z_{(s)}$ gives an output voltage, V_O; or, more simply, divide the output V_O by $I(V_{GEN})$. Using either method results in the value for $Z_{(s)}$, which includes both low-frequency and higher order poles of the model. As mentioned before, $Z_{(s)} = \frac{1}{sR_1C_1 + 1}$ creates an internal 1st-order pole for a CFB; therefore, the plot looks very similar to Figure 6.

By dividing V_O/I_{ERROR}, the plot of $Z_{(s)}$ is shown for an OPA684, where:

$s = j\omega$, and $\omega = 2\pi f$

with *f* as the frequency sweep of the amplifier. Compared to the OPA684 product data sheet, this plot matches the *Open-Loop Transimpedance* typical characteristic plot shown on Page 8.

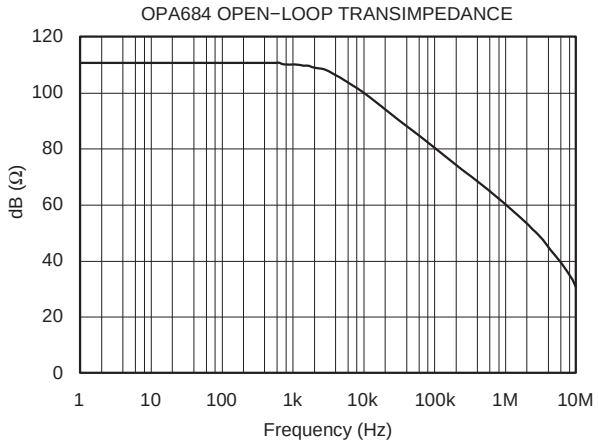

Figure 6. Open-Loop Transimpedance for the OPA684

Figure 6 also shows that the Open-Loop Transimpedance plot for a CFB amp has units of resistance, or dBΩ. The overall gain at dc in ohms is very high; in the case of the OPA684, for example, it is 355KΩ. The amplifier has an initial pole at several kHz, which is set by the compensation network and values of R_C. R_C is derived by taking the inverse log of the magnitude value at low frequencies from the Y axis, or:

$$R_C = 10^{\frac{Z_{(s)}}{20}} \tag{17}$$

The value of the 1st-order pole then has a capacitor value of:

$$C_C = \frac{1}{2\pi R_C \cdot f_{-3db}} \tag{18}$$

or 1.375pF.

3.2 Plotting R_F and Determining Closed-Loop Response

By simplifying Equation 15 (derived earlier), one can solve for values of R_F.

$$\frac{V_{out}}{V_{in}} = \frac{Z_{(s)} \cdot NG}{Z_{(s)} + R_F + R_I \cdot NG} \tag{19}$$

where

$$NG = \left(1 + \frac{R_F}{R_G}\right), Z_{1(s)} = Z_{1(s)} \cdot G_M \cdot Z_{2(s)} \tag{20}$$

Plotting the closed-loop response for a CFB amp on the same graph as the open-loop response is accomplished through the following process:

1. Take the Output voltage times the denominator term $R_F + R_I \cdot NG$, then
2. Subtract the closed-loop gain.

This process is shown in Equation 21:

$$20\log(V_{OUT}) + 20 \cdot \log(R_F + R_I \cdot NG) - 20\log(NG) \tag{21}$$

or in PSpice DB($V_{(6)}$) + DB(1005) − 6, as shown in Figure 7.

Then, subtract the noise gain in dB. For PSpice, this allows you to overlay the closed-loop response over the open-loop response. These responses agree with the data sheet specification. For the OPA684, to determine the −3dB bandwidth for a 2nd-order system with a Q = 0.707 has a crossover frequency intersection of 114MHz on the combined plots.

To find the −3dB frequency, multiply by a constant term based upon Q, which in this case is $\left(\sqrt{2}\right)$:

$$1.41 \cdot 114MHz = 160MHz$$

where f_C is the crossover frequency (114MHz) and the −3dB frequency for the OPA684 is 160MHz, which agrees with the specification stated in the product data sheet.

This −3dB frequency is the point at which the amplifier's phase margin is derived for measuring the phase margin in the chart. For TI OPA parts, the high-speed amps target a phase margin between 60−65°. For this example, the phase margin measures 65°. If the CFB amp is designed for a gain of 1, then R_G is left open or set to ∞, and the equation reduces to a closed-loop transfer or feedback resistor, R_F.

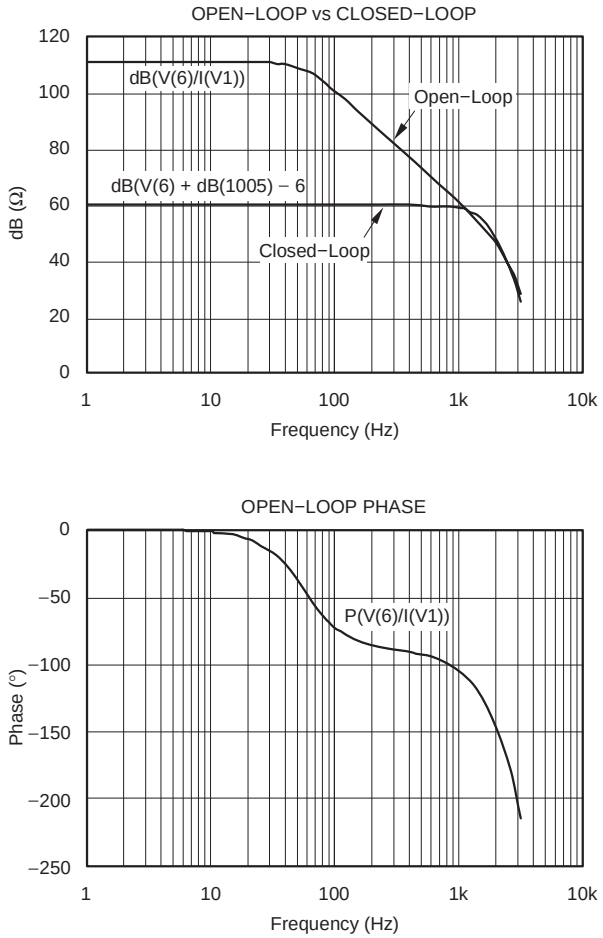

Figure 7. Open-Loop and Closed-Loop Stability Plots for the OPA684

Keep in mind that as the Q increases (or peaking appears), then the constant value $\left(\sqrt{2}\right)$ that multiplies the intersection of the open-loop and closed-loop crossover frequency ($f_{C)}$ changes; therefore, the point where the −3dB frequency and the amplifier's phase are measured will be slightly different. For general cases where the order is different, the f_C can be multiplied by the values shown in Table 1 in order to determine the correct −3dB frequency.

Table 1. Filter Orders

Filter Order	(Constant)·(f_C)
1	(1.57)·f_C
2	(1.11)·f_C
3	(1.05)·f_C

We can find the value of the second capacitor for our model developed previously by the equation below:

$$F_2 = 10 \cdot f_{-3db} \tag{22}$$

where F_2 is the second pole frequency.

It is important to note that CFB amps are generally designed with low value feedback resistors R_F. Therefore, increasing the feedback resistor decreases the bandwidth as well as the closed-loop to open-loop ratio. It also affects the noise by increasing the overall noise for the designed circuit. In some cases, using R_F to slightly improve stability is acceptable. Keep in mind, however, that other affected parameters should be checked to verify that the design meets its overall goals.

4 Correlating the Time Domain to Frequency Analysis

Examining the frequency response is a difficult task without using a network analyzer for measurement. Generally, a lab has an oscilloscope and signal generator available, so it is often easier to measure the time domain response. Therefore, understanding the relationship between a time domain step-function and frequency response is an important tool when evaluating high-speed amplifiers. In practice, such a correlation is generally linear and has a proven design through simulation or some other means of characterization. One acceptable way to determine stability in a given application is to apply a step excitation that is low enough in frequency to allow measurable results.

High-speed amplifiers are designed and analyzed using both frequency and time domain sources. Each amplifier is optimized for these internally-generated, non-linear terms, so that the amplifier behaves properly under a broad spectrum of applications. What commonly happens, though, is that the original stability margin of the amplifier can be degraded, producing unwanted results, when the amp is driving a capacitive load, a reactive feedback-network, a complex input source, or inductances in the supply lead. At this point, the stability of the circuit needs to be verified.

For this application report, we define the resonant peaking M_R for the frequency response plot as the amount of peaking from the low frequency gain (in dB); this is usually measured using a network analyzer. This number is also associated with Q, or the damping factor. Table 2 shows the relationship of frequency peaking in M_R to the time domain overshoot for a given phase margin (ϕ_M) in degrees as functions of Q, or damping factor.

Table 2. Stability for 2nd-Order Systems

Phase Margin (ϕ_M)	Resonant Peaking (M_R)	Relative Overshoot (A_P)	Q	Normalized Resonant Frequency (F_R/F_C)	Normalized Time of Overshoot ($w_C t_{P1}$)
90°	–	–	0.00	–	–
85°	–	–	0.296	–	–
80°	–	–	0.423	–	–
75°	–	0.0%	0.527	–	9.96
70°	–	1.4%	0.623	–	5.27
65°	0.0dB	4.7%	0.717	0.168	4.38
60°	0.3dB	8.8%	0.817	0.501	3.97
55°	0.8dB	13.3%	0.924	0.644	3.74
50°	1.5dB	18.1%	1.050	0.737	3.58
45°	2.3dB	23.3%	1.190	0.804	3.46
40°	3.3dB	28.9%	1.362	0.855	3.38
35°	4.4dB	35.0%	1.577	0.894	3.31
30°	5.7dB	41.6%	1.859	0.925	3.26
25°	7.3dB	48.9%	2.252	0.949	3.22
20°	9.2dB	56.9%	2.841	0.969	3.19
15°	11.7dB	65.9%	3.788	0.982	3.17
10°	15.2dB	75.9%	5.747	0.992	3.15.
5°	21.2dB	87.2%	11.364	0.998	3.14
0°	∞	100%	∞	1	π

The relative stability of a 2nd-order operation for a closed-loop gain, based upon the equation:

$$G = \frac{G_1}{1 + \frac{s}{Q\omega_n} + \frac{s^2}{\omega^2_n}} \tag{23}$$

with $s = j\omega$, $\omega = 2\pi f$, G = output, G_1 = input, ω_n = natural frequency of interest, and Q is the amount of peaking given in the resonant peaking, M_R (dB). (M_R is defined as shown in Figure 9.)

Plotting the peaking and overshoot versus ϕ_M generates a curve that allows one to extract the relationship between the two measurements systems, as seen in Figure 8. The equations to plot these curves are described below.

$$\text{Peaking (dB)} = M_F = 20 \cdot \text{Log}\left[\frac{Q}{\sqrt{1 - \left(\frac{1}{2Q}\right)^2}}\right] \tag{24}$$

$$\phi_M = 90^0 - \arctan\left[\frac{Q}{\sqrt{\sqrt{\left(\frac{1}{Q^4}\right) + 1} + \frac{1}{Q^2}}}\right] \tag{25}$$

$$\frac{V_O(t)}{V_i} = A_P = \left[1 - \frac{e^{\frac{-\omega_n \cdot t}{2Q}}}{\sqrt{1 - \left(\frac{1}{2Q}\right)^2}} \cdot \sin\left[\omega_n \cdot \sqrt{\left(1 - \left(\frac{1}{2Q}\right)^2\right)} \cdot t + \arccos\left(\frac{1}{2Q}\right)\right]\right] \times 100 \quad (26)$$

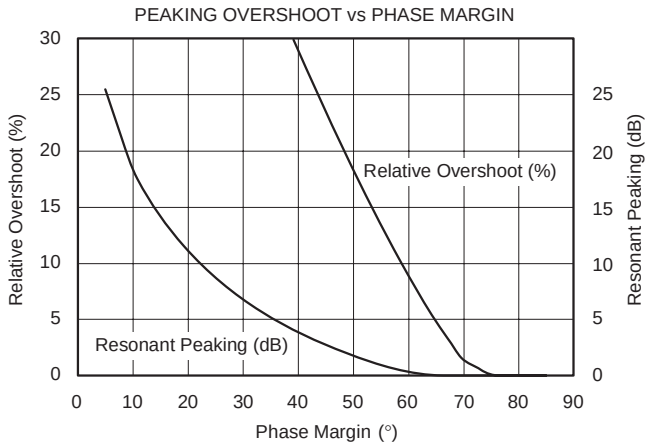

Figure 8. Peaking—Overshoot vs Phase Margin

The relative overshoot curve fits a polynomial equation that can be used to predict the amount of overshoot for a given phase margin. For relative overshoot, the equation for the plot lines is:

$$y = -1^{-06x3} + 0.0002x2 - 0.0258x + 0.9965 \quad (27)$$

so for a given value of phase margin the amount of overshoot (y) can be calculated.

As seen in Figure 9, the greater the amount of Q, the more peaking there is present in the frequency response. As the peaking increases to greater than 10dB in the frequency response, the amplifier becomes marginally stable and can oscillate if a step function is applied to the input.

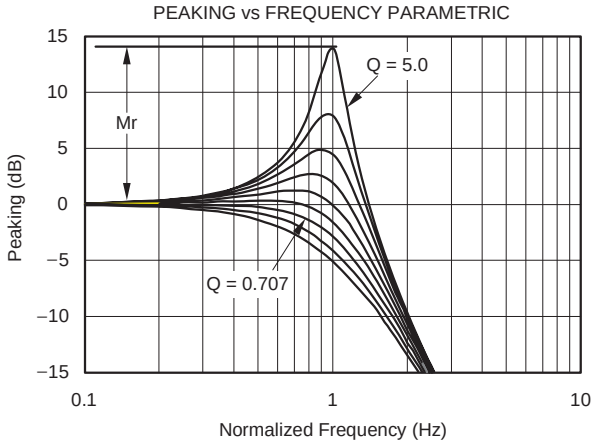

Figure 9. Frequency Peaking vs Q

In Figure 10, time domain applications often require rising and falling edges that are as fast as possible. In this case, more slightly higher Q might be acceptable.

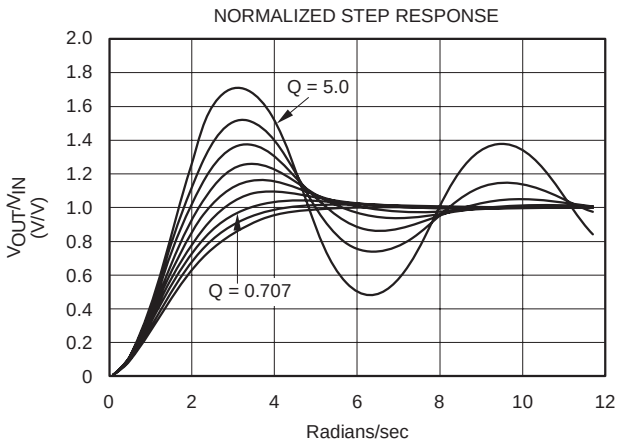

Figure 10. Time Step for Delta Change in Q

5 CFB Amplifiers and Noise

When using an amplifier, the question of how much noise the amplifier adds to the signal is of equal importance as stability. Although the noise analysis is the same for VFB and CFB op amps, a CFB amp has unequal input current noise terms that are often overlooked in the selection or design processes. This oversight occurs because designers tend to select a given voltage feedback for a simpler design, and then select high-value external components that end up adding more noise to the circuit design. Understanding the amplifier topologies can be a positive factor in designing low-noise circuits. Selecting low-value resistors first assures that lower thermal noise will be added to the overall circuit noise. Since multiple noise sources are present, the individual contributions add up differently, as shown in the circuit diagram of Figure 11.

Additionally, since noise is described in terms of power, the noise terms can be added by the sum of their squares. For non-inverting and inverting inputs, the contributions add to the overall noise differently. For the CFB amplifier, larger values of R_F will not only increase the thermal noise, but also increases the overall noise by the current noise term I_{bi}. This is also true for the non-inverting input term, which depends upon R_{in} and I_{bn}. Therefore, lowering resistor values also reduce the overall noise terms.

$$e_{NO}^2 = \left[e_{ni}^2 + \left(i_{bn}R_{in}\right)^2 + 4kTR_{in}\right] \cdot NG^2 + \left[\left(i_{bi}R_F\right)^2 + \left(4kTR_F\right) \cdot NG\right] \quad (28)$$

$$e_{R_T} = \sqrt{4kTR(BW)} \quad (29)$$

where:

k = Boltzmann's constant = 1.38×10^{-23} J/°K

T = °Kelvin

R = resistor

4kT = 16×10^{-21} Joules at T = 290°K

BW = the bandwidth of the signal path or measurement system. As an example of how much noise a resistor creates, calculating for a 1KΩ resistor obtains a noise value of:

$$e_{R_T} = \frac{4.0nV}{\sqrt{Hz}}$$

with a 1Hz bandwidth at room temperature.

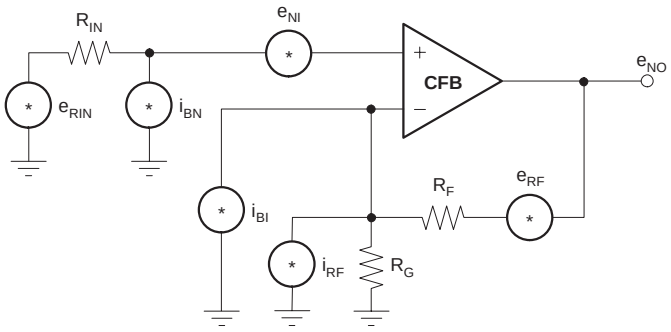

Figure 11. Noise Model for CFB

However, making this selection is not as simple as it appears. Many amplifiers are limited in their selection of resistor values due to the output drive capability, or in some cases the distortion specifications, which require larger loads for better performance. Thus, the load as seen from the output pin of the amplifier is the combination of the feedback components in parallel with the actual load connected to the output pin. This feature shows that careful attention needs to be given to the amplifier's output current and voltage swing limitations.

In any amplifier design, the key is to make the independent noise values and components small enough so that the amplifier noise is the result of one term, e_{in}, or voltage noise.

$$\frac{e_{NO}}{NG} = e_{in\ Total} = \sqrt{\left[e_{ni}^2 + \left(i_{bn}R_{in}\right)^2 + 4kTR_{in}\right] + \left[\frac{\left(i_{bi}R_F\right)^2}{NG^2} + \frac{\left(4kTR_F\right)}{NG}\right]} \quad (30)$$

Changing the previous output noise equation into an input-referred noise equation helps to clarify the components that dominate. If R_{in} and I_{bn} are small, then these terms can be ignored. Making the amplifier gain larger forces contribution magnitude of the last two terms lower, leaving only e_{ni}. For CFB amps (just as with VFB amps), using the amplifier in an inverting state versus a non-inverting state lowers the overall noise by eliminating both I_{bn} and R_{in}, if the non-inverting pin is grounded. Figure 12 shows a plot of total input-referred noise multiplied by the gain. Notice that when all the noise is added and input-referred, the noise is higher at low gains, approaching a minimum threshold at high gains.

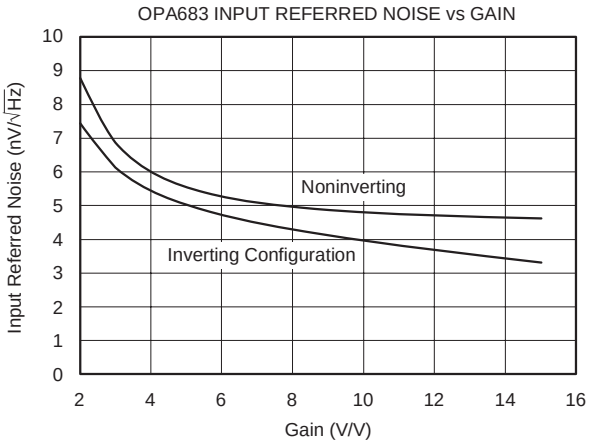

Figure 12. Noise Plot vs Gain (OPA683)

6 External Parasitic Components from PCBs and Complex Loads

CFB amps do have limitations in terms of feedback configurations, since the feedback resistor determines the amplifier's stability. Circuit configurations such as differentiation, gain blocks for filtering, or driving certain loads, however, work equally well for CFB amps.

Laying out components on printed circuit boards (PCBs) introduces parasitic effects that can often move the phase margin of the CFB op amp enough to alter its performance. One solution to this problem is to follow the evaluation board layout supplied by the CFB amp vendor. A second method is to measure the existing PCB critical traces, add the parasitic component values in a simulation, and re-adjust the amplifier's phase margin. Measuring trace values is discussed in application note SBOA094, *Measuring Board Parasitics in High-Speed Design* (available for download at www.ti.com).

As an example, a small capacitance referenced to ground on the non-inverting input can significantly change the peaking in a time domain plot. The circuit in Figure 13 shows the OPA695 at a gain of two, but with capacitance referenced to ground on the inverting input.

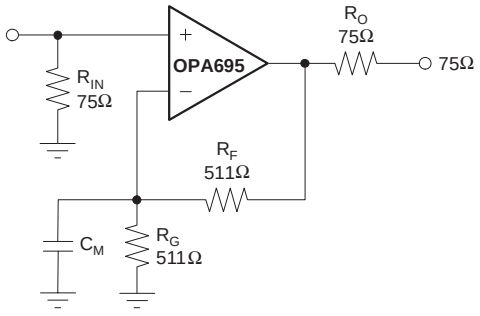

Figure 13. Parasitic Capacitance on Inverting Input

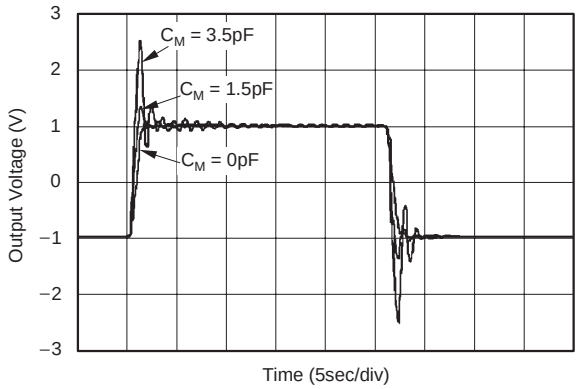

Figure 14. Step-Function of OPA695

Placing the traces for the feedback resistor R_F and R_G over a large area of ground (or power) plane will create unwanted capacitance at the inverting pin. This undesirable capacitance, in turn, affects the stability of the amplifier as seen in the time domain plot of Figure 14.

One way to avoid this effect is by removing any power and ground planes that might be in parallel with critical signal traces. (See the evaluation boards and layout instructions for additional ideas.) One of the biggest sources of instability for high-speed amplifiers is the improper decoupling of the power supply pins. The amount of inductance seen looking from the amplifier pins to the power supply increases the high-impedance return path for the signal. Also, keep in mind that the best return path is the lowest inductive path from the load to the power pins. Placing any recommended decoupling capacitors immediately off the amplifier power pins is mandatory for high-speed design and provides a short for the signal path return.

Another way to optimize this circuit is to adjust the feedback resistor. Using the previously developed procedure, a user can include the stray capacitance and increase the feedback resistor value for additional phase margin. This is done by lowering the closed-loop to open-loop ratio, increasing the noise slightly, and finally giving up bandwidth.

7 External Circuits

Although a differentiator is a popular circuit design, the circuit should be analyzed when using CFB amplifiers in order to properly adjust the phase margin. A typical differentiator topology is shown in Figure 15, and places a capacitor in the place of R_G.

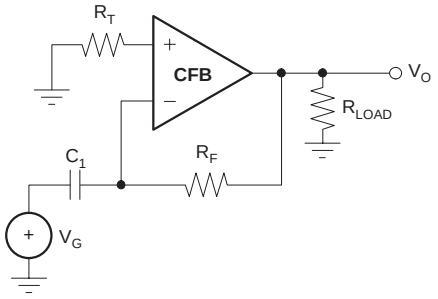

Figure 15. Differentiator CFB Op Amp

The transfer function is simply:

$$V_O = -C_1 \cdot R_F \frac{dV_G}{dt} \quad (31)$$

but often this circuit will oscillate at a frequency of

$$f_D = \frac{1}{2\pi C_1 R_F} \quad (32)$$

as the differentiator characteristic frequency, which corresponds to a lag network of $R_F C_1$ in the feedback path. The differentiator tends to behave as a heavily under-dampened operational circuit with a dampening ratio of

$$Q = 1/2 \sqrt{\left(\frac{f_D}{f_t}\right)}.$$

The problem with this circuit is that as Q increases, a phase shift prior to the stability of the amplifier 0dB crossover point occurs; therefore, the circuit oscillates at f_C frequency.

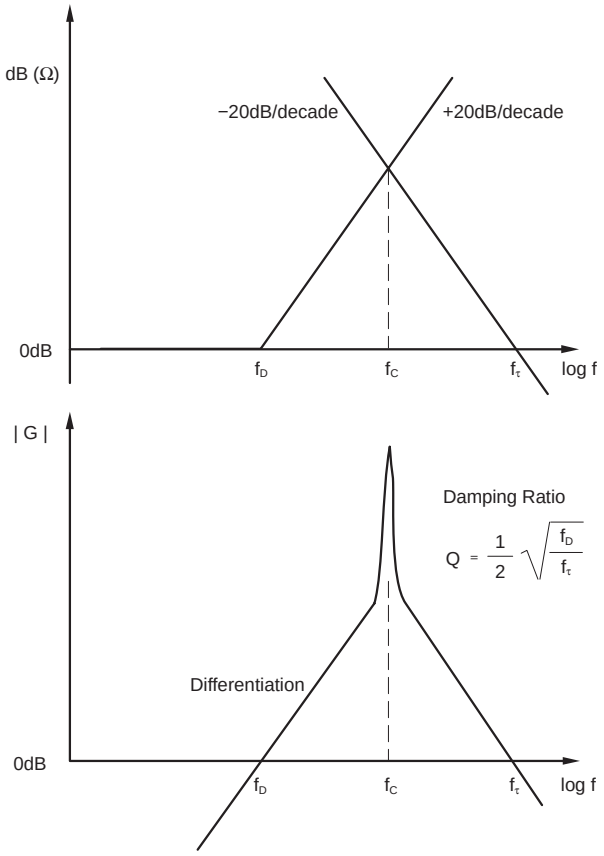

Figure 16. Differentiator Stability Plots

The resolution for this problem is to limit the gain by inserting resistor R_1. The differentiation is now limited by a gain set with the R_F and R_1 resistors. Figure 17 shows the OPA684 used as a differentiator with no series R resistance. The part oscillates as expected.

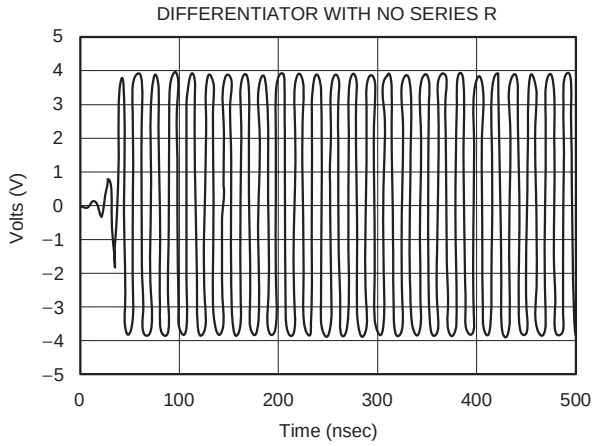

Figure 17. Oscillating Differentiator for CFB

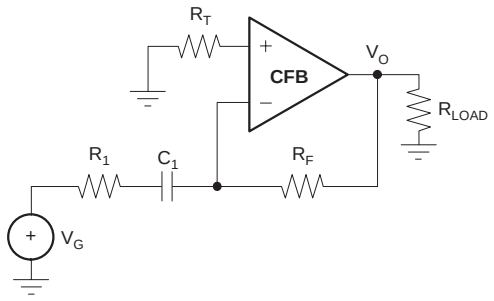

Figure 18. Stable Differentiator for CFB

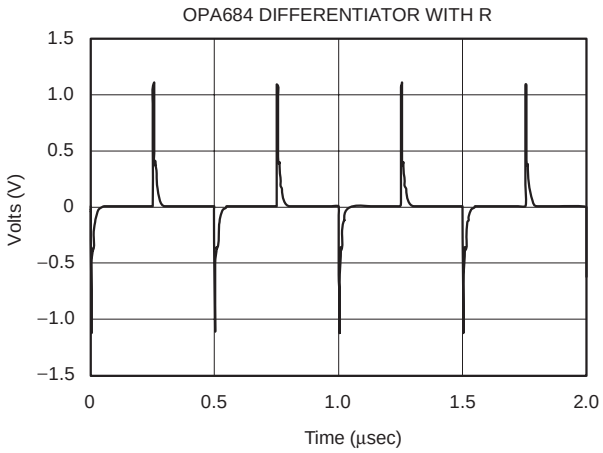

Figure 19. Time Domain Plot of Good Differentiator

For a CFB amplifier, adjusting the feedback circuit stabilizes the design. The plot of Figure 20 shows the OPA684 with a capacitor value of 1000pF, R_G of 20.48, and a feedback resistor R_F of 1K. The circuit oscillates at the f_c value. Increasing the feedback resistor to 5K and 10K shows the overdampened condition and the best solution for the design.

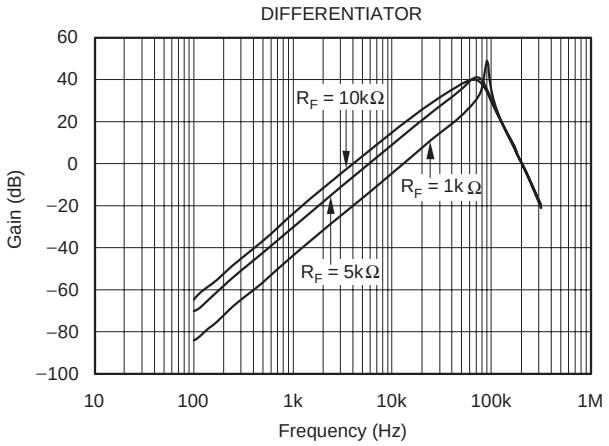

Figure 20. Frequency Response Differentiator

8 Driving Capacitive Loads

Another typical application for high-speed amplifiers is to drive capacitive loads. Occasionally, these loads are cables with a characteristic impedance; at other times, these occur with a capacitive load from a long trace on a PCB. When the capacitance at the output of the amplifier is included, the previously-derived equations are altered and the stability of the amplifier is changed dramatically. A typical circuit configuration might look like Figure 21 below.

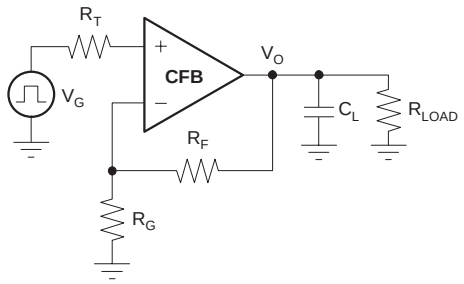

Figure 21. CFB Driving Capacitive Load

When driving a capacitive load, one finds the circuit in Figure 21 will oscillate or ring. This ringing is due to a phase shift caused by the capacitor effect upon the closed-loop stability point. The equation for the closed-loop is altered by the following additional pole, as shown in Figure 22 and Equation 33.

$$\frac{V_{out}}{V_{in}} = \frac{NG}{1 + \frac{R_F}{Z_{(s)}}} \cdot \frac{1}{C_L \frac{R}{a}} \cdot \frac{1}{s + \frac{1+a}{RC_L}} \tag{33}$$

If the NG = 2, then the equation implies that a = 1 and the Rs are equal, as well. This is equivalent to 0% overshoot. As the noise gain is changed, then the ratio of the resistors will need to be changed to maximize the step response. This shift assumes the amplifier phase margin is already optimized for the load.

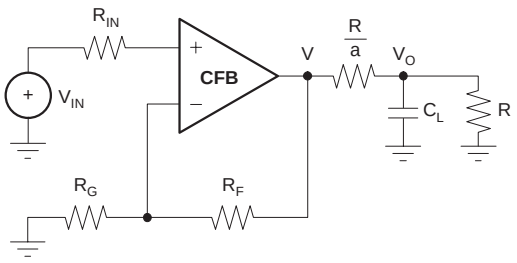

Figure 22. Stable CFB for Driving Capacitive Load

Summary

In summary, CFB op amps cannot replace all circuit applications where standard VFB op amps are implemented. There are certain applications, however, where CFBs will give greater freedom for optimizing for a particular set of design parameters. As an example, for time domains where settling is an issue, a CFB can be used with an R_F resistor to maximize the settling time, while independently adjusting the gain R_g. At high frequencies, where distortion specifications are hard to achieve for large signal swings, CFB amps will do better than VFB amps. Lastly, for designs driven by S/N ratio, a CFB can be considered; but for extremely low-noise applications, a VFB amp is usually a better choice for lowest overall noise.

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