Analog Engineer's Circuit

AC Coupled Instrumentation Amplifier Circuit

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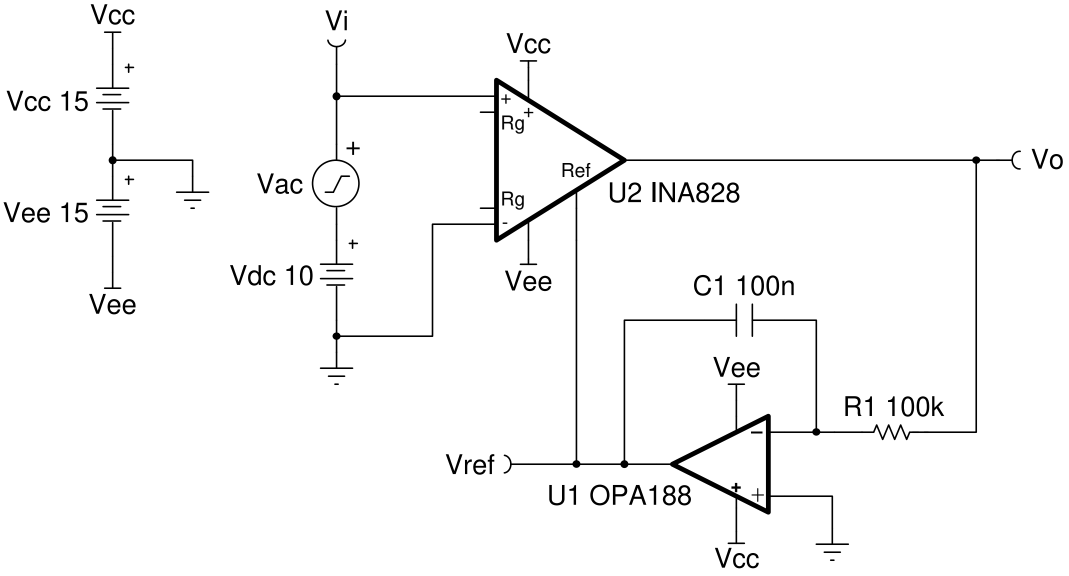
Design Goals

Input		Output		Supply	
V_{iMin}	V_{iMax}	V_{oMin}	V_{oMax}	V_{cc}	V_{ee}
–13V	13V	–14.85V	14.85	15	–15

Lower Cutoff Frequency (f_L)	Gain	Input
16Hz	1	±2VAC; +10VDC

Design Description

This circuit produces an AC-coupled output from a DC-coupled input to an instrumentation amplifier. The output is fed back through an integrator, and the output of the integrator is used to modulate the reference voltage of the amplifier. This creates a high-pass filter and effectively cancels the output offset. This circuit avoids the need for large capacitors and resistors on the input, which can significantly degrade CMRR due to component mismatch.



Design Notes

1. The DC correction from output to reference is unity-gain. U_1 can only correct for a signal within its input/output limitations, thus the magnitude of DC voltage that can be corrected for degrade with increasing instrumentation amplifier gain. See the table in Design Steps for more information.
2. Large values of R_1 and C_1 lower the cutoff frequency, but increase start up transient response time. Start up behavior is observed in the Transient Simulation Results.
3. When AC-coupling this way, the total input voltage must remain within the common-mode input range of the instrumentation amplifier.

Design Steps

1. Set the lower cutoff frequency for circuit (integrator cutoff frequency). The upper cutoff frequency is dictated by the gain and instrumentation amplifier bandwidth.

$$f_L = \frac{1}{2\pi \times R_1 \times C_1} = 16\ \text{Hz}$$

2. Choose a standard value for R_1 and C_1.

$$C_1 = 100\ \text{nF}$$

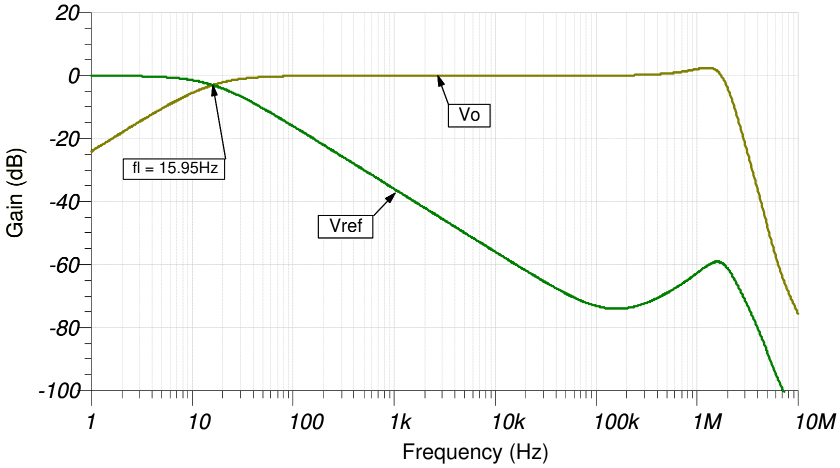
$$R_1 = \frac{1}{2\pi \times 100\ \text{nF} \times 16\ \text{Hz}} = 99.47\ \text{k}\Omega \approx 100\ \text{k}\Omega \quad (\text{standard} \quad \text{value})$$

3. The DC rejection capabilities of the circuit degrade with gain. The following table provides a good estimate of the DC correction range for higher gains.

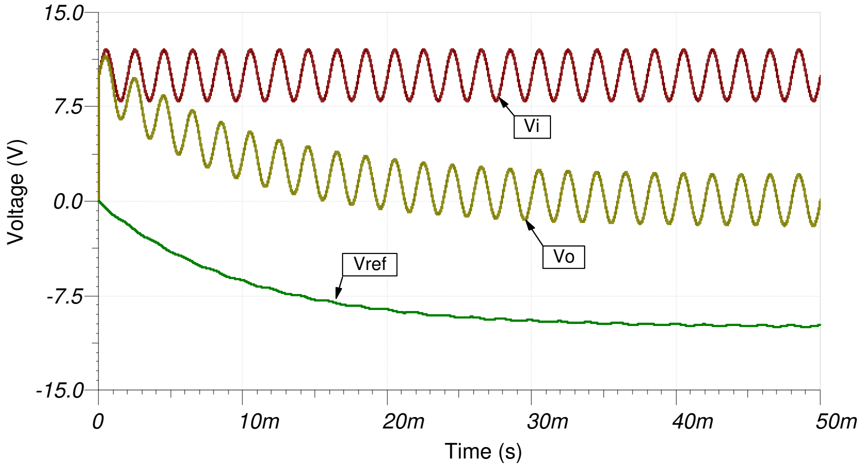
Gain	DC Correction Range
1V/V	±10V
10V/V	±1V
100V/V	±0.1V
1000V/V	±0.01V

Design Simulations

AC Simulation Results



Transient Simulation Results



Design References

Texas Instruments, *SBOMAU0 TINA-TI™ circuit simulation*, file download

Texas Instruments, *TIPD191 Instrumentation Amplifier with DC Rejection*, reference design

Design Featured Instrumentation Amplifier

INA828	
V_{ss}	4.5V to 36V
V_{inCM}	V_{ee}+2V to V_{cc}–2V
V_{out}	V_{ee}+150mV to V_{cc}–150mV
V_{os}	20μV
I_q	600μA
I_b	150pA
UGBW	2MHz
SR	1.2V/μs
#Channels	1
INA828	

Design Featured Op Amp

OPA188	
V_{ss}	8V to 36V
V_{inCM}	V_{ee} to V_{cc}–1.5V
V_{out}	Rail-to-rail
V_{os}	6μV
I_q	450μA
I_b	±160pA
UGBW	2MHz
SR	0.8V/μs
#Channels	1, 2, and 4
OPA188	

Design Alternate Op Amp

TLV171	
V_{ss}	2.7V to 36V
V_{inCM}	V_{ee}–0.1V to V_{cc}–2V
V_{out}	Rail-to-rail
V_{os}	750µV
I_q	525µA
I_b	±10pA
UGBW	3MHz
SR	1.5V/µs
#Channels	1, 2, and 4
TLV171	

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