DRV425-Q1 Functional Safety FIT Rate, FMD and Pin FMA

1 Overview

This document contains information for DRV425-Q1 (WQFN-20 package) to aid in a functional safety system design. Information provided are:

- Functional Safety Failure In Time (FIT) rates of the semiconductor component estimated by the application of industry reliability standards
- Component failure modes and their distribution (FMD) based on the primary function of the device
- Pin failure mode analysis (Pin FMA)

Figure 1 shows the device functional block diagram for reference.

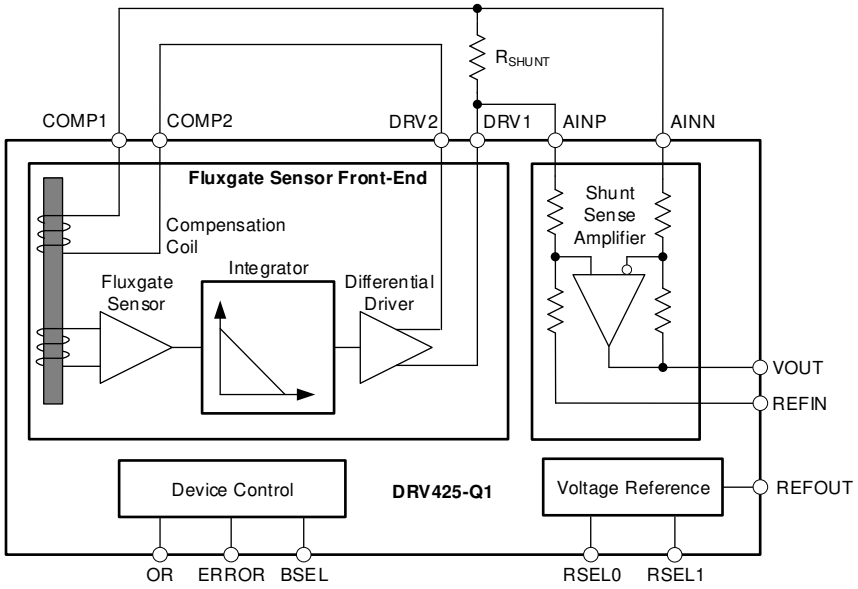

Figure 1. Functional Block Diagram

DRV425-Q1 was developed using a quality-managed development process, but was not developed in accordance with the IEC 61508 or ISO 26262 standards.

2 Functional Safety Failure In Time (FIT) Rates

This section provides Functional Safety Failure In Time (FIT) rates for DRV425-Q1 based on two different industry-wide used reliability standards:

- Table 1 provides FIT rates based on IEC TR 62380 / ISO 26262 part 11
- Table 2 provides FIT rates based on the Siemens Norm SN 29500-2

Table 1. Component Failure Rates per IEC TR 62380 / ISO 26262 Part 11

FIT IEC TR 62380 / ISO 26262	FIT (Failures Per 10^9 Hours)
Total Component FIT Rate	11
Die FIT Rate	1
Package FIT Rate	10

The failure rate and mission profile information in Table 1 comes from the Reliability data handbook IEC TR 62380 / ISO 26262 part 11:

- Mission Profile: Automotive Control
- Power dissipation: 35 mW
- Climate type: World-wide Table 8
- Package factor: Lambda 3 Table 17b
- Substrate Material: FR4
- EOS FIT rate assumed: 0 FIT

Table 2. Component Failure Rates per Siemens Norm SN 29500-2

Table	Category	Reference FIT Rate	Reference Virtual T_J
5	BICMOS Analog mixed < 50V	25 FIT	55°C

The Reference FIT Rate and Reference Virtual T_J (junction temperature) in Table 2 come from the Siemens Norm SN 29500-2 tables 1 through 5. Failure rates under operating conditions are calculated from the reference failure rate and virtual junction temperature using conversion information in SN 29500-2 section 4.

3 Failure Mode Distribution (FMD)

The failure mode distribution estimation for DRV425-Q1 in Table 3 comes from the combination of common failure modes listed in standards such as IEC 61508 and ISO 26262, the ratio of sub-circuit function size and complexity and from best engineering judgment.

The failure modes listed in this section reflect random failure events and do not include failures due to misuse or overstress.

Table 3. Die Failure Modes and Distribution

Die Failure Modes	Failure Mode Distribution (%)
VOUT high (following VDD)	8%
VOUT not in specification	50%
VOUT low (following GND)	8%
VOUT invalid (following VREF)	14%
REFOUT not in specification	12%
REFOUT high (VDD) or low (GND)	3%
Pin to pin short, any two pins	5%

4 Pin Failure Mode Analysis (Pin FMA)

This section provides a Failure Mode Analysis (FMA) for the pins of the DRV425-Q1. The failure modes covered in this document include the typical pin-by-pin failure scenarios:

- Pin short-circuited to Ground (see Table 5)
- Pin open-circuited (see Table 6)
- Pin short-circuited to an adjacent pin (see Table 7)
- Pin short-circuited to VDD (see Table 8)

Table 5 through Table 8 also indicate how these pin conditions can affect the device as per the failure effects classification in Table 4.

Table 4. TI Classification of Failure Effects

Class	Failure Effects
A	Potential device damage that affects functionality
B	No device damage, but loss of functionality
C	No device damage, but performance degradation
D	No device damage, no impact to functionality or performance

Figure 2 shows the DRV425-Q1 pin diagram. For a detailed description of the device pins please refer to the '*Pin Configuration and Functions*' section in the DRV425-Q1 datasheet.

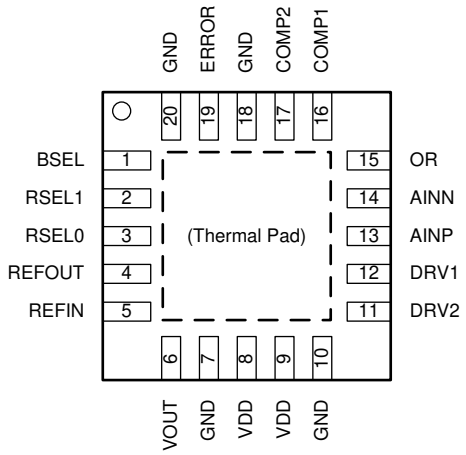

Figure 2. Pin Diagram

Following are the assumptions of use and the device configuration assumed for the pin FMA in this section:

- T_A = -40°C to +125°C
- VDD = 3.0 V to 5.5 V

Table 5. Pin FMA for Device Pins Short-Circuited to Ground

Pin Name	Pin No.	Description of Potential Failure Effect(s)	Failure Effect Class
BSEL	1	BSEL is a high-impedance digital input that accepts inputs from GND to VDD. If BSEL = VDD is expected, bandwidth performance is affected. If BSEL = GND is expected, normal operation.	D if BSEL = GND by design; C otherwise
RSEL1	2	RSEL1 is a high-impedance digital input that accepts inputs from GND to VDD. If RSEL1 = VDD is expected, REFOUT behavior is affected. If RSEL1 = GND is expected, normal operation.	D if RSEL1 = GND by design; C otherwise
RSEL0	3	RSEL0 is a high-impedance digital input that accepts inputs from GND to VDD. If RSEL0 = VDD is expected, REFOUT behavior is affected. If RSEL0 = GND is expected, normal operation.	D if RSEL0 = GND by design; C otherwise
REFOUT	4	REFOUT shorted to GND. Output current will be limited by REFOUT output impedance. Thermal damage is possible if left in this condition for extended periods of time.	B
REFIN	5	REFIN is a high-impedance input. If the pin is driven externally, then the driver output is shorted to GND and could be affected. If the pin is driven by REFOUT, then REFOUT is shorted to GND as in the previous case.	B
VOUT	6	Output shorted to GND. Output current will be limited by VOUT output impedance and short-circuit current limit. Thermal damage is possible if left in this condition for extended periods of time.	B
GND	7	Normal operation.	D
VDD	8	Power supply shorted to GND.	B
VDD	9	Power supply shorted to GND.	B
GND	10	Normal operation.	D
DRV2	11	This pin is connected to an H-bridge and will create a max current of approximately 250mA. Normally this is limited by COMP1 and COMP2 loading which is approximately 100Ω.	B
DRV1	12	This pin is connected to an H-bridge and will create a max current of approximately 250mA. Normally this is limited by COMP1 and COMP2 loading which is approximately 100Ω.	B
AINP	13	This pin is a high-impedance analog input. Shorting to GND will affect functionality.	B
AINN	14	This pin is a high-impedance analog input. Shorting to GND will affect functionality.	B
OR	15	This pin is an open-drain output, and when shorted to GND will create a false positive over-range condition.	C
COMP1	16	This is an input driven by DRV1 and may have a shunt resistance in series. The COMP1 pin has an impedance to COMP2 of about 100Ω. The largest concern is due to the DRV pins connected to these inputs (see DRV1, DRV2).	B
COMP2	17	This is an input driven by DRV2 and may have a shunt resistance in series. The COMP2 pin has an impedance to COMP1 of about 100Ω. The largest concern is due to the DRV pins connected to these inputs (see DRV1, DRV2).	B
GND	18	Normal operation.	D
ERROR	19	This pin is an open-drain output, and when shorted to GND will create a false positive error flag condition.	C
GND	20	Normal operation.	D

Table 6. Pin FMA for Device Pins Open-Circuited

Pin Name	Pin No.	Description of Potential Failure Effect(s)	Failure Effect Class
BSEL	1	BSEL will float to an unknown stage. Bandwidth mode will be unknown.	C
RSEL1	2	RSEL1 will float to an unknown stage. REFOUT mode will be unknown.	C
RSEL0	3	RSEL0 will float to an unknown stage. REFOUT mode will be unknown.	C

Table 6. Pin FMA for Device Pins Open-Circuited (continued)

Pin Name	Pin No.	Description of Potential Failure Effect(s)	Failure Effect Class
REFOUT	4	If REFIN is driven by REFOUT by design, functionality will be affected. If REFIN is driven externally, no impact to system.	B if REFIN = REFOUT by design, D otherwise
REFIN	5	REFIN is required to bias the DRV pins and the output amplifier. If left floating, the reference voltage is unknown and functionality will be affected.	B
VOUT	6	Output can be left open. There is no effect on the IC, but the output will not be measured.	C
GND	7	No ground connection to device. Functionality is lost.	B
VDD	8	No power supply to device. Functionality is lost.	B
VDD	9	No power supply to device. Functionality is lost.	B
GND	10	No ground connection to device. Functionality is lost.	B
DRV2	11	DRV2 drives a compensation coil that is in a negative feedback path. Without this connection the device will not be able to compensate and rail the magnetic field. The device will not function.	B
DRV1	12	DRV1 drives a compensation coil that is in a negative feedback path. Without this connection the device will not be able to compensate and rail the magnetic field. The device will not function.	B
AINP	13	AINP will float to an unknown voltage. VOUT will not provide the correct output.	B
AINN	14	AINN will float to an unknown voltage. VOUT will not provide the correct output.	B
OR	15	Over-range conditions unable to be detected.	C
COMP1	16	COMP1 is a compensation coil input in a negative feedback path. Without this connection the device will not be able to compensate and rail the magnetic field. The device will not function.	B
COMP2	17	COMP2 is a compensation coil input in a negative feedback path. Without this connection the device will not be able to compensate and rail the magnetic field. The device will not function.	B
GND	18	No ground connection to device. Functionality is lost.	B
ERROR	19	Error flag conditions unable to be detected.	C
GND	20	No ground connection to device. Functionality is lost.	B

Table 7. Pin FMA for Device Pins Short-Circuited to Adjacent Pin

Pin Name	Pin No.	Shorted to	Description of Potential Failure Effect(s)	Failure Effect Class
BSEL	1	2 - RSEL1	BSEL and RSEL1 are both digital input pins. If they are being driven to different logic levels then functionality is affected. If they are at the same potential by design, then normal operation.	D if BSEL = RSEL1 by design; B otherwise
RSEL1	2	3 - RSEL0	RSEL1 and RSEL0 are both digital input pins. If they are being driven to different logic levels then functionality is affected. If they are at the same potential by design, then normal operation.	D if RSEL1 = RSEL0 by design; B otherwise
RSEL0	3	4 - REFOUT	RSEL0 is a digital input and REFOUT is an analog output. REFOUT may drive RSEL0 to a different logic level, and may drive short-circuit current into the output of the RSEL0 driver.	B
REFOUT	4	5 - REFIN	Normal operation if REFOUT is intended to drive REFIN. If an external reference is used, REFOUT may drive short-circuit current into the output of the reference driver.	D if REFIN = REFOUT by design; B otherwise
REFIN	5	6 - VOUT	Output shorted to REFIN. Will affect functionality of the output amplifier stage.	B
VOUT	6	7 - GND	Output shorted to GND. Output will be limited by VOUT output impedance and short-circuit current limit. Thermal damage is possible if left in this condition for extended periods of time.	B
GND	7	8 - VDD	Power supply shorted to GND.	B
VDD	8	9 - VDD	Normal operation.	D
VDD	9	10 - GND	Power supply shorted to GND.	B
GND	10	11 - DRV2	DRV2 is connected to an H-bridge and will create a max current of approximately 250mA. Normally this is limited by COMP1 and COMP2 loading which is approximately 100Ω.	B
DRV2	11	12 - DRV1	H-bridge drivers shorted together, causing a short-circuit current condition.	B
DRV1	12	13 - AINP	Normal operation.	D
AINP	13	14 - AINN	The shunt resistor is bypassed and differential amplifier is shorted. VOUT will track REFIN.	B
AINN	14	15 - OR	AINN will be driven by the strongest driver. Normally a pull-up on the OR pin will not dominate, but will create a error as the output changes. During an over-range condition AINN will be driven to GND which could create large currents.	B
OR	15	16 - COMP1	During normal operation the OR pin will be high-impedance and will not impact the COMP1 pin. Once there is an over-range condition, the OR will drive to GND and create a large current.	B
COMP1	16	17 - COMP2	Shorting across COMP1 and COMP2 will cause the feedback loop to fail and create a high current condition. The current will run through the short and not the device.	B
COMP2	17	18 - GND	COMP2 is an input driven by DRV2 and may have a shunt resistance in series. The COMP2 pin has an impedance to COMP1 of about 100Ω. The largest concern is due to the DRV pins connected to these inputs (see DRV1, DRV2).	B
GND	18	19 - ERROR	ERROR is an open-drain output, and when shorted to GND will create a false positive error flag condition.	C
ERROR	19	20 - GND	ERROR is an open-drain output, and when shorted to GND will create a false positive error flag condition.	C
GND	20	1 - BSEL	BSEL is a high-impedance digital input that accepts inputs from GND to VDD. If BSEL = VDD is expected, bandwidth performance is affected. If BSEL = GND is expected, normal operation.	D if BSEL = GND by design; C otherwise

Table 8. Pin FMA for Device Pins Short-Circuited to VDD

Pin Name	Pin No.	Description of Potential Failure Effect(s)	Failure Effect Class
BSEL	1	BSEL is a high-impedance digital input that accepts inputs from GND to VDD. If BSEL = GND is expected, bandwidth performance is affected. If BSEL = VDD is expected, normal operation.	D if BSEL = VDD by design; C otherwise
RSEL1	2	RSEL1 is a high-impedance digital input that accepts inputs from GND to VDD. If RSEL1 = GND is expected, REFOUT behavior is affected. If RSEL1 = VDD is expected, normal operation.	D if RSEL1 = VDD by design; C otherwise
RSEL0	3	RSEL0 is a high-impedance digital input that accepts inputs from GND to VDD. If RSEL0 = GND is expected, REFOUT behavior is affected. If RSEL0 = VDD is expected, normal operation.	D if RSEL0 = VDD by design; C otherwise
REFOUT	4	REFOUT shorted to VDD. Output current will be limited by the output impedance of REFOUT. Thermal damage is possible if left in this condition for extended periods of time.	B
REFIN	5	REFIN is a high-impedance input. If the pin is driven externally, then the driver output is shorted to VDD and could be affected. If the pin is driven by REFOUT, then REFOUT is shorted to VDD as in the previous case.	B
VOUT	6	Output shorted to VDD. Output current will be limited by VOUT output impedance and short-circuit current limit. Thermal damage is possible if left in this condition for extended periods of time.	B
GND	7	Power supply shorted to GND.	B
VDD	8	Normal operation.	D
VDD	9	Normal operation.	D
GND	10	Power supply shorted to GND.	B
DRV2	11	This pin is connected to an H-bridge and will create a max current of approximately 250mA. Normally this is limited by COMP1 and COMP2 loading which is approximately 100Ω.	B
DRV1	12	This pin is connected to an H-bridge and will create a max current of approximately 250mA. Normally this is limited by COMP1 and COMP2 loading which is approximately 100Ω.	B
AINP	13	This pin is a high-impedance analog input. Shorting to VDD will affect functionality.	B
AINN	14	This pin is a high-impedance analog input. Shorting to VDD will affect functionality.	B
OR	15	This pin is an open-drain output, and when shorted to VDD will prevent detection of over-range conditions.	C
COMP1	16	This is an input driven by DRV1 and may have a shunt resistance in series. The COMP1 pin has an impedance to COMP2 of about 100Ω. The largest concern is due to the DRV pins connected to these inputs (see DRV1, DRV2).	B
COMP2	17	This is an input driven by DRV2 and may have a shunt resistance in series. The COMP2 pin has an impedance to COMP1 of about 100Ω. The largest concern is due to the DRV pins connected to these inputs (see DRV1, DRV2).	B
GND	18	Power supply shorted to GND.	B
ERROR	19	This pin is an open-drain output, and when shorted to VDD will prevent detection of error flag conditions.	C
GND	20	Power supply shorted to GND.	B

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