Application Note

Protected, Low-Noise, Combined V-I Output Stage as Analog Output Building Block

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ABSTRACT

This application note is introducing a versatile circuit that can be used as an output stage for either voltage and current. The circuit is using an opamp with disable feature, and adds required circuitry for protection and range selection making the circuit an attractive, flexible, and cost-effective design for driving analog outputs for industrial applications.

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Trademarks

1 Introduction

PLC analog control signals of actuators are typically 4-to 20mA or ±10V. the same is true for 4 and 3-wire Sensor transmitters. A common practice is to use low voltage DACs (3.3V or 5V powered) to drive an output stage (with power > ±10V). The ability to drive either voltage or current on the same output terminals adds desired flexibility to the PLC output module or the sensor transmitter.

This article explores the efficient construction of a combined voltage and current output stage using an opamp with a shutdown feature. Also discussed is the methods to protect the stage against over voltage and over current, as well as the expected performance of such a stage. Additionally, the process of building multi-channel modules using this output stage is shared.

2 Circuit Description

Figure 2-1 shows the combined V/I circuit. The current path is formed by U1 and U2, and the voltage path is formed by U3 and U4.

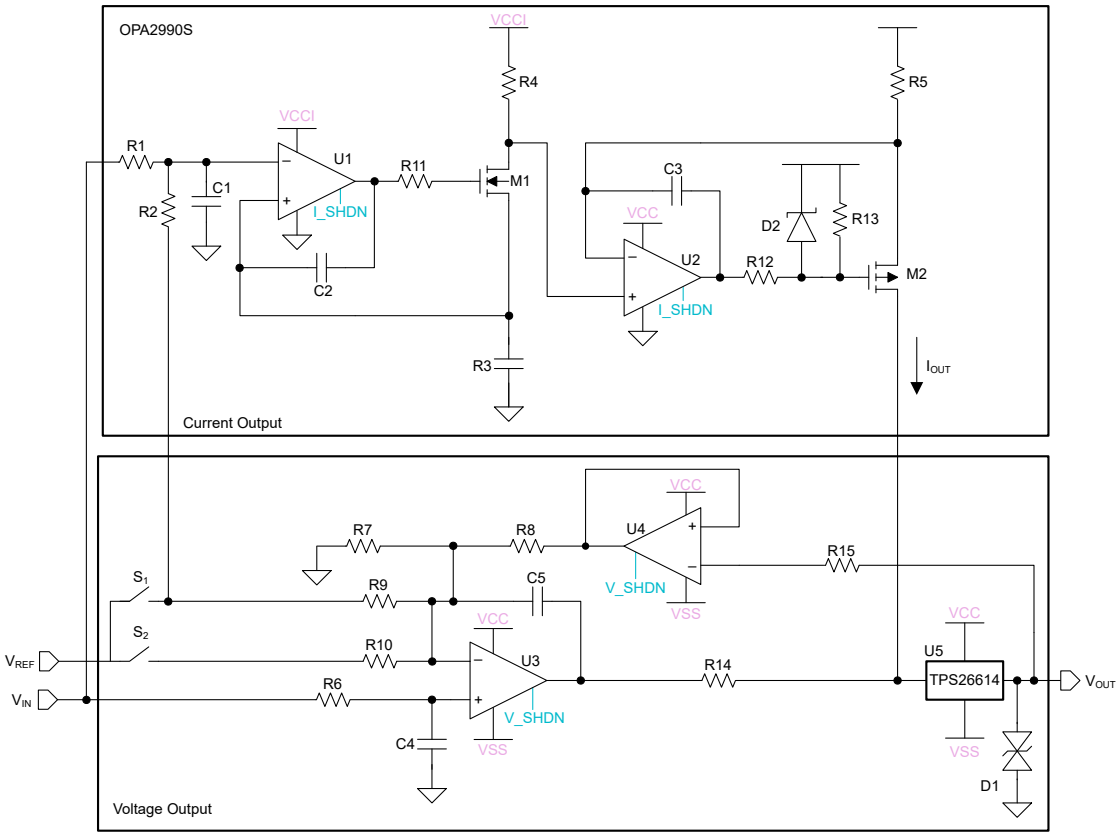

Figure 2-1. Combined V/I Stage Schematic

The current path is a two-stage voltage to current converter. The transfer function is straightforward to derive:

$$I_{OUT} = \left[V_{IN} \times \frac{R_2}{R_1 + R_2} + V_{REF} \times \frac{R_1}{R_1 + R_2}\right] \times \frac{R_5}{R_3 \cdot R_4} \quad (1)$$

If the VREFI input is open circuit, this equation reduces to:

$$I_{OUT} = V_{IN} \times \frac{R_5}{R_3 \cdot R_4} \quad (2)$$

The voltage path is a non-inverting amplifier, with the feedback resistors driven by a unity gain buffer instead of connecting them directly to the output node. Buffering the output reduces the current leaked to the feedback

resistors, and hence reduces the error in the current output mode. Again, the transfer function for the voltage output stage can be easily derived as:

$$V_{OUT} = V_{IN} \times \left[1 + \frac{R_8}{R_7} + \frac{R_8}{R_9}\right] - V_{REF} \times \frac{R_8}{R_9} \quad (3)$$

If the VREF input is open circuit, this equation reduces to

$$V_{OUT} = V_{IN} \times \left[1 + \frac{R_8}{R_9}\right] \quad (4)$$

If the circuit is designed for 0-10V or 0-20mA output, VREF inputs are left floating, and the simple equations are used. Assuming VIN=0 to 2.5V, Vout stage gain needs to be set to 4V/V, and current stage gain = 8mA/V. The gains are set by choosing the proper resistor values.

opamps U1 and U2, as well as U3 and U4 are dual package opamp OPA2990S. This allows the use of different supply rails for each path. The current path has VCCI, and GND as rails, while voltage path has VCC and VSS. And each path has a shutdown signal: ISHDN**I**, and VSHDN. OPA4990S can be also used instead of two dual opamps. In this case, only two supply rails are available for both voltage and current sections.

3 Supporting Multiple Output Ranges

If the circuit is required to support multiple output ranges, the circuit has to do that through changing input and reference ranges, as the stage gain is fixed. Making the gain adjustable can complicate the design and add inaccuracies.

Table 3-1 shows the different configurations for the same stage to support multiple output ranges:

Table 3-1. Configurations for Different Ranges

	0-20mA	**4-20mA**	**0 to 10**	**0 to 5**	**-10 to 10**
VREF switches	S1 open	S1 closed	S2 open	S2 open	S2 closed
VIN range	0-2.5	0-2.5	0-2.5	0-1.25	0-2.5
R ratios	$\frac{R_5}{R_3 \cdot R_4} = 0.008$	$\frac{R_1}{R_1 + R_2} = 0.2$	$\frac{R_8}{R_7} = 3$		$\frac{R_8}{R_9} = 4$

Table 3-1 shows that different output ranges can be achieved by controlling the different switches, and the input range, with the resistor ratios remaining constant.

A DAC source which has 2.5V or 1.25V full-scale is required to drive the stage, as well as a 2.5V reference.

4 Resistor Sizing, M2 Selection, and Other Design Considerations

Resistor sizing for current path starts with R5, lower value means smaller headroom, but U2 inputs closer to supply as well which can violate input common mode. R5=49.9 Ohm is reasonable choice.

The R4:R5 ratio determines the ratio of the current in M1 to the output current in M2. Lower Intermediate current (in M1) means lower current consumption, but increases output noise and degrades dynamic performance. We select a ratio of 1:10, hence R4=499Ω.

With the maximum I(M1)=2mA determined, R3=1.24kΩ.

R12=10 kΩ is used to pull-up M2 gate, while C2=C3=200pF are used to compensate U1 and U2.

M2 choice is driven by the maximum power dissipation assume 24V×20mA which is about 0.5W, and the maximum Vce voltage expected, >40V device is required. DMP6110SVT-7 is 1.2W, 60V PMOS that can be used in this circuit. M1 selection is less critical. PMV88ENEAR 0.6W, 60V NMOS is selected.

For voltage mode, R7, R8 and R9 are chosen to minimize power consumption without increasing output noise. R8=34kOhm, R7=11.3kΩ, and R9=8.45kOhm are selected.

5 Mode and Range Control

Range control switches S1, and S2 can be implemented using 1:1 SPST switch pair, which is powered by 2.7V to 5V which is typically available for data converters. TMUX1511 is a cost-effective choice here for 4 switches, for example, can support two combined V/I channels. TMUX1511 can be controlled with 1.8V volt logic.

The shutdown for the OPA2990S opamps are referred to the negative supply of the opamp, with disable threshold at 0.8V. for current path which is referred to the GND, a logic signal 1.8V or higher can be used to disable U1 and U2. For U3, and U4 though, a level shifter is required. A simple P MOSFET level shifter can be used.

6 Supply Level for Current Output

Current output stage has unipolar supply VCCI. OPA2990S can be powered by a supply voltage down to 2.7V. Assuming maximum output can reach Vout (max)=VCCI-1.5V. The maximum load for current output is RLoad(max)=Vout (max)/ 20mA. These equations can give you the minimum supply required for specific maximum load target. For RLoad=600Ω which is a common value, the minimum supply level is around 13.5V. to drive a 1kOhm load though, you need 22V instead. If 20% over current (24mA) is going to be used, then 20% higher voltage is needed.

7 Supply Levels for Voltage Output

Voltage output stage has bipolar supply VCC, VSS. OPA2990S is rail to rail opamp, with output headroom only about 150-300mV from supply rails based on the output current. For bipolar output, make sure the supply is at least +0.5V from the maximum positive output, and -0.5V from the minimum output.

For the unipolar output case 0-5V and 0-10V, to make sure true-zero output a simple negative charge pump can be used to generate VSS. LM7705 is low noise, low cost charge pump that can generate -0.23V and is capable of sinking up to 26mA, making LM7705 a good choice for generating VSS in unipolar output case.

The minimum load in voltage mode, RLoad(min)=Vout(max)/Iout(max), assuming the voltage output is designed for 20mA output, then RLoad(min)=500Ω in case of ±10V output range.

8 Protection Features

The circuit in Figure 2-1 has unique protection device U5, the TPS26614 which features both overvoltage and overcurrent protection with automatic retry. For current output mode, the device can switch off the current path in case the output node exceeded VSS or VCCI protecting the output stage from reverse current. For voltage output mode, TPS26614 can switch off if current exceeded 30mA protecting the U3 from overload or short circuit. The device can also switch off in case of voltage exceeding VCCI or VSS. To make sure proper protection for the voltage output stage, The recommendation is to keep VCC=VCCI.

The output transistor M2 gate is protected by Zener D2 to limit the Vgs(M2) voltage in case of output open circuit. In this case, U2 can pull down the Vg(M2) which can exceed the operating limits of gate voltage which is 20V for the chosen transistor. R12 can limit the current in D2 in case of such event. R13 is pulling up Vg(M2) making sure the M2 turns off in start-up.

TVS Diode D1 is protecting the output pin from Surge, EFT events, and limit the voltage of the output pin during these events. R14 protects the input of U4 by limiting the current. R1,R6, and R9 are doing the same protecting the inputs of U1 and U3 especially in the case if the input is applied on unpowered devices.

9 Measurement Results

A prototype is built for the proposed circuit and several measurements were conducted to test the performance, the following sections show those results in detail.

Conditions: ±12V supply rails, 1kΩ Load, output is averaged over 8k samples. Table 9-1 shows the measured output, supply currents in mA, and rms noise in uV, as well as corresponding effective resolution in bits. For this test, both inputs and Vref=2.5V are generated by a low noise source.

Table 9-1. Bipolar ±10V Voltage mode

vin	Vout	I(vcc)	I(vss)	rms noise	Resolution
0	-10.09124	0.232	-10.592	0.345	17.1
0.625	-5.03302	0.233	-5.418	0.366	17.1
1.25	13.63853m	0.274	0.297	0.365	17.1
1.875	5.06036	5.373	0.238	0.369	17.0
2.5	10.10703	10.533	0.24	0.374	17.0

Conditions: ±12V supply rails, 1kΩ Load, output is averaged over 8k samples. Table 9-2 shows the measured output, supply currents in mA, and rms noise in uV, as well as corresponding effective resolution in bits.

Table 9-2. Unipolar 0-5V Voltage Mode

vin	vout	I(vcc)	rms noise	Resolution
0	-0.739mV	0.221	0.109	17.5
0.625	2.51609	2.791	0.112	17.4
1.25	5.04145	5.369	0.14	17.1

Conditions: +24V supply, 1kΩ Load, output is averaged over 8k samples. Table 9-3 shows the measured output, supply currents in mA, and rms noise in nA, as well as corresponding effective resolution in bits.

Table 9-3. 0-20mA Current Mode

vin	iout	I(vcc)	rms noise	Resolution
0	1.37077u	0.253	207	18.9
1.25	10.08287	11.73	283	18.4
2.5	20.16957	22.919	279	18.4

If the 4-20mA mode is enabled, Table 9-4 shows the case of zero input

Table 9-4. 4-20mA Current Mode

vin	iout	I(vcc)	rms noise	Resolution
0	4.07328	5	276.8	18.5

10 Power Consumption

To calculate the efficiency of the output stage, power consumption of different parts of the circuits are shown in the following tables for both voltage and current modes (using VCC=24V supply and VSS=-12V), and no load for voltage mode.

Table 10-1. Power Consumption in Current Output Mode

Output	U1 and U2	I(M1)	TPS26614	U3 and U4	Total (mA)
4mA	0.55	0.4	0.8	0.03	1.78
20mA	0.7	2	0.8	0.03	3.53

Table 10-2. Power Consumption in Voltage Output Mode

Output	U1 and U2	I(M1)	TPS26614	U3 and U4 VCC, VSS	Total (mA) VCC, VSS
-10	0.03	0	0.8	0.23, -0.59	1.06, -0.59
0	0.03	0	0.8	0.23, -0.24	1.06, -0.24
10	0.03	0	0.8	0.53, -0.24	1.36, -0.24

11 Error Monte-Carlo Analysis

Prototype measurement does not give information about the full extent of the error distribution due to resistor tolerance. Monte-Carlo analysis was conducted to evaluate the error distribution for given resistor tolerance and opamp offset distribution and drift.

Table 11-1 shows the expected error (in that case unadjusted gain error) in case of using resistors with certain tolerance. Note that only R1 to R5 contributes to the accuracy of the current output path.

Table 11-1. Error Dependency on Resistor Tolerance

Resistor tolerance	1%	0.5%	0.1%	Ideal Resistors
±3 sigma error	1.73%	0.87%	0.25%	0.18%
Max error	2.3%	1%	0.3%	0.25%

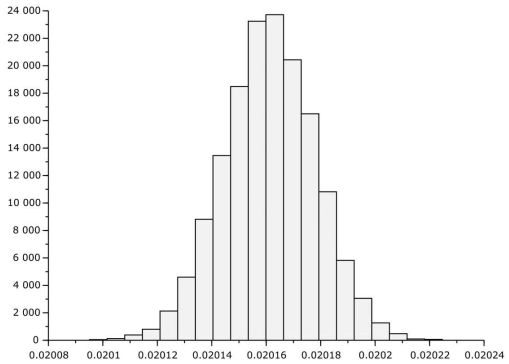

Figure 11-1. Output Current Histogram for 2.5V Input, and 0.5% Resistors

12 Rise and Fall Times

Full scale rise and fall times for bipolar voltage output are below 15us as shown in Figure 12-1.

Rise and fall times for current mode is below 20us for either 0-20mA or 4-20mA modes as shown in the following figures.

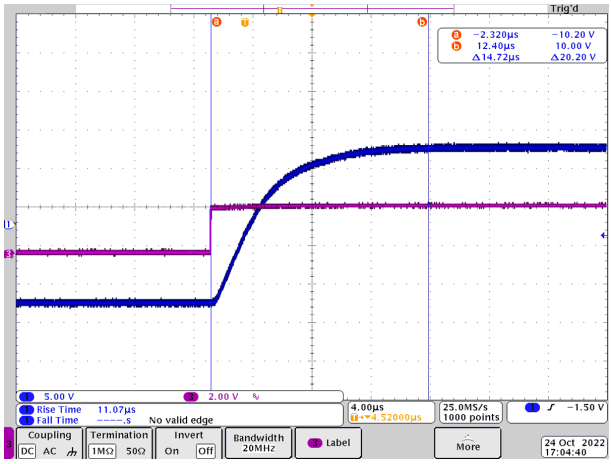

Figure 12-1. Risetime, Bipolar Voltage

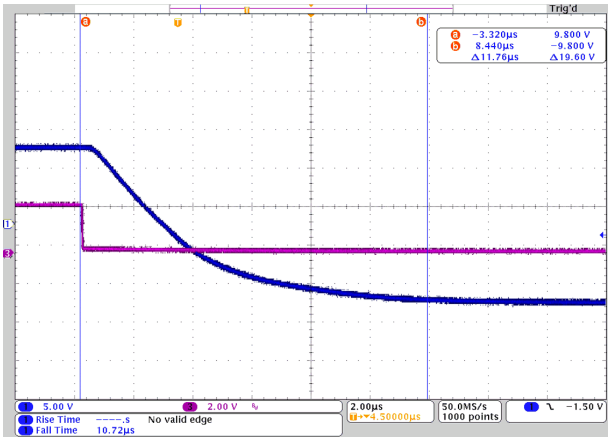

Figure 12-2. Falltime, Bipolar Voltage

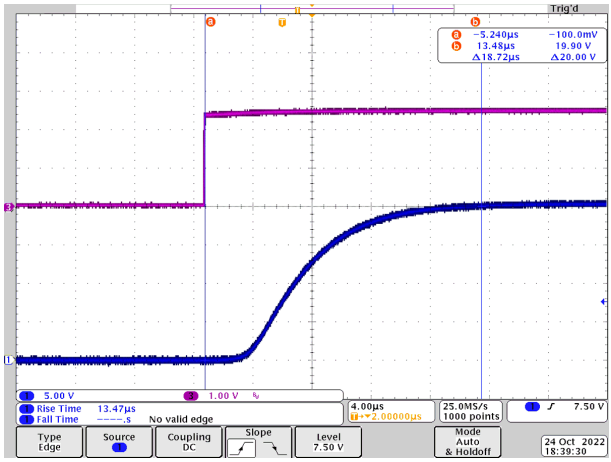

Figure 12-3. Risetime, Current Mode

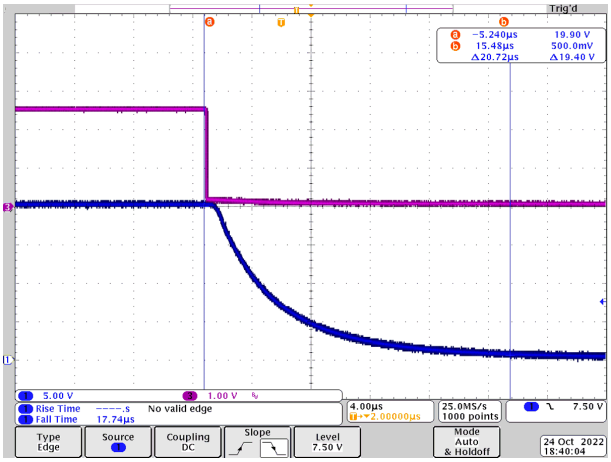

Figure 12-4. Falltime, Current Mode

13 Building Multi-Channel Output

The combined V/I circuit can be connected to a standard DAC to build configurable multi-channel output module. The DAC8050x family is a good fit for this, it offers 1 up to 8 channels, with 16b of resolution, and 1LSB INL, buffered voltage output, it has also the counterparts in 12, and 14 bits (DAC6050x, and DAC7050x). The DAC has integrated 2.5V reference which is available on external pin.

The DAC output range can be adjusted to either 2.5V or 1.25V but setting the DAC GAIN to either x1 or x2 enabling the DAC to achieve the easily implement the 0-5V output range.

Figure 13-1 shows a simplified block diagram for a 2-channel configurable range AOUT. Each of BUF1 and BUF2 represent the V/I circuit proposed.

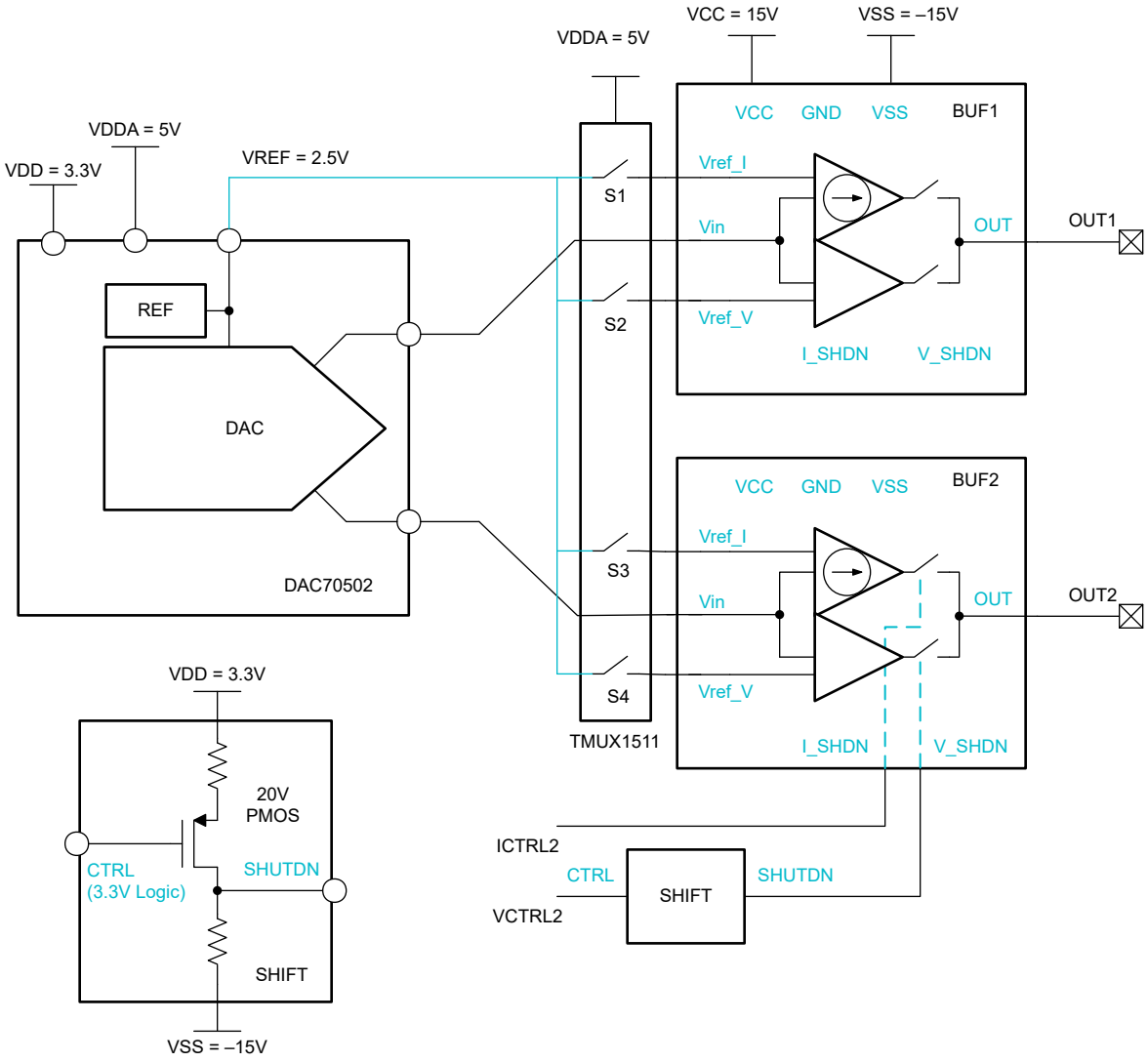

Figure 13-1. 2-Channel Output Block Diagram

14 Summary

A flexible combined V/I output stage with adjustable output range, and full protection is presented. Table 14-1 summarizes the typical performance of the output stage

Table 14-1. Performance Specification Summary

Modes	Supported mode
	Voltage 0-5V, 0-10V, ±10V
	Current 0-20mA, 4-20mA
Effective Resolution	Voltage mode: 17b Current mode: 18b
Unadjusted error	0.87%FSR for 0.5%,25ppm resistors
Power supply	VCC-VSS=5V to 40V
temperature	-40 to 125℃
Settling time(FS)	20us resistive load
Protection	Surge, OV, UV, OC

15 References

- Texas Instruments, *Bipolar ±10-V output from a unipolar DAC reference design for industrial voltage drivers,* design guide.
- Texas Instruments, *High-side Current Sources for Industrial Applications,* analog design journal.
- Electronic Products, *Programmable Analog Output Circuit Maximizes Industrial System flexibility.*

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