Application Note

Using the TMCS11xx in High Electromagnetic Interference Applications

Carolus Andrews, Joe Vanacore

ABSTRACT

As electrification continues to drive demand further into high voltage and high power applications, power density is becoming more important, with form factors shrinking for classic designs. With these size reductions, electromagnetic interference (EMI) is becoming a greater challenge in applications to correctly design for and mitigate when tradeoffs do not allow designed for layout conditions. This application note briefly discusses both conducted and radiated emissions and how the emissions relate to the susceptibility of TMCS112x and TMCS113x devices. A brief overview of common-mode and differential-mode noise are discussed, and schematic and layout techniques are provided for the device for the purposes of noise mitigation in the system.

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Trademarks

1 Introduction

Electrification throughout the world has exploded in the last decade. Electric vehicles, clean energy in the form of solar PV and type III and IV wind, data centers, higher efficiency power supplies and more have all skyrocketed in demand, with designers racing to develop designs that are cutting edge while simultaneously refining those designs for better performance, lower cost, and smaller form factor. The United States government has set a high bar in this area, with the Department of Energy tasking companies to reach new milestones in these various areas, such as a 100kW/L power density target by 2025 (with even more stringent targets listed for 2030 and 2035) for high voltage power designs, with a simultaneous cost target of only $1.80/kW and efficiency target of 98%. Furthermore, the Department of Energy have provided several companies grants and incentives to perform research and development in this area to make sure the US remains a key competitor in these spaces.

These targets are not easy to achieve. As form factors continue to shrink, components must be placed continually closer to each other in proximity, and as a result the design problem becomes more complex to also include more cumbersome thermal management, as well as the handling of electromagnetic interference. In these systems, there are often multiple field-effect transistor (FET) devices switching at relatively high speeds in power quantities great enough to produce near-field emissions that can affect other electrical components in proximity. The designer's historic ability to potentially mitigate these issues by strategic placement of sensitive components away from these intentional radiators is removed, and designs must now be developed to effectively *EMI harden* integrated circuits and components on the PCB to achieve the lofty targets set forth by the desired specification.

In this paper, the TMCS112x and TMCS113x family of devices is used as an example in the derivation of an *EMI hardened* approach to circuit design. These components are examined at the pin level for the ability to attenuate both common-mode and differential-mode forms of noise. Layout is also examined and discussed, as layout in the high-frequency domain becomes of the utmost importance. Proper layout guidelines need to be followed, and layout optimized well before attempting the techniques discussed in this paper, as the use of ferrite beads and filters can only correct signals to a certain extent, and often come with design tradeoffs, including, but not limited to system losses, accuracy, additional board space (and therefore loss of power density), and additional cost.

Note that this analysis focuses primarily on conducted emissions, and radiated emissions analysis needs to also be examined for the most robust performance. Analysis is also only performed on the low voltage side of the TMCS device, and additional noise analysis can be necessary on the high voltage side at the device inputs to make sure of a performance designed for a specific design.

2 How Noise Couples Into a System

2.1 Conducted Emissions and Radiated Emissions

To reach the aforementioned goals, switching frequencies and slew rates continue to increase higher in modern power supplies. Historically, switching frequencies were kept at sub 100kHz levels, as increases in switching frequency correlate directly to greater switching losses in the system. However, techniques such as soft switching, and technologies such as Gallium Nitride FETs have allowed designers to push the boundaries of switching frequencies in the designers products higher. This drive has led to size reduction in the needed components across the system. This has also led to increasing edge rates for both voltage and current in systems. However, these frequency increases, along with the corresponding harmonics that come with the classical square and triangle waves used in the rectification process of the modern DC/DC converter have created scenarios where noise is becoming a far greater cause for concern. Furthermore, many ICs struggle with extremely high slew rates, which are intentional by design in power systems to minimize switching losses in the transition region of the FET.

Noise enters a circuit primarily in two ways: either through conduction, or through radiation. Conducted noise refers to noise that propagates physically through a system, for example, through wires, traces, or other conductive paths. One example of conducted noise can be a noisy low voltage supply node shared by multiple victim devices. This noise is typically on the order of 150kHz to 108MHz as per CISPR 25 automotive standards (standards for other product types can move these ranges). Radiated noise, also, radiates at much higher frequencies, and is defined by CISPR 25 automotive standards to be between 150kHz and 5.925GHz. Radiated emissions tend to propagate through the air, and require no physical contact with the device under test to necessarily influence change in the system.

The most probable radiated emissions coupling mechanisms from a nearby aggressor to a potential victim are either directly through the victim, parasitic inductive coupling, or parasitic capacitive coupling. Similar to mutual induction, parasitic inductive coupling occurs when a magnetic field is generated and couples into a trace or directly into a victim device. Parasitic capacitive coupling occurs when a neighboring aggressor emits an electric field that couples through a parasitic capacitive path to a trace or victim device. For example, a high speed GaN FET switching node adjacent to an unshielded signal trace can couple through parasitic capacitance created by the distance of the switching node and said signal trace. While less common, radiated signals can also conduct into the system through antenna effects due to poor layout or problematic areas on a PCB where traces effectively act as antennae and attract these signals into the trace. The antenna effect usually occurs with harmonics in the gigahertz frequency range where short trace lengths are ⅒ to ½ wavelength of the emitter frequency.

Figure 2-1 provides a visualization of these EMI types propagating from an *aggressor* to a *victim* mounted on a PCB. Most commonly for power supplies, the aggressor can be either the high-current loop of the inductor, or the high-voltage switching node of said power supply. In these situations, multiple victims can have degraded performance due to the susceptibility to EMI. This application note primarily focuses on how to mitigate the effects of conducted and radiated emissions on the TMCS112x and TMCS113x family.

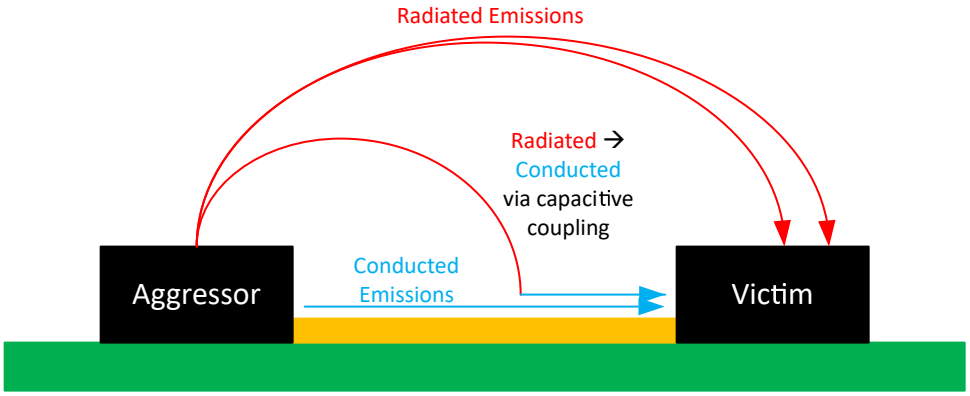

Figure 2-1. Example of an Aggressor Affecting a Victim IC

2.2 Differential Mode Versus Common-Mode Noise

When examining conducted and radiated emissions in a given system, the emissions are broken down into two types: differential-mode (DM) noise and common-mode (CM) noise. By examining and understanding the pathways these noise types can take, techniques can be developed to help mitigate or remove noise from the TMCS11xx.

Differential-mode noise has an opposite polarity when looking into the pins of the device. The aforementioned conducted emissions are seldom common-mode noise and are typically differential-mode where potentially one signal trace on a PCB is the noise source with respect to a clean analog ground signal. In most cases for the TMCS112x or TMCS113x, the reference can be GND pin of the device, which is independent of the earth or chassis GND (but *can* be referenced to one or the other based on the application). Differential-mode noise is recognized by most engineers, as this is the typical *noise* most engineers think of when observing an output signal from an IC on an oscilloscope.

Common-mode noise is most often created from a radiating aggressor emitting electric fields or magnetic fields and coupling via parasitic capacitance and/or parasitic inductance. Therefore, a distinct path to GND is not necessary to propagate this type of noise in the system. Once coupled into a nearby victim circuit, the common-mode currents travel into the pins of a victim device with the same polarity and terminate into an earth or chassis ground. As a result, this type of noise is more difficult to measure in a system. Figure 2-2 provides a visualization of these noise types and how the noise types can flow into the TMCS112x/3x. With CM and DM noise present on both L1 and L2, probing the differential voltage between these two nodes can disregard common-mode noise while effectively measuring differential-mode noise.

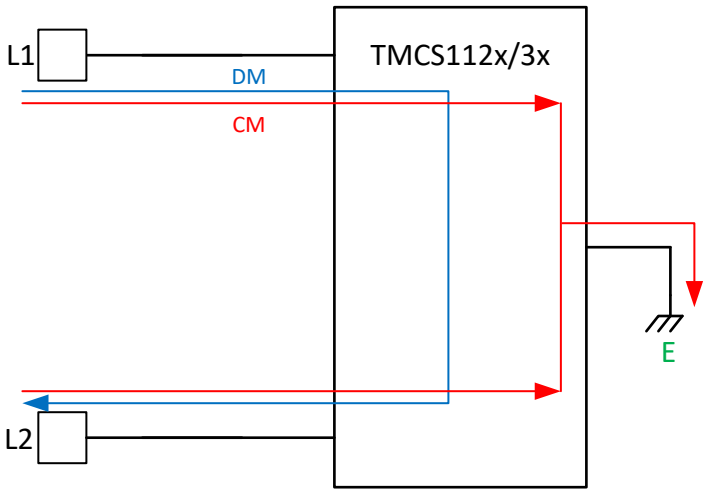

Figure 2-2. Differential-Mode (DM) vs. Common-Mode (CM) Noise Paths Through an IC

The challenge then becomes providing low-impedance pathways for these unwanted signals to traverse while simultaneously preserving the integrity of the desired signal chain. The classical way to achieve this in power systems is through the use of reactive components, as losses in these components are typically minimal, but come with the tradeoff of resonant peaking that must be addressed to make sure a successful design. In fact, most power supply designs today start at the inputs with some form of an EMI filter. Figure 2-3 shows a visualization of the relevant filter networks that must be developed to effectively control these noise sources away from the TMCS112x/3x. Note that the purpose of these networks is to provide a designed for, low-impedance path for these high-frequency signals to return upon, and failure to design an impedance path lower than that of the part does not result in a proper filter. However, this is typically manifested in the frequency response of the filter, and therefore design of these filters can be concentrated in the area of frequency shaping.

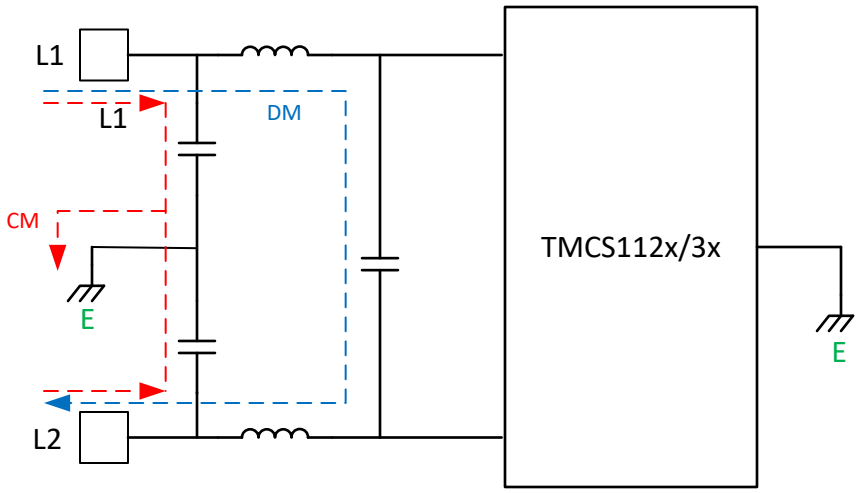

Figure 2-3. Filtering Techniques to Shape Noise Paths Away From TMCS112x/3x

3 Conducted Emissions Design Techniques

3.1 Design of the TMCS112x and TMCS112x3x EMI Topology

To design the desired topology, we begin with the overall schematic presented in Figure 3-1. This schematic implements components necessary for EMI resiliency on all pins of the low-voltage side of the TMCS112x/3x. Also note that in most design use cases, not all of these components are necessary. Proper testing needs to be conducted to determine on which pins noise propagates, and the appropriate implementation is needed on those pins only. Note that C1, C5, and C6 are not populated by default. These capacitors help to address common-mode noise in the system, but come with potential bandwidth limitations that must be considered. The effects of these capacitors can be discussed later in the application note.

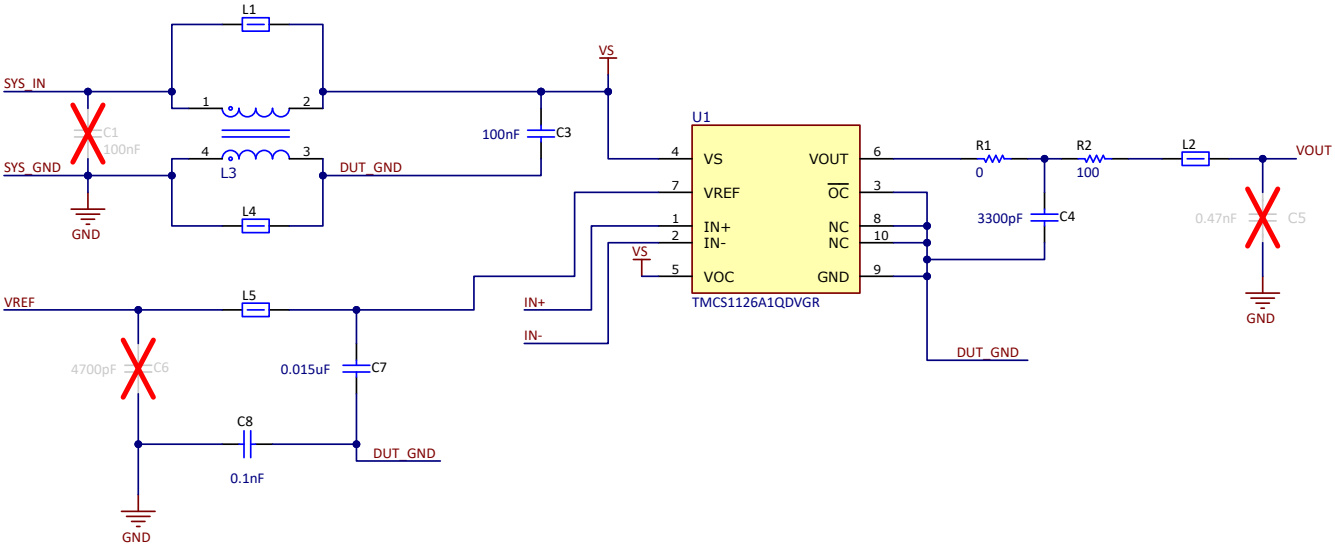

Figure 3-1. Schematic for EMI Resilience on all Low Voltage Pins of TMCS112x and TMCS112x3x, CM and DM Noise

The main device used to combat EMI here is the ferrite bead. Ferrite beads can be used on signal paths to reduce noise on differential lines, and suppress high-frequency signals that can cause problems in the circuit. The ferrite beads provide the following benefits:

- Low DC resistance when placed in the series path of a signal, resulting in a minimal voltage drop for the DC portion of the signal. This makes them designed for DC signals, such as potentially noisy supply voltages
- A variable AC impedance, R_{AC}, that attenuates a specific band of frequencies based on the specific devices' data sheet
- Ferrite beads dissipate energy as heat, unlike inductors, which store energy. This allows the device to reduce noise at targeted frequencies while preserving the integrity of the signal chain
- Used in conjunction with capacitors, LC filter combinations result in a -40dB/decade attenuation, where traditional RC filters can only provide -20dB/decade attenuation

Every ferrite bead can be slightly different due to not only the properties discussed previously, but also the parasitics associated with the device. These parasitics are typically inherent to the device, and can depend on dimensions, material, footprint, and several other factors. Due to the complexity, these parasitics bring to the design, this is recommended, when available, that filter design be completed through the use of manufacturer provided spice models, as the parasitics present in the device can affect both the magnitude and location of the resonant peak formed by the filter. An example properties curve is shown for the Murata BLM31KN102SH1L size 1206, 1kΩ at 1MHz ferrite bead in Figure 3-2.

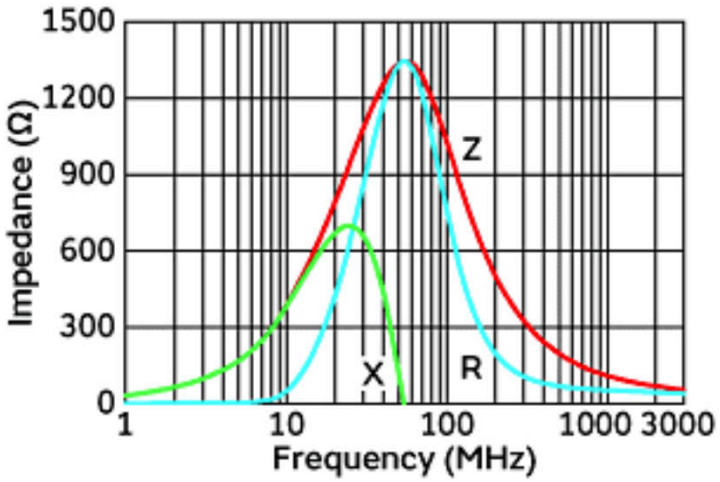

Figure 3-2. Murata BLM31KN102SH1L Ferrite Bead Characteristic Impedance Curves

3.1.1 Components for Differential-Mode Noise Reduction

The highlighted components in Figure 3-3 are required to reduce DM noise on the given pin of the device. Ferrite beads L1, L2, L4, and L5 serve to create high-impedance pathways between the system traces and the device, discouraging noise away from these traces. For the portion that does travel into the local area of the TMCS112x/3x, capacitors C3, C4, and C7 form low pass filters with these components to shunt away the noise before reaching the device.

Note that the TMCS112x/3x has data sheet limits on the amount of capacitance able to be supported by the VOUT and VREF pins of 4.7nF and 20nF, respectively, that must be adhered to. Resistor R1 serves as an optional isolation resistor to bolster the output impedance of the output pin, allowing for capacitance greater than 4.7nF to be used (by default this is set to 0Ω to simply pass the VOUT signal out from the device). Care must be taken when populating R1 with a non-zero value, as this can form a low pass filter with the device's output, and potentially reduce the bandwidth of the device. Filter design can also be affected, and this component need to be modeled if used.

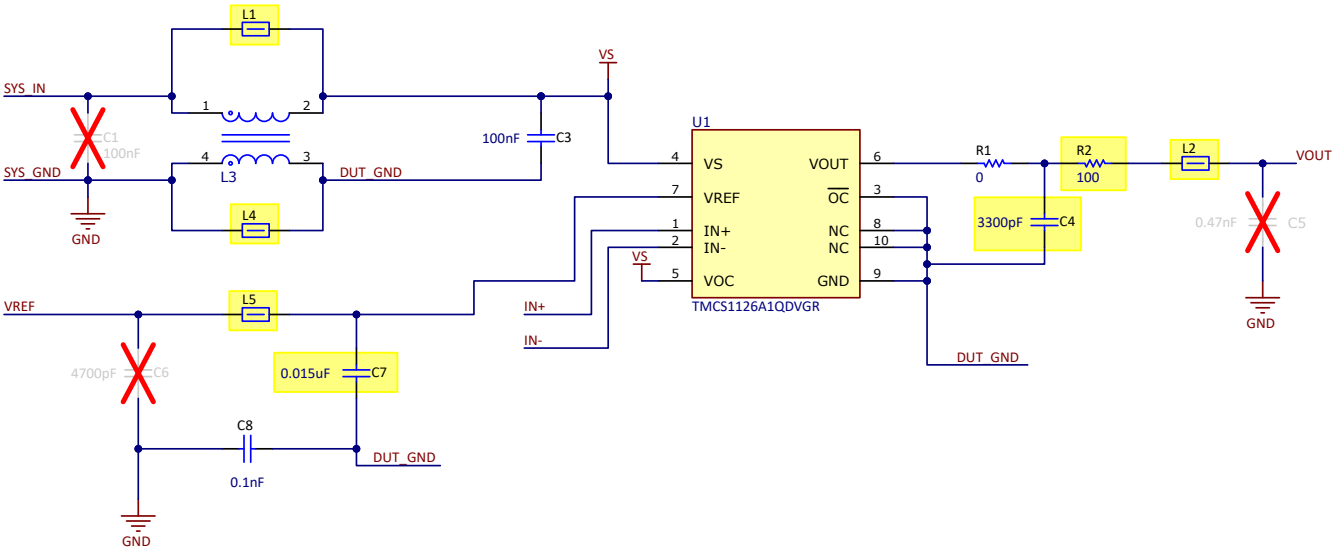

Figure 3-3. Components for Differential-Mode Noise Reduction

Resistor R2 is placed for resonance reasons. As an example, assume noise signatures are identified in the system at a frequency 2.62MHz. The measurements made show up to 1Vpp noise present on the output pin of the TMCS112x/3x for this given frequency, and the design goal is to reduce this to less than 200mVpp. In dB, this can equate to a 14dB attenuation as shown in Equation 1.

$$20 \times \log\left(\frac{1}{0.2}\right) \quad = \quad 14dB \tag{1}$$

These values are summarized in Table 3-1.

Table 3-1. Example of Problematic Frequency Measurement

Frequency (MHz)	Measured Noise (Vpp)	Target Attenuation (dB)
2.62	1	14

Several tools exist to help achieve these types of designs, such as Murata's Sim-Surfing suite of filter design tools. A 3.3nF capacitor is chosen to make sure the data sheet limit for the V_{OUT} pin is met, and then an appropriate ferrite was determined. Upon choosing components, simulations were performed as shown in Figure 3-4 and Figure 3-5. While the ferrite and capacitor yield the desired -40dB/decade attenuation, can be observed that a resonance has formed between these components and a near 40x gain has been formed at 1.24MHz. This resonance results in a failure to obtain the desired attenuation at 2.62MHz.

Resistor R2 is then placed in the system. This resistor serves to dampen the resonance between these components. Figure 3-6 and Figure 3-7 show the re-run simulation with resistor populated. The observation is that placement of the resistor eliminates the resonant peak from the response, and also corrects the attenuation into acceptable limits. The 40dB attenuation also removes additional high frequency content from the response out to approximately 150Mhz.

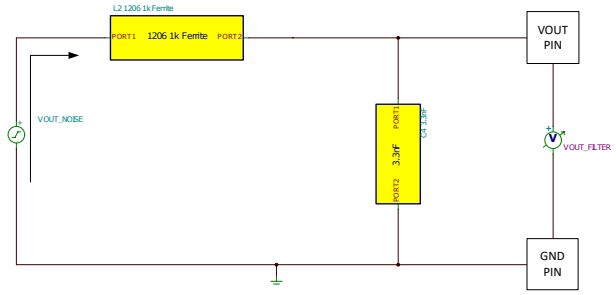

Figure 3-4. DM Filter Modeling of VOUT pin, R2 not Populated

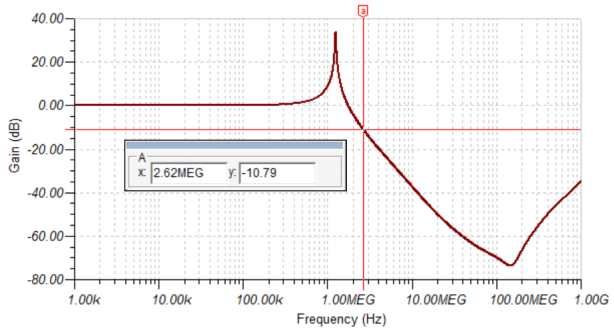

Figure 3-5. DM Filter Simulation Results, VOUT pin, R2 not Populated

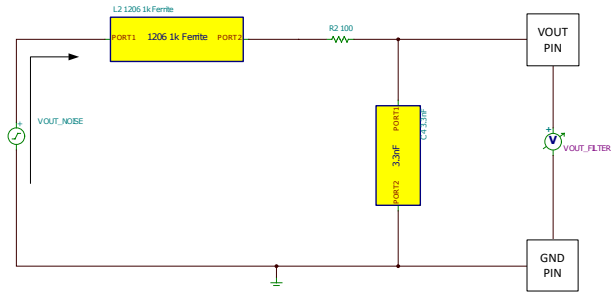

Figure 3-6. DM Filter Modeling of VOUT pin, R2 Populated

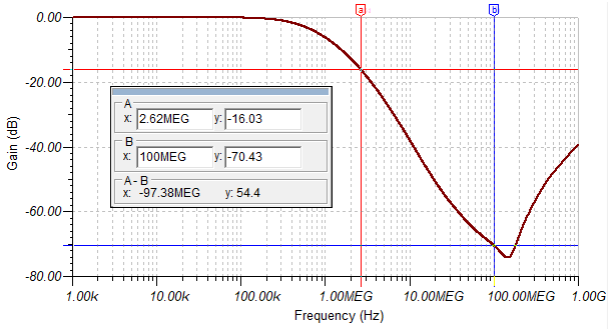

Figure 3-7. DM Filter Simulation Results, VOUT pin, R2 Populated

3.1.2 Components for Common-Mode Noise Reduction

The highlighted components in Figure 3-8 are necessary for implementation when CM noise is present in the system. Note that capacitors C1, C5, and C6 are not populated, and the schematic as presented in this document is for the handling of differential mode noise only. Common-mode choke, L3, is also not populated. This is shown in the schematic, but typically only ferrite beads or the choke can be implemented, but not both. In this document, beads L1 and L4 are populated instead.

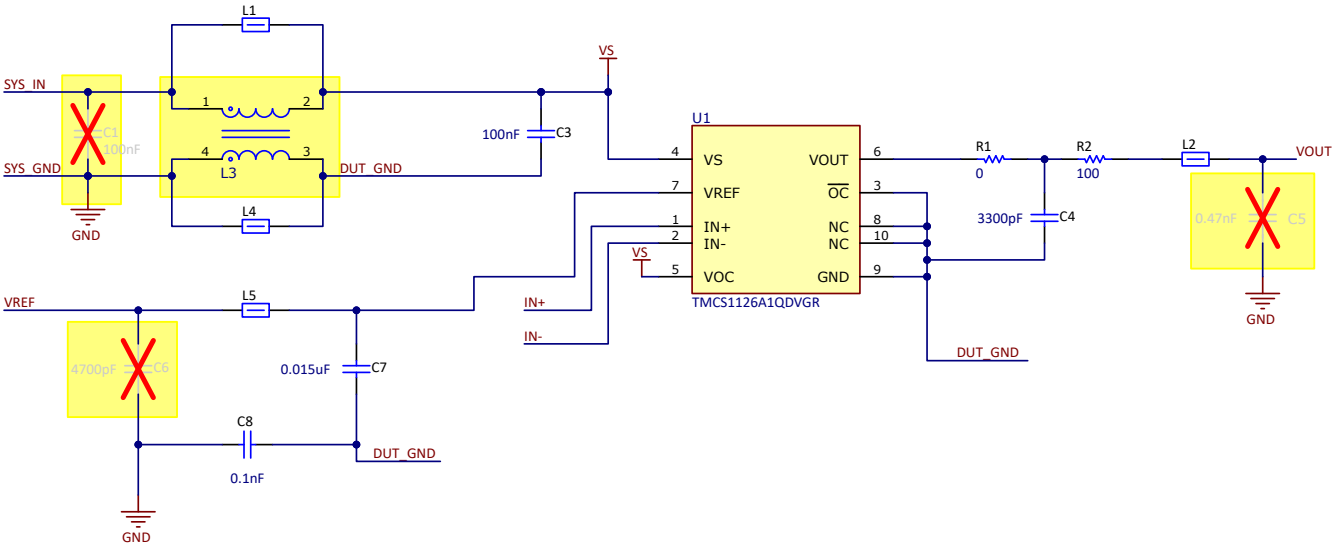

Figure 3-8. Components for Common-Mode Noise Reduction

Common-mode components are less forgiving than the components DM counterparts, as population of these components form low pass-filters with the ferrite beads on the outgoing signals of the device, and therefore have the potential to directly affect bandwidth and response capabilities in the signal chain. Starting from the differential mode filter designed above, we now reverse the drive signal and measurement point to simulate the output being driven as per normal device operation. Figure 3-9 shows the setup of the schematic in TINA-TI, while Figure 3-10 shows an AC sweep of the frequency response of the output pin. The simulation shows that, as designed, the filter can have no impact on the output bandwidth of the device for outward bound signals.

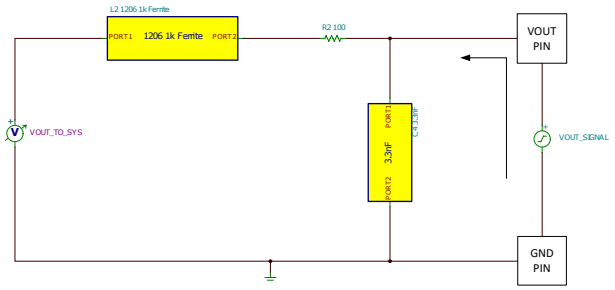

Figure 3-9. DM Filter Drive Schematic, VOUT pin, R2 Populated

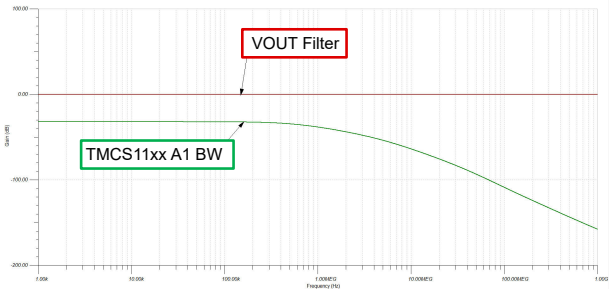

Figure 3-10. DM Filter Drive Frequency Response, VOUT pin, R2 Populated

3.2 Layout Considerations for EMI Resilience

Making sure robustness against EMI starts with a good layout, not only for the TMCS112x/3x, but all components on the PCB. In general, boards containing 4-layers or more provide the best return path scenario, as ground planes on the inner layers provide a designed for return path for all signals; wherever traces were run, signal or power, there is always a return directly underneath the signal. However, newer designs are pushing higher power into the PCB, demanding new techniques be implemented to help manage the thermal problem. This can lead to scenarios such as inner plane replication which can segment ground planes, or designs reducing layer count down to 2 in an effort to further reduce cost in the system. Even though preventing the EMI aggressors is the best course of action is not always possible. In these scenarios, EMI-resilient design is possible, but additional steps and best practice must be considered to make sure of the designed for performance. In general, the best practice is to route return paths directly beneath the signal. In addition, consider the following best practices as you lay out the TMCS112x/3x in your design:

- If possible, use a 4 layer board. Create a GND plane on an internal layer for the purposes of providing a clean return path for all signals traced on the outer layers.
  - The best practice is to not route traces in the ground place at all. If this *must* happen, make sure the trace layout is optimized to keep splitting of the ground plane to a minimum, as this can reroute return paths through unwanted areas, or increase loop size in signals
- Isolate the device from high sources of EMI as much as possible. Fast switching inductors loops and high voltage switch nodes are of largest concern.
  - Inductance increases with length, and decreases with width. Therefore, high-frequency current paths need to be made as wide, and as short as possible.
- All capacitors need to be sized to 0402 or 0603 for the lowest ESR, for example, best high frequency response. Typically, the smallest footprint device can result in lowest parasitics, and therefore, these smaller options tend to perform better in high-EMI environments
  - At a minimum, make sure at least one bypass capacitor is used between the V+ and GND pins of the device.
  - If multiple bypass capacitors are used, make sure the lowest capacitance (which targets the highest frequencies) is placed closest to the device. This is performed to make sure that all HF content is removed prior to reaching the part. If the lowest capacitance were placed farthest from the part, HF content can potentially couple onto the trace beyond the capacitor and then migrate into the device.
- Shield signal traces with the respective return path if possible. In most cases, this can be the common GND. This technique can help reduce the antenna effects of unshielded traces. An example of this can be seen in Figure 3-11.

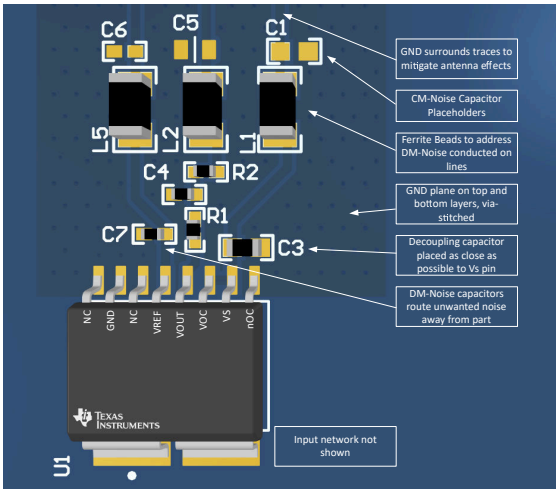

Figure 3-11. TMCS1126 Layout Example, Differential-Mode Noise Only

For designs where high CM noise is also present, additional isolation techniques through grounds can be used. Figure 3-12 shows an example of *islanding* the GND of the TMCS112x/3x. This technique effectively severs the noisy system GND from the device, and makes sure CM noise does not couple into the device. If CM noise is not present in the system, the TMCS112x/3x can be referenced to GND as normal, and capacitor C8 is not needed. The following practices need to also be noted if using this technique:

- Ferrite beads (L1, L2, L4, L5) needs to be sized as large as possible to maximize space between GND planes.
- The 100pF *stitching cap* between GNDs (C8) gives a return path for high frequency radiated noise
  - Without this cap, radiated noise can couple into the TMCS GND plane and see a high impedance return path to the MCU GND.
  - This can *trap* the HF noise and force the noise to couple into our device pins as these are lower impedance than the ferrite beads.
  - This capacitor provides a low impedance path at HF to return noise to MCU GND.
- Input capacitors C1, C5, and C6 are only needed if CM noise is measured in the system. Please place pads for all components in this schematic for troubleshooting.
- While not shown in the layout, a common-mode choke can be used in place of beads L1 and L4 to further limit common mode noise into the device. Usage of both ferrite beads and a choke is not necessary here, and can only further increase cost and component count.

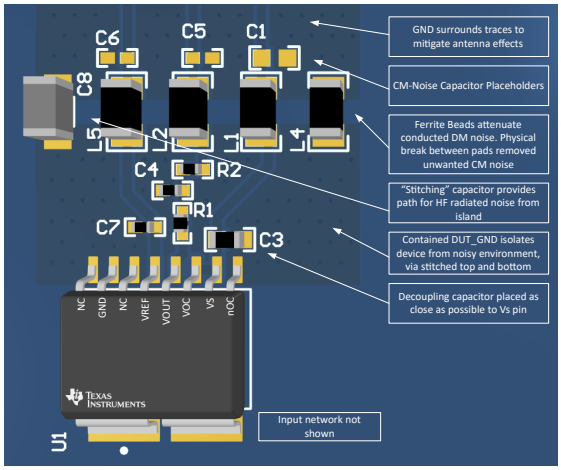

Figure 3-12. TMCS1126 Layout Example, Differential-Mode Noise and Common-Mode Noise

4 Summary

In this application note, electromagnetic interference is shown to be a rising problem in many power systems due to power systems demand as electrification continues to spread to new areas. Movement to higher voltage systems, minimization of space for the increase of power density and reduction of cost, and several other factors are making the forced proximity of sensitive components necessary in design to achieve the lofty goals being set forth by both public and private sectors. A background was given into how these noise sources are created and quantified, and techniques are presented that allow the designer to help design the layouts to remain as robust as possible in the face of these challenges.

5 References

- U.S. Department of Energy, *Electrification 2023 Annual Progress Report*.
- Texas Instruments, *Mitigating Noise in DC/DC Converters*, video.
- Murata, *BLM31KN102SH1# Product Information*.
- Texas Instruments, *PCB Design Guidelines For Reduced EMI*, application note.

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