*Application Brief*

# *Utilizing Configurable Logic in System Design*

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## Introduction

Configurable logic gates differ from programmable logic devices like FPGA, MCU, or CPLD products primarily in that configurable logic devices do not include any memory or fuses for configuration purposes. Configurable logic gates are integrated combinational logic circuits that provide a single Boolean logic function, but can be utilized to create a variety of logic functions depending on how the inputs are connected. The combinational logic circuit always remains the same, while only the used portion of that functionality changes. Each configurable function number provides a unique logic truth table which can be cleverly utilized to produce multiple logic functions. There are five primary configurable logic function numbers: '57, '58, '97, '98, '99. There are additionally two D-type flip-flops that include configurable logic which are denoted by the '100 and '101 functions.

Many automotive power-train architectures today require multiple gate drivers to efficiently and stably operate power MOSFETs. For correct operation, logic devices are utilized around these gates drivers to control various fault conditions. These commonly include both over current and over temperature detection signals in the form of PWMs. Depending on the system requirements, a variation of logic devices including flip-flops, buffers, inverters and logic gates are typically utilized to fully implement this PWM control logic. Though, with configurable logic products, many of these functions can be integrated into a singular chip. which in turn enables significant board space savings, BOM consolidation, and lower supply current consumption.

Configurable logic devices additionally include Schmitt-trigger input architecture on all inputs. Particularly in automotive applications where slow edges and transient voltage spikes are common, many logic circuits require multiple external Schmitt-trigger buffers to tolerate noisy or slow digital logic signals. The inclusion of Schmitt-trigger architecture allows for even greater consolidation of logic for additional board space savings.

## Configurable Logic Gates

**Table 1. Configurable Logic Boolean Equations**

| Configurable Function Number | Complete Boolean Equation |
|---|---|
| '57 | $\overline{A}$•$\overline{C}$+B•C |
| '58 | !($\overline{A}$•$\overline{C}$+B•C) |
| '97 | A•C+B•$\overline{C}$ |
| '98 | !(A•C+B•$\overline{C}$) |
| '99 | (A•$\overline{C}$+B•C)⊕D |

The majority of logic devices have part numbers of the form SN74**xx yyy** with **xx** being the family and **yyy** being the function number. Configurable logic devices additionally have the number of independent logic functions (or gates) in the function number, with 1G meaning one channel, 2G meaning two channels, and 3G meaning 3 channels. An example part number is SN74LVC1G57, which is the LVC logic family's single channel '57 configurable logic function.

Throughout this document, the inputs of each device are labeled generically (A, B, C, etc.). Actual pin names can vary. See the appropriate data sheet for further information. The overbar ($\overline{A}$) and exclamation point (!) are used interchangeably in this document to indicate a Boolean negation.

**Table 2. Function Selection Table**

| Function Name | Boolean Equation | '57 | '58 | '97 | '98 | '99 |
|---|---|---|---|---|---|---|
| AND | A•B | ✓ | | ✓ | | ✓ |

**Table 2. Function Selection Table (continued)**

| Function Name | Boolean Equation | '57 | '58 | '97 | '98 | '99 |
|---|---|---|---|---|---|---|
| AND with 1 input inverted | A•$\overline{B}$ | | ✓ | ✓ | ✓ | ✓ |
| NAND | $\overline{A•B}$ | | ✓ | | ✓ | ✓ |
| NAND with 1 input inverted | !(A•$\overline{B}$) | ✓ | | ✓ | ✓ | ✓ |
| OR | A+B | | ✓ | ✓ | | ✓ |
| OR with 1 input inverted | A+$\overline{B}$ | ✓ | | ✓ | ✓ | ✓ |
| NOR | $\overline{A+B}$ | ✓ | | | ✓ | ✓ |
| NOR with 1 input inverted | !(A+$\overline{B}$) | | ✓ | ✓ | ✓ | ✓ |
| XOR | A•$\overline{B}$+$\overline{A}$•B | | ✓ | | | ✓ |
| XNOR | A•B+$\overline{A}$•$\overline{B}$ | ✓ | | | | ✓ |
| 2-to-1 Data selector | A•$\overline{C}$+B•C | | | ✓ | | ✓ |
| 2-to-1 Data selector with inverted output | !(A•$\overline{C}$+B•C) | | | | ✓ | ✓ |

Configurable logic devices are available in multiple logic families. Table 3 shows what functions are available from each family. There are three possible values shown in the table: 85°C, 125°C, and AEC-Q100. The first two indicate a catalog rated device with maximum ambient operating temperature of the value listed. The third indicates an automotive rated device with 125°C maximum operating temperature. Only the highest rating of the three is shown for devices with multiple options.

**Table 3. Function Availability by Logic Family**

| Family | '57 | '58 | '97 | | '98 | | '99 | '100 | '101 |
|---|---|---|---|---|---|---|---|---|---|
| | 1 Ch | 1 Ch | 1 Ch | 3 Ch | 1 Ch | 3 Ch | 1 Ch | 2 Ch | 2 Ch |
| **AC** | | | | 125°C | | 125°C | | 125°C | 125°C |
| **AUP** | 85°C | 85°C | 85°C | | 85°C | | 85°C | | |
| **LVC** | 125°C | 125°C | AEC-Q100 | 125°C | AEC-Q100 | 125°C | AEC-Q100 | AEC-Q100 | AEC-Q100 |

- **AC** - Part number example: SN74**AC**2G100
  - Voltage Range ($V_{CC}$): 1.5 to 5.5V
  - Output Current ($I_{OL}$): 75mA at 5.5V for up to 2ms
  - Supply Current ($I_{CC}$): 20µA
  - Available ratings: Catalog
  - Special features: Positive input clamp diodes
- **AUP** - Part number example: SN74**AUP**1G57
  - Voltage Range ($V_{CC}$): 0.8 to 3.6V
  - Output Current ($I_{OL}$): 4mA
  - Supply Current ($I_{CC}$): 0.9µA
  - Special features: Over-voltage tolerant inputs to 3.6V, Partial power-down protection ($I_{off}$)
- **LVC** - Part number example: SN74**LVC**3G98
  - Voltage Range ($V_{CC}$): 1.65 to 5.5V
  - Output Current ($I_{OL}$): 32mA
  - Supply Current ($I_{CC}$): 10µA
  - Special features: Over-voltage tolerant inputs to 5.5V, Partial power-down protection ($I_{off}$)

### Example Logic Equation Simplification

In this application, the user desires a logic function of X = $\overline{G}$•H. Utilizing De Morgan's law, the Boolean equation can also be written as X = !(G+$\overline{H}$). These equations can also be referred to as *AND with one inverted input* and *NOR with one inverted input*, respectively. Referring to Table 2, we can see that the '58, '97, '98, and '99 functions all work for this application. We arbitrarily selected the '58 function for this example.

For demonstration purposes, we walk through each step required to convert the full Boolean logic equation of the '58 configurable logic gate into the required function of X = $\overline{G}$•H. This is not typically required to use a configurable logic gate as the data sheets provide a complete list of functions with appropriate logic tables and diagrams.

The Boolean equation for the '58 function is: Y = !(A•$\overline{C}$+B•C). By setting A to a logic low, the equation simplifies to Y = C•$\overline{B}$ using the following steps:

- Y = !(A•$\overline{C}$+B•C) **[Starting equation]**
- Y = !(L•$\overline{C}$+B•C) **[A is set to LOW]**
- Y = !(H•$\overline{C}$+B•C) **[$\overline{L}$ = H]**
- Y = !($\overline{C}$+B•C) **[Identity law]**
- Y =!($\overline{C}$+B) **[Simplify, $\overline{C}$+B•C = $\overline{C}$+B]**
- Y = C•$\overline{B}$ **[De Morgan's theorem]**
- X = $\overline{G}$•H **[Final simplified equation]**

### D-Type Flip-Flops with Configurable Logic Inputs

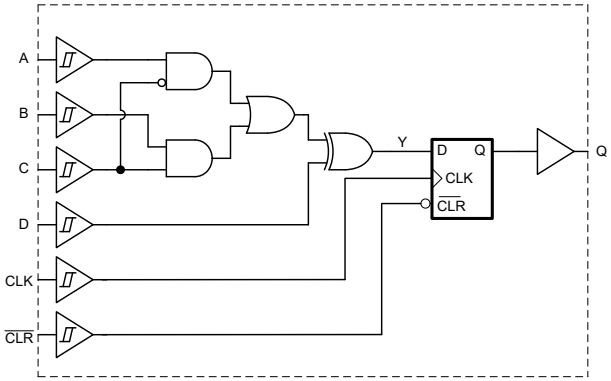


**Figure 1. Functional Block Diagram for the '100 D-Type Flip-Flop**

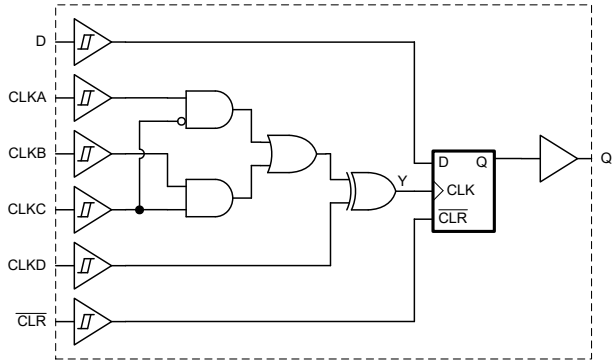


**Figure 2. Functional Block Diagram for the '101 D-Type Flip-Flop**

TI offers two variants of the D-Type flip-flop with configurable logic inputs. The '100 function includes the ultra-configurable '99 function at the data input, while the '101 function provides the same ultra-configurable '99 function but at the clock input instead. The configurable logic block for both the '100 and '101 function is the same, producing the Boolean logic Y = (A•$\overline{C}$+B•C)⊕D.

These flip-flops allow for integrating simple logic functions for either data or clock inputs as the application requires. The most common application for this type of logic is in the power sequencing of a device, as the configurable logic provides a wide variety of configurations for latching on a power supply under various conditions.

### Application: Software Controlled Latching Button

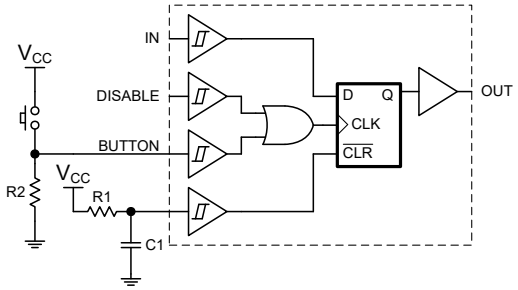


**Figure 3. Application Schematic**

In this application, we utilize the SN74AC2G101 to create a circuit that produces a latching button that can be state-selected and disabled by an internal signal. We configure the SN74AC2G101 to have a 2-input OR gate on the clock pin as shown in Figure 3. This configuration provides the ability to select the output state when the button is pressed through the IN signal, and the ability to disable the button through the DISABLE input. There are many configurations for this circuit, but in this case, the input was configured such that a high state at DISABLE prevents the button input from being detected.

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