LVT Family Characteristics

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TEXAS INSTRUMENTS

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Introduction

To address the need for a complete low-voltage interface solution, Texas Instruments has developed a new generation of logic devices capable of mixed-mode operation. The LVT series relies on a state-of-the-art submicron BiCMOS process to provide up to a 90% reduction in static power dissipation over ABT, as well as the following family characteristics:

5.5-V maximum input voltage

Specified 2.7-V to 3.6-V supply voltage

I/O structures that support live insertion

Standard TTL output drives of:
V_{OH} = 2 V at I_{OH} = –32 mA
V_{OL} = 0.55 V at I_{OL} = 64 mA

Rail-to-rail switching for driving CMOS

Maximum supply currents of:
$I_{CCL} \leq 15$ mA
$I_{CCH} \leq 200$ μA
$I_{CCZ} \leq 200$ μA

Propagation delays of:
$t_{pd} < 4.6$ ns
t_{pd} (LE to Q) < 5.1 ns
t_{pd} (CLK to Q) < 6.3 ns

Surface-mount packaging support including fine-pitch packages:
48-/56-pin SSOP and TSSOP for LVT Widebus™
20-/24-pin SOIC and TSSOP for standard LVT

LVT Input/Output Characteristics

Figure 1 shows a simplified LVT output and illustrates the mixed-mode-signal drive designed into the output stage. This combination of a high-drive TTL stage along with the rail-to-rail CMOS switching gives the LVT series of products extreme application flexibility. These parts have the same drive characteristics as 5-V ABT devices (see Figure 2), and provide the dc drive needed for existing 5-V backplanes. This allows for a simple solution to reduce system power via the migration to 3.3-V operation.

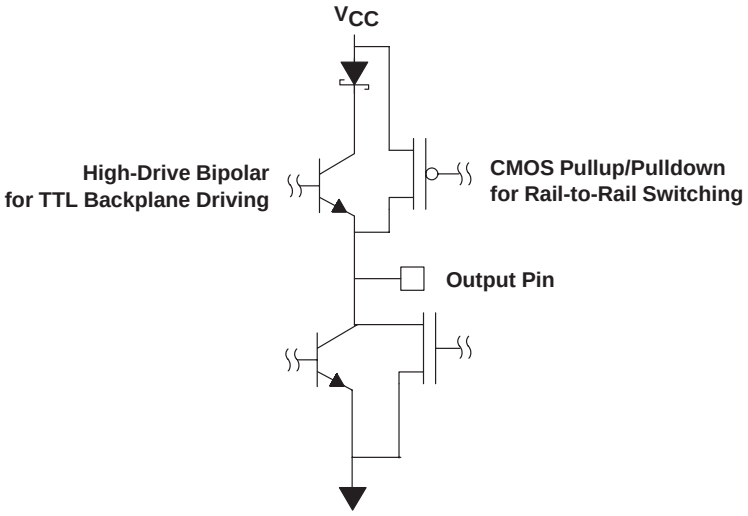


Figure 1. Simplified LVT Output Structure

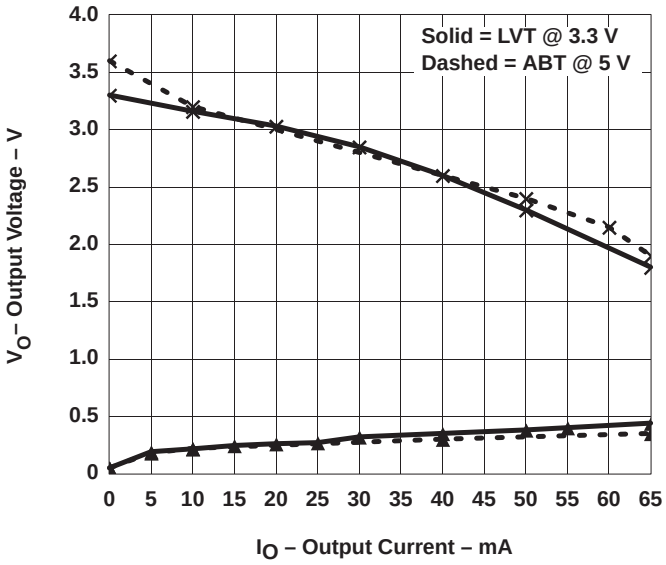


Figure 2. ABT Versus LVT Output-Drive Comparison

Not only can LVT devices operate as 3-V to 5-V level translators by supporting input or I/O voltages of 5.5 V with V_{CC} = 2.7 V to 3.6 V, the inputs can withstand 5.5 V even when V_{CC} = 0 V. This allows for the devices to be used under partial system power-down applications or those that require live insertion.

Bus Hold

Many times, devices are used in applications that do not provide a pullup or pulldown voltage to the input or I/O pin when the driving device goes into a high-impedance state, as in the case of CMOS buses or nonbused lines. To prevent application problems or oscillations, a large pullup resistor typically is used, but this consumes board area and contributes to driver loading. The LVT series of devices incorporates active circuitry that holds unused or floating inputs or I/Os at a valid logic level. This circuitry provides for a typical holding current, ± 100 μA, that is sufficient enough to overcome any CMOS-type leakages. Since this is an active circuit, it does take current, approximately ± 500 μA, to toggle the state of the input. This current is trivial when compared to the current that is needed to charge a capacitive load, thereby not affecting the propagation delay of the driving output.

Conclusion

LVT devices solve the system need for a transparent seam between the low-voltage and 5-V sections by providing for mixed-signal operation. The devices support live-insertion or partial-power applications, while providing for low-input leakage currents. The outputs can drive today's 5-V backplanes, with a considerable reduction in device power consumption, as well as being packaged in state-of-the-art, fine-pitch surface-mount packages.

’LVT244 Characteristics

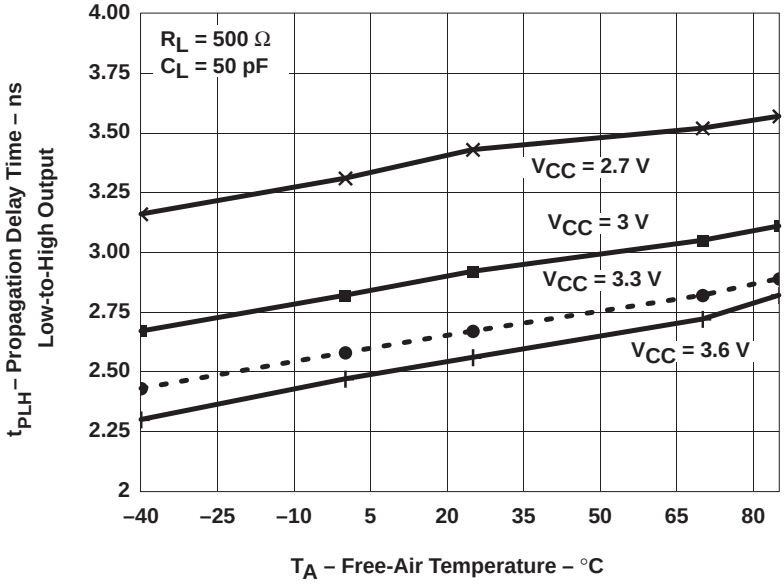


Figure 3. Propagation Delay (t_{PLH}) Versus Free-Air Temperature

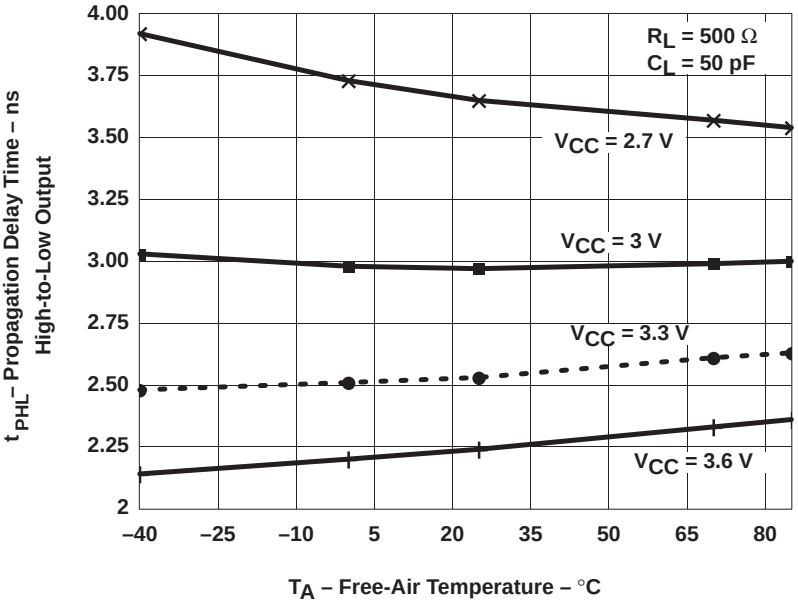


Figure 4. Propagation Delay (t_{PLH}) Versus Free-Air Temperature

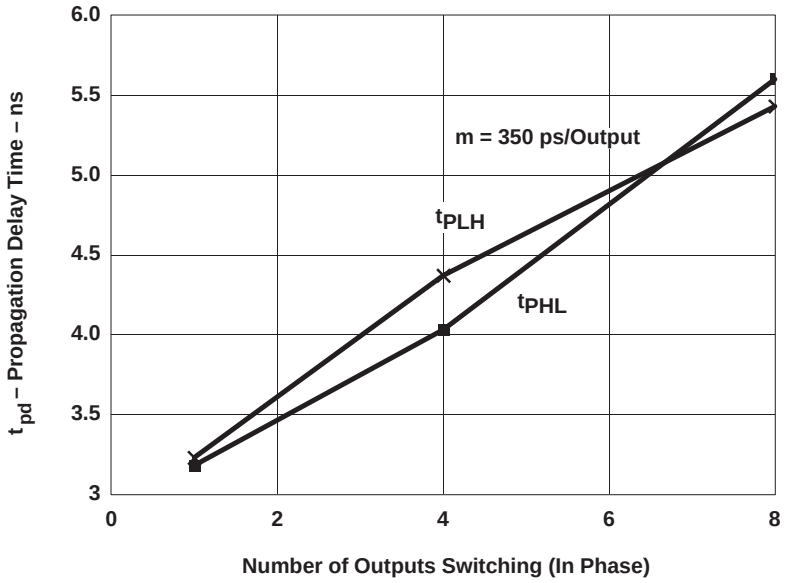


Figure 5. Propagation Delay Versus Outputs Switching

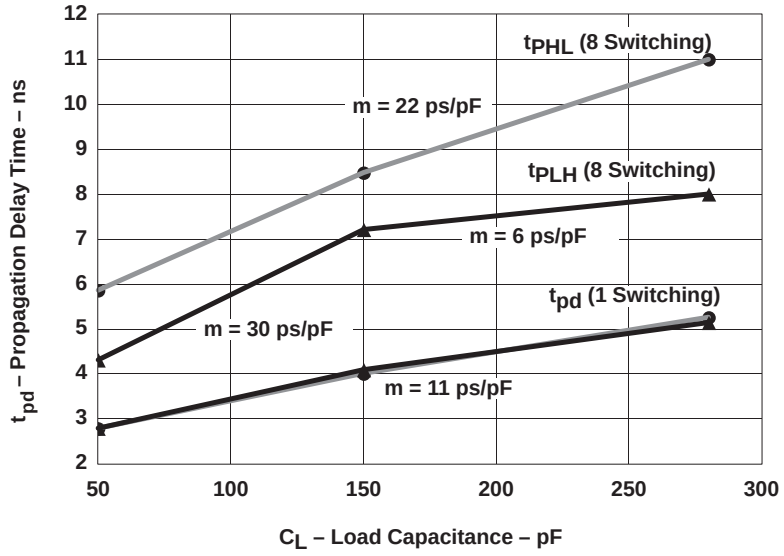


Figure 6. Propagation Delay Versus Load Capacitance

’LVT244 Typical dc Characteristics

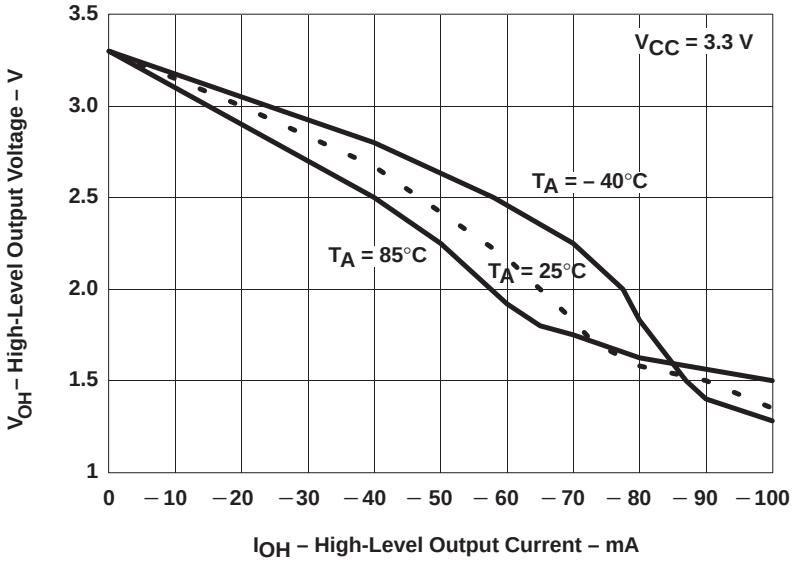


Figure 7. High-Level Output Voltage Versus High-Level Output Current, V_{CC} = 3.3 V

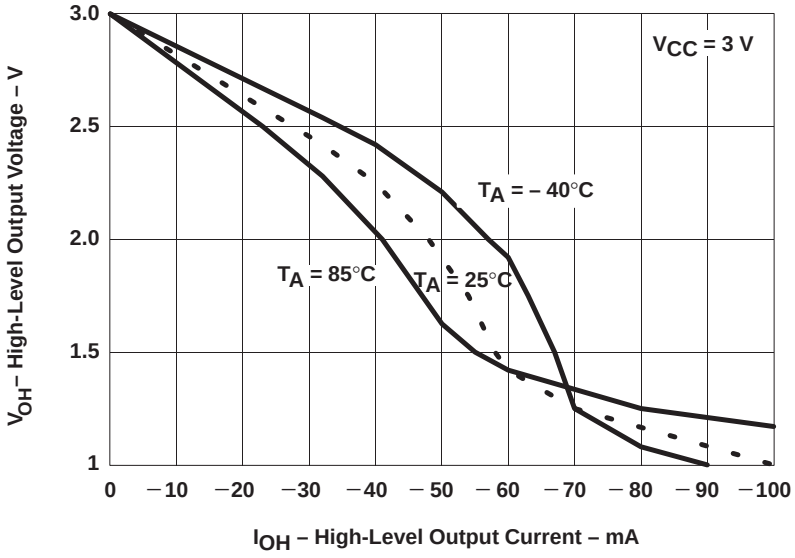


Figure 8. High-Level Output Voltage Versus High-Level Output Current, V_{CC} = 3 V

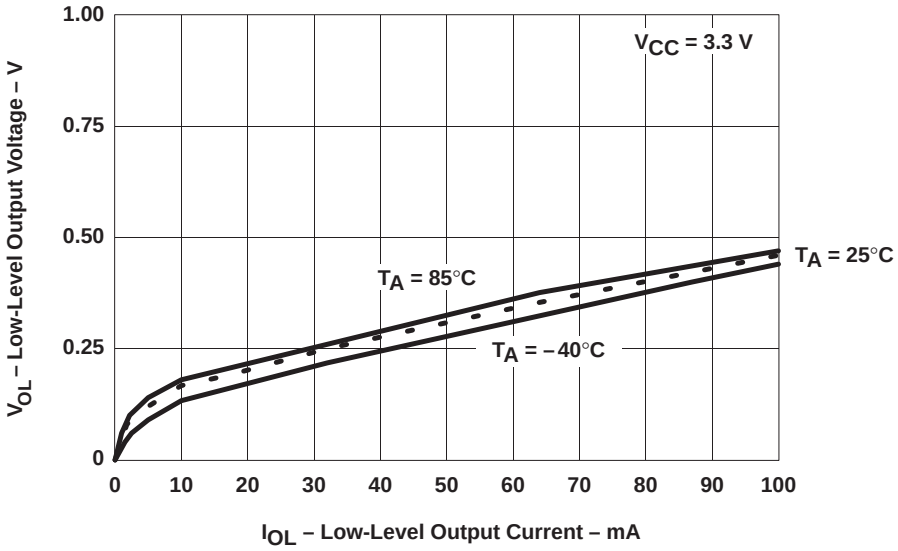


Figure 9. Low-Level Output Voltage Versus Low-Level Output Current

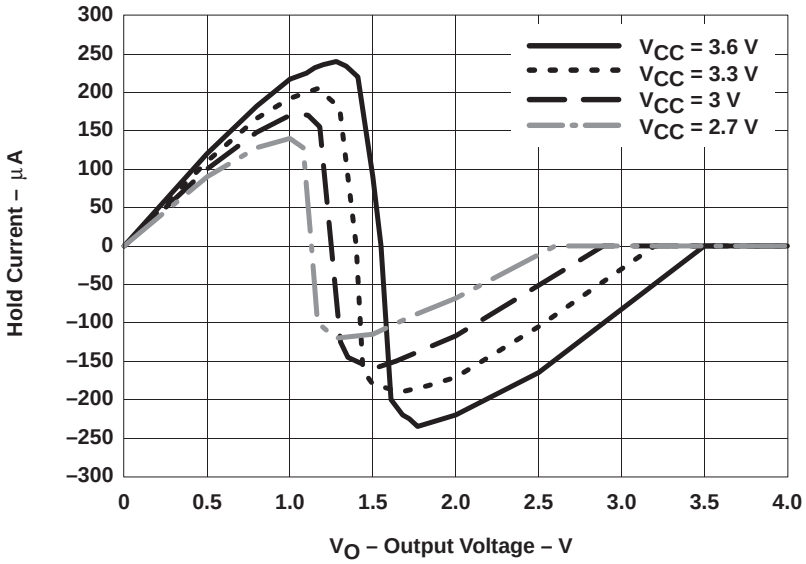


Figure 10. Hold Current Versus Output Voltage

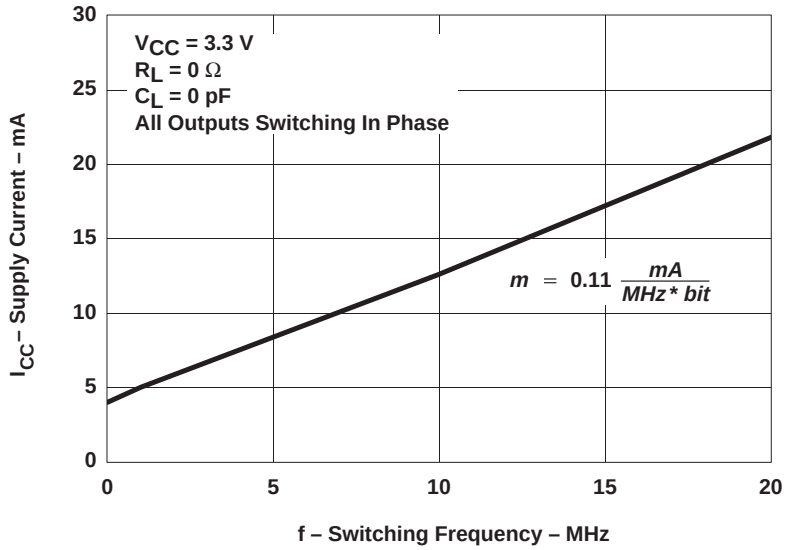


Figure 11. Supply Current Versus Switching Frequency

Unloaded t_r and t_f Rates

The circuit shown in Figure 12 was used to measure the unloaded transition rates of the output.

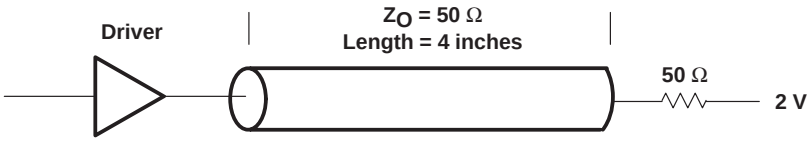


Figure 12. Load Circuit

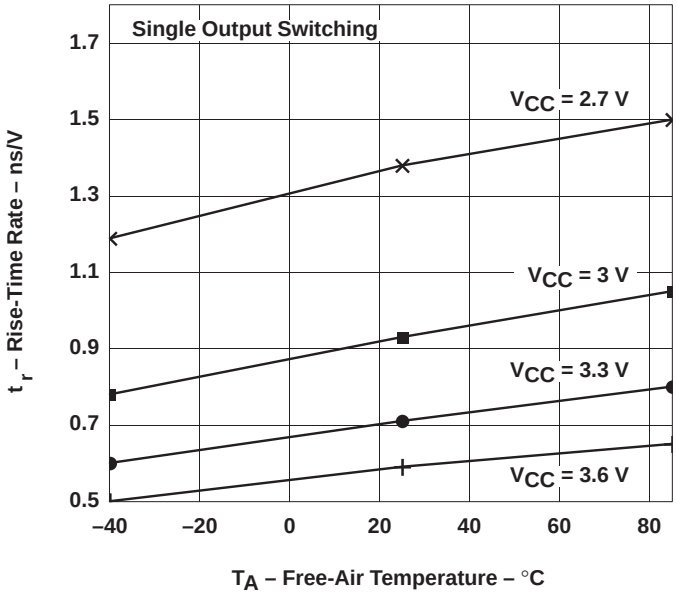


Figure 13. Rise-Time Rate Versus Free-Air Temperature, Single Output Switching

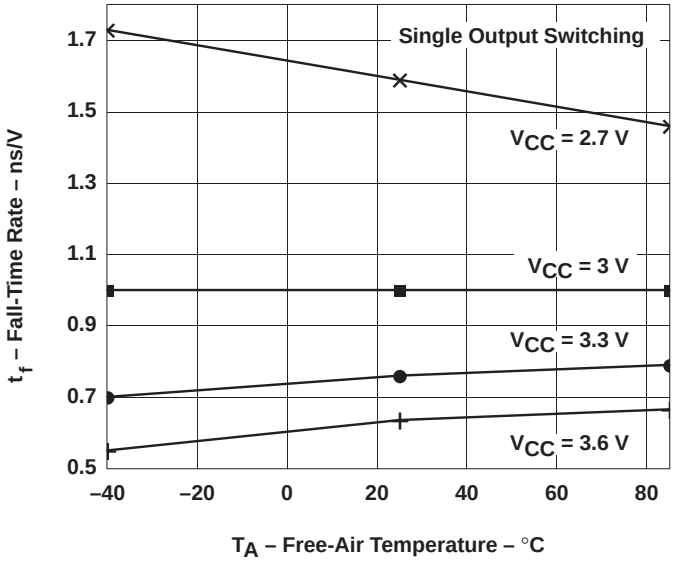


Figure 14. Fall-Time Rate Versus Free-Air Temperature, Single Output Switching

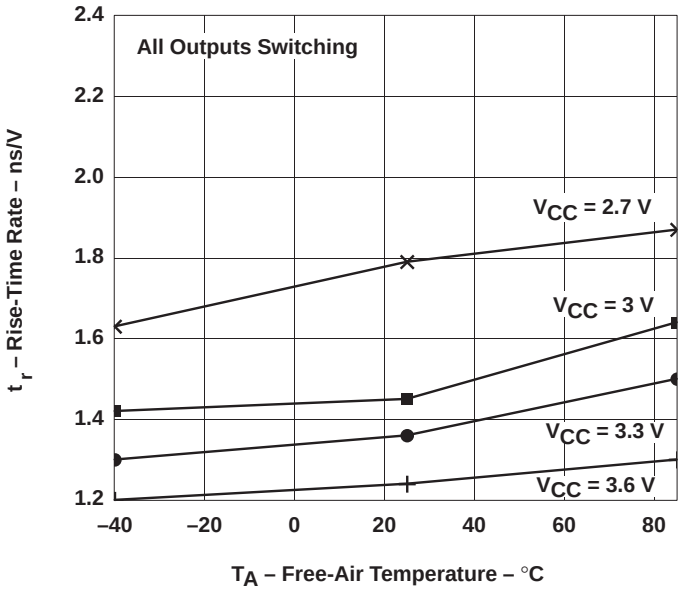


Figure 15. Rise-Time Rate Versus Free-Air Temperature, All Outputs Switching

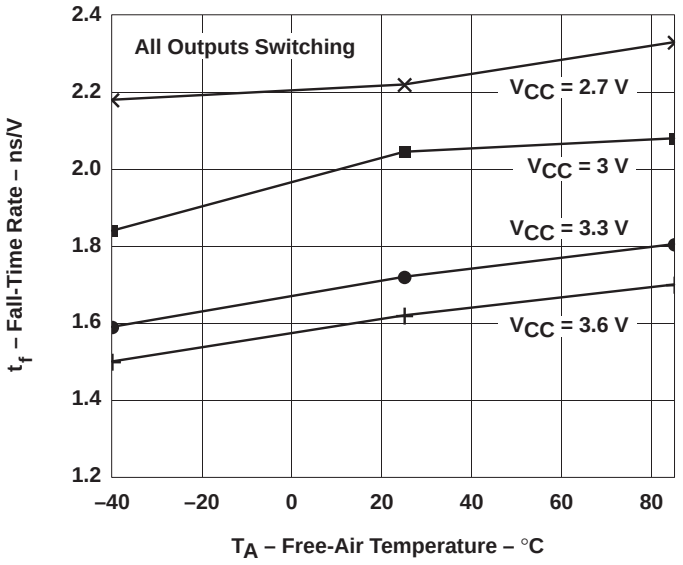


Figure 16. Fall-Time Rate Versus Free-Air Temperature, All Outputs Switching

’LVT646 Characteristics

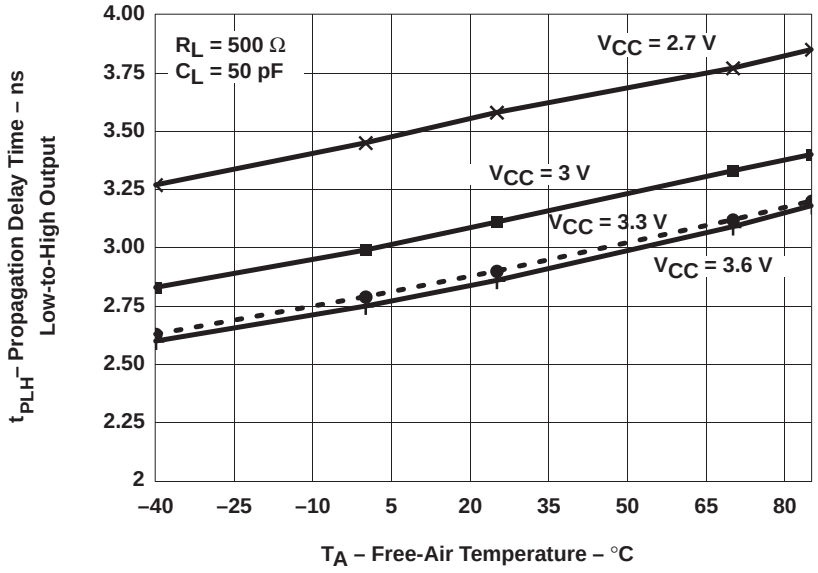


Figure 17. Through-Mode Propagation Delay (t_{PLH}) Versus Free-Air Temperature

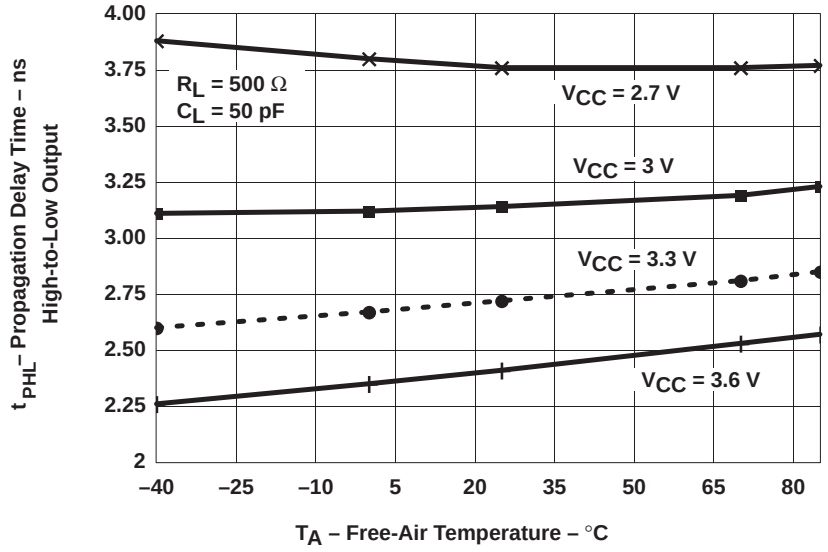


Figure 18. Through-Mode Propagation Delay (t_{PHL}) Versus Free-Air Temperature

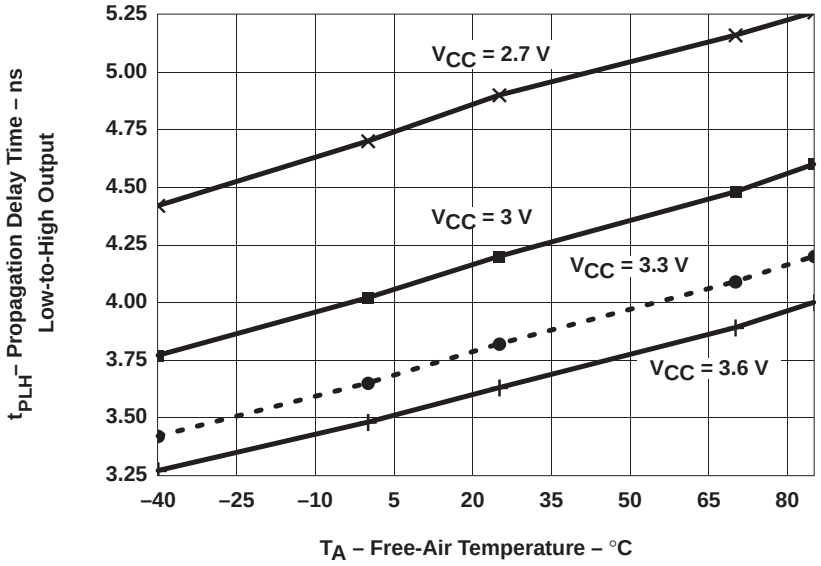


Figure 19. Clock-to-Q Propagation Delay (t_{PLH}) Versus Free-Air Temperature

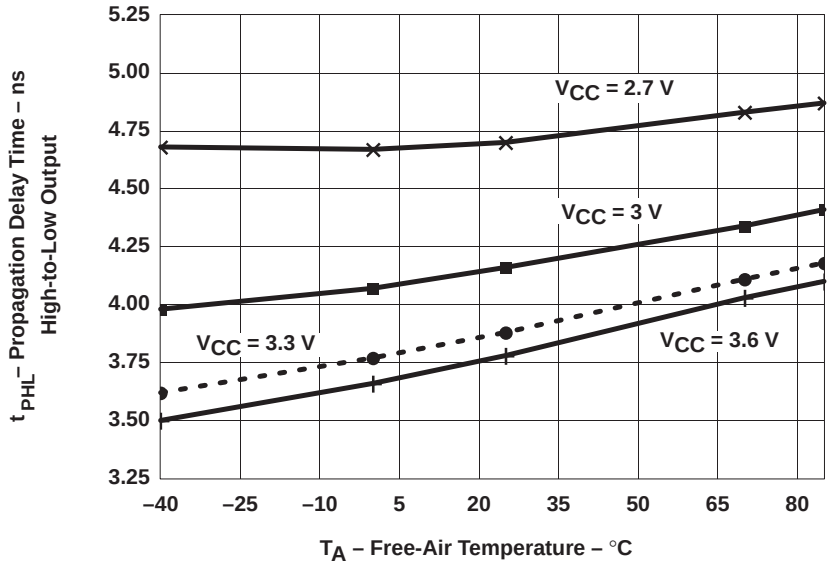


Figure 20. Clock-to-Q Propagation Delay (t_{PHL}) Versus Free-Air Temperature

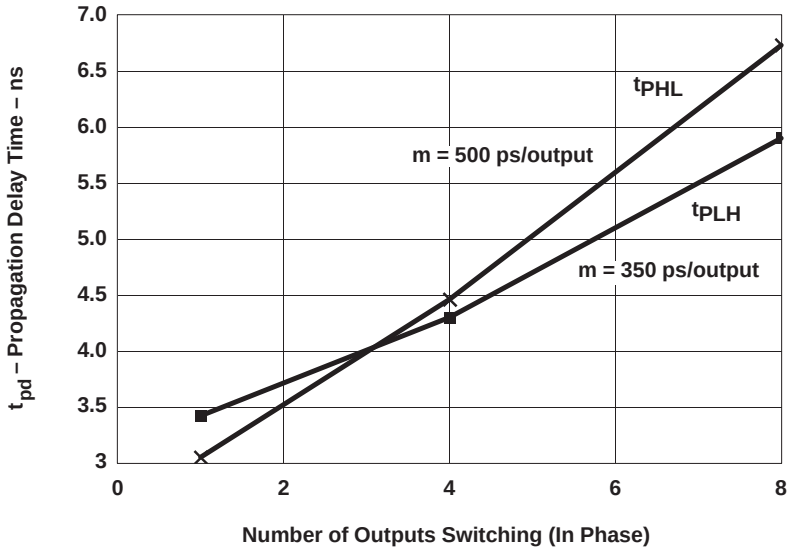


Figure 21. Propagation Delay Versus Outputs Switching

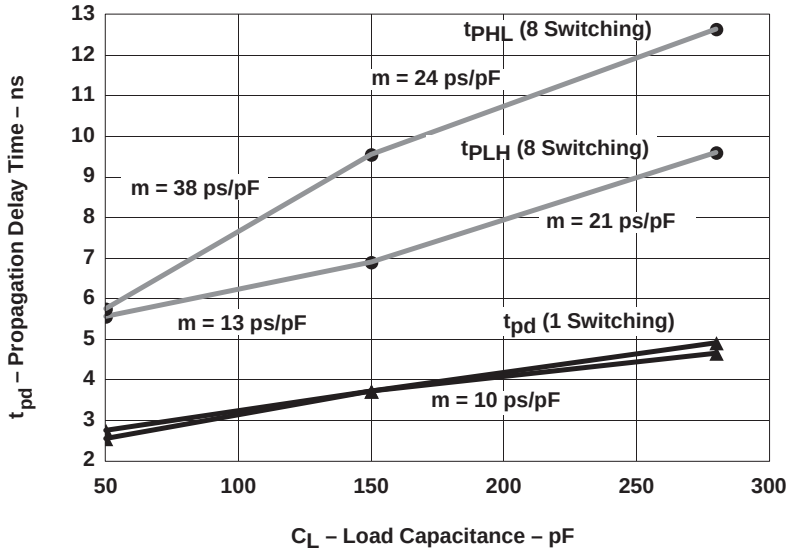
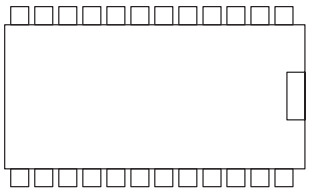


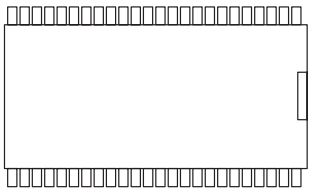
Figure 22. Propagation Delay Versus Load Capacitance

Packaging Options



24-Pin SOIC (DW)†
Area = 165 mm²
Height = 2.65 mm
Lead pitch = 1.27 mm

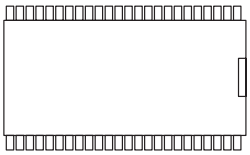
Widebus™



48-Pin SSOP (DL)†
Area = 171 mm²
Height = 2.74 mm
Lead pitch = 0.635 mm

24-Pin TSSOP (PW)†
Area = 54 mm²
Height = 1.1 mm
Lead Pitch = 0.65 mm

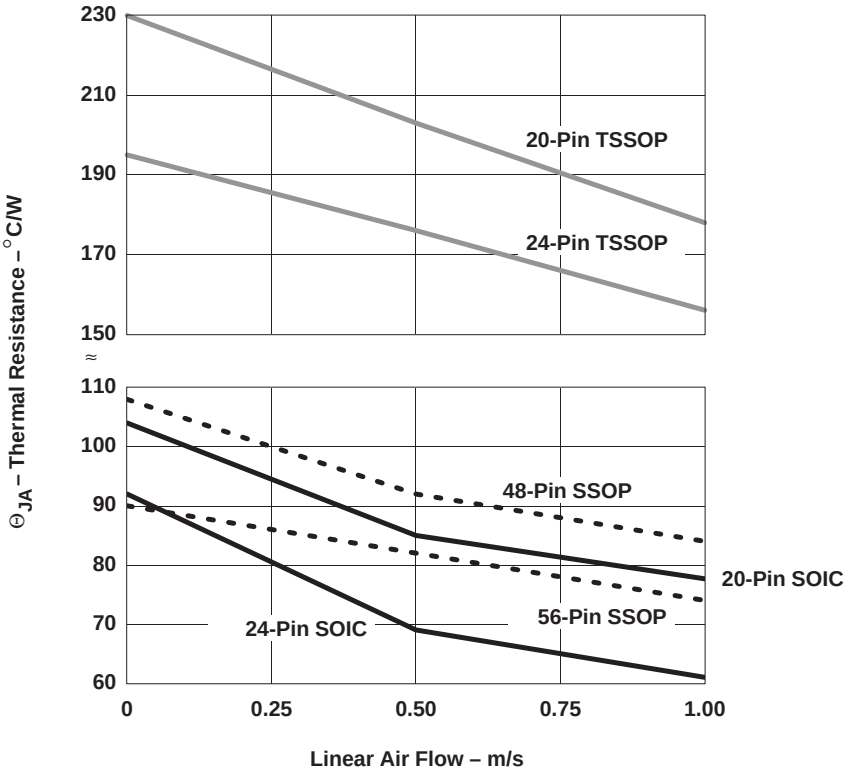
Shrink Widebus™



48-Pin TSSOP (DGG)†
Area = 108 mm²
Height = 1.1 mm
Lead Pitch = 0.5 mm

† TI package designators

Thermal Characteristics



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